Edited by Muhammad Rashid

POWER ELECTRONICS HANDBOOK

4th Edition



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Fourth Edition

Edited by

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1 Introduction

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1.1 Power Electronics Defined[1]

It has been said that people do not use electricity, but rather they use communication, light, mechanical work, entertainment, and all the tangible benefits of energy and electronics. In this sense, electrical engineering as a discipline is much involved in energy conversion and information. In the general world of electronics engineering, the circuits engineers design and use are intended to convert information. This is true of both analog and digital circuit design. In radio-frequency applications, energy and information are on more equal footing, but the main function of any circuit is information transfer.

What about the conversion and control of energy itself? Energy is a critical need in every human endeavor. The capabilities and flexibility of modern electronics must be brought to bear to meet the challenges of reliable, efficient energy. Electronic circuits and systems can be applied to the challenges of energy conversion and management. This is the framework of *power electronics*, a discipline defined in terms of *electrical energy conversion, applications*, and *electronic devices*. More specifically,

> **Definition** Power electronics involves the study of electronic circuits intended to control the flow of electrical energy. These circuits handle power flow at levels much higher than the individual device ratings.

Rectifiers are typical examples of circuits that meet this definition. Inverters (a general term for dc-ac converters) and dc-dc converters for power supplies are also common applications. As shown in Fig. 1.1, power electronics represents a median point at which the topics of energy systems, electronics, and control converge and combine [1]. Any useful circuit design for an energy application must address issues of devices, control, and systems, as well as of the energy itself. Among the unique aspects of power electronics are its emphasis on large semiconductor devices, the application of magnetic devices for energy storage, special control methods that must be applied to nonlinear systems, and its fundamental place as a central component of today's energy systems and alternative resources. In any study of electrical engineering, power electronics must be placed on a par with digital, analog, and radio-frequency electronics to reflect the distinctive design methods and unique challenges.

Applications of power electronics continue to expand. It is not possible to build practical computers, mobile phones,

[1] Portions of this chapter are taken from P. T. Krein, *Elements of Power Electronics*. New York: Oxford University Press, 1998. © 1998, Oxford University Press, used with permission.

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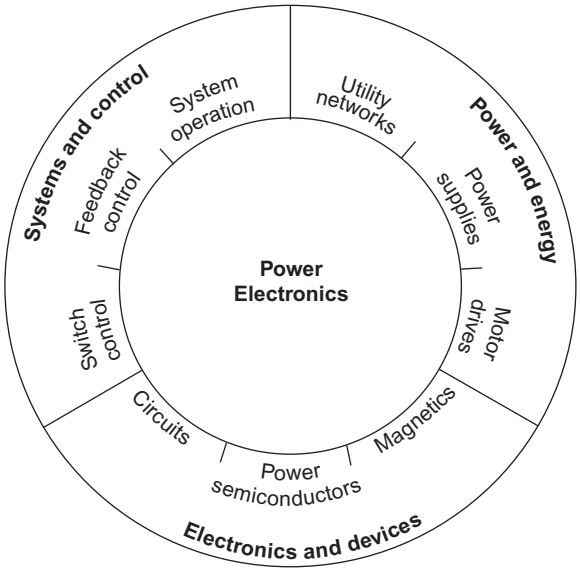


FIG. 1.1 Control, energy, and power electronics are interrelated.

handheld devices, cars, airplanes, industrial processes, and a host of other everyday products without power electronics. Alternative energy systems such as wind generators, solar power, fuel cells, and others require power electronics to function. Technology advances such as electric and hybrid transportation, laptop computers, microwave ovens, flat-panel displays, LED lighting, and hundreds of other innovations were not possible until advances in power electronics enabled their implementation. Although no one can predict the future, it is certain that power electronics will be at the heart of fundamental energy innovations.

The history of power electronics [2–5] has been closely allied with advances in electronic devices that provide the capability to handle high power levels. Since about 1990, devices have become so capable that a transition from a "device-driven" field to an "application-driven" field continues. This transition has been based on two factors: (1) Advanced semiconductors with suitable power ratings exist for almost every application of wide interest, and (2) the general push toward miniaturization is bringing advanced power electronics into a growing variety of products. Although the devices continue to improve, especially related to the use of wide bandgap semiconductor materials, their development generally tends to follow innovative applications.

1.2 Key Characteristics

All power electronic circuits manage the flow of electrical energy between an electrical source and a load. The parts in a circuit must direct electrical flows, not impede them. A general power conversion system is shown in Fig. 1.2. The power converter in the middle controls the energy flow between

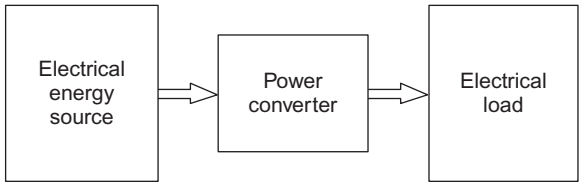


FIG. 1.2 General system for electric power conversion. (From P. T. Krein, Elements of Power Electronics, Oxford University Press, New York, 1998, Copyright 1998, Oxford University Press, used with permission.)

a source and a load. For our purposes, the power converter will be implemented with a power electronic circuit. Because a power converter appears between a source and a load, any energy used within the converter is lost to the overall system. A crucial point emerges: to build a power converter, we should consider only lossless components. A realistic converter design must approach 100% efficiency.

A power converter connected between a source and a load also affects system reliability. If the energy source is perfectly reliable (it is available all the time), then a failure in the converter affects the user (the load) just as if the energy source had failed. An unreliable power converter creates an unreliable system. To put this in perspective, consider that a typical American household loses electric power only a few minutes a year. Energy is available 99.999% of the time. A converter must be better than this to prevent system degradation. An ideal converter implementation will not suffer any failures over its application lifetime. Extreme high reliability can be a more difficult objective than high efficiency.

1.2.1 The Efficiency Objective—The Switch

A circuit element as simple as a light switch reminds us that the extreme requirements in power electronics are not especially novel. Ideally, when a switch is on, it has zero voltage drop and will carry any current imposed on it. When a switch is off, it blocks the flow of current regardless of the voltage across it. The *device power*, the product of the switch voltage and current, is identically zero at all times. A switch therefore controls energy flow with no loss. In addition, reliability is also high. Household light switches perform over decades of use and perhaps 100,000 operations. Unfortunately, a mechanical switch does not meet all practical needs. A switch in a power supply may function 100,000 times each second. Even the best mechanical switch will not last beyond a few million cycles. Semiconductor switches (without this limitation) are the devices of choice in power converters.

A circuit built from ideal switches will be lossless. As a result, switches are the main components of power converters, and many people equate power electronics with the study of switching power converters. Magnetic transformers and lossless storage elements such as capacitors and inductors are also

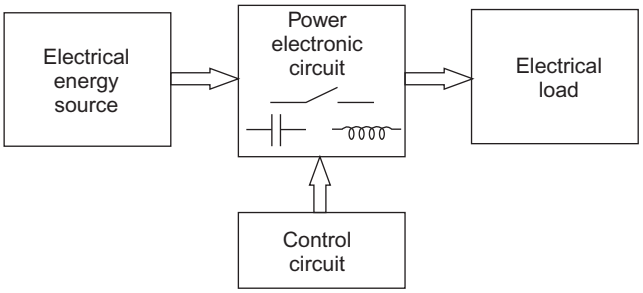


FIG. 1.3 A basic power electronic system. (From P. T. Krein, Elements of Power Electronics, Oxford University Press, New York, 1998, Copyright 1998, Oxford University Press, used with permission.)

valid components for use in power converters. The complete concept, shown in Fig. 1.3, represents a *power electronic system*. Such a system consists of an electrical energy source, an electrical load, a *power electronic circuit*, and a control function.

The power electronic circuit contains switches, lossless energy storage elements, and magnetic transformers. The controls take information from the source, the load, and the designer and then determine how the switches operate to achieve the desired conversion. The controls are built up with low-power analog and digital electronics.

Switching devices are selected based on their *power handling* rating—the product of their voltage and current ratings—rather than on power dissipation ratings. This contrasts with other applications of electronics, in which power dissipation ratings dominate. For instance, a typical stereo receiver performs a conversion from ac line input to audio output. Many audio amplifiers do not use the techniques of power electronics, and the semiconductor devices do not act as switches. A commercial 100 W amplifier, using a class A, B, or AB design, usually employs transistors big enough to dissipate the full 100 W, and the circuit is likely to be <10% energy efficient in normal use. In contrast, *switching amplifiers,* class D, E, or F, use the techniques of power electronics. They provide dramatic efficiency improvements. A home theater system implemented with switching amplifiers can exceed 90% energy efficiency in a small package. The amplifiers can even be packed inside the loudspeakers.

Switches can reach extreme power levels, far beyond what might be expected for a given size. Consider the following examples:

Example 1.1 The NTP30N20 is a metal-oxide-semiconductor field-effect transistor (MOSFET) with a drain current rating of 30 A, a maximum drain-source breakdown voltage of 200 V, and a rated power dissipation of up to 200 W under ideal conditions. Without a heat sink, however, the device can tolerate no more than 2.5 W of dissipation. For power electronics purposes, the power handling rating is $30\ \text{A} \times 200\ \text{V} = 6\ \text{kW}$. Several manufacturers have developed controllers for domestic refrigerators, air conditioners, and high-end machine tools based on this and similar devices. The second part of the definition of power electronics in Section 1.1 points out that the circuits handle power at levels much higher than that of the ratings of individual devices. Here, a device is used to handle 6000 W—compared with its individual rating of no more than 200 W. The ratio 30:1 is high, but not unusual in power electronics contexts. In contrast, the same ratio in a "linear" audio amplifier is close to unity.

Example 1.2 The IGW60T120 is an insulated-gate bipolar transistor (IGBT)—a relative of the bipolar transistor that has been developed specifically for power electronics—rated for 1200 V and 60 A. Its power handling rating is 72 kW that is sufficient for a set of them to control an electric or hybrid car.

1.2.2 The Reliability Objective—Simplicity and Integration

High-power applications lead to interesting issues. In an inverter, the semiconductors often manipulate 30 times their power dissipation capability or more, which implies that only about 3% of the power being controlled is lost. A small design error, unexpected thermal problem, or minor change in layout could alter this somewhat. For instance, if the loss turns out to be 4% rather than 3%, the device stresses are 33% higher, and quick failure is likely to occur. The first issue for reliability in power electronic circuits is to keep device voltage, current, and power dissipation levels well within rating limits. This is challenging when power handling levels are high.

The second issue for reliability is simplicity. It is well established in electronics design that the more parts there are in a system, the more likely it is to fail. Power electronic circuits tend to have few parts, especially in the main energy flow paths. Necessary operations must be carried out through shrewd use of these parts. Often, this means that sophisticated control strategies are applied to seemingly simple conversion circuits.

The third issue for reliability is integration. One way to avoid the reliability-complexity trade-off is to integrate multiple components and functions together. A microprocessor, for example, might contain millions of gates. All interconnections and signals flow within a single chip, and the reliability is nearly that of a single part. Integrated power electronic modules [6] achieve this. Manufacturers package multiple switching devices, with their interconnections and protection components, together as a unit. Control circuits for converters are also integrated as much as possible to keep the reliability high. The package itself is a factor in reliability, and one that is a subject of active research. Many semiconductor packages include small bonding wires that can be susceptible to thermal or vibration damage. The small geometries also tend to enhance electromagnetic interference among the internal circuit components.

1.3 Trends in Power Supplies

Two distinct trends drive electronic power supplies, one of the major classes of power electronic circuits. At the high end, microprocessors, memory chips, and other advanced digital circuits require increasing power levels and increasing performance at very low voltage. It is a challenge to deliver 100 A or more efficiently at voltages that can be less than 1 V. These types of power supplies are expected to deliver precise voltages, even though the load can change by an order of magnitude in nanoseconds.

At the other end are portable devices with rechargeable batteries. The power supplies for these devices and for other consumer products must be cheap and efficient. It is increasingly important to use the best possible power electronics design techniques for these supplies to save energy while minimizing costs and matching many different global standards. Efficiency standards such as the Energy Star program place stringent requirements on a wide range of low-end power supplies.

In the past, bulky "linear" power supplies were designed with transformers and rectifiers from the ac line frequency to provide dc voltages for electronic circuits. In a well-designed power electronic system today, called a *switch-mode power supply*, an ac source from a wall outlet (which could be nearly anywhere in the world) is rectified without direct transformation. The resulting high dc voltage is converted through a dc-dc converter to the 1, 3, 5, and 12 V or other levels required. A personal computer commonly requires multiple 3.3 and 5 V supplies, 12 V supplies, additional levels, and a separate converter for 1 V delivery to the microprocessor. This is in addition to supplies for the video display or peripheral devices. Only a switch-mode supply can support such complex requirements with acceptable costs.

Switch-mode supplies often take advantage of MOSFET semiconductor technology. Trends toward high reliability, low cost, and miniaturization have reached the point where a 5 V power supply sold today might last more than 1,000,000 h (more than a century), provide 100 W of output in a package with volume no more than 15 cm^3, and sell for a price less than US$ 0.10/W. This type of supply brings an interesting dilemma: the ac line cord to plug it in takes up more space than the power supply itself. Innovative concepts such as integrating a power supply within a connection cable or using a block the size of a typical plug are becoming common.

Device technology for power supplies is being driven by expanding needs in the automotive and telecommunication industries and in markets for portable equipment. Power conversion for transportation must be cost effective yet rugged enough to survive the high vibration and wide temperature range to which a truck or passenger car is exposed. Global communication is possible only when sophisticated equipment can be used almost anywhere. Electricity supplies are neither reliable nor consistent throughout much of the world. Although voltage swings in the domestic ac supply in North America are often ±5% around a nominal value, in many developing nations, the swing can be ±25%—when power is available. Power converters for communications equipment must tolerate these swings and must also be able to make use of a wide range of possible backup sources. Designers are challenged to obtain maximum performance from small batteries and to create equipment with minimal energy requirements with power supplies that can operate anywhere in the world.

1.4 Conversion Examples

1.4.1 Single-Switch Circuits

Electrical energy sources take the form of dc voltage sources at various values, sinusoidal ac sources and polyphase sources, among others. A power electronic circuit might be asked to transfer energy between two different dc voltage levels, between an ac source and a dc load or between sources at different frequencies. It might be used to adjust an output voltage or power level, drive a nonlinear load, or control a load current. In this section, a few basic converter arrangements are introduced, and energy conservation provides a tool for analysis.

Example 1.3 Consider the circuit shown in Fig. 1.4. It contains an ac source, a switch, and a resistive load. It is a simple power electronic system.

Let us assign a (somewhat arbitrary) control scheme to the switch. What if the switch is turned on whenever $V_{ac} > 0$ and turned off otherwise? The input and output voltage waveforms are shown in Fig. 1.5. The input has a time average of 0 and root-mean-square (RMS) value equal to $V_{peak}/\sqrt{2}$,

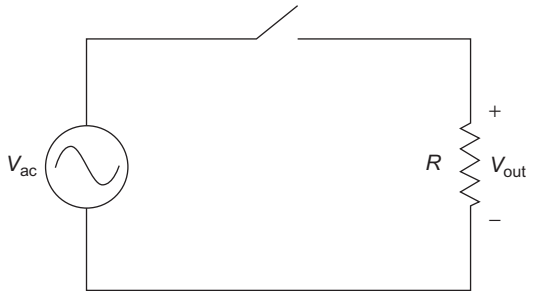


FIG. 1.4 A simple power electronic system. (From P. T. Krein, Elements of Power Electronics, Oxford University Press, New York, 1998, Copyright 1998, Oxford University Press, used with permission.)

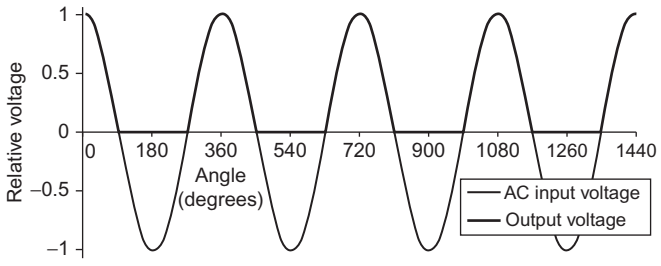


FIG. 1.5 Input and output waveforms for Example 1.5.

where V_{peak} is the maximum value of V_{ac}. The output has a nonzero average value given by

$$\langle v_{out}(t)\rangle = \frac{1}{2\pi}\left(\int_{-\pi/2}^{\pi/2} V_{peak}\cos\theta\,d\theta + \int_{\pi/2}^{3\pi/2} 0\,d\theta\right) = \frac{V_{peak}}{\pi} = 0.3183\,V_{peak} \tag{1.1}$$

and an RMS value equal to $V_{peak}/2$. Since the output has nonzero dc voltage content, the circuit can be used as an ac-dc converter. To make it more useful, a low-pass filter would be added between the output and the load to smooth out the ac portion. This filter needs to be lossless and will be constructed from only inductors and capacitors.

The circuit in Example 1.3 acts as a half-wave rectifier with a resistive load. With the hypothesized switch action, a diode can substitute for the ideal switch. The example confirms that a simple switching circuit can perform power conversion functions. But note that a diode is not, in general, the same as an ideal switch. A diode places restrictions on the current direction, but a true switch would not. An ideal switch allows control over whether it is on or off. In contrast, a diode's operation is constrained by circuit variables.

Consider a second half-wave circuit, now with a series $L-R$ load, shown in Fig. 1.6:

Example 1.4 A series diode $L-R$ circuit has ac voltage source input. This circuit operates much differently than the half-wave rectifier with resistive load. A diode will be on if forward-biased and off if reverse-biased. In this circuit, when the diode is off, the current will be zero. Whenever the diode is on, the circuit is the ac source with $L-R$ load. Let the ac voltage be $V_0\cos(\omega t)$. From Kirchhoff's voltage law (KVL),

$$V_0\cos(\omega t) = L\frac{di}{dt} + Ri.$$

Let us assume that the diode is initially off (this assumption is arbitrary, and we will check it as the example is solved). If the diode is off, the diode current is $i=0$, and the voltage across the diode will be v_{ac}. The diode will become forward-biased when v_{ac} becomes positive, so it will turn on when the input voltage makes a zero crossing in the positive direction. This allows us to establish initial conditions for the circuit, $i(t_0)=0, t_0=-\pi/(2\omega)$. The differential equation can be solved in a conventional way to give

$$i(t) = V_0\left[\frac{\omega L}{R^2+\omega^2L^2}\exp\left(\frac{-t}{\tau}-\frac{\pi}{2\omega\tau}\right) + \frac{R}{R^2+\omega^2L^2}\cos(\omega t) + \frac{\omega L}{R^2+\omega^2L^2}\sin(\omega t)\right] \tag{1.2}$$

where τ is the time constant L/R. What about when the diode is turned off? The first guess might be that the diode turns off when the voltage becomes negative, which is not correct. From the solution, we can determine that the current is not zero when the voltage first becomes negative. If the switch attempts to turn off, it must instantly drop the inductor current to zero. The derivative of current in the inductor, di/dt, would become negative infinite. The inductor voltage $L(di/dt)$ similarly becomes negative infinite, and the devices are destroyed. What really happens is that the falling current allows the inductor to maintain forward bias on the diode. The diode will turn off only when the *current* reaches zero. A diode has definite properties that determine the circuit action, and both the voltage and current are relevant. Fig. 1.7 shows the input and output waveforms for a time constant τ equal to about one-third of the ac waveform period.

1.4.2 The Method of Energy Balance

Any circuit must satisfy conservation of energy. In a lossless power electronic circuit, energy is delivered from source to load, possibly through an intermediate storage step. The energy flow must balance over time such that the energy drawn from the source matches that delivered to the load. The converter in Fig. 1.8 serves as an example of how the method of energy balance can be used to analyze circuit operation.

Example 1.5 The switches in the circuit of Fig. 1.8 are controlled cyclically to operate in alternation: when the

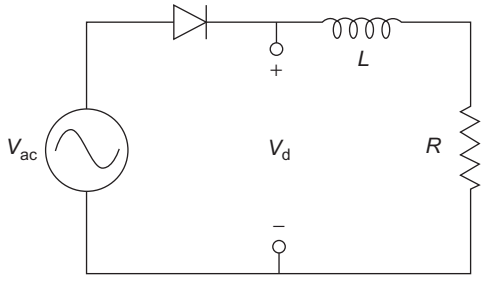


FIG. 1.6 Half-wave rectifier with $L-R$ load for Example 1.5.

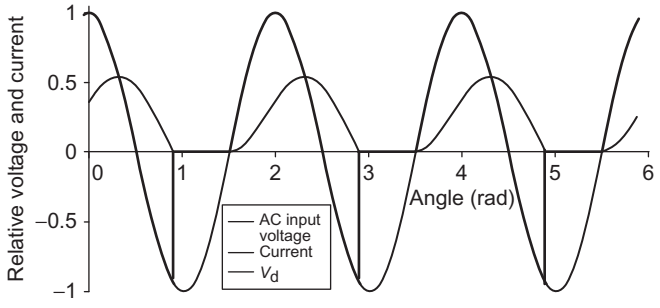


FIG. 1.7 Input and output waveforms for Example 1.5.

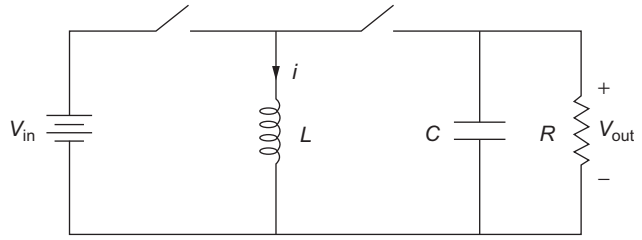


FIG. 1.8 Energy transfer switching circuit for Example 1.5. (From P. T. Krein, Elements of Power Electronics, Oxford University Press, New York, 1998, Copyright 1998, Oxford University Press, Inc., used with permission.)

left switch is on, the right switch is off and so on. What does the circuit do if each switch operates half the time? The inductor and capacitor have large values.

When the left switch is on, the source voltage V_{in} appears across the inductor. When the right switch is on, the output voltage V_{out} appears across the inductor. If this circuit is to be viewed as a useful converter, the inductor should receive energy from the source and then deliver it to the load without loss. Over time, this means that energy does not build up in the inductor, but instead flows through on average. The power into the inductor, therefore, must equal the power out, at least over a cycle. Therefore, the *average* power in must equal the *average* power out of the inductor. Let us denote the inductor current as i. The input is a constant voltage source. Because L is large, this constant voltage source will not be able to change the inductor current quickly, and we can assume that the inductor current is also constant. The average power into L over the cycle period T is

$$P_{in} = \frac{1}{T}\int_0^{T/2} V_{in} i \, dt = \frac{V_{in} i}{2}. \tag{1.3}$$

For the average power out of L, we must be careful about current directions. The current *out* of the inductor will have a value $-i$. The average output power is

$$P_{out} = \frac{1}{T}\int_{T/2}^{T} -i V_{out} \, dt = -\frac{V_{out} i}{2} \tag{1.4}$$

For this circuit to be viewed useful as a converter, the net energy should flow from the source to the load over time. The power conservation relationship $P_{in} = P_{out}$ requires that $V_{out} = -V_{in}$.

The method of energy balance shows that, when operated as described in the example, the circuit shown in Fig. 1.8 serves as a polarity reverser. The output voltage magnitude is the same as that of the input, but the output polarity is negative with respect to the reference node. The circuit is often used to generate a negative supply for analog circuits and other applications from a single positive input source. Other output voltage magnitudes can be achieved at the output if the switches alternate at unequal times.

If the inductor in the polarity reversal circuit is moved instead to the input, a step-up function is obtained. Consider the circuit shown in Fig. 1.9 in the following example.

Example 1.6 The switches shown in Fig. 1.9 are controlled cyclically in alternation. The left switch is on for two-thirds of each cycle and the right switch for the remaining one-third of each cycle. Determine the relationship between V_{in} and V_{out}. The inductor's energy should not build up when the circuit is operating normally as a converter.

A power balance calculation can be used to relate the input and output voltages. Let i be the inductor current. When the left switch is on, power is injected into the inductor. Its average value is

$$P_{in} = \frac{1}{T}\int_0^{2T/3} V_{in} i \, dt = \frac{2V_{in} i}{3}. \tag{1.5}$$

Power leaves the inductor when the right switch is on. Care must be taken with respect to polarities, and the current should be set negative to represent output power. The result is

$$P_{out} = \frac{1}{T}\int_{2T/3}^{T} -(V_{in} - V_{out}) i \, dt = -\frac{V_{in} i}{3} + \frac{V_{out} i}{3}. \tag{1.6}$$

When the input and output power are equated,

$$\frac{2V_{in} i}{3} = -\frac{V_{in} i}{3} + \frac{V_{out} i}{3}, \quad \text{and} \quad 3V_{in} = V_{out} \tag{1.7}$$

and the output voltage is found to be triple the input. Many seasoned engineers find the dc-dc step-up function shown in Fig. 1.9 to be surprising. It is just one example of such action, though. Others (including flyback circuits related to Fig. 1.8) are used in systems ranging from controlled power supplies to spark ignitions for automobiles.

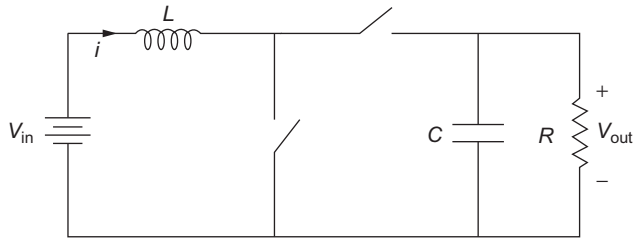


FIG. 1.9 Switching converter Example 1.6. (From P. T. Krein, Elements of Power Electronics, Oxford University Press, New York, 1998, Copyright 1998, Oxford University Press, used with permission.)

The circuits in the preceding examples have few components, provide useful conversion functions, and are efficient. If the switching devices are ideal, each circuit is lossless. Over the history of power electronics, development has tended to flow around the discovery of such circuits: a circuit with a particular conversion function is discovered, analyzed, and applied. As the circuit moves from laboratory testing to a complete commercial product, control and protection functions are added. The power portion of the circuit remains close to the original idea. The natural question arises as to whether a systematic approach to conversion is possible: can we start with a desired function and design an appropriate converter, rather than starting from the converter and working backward toward the application? What underlying principles can be applied to design and analysis? In this chapter, a few of the key concepts are introduced. Note that, although many of the circuits look deceptively simple, all these circuits are nonlinear systems with unusual behavior.

1.5 Tools for Analysis and Design

1.5.1 The Switch Matrix

The most readily apparent difference between a power electronic circuit and other types of electronic circuits is the switch action. In contrast to a digital circuit, the switches do not indicate a logic level. Control is effected by determining the times at which switches should operate. Whether there is just one switch or a large group, there is a complexity limit: if a converter has m inputs and n outputs, even the densest possible collection of switches would have a single switch between each input and output line. The $m \times n$ switches in the circuit can be arranged according to their connections. The pattern suggests a matrix, as shown in Fig. 1.10.

Power electronic circuits fall into two broad classes [2]:

1. Direct switch matrix circuits. In these circuits, energy storage elements are connected to the matrix only at the input and output terminals. The storage elements effectively become part of the source or the load. In the literature, ac-ac versions of these circuits are sometimes called *matrix converters.*
2. Indirect switch matrix circuits, also termed *embedded* converters. These circuits, like the polarity-reverser example, have energy storage elements connected *within* the matrix structure. Indirect switch matrix circuits are most commonly analyzed as a cascade connection of direct switch matrix circuits with storage in between.

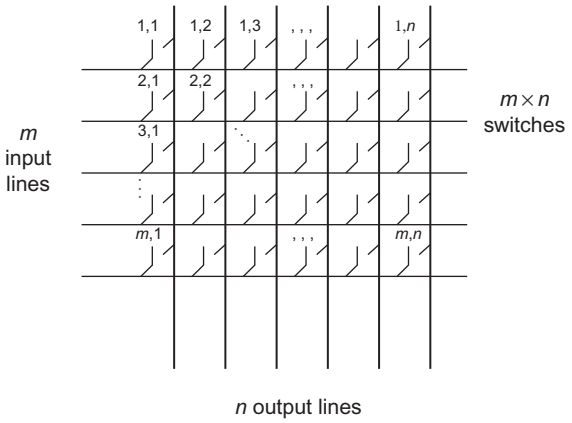


FIG. 1.10 The general switch matrix.

The switch matrices in realistic applications are small. A 2×2 switch matrix, for example, covers all possible cases with a single-port input source and a two-terminal load. The matrix is commonly drawn as the *H-bridge* shown in Fig. 1.11. A three-phase bridge rectifier is shown in Fig. 1.12. There are three possible inputs, and the two terminals of the dc circuit provide outputs, which gives a 3×2 switch matrix. In a computer power supply with five separate dc loads, the switch matrix could be 2×10. Very few practical converters have more than 24 switches, and most designs use fewer than 12.

A switch matrix provides a way to organize devices for a given application. It also helps us focus on three major task

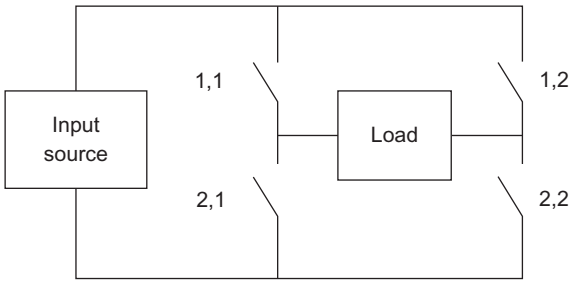


FIG. 1.11 H-bridge configuration of a 2×2 switch matrix.

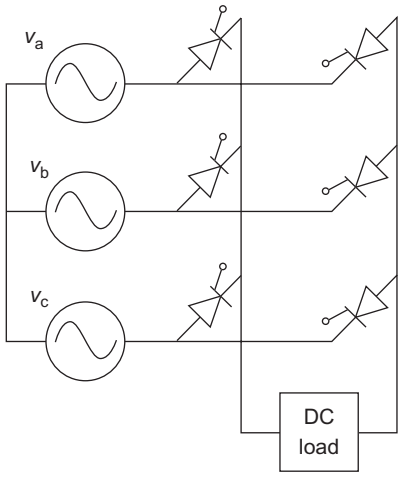


FIG. 1.12 Three-phase bridge rectifier circuit, a 3×2 switch matrix.

areas, which must be addressed individually and effectively in order to produce a useful power electronic system:

- The "hardware" task—Build a switch matrix. This involves the selection of appropriate semiconductor switches and the auxiliary elements that drive and protect them.
- The "software" task—Operate the matrix to achieve the desired conversion. All operational decisions are implemented by adjusting switch timing.
- The "interface" task—Add energy storage elements to provide the filters or intermediate storage necessary to meet the application requirements. Lossless filters with simple structures are required.

In a rectifier or other converter, we must choose the electronic parts, how to operate them, and how best to filter the output to satisfy the needs of the load.

1.5.2 Implications of Kirchhoff's Voltage and Current Laws

A major challenge of switch circuits is their capacity to "violate" circuit laws. First, consider the simple circuits shown in Fig. 1.13. We might try the circuit shown in Fig. 1.13A for ac-dc conversion, but there is a problem. According to Kirchhoff's voltage law (KVL), the "sum of voltage drops around a closed loop is zero." However, with the switch closed, the sum of voltages around the loop is not zero. In reality, this is not a valid result. Instead, a very large current will flow and cause a large $I \cdot R$ drop in the wires. KVL *will* be satisfied by the wire voltage drop, but a fire or, better yet, fuse action, might result. There is, however, nothing that would prevent an operator from trying to close the switch. KVL, then, implies a crucial restriction: a switch matrix must not attempt to interconnect unequal voltage sources directly. Notice that a wire or dead short can be thought of as a voltage source with $V = 0$, so KVL is a generalization of avoiding shorts across an individual voltage source.

A similar constraint holds for Kirchhoff's current law (KCL) that states that "currents into a node must sum to zero." When current sources are present in a converter, we must avoid any attempts to violate KCL. In Fig. 1.13B, if the current sources are different and if the switch is opened, the sum of the currents into the node will not be zero. In a real circuit, high voltages will build up and cause an arc to create another current path. This situation has real potential for damage, and a fuse will not help. As a result, KCL implies the restriction that a switch matrix must not attempt to interconnect unequal current sources directly. An open circuit can be thought of as a current source with $I = 0$, so KCL applies to the problem of opening an individual current source.

In contrast to conventional circuits, in which KVL and KCL are automatically satisfied, switches do not "know" KVL or KCL. If a designer forgets to check and accidentally shorts two voltages or breaks a current source connection, some problem or damage will result. KVL and KCL place necessary constraints on the operation of a switch matrix. In the case of voltage sources, switches must not act to create short-circuit paths among unlike sources. In the case of KCL, switches must act to provide a path for currents. These constraints drastically reduce the number of valid switch-operating conditions in a switch matrix, thereby leading to manageable operating design problems.

When energy storage is included, there are interesting implications of the circuit law restrictions. Fig. 1.14 shows two "circuit law problems." In Fig. 1.14A, the voltage source will cause the inductor current to ramp up indefinitely, since $V = L\mathrm{d}i/\mathrm{d}t$. We might consider this to be a "KVL problem" because the long-term effect is similar to shorting the source. In Fig. 1.14B, the current source will cause the capacitor voltage to ramp toward infinity. This causes a "KCL problem"; eventually, an arc will be formed to create an additional current path, just as if the current source had been opened. However, these connections are not problematic if they are only temporary. It should be evident that an inductor will not support dc voltage, and a capacitor will not support dc current. On average, over an extended time interval, the voltage across an inductor must be zero, and the current into a capacitor must be zero.

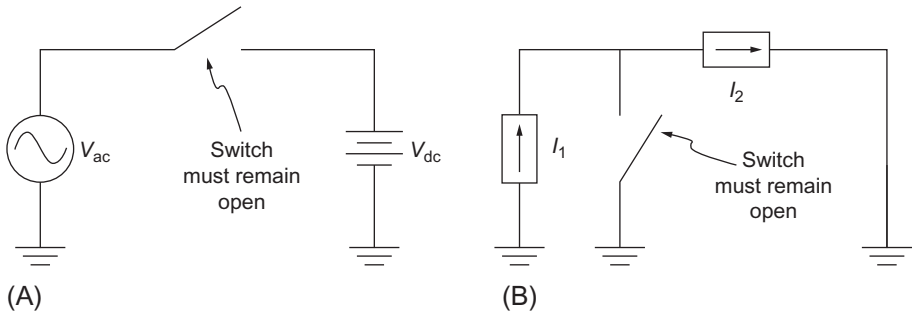


FIG. 1.13 Hypothetical power converters, (A) possible ac-dc converter and (B) possible dc-dc converter. (From P. T. Krein, Elements of Power Electronics, Oxford University Press, New York, 1998, Copyright 1998, Oxford University Press, used with permission.)

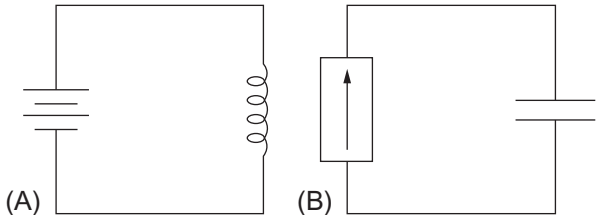


FIG. 1.14 Short-term KVL and KCL problems in energy storage circuits: (A) An inductor cannot sustain dc voltage indefinitely, and (B) a capacitor cannot sustain dc current indefinitely.

1.5.3 Resolving the Hardware Problem—Semiconductor Devices

A switch is either on or off. When on, an ideal switch will carry any current in any direction. When off, it will never carry current, no matter what voltage is applied. It is entirely lossless and changes from its on-state to its off-state instantaneously. A *real switch* can only approximate an ideal switch. The following are the aspects of real switches that differ from the ideal:

- Limits on the amount and direction of on-state current.
- A nonzero on-state voltage drop (such as a diode forward voltage).
- Some levels of leakage current when the device is supposed to be off.
- Limitations on the voltage that can be applied when off.
- Operating speed. The duration of transition between the on-states and off-states is important.

The degree to which the properties of an ideal switch must be met by a real switch depends on the application. For example, a diode can easily be used to conduct dc current; the fact that it conducts only in one direction is often an advantage, not a weakness.

Many different types of semiconductors have been applied in power electronics. In general, these fall into three groups:

1. Diodes, which are used in rectifiers, dc-dc converters, and in a wide range of supporting roles.
2. Transistors, which in general are suitable for control of single-polarity circuits. Several types of transistors are applied to power converters. The insulated-gate bipolar transistor (IGBT) type is unique to power electronics and has good characteristics for applications such as inverters.
3. Thyristors, which are multijunction semiconductor devices with latching behavior. In general, thyristors can be switched with short pulses and then maintain their state until current is removed. The characteristics are especially well suited to high-power controllable rectifiers, but they have been applied to all power conversion applications.

Some of the features of the most common power semiconductors are listed in Table 1.1. The table shows a wide variety of speeds and rating levels. As a rule, faster speeds apply to lower ratings. For each device type, cost tends to increase both for faster devices and for devices with higher power handling capacity.

TABLE 1.1 Examples of semiconductor devices used in power electronics

Device type	Characteristics of power devices
Diode	Current ratings from under 1 A to more than 5000 A. Voltage ratings from 10 V to 10 kV or more. The fastest power devices switch in <10 ns, whereas the slowest require 100 μs or more. The function of a diode applies in rectifiers and dc-dc circuits
BJT	(Bipolar junction transistor) Conducts collector current (in one direction) when sufficient base current is applied. The function applies to dc-dc circuits. Power BJTs for switching have been supplanted by FETs and IGBTs
FET	(Field-effect transistor) Conducts drain current when sufficient gate voltage is applied. Power FETs (nearly always enhancement-mode MOSFETs) have a parallel connected reverse diode by virtue of their construction. Ratings from about 0.5 A to about 150 A and 20 V up to 1200 V. Switching times are fast, from 20 ns or less up to 200 ns. The function applies to dc-dc conversion, where the FET is in wide use, and to inverters
IGBT	(Insulated-gate bipolar transistor) A transistor that has the function of a BJT with its base driven by an FET. Faster than a BJT of similar ratings and easy to use. Ratings from 10 A to more than 600 A, with voltages of 600–4500 V. The IGBT is common in inverters from about 1–200 kW or more. It is found almost exclusively in power electronic applications
SCR	(Silicon-controlled rectifier) A thyristor that conducts like a diode after a gate pulse is applied. Turns off only when current becomes zero. Prevents current flow until a pulse appears. Ratings from 10 A up to more than 5000 A and from 200 V up to 6 kV. Switching requires 1–200 μs. Widely used for controlled rectifiers. The SCR is found almost exclusively in power electronic applications and is the most common member of the thyristor family
GTO	(Gate turn-off thyristor) An SCR that can be turned off by sending a negative pulse to its gate terminal. The ratings approach those of SCRs, and the speeds are similar as well
TRIAC	A semiconductor constructed to resemble two SCRs connected in reverse parallel. Ratings from 2 to 50 A and 200–800 V. Used in lamp dimmers, home appliances, and hand tools. Not as rugged as many other device types, but convenient for many ac applications
IGCT	(Integrated gate-commutated thyristor) A combination device that includes a high-power GTO and external electronics to control it. This device is a member of a larger family of combination devices, in which multiple semiconductor chips packaged together perform a single power function. The IGCT provides a high-performance switch for power levels above 1 MW

Conducting direction and blocking behavior are fundamentally tied to the device type, and these basic characteristics constrain the choice of device for a given conversion function. Consider again a diode. It carries current in only one direction and always blocks current in the other direction. Ideally, the diode exhibits no forward voltage drop or off-state leakage current. Although an ideal diode lacks the many features of an

ideal switch, it is an important switching device. Other real devices operate with polarity limits on current and voltage and have corresponding ideal counterparts. It is convenient to define a special type of switch to represent this behavior, the *restricted switch*:

> **Definition** A restricted switch is an ideal switch with the addition of restrictions on the direction of current flow and voltage polarity. The ideal diode is one example of a restricted switch.

The diode always permits current flow in one direction, while blocking flow in the other direction. It therefore represents a *forward-conducting reverse-blocking* restricted switch and operates in one quadrant on a graph of device current versus voltage. This *unipolar* function is automatic; the two diode terminals provide all the necessary information for switch action. Other restricted switches require a third *gate*-terminal to determine their state. Consider the polarity possibilities given in Table 1.2. Additional functions such as bidirectional-conducting reverse-blocking can be obtained by reverse connection of one of the five types in the table.

The quadrant operation shown in the table indicates polarities. For example, the current in a diode will be positive when on, and the voltage will be negative when off. This means diode operation is restricted to the single quadrant comprising the upper vertical (current) axis and the left horizontal (voltage) axis. Other combinations appear in the table. Symbols for restricted switches can be built up by interpreting the diode's triangle as the current-carrying direction and the bar as the blocking direction. Five types of symbols can be drawn as shown in Table 1.2. These symbols are used infrequently but are useful for showing the polarity behavior of switching devices. A circuit drawn with restricted switches represents an idealized power converter.

TABLE 1.2 The types of restricted switches

Action	Device	Quadrants	Restricted switch symbol	Device symbol
Carries current in one direction, blocks in the other (forward-conducting reverse-blocking)	Diode			
Carries or blocks current in one direction (forward-conducting forward-blocking)	BJT, IGBT			
Carries in one direction or blocks in both directions (forward-conducting bidirectional-blocking)	GTO			
Carries in both directions but blocks only in one direction (bidirectional-conducting forward-blocking)	FET			
Fully bidirectional	Ideal switch			

Restricted switch concepts guide the selection of devices. For example, consider an inverter intended to deliver ac load current from a dc voltage source. A switch matrix built to perform this function must be able to manipulate ac current and dc voltage. Regardless of the physical arrangement of the matrix, we would expect bidirectional-conducting forward-blocking switches to be useful for this conversion. This is a correct result: modern inverters operating from dc voltage sources are built with field effect transistors (FETs) or with IGBTs packaged with reverse-parallel diodes. As new power devices are introduced to the market, it is straightforward to determine what types of converters will use them.

1.5.4 Resolving the Software Problem—Switching Functions

The physical $m \times n$ switch matrix can be associated with a mathematical $m \times n$ *switch state matrix*. Each element of this matrix, called a *switching function*, shows whether the corresponding physical device is on or off:

> **Definition** A *switching function*, $q(t)$, has a value of 1 when the corresponding physical switch is on and 0 when it is off. Switching functions are discrete-valued functions of time, and control of switching devices can be represented with them.

Fig. 1.15 shows a typical switching function. It is periodic, with period T, representing the likely repetitive switch action in a power converter. For convenience, it is drawn on a relative time scale that begins at 0 and draws out the square wave period by period. The actual timing is arbitrary, so the center of the first pulse is defined as a specified time t_0 in the figure. In many converters, the switching function is generated as an actual control voltage signal that might drive the gate of an FET or IGBT.

The timing of switch action is the only alternative for control of a power converter. Because switch action can be represented with a discrete-valued switching function, timing can be

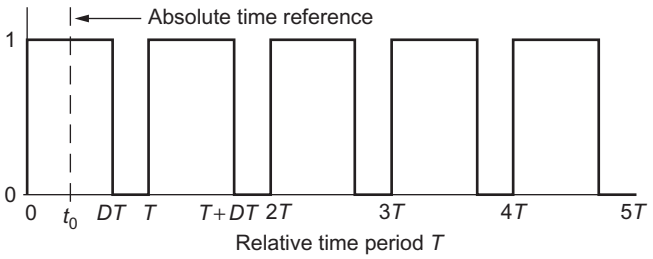


FIG. 1.15 A generic switching function with period T, duty ratio D, and time reference t_0.

represented within the switching function framework. On the basis of Fig. 1.15, a generic switching function can be characterized completely with three parameters:

1. The *duty ratio*, D, is the fraction of time during which the switch is on. For control purposes, the on-time interval or pulse width can be adjusted to achieve a desired result. We can term this adjustment process *pulse-width modulation* (PWM), perhaps the most important process for implementing control in power converters.
2. The frequency $f_{\text{switch}} = 1/T$ (with radian frequency $\omega = 2\pi f_{\text{switch}}$) is most often constant, although not in all applications. For control purposes, frequency can be adjusted. This strategy is sometimes used in low-power-dc-dc converters to manage wide load ranges. In other converters, frequency control is unusual because the operating frequency is often dictated by the application.
3. The time delay t_0 or phase $\varphi_0 = \omega t_0$. Rectifiers often use *phase control* to provide a range of adjustment. Phase-shifted bridge circuits are common for high-power dc-dc conversion. A few specialized ac-ac converter applications use phase modulation.

With just three parameters to vary, there are relatively few possible ways to control any power electronic circuit. Inverters and dc-dc converters usually rely on duty ratio adjustment (PWM) to alter their behavior. Phase control is common in controlled rectifier applications.

Switching functions are powerful tools for the general representation of converter action [7]. The most widely used control approaches derive from averages of switching functions [2,8]. Their utility comes from their application in writing circuit equations. For example, in the boost converter shown in Fig. 1.9, the loop and node equations change depending on which switch is acting at a given moment. The two possible circuit configurations each have distinct equations. Switching functions allow them to be combined. By assigning switching functions $q_1(t)$ and $q_2(t)$ to the left- and right-switching devices, respectively, we obtain

$$\begin{aligned} &q_1\left(V_{\text{in}} - L\frac{\mathrm{d}i_L}{\mathrm{d}t} = 0\right), \\ &q_1\left(C\frac{\mathrm{d}v_C}{\mathrm{d}t} + \frac{v_C}{R} = 0\right), \text{ left switch on} \end{aligned} \tag{1.8}$$

$$\begin{aligned} &q_2\left(V_{\text{in}} - L\frac{\mathrm{d}i_L}{\mathrm{d}t} = v_C\right), \\ &q_2\left(C\frac{\mathrm{d}v_C}{\mathrm{d}t} + \frac{v_C}{R} = i_L\right), \text{ right switch on} \end{aligned} \tag{1.9}$$

Because the switches alternate and the switching functions must be 0 or 1, these sets of equations can be combined to give

$$V_{\text{in}} - L\frac{\mathrm{d}i_{\text{L}}}{\mathrm{d}t} = q_2 v_{\text{C}}, \quad C\frac{\mathrm{d}v_{\text{C}}}{\mathrm{d}t} + \frac{v_{\text{C}}}{R} = q_2 i_{\text{L}} \tag{1.10}$$

The combined expressions are simpler and easier to analyze than the original equations.

For control purposes, the average of equations such as Eq. (1.10) often proceeds with the replacement of switching functions q with duty ratios d. The discrete-time action of a switching function thus will be represented by an average duty ratio parameter. Switching functions, advantages gained by averaging, and control approaches such as PWM are discussed at length in several chapters in this handbook.

1.5.5 Resolving the Interface Problem—Lossless Filter Design

Lossless filters for power electronic applications are sometimes called smoothing filters [9]. In applications in which dc outputs are of interest, such filters are commonly implemented as simple low-pass LC structures. The analysis is facilitated because in most cases the residual output waveform, termed ripple, has a predictable shape. Filter design for rectifiers or dc-dc converters is a question of choosing storage elements large enough to keep ripple low, but not so large that the whole circuit becomes unwieldy or expensive.

Filter design is more challenging when ac outputs are desired. In some cases, this is again an issue of low-pass filter design. However, in many applications, low-pass filters are not adequate to meet low noise requirements. In these situations, active filters can be used. In power electronics, the term active filter refers to lossless switching converters that actively inject or remove energy moment by moment to compensate for distortion. The circuits (discussed in Chapter 41—active filters in this handbook) are not related to the linear active filter op-amp circuits used in analog signal processing. In ac applications, there is a continuing opportunity for innovation in filter design.

1.6 Sample Applications

Although power electronics is becoming universal for electronic systems, a few emerging applications have generated wide interest. Some are discussed briefly here to introduce the breadth of activity in the field.

A hybrid or fully electric vehicle typically has two major power electronic systems and dozens or even hundreds of smaller ones [10]. The two large units are the inverter, which controls the electric drive motor, and a rectifier, which manages battery charging. Smaller systems include motor controllers in electric power-steering units, lighting electronics for solid-state lamps, controllers for small motors that actuate everything from windshield wipers to DVD players, and power supplies for the host of microcontrollers embedded in a modern car. As plug-in hybrid and electric cars continue to develop, the efficiency and sophistication of battery chargers and drive motor controllers will increase.

In a hybrid car, a typical inverter rating is about 50 kW. Fully electric automobiles have inverter ratings to about 200 kW. Hybrid and electric drive power levels increase from there to include multimegawatt inverters that power high-speed trains.

At the other power extreme, designers have been working on small power electronic systems that extract energy from various ambient sources for local purposes [11]. These energy harvesting applications are an emerging growth area. An example application is a corrosion sensor, built into a highway bridge that gathers energy from vibration. The vibration energy is converted and stored and then used for intermittent communication with a central monitoring computer. Typical power levels can be less than 0.001 W.

Solar, wind, and other alternative energy resources are tightly linked to power electronics. A typical solar panel produces about 30 V dc, with tolerances from 20 to 40 V or more. This randomly changing dc source must be converted to clean, tightly regulated ac voltage that synchronizes to the electricity grid and delivers energy. Solar inverter efficiency, reliability, and cost are major factors in successful energy innovation. A dual application, meaning that energy flows in the opposite direction but that many other characteristics are shared, is that of solid-state lighting [12]. In that case, flexible control of a dc current must be provided from an ac grid source.

For wind energy [13], a typical large-scale wind turbine can produce 2 MW of variable-frequency ac power. The frequency and voltage vary rapidly according to wind speed. This power must be converted to fixed frequency and voltage for grid interconnection.

1.7 Summary

Power electronics is the study of electronic circuits for the control and conversion of electrical energy. The technology is a critical part of our energy infrastructure and is central for a wide range of uses of electricity. For power electronics design, we consider only those circuits and devices that, in principle, introduce no loss and achieve near-perfect reliability. The two key characteristics of high efficiency and high reliability are implemented with switching circuits, supplemented with energy storage. Switching circuits can be organized as switch matrices. This facilitates their analysis and design.

In a power electronic system, the three primary challenges are the hardware problem of implementing a switch matrix, the software problem of deciding how to operate that matrix, and the interface problem of removing unwanted distortion and providing the user with the desired clean power source. The hardware is implemented with a few special types of power semiconductors. These include several types of transistors, especially FETs and IGBTs, and several types of thyristors, especially SCRs and GTOs. The software problem can be represented in terms of switching functions. The frequency, duty ratio, and phase of switching functions are available for operational purposes. The interface problem is addressed by means of lossless filter circuits. Most often, these are lossless LC passive filters to smooth out ripple or reduce harmonics. Active filter circuits also have been applied to make dynamic corrections in power conversion waveforms.

Improvements in devices and advances in control concepts have led to steady improvements in power electronic circuits and systems. This is driving tremendous expansion of applications. Personal computers, for example, would be unwieldy and inefficient without power electronic dc supplies. Mobile devices and laptop computers would be impractical. High-efficiency lighting, motor controls, and a wide range of industrial controls depend on power electronics. Strong growth is occurring in transportation applications, in lighting, in dc power supplies for portable devices, in high-end converters for advanced microprocessors, and in alternative and renewable energy. During the next generation, we will reach a time when almost all electrical energy is processed through power electronics somewhere in the path from generation to end use [14].

References

[1] J. Motto (Ed.), Introduction to Solid State Power Electronics, Westinghouse, Youngwood, PA, 1977.
[2] P.T. Krein, Elements of Power Electronics, Oxford University Press, New York, 1998.
[3] T.M. Jahns, E.L. Owen, Ac adjustable-speed drives at the millennium: how did we get here? in: Proceedings of IEEE Applied Power Electronics Conference, 2000, pp. 18–26.
[4] C.C. Herskind, W. McMurray, History of the static power converter committee, IEEE Trans. Ind. Appl. IA-20 (4) (1984) 1069–1072.
[5] E.L. Owen, Origins of the inverter, IEEE Ind. Appl. Mag. 2 (1996) 64.
[6] J.D. Van Wyk, F.C. Lee, Power electronics technology at the dawn of the new millennium—status and future, in: Rec. IEEE Power Electronics Specialists Conference, 1999, pp. 3–12.
[7] P. Wood, Switching Power Converters, Van Nostrand Reinhold, New York, 1981.
[8] R. Erickson, D. Maksimovic, Fundamentals of Power Electronics, second ed., Springer, New York, 2001.
[9] P.T. Krein, D.C. Hamill, Smoothing circuits, in: J. Webster (Ed.), Wiley Encyclopedia of Electrical and Electronics Engineering, John Wiley, New York, 1999.
[10] A. Emadi, K. Rajashekara, S.S. Williamson, S.M. Lukic, Topological overview of hybrid electric and fuel cell vehicular power system architectures and configurations, IEEE Trans. Veh. Technol. 54 (3) (2005) 763–770.
[11] E. Sazonov, L. Haodong, D. Curry, P. Pillay, Self-powered sensors for monitoring of highway bridges, IEEE Sensors J. 9 (11) (2009) 1422–1429.
[12] K.H. Loo, W.-K. Lun, S.-C. Tan, Y.M. Lai, C.K. Tse, On driving techniques for LEDs: toward a gener-alized methodology, IEEE Trans. Power Electron. 24 (12) (2009) 2967–2976.
[13] T. Dang, M.H. Rashid, Introduction, history, and theory of wind power, in: Proceedings of IEEE North American Power Symposium, 2009.
[14] P.T. Krein, Elements of Power Electronics, second ed., Oxford University Press, New York, 2015.

Section I

Power Electronic Devices

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2

Semiconductor Diodes and Transistors

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2.1 Semiconductor Diode

Understanding a semiconductor diode makes possible to understand other complex devices. A semiconductor diode is a structure containing a PN junction that, within its voltage and current rates, allows the conduction of current only in one direction. If the P region experiences a higher potential compared with the region N, the diode is said to be forward-biased, and a current can flow through the diode. On the other hand, if the region N experiences a higher voltage compared with the region P, the diode is said to be reversed-biased. In this case, no current flows through the diode. Fig. 2.1 shows a simplified illustration of such a diode structure.

The regions P and N are united by a metallurgical connection. When a negative voltage is applied between the PN junctions, this voltage appears at the depletion area due to the fact that this area presents higher resistance compared with the rest of the structure. Such voltage makes the electrons in the N region to travel to the P region and vice versa, creating a so-called potential barrier, which, in turn, defines the size of the depletion area. The potential barrier opposes the electron and hole movements across the junction. The potential is approximately 0.7 and 0.3 V for silicon and germanium diodes, respectively, and it is defined as threshold voltage [1].

When a positive voltage higher than the threshold is applied between the PN junctions, the potential barrier is reduced, minimizing the depletion area, and the carriers are free to conduct through the regions, leading the diode to be forward-biased.

Diodes in electric circuits are represented by the symbol depicted in Fig. 2.2. The terminals of the diode are known as anode (A) that corresponds to the P region and cathode (K) that corresponds to the N region. The conventional current

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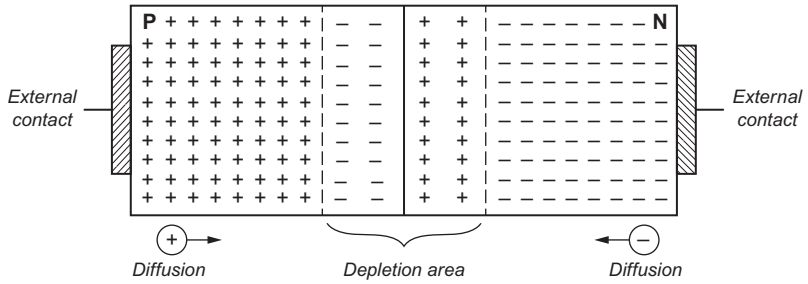


FIG. 2.1 Simplified illustration of a junction diode structure.

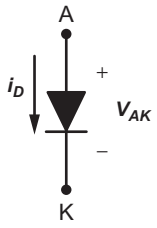


FIG. 2.2 The symbol used for a diode and its current and voltage references.

and voltage references through a diode are also shown. The electron flow is in the opposite direction related to the current reference.

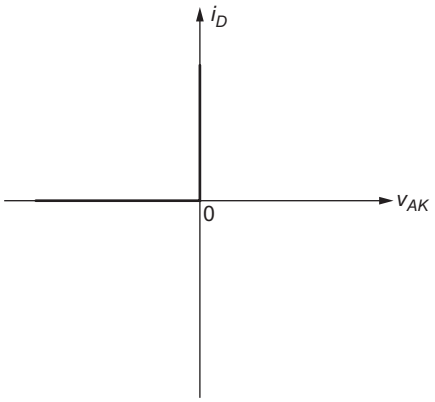


FIG. 2.3 Static characteristic of an ideal diode.

2.1.1 Static Characteristics

The static characteristic of an ideal diode is portrayed in Fig. 2.3. For voltages $v_{AK} > 0$, the diode conducts with current i_F under null voltage. Consequently, the diode can be represented as a short circuit. For voltages $v_{AK} < 0$, the diode holds a negative voltage, and it does not conduct any current. Therefore, the diode can be represented by an open circuit.

The use of an ideal diode in analyzing circuits is accepted in power electronic applications, since it is necessary only to know if the diode is forward- or reversed-biased. However, in applications where a deeper analysis is required, it is necessary to consider the diode real features. Fig. 2.4A presents the static characteristic of a real diode. The characteristic curve is not on scale for better visualization. The first quadrant is the region where the diode is forward-biased. In this case, the diode is in ON state. The third quadrant is the region of reverse bias. Thus, the diode is in OFF state. Fig. 2.4B presents a more realistic diode structure with its layers length.

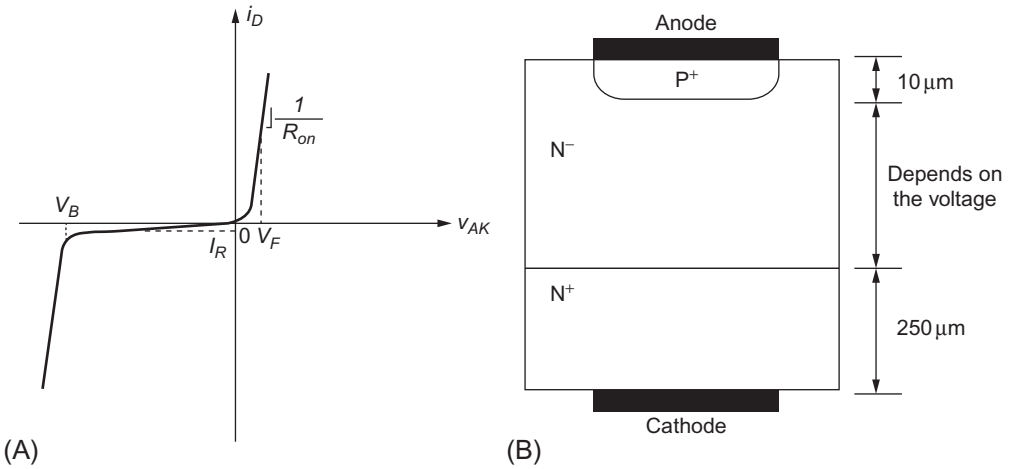


FIG. 2.4 (A) Static characteristic of a real diode and (B) more realistic diode structure.

The following details can be highlighted from the previous chart [2]:

- *Forward voltage, V_F*: The voltage drop across the diode, from terminal *A* to *K*, at a specific current when the diode is forward-biased.
- *Breakdown voltage, V_B*: The maximum reverse voltage across the diode before the diode starts reverse conduction and gets severe damaged. The point at *Vb* is also known as avalanche point.
- *Reverse current I_R*: The current at a particular reverse voltage. This current is usually in the range of μA and hardly taken into account in analysis of power electronic circuits.
- *Conduction resistance R_{ON}*: The equivalent resistance presented by the diode when forward-biased and conducting current. The inverse of this resistance is the slope of the curve in forward region. This characteristic is more relevant in high-voltage devices in which the semiconductor length is larger.

A more complete diode model, during conduction, is shown in Fig. 2.5.

2.1.2 Dynamic Characteristics

The static characteristics of a diode are valid for analysis in steady-state condition, with the diode completely in the state ON or OFF. For the period when the diode is changing between these states, the diode presents a dynamic behavior. Fig. 2.6 presents the circuit used to analyze the turn-on and turn-off characteristic of a power diode. The turn-on process is defined by the change from the OFF to ON state, while the turn-off process is the change from ON to OFF state. The voltage source is supposed to produce a square waveform. The inductor represents the inductive effect of the circuit (ration of the magnetic flux and current) that is present in any electric circuit. The inductance value can be very low, depending on the circuit topology, but can have an important rule to limit the di/dt.

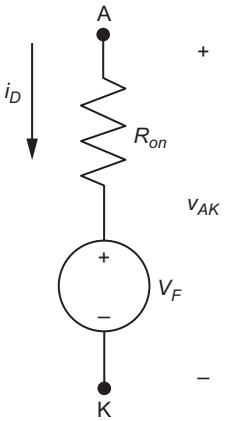


FIG. 2.5 Equivalent circuit of a real diode when forward-biased.

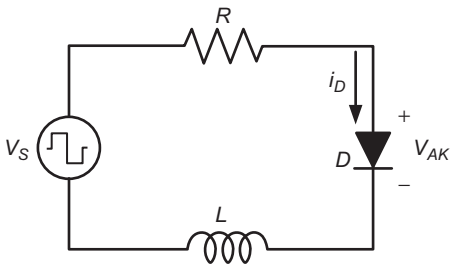


FIG. 2.6 Circuit used to analyze the switching characteristic of a power diode.

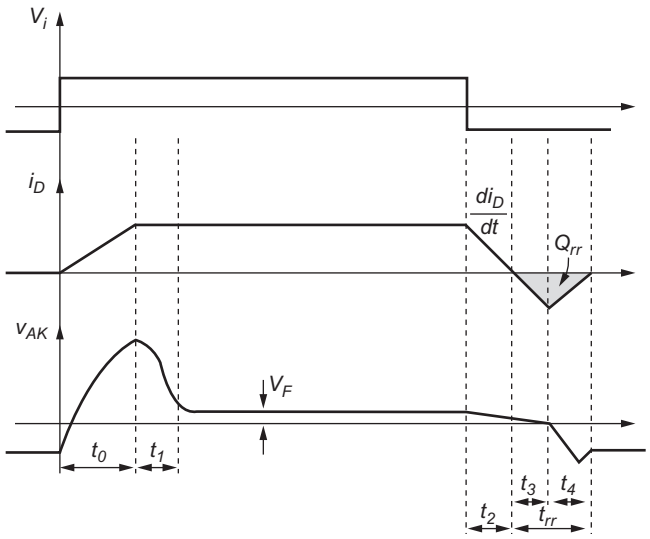


FIG. 2.7 Typical dynamic behavior for the voltage and current of a diode during the turn-on and turn-off periods.

Fig. 2.7 presents a typical dynamic behavior for the voltage and current of a diode during the turn-on and turn-off intervals. The waveform can change slightly from diode to diode and based on intrinsic properties and also if the circuit contains inductive load.

The time intervals highlighted in the figure are defined as follows:

- *Time interval t_0*: The time interval t_0 begins when the voltage source changes its value from negative to positive, initializing the turn-on process. During t_0, the storage charges in the depletion area are removed. The diode current begins to rise, while the diode voltage suffers a peak due to the fact that there is no enough injection of carriers into the depletion area and also due to the resistance of the N region.
- *Time interval t_1*: At this interval, the injection of carriers is completed, and the diode voltage falls to the forward voltage. In power diodes, the intervals t_0 and t_1 are in the range of ten to hundreds of nanoseconds. At the end of t_1, the turn-on process is completed.

- *Time interval* t_2: The interval t_2 begins when the voltage source changes in value from positive to negative, initializing the turn-off process. The minority carriers (electrons in P region and holes in N region) must be removed before the formation of the potential barrier, during such time the diode keeps conducting. The diode voltage falls slightly due to the fall in the resistance R_{ON}.
- *Time interval* t_3: The interval t_3 keeps the behavior of the previous interval, but the diode current is achieving negative current. When the current achieves its negative peak, the minority carriers were reversed, and the diode begins to be reversed-biased.
- *Time interval* t_4: The interval t_4 is the time required for the current to achieve null value, recharging the depletion area. The voltage across de diode suffers an overvoltage mainly due to the parasitic inductances found in the circuit.
- *Time interval* t_{rr}: The time interval t_{rr} is the sum of the intervals t_3 and t_4 and it is known as reverse recovery time. The area under the t-axis in the current waveform is equivalent to the so-called reverse recovery charge.

The reverse recovery time is an important parameter to decide the switching frequency of applications involving diodes. The reverse recovery time must finish before the diode can be forward-biased again. The lower the t_{rr} is, the faster the diode can be switched. Diodes with low reverse recovery time are known as fast diodes or sometimes ultrafast diodes.

Another important feature concerning reverse recovery process is how severe the diode current behaves during the reverse recovery time. For this purpose, the terms soft- and hard-recovery diodes are used. Soft-recovery diodes present slow current fall, while hard-recovery diodes present fast current fall. A slow current fall is more attractive because the voltage produced at the parasitic inductances is lower compared with other case.

2.1.3 Common Types of Diodes

Diodes can be classified into the following major types [2,3]:

Small signal diode: This type of diode has a niche of application in low-power rectifiers, limiters, amplifiers, and in waveshaping. These applications are low-voltage, low-current devices. Forward voltage, reverse breakdown voltage, and reverse recovery current and time are parameters that must be known by a designer when applying small signal diode in power electronic applications.

Power rectifier diode: This type of diode has high forward current and high reverse breakdown voltage capabilities. They are suited for power applications like rectifiers, inverters, and power supplies. The thermal resistance is an important factor for a designer, since these diodes usually require heat sink for heat dissipation.

Zener diode: This type of diode is mainly used in voltage regulation. It operates on the reverse-biased mode. A current called zener current conducts through it in order to clamp the voltage. The behavior on the breakdown voltage is designed to support the dissipation without damaging the device.

Schottky diodes: The aforementioned diodes have an ohmic behavior in the contact between the metal terminal and the semiconductor. Schottky diodes are formed by allocating a thin film of metal directly to the semiconductor material. As result, the behavior in the referred region has a rectifier effect. The forward voltage drop in Schottky diodes is usually 0.3 V, and they are used in low-voltage applications.

2.1.4 Evaluating the Dynamic Characteristics of Real Diodes

In order to visualize how is the real reverse recovery behavior of some types of diodes, the circuit shown in Fig. 2.8 was built. The circuit is composed by a square-wave source. A fast diode (SK3GL04), a slow rectifier diode (1N5404), and a Schottky diode (1N5818) are connected in the circuit through the switches Sw1, Sw2, and Sw3, respectively. A resistor R is used as load. Switch Sw4 is used to insert or remove an inductor in the circuit. Initially, this switch Sw4 is ON, bypassing the inductor. Each diode is analyzed individually in the circuit.

Fig. 2.9 shows the current of each diode during the turn-off process. For the fast and Schottky diodes, the reverse recovery time is in the range of 2–3 μs. For the slow rectifier diode, the time is approximately 10 μs, and the reserve recovery charge is considerably higher than those for the other diodes. The negative current is limited by the external resistance. It is clear that the rectifier diode can be used only in low-frequency applications with low *dv/dt*, as in 50 and 60 Hz AC systems.

Fig. 2.10 shows the current and voltage in the small signal diode when the switch Sw_4 is OFF, inserting the inductor in the circuit. Both waveforms oscillate during the reverse recovery time. The oscillation in the voltage may lead the diode to be forward-biased improperly if its value reaches higher value than the threshold.

2.1.5 Series and Parallel Connection of Power Diodes

Two important parameters of power diodes concerning voltage ratings are repetitive peak inverse voltage (V_{RRM}) and nonrepetitive peak inverse voltage. The first states about the capability of the diode in holding reverse voltage in a sustained manner.

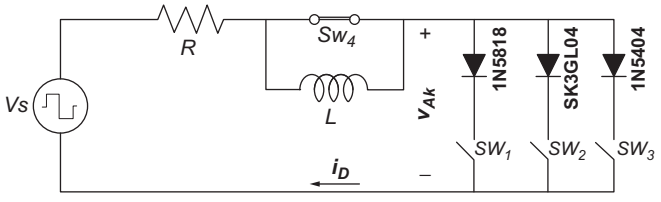


FIG. 2.8 Circuit used to evaluate the real reverse recovery behavior of diodes.

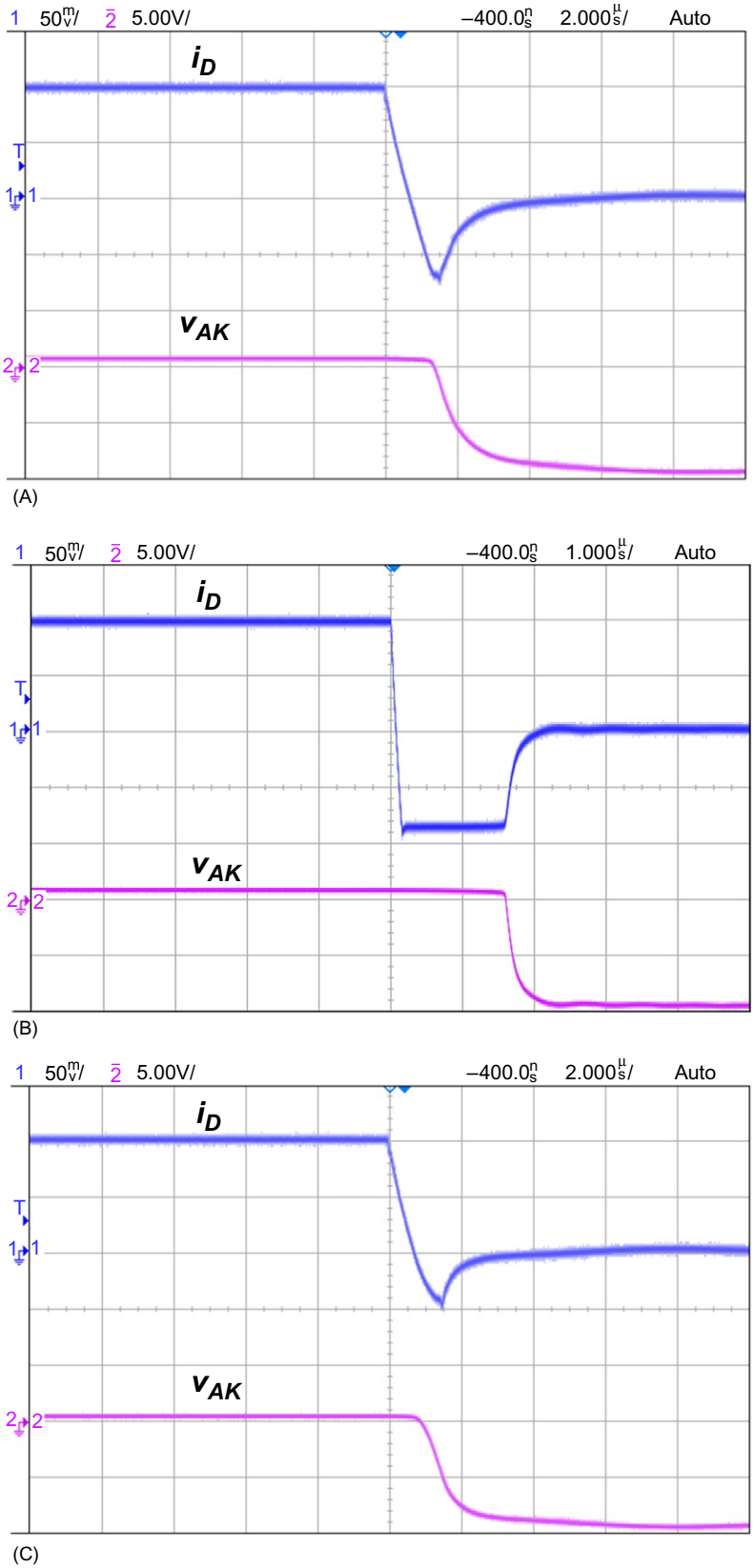


FIG. 2.9 Current of each diode during the turn-off process. (A) SK3GL04 (fast diode) SW1 is ON, (B) 1N5404 (rectifier) SW2 is ON, and (C) 1N5818 (Schottky) SW3 is ON.

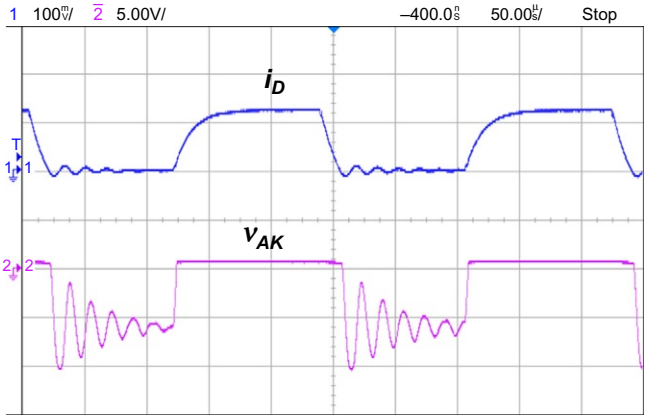


FIG. 2.10 Current and voltage in the small signal diode when the switch *Sw4* is OFF.

The second is the capability of the diode in holding reverse voltage that occurs occasionally.

Concerning current rating, power diodes have the following parameters: average current, RMS current, and peak current. These parameters vary in accordance to the diode temperature. Therefore, by properly dissipating the heat of a diode, the current capability is better utilized.

When an application requires current or voltage ratings that is beyond its capability, parallel or series shall be considered. Connecting diodes in series gives a structure with high-voltage rating, once the voltage will be divided among them. On the other hand, connecting diodes in parallel allows a high-current rating, once the current is divided among the diodes. The major concern in making series or parallel connection is to match their parameters, especially in reverse recovery properties. Otherwise, voltage and current unbalance may occur among the diodes.

In order to overcome such unbalance in series connection, a bank of resistor and capacitor is placed in parallel with the diode string. Fig. 2.11 presents the series connection of diodes with banks of resistor and capacitors. During the transitions, the capacitors equalize the voltage. During the OFF state, the resistive path equally divides the total voltage. The current through the resistor must be higher than the diode reverse leakage current [2].

The A–K points are the terminals of a fictitious high-voltage capacity diode. Ideally, when reverse-biased, the reverse voltage is dived equally among the three diodes.

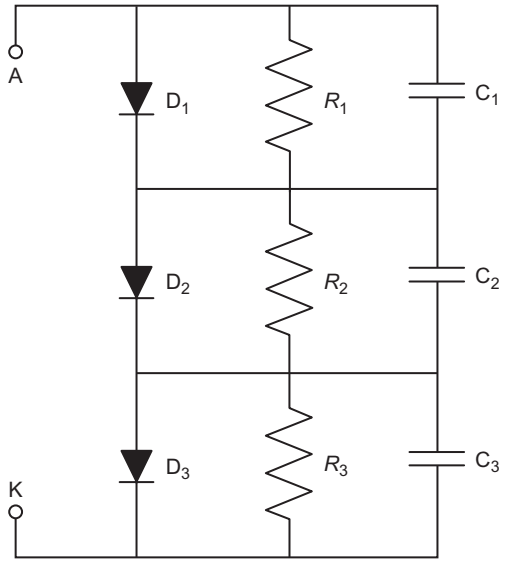


FIG. 2.11 Series connection of diodes with resistor and capacitors for equalization.

The parallel connection of diodes is intended to divide a current equally through the diodes. However, if one diode turns on before the others, the entire current passes through it. Such occurrence may destroy the diode. In order to overcome that, a resistor can be connected in series with each diode. The resistor limits the current in case one diode turns on before the others. Including a resistor is series with each diode decreases considerably the efficiency of the circuit.

For both parallel and series connection of diodes, a special attention must be paid concerning the construction of the printed circuit board (PCB) layout. Parasitic inductances can cause a diode to be forward-biased before the other. Therefore, the layout must be designed aiming an equal parasitic inductance in the path where diodes are being associated in parallel and series.

2.1.6 Typical Application of Diodes

2.1.6.1 Rectifiers

Diodes are widely used as rectifiers. Fig. 2.12 presents the half- and full-wave single-phase rectifiers. An input transformer (not

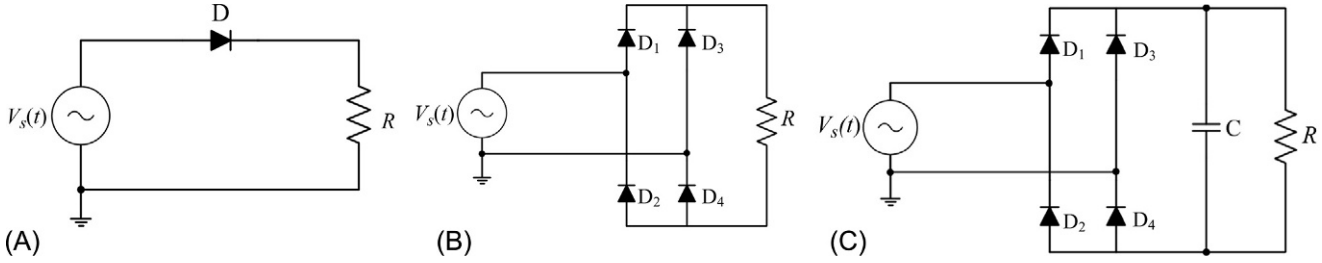


FIG. 2.12 (A) Half-wave rectifier, (B) full-wave rectifier, and (C) full-wave rectifier with capacitor.

shown) can be placed at the input of rectifiers for isolation and voltage leveling purpose. The use of a half-wave rectifier is exclusively for low-power applications, once the average input current is not zero. A capacitor can be used at the output of full-wave rectifier in order to minimize the voltage ripple.

The diodes make only the positive voltage to appear across the load. Fig. 2.13 presents the output voltage for the half-wave, full-wave, and full-wave rectifier with capacitor. In this case, the diodes are considered ideal with no forward voltage drop.

2.1.6.2 Freewheeling

A diode can be used as a freewheeling path for keeping an inductor current conducting continuously. Fig. 2.14 presents a DC–DC converter where the diode operates as freewheeling path. The switch represents a transistor. Without the diode, the inductor would cause an extremely high *dv/dt* across it when the transistor changes from ON to OFF state. Such high *dv/dt* would appear across the transistor, probably destructing it. However, the diode allows a path to the inductor current avoiding high *dv/dt*. The voltage produced by the inductor current will be high enough to directly polarize the diode. In this converter, this voltage is just higher than the output voltage. The transistor and the diode are considered ideal.

Fig. 2.15 presents the inductor current, the transistor current, and the diode current. Notice that the inductor current passes through the transistor when this is ON and through the diode when the transistor is OFF.

2.1.6.3 Voltage Multiplier

Fig. 2.16 presents a voltage multiplier circuit with the output voltage four times higher than the amplitude of the input voltage, neglecting the diode voltage drops. This circuit is used when a higher voltage compared with the input is required. The transformer in this case is used only for isolation.

2.1.7 PSPICE Model

SPICE is a general-purpose circuit platform that can be used to simulate electronic and electric circuits [4]. SPICE was originally developed at the Electronics Research Laboratory of the University of California, Berkeley (1975). The name stands for simulation program for integrated circuits emphasis. A circuit must be specified in terms of element names, element values, nodes, variable parameters, and sources. SPICE can do several types of circuit analyses:

- Nonlinear DC analysis, calculating the DC transference
- Nonlinear transient analysis—calculates signals as a function of time
- Linear AC analysis—computes the Bode plots as a function of frequency
- Noise analysis
- Sensitivity analysis
- Distortion analysis
- Fourier analysis
- Monte Carlo analysis

In addition, PSPICE has analog and digital libraries of standard components such as operational amplifiers, digital gates, and flip-flops. This makes it a useful tool for a wide range of analog and digital applications. An input file, called source file, consists of three parts: (1) data statements, with description of the components and the interconnections; (2) control statements, which tells SPICE what type of analysis to perform; and (3) output statements, with specifications that outputs are to be printed or plotted. Two other statements are required: the title statement and the end statement. The title statement is the first line and can contain any information, while the end statement is always .END. In addition, there are also comment statements that must begin with an asterisk (*) and are ignored by SPICE.

A set of device model parameters is defined on a separate .MODEL card and assigned to a unique model name. Parameter values are defined by appending the parameter name, followed by an equal sign and its value. Model parameters without specific value are assigned the default values.

As an example, the model parameter for the Schottky diode 1N5818 is given by the following text:

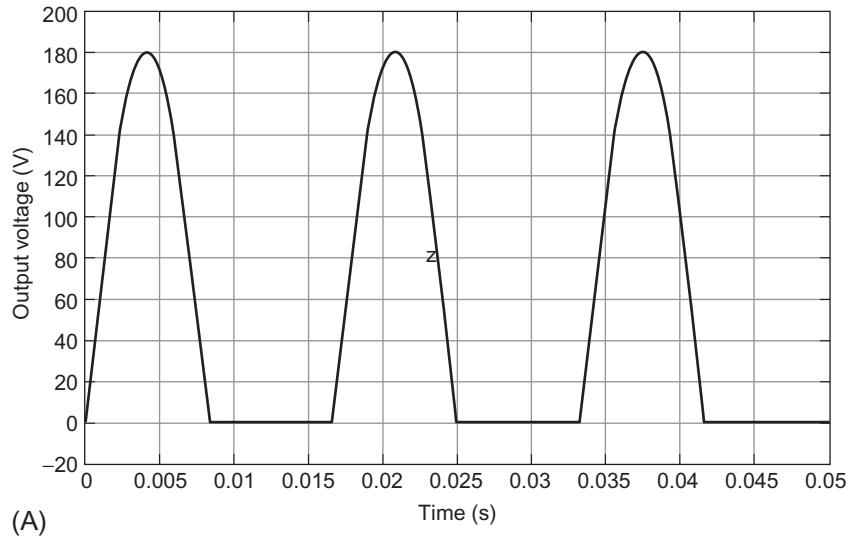
```
.MODEL 1N5818 D (IS=263u RS=73.1m BV=30.0 IBV=1.00m+
CJO=203p M=0.333 N=1.90 TT=4.32u )
```

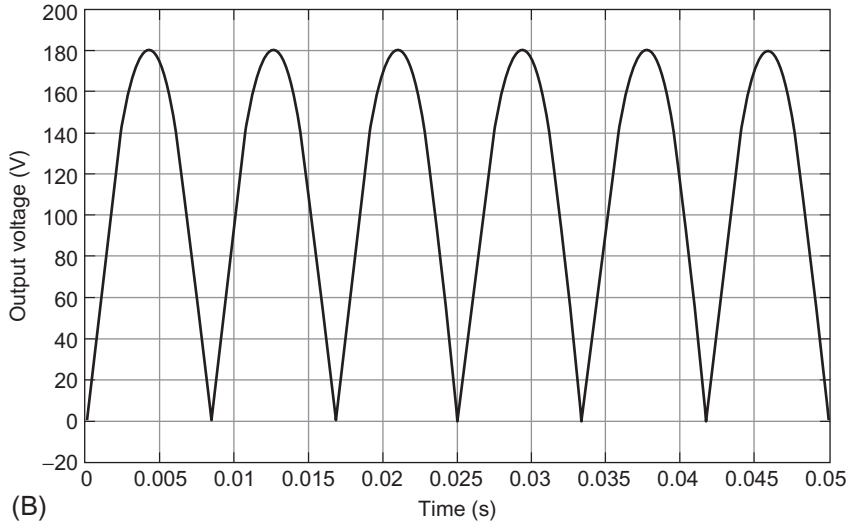
The definition of each parameter is given in Table 2.1. The description of the parameter is beyond the scope of this chapter.

The designer will have to decide, depending on the application or the study, if he or she should use of a more or a less sophisticated model of diodes in their circuit simulation.

2.2 Power Bipolar Transistor

The first transistor was created in 1948 by a team of physicists at the Bell Telephone Laboratories and soon became a semiconductor device of major importance. In addition of becoming an important switch for power electronic applications, all microprocessors, microcontrollers, and FPGAs have in their microelectronic design a transistor to implement the required logic circuits. Before the transistor was developed, amplification was achieved with vacuum tubes or magnetic devices. Even though there are now integrated circuits with millions of transistors, the flow and control of all the electric energy still require single transistors. Therefore, power semiconductor switches constitute the heart of modern power electronics. Depending on the application, such devices should have larger voltage or current ratings, instant turn-on and turn-off characteristics, very low-voltage drop when fully on, zero leakage current in blocking condition, and ruggedness to switch highly inductive loads, which are measured in terms of the safe operation area (SOA) and reverse-biased second breakdown,





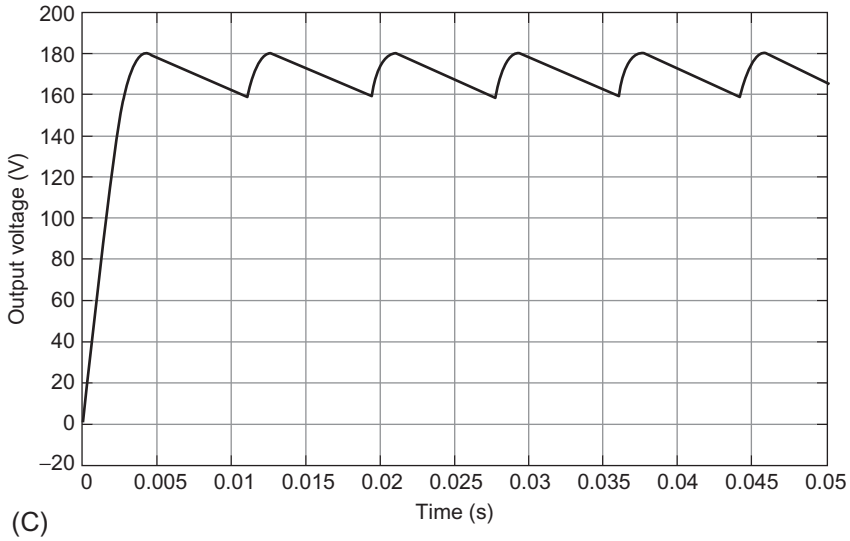


FIG. 2.13 (A) Half-wave rectifier, (B) full-wave rectifier, and (C) full-wave rectifier with capacitor.

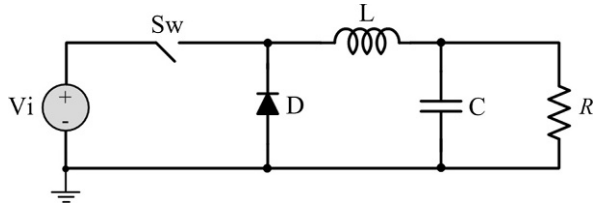


FIG. 2.14 A DC–DC converter showing a diode operating in a freewheeling path.

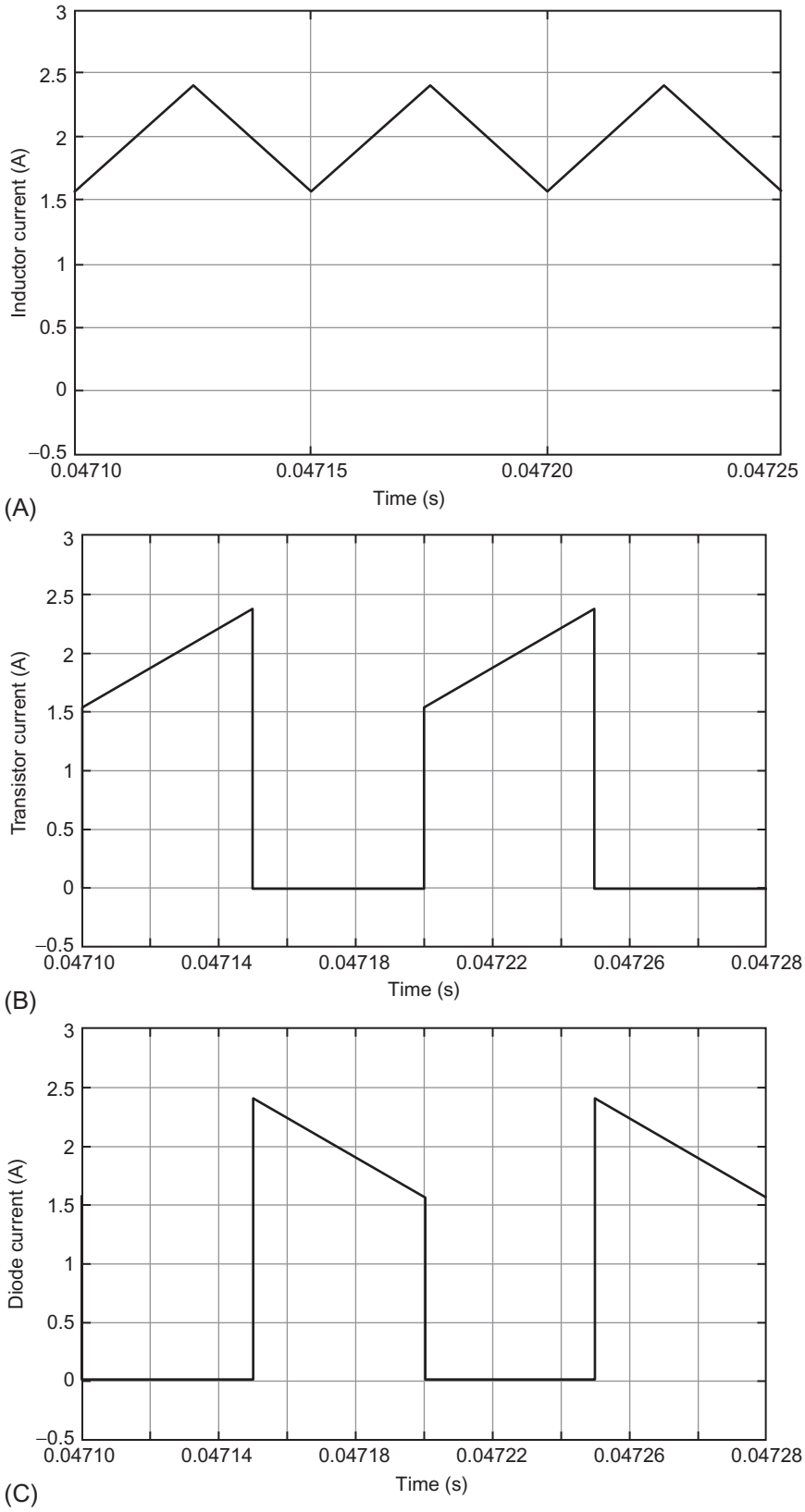


FIG. 2.15 (A) Inductor current, (B) transistor current, and (C) diode current.

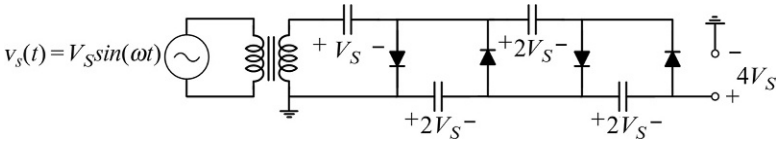


FIG. 2.16 Voltage multiplier circuit.

TABLE 2.1 Parameter definition of a diode model

Parameter	Definition
IS	Saturation current
RS	Parasitic resistance
BV	Reverse breakdown voltage
IBV	Reverse breakdown current
CJO	Zero-bias P–N capacitance
N	Emission coefficient
TT	Transit time
M	Junction grading coefficient

high-temperature and radiation capabilities, and high reliability. The right combination of such features restricts the devices suitability to certain applications. High-voltage and high-current ratings permit applications in large motor drives, induction heating, renewable energy inverters, high-voltage DC (HVDC) converters, static reactive energy compensators, and active filters. On the other hand, low-voltage and high-frequency applications concern switching mode power supplies, resonant converters, and motion control systems. Low frequency with high-current and high-voltage devices are restricted to cycloconverter-fed and multimegawatt drives [5,6].

Bipolar junction transistors (BJT) are used to be the traditional component for driving several of those industrial applications. However, insulated gate bipolar transistor (IGBT) and metal-oxide-semiconductor field-effect transistor (MOSFET) technology have progressed so that they are viable replacements for the BJT. However, BJTs still have performance areas in which they may be preferably used, especially when the cost is the main concern.

2.2.1 Basic Structure and Operation

The BJT consists of a three-region structure of N-type and P-type semiconductor materials. It can be constructed as NPN and PNP. Fig. 2.17 shows the physical structure of a planar NPN BJT. The operation is closely related to that of a junction diode where in normal conditions the PN junction between the base and emitter is forward-biased ($V_{BE} > 0$) causing electrons to be injected from the emitter into the base. Since the base region is thin, the electrons travel across it arriving at the reverse-biased base-collector junction ($V_{BC} < 0$) where there is an electric field (depletion region). Upon arrival at this junction, the electrons are pulled across the depletion region and draw into the collector. These electrons flow through the collector region and out the collector contact. Because electrons are negative carriers, their motion constitutes positive current flowing into the external collector terminal. Even though the forward-biased base-emitter junction injects holes from base to emitter, they do not contribute to the collector current, but result in a net current flow component into the base from the external base terminal. Therefore, the emitter current is composed of those two components: electrons destined to be injected across the base-emitter junction and holes injected from the base into the emitter.

The emitter current is exponentially related to the base-emitter voltage according to (2.1):

$$i_E = i_{E0}\left(e^{V_{BE}/\eta V_T} - 1\right) \tag{2.1}$$

where i_E is the saturation current of the base-emitter junction that is a function of the doping levels, temperature, and the area

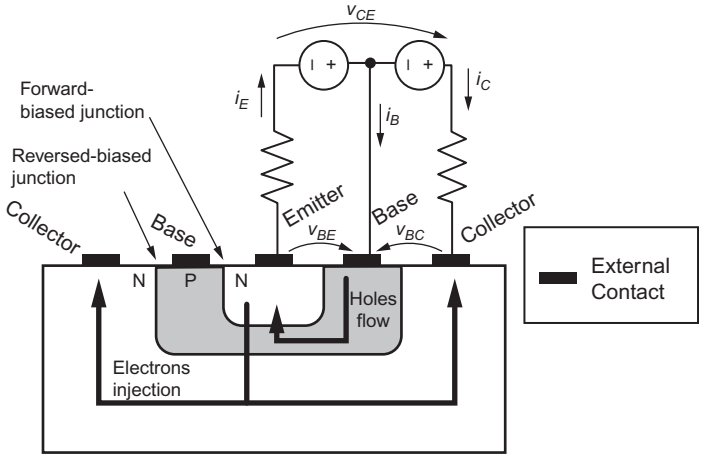


FIG. 2.17 Structure of a planar bipolar junction transistor.

of the base-emitter junction; V_T is the thermal voltage Kt/q; and η is the emission coefficient. The electron current arriving at the collector junction can be expressed as a fraction α of the total current crossing the base-emitter junction as shown in (2.2):

$$i_C = \alpha i_E \tag{2.2}$$

Since the transistor is a three-terminal device, i_E is equal to $i_C + i_B$; hence, the base current can be expressed as the remaining fraction, given by (2.3):

$$i_B = (1-\alpha) i_E \tag{2.3}$$

The collector and base currents are thus related by the ratio given in (2.4):

$$\frac{i_C}{i_B} = \frac{\alpha}{1-\alpha} = \beta \tag{2.4}$$

The values of α and β for a given transistor depend primarily on the doping densities in the base, collector, and emitter regions and on the device geometry. Carrier recombination and temperature also affect the values for both parameters. A power transistor requires a large blocking voltage in the OFF state and a high-current capability in the ON state. A vertically oriented four-layer structure as shown in Fig. 2.18 is preferable because it maximizes the cross-sectional area through which the current flows, reducing the on-state resistance and power dissipation in the device. There is an intermediate collector region with moderate doping. The emitter region is controlled so as to have a homogenous electric field.

Optimization of doping and base thickness is required to achieve high breakdown voltage and amplification capabilities. Power transistors have their emitter and base interleaved to reduce parasitic ohmic resistance in the base current path and also to improve the device for second breakdown failure. The transistor is usually designed to maximize the emitter periphery per unit area of silicon, for the purpose of achieving the highest current gain at a specific current level. In order to ensure those features, transistors have the greatest possible safety margin; they are designed to dissipate substantial power and, thus, have low thermal resistance. It is for this reason, among others, that the chip area must be large and that the emitter periphery per unit area is sometimes not optimized. Most transistor manufacturers use aluminum metallization, since it has many attractive advantages, among these are ease of application by vapor deposition and ease of definition by photolithography. A major problem with aluminum is that only a thin layer can be applied by normal vapor deposition techniques. Thus, when high currents are applied along the emitter fingers, a voltage drop occurs along them, and the injection efficiency on the portions of the periphery that are furthest from the emitter contact is reduced. This limits the amount of current each finger can conduct. If copper metallization is used, then it is possible to reduce the resistance from the emitter contact to the operating regions of the transistors (the emitter periphery).

From a circuit point of view, Eqs. (2.1)–(2.4) are used to relate the variables of the BJT input port (formed by base and emitter) to the output port (collector and emitter). The circuit symbols are shown in Fig. 2.19. Most of the power electronic applications use NPN transistor because electrons move faster than holes, and therefore, NPN transistors have considerable faster commutation times compared with the equivalent PNP transistors.

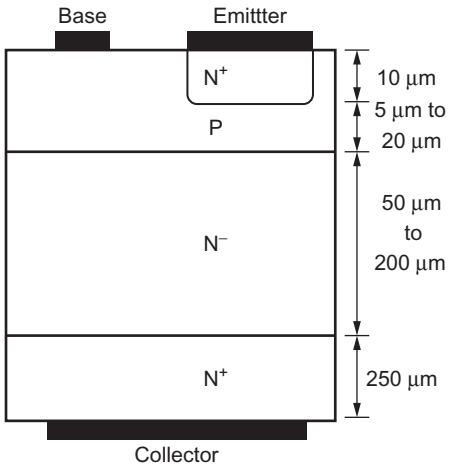


FIG. 2.18 Power transistor vertical structure.

2.2.2 Static Characteristics

The static ratings determine the maximum allowable limits of current and voltage. The absolute voltage limit mechanism is concerned to the avalanche such that thermal runaway does not occur. Forward current ratings are specified at which the junction temperature does not exceed a rated value. Fig. 2.20 shows the base current i_B plotted as a function of the base-emitter voltage V_{BE}. The V_f voltage is around 0.7 V for silicon BJTs.

Fig. 2.21 depicts the collector current i_C as a function of the collector-emitter voltage V_{CE} with i_B as the controlling variable. The curves are distinguished each other by the value of the base

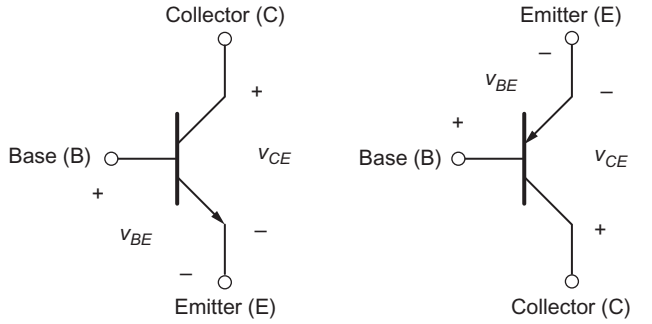


FIG. 2.19 Circuit symbols, (A) NPN transistor and (B) PNP transistor.

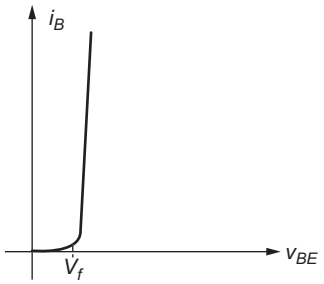


FIG. 2.20 Base current plotted as a function of the base-emitter voltage.

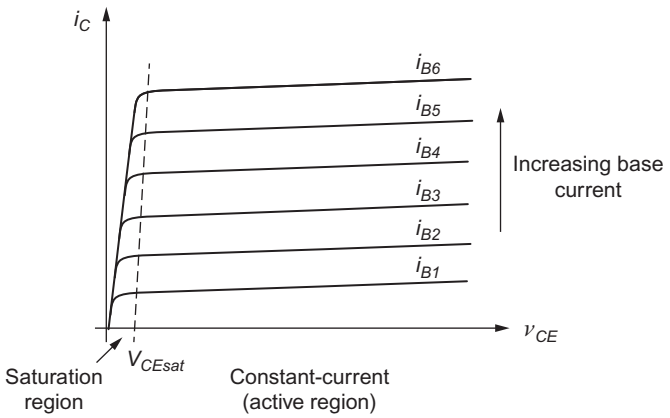


FIG. 2.21 Collector current as a function of the collector-emitter voltage with the base current as the controlling variable.

current. A small base current drives the flow of a much larger current between collector and emitter; such gain called beta (Eq. 2.4) depends upon temperature, V_{CE}, and i_C.

The active region is defined where flat, horizontal portions of voltage-current curves show "constant" i_C current, because the collector current does not change significantly with V_{CE} for a given i_B. Those portions are used for transistors operating as linear amplifiers. In this region, as the voltage and current can present high values, the dissipated power is high. Switching power electronic systems on the other hand requires transistors to operate either in the saturation region where V_{CE} is small or in the cutoff region where the current is zero and the voltage is uphold by the device. In both situations, the dissipated power is low. The crossing of the active region must be as fast as possible to minimize the losses and the consequent temperature increase. The saturation region is characterized by the forward-biased of base-collector junction, and it occurs when $V_{CE} < 0.7V$.

High-voltage BJTs typically have low-current gain, and hence, Darlington-connected devices, as indicated in Fig. 2.22, are commonly used.

Considering gains β_1 and β_2 for each one of those transistors, the Darlington connection will have total gain of $\beta_1 + \beta_2 + \beta_1\beta_2$. Diode D_1 speeds up the turn-off process, by allowing the base driver to remove the stored charge on the T_2 base.

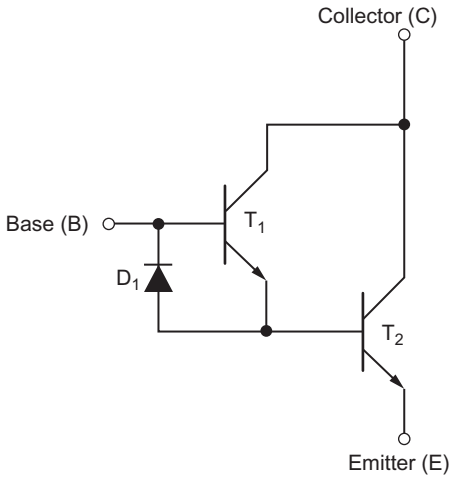


FIG. 2.22 Darlington-connected BJTs.

Vertical-structure power transistors have an additional region of operation called quasi saturation, indicated in the characteristic curve of Fig. 2.23. Such feature is a consequence of the lightly doped collector drift region (N^-) where the collector-base junction supports a low reverse bias. If the transistor enters in the hard-saturation region, the on-state power dissipation is minimized but has to be traded off with the fact that in quasi saturation, the stored charges are smaller. At high collector currents, beta gain decreases with increased temperature, and with quasi-saturation operation, such negative feedback allows careful device paralleling. Two mechanisms on microelectronic level determine the fall off in beta, namely, conductivity modulation and emitter crowding.

Concerning the voltage, there is a region called primary breakdown due to conventional avalanche of the collector-base junction and the attendant large flow of current. The BV_{SUS} is the limit for primary breakdown; it is the maximum collector-emitter voltage that can be sustained across the transistor when it is carrying collector current. The BV_{SUS} is lower than BV_{CEO} or BV_{CBO} that measure the transistor's voltage standoff capability when the base current is zero or negative. The bipolar

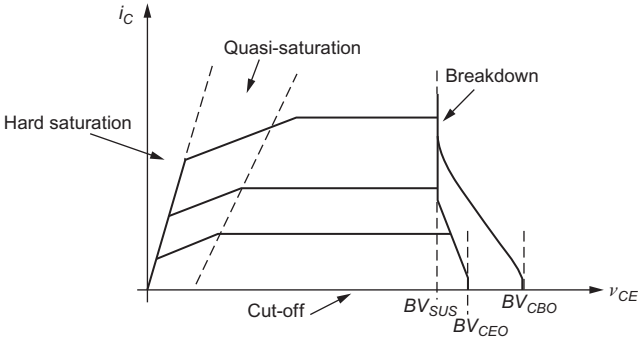


FIG. 2.23 Voltage-current characteristics for a vertical power transistor.

transistor has another potential failure mode called second breakdown, which shows as a precipitous drop in the collector-emitter voltage at large currents. Because the power dissipation is not uniformly spread over the device, but it is rather concentrated on regions, a local gradient of temperature can rise very quickly. Such thermal runaway brings hot spots that can eventually melt and recrystallize the silicon resulting in the device destruction. The key to avoid second breakdown is to (1) keep power dissipation under control, (2) use a controlled rate of change of base current during turnoff, (3) use of protective snubbers circuitry, and (4) position the switching trajectory within the SOA boundaries [2,5,7].

2.2.3 Safe Operation Area

In order to describe the maximum values of current and voltage the transistor should hold, two diagrams are used: the forward-bias safe operating area (FBSOA), known also simply as SOA, given in Fig. 2.24, and the reverse-bias safe operating area (RBSOA) shown in Fig. 2.25.

In the FBSOA, the current I_{CM} is the maximum current of the device; there is a boundary defining the maximum thermal dissipation and a margin defining the second breakdown limitation. Those regions are expanded for switching mode operation. Inductive load generates higher peak energy at turnoff than its resistive counterpart. It is then possible to have a secondary breakdown failure if RBSOA is exceeded.

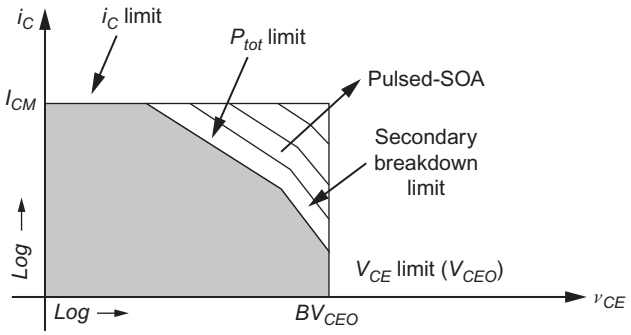


FIG. 2.24 Forward-bias safe operating area (FBSOA).

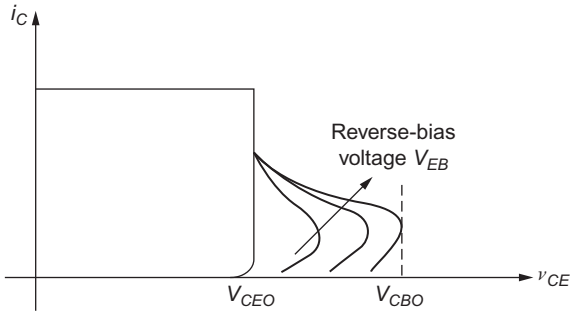


FIG. 2.25 Reverse-bias safe operating area (RBSOA).

A reverse base current helps the cutoff characteristics expanding RBSOA. The RBSOA curve shows that for voltages below V_{CEO}, the safe area is independent of reverse-bias voltage V_{EB} and is only limited by the device collector current, whereas above V_{CEO}, the collector current must be under control depending upon the applied reverse-bias voltage; in addition, temperature effects derate the SOA.

Ability for the transistor to switch high currents reliably is thus determined by its peak power handling capabilities. This ability is dependent upon the transistor's current and thermal density throughout the active region. In order to optimize the SOA capability, the current density and thermal density must be low. In general, it is a hot spot occurring at the weakest area of the transistor that will cause a device to fail due to second breakdown phenomenon. Although a wide base width will limit the current density across the base region, good heat sinking directly under the collector will enable the transistor to withstand high peak power. When the power and heat are spread over a large silicon area, these destructive tendencies are held to a minimum, and the transistor will have the highest SOA capability.

When the transistor is ON, one can ignore the base current losses and calculate the power dissipation on the ON state (conduction losses) by (2.5). Hard saturation minimizes collector-emitter voltage, decreasing on-state losses:

$$P_{ON} = I_C V_{CE(sat)} \tag{2.5}$$

2.2.4 Switching Characteristics

Switching characteristics are important to define the device commutation from conduction (ON) to blocking (OFF) states. Such transition is of paramount importance also because most of the losses are due to high-frequency switching. Fig. 2.26A presents the switching characteristics of a BJT under resistive load. Index "r" refers to the rising time (from 10 to 90% of maximum value); for example, t_{ri} is the current rise time. The falling time is indexed by "f"; the parameter t_f is the current falling time, that is, when the transistor is blocking such time corresponds to crossing from the saturation to the cutoff state. Fig. 2.26B presents operation points over the static characteristic curves. The thicker line indicates the trajectory of how the BJT passes through the cutoff region to the saturation region. Initially, the collector-emitter voltage is equal to VCC. At the end, the BJT is at the saturation region. The BJT passes through the active region in a linear manner.

In order to reduce t_f, the base current for blocking must be negative, and the device must be kept in quasi saturation to minimize the stored charges. The delay time is denoted by t_d, corresponding to the time to discharge the capacitance of base-emitter junction, which can be reduced with a larger current base with high slope. Storage time (t_s) is a very important parameter for BJT transistor. It is the required time to

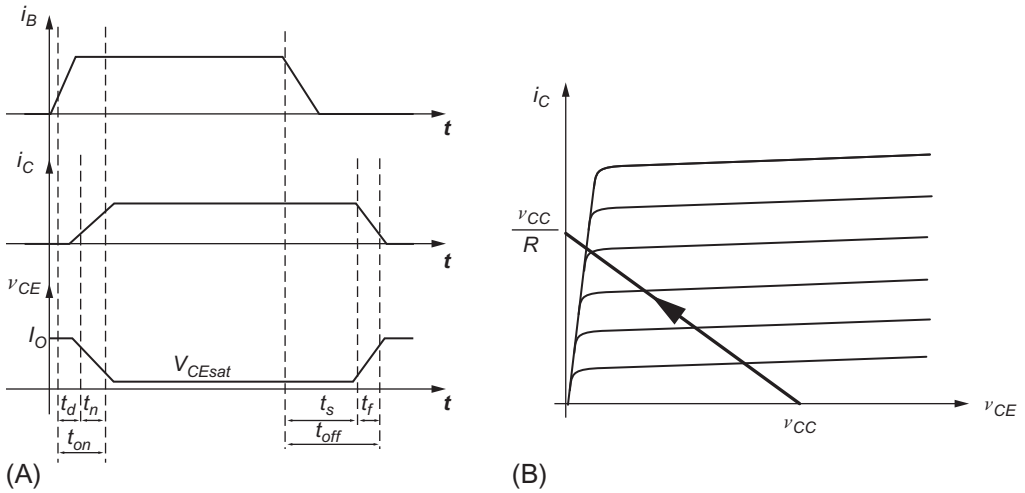


FIG. 2.26 (A) Switching characteristics of a BJT under resistive load and (B) the trajectory over the static characteristic curves under resistive load.

neutralize the minority carriers stored in the collector and base. Storage time and switching losses are key points to deal extensively with bipolar power transistors.

Fig. 2.27 presents switching characteristics of a BJT with inductive load. The waveforms slightly change compared with the previous case. The collector current presents overshoot due to the required reversed recover current of a diode connected across the inductive load. The power waveform is also shown in order to present how the power losses in a transistor. The losses are defined as switching losses and conduction losses. With inductive load, at turn-on, the collector-emitter voltage falls only after the collector current reaches the load current level. At the turnoff, the collector-emitter voltage varies quickly, allowing the collector current to start to decrease. Fig. 2.27B presents the trajectory over the static characteristic curves.

Most advantageous operation in BJT is achieved when fast transitions are optimized. Such requirement minimizes switching losses. Therefore, a good bipolar drive circuit highly influences the transistor performance. A base drive circuit should provide a high forward base drive current (I_{B1}) as indicated in Fig. 2.28 to ensure the power semiconductor turn-on quickly. Base drive current should keep the BJT close to the saturation to minimize forward conduction losses, but a level I_{B2} would maintain the transistor in a quasi-saturation condition, avoiding excess of charges in the base. Controllable slope and reverse current I_{BR} sweeps out stored charges in the transistor base, speeding up the device turnoff.

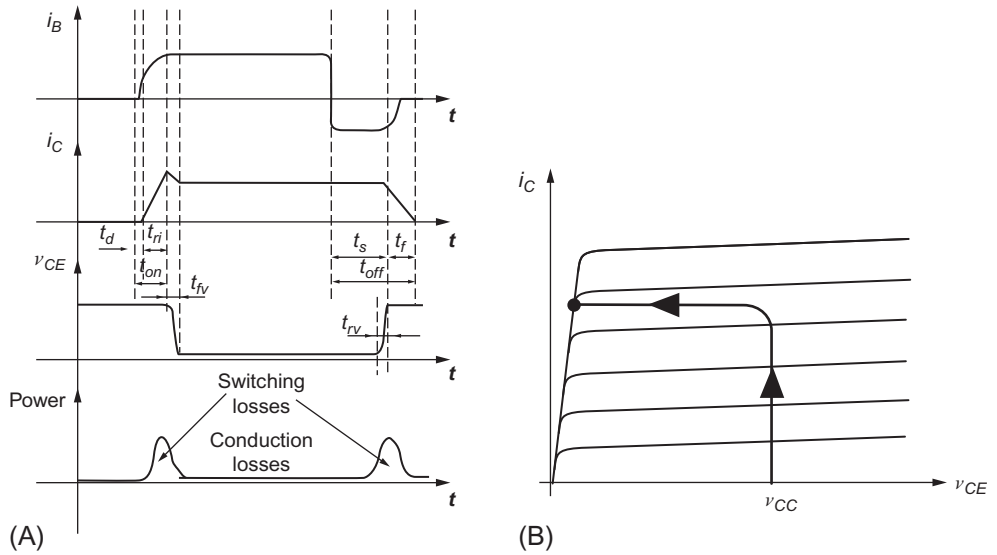


FIG. 2.27 (A) Switching characteristics of a BJT with inductive load and (B) the trajectory over the static characteristic curves under inductive load.

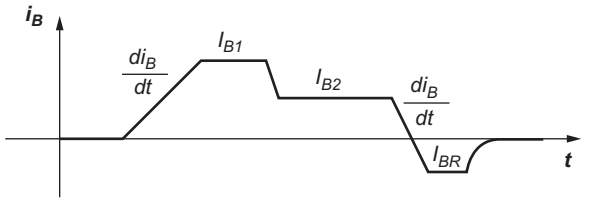


FIG. 2.28 Recommended base current for BJT driving.

2.2.5 Transistor Base Driver Circuits

Several circuits have been suggested to successfully command transistors for operating in power electronic switching systems. Such circuits try to satisfy the following requirements: supply the right collector current, adapt the base current to the collector current, and extract a reverse current from base to speed up the device blocking. A good base driver reduces the commutation times and total losses, increasing efficiency and operating frequency. Depending upon the grounding requirements between the control and the power circuits, the base drive might be isolated or nonisolated types. Fig. 2.29 shows a nonisolated circuit. When T_1 is switched on, T_2 is driven, and diode D_1 is forward-biased providing a reverse bias keeping T_3 off. The base current I_B is positive and saturates the power transistor T_P. When T_1 is switched off, T_3 switches on due to the negative path provided by R_3 and $-V_{CC}$, providing a negative current for switching off the power transistor T_P.

When a negative power supply is not provided for the base drive, a simple circuit like Fig. 2.30 can be used in low-power applications (low-power motors, small DC-DC converters, relays, and pulsed circuits). When the input signal is high, T_1 switches on, and a positive current goes to T_P keeping the capacitor charged with the zener voltage; when the input signal goes low, T_2 provides a path for the discharge of the capacitor,

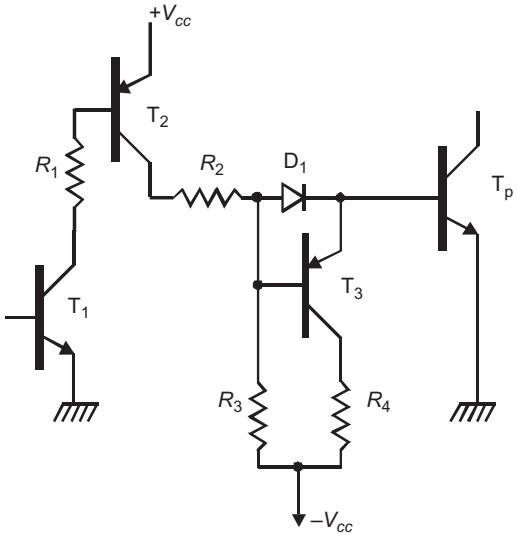


FIG. 2.29 Nonisolated base driver.

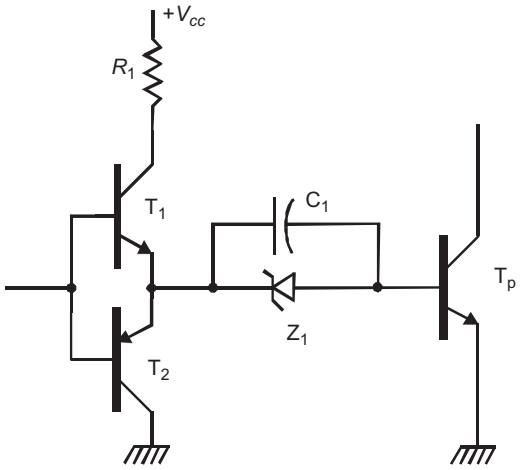


FIG. 2.30 Base command without negative power supply.

imposing a pulsed negative current from the base-emitter junction of T_P.

A combination of large reverse base drive and antisaturation techniques may be used to reduce storage time to almost zero. A circuit called Baker's clamp may be employed as illustrated in Fig. 2.31. When the transistor is on, its base is two diode drops below the input. Assuming that diodes D_2 and D_3 have a forward-bias voltage of about 0.7 V, then, the base will be 1.4 V below the input terminal. Due to diode D_1, the collector is one diode drop or 0.7 V below the input. Therefore, the collector will always be more positive than the base by 0.7 V, staying out of saturation, and because collector voltage increases, the gain β also increases a little bit. Diode D_4 provides a negative path for the reverse base current.

Several situations require ground isolation, off-line operation, and floating transistor topology. In addition, safety needs may call for an isolated base drive circuit. Numerous circuits

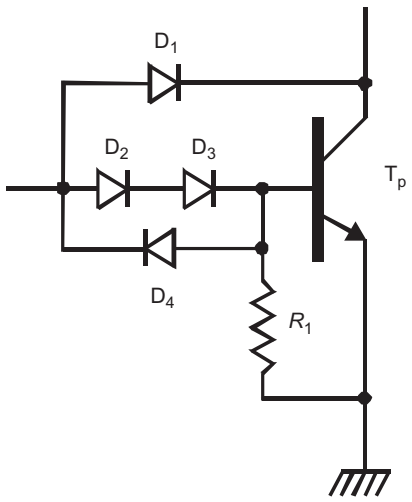


FIG. 2.31 Antisaturation diodes (Baker's clamp) improve power transistor storage time.

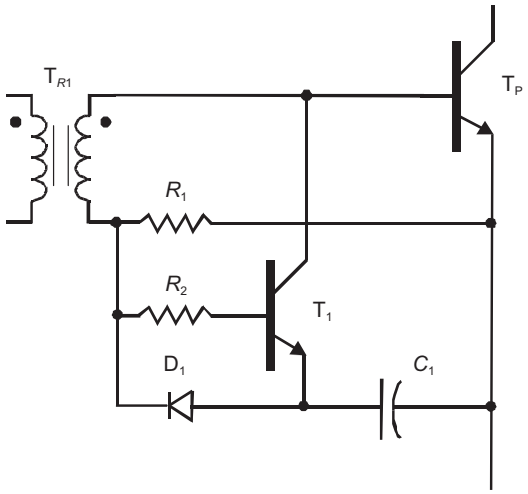


FIG. 2.32 Isolated base drive circuit.

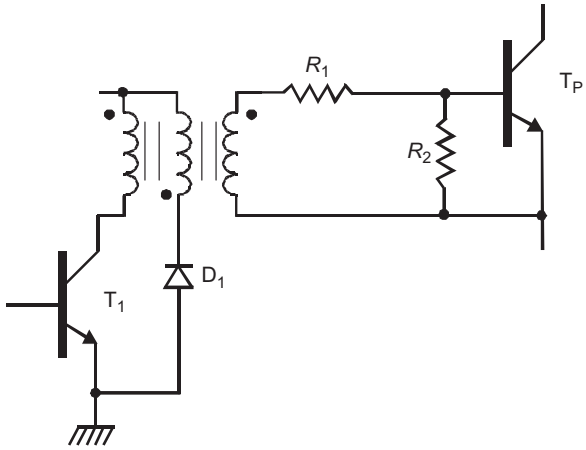


FIG. 2.33 Transformer-coupled base drive with tertiary winding transformer.

have been demonstrated in switching power supplies isolated topologies, usually integrating base drive requirements with their power transformers. Isolated base drive circuits may provide either constant current or proportional current excitation. A very popular base drive circuit for floating switching transistor is shown in Fig. 2.32. When a positive voltage is impressed on the secondary winding (V_S) of T_{R1}, a positive current flows into the base of the power transistor T_P, which switches on (resistor R_1 limits the base current). The capacitor C_1 is charged by $(V_S - V_{D1} - V_{BE})$, and T_1 is kept blocked because the diode D_1 reverse biases T_1 base-emitter. When V_S is zipped off, the capacitor voltage V_C brings the emitter of T_1 to a negative potential with respect to its base. Therefore, T_1 is excited so as to switch on and start pulling a reverse current from T_P base.

Another very effective circuit is shown in Fig. 2.33 with a minimum number of components. The base transformer has a tertiary winding that uses the energy stored in the transformer to generate the reverse base current during the turn-off command. Other configurations are also possible by adding to the isolated circuits the Baker clamp diodes or zener diodes with paralleled capacitors.

Sophisticated isolated base drive circuits can be used to provide proportional base drive currents where it is possible to control the value of β, keeping it constant for all collector currents leading to shorter storage time. Fig. 2.34 shows one of the possible ways to realize a proportional base drive circuit. When transistor T_1 turns on, the transformer T_{R1} is in negative saturation, and the power transistor T_P is off. During the time that T_1 is on, a current flows through winding N_1, limited by

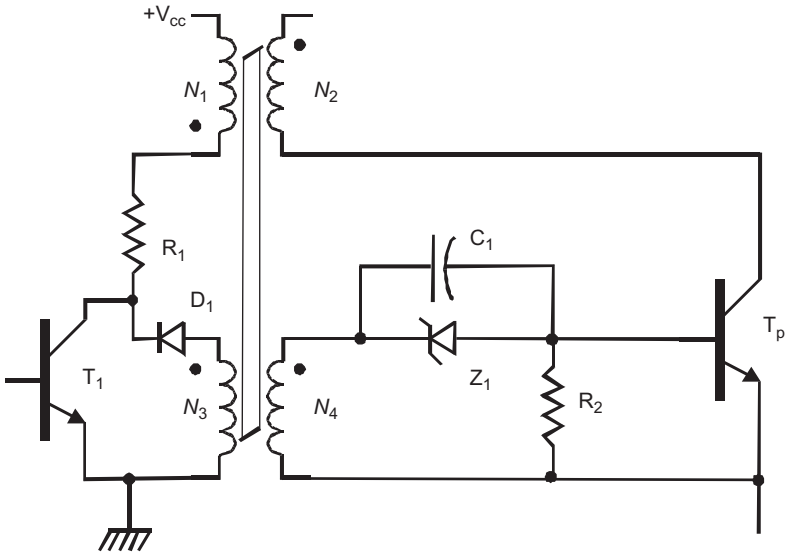


FIG. 2.34 Proportional base drive circuit.

resistor R_1, storing energy in the transformer and holding it into saturation. When the transistor T_1 turns off, the energy stored in N_1 is transferred to winding N_4, pulling the core from negative to positive saturation. The windings N_2 and N_4 will withstand as a current source, the transistor T_P will stay on, and the gain β will be imposed by the turn ratio given by (2.6):

$$\beta = \frac{N_4}{N_2} \tag{2.6}$$

In order to use the proportional drive given in Fig. 2.35, careful design of the transformer must be done, so as to have flux balanced, which will keep core under saturation. The transistor gain must be somewhat higher than the value imposed by the transformer turns ratio, which requires cautious device matching.

The most critical portion of the switching cycle occurs during transistor turnoff, since normally reverse base current is made very large in order to minimize storage time. Such conditions may avalanche the base-emitter junction leading to failure. There are two options to prevent this behavior: turning off the transistor at low values of collector-emitter voltage (which is not practical in most of the applications) or reducing collector current with rising collector voltage, implemented by *RC* protective networks called snubbers. Therefore, an *RC* snubber network can be used to divert the collector current during the turnoff, improving the RBSOA. In addition, the snubber circuit dissipates a fair amount of switching power relieving the transistor. Fig. 2.35 shows a turn-off snubber network. When the power transistor is off, the capacitor *C* is charged through diode D_1. Such collector current flows temporarily into the capacitor as the collector-voltage rises; as the power transistor turns on, the capacitor discharges through the resistor *R* back into the transistor.

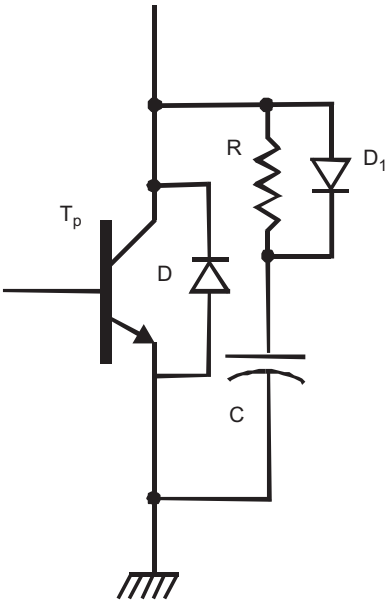


FIG. 2.35 Turn-off snubber network.

2.2.6 BJT Applications

Bipolar junction power transistors are applied to a variety of power electronic functions, switching mode power supplies, and motor drivers [8,9]. A buck-boost converter is exemplified in Fig. 2.36. The BJT operates in the cutoff and saturation regions. This converter can present a higher or lower voltage on its output terminal related to its input voltage source. This depends on the duty cycle of the BJT. The duty cycle is defined as the time a transistor keeps ON over a switching period. For duty cycles lower than 0.5, the buck-boost output voltage is lower than the input voltage. On the other hand, for duty cycles higher than 0.5, the output voltage is higher than the input voltage. The buck-boost converter has also a feature of presenting a contrary polarity on its output terminal related to the input voltage.

BJT are also commonly applied in chopper drivers. These circuits are connected between a fixed-voltage dc source and a dc motor to vary the armature voltage. In addition to armature voltage control, a dc chopper can provide regenerative braking of the motors and can return energy back to the supply. This energy-saving feature is attractive to transportation systems as mass rapid transit (MRT); chopper drives are also used in battery electric vehicles. A dc motor can be operated in one of the four quadrants by controlling the armature or field voltages (or currents). It is often required to reverse the armature or field terminals in order to operate the motor in the desired quadrant. Fig. 2.37 shows a circuit arrangement of a chopper-fed dc separately excited motor. By varying the duty cycle, the power flow to the motor (and speed) can be controlled.

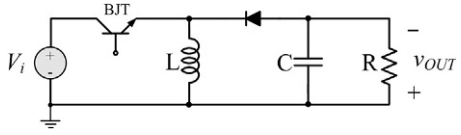


FIG. 2.36 Buck-boost converter with BJT.

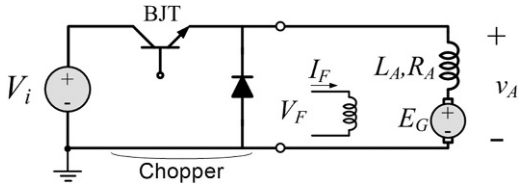


FIG. 2.37 Chopper driver with DC motor.

TABLE 2.2 Parameter definition of a BJT model

Parameter	Definition
IS	Saturation current
XTI	IS temperature effect exponent
EG	Bandgap voltage (barrier height)
VAF	Forward early voltage
BF	Ideal maximum forward beta
NE	Base-emitter leakage emission coefficient
ISE	Base-emitter leakage saturation current
IKF	Corner for forward beta high-current roll-off
XTB	Forward and reverse beta temperature coefficient
BR	Ideal maximum reverse beta
NC	Base-collector leakage emission coefficient
ISC	Base-collector leakage saturation current
IKR	Corner for reverse beta high-current roll-off
RC	Collector ohmic resistance
CJC	Base-collector zero-bias P–N capacitance
MJC	Base-collector P–N grading factor
VJC	Base-collector built-in potential
FC	Forward-bias depletion capacitor coefficient
CJE	Base-emitter zero-bias P–N capacitance
MJE	Base-emitter P–N grading factor
VJE	Base-emitter built-in potential
TR	Ideal reverse transit time
TF	Ideal forward transit time
ITF	Transit-time dependency on Ic
VTF	Transit-time dependency on Vbc
XTF	Transit-time bias dependence coefficient
RB	Zero-bias (maximum) base resistance

2.2.7 PSPICE Model

The PSPICE model for the BJT is based on the integral-charge model of Gummel and Poon. However, if the Gummel-Poon parameters are not specified, the model reduces to piecewise-linear Ebers-Moll model as depicted in the following text for the 2N2222A NPN transistor [2]:

```
.MODEL Q2N2222A NPN (IS=14.34F XTI=3 EG=1.11
VAF=74.03 BF=255.9 NE=1.307 ISE=14.34 F IKF=.2847
XTB=1.5 BR=6.092 NC=2 ISC=0 IKR=0 RC=1 CJC=7.306P
MJC=.3416 VJC=.75 FC=.5 CJE=22.01P MJE=.377 VJE=.75
TR=46.91 N TF=411.1P ITF=.6 VTF=1.7 XTF=3 RB=10)
```

In either case, charge-storage effects, ohmic resistances, and current-dependent output conductance may be included.

The definition of each parameter is given in Table 2.2 [4].

2.3 Power MOSFET

The MOSFET technology became available by the early 1980s. The novelty of MOSFET over the BJT was the fact that MOSFET uses only majority carriers in conduction and it is commanded by voltage signal instead of current, as in BJT. Additionally, the manner how the electric terminals are constructed presented a great advancement in producing high-speed transistors. Actually, power MOSFET can switch at around 1 MHz. All these features resulted in a different physical behavior of MOSFET compared with BJT [6,10].

2.3.1 Basic Structure

Fig. 2.38 presents a basic structure of a vertical N-channel MOSFET. The MOSFET has three terminals called drain (D), source (S), and gate (G). The gate terminal is isolated from the rest of the semiconductor by means of a SiO_2 layer. The PN junction represents a diode from source to drain terminals. This diode conducts when the drain-source voltage is negative. Additionally, this diode holds the reverse voltage applied to the MOSFET. The MOSFET operates as a transistor when the drain-source voltage is positive.

In case of a positive gate-source voltage, the gate potential repels the positive charges in the P regions and attracts free electrons. When such voltage reaches a threshold voltage, a complete path between source and drain is formed, called channel. This allows a current to be conducted through the drain and source. As the gate-source voltage increases, more carriers are attracted, and more current can be conducted. The carriers are only electrons in the N^+ source region along the channel and in the drain (N^+ and N^-) regions. Fig. 2.39 presents a vertical MOSFET with the N-channel created.

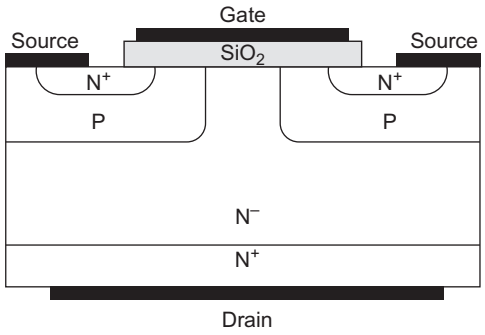


FIG. 2.38 Basic structure of a vertical N-channel MOSFET.

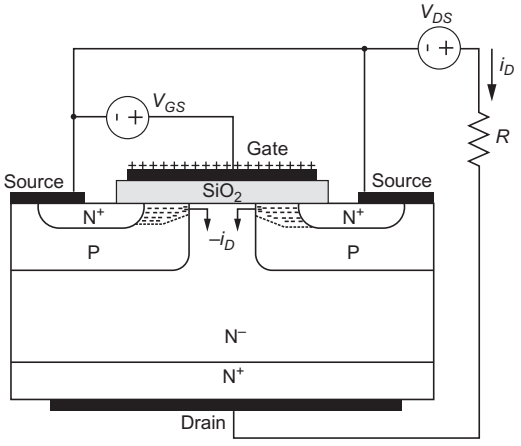


FIG. 2.39 Vertical MOSFET with the N-channel created.

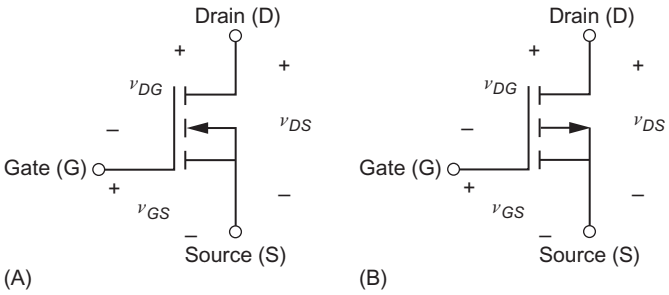


FIG. 2.40 MOSFET symbols for (A) N-channel and (B) P-channel types.

Fig. 2.40 presents the MOSFET symbols for P- and N-channel types. The voltages across the terminals are highlighted.

2.3.2 Static Characteristics

Fig. 2.41 presents the static characteristics of an N-channel MOSFET. The chart shows three regions of operation. In power electronic applications, the MOSFET is preferentially operated in the ohmic and cutoff regions, once either the drain-source voltage or the drain current is small, compared with the active region, thus reducing the power losses. In the active region, the MOSFET operates as an amplifier. *BV* is the breakdown voltage, which is the maximum allowable drain-source voltage across the MOSFET before failure.

2.3.2.1 Ohmic Region

In the ohmic region, also known as triode region or constant resistance region, the channel of the MOSFET behaves like a constant resistance. Such resistance is called R_{DSon}, and it is linearly proportional to drain-source voltage and the drain current. The value of R_{DSon} can vary from some milliohms (low-voltage device) to few ohms (high-voltage device). The manufactures usually inform the value of R_{DSon} on their datasheets. The value of R_{DSon}, together with the drain current, determines the conduction power losses of the MOSFET.

The MOSFET operates at the ohmic region when the constraint shown in (2.7) is satisfied:

$$v_{DS} < v_{GS} - V_{TH} \quad and \quad v_{GS} > V_{TH} \tag{2.7}$$

2.3.2.2 Cut-off Region

The cutoff region is characterized by the absence of the channel formation. This happens when the gate-source voltage is lower than the threshold voltage, as stated in (2.8):

$$v_{DS} > 0 \quad and \quad v_{GS} < V_{TH} \tag{2.8}$$

In this case, no current flows through the drain and source terminals of the MOSFET.

2.3.2.3 Active Region

The active region is also known as saturation region in MOSFETs. However, naming it as saturation region may be misunderstood as the saturation region of BJT. Therefore, throughout this chapter, the name active region is used.

The active region is characterized by a constant drain current, controlled by the gate-source voltage. The MOSFET operates at the active region when the constraint stated in (2.9) is satisfied. In this case, the channel width limits the current flow:

$$v_{DS} > v_{GS} - V_{TH} \quad and \quad v_{GS} > V_{TH} \tag{2.9}$$

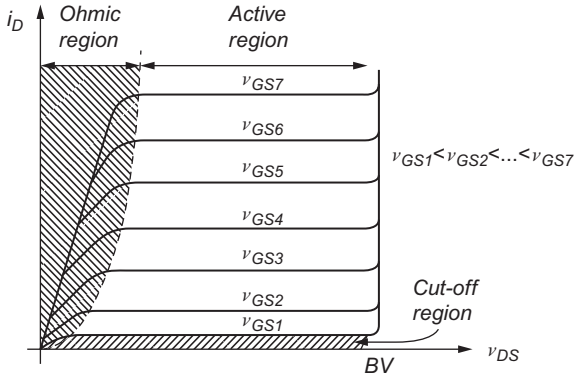


FIG. 2.41 Static characteristics for an N-channel enhancement-type MOSFET.

2.3.3 Switching Characteristics

In order to understand the switching characteristics, the MOSFET is represented by an equivalent circuit model shown in Fig. 2.42. The model consists of a voltage-controlled current source and internal capacitances located among the MOSFET terminals.

The internal capacitances are the gate-drain capacitance C_{GD}, the gate-source capacitance C_{GS}, and the drain-

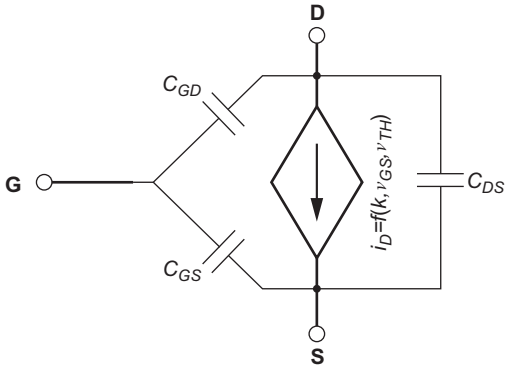


FIG. 2.42 Equivalent circuit model for a MOSFET.

sourcecapacitance C_{DS}. These are nonlinear capacitances that vary according to the MOSFET structure and bias voltage.

The voltage-controlled current source is mathematically approximated by (2.10):

$$\begin{cases} i_D = k\left[2(v_{GS} - V_{TH})v_{DS} - {v_{DS}}^2\right] & \textit{for ohmic region} \\ i_D = k(v_{GS} - V_{TH})^2 & \textit{for active region} \\ i_D = 0 & \textit{for cut} - \textit{off region} \end{cases} \quad (2.10)$$

where k is a constant that depends on the MOSFET construction.

From (2.7) to (2.9), the drain-to-source voltage at the boundary between the active and ohmic region is given by (2.11):

$$v_{DS} = v_{GS} - V_{TH} \quad (2.11)$$

Therefore, (2.10) results in (2.12):

$$i_D = k{v_{DS}}^2 \quad (2.12)$$

From (2.12), the MOSFET input transfer characteristic can be obtained. Fig. 2.43 presents the input transfer function characteristics, valid for the active region. G_m is the slope for an operation point with a v_{GS} voltage and i_D current.

In the ohmic region, the MOSFET can be represented by the circuit shown in Fig. 2.44.

2.3.3.1 Turn-on Analysis

The circuit used to analyze the turn-on and turn-off characteristics of a MOSFET is shown in Fig. 2.45. The circuit contains a DC source (+Vcc), a MOSFET, an inductor (L), a resistor (R), a diode (D), and the gate driver, which is composed of the voltage source V_g and the resistor R_G. The diode is considered ideal (without reverse recovery behavior). The inductor is the load of the circuit. Its inductance value is large enough so that the current thought it is considered constant. The diode is used to supply a path for the load current when the MOSFET is off.

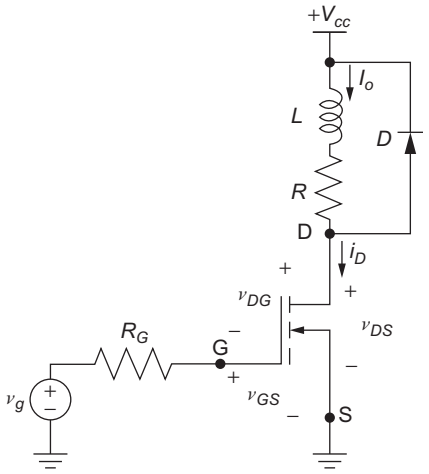


FIG. 2.45 Circuit used to analyze the turn-on and turn-off characteristics of a MOSFET.

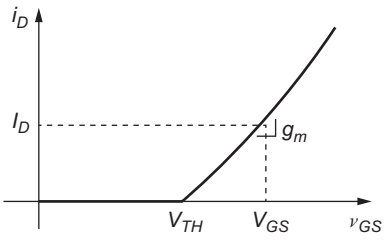


FIG. 2.43 Input transfer function characteristics for a MOSFET.

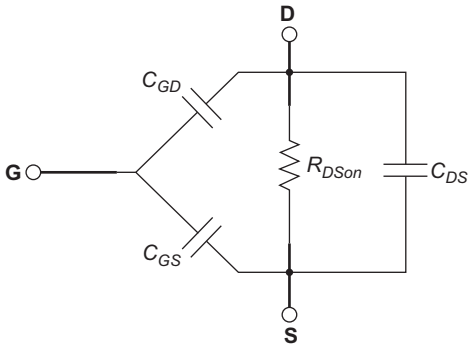


FIG. 2.44 Equivalent circuit valid for the ohmic region.

Fig. 2.46 presents waveforms during the turn-on. The x-axis is divided into four intervals, as follows:

Initially, the MOSFET is in the cutoff region. Thus, the drain current is null, and the drain-to-source voltage is equal to the +Vcc. This makes the gate-drain capacitance to be charged. The interval t_1 begins with the voltage source V_G going from zero to its nominal value. The gate-source capacitance begins to be charged through the resistor R_G, while the gate-drain capacitance begins to be discharged. The drain current keeps null until the gate-to-source voltage reaches the threshold voltage. The time interval t_1 ends when the gate-source voltage

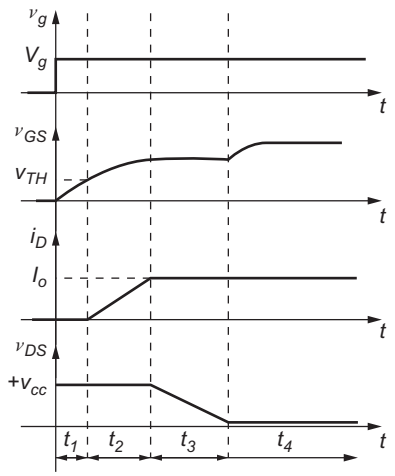


FIG. 2.46 Waveforms during the turn-on process.

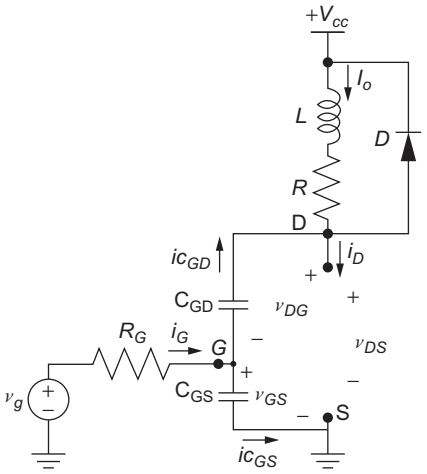


FIG. 2.47 Equivalent circuit for the interval t_1.

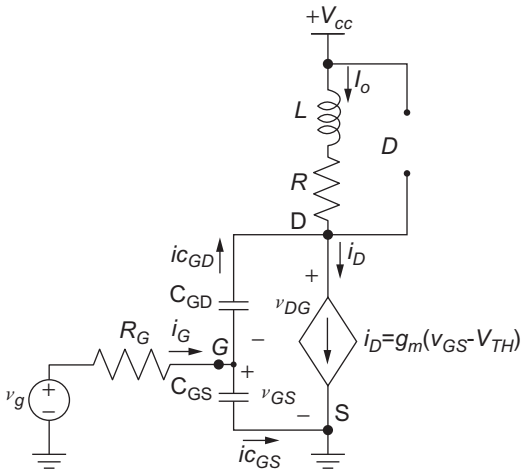


FIG. 2.49 Equivalent circuit for the interval t_3.

reaches the threshold voltage. Once the MOSFET leaves the cutoff region at this moment, the interval t_1 represents the turn-on delay time. Fig. 2.47 presents the equivalent circuit for the time interval t_1. Since the diode is ON, the drain-source voltage does not change.

At the beginning of the interval t_2, the gate-source voltage is higher than the threshold voltage, and the MOSFET starts conducting. The diode keeps conducting, while the drain current is lower than I_o. The gate-source voltage remains growing, while the drain-source voltage keeps unchanged. Fig. 2.48 presents the equivalent circuit for the time interval t_2. The diode was replaced by a short circuit in order to emphasize its conduction state.

The interval t_3 begins when the load current is conducted entirely through the MOSFET ($i_D = I_o$), turning off the diode. The drain-source voltage falls throughout this interval, reaching its minimum value at the end. The gate-drain capacitance is discharged by the gate current. Its voltage varies together with the drain-source voltage. Fig. 2.49 shows the equivalent circuit for the time interval t_3. The diode was replaced by an open circuit.

The interval t_4 begins when the drain-source voltage reaches its minimum value, which is given by (2.13):

$$v_{DS} = I_o R_{DSon} \tag{2.13}$$

The gate current finishes charging the gate-source capacitance, the gate-source voltages reaches its nominal value, and the MOSFET entered into the ohmic region. Fig. 2.50 presents the equivalent circuit for the time interval t_4.

During intervals t_2 and t_3, the MOSFET is passing through the active region with considerable drain-source voltage and drain current. As a result, power dissipation occurs during these intervals, contributing to the switching losses.

2.3.3.2 Turn-off Analysis

In order to analyze the turn-off characteristic, the same circuit shown in Fig. 2.45 was adopted. The MOSFET is initially

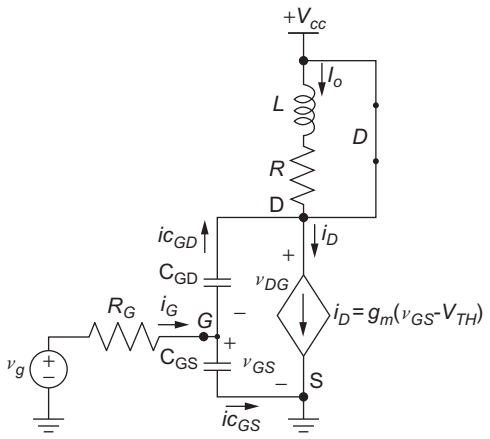


FIG. 2.48 Equivalent circuit for the interval t_2.

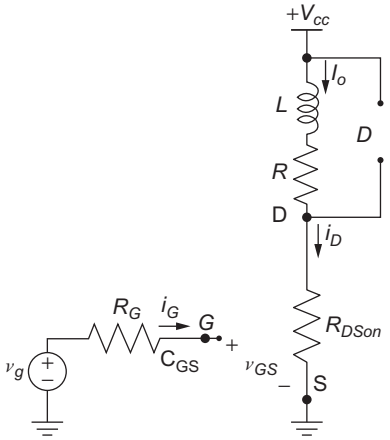


FIG. 2.50 Equivalent circuit for the interval t_4.

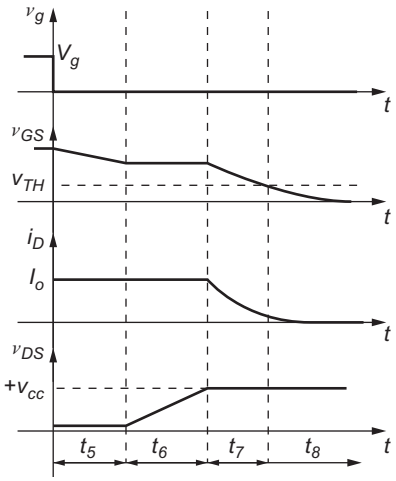


FIG. 2.51 Waveforms during the turn-off process.

considered in the ohmic region with the values shown in the waveform of Fig. 2.46. Fig. 2.51 presents the waveforms during the turn-off switching.

The turnoff of the MOSFET begins when the source Vg is set to zero (a negative voltage is also possible). During interval t_5, the gate-source voltage begins to fall, discharging the gate-source capacitance and charging the gate-drain capacitance. The drain current and the drain-source voltage keep unchanged.

During interval t_6, the drain-source voltage rises, while the gate-source voltage keeps constant. At the end of interval t_6, the drain-source voltage reaches the value of the DC source (+Vcc), turning on the diode, and the drain current begins to fall.

The interval t_7 corresponds to the time required to the gate-source voltage to reach the threshold voltage. After that, the drain current is null, and the MOSFET is in the cutoff region.

Similarly to the turn-on behavior, the intervals t_6 and t_7 present considerable drain current and drain-source voltage, contributing to the switching losses.

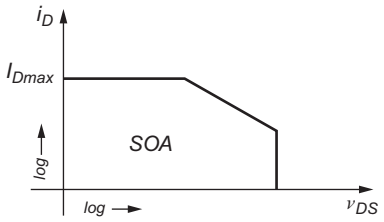


FIG. 2.52 Safe operation area of the MOSFET.

2.3.4 Safe Operation Area

The SOA of the MOSFET is shown in Fig. 2.52. The area SOA shows the values of drain current, and drain-source voltage can hold without destructive failure. MOSFETs do not present the second breakdown.

2.3.5 MOSFET Applications

The majority of applications of BJT can also be employed with MOSFET, especially those in DC–DC converters. Nevertheless, MOSFETs have been widely used in the field of electric vehicles [11]. Fig. 2.53 presents a typical bidirectional DC charger for electric vehicles using MOSFETs. The left side of the high-frequency transformer is the charger. The right side is the battery and the converter of the electric vehicle.

2.3.6 PSPICE Model

The following text presents the PSPICE model for the MOSFET IRFBC30:

```
.Model IRFBC30 NMOS(Level=3 Gamma=0 Delta=0 Eta=0
Theta=0 Kappa=0.2 Vmax=0 Xj=0 + Tox=100n Uo=600 Phi=.6
Rs=5.002m Kp=20.43u
W=.35 L=2u Vto=3.625 + Rd=1.851 Rds=2.667MEG Cbd=790.1p
Pb=.8 Mj=.5
Fc=.5 Cgso=1.64n + Cgdo=123.9p Rg=1.052 Is=720.2p N=1
Tt=685)
```

The definition of each parameter is given in Table 2.3 [4].

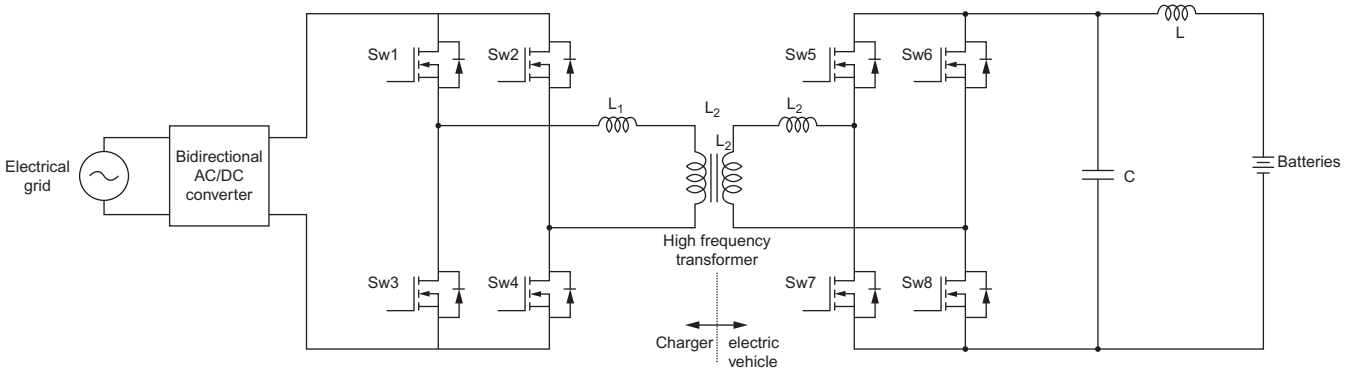


FIG. 2.53 Typical bidirectional DC charger for electric vehicles using MOSFET.

TABLE 2.3 Parameter definition of a MOSFET model

Parameter	Definition
Level	Model type (1, 2, or 3)
Gamma	Bulk threshold parameter
Delta	Width effect on threshold
Eta	Static feedback (LEVEL = 3)
Kappa	Saturation field factor (LEVEL = 3)
Vmax	Maximum drift velocity
Xj	Metallurgical junction depth
Tox	Oxide thickness
Uo	Surface mobility
Phi	Surface potential
R_s	Source ohmic resistance
K_p	Transconductance
W	Channel width
L	Channel length
V_{to}	Zero-bias threshold voltage
R_d	Drain ohmic resistance
R_{ds}	Drain-source shunt resistance
C_{bd}	Bulk-drain zero-bias P–N capacitance
P_b	Bulk P–N potential
Mj	Bulk P–N bottom grading coefficient
Fc	Bulk P–N forward-bias capacitance coefficient
Cgso	Gate-source overlap capacitance/channel width
Cgdo	Gate-drain overlap capacitance/channel width
Rg	Gate ohmic resistance
IS	Bulk P–N saturation current
N	Bulk emission coefficient n
T_t	Transit time

2.4 Insulated Gate Bipolar Transistor

The IGBT is a device that integrates the advantage of having low on-voltage from BJT with the advantage of having an insulated-gate input from MOSFET. Such integration makes the IGBT a device with some superior characteristics compared with the BJT or MOSFET, with relative high switching speed. The IGBT can be gated like a MOSFET, and the output current is handled in a manner similar to the BJT. IGBTs do not have the body diode found in MOSFET. Thus, an external fast recovery diode is usually mounted in the same package for holding high reverse voltage.

2.4.1 Basic Structure

Fig. 2.54 presents a basic structure of a vertical IGBT. The IGBT has three terminal called collector (C), emitter (E), and gate (G). The gate terminal is isolated from the rest of the semiconductor by means of a SiO_2 layer. The P+, N+N−, and P junctions constitute a parasitic BJT. By the application of a positive voltage higher than the threshold between the gate and emitter, the N-channel is created, similar to MOSFET, providing a path for a current from the collector to the emitter terminal. As the junctions P+N+ are forward-biased, it injects carriers into the N region, enhancing the conductivity and reducing the voltage drop along this region. This is the main

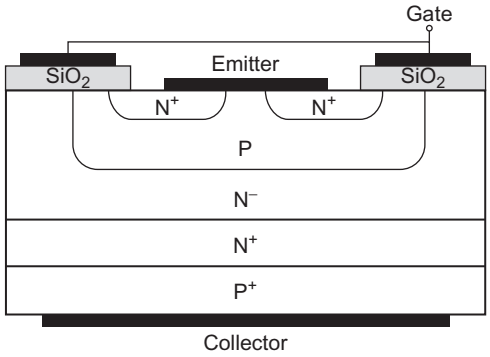


FIG. 2.54 Basic structure of a vertical IGBT.

difference between IGBT and MOSFET. The PN junction blocks reverse voltage when the IGBT is off. In spite of P-channel be possible, as its commutation intrinsically slower than N-channel, it is not convenient for power applications.

Fig. 2.55 presents the symbol for an N-channel type IGBT. The symbol is similar to a BJT, except that the gate terminal is insulated from the rest of the device. Other symbols for IGBT can be found in the literature.

2.4.2 Static Characteristics

Fig. 2.56 presents the static characteristic of an N-channel IGBT. The curves are similar to that for BJT, except that the

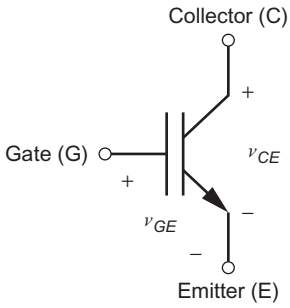


FIG. 2.55 Symbol for an N-channel type IGBT.

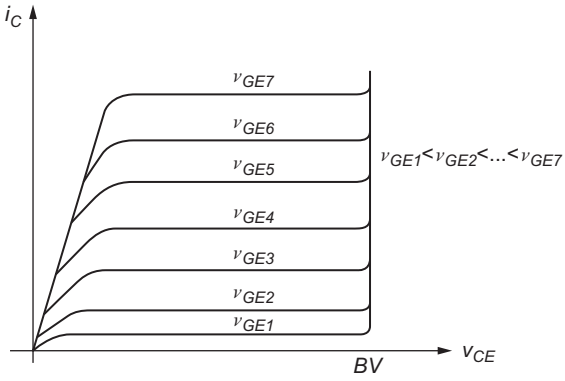


FIG. 2.56 Static characteristics of an N-channel IGBT.

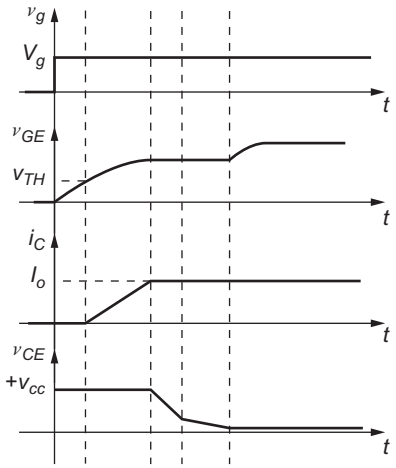


FIG. 2.57 Waveforms during the turn-on process of an IGBT.

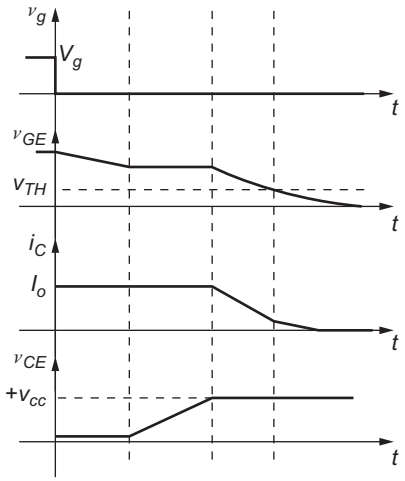


FIG. 2.58 Waveforms during the turn-off process of an IGBT.

controlling variable is the gate-emitter voltage. *BV* is the breakdown voltage.

2.4.3 Switching Characteristics

2.4.3.1 Turn-on Analysis

The turn-on process of IGBT is similar to that for MOSFET, once the IGBT has the insulated-gate terminal. However, the v_{CE} typically falls slower compared with a MOSFET with the same ratings. Fig. 2.57 presents the waveforms during the turn-on process of an IGBT. The circuit used to analyze these waveforms is that shown in Fig. 2.43, except that the MOSFET is replaced by an IGBT.

2.4.3.2 Turn-off Analysis

The turn-off process of IGBT depends on the removal of carriers that came from the P+ region. Since IGBT has insulated gate, such removal cannot be made through the gate terminal. The solution is the inclusion of the N+ layer, which the recombination tax is faster than the N-layer. By diffusion, the storage charges in the N-layer are extinguished, reestablishing the potential barrier. Fig. 2.58 presents the waveforms during the turn-off process of an IGBT.

2.4.4 IGBT Applications

IGBTs have a vast field of application. One of the most relevant is in DC-AC converters, known also as inverters. Such inverters are usually applied in uninterrupted power supplies, motor drivers, and grid interfaces for connecting renewable sources into the distribution/transmission systems [1,3,8,11]. Fig. 2.59 presents a single-phase inverter using IGBTs with LC filter. The inverter has a DC source as input. The terminals A and B are the output of the inverter. The inductor and capacitor are used to filter the high-frequency components of the inverter output voltage. When an induction motor is used as load, the LC filter can be removed, since the motor windings work as filter for the current.

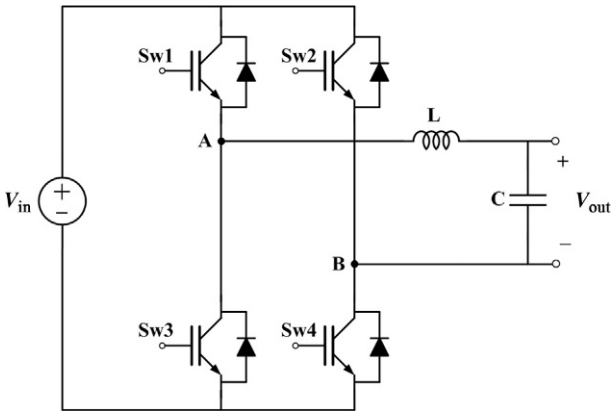


FIG. 2.59 Single-phase inverter using IGBTs with LC filter.

Another field of application of IGBT-based inverters is in power quality improvements. Fig. 2.60 presents a unified power quality conditioner (UPQC) [12] with electronic converters using IGBTs. The UPQC is composed of series and shunt active filters. The first is used to filter the voltage applied to the load, while the second is used to filter the harmonic current produced by the load.

2.4.5 PSPICE Model

The following text presents the PSPICE model for the IGBT IXGT32N170A:

```
.MODEL IXGT32N170A NIGBT (+ TAU=63.552E-9 + KP=14.397 +
AREA=16.000E-6 + AGD=6.4000E-6 + WB=117.00E-6 +
VT=5.3804 + MUN=1.0000E6 + MUP=150 + BVF=9.9990 +
KF=.5005 + CGS=38.737E-9 + COXD=88.530E-9 + VTD=-5)
```

The definition of each parameter is given in Table 2.4 [4].

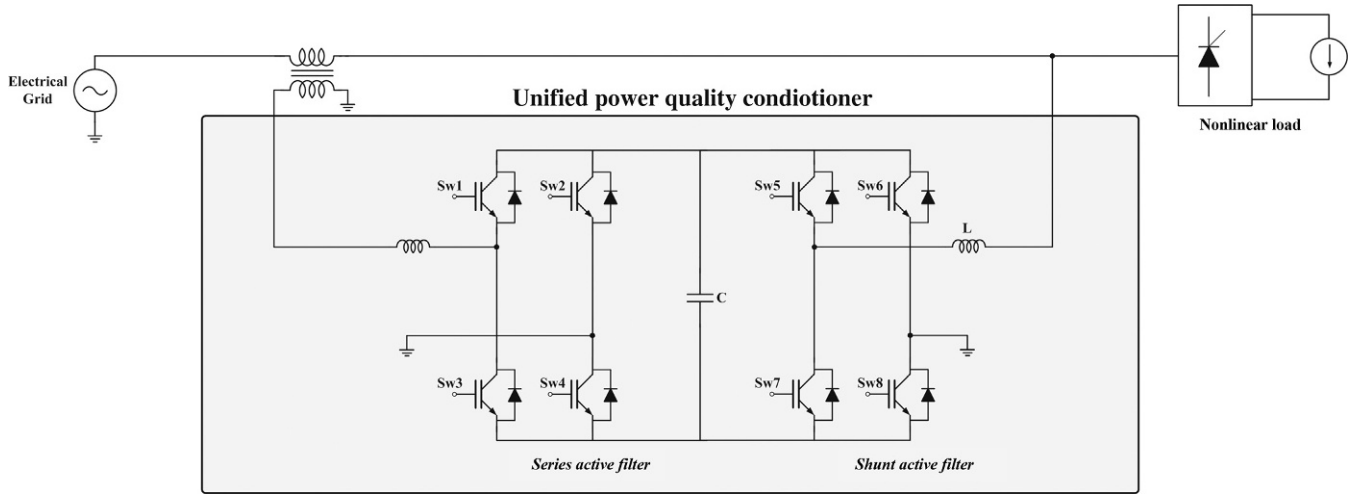


FIG. 2.60 Unified power quality conditioner (UPQC) with electronics converters using IGBTs.

TABLE 2.4 2.4 Parameter definition of a IGBT model

Parameter	Definition
TAU	Ambipolar recombination lifetime
KP	MOS transconductance
AREA	Area of the device
AGD	Gate-drain overlap area
WB	Metallurgical base width
VT	Threshold voltage
MUN	Electron mobility
MUP	Hole mobility
BVF	Avalanche uniformity factor
KF	Triode region factor
CGS	Gate-source capacitance
COXD	Gate-drain overlap oxide capacitance
VTD	Gate-drain overlap depletion threshold

2.5 Swtiching evaluation of a Real MOSFET

In order to verify real switching characteristics of a MOSFET, the circuit shown in Fig. 2.61 was built. The MOSFET is connected to a circuit composed of the main source (Vcc) and an *RL* load. The switch Sw1 is used to insert or remove the inductance of the load. The diode *D* is used as freewheeling path for the load. The gate driver is composed of a square-wave source (V_g), a resistor, a potentiometer, a capacitor, and a switch Sw2, used to insert or remove the capacitor. The potentiometer can vary from 0 to 1 k**Ω**. The MOSFET is the IRF530.

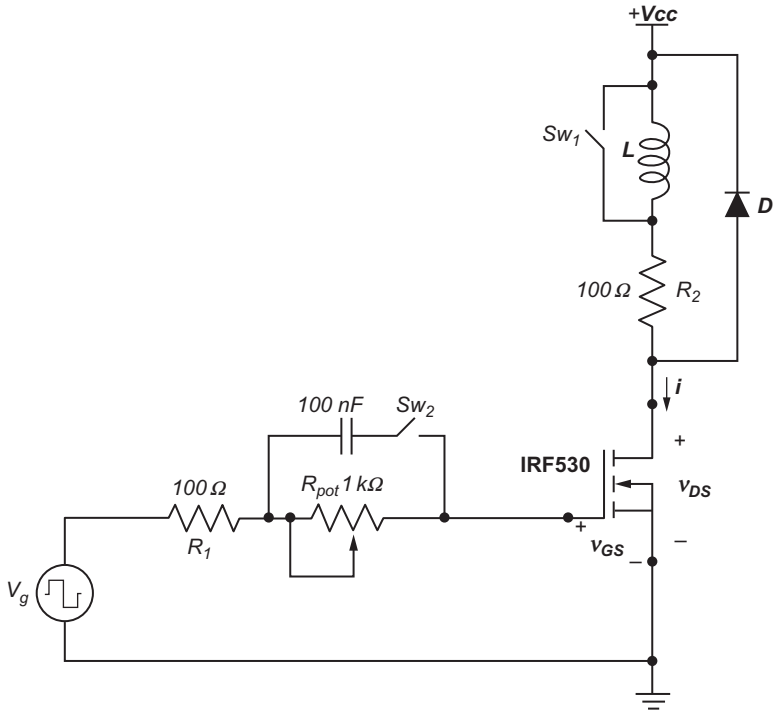


FIG. 2.61 Circuit used to verify real switching characteristics of transistors.

2.5.1 Results for Sw1 ON and Sw2 OFF and *Rpot* at the Maximum Resistance

The switch Sw1 is ON, bypassing the inductor *L*. The switch Sw2 is OFF, disconnecting the capacitor of the gate driver. The R_{pot} is at its maximum resistance. Fig. 2.62 presents waveforms for V_g source and the drain-source voltage. The V_g source goes from −3 to +10 V with frequency equal to 5 kHz.

Fig. 2.63 presents details of the turn-on process. The V_g source changes from −3 to 10 V almost instantaneously. The turn-on delay of the MOSFET is measured from the moment where the V_g source begins to rise until the drain-source voltage begins to fall. Therefore, the turn-on delay for the MOSFET is 0.7 µs.

Fig. 2.64 presents details of the turn-off process. Similarly, the V_g source changes almost instantaneously from +10 to −3 V, and the turn-off delay is measured from the moment the V_g source begins to fall until the moment the drain-source voltage begins to rise. The turn-off delay for the MOSFET is 1.5 µs.

Fig. 2.65 presents the drain-source voltage and the gate-source voltage during the turn-on process. The threshold voltage of the MOSFET is evident. As soon as the threshold is achieved, the drain-source voltage begins to fall.

Fig. 2.66 presents the drain-source voltage and the gate-source voltage during the turn-off process.

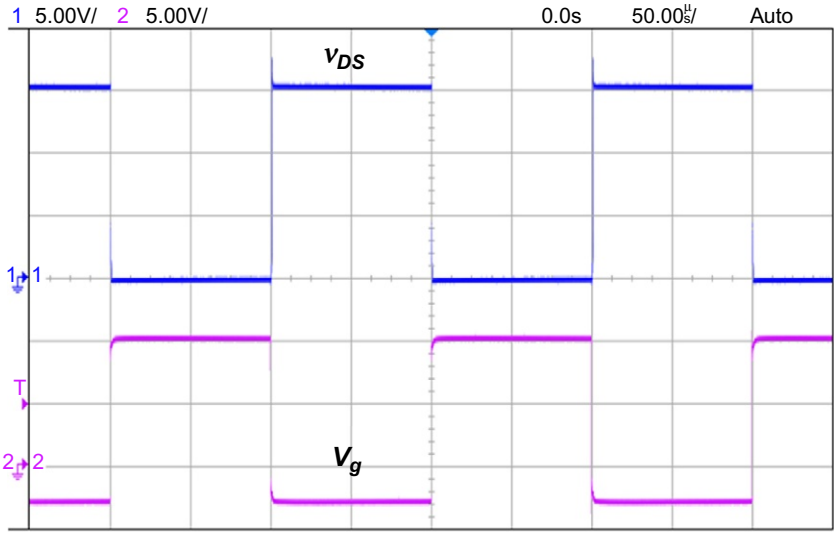


FIG. 2.62 Waveforms for Vg source and the drain-source voltage.

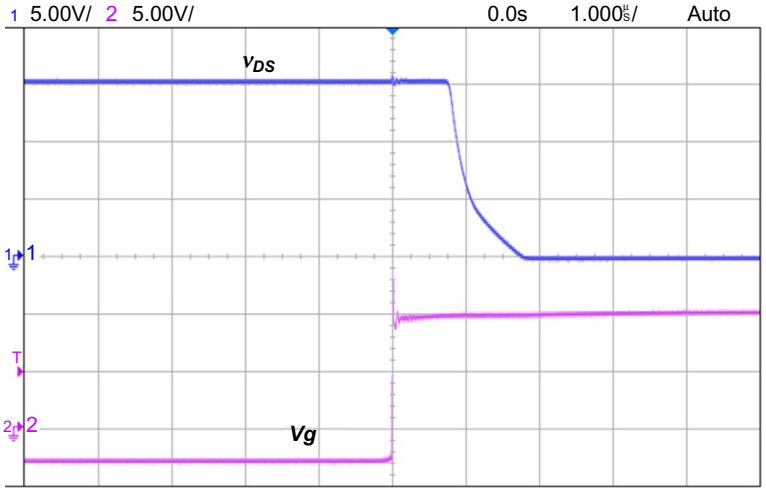


FIG. 2.63 Details of the turn-on process for Sw1 ON and Sw2 OFF and *Rpot* at the maximum resistance.

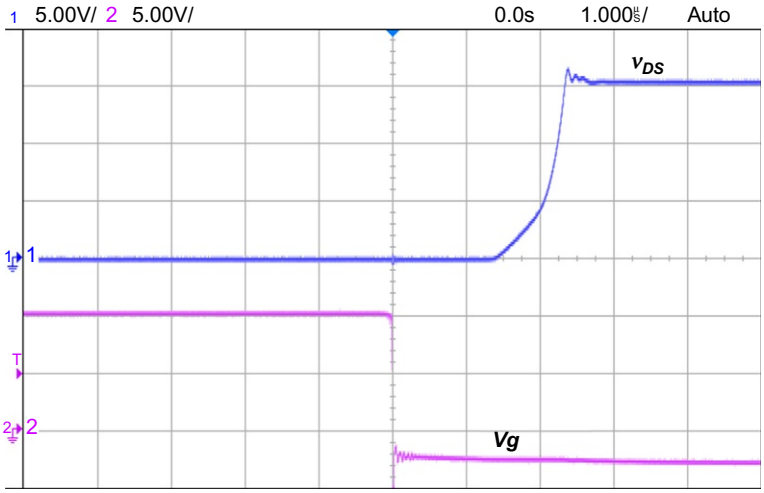


FIG. 2.64 Details of turn-off process for Sw1 ON and Sw2 OFF and *Rpot* at the maximum resistance.

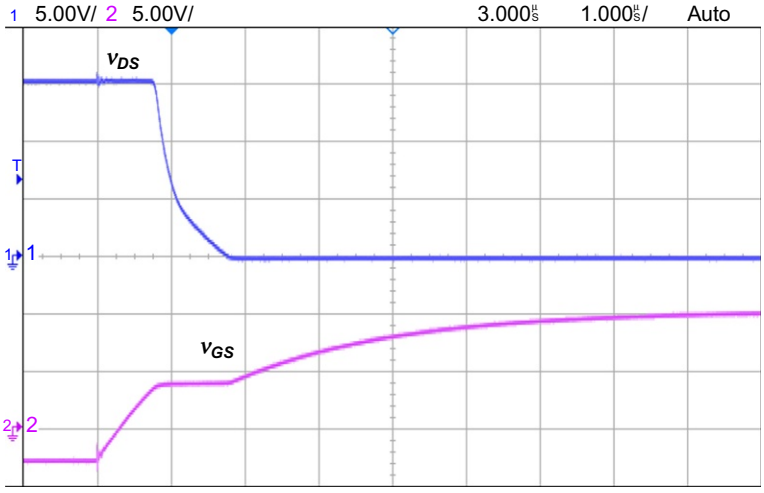


FIG. 2.65 Drain-source voltage and the gate-source voltage during the turn-on process for Sw1 ON and Sw2 OFF and *Rpot* at the maximum resistance.

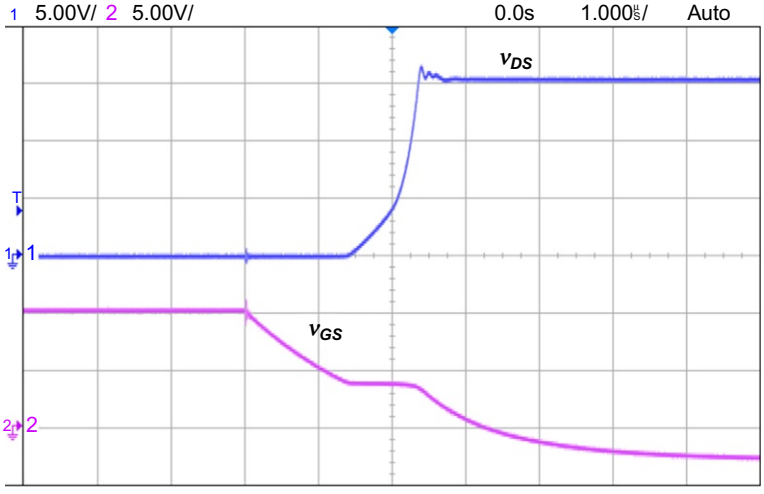


FIG. 2.66 Drain-source voltage and the gate-source during the turn-off process for Sw1 ON and Sw2 OFF and R_{pot} at the maximum resistance.

2.5.2 Results for Sw1 ON and Sw2 OFF and *Rpot* at the Minimum Resistance

The R_{pot} is set to its minimum resistance (0 Ω). Fig. 2.67 presents the details of the turn-on process. The turn-on delay of the MOSFET is approximately 0.15 µs. The delay is lower compared with the previous case. Since the R_{pot} is at its minimum resistance, the gate-driver resistance is made only by R_1, resulting in a lower time constant for charging the MOSFET capacitance. Consequently, the turn-on process is faster.

Fig. 2.68 presents the details of the turn-off process. The turn-off delay of the MOSFET is 0.3 µs.

Fig. 2.69 presents the drain-source voltage and the gate-source voltage during the turn-on process.

Fig. 2.70 presents the drain-source voltage and the gate-source voltage during the turn-off process.

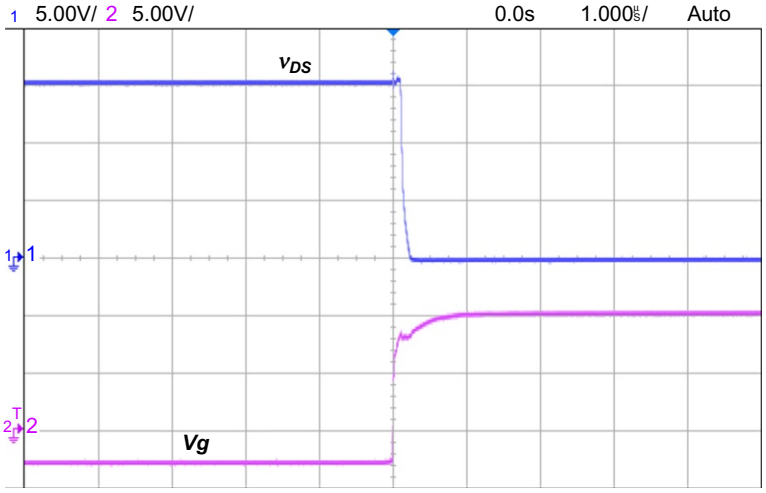


FIG. 2.67 Details of turn-on process for Sw1 ON and Sw5 OFF and *Rpot* at the minimum resistance.

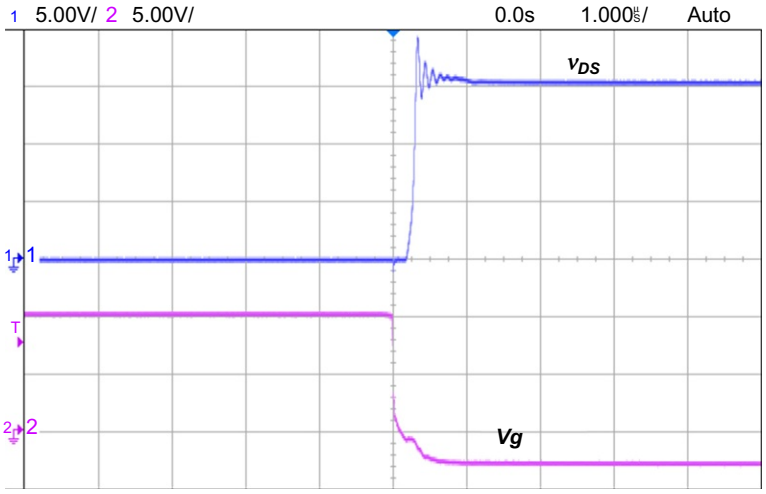


FIG. 2.68 Details of turn-off process for Sw1 ON and Sw5 OFF and R_{pot} at the minimum resistance.

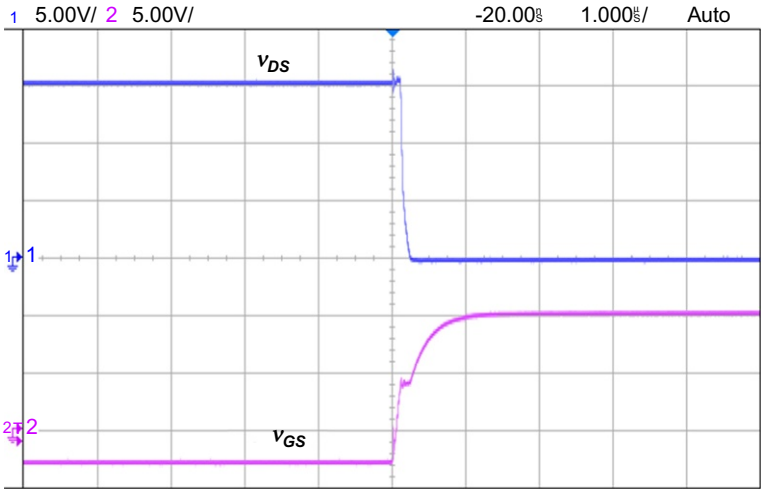


FIG. 2.69 Drain-source voltage and the gate-source voltage during the turn-on process for Sw1 ON and Sw2 OFF and R_{pot} at the maximum resistance.

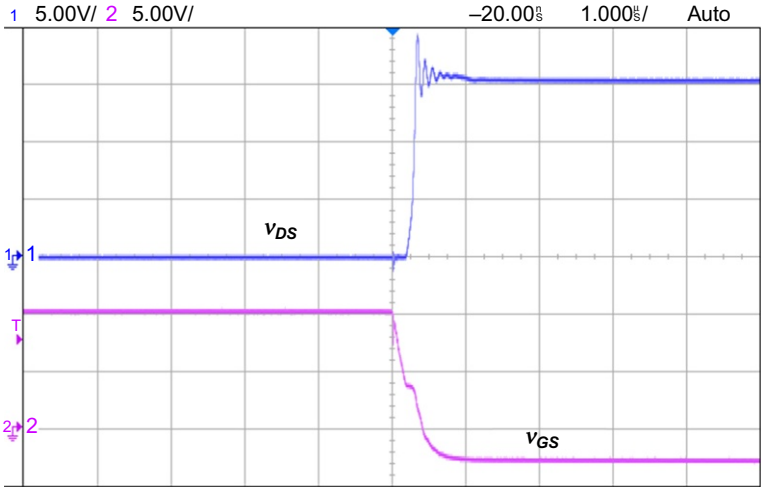


FIG. 2.70 Drain-source voltage and the gate-source during the turn-off process for Sw1 ON and Sw2 OFF and R_{pot} at the maximum resistance.

2.5.3 Results for Sw1 and Sw2 ON and *Rpot* at the Maximum Resistance

The switch Sw2 is now ON, connecting the capacitor to the gate driver. Fig. 2.71 presents the details of the turn-on process. The turn-on delay of the MOSFET is approximately 100 ns. The inclusion of the capacitor makes the transistor faster due to the fact that at initial turn-on process, the capacitor is seen as a short circuit by the voltage source. Thus, the gate current goes through it and charges faster the MOSFET capacitance. As soon as the capacitor is charged, the gate current passes through the potentiometer.

Fig. 2.72 presents the details of the turn-off process. The turn-off of the MOSFET is 200 ns.

2.5.4 Results for Sw1 and Sw2 OFF and *Rpot* at the Maximum Resistance

The switches Sw1 and Sw2 are OFF. The inductor now has effect on the circuit. Fig. 2.73 presents the load current (drain

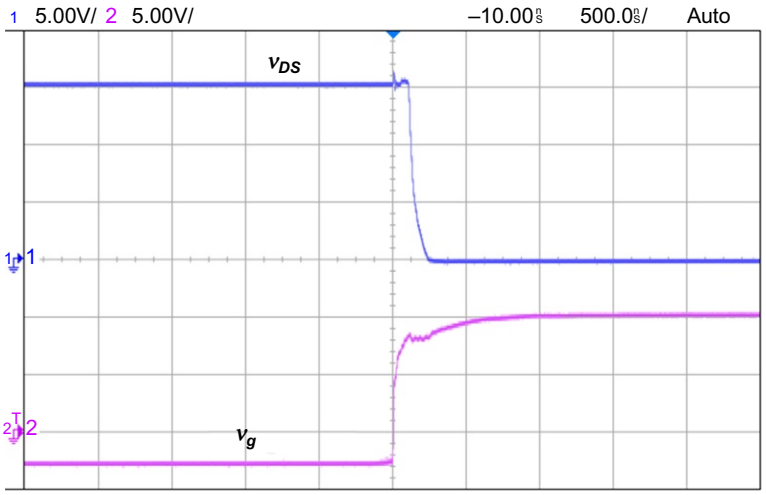


FIG. 2.71 Details of turn-on process for Sw1 and Sw2 ON and *Rpot* at the maximum resistance.

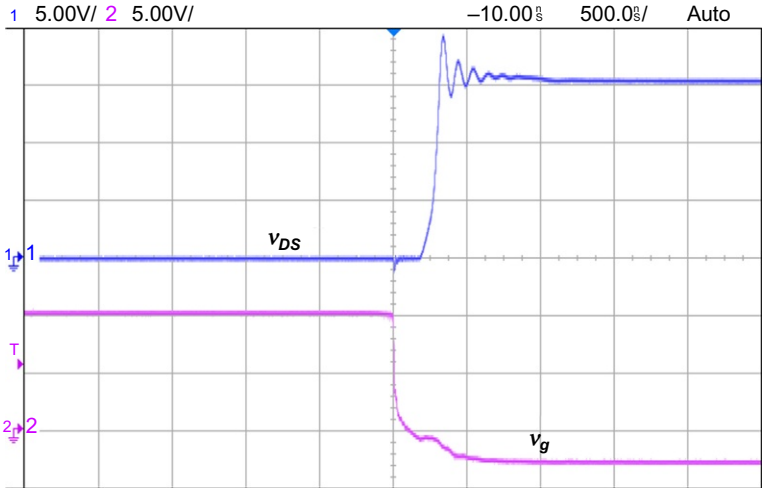


FIG. 2.72 Details of turn-off process for Sw1 and Sw2 ON and R_{pot} at the maximum resistance.

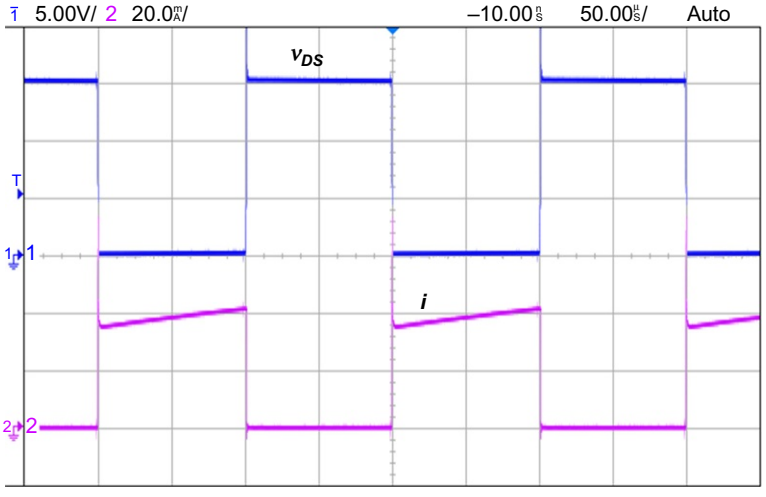


FIG. 2.73 Load current (drain current) and the drain-source voltage.

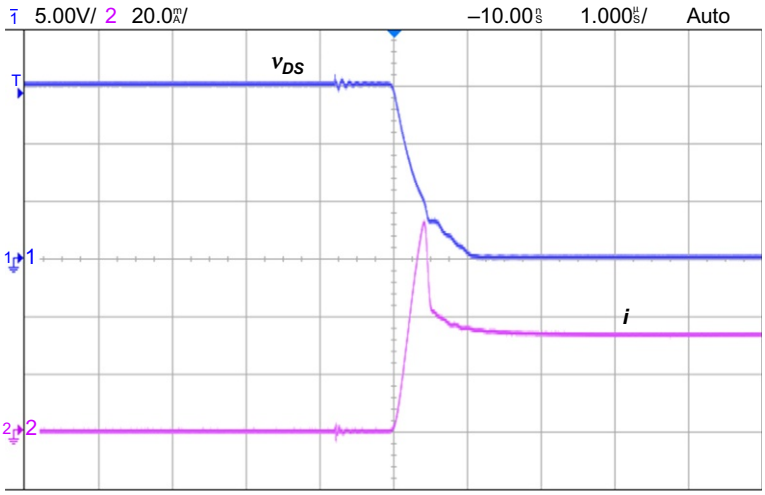


FIG. 2.74 Detail of the turn-on process when Sw1 and Sw2 are OFF and R_{pot} at the maximum resistance.

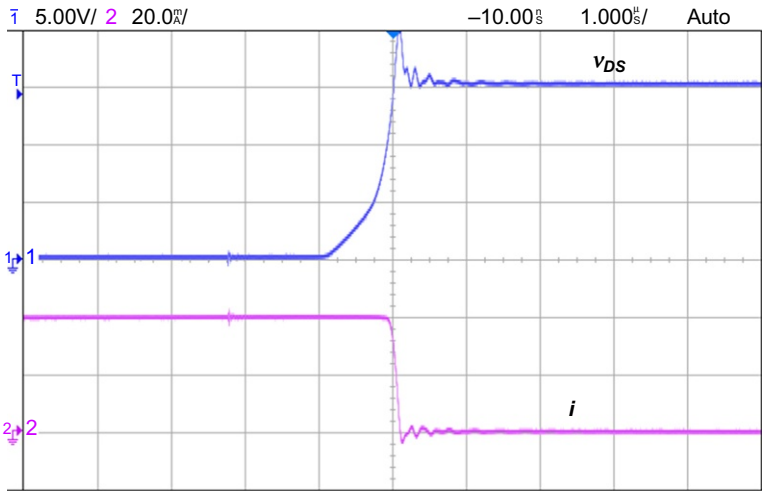


FIG. 2.75 Detail of the turn-off process when Sw1 and Sw2 are OFF and R_{pot} at the maximum resistance.

current) and the drain-source voltage. The current keeps growing during the conduction of the MOSFET.

Fig. 2.74 presents the details of the turn-on process when Sw1 and Sw2 are OFF and R_{pot} at the maximum resistance.

Fig. 2.75 presents the details of the turn-off process when Sw1 and Sw2 are OFF and R_{pot} at the maximum resistance.

2.6 Heatsink Thermal Design for Power Semiconductors

In power semiconductor devices, the heat from Joule's effect is produced in the semiconductor wafer. Then, the heat flows to colder environments like the device case and the ambient. This heat flux depends on the temperature gradient and the thermal characteristics of the materials involved.

Usually, an analogy with electric circuit is made to evaluate the heat flow. The average power dissipated in a semiconductor is represented by a current source. The temperatures in junction, case, sink, and ambient are represented by voltage nodes, while the thermal resistances are the circuit resistances. Fig. 2.76 presents the equivalent electric circuit for thermal design, valid for steady-state situation. The heat sink thermal resistances are represented by R_{Tsa}. R_{Tcs} represents the material placed between the semiconductor case and the heat sink. Usually, mica is used. Its thermal resistance is low. The dashed lines indicate that the heat sink will be connected after the electric circuit thermal analysis is performed.

Table 2.5 presents the nomenclature of the equivalent voltage nodes.

Table 2.6 presents the nomenclature of the equivalent resistances.

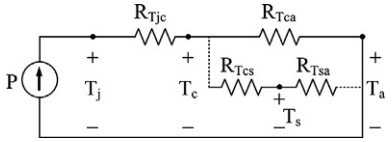


FIG. 2.76 Equivalent electric circuit for thermal design, valid for steady-state situation.

TABLE 2.5 Nomenclature of the equivalent voltage nodes

Parameter	Definition
T_j	Junction temperature
T_c	Case temperature
T_a	Ambient temperature
T_s	Heat-sink temperature

TABLE 2.6 Nomenclature of the equivalent resistances

Parameter	Definition
R_{Tjc}	Junction-to-case resistance
R_{Tca}	Case-to-ambient resistance
R_{Tcs}	Case-to-heat-sink resistance
R_{Tsa}	Heat-sink-to-ambient resistance

The objective of heat-sink thermal design is to guarantee that the semiconductor junction does not exceed its maximum allowed temperature. The ambient temperature is considered constant. The junction-to-case and case-to-ambient resistances are informed by manufactures.

According to Fig. 2.76, the junction temperature is given by (2.14):

$$T_j = T_a + P\left(R_{Tjc} + R_{Tca}\right) \tag{2.14}$$

EXAMPLE 2.1 Find the junction and case temperatures for a semiconductor with the parameters given in Table 2.7.

From Fig. 2.74 and Table 2.7, the case and junction temperatures are given by (2.15) and (2.16), respectively:

$$T_c = T_a + P \cdot R_{Tca} = 240°\text{C} \tag{2.15}$$

$$T_j = T_a + P \cdot R_{Tjc} = 280°\text{C} \tag{2.16}$$

TABLE 2.7 Semiconductor parameters

Parameter	Value	Description
P	20 W	Dissipated power
R_{Tjc}	2°C/W	Obtained from a manufacture catalog
R_{Tca}	10°C/W	Obtained from a manufacture catalog
T_a	40°	Chose by the designer depending on the location
T_{jmax}	120°	Maximum junction temperature before failure. Obtained from a manufacture catalog

2.6.1 Heatsink Design

From the previous example, the value resulted in (2.16) is much higher than the value given in Table 2.7 for the maximum junction temperature. This leads the semiconductor to destruction. Considering the impossibility to reduce the dissipated power and that there is no way to change the thermal resistance, the solution to ovoid the semiconductor destruction is to add a heat sink between the case and ambient with low thermal resistance. The heat sink introduces a low thermal resistance in parallel to the case-to-ambient resistance. This causes a reduction in the case temperature and consequently in the junction temperature. The following example explains hot to design the heat sink.

EXAMPLE 2.2 Design a heat sink for the semiconductor given in Example 2.1.

The design of the heat sink consists on finding the value for the heat-sink-to-ambient resistance R_{Tsa}. From Fig. 2.74 and Table 2.7, the equivalent resistance between the case and the ambient is given by (2.17). The maximum junction temperature is used because the final result in this example will give the maximum heat-sink-to-ambient resistance:

$$R_{Teq} = \frac{T_{jmax} - T_a}{P} - R_{Tjc} = {}^{2°\text{C}}\!/_{W} \tag{2.17}$$

The case-to-heat-sink resistance is given by (2.18), obtained from a manufacture catalog:

$$R_{Tcs} = {}^{0.7°\text{C}}\!/_{W} \tag{2.18}$$

The equivalent resistance is also given by (2.19):

$$R_{Teq} = \frac{R_{Tca}\left(R_{Tcs} + R_{Tsa}\right)}{R_{Tca} + R_{Tcs} + R_{Tsa}} \tag{2.19}$$

Replacing (2.17) and (2.18) in (2.19) and with the values from Table 2.7, the heat-sink-to-ambient resistance is given by (2.20):

$$R_{Tsa} = {}^{1.8°\text{C}}\!/_{W} \tag{2.20}$$

At this point, a manufacture catalog must be examined in order to find a heat sink with the same or lower thermal resistance.

The previous results are valid for steady-state condition and assuming that the power dissipated in the semiconductor is represented by its average value. However, the power may present peaks with value higher than the average. These peaks can be taken into account for the heat-sink design.

The junction temperature calculation considering the power peak is made using an electric quantity called thermal impedance (Z_{Tjc}). Its value is obtained through normalized current found in manufactures catalog. Fig. 2.77 presents typical curves for normalized thermal impedance. The x-axis values are the duration of the pulse over the switching period when the power peak occurs. The impedance is normalized over the junction-to-case thermal resistance.

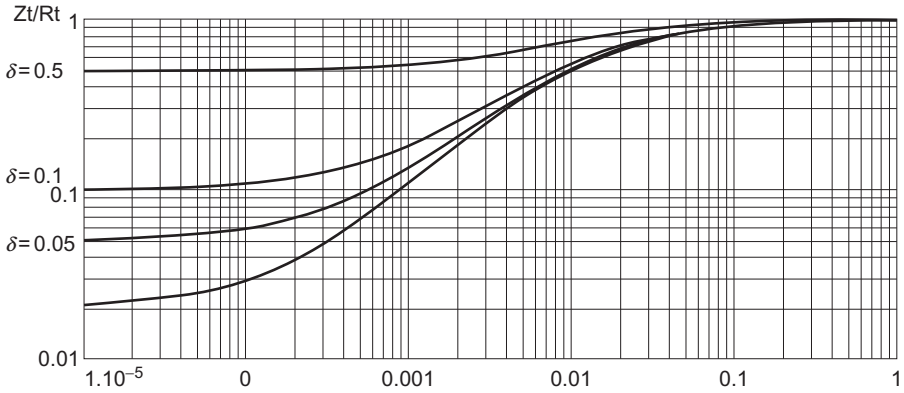


FIG. 2.77 Typical curves for normalized thermal impedance.

The peak junction temperature is given by (2.21):

$$T_{j_pk} = T_c + P_{pk} Z_{Tjc} \tag{2.21}$$

where the index *pk* means peak.

In case the value obtained in (2.21) is higher than the maximum junction temperature, the heat-sink-to-ambient resistance should be recalculated.

2.7 Transistor Selection Criteria

The transistor selection for a power electronic application depends on some criteria. The most common is to identify the required reverse voltage and forward current. Switching frequency appears as criteria directly related to the volume of passive elements, such as inductors and capacitors. For applications with desired low volume, a high-frequency transistor is the best choice. With these criteria defined, the next step is to verify if there are transistors available on the market that satisfies such criteria. Fig. 2.78 presents approximated power rate for currently available BJT, MOSFET, and IGBT, valid for silicon-based transistors [3,13].

Cost and efficiency can also be considered in choosing a transistor. For example, an application where the transistor must hold 500 V and 10 A, according to the previous chart, BJT, MOSFET, or IGBT can be employed. Considering the cost as the main concern, the BJT would likely appear as the best option. On the other hand, if the efficiency is the priority, IGBT is a potential candidate.

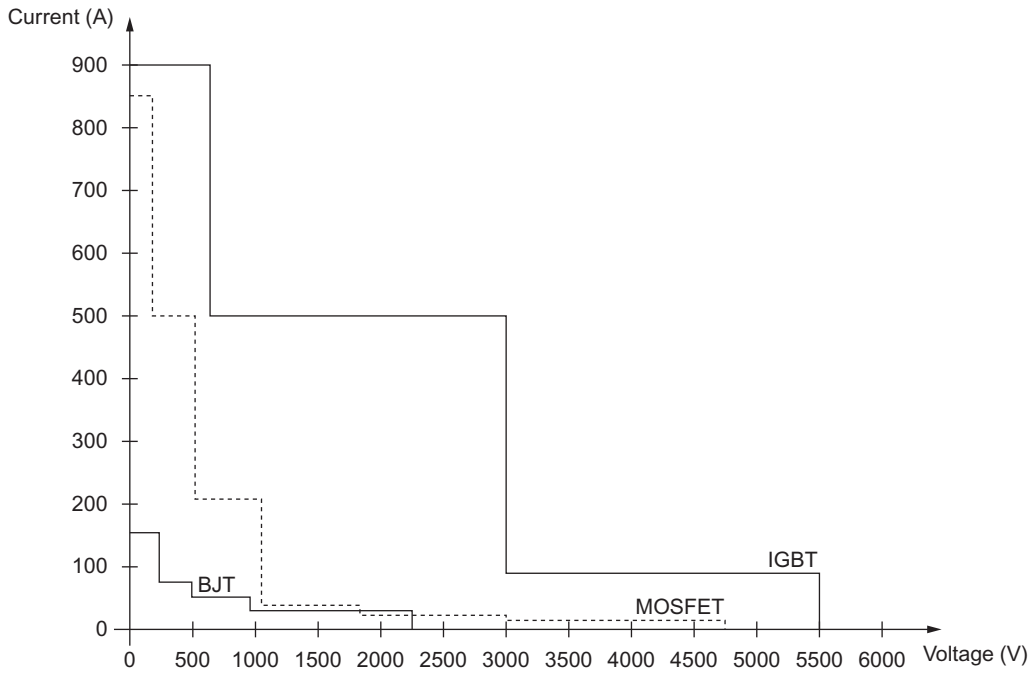


FIG. 2.78 Approximated power rate for currently available BJT, MOSFET, and IGBT.

Efficiency can be exploited taking into account the transistor material. Emerging transistors based on silicon carbide or gallium nitride [6,10,14,15] are a promising technology to enhance the switching behavior and consequently reduce the power losses. Such transistors are considered as wide bandgap power devices. Details of these devices are found in the chapter entitled "Wide Bandgap Materials and Power Semiconductor Devices."

References

[1] E.N. Lurch, Fundamentals of Electronics, Wiley, 1980. 634 p.

[2] M. Rashid, Power Electronics Handbook, Elsevier, 2011. 1409 p.

[3] N. Mohan, T.M. Undeland, W.P. Robbins, Power Electronics: Converters, Applications, and Design, Wiley, 2002. 824 p.

[4] M.H. Rashid, SPICE for Power Electronics and Electric Power, second ed., CRC Press, 2005. 582 p.

[5] B.J. Baliga, Fundamentals of Power Semiconductor Devices, Springer Science & Business Media, 2010. 1085 p.

[6] B.J. Baliga, Power semiconductor device figure of merit for high-frequency applications, IEEE Electron Device Lett. 10 (10) (1989) 455–457.

[7] R.E. Tarter, Solid-State Power Conversion Handbook, John Wiley & Sons, 1993. 734 p.

[8] B.K. Bose, Power Electronics and AC Drives, Prentice-Hall, 1986. 422 p.

[9] G. Chryssis, High-Frequency Switching Power Supplies: Theory and Design, McGraw-Hill, 1989. 312 p.

[10] B.J. Baliga, Trends in power semiconductor devices, IEEE Trans. Electron Devices 43 (10) (1996) 1717–1731.

[11] A.M. Trzynadlowski, Power Electronic Converters and Systems: Frontiers and Applications, Institution of Engineering and Technology, 2015. 657 p.

[12] H. Akagi, E.H. Watanabe, M. Aredes, Instantaneous Power Theory and Applications to Power Conditioning, John Wiley & Sons, 2007. 396 p.

[13] Internet information on http://www.digikey.com and http://www.mouser.com/ (Accessed 23.02.17).

[14] B.J. Baliga, SiC power devices: from conception to social impact, in: 2016 46th European Solid-State Device Research Conference (ESSDERC), 2016, , pp. 192–197.

[15] P. Friedrichs, T. Kimoto, L. Ley, G. Pensl, Silicon Carbide, Volume 2: Power Devices and Sensors, John Wiley & Sons, 2011. 523 p.

3

Thyristors

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3.1 Introduction

Thyristors are usually three-terminal devices that have four layers of alternating *p*-type and *n*-type material (i.e., three *p*-*n* junctions) comprising its main power handling section. In contrast to the linear relation that exists between load and control currents in a transistor, the thyristor is bistable. The control terminal of the thyristor, called the gate (*G*) electrode, may be connected to an integrated and complex structure as a part of the device. The other two terminals, called the anode (*A*) and cathode (*K*), handle the large applied potentials (often of both polarities) and conduct the major current through the thyristor. The anode and cathode terminals are connected in series with the load to which power is to be controlled.

Thyristors are used to approximate ideal closed (no voltage drop between anode and cathode) or open (no anode current flow) switches for control of power flow in a circuit. This differs from low-level digital switching circuits that are designed to deliver two distinct small voltage levels while conducting small currents (ideally zero). Thyristor circuits must have the capability of delivering large currents and be able to withstand large externally applied voltages. All thyristor types are controllable in switching from a forward-blocking state (positive potential applied to the anode with respect to the cathode, with correspondingly little anode current flow) into a forward-conduction state (large forward anode current flowing, with a small anode-cathode potential drop). Most thyristors have the characteristic that after switching from a forward-blocking state into the forward-conduction state, the gate signal can be removed and the thyristor will remain in its forward-conduction mode. This property is termed "latching" and is an important distinction between thyristors and other types of power electronic devices. Some thyristors are also controllable in switching from forward-conduction back to a forward-blocking state. The particular design of a thyristor will determine its controllability and often its application.

Thyristors are typically used at the highest energy levels in power-conditioning circuits because they are designed to handle the largest currents and voltages of any device technology (systems approximately with voltages above 1 kV or currents

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above 100 A). Many medium-power circuits (systems operating at less than 1 kV or 100 A) and particularly low-power circuits (systems operating below 100 V or several amperes) generally make use of power bipolar transistors, power metal-oxide-semiconductor field-effect transistors (MOSFETs), or insulated gate bipolar transistors (IGBTs) as the main switching elements because of the relative ease in controlling them. IGBT technology, however, continues to improve and multiple silicon die are commonly packaged together in a module. These modules are replacing thyristors in applications operating up to 3 kV that require controllable turn-off because of easier gate-drive requirements. Power diodes are used throughout all levels of power-conditioning circuits and systems for component protection and wave shaping.

A thyristor used in some ac power circuits (50 or 60 Hz in commercial utilities or 400 Hz in aircraft) to control ac power flow can be made to optimize internal power loss at the expense of switching speed. These thyristors are called phase-control devices, because they are generally turned from a forward-blocking into a forward-conducting state at some specified phase angle of the applied sinusoidal anode-cathode voltage waveform. A second class of thyristors is used in association with dc sources or in converting ac power at one amplitude and frequency into ac power at another amplitude and frequency and must generally switch on and off relatively quickly. A typical application for the second class of thyristors is in converting a dc voltage or current into an ac voltage or current. A circuit that performs this operation is often called an inverter, and the associated thyristors used are referred to as inverter thyristors.

There are four major types of thyristors: (i) the silicon-controlled rectifier (SCR), (ii) the gate turn-off thyristor (GTO) and its close relative the integrated gate-commutated thyristor (IGCT), (iii) the MOS-controlled thyristor (MCT) and its various forms, and (iv) the static induction thyristor (SITh). MCTs are so-named because many parallel enhancement-mode, MOSFET structures of one charge type are integrated into the thyristor for turn-on, and many more MOSFETs of the other charge types are integrated into the thyristor for turn-off. An SITh or field-controlled thyristor (FCTh) has essentially the same construction as a power diode with a gate structure that can pinch-off anode current flow. Although MCTs, derivative forms of the MCT and SIThs, have the advantage of being essentially voltage-controlled devices (i.e., little control current is required for turn-on or turnoff and therefore require simplified control circuits attached to the gate electrode), they are currently only found in niche applications such as pulse power. Detailed discussion of variations of MCTs and SIThs and additional references on these devices are discussed by Hudgins in [1]. Other types of thyristors include the triac (a pair of antiparallel SCRs integrated together to form a bidirectional current switch) and the programmable unijunction transistor (PUT).

The SCRs and GTOs are designed to operate at all power levels. These devices are primarily controlled using electric signals (current), though some types are made to be controlled using optical energy (photons) for turn-on. Subclasses of SCRs and GTOs are reverse conducting types and symmetrical structures that block applied potentials in the reverse and forward polarities. Other variations of GTOs are the gate-commutated turnoff thyristor (GCT), commonly available as the IGCT and the bidirectional-controlled thyristor (BCT).

All power electronic devices must be derated (e.g., power dissipation levels, current conduction, voltage blocking, and switching frequency must be reduced), when operating above room temperature (defined as approximately 25°C). Bipolar-type devices have thermal runaway problems, in that if allowed to conduct unlimited current, these devices will heat up internally causing more current to flow, thus generating more heat and so forth until destruction. Devices that exhibit this behavior are *pin* diodes, bipolar transistors, and thyristors.

Almost all power semiconductor devices are made from silicon (Si). Research and development continues in developing other types of devices in silicon carbide (SiC), gallium nitride (GaN), and related material systems. However, the physical description and general behavior of thyristors is unimportant to the semiconductor material system used, though the discussion and any numbers cited in the chapter will be associated with Si devices.

3.2 Basic Structure and Operation

Fig. 3.1 shows a conceptual view of a typical thyristor with the three *p-n* junctions and the external electrodes labeled. Also shown in the figure is the thyristor circuit symbol used in electric schematics.

A high-resistivity region, n^--base, is present in all thyristors. It is this region, the n^--base and associated junction, J_2 of Fig. 3.1, which must support the large applied forward voltages that occur when the switch is in its off- or forward-blocking state (nonconducting). The n^--base is typically doped with impurity phosphorous atoms at a concentration of 10^{13}–10^{14} cm^{-3}.

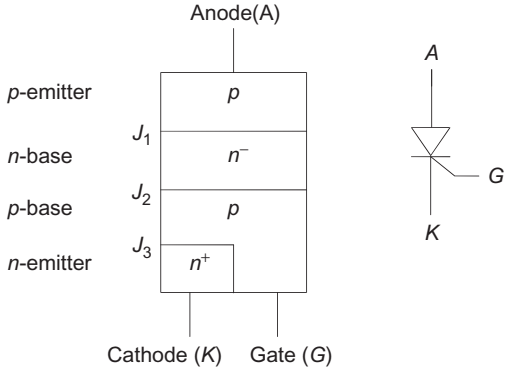


FIG. 3.1 Simple cross section of a typical thyristor and the associated electric schematic symbols.

The n^--base can be tens to hundreds of micrometer thick to support large voltages. High-voltage thyristors are generally made by diffusing aluminum or gallium into both surfaces to create p-doped regions forming deep junctions with the n^--base. The doping profile of the p-regions ranges from about 10^{15} to 10^{17} cm^{-3}. These p-regions can be up to tens of micrometer thick. The cathode region (typically only a few micrometers thick) is formed by using phosphorous atoms at a doping density of 10^{17}–10^{18} cm^{-3}.

The higher the forward-blocking voltage rating of the thyristor, the thicker the n^--base region must be. However, increasing the thickness of this high-resistivity region results in slower turn-on and turn-off (i.e., longer switching times and/or lower frequency of switching cycles because of more stored charge during conduction). For example, a device rated for a forward-blocking voltage of 1 kV will, by its physical construction, switch much more slowly than one rated for 100 V. In addition, the thicker high-resistivity region of the 1 kV device will cause a larger forward voltage drop during conduction than the 100 V device carrying the same current. Impurity atoms, such as platinum or gold, and electron irradiation are used to create charge-carrier recombination sites in the thyristor. The large number of recombination sites reduces the mean carrier lifetime (average time that an electron or hole moves through the Si before recombining with its opposite charge-carrier type). A reduced carrier lifetime shortens the switching times (in particular the turnoff or recovery time) at the expense of increasing the forward conduction drop. There are other effects associated with the relative thickness and layout of the various regions that make up modern thyristors, but the major trade-off between forward-blocking voltage rating and switching times and between forward-blocking voltage rating and forward voltage drop during conduction should be kept in mind. (In signal-level electronics, an analogous trade-off appears as a lowering of amplification (gain) to achieve higher operating frequencies and is often referred to as the gain-bandwidth product.)

Operation of thyristors is as follows. When a positive voltage is applied to the anode (with respect to cathode), the thyristor is in its forward-blocking state. The center junction J_2 (see Fig. 3.1) is reverse biased. In this operating mode, the gate current is held to zero (open circuit). In practice, the gate electrode is biased to a small negative voltage (with respect to the cathode) to reverse bias the GK junction J_3 and prevent charge carriers from being injected into the p-base. In this condition, only thermally generated leakage current flows through the device and can often be approximated as zero in value (the actual value of the leakage current is typically many orders of magnitude lower than the conducted current in the on-state). As long as the forward applied voltage does not exceed the value necessary to cause excessive carrier multiplication in the depletion region around J_2 (avalanche breakdown), the thyristor remains in an off-state (forward-blocking). If the applied voltage exceeds the maximum forward-blocking voltage of the thyristor, it will switch to its on-state. However, this mode of turn-on causes nonuniformity in the current flow, is generally destructive, and should be avoided.

When a positive gate current is injected into the device, J_3 becomes forward biased and electrons are injected from the n-emitter into the p-base. Some of these electrons diffuse across the p-base and get collected in the n^--base. This collected charge causes a change in the bias condition of J_1. The change in bias of J_1 causes holes to be injected from the p-emitter into the n^--base. These holes diffuse across the n^--base and are collected in the p-base. The addition of these collected holes in the p-base acts the same as gate current. The entire process is regenerative and will cause the increase in charge carriers until J_2 also becomes forward biased and the thyristor is latched in its on-state (forward conduction). The regenerative action will take place as long as the gate current is applied in sufficient amount and for a sufficient length of time. This mode of turn-on is considered to be the desired one as it is controlled by the gate signal.

This switching behavior can also be explained in terms of the two-transistor analog shown in Fig. 3.2. The two transistors are regeneratively coupled so that if the sum of their forward current gains (α's) exceeds unity, each drives the other into saturation. Eq. (3.1) describes the condition necessary for the thyristor to move from a forward-blocking state to the forward-conduction state. The forward current gain (expressed as the ratio of collector current to emitter current) of the *pnp* transistor is denoted by α_p and that of the *npn* as α_n. The α's are current dependent and increase slightly as the current increases. The center junction J_2 is reverse biased under forward applied voltage (positive, v_{AK}). The associated electric field in the depletion region around the junction can result in significant carrier multiplication, denoted as a multiplying factor M on the current components, I_{co} and i_G.

$$i_A = \frac{MI_{co} + M\alpha_n i_G}{1 - M(\alpha_n + \alpha_p)} \tag{3.1}$$

In the forward-blocking state, the leakage current I_{co} is small, both α's are small, and their sum is less than unity. Gate current increases the current in both transistors, increasing their α's.

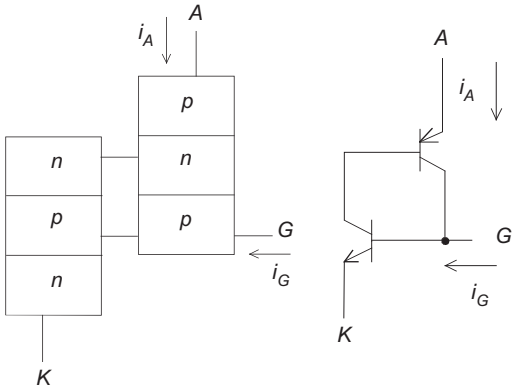


FIG. 3.2 Two-transistor behavioral model of a thyristor.

Collector current in the *npn* transistor acts as base current for the *pnp*, and analogously, the collector current of the *pnp* acts as base current driving the *npn* transistor. When the sum of the two α's equals unity, the thyristor switches to its on-state (latches). This condition can also be reached, without any gate current, by increasing the forward applied voltage so that carrier multiplication ($M \gg 1$) at J_2 increases the internal leakage current, thus increasing the two α's. A third way to increase the α's exists by increasing the device (junction) temperature. Increasing the temperature causes a corresponding increase in the leakage current I_{co} to the point where latching can occur. The typical manifestation of this temperature dependence is to cause an effective lowering of the maximum blocking voltage that can be sustained by the thyristor.

Another way to cause a thyristor to switch from forward-blocking to forward-conduction exists. Under a forward applied voltage, J_2 is reverse biased, while the other two junctions are forward biased in the blocking mode. The reverse-biased junction of J_2 is the dominant capacitance of the three and determines the displacement current that flows. If the rate of increase in the applied $v_{AK}(dv_{AK}/dt)$ is sufficient, it will cause a significant displacement current through the J_2 capacitance. This displacement current can initiate switching similar to an externally applied gate current. This dynamic phenomenon is inherent in all thyristors and causes there to be a limit (dv/dt) to the time rate of applied v_{AK} that can be placed on the device to avoid uncontrolled switching. Alterations to the basic thyristor structure can be produced that increase the dv/dt limit.

Once the thyristor has moved into forward conduction, any applied gate current is superfluous. The thyristor is latched and, for SCRs, cannot be returned to a blocking mode by using the gate terminal. Anode current must be commutated away from the SCR for a sufficient time to allow stored charge in the device to recombine. Only after this recovery time has occurred, can a forward voltage be reapplied (below the dv/dt limit of course), and the SCR again be operated in a forward-blocking mode. If the forward voltage is reapplied before sufficient recovery time has elapsed, the SCR will move back into forward conduction. For GTOs and IGCTs, a large applied reverse gate current (typically in the range of 10%–50% of the anode current for GTOs and 100% of the anode current for IGCTs) applied for a sufficient time can remove enough charge near the GK junction to cause it to turn off. This interrupts the base current to the *pnp* transistor, leaving the *pnp* open base, causing thyristor turn-off. This is similar in principle to use negative base current to quickly turn off a traditional bipolar transistor.

3.3 Static Characteristics

3.3.1 Current–Voltage Curves for Thyristors

A plot of the anode current (i_A) as a function of anode-cathode voltage (v_{AK}) is shown in Fig. 3.3. The forward-blocking mode

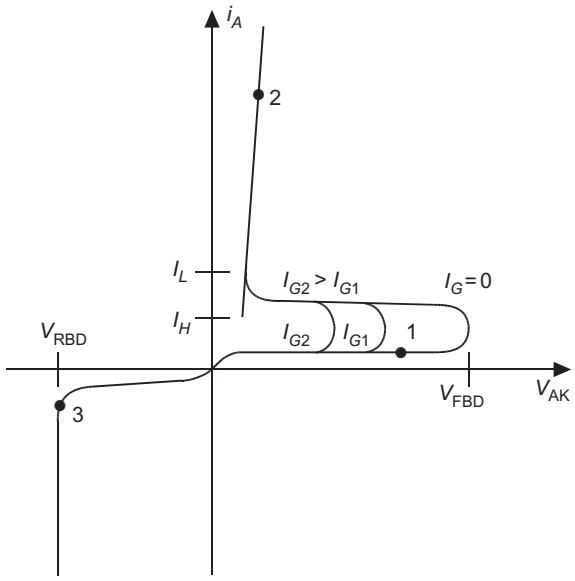


FIG. 3.3 Static characteristic *i-v* curve typical of thyristors.

is shown as the low-current portion of the graph (solid curve around operating point "1"). With zero gate current and positive v_{AK}, the forward characteristic in the off- or blocking state is determined by the center junction J_2, which is reverse biased. At operating point "1," very little current flows (I_{co} only) through the device. However, if the applied voltage exceeds the forward-blocking voltage, the thyristor switches to its on- or conducting state (shown as operating point "2") because of carrier multiplication (M in Eq. (3.1)). The effect of gate current is to lower the blocking voltage at which switching takes place. The thyristor moves rapidly along the negatively sloped portion of the curve until it reaches a stable operating point determined by the external circuit (point "2"). The portion of the graph indicating forward conduction shows the large values of i_A that may be conducted at relatively low values of v_{AK}, similar to a power diode.

As the thyristor moves from forward-blocking to forward-conducting, the external circuit must allow sufficient anode current to flow to keep the device latched. The minimum anode current that will cause the device to remain in forward conduction as it switches from forward-blocking is called the latching current I_L. If the thyristor is already in forward conduction and the anode current is reduced, the device can move its operating mode from forward conduction back to forward-blocking. The minimum value of anode current necessary to keep the device in forward conduction after it has been operating at a high anode current value is called the holding current I_H. The holding current value is lower than the latching current value as indicated in Fig. 3.3.

The reverse thyristor characteristic, quadrant III of Fig. 3.3, is determined by the outer two junctions (J_1 and J_3), which are reverse biased in this operating mode (applied v_{AK} is negative). Symmetrical thyristors are designed so that J_1 will reach reverse

breakdown due to carrier multiplication at an applied reverse potential near the forward breakdown value (operating point "3" in Fig. 3.3). The forward- and reverse-blocking junctions are usually fabricated at the same time with a very long diffusion process (10–50 h) at high temperatures (>1200°C). This process produces symmetrical blocking properties. Wafer-edge termination processing causes the forward-blocking capability to be reduced to about 90% of the reverse-blocking capability. Edge termination is discussed below. Asymmetrical devices are made to optimize forward conduction and turnoff properties and as such reach reverse breakdown at a lower voltage than that applied in the forward direction. This is accomplished by designing the asymmetrical thyristor with a much thinner n^--base than is used in symmetrical structures. The thin n^--base leads to improved properties such as lower forward drop and shorter switching times. Asymmetrical devices are generally used in applications when only forward voltages (positive, v_{AK}) are to be applied (including many inverter designs).

The form of the gate-to-cathode *i-v* characteristic of SCRs, GTOs, and IGCTs is similar to that of a diode. With positive gate bias, the gate-cathode junction is forward biased and permits the flow of a large current in the presence of a low voltage drop. When negative gate voltage is applied to an SCR, the gate-cathode junction is reverse biased and prevents the flow of current until the avalanche breakdown voltage is reached. In a GTO or IGCT, a negative gate voltage is applied to provide a low-impedance path for anode current to flow out of the device instead of out the cathode. In this way, the cathode region (base-emitter junction of the equivalent *npn* transistor) turns off, thus pulling the equivalent *npn* transistor out of conduction. This causes the entire thyristor to return to its blocking state. The problem with the GTO and IGCT is that the gate-drive circuitry is typically required to sink 10%–50% (for the GTO) or 100% (for the IGCT) of the anode current to achieve turn-off.

3.3.2 Edge and Surface Terminations

Thyristors are often made with planar diffusion technology to create the cathode region. Formation of these regions creates cylindrical curvature of the metallurgical gate-cathode junction. Under reverse bias, the curvature of the associated depletion region results in electric field crowding along the curved section of the p^+ diffused region. The field crowding seriously reduces the breakdown potential below that expected for the bulk semiconductor. A floating field ring, an extra *p* diffused region with no electric connection at the surface, is often added to modify the electric field profile and thus reduce it to a value below or at the field strength in the bulk. An illustration of a single floating field ring is shown in Fig. 3.4. The spacing, *W*, between the main anode region and the field ring is critical. Multiple rings can also be employed to further modify the electric field in high-voltage rated thyristors.

Another common method for altering the electric field at the surface is by using a field plate as shown in cross section in Fig. 3.5. By forcing the potential over the oxide to be the same as at the surface of the p^+ region, the depletion region can be extended so that the electric field intensity is reduced near the curved portion of the diffused p^+ region. A common practice is to use field plates with floating field rings to obtain optimum breakdown performance.

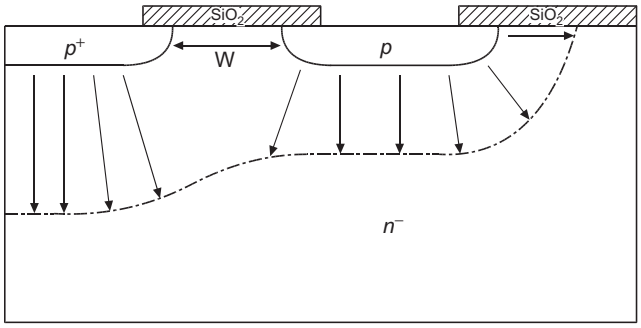


FIG. 3.4 Cross section showing a floating field ring to decrease the electric field intensity near the curved portion of the main anode region (leftmost p^+ region).

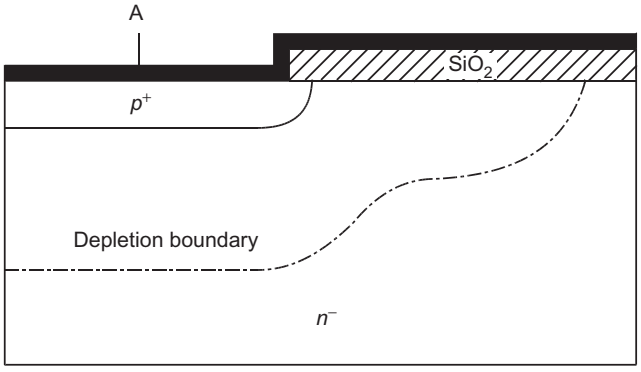


FIG. 3.5 Cross section showing a field plate used to reduce the electric field intensity near the curved portion of the p^+-region (anode).

High-voltage thyristors are made from single wafers of Si and must have edge terminations other than floating field rings or field plates to promote bulk breakdown and limit leakage current at the surface. Controlled bevel angles can be created using lapping and polishing techniques during production of large-area thyristors. Two types of bevel junctions can be created: (i) a positive bevel defined as one in which the junction area decreases when moving from the highly doped to the lightly doped side of the depletion region and (ii) a negative bevel defined as one in which the junction area increases when moving from the highly doped to the lightly doped side of the depletion region. In practice, the negative bevel must be lapped at an extremely shallow angle to reduce the surface field below the field intensity in the bulk. All positive bevel angles between 0 and 90 degrees result in a lower surface field than in the bulk. Fig. 3.6 shows the use of a positive bevel for the J_1 junction and a shallow negative bevel for the J_2 and J_3 junctions on a thyristor

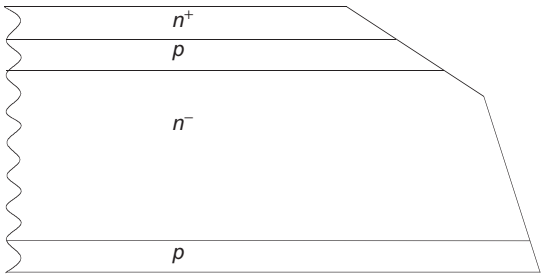


FIG. 3.6 Cross section of a thyristor showing the negative bevel (upper p-n^- and p-n^+ junctions) and positive bevel (lower p-n^- junction) used for edge termination of large-area devices.

cross section to make maximum use of the Si area for conduction and still reduce the surface electric field. Further details of the use of beveling, field plates, and field rings can be found in Ghandi [1] and Baliga [2].

3.3.3 Packaging

Thyristors are available in a wide variety of packages, from small plastic ones for low-power (i.e., TO-247), to stud-mount packages for medium-power, to press pack (also called flat pack) for the highest power devices. The press packs must be mounted under pressure to obtain proper electric and thermal contact between the device and the external metal electrodes. Special force-calibrated clamps are made for this purpose. Large-area thyristors cannot be directly attached to the large copper pole piece of the press pack because of the difference in the coefficient of thermal expansion (CTE), hence the use of a pressure contact for both anode and cathode. Fig. 3.7 shows typical thyristor stud-mount and press-pack packages.

Many medium-power thyristors are appearing in modules where a half- or full bridge (and associated antiparallel diodes) is put together in one package. A power module package should have five characteristics:

(i) Electric isolation of the baseplate from the semiconductor
(ii) Good thermal performance
(iii) Good electric performance
(iv) Long life/high reliability
(v) Low cost

Electric isolation of the baseplate from the semiconductor is necessary in order to contain both halves of a phase leg in one package and for convenience (modules switching different phases can be mounted on one heat sink) and safety (heat sinks can be held at ground potential).

Thermal performance is measured by the maximum temperature rise in the Si die at a given power dissipation level with a fixed heat sink temperature. The lower the die temperature, the better the package. A package with a low thermal resistance from junction-to-sink can operate at higher power densities for the same temperature rise or lower temperatures for the same power dissipation than a more thermally resistive package. While maintaining low device temperature is generally preferable, temperature variation affects majority carrier and bipolar devices differently. Roughly speaking, in a bipolar device such as a thyristor, switching losses increase and conduction losses decrease with increasing temperature. In a majority carrier device, such as a MOSFET, conduction losses increase with increasing temperature. The thermal conductivity of typical materials used in thyristor packages is shown in Table 3.1.

Electric performance refers primarily to the stray inductance in series with the die and the capability of mounting a low-inductance bus to the terminals. Another problem is the minimization of capacitive cross talk from one switch to another, which can cause an abnormal on-state condition by charging the gate of an off-state switch or from a switch to any circuitry in the package (as would be found in a hybrid power module). Capacitive coupling is a major cause of electromagnetic interference (EMI). As the stray inductance of the module and the bus sets a minimum switching loss for the device—because the switch must absorb the stored inductive energy—it is very important to minimize inductance within the module. Reducing the parasitic inductance reduces the high-frequency ringing during transients that is another cause of radiated EMI. Since

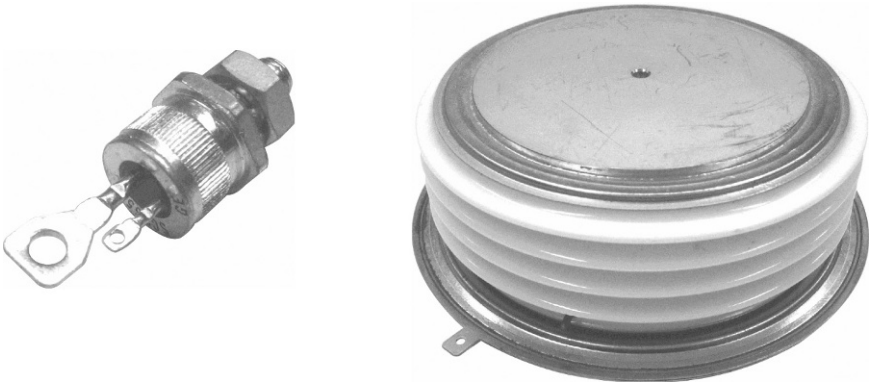


FIG. 3.7 Examples of thyristor packaging: stud-mount (left) and press-pack/capsule (right).

TABLE 3.1 Thermal conductivity of thyristor package materials

Material	Thermal conductivity (W/m·K) at 300 K
Silicon	150
Copper (baseplate and pole pieces)	390–400
AlN substrate	170
Al_2O_3 (alumina)	28
Aluminum (Al)	220
Tungsten (W)	167
Molybdenum (Mo)	138
Metal matrix composites (MMC)	170
Thermal grease (heat sink compound)	0.75
60/40 solder (Pb/Sn eutectic)	50
95/5 solder (Pb/Sn high temperature)	35

stray inductance can cause large peak voltages during switching transients, minimizing it helps to maintain the device within its safe area of operation.

Long life and high reliability are primarily attained through minimization of thermal cycling, minimization of ambient temperature, and proper design of the transistor stack. Thermal cycling fatigues material interfaces because of CTE mismatch between dissimilar materials. As the materials undergo temperature variation, they expand and contract at different rates that stresses the interface between the layers and can cause interface deterioration (e.g., cracking of solder layers or wire debonding). Chemical degradation processes such as dendrite growth and impurity migration are accelerated with increasing temperature, so keeping the absolute temperature of the device low and minimizing the temperature changes to which it is subjected is important. Typical CTE values for common package materials are given in Table 3.2.

Low cost is achieved in a variety of ways. Both manufacturing and material costs must be taken into account when designing a power module. Materials that are difficult to machine or process, even if they are relatively cheap in raw form (e.g., molybdenum), should be avoided. Manufacturing processes that lower yield also drive up costs. In addition, a part that is very reliable can reduce future costs by reducing the need for repair and replacement.

TABLE 3.2 CTE for thyristor package materials

Material	CTE (μm/m·K) at 300 K
Silicon	4.1
Copper (baseplate and pole pieces)	17
AlN substrate	4.5
Al_2O_3 (Alumina)	6.5
Tungsten (W)	4.6
Molybdenum (Mo)	4.9
Aluminum (Al)	23
Metal matrix composites (MMC)	5–20
60/40 solder (Pb/Sn eutectic)	25

The basic half-bridge module has three power terminals: plus, minus, and phase. Advanced modules differ from traditional high-power commercial modules in several ways. The baseplate is metallized aluminum nitride (AlN) ceramic rather than the typical 0.125 in. thick nickel-plated copper baseplate with a soldered metallized ceramic substrate for electric isolation. This AlN baseplate stack provides a low thermal resistance from die to heat sink. The copper terminal power buses are attached by solder to the devices in a wirebond-free, low-inductance, low-resistance, device interconnect configuration. The balance of the assembly is typical for module manufacturing with attachment of shells, use of dielectric gels, and hard epoxies and adhesive to seal the finished module. Details of the thermal performance of modules and advanced modules can be found in Beker et al. [3] and Godbold et al. [4].

3.4 Dynamic Switching Characteristics

The time rate of rise of anode current (di/dt) during turn-on and the time rate of rise of anode-cathode voltage (dv/dt) during turnoff are important parameters to control for ensuring proper and reliable operation. All thyristors have maximum limits for di/dt and dv/dt that must not be exceeded. Devices capable of conducting large currents in the on-state are necessarily made with large surface areas through which the current flows. During turn-on, localized areas of a device (near the gate region) begin to conduct current. The initial turn-on of an SCR is shown in Fig. 3.8. The cross section illustrates how injected gate current flows to the nearest cathode region, causing this portion of the *npn* transistor to begin conducting. The *pnp* transistor then follows the *npn* into conduction such that anode current begins flowing only in a small portion of the cathode region. If the local current density becomes too large (in excess of several thousand amperes per square centimeter), then self-heating will damage the device. Sufficient time (referred to as plasma spreading time) must be allowed for the entire cathode area to begin conducting before the localized currents become too high. This phenomenon results in a maximum allowable rate of rise of anode current in a thyristor and is referred to as a di/dt limit. In many high-frequency applications, the entire cathode region is never fully in conduction. Prevention of di/dt failure can be accomplished if the rate of increase of conduction area exceeds the di/dt rate such that the internal junction temperature does not exceed a specified critical temperature (typically approximately 350°C). This critical temperature decreases as the blocking voltage increases. Adding series inductance to the thyristor to limit di/dt below its maximum usually causes circuit design problems.

Another way to increase the di/dt rating of a device is to increase the amount of gate-cathode periphery. Inverter SCRs (so-named because of their use in high-frequency power-converter circuits that convert dc to ac, i.e., invert) are designed so that there is a large amount of gate edge adjacent to a

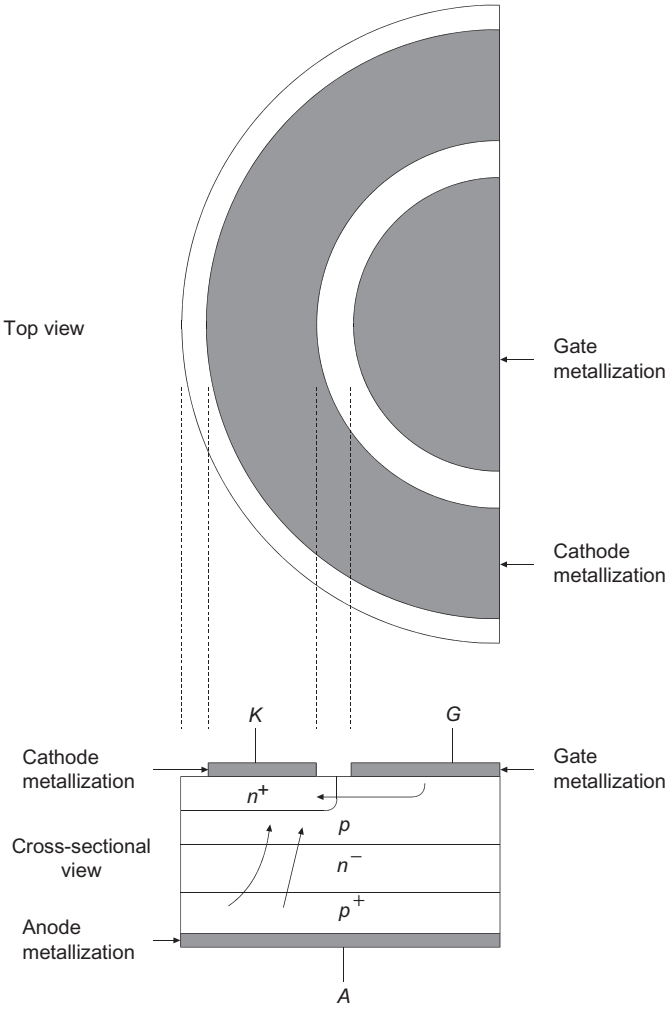


FIG. 3.8 Top view and associated cross section of gate-cathode periphery showing initial turn-on region in a center-fired thyristor.

significant amount of cathode edge. A top surface view of two typical gate-cathode patterns, found in large thyristors, is shown in Fig. 3.9. An inverter SCR often has a stated maximum *di/dt* limit of approximately 2000 A/μs. This value has been shown to be conservative in Hadgins [5], and by using excessive gate current under certain operating conditions, an inverter SCR can be operated reliably at 10,000–20,000 A/μs.

A GTO takes the interdigitation of the gate and cathode to the extreme (Fig. 3.9, left). In Fig. 3.10, a cross section of a GTO shows the amount of interdigitation. A GTO often has cathode islands that are formed by etching the Si. A metal plate can be placed on the top to connect the individual cathodes into a large arrangement of electrically parallel cathodes. The gate metallization is placed so that the gate surrounding each cathode is electrically in parallel as well. This construction not only allows high *di/dt* values to be reached, as in an inverter SCR but also provides the capability to turn off the anode current by shunting it away from the individual cathodes and out of the gate electrode upon reverse biasing of the gate. During turnoff, current is decreasing while voltage across the device is increasing. If the forward voltage becomes too high while sufficient

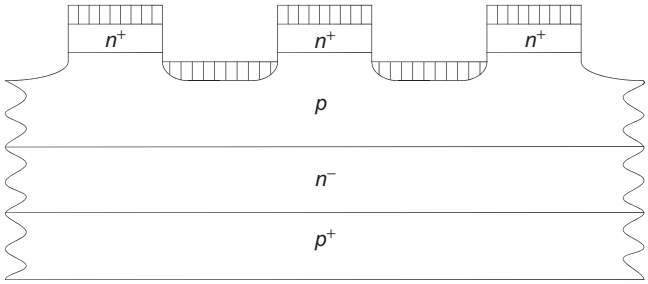


FIG. 3.10 Cross section of a GTO showing the cathode islands and interdigitation with the gate (*p*-base).

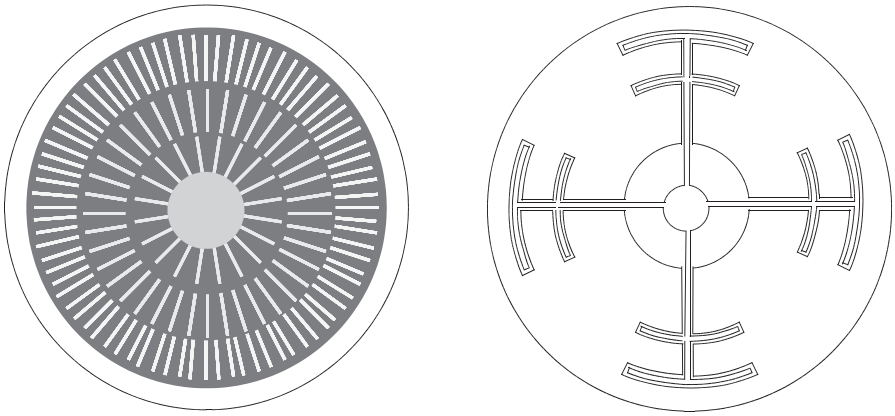


FIG. 3.9 Top view of typical interdigitated gate-cathode patterns used for thyristors.

current is still flowing, then the device will drop back into its conduction mode instead of completing its turn-off cycle. Also, during turnoff, the power dissipation can become excessive if the current and voltage are simultaneously too large. Both of these turn-off problems can damage the device and other portions of the circuit.

Another switching problem that occurs is associated primarily with thyristors, though other power electronic devices suffer some degradation of performance from the same problem. This problem is that thyristors can self-trigger into a forward-conduction mode from a forward-blocking mode if the rate of rise of forward anode-cathode voltage is too large. This triggering method is due to displacement current through the associated junction capacitances (the capacitance at J_2 dominates because it is reverse biased under forward applied voltage). The displacement current contributes to the leakage current I_{co}, shown in Eq. (3.1). The SCRs, GTOs, and IGCTs, therefore, have a maximum dv/dt rating that should not be exceeded (typical values are 100–1000 V/μs). Switching into a reverse-conducting from a reverse-blocking state, due to an applied reverse dv/dt, is not possible because the values of the reverse α's of the equivalent transistors can never be made large enough to cause the necessary feedback (latching) effect. An external capacitor is often placed between the anode and cathode of the thyristor to help control the dv/dt experienced. Capacitors and other components that are used to form such protection circuits, known as snubbers, may be found in all power semiconductor devices.

3.4.1 Cathode Shorts

As the temperature in the thyristor increases above 25°C, the minority carrier lifetime and the corresponding diffusion lengths in the n- and p-bases increase. This leads to an increase in the α's of the equivalent transistors. Discussion of the details of the minority carrier diffusion length and its role in determining the current gain factor α can be found in Sze [6]. Referring to Eq. (3.1), it is seen that a lower applied bias will give a carrier multiplication factor M sufficient to switch the device from forward-blocking into conduction, because of this increase of the α's with increasing temperature. Placing a shunt resistor in parallel with the base-emitter junction of the equivalent npn transistor (shown in Fig. 3.11) will result in an effective current gain, α_{neff}, that is lower than α_n, as given by Eq. (3.2), where v_{GK} is the applied gate-cathode voltage, R_s is the equivalent lumped value for the distributed current shunting structure, and the remaining factors form the appropriate current factor based on the applied bias and characteristics of the gate-cathode junction. The shunt current path is implemented by providing intermittent shorts, called cathode shorts, between the p-base (gate) region and the n^+-emitter (cathode) region in the thyristor as illustrated in Fig. 3.12. The lumped shunt resistance value is in the range of 1–15 Ω as measured from gate to cathode.

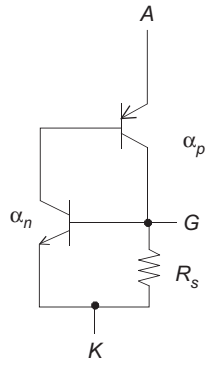


FIG. 3.11 Two-transistor equivalent circuit showing the addition of a resistive shunt path for anode current.

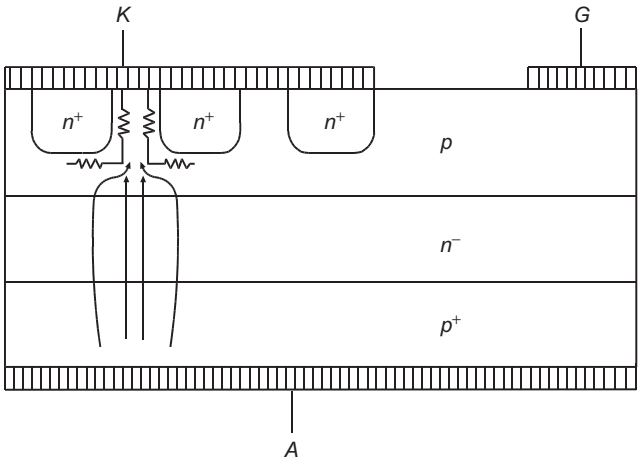


FIG. 3.12 Cross section showing cathode shorts and the resulting resistive shunt path for anode current.

$$\alpha_{neff} = \alpha_n \left(\frac{1}{1 + (v_{GK}\alpha_n)/(R_s i_0 \exp(q v_{GK}/kT))} \right) \tag{3.2}$$

Low values of anode current (e.g., those associated with an increase in temperature under forward-blocking conditions) will flow through the shunt path to the cathode contact, bypassing the n^+-emitter and keeping the device out of its forward-conduction mode. As the anode current becomes large, the potential drop across the shunt resistance will be sufficient to forward bias the gate-cathode junction, J_3, and bring the thyristor into forward conduction. The cathode shorts also provide a path for displacement current to flow without forward-biasing J_3. The dv/dt rating of the thyristor is thus improved and the forward-blocking characteristics by using cathode shorts. However, the shorts do cause a lowering of cathode current handling capability because of the loss of some of the cathode area (n^+-region) to the shorting pattern, an increase in the necessary gate current to obtain switching from forward-blocking to forward conduction and an increase in complexity of manufacturing of the thyristor. The loss of cathode area due to the shorting

structure is from 5% to 20%, depending on the type of thyristor. By careful design of the cathode short windows to the p-base, the holding current can be made lower than the latching current. This is important so that the thyristor will remain in forward conduction when used with varying load impedances.

3.4.2 Anode Shorts

A further increase in forward-blocking capability can be obtained by introducing anode shorts in addition to the cathode shorts. This reduces α_p in a similar manner that cathode shorts reduce α_n. An illustration of this is provided in Fig. 3.13. In this structure, both J_1 and J_3 are shorted (anode and cathode shorts), so that the forward-blocking capability of the thyristor is completely determined by the avalanche breakdown characteristics of J_2. Anode shorts will result in the complete loss of reverse-blocking capability and are only suitable for thyristors used in asymmetrical circuit applications.

3.4.3 Amplifying Gate

The cathode-shorting structure will reduce the gate sensitivity dramatically. To increase this sensitivity and yet retain the benefits of the cathode shorts, a structure called an amplifying gate (or regenerative gate) is used, as shown in Fig. 3.14 (and Fig. 3.9, right). When the gate current (1) is injected into the p-base through the pilot-gate contact, electrons are injected into the p-base by the n^+-emitter with a given emitter injection efficiency. These electrons traverse through the p-base (the time taken for this process is called the transit time) and accumulate near the depletion region. This negative charge accumulation leads to injection of holes from the anode. The device then turns on after a certain delay, dictated by the p-base transit time, and the pilot anode current (2) begins to flow through a small region near the pilot-gate contact as shown in Fig. 3.14.

This flow of pilot anode current corresponds to the initial sharp rise in the anode current waveform (phase I), as shown in Fig. 3.15. The device switching then goes into phase II, during which the anode current remains fairly constant, suggesting that the resistance of the region has reached its lower limit. This is due to the fact that the pilot anode current (2) takes a finite time to traverse through the p-base laterally and become the gate current for the main cathode area. The n^+-emitters start to inject electrons which traverse the p-base vertically and after a certain finite time (transit time of the p-base) reach the depletion region. The total time taken by the lateral traversal of pilot anode current and the electron transit time across the p-base is the reason for observing this characteristic phase II interval. The width of the phase II interval is comparable to the switching delay, suggesting that the p-base transit time is of primary importance. Once the main cathode region turns on, the resistance of the device decreases and the anode current begins to rise again (transition from phase II to III). From this time onward in the switching cycle, the plasma spreading velocity will dictate the rate at which the conduction area will increase. The current density during phases I and II can be quite large, leading to a considerable increase in the local temperature and device failure. The detailed effect of the amplifying gate on the

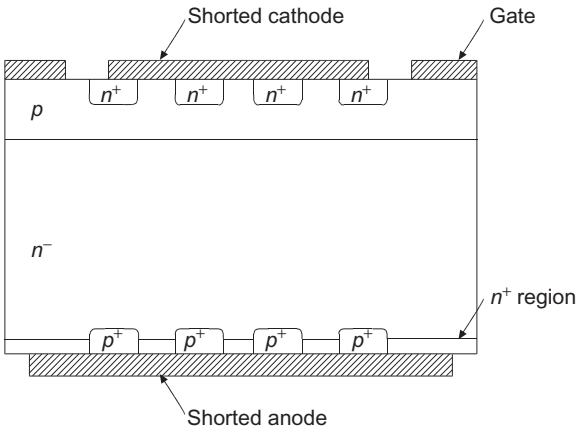


FIG. 3.13 Cross section showing integrated cathode and anode shorts.

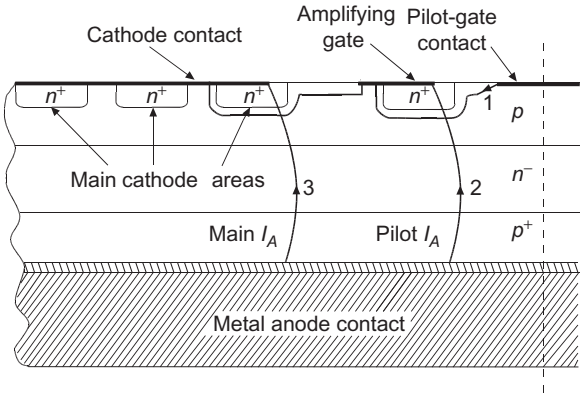


FIG. 3.14 Cross section showing the amplifying gate structure in a thyristor.

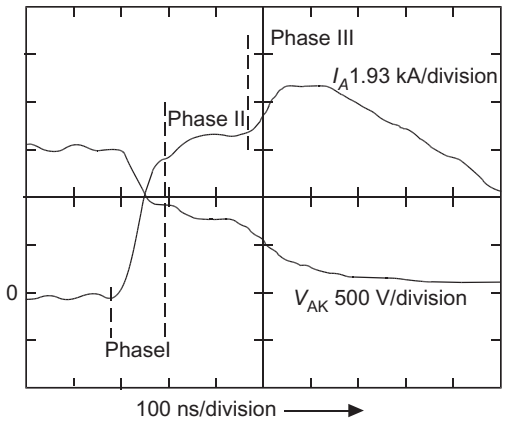


FIG. 3.15 Turn-on waveforms showing the effect of the amplifying gate in the anode current rise.

anode current rise will only be noticed at high levels of *di/dt* (in the range of 1000 A/μs), shown in Fig. 3.15. It can be concluded that the amplifying gate will increase gate sensitivity at the expense of some *di/dt* capability, as demonstrated by Sankaran [7]. This lowering of *di/dt* capability can be somewhat offset by an increase in gate-cathode interdigitation as previously discussed.

3.4.4 Temperature Dependencies

The forward-blocking voltage of an SCR has been shown to be reduced from 1350 V at 25°C to 950 V at −175°C in a near linear fashion [8]. Above 25°C, the forward-blocking capability is again reduced, due to changes in the minority carrier lifetime, which cause the leakage current to increase and the associated breakover voltage to decrease. Several dominant physical parameters associated with semiconductor devices are sensitive to temperature variations, causing their dependent device characteristics to change dramatically. The most important of these parameters are (i) the minority carrier lifetimes (which control the high-level injection lifetimes), (ii) the hole and electron mobilities, (iii) the impact ionization collision cross sections, and (iv) the free-carrier concentrations (primarily the ionized impurity atom concentration). Almost all of the impurity atoms are ionized at temperatures above 0°C, and so further discussion of the temperature effects on ionization is not relevant for normal operation. As the temperature increases above 25°C, the following trends are observed: the carrier lifetimes increase, giving longer recovery times and greater switching losses; the carrier mobilities are reduced, increasing the on-state voltage drop; and at very high temperatures, the intrinsic carrier concentration becomes sufficiently high that the depletion layer will not form and the device cannot switch off. A more detailed discussion of these physical parameters is beyond the scope of this book, but references are listed for those persons interested in pursuing relevant information about temperature effects.

It is well known that charge-carrier recombination events are more efficient at lower temperatures. This shows up as a larger potential drop during forward conduction and a shorter recovery time during turnoff. A plot of the anode current during turnoff, at various temperatures, for a typical GTO is shown in Fig. 3.16.

An approximate relation between the temperature and the forward drop across the n^--base of a thyristor is discussed in detail by Herlet [9] and Hudgins et al. [10]. Temperature-dependent equations relating the anode current density, J_A, and the applied anode-cathode voltage V_{AK} are also given in Ref. [10]; these include the junction potential drops in the device, the temperature dependence of the band-gap energy, and the n^--base potential drop. Data from measurements at forward current densities of approximately 100 A/cm^2 on a GTO rated for 1 kV symmetrical blocking give forward voltage drops of 1.7 V at −50°C and 1.8 V at 150°C.

3.5 Thyristor Parameters

Understanding of a thyristor's maximum ratings and electric characteristics is required for proper application. Use of a manufacturer's data sheet is essential for good design practice. *Ratings* are maximum or minimum values that set limits on device capability. A measure of device performance under specified operating conditions is a *characteristic* of the device. A summary of some of the maximum ratings that must be considered when choosing a thyristor for a given application

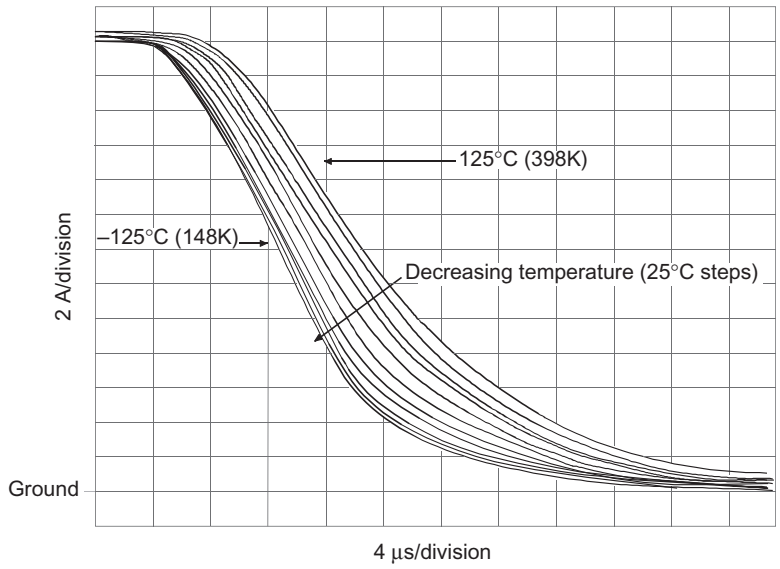


FIG. 3.16 Temperature effect on the anode current tail during turnoff.

TABLE 3.3 Thyristor maximum ratings specified by manufacturers

Symbol	Description
V_{RRM}	Peak repetitive reverse voltage
V_{RSM}	Peak nonrepetitive reverse voltage (transient)
$V_{R(DC)}$	DC reverse-blocking voltage
V_{DRM}	Peak repetitive forward off-state voltage
V_{DSM}	Peak nonrepetitive forward off-state voltage (transient)
$V_{D(DC)}$	DC forward-blocking voltage
$I_{T(RMS)}, I_{F(RMS)}$	RMS forward on-state current
$I_T(AV), I_{F(AV)}$	Average forward on-state current at specified case or junction temperature
$I_{TSM}, I_{F(TSM)}$	Peak one-cycle surge on-state current (values specified at 60 and 50 Hz)
I_{TGQ} (GTO)	Peak controllable current
I^2t	Nonrepetitive pulse overcurrent capability ($t = 8.3$ ms for a 60 Hz half cycle)
P_T	Maximum power dissipation
di/dt	Critical rate of rise of on-state current at specified junction temperature, gate current, and forward-blocking voltage
P_{GM} (P_{FGM} for GTO)	Peak gate power dissipation (forward)
P_{RGM} (GTO)	Peak gate power dissipation (reverse)
$P_{G(AV)}$	Average gate power dissipation
V_{FGM}	Peak forward gate voltage
V_{RGM}	Peak reverse gate voltage
I_{FGM}	Peak forward gate current
I_{RGM} (GTO)	Peak reverse gate current
T_{STG}	Storage temperature
T_j	Junction operating temperature
V_{RMS}	Voltage isolation (modules)

TABLE 3.4 Typical thyristor characteristic maximum and minimum values specified by manufacturers

Symbol	Description
V_{TM}, V_{FM}	Maximum on-state voltage drop (at specified junction temperature and forward current)
I_{DRM}	Maximum forward off-state current (at specified junction temperature and forward voltage)
I_{RRM}	Maximum reverse off-state current (at specified junction temperature and reverse voltage)
dv/dt	Minimum critical rate of rise of off-state voltage at specified junction temperature and forward-blocking voltage level
V_{GT}	Maximum gate trigger voltage (at specified temperature and forward applied voltage)
V_{GD}, V_{GDM}	Maximum gate nontrigger voltage (at specified temperature and forward applied voltage)
I_{GT}	Maximum gate trigger current (at specified temperature and forward applied voltage)
T_{gt} (GTO)	Maximum turn-on time (under specified switching conditions)
T_q	Maximum turn-off time (under specified switching conditions)
t_D	Maximum turn-on delay time (for specified test)
$R_{\Theta(J-C)}$	Maximum junction-to-case thermal resistance
$R_{\Theta(C-S)}$	Maximum case-to-sink thermal resistance (interface lubricated)

is provided in Table 3.3. Thyristor types shown in parentheses indicate a maximum rating unique to that device. Both forward and reverse repetitive and nonrepetitive voltage ratings must be considered, and a properly rated device must be chosen so that the maximum voltage ratings are never exceeded. In most cases, either forward- or reverse-voltage transients in excess of the nonrepetitive maximum ratings result in destruction of the device. The maximum root mean square (RMS) or average current ratings given are usually those which cause the junction to reach its maximum rated temperature. Because the maximum current will depend upon the current waveform and upon thermal conditions external to the device, the rating is usually shown as a function of case temperature and conduction angle. The peak single half-cycle surge-current rating must be considered, and in applications where the thyristor must be protected from damage by overloads, a fuse with an I^2t rating smaller than the maximum rated value for the device must be used. Maximum ratings for both forward and reverse gate voltage, current, and power also must not be exceeded.

The maximum rated operating junction temperature T_J must not be exceeded, since device performance, in particular voltage-blocking capability, will be degraded. Junction temperature cannot be measured directly but must be calculated from a knowledge of steady-state thermal resistance $R_{\Theta(J-C)}$ and the average power dissipation. For transients or surges, the transient thermal impedance ($Z_{\Theta(J-C)}$) curve must be used (provided in manufacturer's data sheets). The maximum average power dissipation P_T is related to the maximum rated operating junction temperature and the case temperature by the steady-state thermal resistance. In general, both the maximum dissipation and its derating with increasing case temperature are provided.

The number and type of thyristor characteristics specified varies widely from one manufacturer to another. Some characteristics are given only as typical values of minima or maxima, while many characteristics are displayed graphically. Table 3.4 summarizes some of the typical characteristics provided as maximum values. The maximum value means that the manufacturer guarantees that the device will not exceed the value given under the specified operating or switching conditions. A minimum value means that the manufacturer guarantees that the device will perform at least, as well as the characteristic given under the specified operating or switching conditions. Thyristor types shown in parenthesis indicate a characteristic unique to that device. Gate conditions of both voltage and current to ensure either nontriggered or triggered device operation are included. The turn-on and turn-off transients of the thyristor are characterized by switching times like the turn-off time listed in Table 3.4. The turn-on transient can be divided into three intervals: (i) gate-delay interval, (ii) turn-on of initial area, and (iii) spreading interval. The gate-delay interval is simply the time between application of a turn-on pulse at the gate and the time the initial cathode area turns on. This delay

TABLE 3.5 Symbols and definitions of major thyristor parameters

R_θ	Thermal Resistance	Specifies the degree of temperature rise per unit of power, measuring junction temperature from a specified external point. Defined when junction power dissipation results in steady-state thermal flow
$R_{\theta(J-A)}$	Junction-to-ambient thermal resistance	The steady-state thermal resistance between the junction and ambient
$R_{\theta(J-C)}$	Junction-to-case thermal resistance	The steady-state thermal resistance between the junction and case surface
$R_{\theta(J-S)}$	Junction-to-sink thermal resistance	The steady-state thermal resistance between the junction and the heat sink mounting surface
$R_{\theta(C-S)}$	Contact thermal resistance	The steady-state thermal resistance between the surface of the case and the heat sink mounting surface
Z_θ	Transient thermal impedance	The change of temperature difference between two specified points or regions at the end of a time interval divided by the step function change in power dissipation at the beginning of the same interval causing the change of temperature difference
$Z_{\theta(J-A)}$	Junction-to-ambient transient thermal impedance	The transient thermal impedance between the junction and ambient
$Z_{\theta(J-C)}$	Junction-to-case transient thermal impedance	The transient thermal impedance between the junction and the case surface
$Z_{\theta(J-S)}$	Junction-to-sink transient thermal impedance	The transient thermal impedance between the junction and the heat sink mounting surface
T_A	Ambient temperature	It is the temperature of the surrounding atmosphere of a device when natural or forced-air cooling is used and is not influenced by heat dissipation of the device
T_S	Sink temperature	The temperature at a specified point on the device heat sink
T_C	Case temperature	The temperature at a specified point on the device case
T_J	Junction temperature	The device junction temperature rating. Specifies the maximum and minimum allowable operation temperatures
T_{STG}	Storage temperature	Specifies the maximum and minimum allowable storage temperatures (with no electric connections)
V_{RRM}	Peak reverse-blocking voltage	Within the rated junction temperature range and with the gate terminal open circuited, specifies the repetitive peak reverse anode-to-cathode voltage applicable on each cycle
V_{RSM}	Transient peak reverse-blocking voltage	Within the rated junction temperature range and with the gate terminal open circuited, specifies the nonrepetitive peak reverse anode-to-cathode voltage applicable for a time width equivalent to less than 5 ms
$V_{R(DC)}$ SCR only	Dc reverse-blocking voltage	Within the rated junction temperature range and with the gate terminal open-circuited, specifies the maximum value for dc anode-to-cathode voltage applicable in the reverse direction

Continued

decreases with increasing gate-drive current and is of the order of a few microseconds. The second interval, the time required for turn-on of the initial area, is quite short, typically less than 1 μs. In general, the initial area turned on is a small percentage of the total useful device area. After the initial area turns on, conduction spreads (spreading interval or plasma spreading time) throughout the device in tens of microseconds for high speed or thyristors. The plasma spreading time may take up to hundreds of microseconds in large-area phase-control devices.

Table 3.5 lists many of the thyristor parameters that appear as listed values or as information on graphs. The definition of each parameter and the test conditions under which they are measured are given in the table as well.

3.6 Types of Thyristors

In recent years, most development effort has gone into continued integration of the gating and control electronics into thyristor modules and the use of MOS technology to create gate structures integrated into the thyristor itself. Many variations of this theme are being developed and some technologies should rise above the others in the years to come. Further details concerning most of the following discussion of thyristor types can be found in [11].

3.6.1 SCRs and GTOs

The highest power handling devices continue to be bipolar thyristors. High-powered thyristors are large diameter devices, some well in excess of 100 mm, and as such have a limitation on the rate of rise of anode current, a di/dt rating. The depletion capacitances around the p-n junctions, in particular the center junction J_2, limit the rate of rise in forward voltage that can be applied even after all the stored charge, introduced during conduction, is removed. The associated displacement current under application of forward voltage during the thyristor blocking state sets a dv/dt limit. Some effort in improving the voltage hold-off capability and overvoltage protection of conventional SCRs is underway by incorporating a lateral high-resistivity region to help dissipate the energy during

TABLE 3.5 Symbols and definitions of major thyristor parameters—cont'd

V_{DRM}	Peak forward-blocking voltage	Within the rated junction temperature range and with the gate terminal open circuited (SCR) or with a specified reverse voltage between the gate and cathode (GTO), specifies the repetitive peak off-state anode-to-cathode voltage applicable on each cycle. This does not apply for transient off-state voltage application
V_{DSM}	Transient peak forward-blocking voltage	Within the rated junction temperature range, and with the gate terminal open circuited (SCR), or with a specified reverse voltage between the gate and cathode (GTO), specifies the nonrepetitive off-state anode-to-cathode voltage applicable for a time width equivalent to less than 5 ms. This gives the maximum instantaneous value for nonrepetitive transient off-state voltage
$V_{D(DC)}$	Dc forward-blocking voltage	Within the rated junction temperature range and with the gate terminal open circuited (SCR) or with a specified reverse voltage between the gate and cathode (GTO), specifies the maximum value for dc anode-to-cathode voltage applicable in the forward direction
dv/dt	Critical rate of rise of off-state voltage $dv/dt = (0.632V_D)/\tau V_D$ is specified off-state voltage τ is time constant for exponential	At the maximum rated junction temperature range, and with the gate terminal open circuited (SCR), or with a specified reverse voltage between the gate and cathode (GTO), this specifies the maximum rate of rise of off-state voltage that will not drive the device from an off-state to an on-state when an exponential off-state voltage of specified amplitude is applied to the device
V_{TM}	Peak on-state voltage	At specified junction temperature, and when on-state current (50 or 60 Hz, half sine wave of specified peak amplitude) is applied to the device, indicates peak value for the resulting voltage drop
$I_{T(RMS)}$	RMS on-state current	At specified case temperature, indicates the RMS value for on-state current that can be continuously applied to the device
$I_{T(AV)}$	Average on-state current	At specified case temperature, and with the device connected to a resistive or inductive load, indicates the average value for forward current (sine half wave, commercial frequency) that can be continuously applied to the device
I_{TSM}	Peak on-state current	Within the rated junction temperature range, indicates the peak value for nonrepetitive on-state current (sine half wave, 50 or 60 Hz). This value indicated for one cycle or as a function of a number of cycles
I^2t	Current-squared time	The maximum, on-state, nonrepetitive short-time thermal capacity of the device and is helpful in selecting a fuse or providing a coordinated protection scheme of the device in the equipment. This rating is intended specifically for operation less than one half cycle of a 180 (degree) conduction angle sinusoidal wave form. The off-state blocking capability cannot be guaranteed at values near the maximum I^2t
di/dt	Critical rate of rise of on-state current	At specified case temperature, specified off-state voltage, specified gate conditions, and at a frequency of less than 60 Hz, indicates the maximum rate of rise of on-state current which the thyristor will withstand when switching from an off-state to an on-state, when using recommended gate drive
I_{RRM}	Peak reverse leakage current	At maximum rated junction temperature, indicates the peak value for reverse current flow when a voltage (sine half wave, 50 or 60 Hz, and having a peak value as specified for repetitive peak reverse-voltage rating) is applied in a reverse direction to the device
I_{DRM}	Peak forward-leakage current	At maximum rated junction temperature, indicates the peak value for off-state current flow when a voltage (sine half wave, 50 or 60 Hz, and having a peak value for repetitive off-state voltage rating) is applied in a forward direction to the device. For a GTO, a reverse voltage between the gate and cathode is specified
P_{GM} (SCR) P_{GFM} (GTO)	Peak gate power dissipation peak gate forward power dissipation	Within the rated junction temperature range, indicates the peak value for maximum allowable power dissipation over a specified time period, when the device is in forward conduction between the gate and cathode
$P_{G(AV)}$	Average gate power dissipation	Within the rated junction temperature range, indicates the average value for maximum allowable power dissipation when the device is forward-conducting between the gate and cathode

TABLE 3.5 Symbols and definitions of major thyristor parameters—cont'd

P_{GRM} GTO only	Peak gate reverse power dissipation	Within the rated junction temperature range, indicates the peak value for maximum allowable power dissipation in the reverse direction between the gate and cathode, over a specified time period
$P_{GR(AV)}$ GTO only	Average gate reverse power dissipation	Within the rated junction temperature range, indicates the average value for maximum allowable power dissipation in the reverse direction between the gate and cathode
I_{GFM}	Peak forward gate current	Within the rated junction temperature range, indicates the peak value for forward current flow between the gate and cathode
I_{GRM} GTO only	Peak reverse gate current	Within the rated junction temperature range, indicates peak value for reverse current that can be conducted between the gate and cathode
V_{GRM}	Peak reverse gate voltage	Within the rated junction temperature range, indicates the peak value for reverse voltage applied between the gate and cathode
V_{GFM}	Peak forward gate voltage	Within the rated junction temperature range, indicates the peak value for forward voltage applied between the gate and cathode
I_{GT}	Gate current to trigger	At a junction temperature of 25°C, and with a specified off-voltage, and a specified load resistance, indicates the minimum gate dc current required to switch the thyristor from an off-state to an on-state
V_{GT}	Gate voltage to trigger	At a junction temperature of 25°C, and with a specified off-state voltage, and a specified load resistance, indicates the minimum dc gate voltage required to switch the thyristor from an off-state to an on-state
V_{GDM} SCR only	Nontriggering gate voltage	At maximum rated junction temperature, and with a specified off-state voltage applied to the device, indicates the maximum dc gate voltage which will not switch the device from an off-state to an on-state
I_{TGQ} GTO only	Gate-controlled turn-off current	Under specified conditions, indicates the instantaneous value for on-current usable in gate control, specified immediately prior to device turn-off
R_θ	Thermal resistance	Specifies the degree of temperature rise per unit of power, measuring junction temperature from a specified external point. Defined when junction power dissipation results in steady-state thermal flow
t_{on} SCR only	Turn-on time	At specified junction temperature, and with a peak repetitive off-state voltage of half rated value, followed by device turn-on using specified gate current, and when specified on-state current of specified di/dt flows, indicated as the time required for the applied off-state voltage to drop to 10% of its initial value after gate current application. Delay time is the term used to define the time required for applied voltage to drop to 90% of its initial value following gate-current application. The time required for the voltage level to drop from 90% to 10% of its initial value is referred to as rise time. The sum of both these defines turn-on time
T_q SCR only	Turn-off time	Specified at maximum rated junction temperature. Device set up to conduct on-state current, followed by application of specified reverse anode-cathode voltage to quench on-state current and then increasing the anode-cathode voltage at a specified rate of rise as determined by circuit conditions controlling the point where the specified off-state voltage is reached. Turn-off time defines the minimum time which the device will hold its off-state, starting from the time on-state current reached zero until the time forward voltage is again applied (i.e., applied anode-cathode voltage becomes positive again)
t_{gt} GTO only	Turn-on time	When applying forward current to the gate, indicates the time required to switch the device from an off-state to an on-state
t_{qt} GTO only	Turn-off time	When applying reverse current to the gate, indicates the time required to switch the device from an on-state to an off-state

breakover. Most effort, though, is being placed in the further development of high-performance GTOs and IGCTs because of their controllability and to a lesser extent in optically triggered structures that feature gate circuit isolation.

High-voltage GTOs with symmetrical blocking capability require thick n^--base regions to support the high electric field. The addition of an n^+ buffer layer next to the p^+-anode allows high-voltage forward-blocking and a low forward voltage drop during conduction because of the thinner n^--base required. Cylindrical anode shorts have been incorporated to facilitate excess carrier removal from the n^--base during turnoff and still retain the high blocking capability. This device structure can control 200 A, operating at 900 Hz, with a 6 kV hold-off. Some of the design trade-off between the n^--base width and turn-off energy losses in these structures has been determined. A similar GTO incorporating an n^+-buffer layer and a *pin* structure has

been fabricated that can control up to 1 kA (at a forward drop of 4 V) with a forward-blocking capability of 8 kV. A reverse conducting GTO has been fabricated that can block 6 kV in the forward direction, interrupt a peak current of 3 kA, and has a turn-off gain of about 5.

The IGCT is a modified GTO structure. It is designed and manufactured so that it commutates all of the cathode current away from the cathode region and diverts it out of the gate contact. The IGCT is similar to a GTO in structure except that it always has a low-loss *n*-buffer region between the n^--base and *p*-emitter. The IGCT device package is designed to result in a very low parasitic inductance and is integrated with a specially designed gate-drive circuit. The gate drive contains all the necessary *di/dt* and *dv/dt* protection; the only connections required are a low-voltage power supply for the gate drive and an optical signal for controlling the gate. The specially designed gate drive and ring-gate package circuit allows the IGCT to be operated without a snubber circuit and to switch with a higher anode *di/dt* than a similar GTO. At blocking voltages of 4.5 kV and higher, the IGCT provides better performance than a conventional GTO. The speed at which the cathode current is diverted to the gate (di_{GQ}/dt) is directly related to the peak snubberless turn-off capability of the IGCT. The gate-drive circuit can sink current for turn-off at di_{GQ}/dt values in excess of 7000 A/μs. This hard gate drive results in a low charge storage time of about 1 μs. The low storage time and the fail-short mode make the IGCT attractive for high-power, high-voltage series applications; examples include high-power converters in excess of 100 MVA, static volt-ampere reactive (VAR) compensators, and converters for distributed generation such as wind power.

3.6.1.1 On-State Characteristics

In the on-state, the GTO operates in a similar manner to the thyristor. If the anode current remains above the holding current level, then positive gate drive may be reduced to zero, and the GTO will remain in conduction. However, as a result of the turn-off ability of the GTO, it does possess a higher holding current level than the standard thyristor, and in addition, the cathode of the GTO thyristor is subdivided into small finger elements to assist turn-off. Thus, if the GTO thyristor anode current transiently dips below the holding current level, localized regions of the device may turn off, thus forcing a high anode current back into the GTO at a high rate of rise of anode current after this partial turnoff. This situation could be potentially destructive. It is recommended, therefore, that the positive gate drive is not removed during conduction but is held at a value $I_{G(ON)}$, where $I_{G(ON)}$ is greater than the maximum critical trigger current (I_{GT}) over the expected operating temperature range of the GTO thyristor.

Fig. 3.17 shows the typical on-state *V-I* characteristics for a 4000 1A, 4500 V GTO from Dynex range of GTOs [1] at junction temperatures of 25 and 125°C. The curves can be approximated to a straight line of the form

$$V_{TM} = V_0 + IR_0 \tag{3.3}$$

where V_0 = voltage intercept models the voltage across the cathode and anode forward-biased junctions and R_0 = on-state resistance. When average and RMS values of on-state current (I_{TAV}, I_{TRMS}) are known, then the on-state power dissipation P_{ON} can be determined using V_0 and R_0. That is,

$$P_{ON} = V_0 I_{TAV} + R_0 I_{TRMS}^2 \tag{3.4}$$

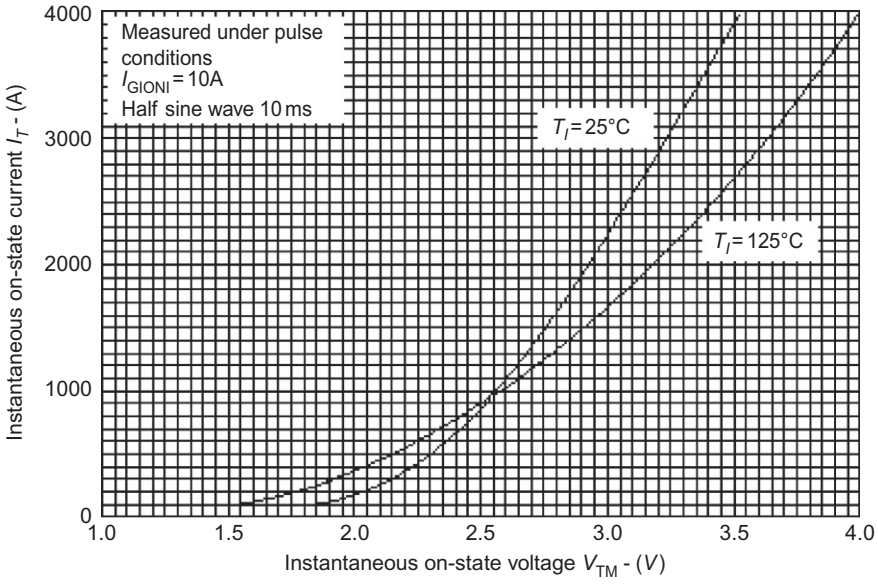


FIG. 3.17 *V-I* characteristics of GTO [12].

3.6.1.2 Off-State Characteristics

Unlike the standard thyristor, the GTO does not include cathode emitter shorts to prevent nongated turn-on effects due to dv/dt induced forward-biased leakage current. In the off-state of the GTO, steps should, therefore, be taken to prevent such potentially dangerous triggering. This can be accomplished by either connecting the recommended value of resistance between the gate and the cathode (R_{GK}) or by maintaining a small reverse bias on the gate contact ($V_{RG} = -2$ V). This will prevent the cathode emitter becoming forward biased and therefore sustain the GTO thyristor in the off-state.

The peak off-state voltage is a function of resistance R_{GK}. This is shown in Fig. 3.18. Under ordinary operating conditions, GTOs are biased with a negative gate voltage of around −15 V supplied from the gate-drive unit during the off-state interval. Nevertheless, provision of R_{GK} may be desirable design practice in the event of the gate-drive failure for any reason ($R_{GK} < 1.5\,\Omega$ is recommended for a large GTO). R_{GK} dissipates energy and hence adds to the system losses.

3.6.1.3 Rate of Rise of Off-State Voltage (dv_D/dt)

The rate of rise of off-state voltage (dv_D/dt) depends on the resistance R_{GK} connected between the gate and the cathode and the reverse bias applied between the gate and the cathode. This relationship is shown in Fig. 3.19.

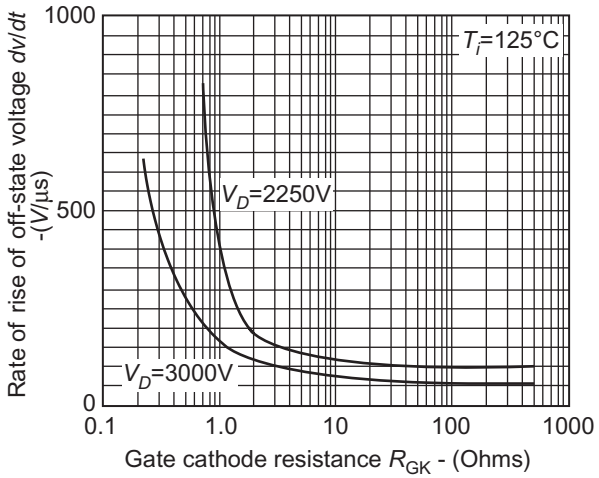


FIG. 3.19 dv_D/dt versus R_{GK} [12].

3.6.1.4 Gate Triggering Characteristics

The gate trigger current (I_{GT}) and the gate trigger voltage (V_{GT}) are both dependent on junction temperature T_j as shown in Fig. 3.20. During the conduction state of the GTO, a certain value of gate current must be supplied, and this value should be larger than the I_{GT} at the lowest junction temperature at which the GTO operates. In dynamic conditions, the specified I_{GT} is not sufficient to trigger the GTO switching from higher

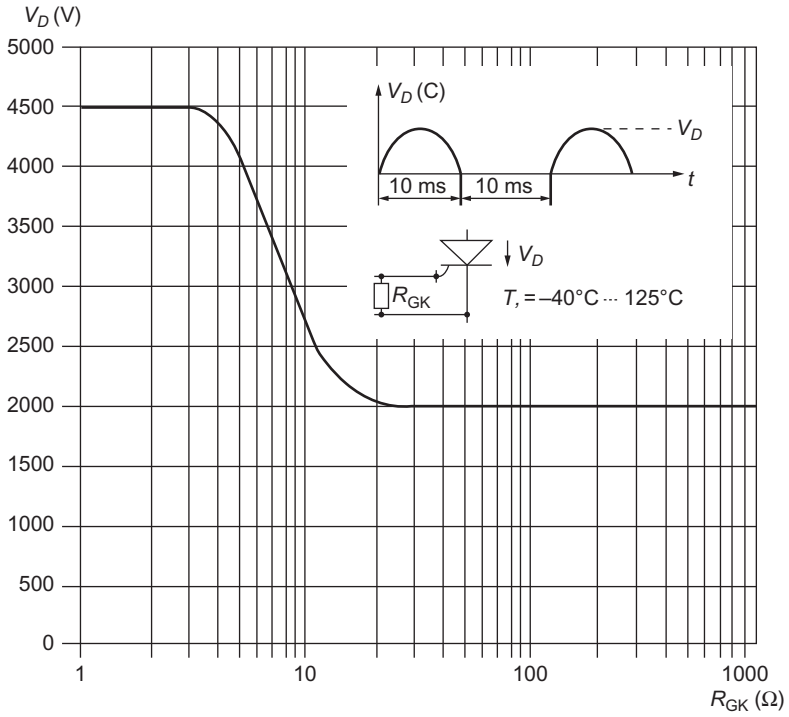


FIG. 3.18 GTO blocking voltage versus R_{GK} [12].

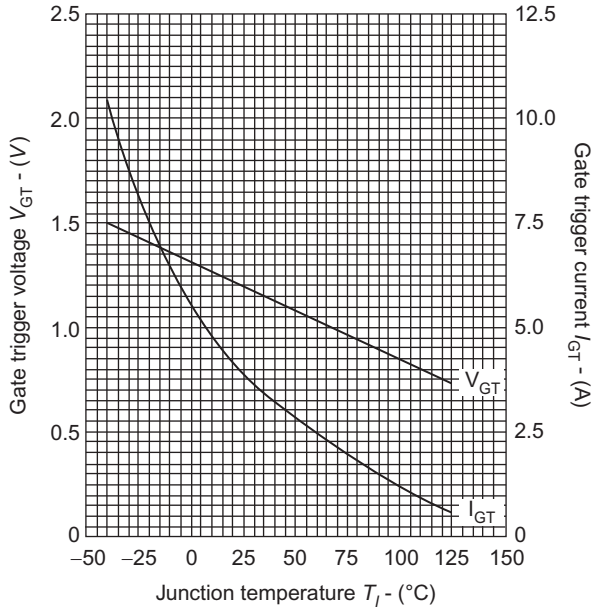


FIG. 3.20 GTO trigger characteristics (see data sheet in Ref. [1]).

voltage and high *di*/*dt*. In practice, a much high peak gate current I_{GM} (in order of 10 times I_{GT}) at T_j min is recommended to obtain good turn-on performance.

3.6.1.5 GTO Switching Phases

The switching process of a GTO thyristor goes through four operating phases.

Turn-on

A GTO has a highly interdigitated gate structure with no regenerative gate. Thus, it requires a large initial gate trigger pulse. A typical turn-on wave diagrams and their important parameters are shown in Fig. 3.21. Minimum and maximum values of I_{GM} can be derived from the device data sheet. A value of di_g/dt is given in device characteristics of the data sheet, against turn-on time. The rate of rise of gate current, di_g/dt will affect the device turn-on losses. The duration of the I_{GM} pulse should not be less than half the minimum on time given in data sheet ratings. A longer period will be required if the anode current *di*/*dt* is low such that I_{GM} is maintained until a sufficient level of anode current is established.

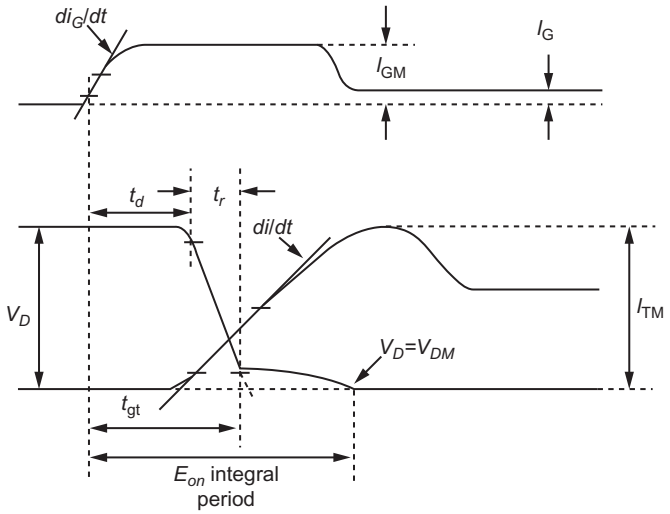


FIG. 3.21 A typical GTO turn-on wave diagrams [13].

On-state

Once the GTO is turned on, forward gate current must be continued for the whole of the conduction period. Otherwise, the device will not remain in conduction during the on-state period. If large negative *di*/*dt* or anode current to reversal occurs in the circuit during the on-state, then higher values of I_G may be required. Much lower values of I_G are, however, required when the device has heated up.

Turn-off

The turn-off performance of a GTO is greatly influenced by the characteristics of the gate turn-off circuit. Thus, the characteristics of the turn-off circuit must match with the device requirements. Fig. 3.22 shows the typical anode and gate currents during the turn-off. The gate turn-off process involves the extraction of the gate charge, the gate avalanche period, and the anode current decay. The amount of the charge extraction is a device parameter and its value is not significantly affected by the external circuit conditions. The initial peak turn-off current and turn-off time, which are important parameters of the turning-off process, depend on the external circuit components. The device data sheet gives typical values for I_{GQ}.

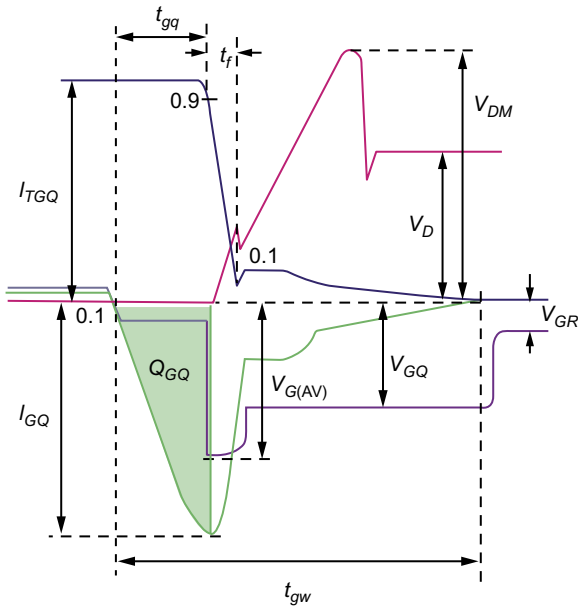


FIG. 3.22 A typical GTO turn-off currents [13].

The turn-off circuit arrangement of a GTO is shown in Fig. 3.22. The turn-off current gain of a GTO is low, typically 6–15. Thus, for a GTO with a turn-off gain of 10, it will require a turn-off gate current of 10 A to turn off an on-state of 100 A. A charged capacitor C is normally used to provide the required turn-off gate current. Inductor L limits the turnoff di/dt of the gate current through the circuit formed by R_1, R_2, SW_1, and L. The gate circuit supply voltage V_{GS} should be selected to give the required value of V_{GQ}. The values of R_1 and R_2 should also be minimized.

Off-state period

During the off-state period, which begins after the fall of the tail current to zero, the gate should ideally remain reverse biased. This reverse bias ensures maximum blocking capability and dv/dt rejection. The reverse bias can be obtained either by keeping SW_1 closed during the whole off-state period or via a higher impedance circuit SW_2 and R_3 provided a minimum negative voltage exits. This higher impedance circuit SW_2 and R_3 must sink the gate leakage current.

In case of a failure of the auxiliary supplies for the gate turn-off circuit, the gate may be in reverses biased condition, and the GTO may not be able to block the voltage. To ensure blocking voltage of the device is maintained, then a minimum gate-cathode resistance (R_{GK}) should be used. The value of R_{GK} for a given line voltage can be derived from the data sheet.

3.6.1.6 GTO SPICModel

A GTO may be modeled with two transistors shown in Fig. 3.2. However, a GTO model [14] consisting of two thyristors, which are connected in parallel, yields improved on-state, turn-on, and turn-off characteristics. The model is shown in Fig. 3.23 with four transistors.

When the anode-to-cathode voltage V_{AK} is positive and there is no gate voltage, the GTO model will be in the off-state like a standard thyristor. If a positive voltage (V_{AK}) is applied to the anode with respect to the cathode and no gate pulse applied, $I_{B1} = I_{B2} = 0$ and therefore $I_{C1} = I_{C2} = 0$. Thus, no anode current will flow, $I_A = I_K = 0$.

When a small voltage is applied to the gate, then I_{B2} is nonzero, and therefore, both $I_{C1} = I_{C2} = 0$ are nonzero. Thus, the internal circuit will conduct, and there will a current flow from the anode to the cathode.

When a negative gate pulse is applied to the GTO model, the PNP junction near to the cathode will behave as a diode. The diode will be reverse biased since the gate voltage is negative with to the cathode. Therefore, the GTO will stop conduction.

When the anode-to-cathode voltage is negative, that is, the anode voltage is negative with respect to the cathode, the GTO model will act like a reverse biased diode. This is because the PNP transistor will see a negative voltage at the emitter and the NPN transistor will see a positive voltage at the emitter. Therefore, both transistors will be in the off-state and hence the GTO will not conduct. The SPICE subcircuit description of the GTO model will be as follows:

Subcircuit		1		2	3	GTO subcircuit definition
*Terminal			Anode	Cathode	Gate	
Q1	5	4	1 DMOD1		PNP	PNP transistor with model DMOD1
Q3	7	6	1 DMOD1		PNP	
Q2	4	5	2 DMOD2		NPN	PNP transistor with model DMOD2
Q4	6	7	2 DMOD2		NPN	
R1	7	5	10 Ω			
R2	6	4	10 Ω			
R3	3	7	10 Ω			
MODEL		DMOD1			PNP	Model statement for a PNP transistor
MODEL		DMOD2			NPN	Model statement for an NPN transistor
ENDS						End of subcircuit definition

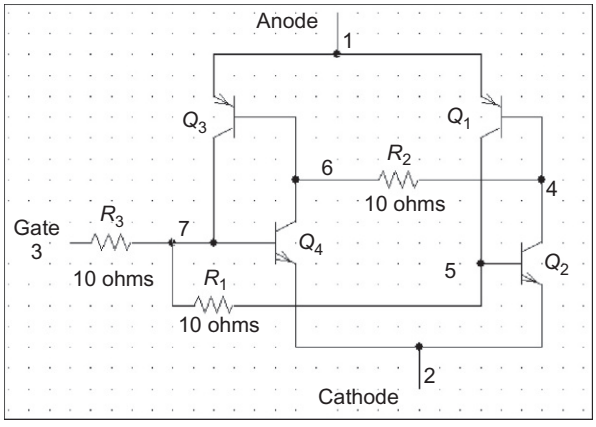


FIG. 3.23 Four-transistor GTO model.

3.6.2 MOS-Controlled Thyristors

An effort to combine the advantages of bipolar junction and field-effect structures has resulted in hybrid devices such as the IGBT and the MOS-controlled thyristor (MCT). While an IGBT is an improvement over a bipolar junction transistor (BJT) using a MOSFET to turn-on and turn-off current, an MCT is an improvement over a thyristor with a pair of MOSFETs to turn-on and turn-off current. The MCT overcomes several of the limitations of the existing power devices and promises to be a better switch for the future.

The cross section of the p-type MCT unit cell is given in Fig. 3.24. When the MCT is in its forward-blocking state and

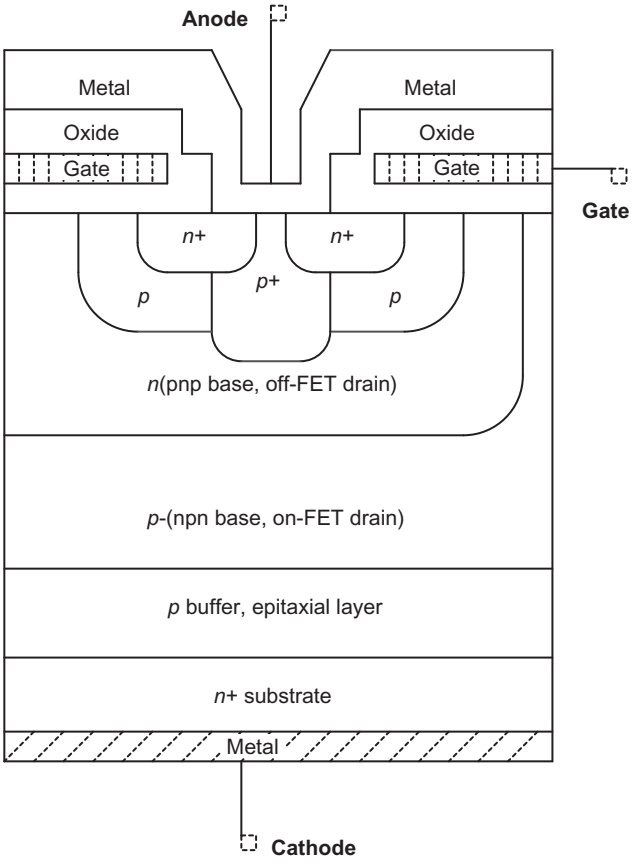


FIG. 3.24 Cross section of unit cell of a *p*-type MCT.

a negative gate-anode voltage is applied, an inversion layer is formed in the *n*-doped material that allows holes to flow laterally from the *p*-emitter (*p*-channel FET source) through the channel to the *p*-base (*p*-channel FET drain). This hole flow is the base current for the *npn* transistor. The *n*-emitter then injects electrons which are collected in the n^--base, causing the *p*-emitter to inject holes into the n^--base so that the *pnp* transistor is turned on and latches the MCT. The MCT is brought out of conduction by applying a positive gate-anode voltage. This signal creates an inversion layer that diverts electrons in the n^--base away from the *p*-emitter and into the heavily doped *n*-region at the anode. This *n*-channel FET current amounts to a diversion of the *pnp* transistor base current so that its base-emitter junction turns off. Holes are then no longer available for collection by the *p*-base. The elimination of this hole current (*npn* transistor base current) causes the *npn* transistor to turn off. The remaining stored charge recombines and returns the MCT to its blocking state.

The seeming variability in fabrication of the turn-off FET structure continues to limit the performance of MCTs, particularly current interruption capability, though these devices can handle two to five times the conduction current density of IGBTs. Numerical modeling and its experimental verification show that ensembles of cells are sensitive to current filamentation during turnoff. All MCT device designs suffer from the problem of current interruption capability. Turn-on is relatively simple, by comparison; both the turn-on and conduction properties of the MCT approach the one-dimensional thyristor limit.

Other variations on the MCT structure have been demonstrated, namely, the emitter switched thyristor (EST) and the dual-gate emitter switched thyristor (DG-EST) [15]. These comprise integrated lateral MOSFET structures that connect a floating thyristor *n*-emitter region to an n^+ thyristor cathode region. The MOS channels are in series with the floating *n*-emitter region, allowing triggering of the thyristor with electrons from the n^--base and interruption of the current to initiate turn-off. The DG-EST behaves as a dual-mode device, with the two gates allowing an IGBT mode to operate during switching and a thyristor mode to operate in the on-state.

3.6.2.1 Equivalent Circuit and Switching Characteristics

The SCR is a four-layer *pnpn* device with a control gate, and applying a positive gate pulse turns it on when it is forward biased. The regenerative action in the device helps to speed up the turn-on process and to keep it in the "ON" state even after the gate pulse is removed. The MCT uses an auxiliary MOS device (PMOSFET) to turn-on, and this simplifies the gate control. The turn-on has all the characteristics of a power MOSFET. The turnoff is accomplished using another MOSFET (NMOSFET), which essentially diverts the base current of one of the BJTs and breaks the regeneration.

The transistor-level equivalent circuit of a P-channel MCT and the circuit symbol are shown in Fig. 3.25. The MCT is modeled as an SCR merged with a pair of MOSFETs. The SCR consists of the bipolar junction transistors (BJTs) Q_1 and Q_2, which are interconnected to provide regenerative feedback such that the transistors drive each other into saturation. Of the two MOSFETs, the PMOS located between the collector and emitter of Q_2 helps to turn the SCR on, and the NMOS located across the base-emitter junction of Q_2 turns it off. In the actual fabrication, each MCT is made up of a large number (~100,000) cells, each of which contains a wide-base *npn* transistor and a narrow-base *pnp* transistor. While each *pnp* transistor in a cell is provided with an *N*-channel MOSFET across its emitter and base, only a small percentage (~4%) of *pnp* transistors are provided with P-channel MOSFETs across their emitters and collectors. The small percentage of PMOS cells in an MCT provides just enough current for turn-on and the large number of NMOS cells provide plenty of current for turnoff.

3.6.2.2 Turn-On and Turn-Off

When the MCT is in the forward-blocking state, it can be turned on by applying a negative pulse to its gate with respect to the anode. The negative pulse turns on the PMOSFET (On-FET) whose drain current flows through the base-emitter

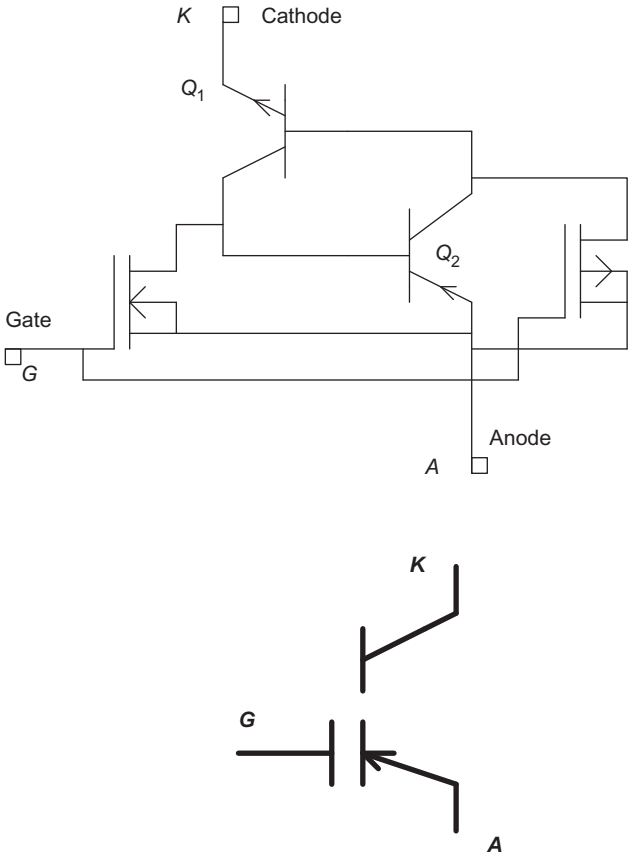


FIG. 3.25 Equivalent circuit and symbol of an MCT.

junction of Q_1 (*npn*), thereby turning it on. The regenerative action within $Q_1 - Q_2$ turns the MCT on into full conduction within a very short time and maintains it even after the gate pulse is removed. The MCT turns on without a plasma spreading phase, giving a high *di/dt* capability and ease of overcurrent protection. The on-state resistance of an MCT is slightly higher than that of an equivalent thyristor because of the degradation of the injection efficiency of the n^+-emitter/*p*-base junction. Also, the peak current rating of an MCT is much higher than its average or *rms* current rating.

An MCT will remain in the "ON" state until the device current is reversed or a turn-off pulse is applied to its gate. Applying a positive pulse to its gate turns off a conducting MCT. The positive pulse turns on the NMOSFET (Off-FET), thereby diverting the base current of Q_2 (*pnp*) away to the anode of the MCT and breaking the latching action of the SCR. This stops the regenerative feedback within the SCR and turns the MCT off. All the cells within the device are to be turned off at the same time to avoid a sudden increase in current density. When the Off-FETs are turned on, the SCR section is heavily shorted and this results in a high *dv/dt* rating for the MCT. The highest current that can be turned off with the application of a gate bias is called the "maximum controllable current." The MCT can be gate controlled if the device current is less than the maximum controllable current. For smaller device currents, the width of the turn-off pulse is not critical. However, for larger currents, the gate pulse has to be wider and more often has to occupy the entire off-period of the switch.

3.6.2.3 Comparison of MCT and Other Power Devices

An MCT can be compared with a power MOSFET, a power BJT, and an IGBT of similar voltage and current ratings. The operation of the devices is compared under on-state, off-state, and transient conditions. The comparison is simple and very comprehensive.

The current density of an MCT is ≈70% higher than that of an IGBT having the same total current [16]. During its on-state, an MCT has a lower conduction drop compared with other devices. This is attributed to the reduced cell size and the absence of emitter shorts present in the SCR within the MCT. The MCT also has a modest negative temperature coefficient at lower currents with the temperature coefficient turning positive at larger current [16]. Fig. 3.26 shows the conduction drop as a function of current density. The forward drop of a 50 A MCT at 25°C is around 1.1 V, while that for a comparable IGBT is over 2.5 V. The equivalent voltage drop calculated from the value of r_{DS}(ON) for a power MOSFET will be much higher. However, the power MOSFET has a much lower delay time (30 ns) compared with that of an MCT (300 ns). The turn-on of a power MOSFET can be so much faster than an MCT or an IGBT; therefore, the switching losses would be negligible compared with the conduction losses. The turn-on of an IGBT is intentionally slowed down to control the reverse recovery of the freewheeling diode used in inductive switching circuits [17].

The MCT can be manufactured for a wide range of blocking voltages. Turn-off speeds of MCTs are supposed to be higher as initially predicted. The turn-on performance of Generation-2 MCTs is reported to be better compared with Generation-1 devices. Even though the Generation-1 MCTs have higher turn-off times compared with IGBTs, the newer ones with higher radiation (hardening) dosage have comparable turn-off times. At present, extensive development activity in IGBTs

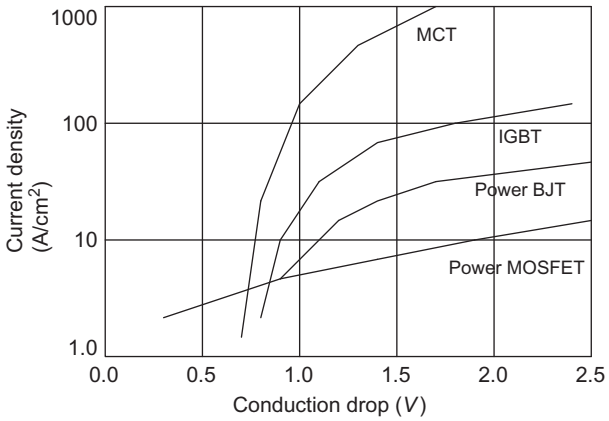


FIG. 3.26 Comparison of forward drop for different devices.

has resulted in high-speed switched mode power supply (SMPS) IGBTs that can operate at switching speeds ≈150 kHz [18]. The turn-off delay time and the fall time for an MCT are much higher compared with a power MOSFET, and they are found to increase with temperature [16]. Power MOSFETs become attractive at switching frequencies above 200 kHz, and they have the lowest turn-off losses among the three devices.

The turn-off safe operating area (SOA) is better in the case of an IGBT than an MCT. For an MCT, the full switching current is sustainable at ≈50%–60% of the breakdown voltage rating, while for an IGBT, it is about 80%. The use of capacitive snubbers becomes necessary to shape the turn-off locus of an MCT. The addition of even a small capacitor improves the SOA considerably.

The MCT has a MOS gate similar to a power MOSFET or an IGBT, and hence, it is easy to control. In a PMCT, the gate voltage must be applied with respect to its anode. A negative voltage below the threshold of the On-FET must be applied to turn on the MCT. The gate voltage should fall within the specified steady-state limits in order to give a reasonably low delay time and to avoid any gate damage due to overvoltage [17]. Similar to a GTO, the gate voltage rise time has to be limited to avoid hot spots (current crowding) in the MCT cells. A gate voltage less than −5 V for turnoff and greater than 10 V for turn-on ensures proper operation of the MCT. The latching of the MCT requires that the gate voltage be held at a positive level in order to keep the MCT turned off.

Because the peak-to-peak voltage levels required for driving the MCT exceed those of other gate-controlled devices, the use of commercial drivers is limited. The MCT can be turned on and off using a push-pull pair with discrete NMOS-PMOS devices, which, in turn, are driven by commercial integrated circuits (ICs). However, some drivers developed by MCT manufacturers are not commercially available [17].

A Baker's clamp push-pull can also be used to generate gate pulses of negative and positive polarity of adjustable width for driving the MCT [19–21]. The Baker's clamp ensures that the push-pull transistors will be in the quasisaturated state prior to turnoff, and this results in a fast switching action. Also, the negative feedback built into the circuit ensures satisfactory operation against variations in load and temperature. A similar circuit with a push-pull transistor pair in parallel with a pair of power BJTs is available [22]. An intermediate section, with a BJT that is either cut off or saturated, provides −10 V and +15 V through potential division.

3.6.2.4 Protection of MCTs

Paralleling of MCTs

Similar to power MOSFETs, MCTs can be operated in parallel. Several MCTs can be paralleled to form larger modules with only slight derating of the individual devices provided the devices are matched for proper current sharing. In particular, the forward voltage drops of individual devices have to be matched closely.

Overcurrent protection

The anode-to-cathode voltage in an MCT increases with its anode current, and this property can be used to develop a protection scheme against overcurrent [19,20]. The gate pulses to the MCT are blocked when the anode current and hence the anode-to-cathode voltage exceed a preset value. A Schmitt trigger comparator is used to allow gate pulses to the MCT when it is in the process of turning on, during which time the anode voltage is relatively large and decreasing.

Snubbers

As with any other power device, the MCT is to be protected against switching-induced transient voltage and current spikes by using suitable snubbers. The snubbers modify the voltage and current transients during switching such that the switching trajectory is confined within the SOA. When the MCT is operated at high frequencies, the snubber increases the switching loss due to the delayed voltage and current responses. The power circuit of an MCT chopper including an improved snubber circuit is shown in Fig. 3.27 [19,21]. The turn-on snubber consists of L_s and DL_S, and the turn-off snubber consists of R_s, C_s, and DL_S. The series-connected turn-on snubber reduces the rate of change of the anode current dI_A/dt. The MCT does not support V_s until the current through the freewheeling diode reaches zero at turn-on. The turn-off snubber helps to reduce the peak power and the total power dissipated by the MCT by reducing the voltage across the MCT when the anode current decays to zero. The analysis and design of the snubber and the effect of the snubber on switching loss and EMI are given in Refs. [19] and [21]. An alternative snubber configuration for the two MCTs in an ac-ac converter has also been reported [22]. This snubber uses only one capacitor and one inductor for both the MCT switches (PMCT and NMCT) in a power-converter leg.

Simulation model of an MCT

The operation of power converters can be analyzed using PSPICE and other simulation software. As it is a new device,

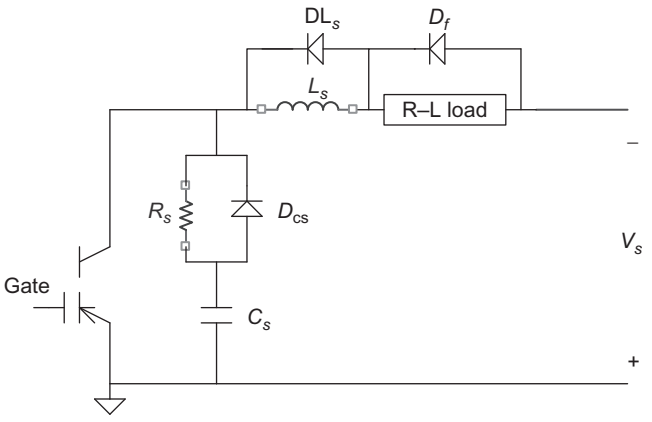


FIG. 3.27 An MCT chopper with turn-on and turn-off snubbers.

models of MCTs are not provided as part of the simulation libraries. However, an appropriate model for the MCT would be helpful in predicting the performance of novel converter topologies and in designing the control and protection circuits. Such a model must be simple enough to keep the simulation time and effort at a minimum and must represent most of the device properties that affect the circuit operation. The PSPICE models for Harris PMCTs are provided by the manufacturer and can be downloaded from the internet. However, a simple model presenting most of the characteristics of an MCT is available [23,24]. It is derived from the transistor-level equivalent circuit of the MCT by expanding the SCR model already reported the literature. The improved model [24] is capable of simulating the breakover and breakdown characteristics of an MCT and can be used for the simulation of high-frequency converters.

3.6.3 Generation-1 and Generation-2 MCTs

The Generation-1 MCTs were commercially introduced by Harris Semiconductors in 1992. However, the development of Generation-2 MCTs is continuing. In Gen-2 MCTs, each cell has its own turn-on field-effect transistor (FET). Preliminary test results in Generation-2 devices and a comparison of their performance with those of Generation-1 devices and high-speed IGBTs are available [25,26]. The Generation-2 MCTs have a lower forward drop compared with the Generation-1 MCTs. They also have a higher *di/dt* rating for a given value of capacitor used for discharge. During hard switching, the fall time and the switching losses are lower for the Gen-2 MCTs. The Gen-2 MCTs have the same conduction loss characteristics as Gen-1 with drastic reductions in turn-off switching times and losses [27].

Under zero-current switching conditions, Gen-2 MCTs have negligible switching losses [27]. Under zero-voltage switching, the turn-off losses in a Gen-2 device are one-half to one-fourth (depending on temperature and current level) the turn-off losses in Gen-1 devices. In all soft-switching applications, the predominant loss, namely, the conduction loss, reduces drastically allowing the use of fewer switches in a module.

3.6.4 *N*-channel MCT

The PMCT discussed in this chapter uses an NMOSFET for turnoff, and this results in a higher turn-off current capability. The PMCT can only replace a P-channel IGBT and inherits all the limitations of a P-channel IGBT. The results of a 2-D simulation show that the NMCT can have a higher controllable current [27]. It is reported that NMCT versions of almost all Harris PMCTs have been fabricated for analyzing the potential for a commercial product [17]. The NMCTs are also being evaluated for use in zero-current soft-switching applications. However, the initial results are not quite encouraging in that the peak turn-off current of an NMCT is one-half to one-third of the value achievable in a PMCT. It is hoped that the NMCTs will eventually have a lower switching loss and a larger SOA as compared with PMCTs and IGBTs.

3.6.5 Base Resistance-Controlled Thyristor [28]

The base resistance-controlled thyristor (BRT) is another gate-controlled device that is similar to the MCT but with a different structure. The Off-FET is not integrated within the *p*-base region but is formed within the n^--base region. The diverter region is a shallow *p*-type junction formed adjacent to the *p*-base region of the thyristor. The fabrication process is simpler for this type of structure. The transistor-level equivalent circuit of a BRT is shown in Fig. 3.28.

The BRT will be in the forward-blocking state with a positive voltage applied to the anode and with a zero gate bias. The forward-blocking voltage will be equal to the breakdown voltage of the open-base *pnp* transistor. A positive gate bias turns on the BRT. At low current levels, the device behaves similarly to an IGBT. When the anode current increases, the operation changes to thyristor mode resulting in a low forward drop. Applying a negative voltage to its gate turns off the BRT. During the turn-off process, the anode current is diverted from the n^+ emitter to the diverter. The BRT has a current tail during turnoff that is similar to an MCT or an IGBT.

3.6.6 MOS Turn-off Thyristor [29]

The MOS turn-off (MTO) thyristor or the MTOT is a replacement for the GTO and it requires a much smaller gate drive. It is more efficient than a GTO; it can have a maximum blocking voltage of about 9 kV, and it will be used to build power converters in the 1–20 MVA range. Silicon Power Corporation (SPCO) manufactures the device.

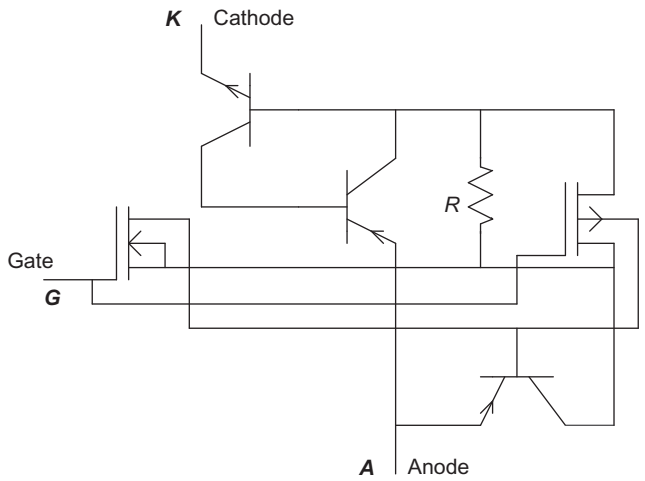


FIG. 3.28 Equivalent circuit of base resistance-controlled thyristor (BRT).

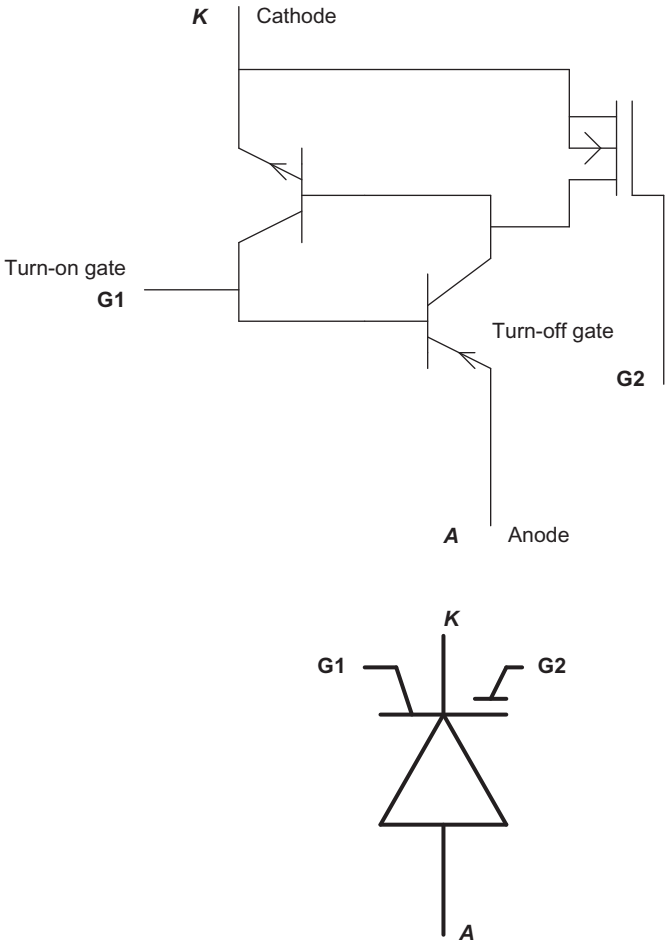


FIG. 3.29 Equivalent circuit and symbol of a MOS turn-off (MTO) thyristor.

The transistor-level equivalent circuit of the MTOT (hybrid design) and the circuit symbol are shown in Fig. 3.29. Applying a current pulse at the turn-on gate (G_1), as with a conventional GTO, turns on the MTOT. The turn-on action, including regeneration, is similar to a conventional SCR. Applying a positive voltage pulse to the turn-off gate (G_2), as with an MCT, turns off the MTOT. The voltage pulse turns on the FET, thereby shorting the emitter and base of the *npn* transistor and breaking the regenerative action. The MTOT is a faster switch than a GTO in that it is turned off with a reduced storage time compared with a GTO. The disk-type construction allows double-sided cooling.

3.6.7 Static Induction Thyristors

An SITh or FCTh has a cross section similar to that shown in Fig. 3.30. Other SITh configurations have surface-gate structures. The device is essentially a *pin* diode with a gate structure that can pinch-off anode current flow. High-power SIThs have a subsurface gate (buried-gate) structure to allow larger cathode

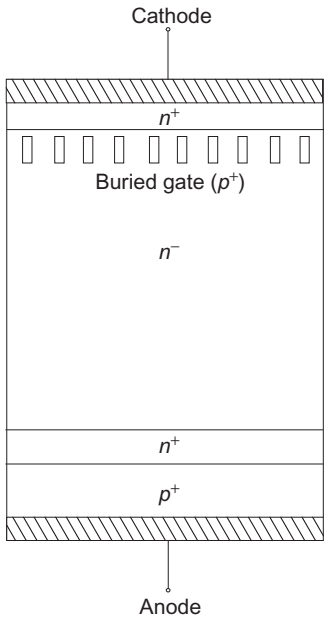


FIG. 3.30 Cross section of an SITh or FCT.

areas to be utilized, and hence, larger current densities are possible.

Planar gate devices have been fabricated with blocking capabilities of up to 1.2 kV and conduction currents of 200 A, while step-gate (trench-gate) structures have been produced that are able to block up to 4 kV and conduct 400 A. Similar devices with a "Verigrid" structure have been demonstrated that can block 2 kV and conduct 200 A, with claims of up to 3.5 kV blocking and 200 A conduction. Buried-gate devices that block 2.5 kV and conduct 300 A have also been fabricated. Recently, there has been a resurgence of interest in these devices for fabrication in SiC.

3.6.8 Optically Triggered Thyristors

Optically gated thyristors have traditionally been used in power utility applications where series stacks of devices are necessary to achieve the high voltages required. Isolation between gate-drive circuits for circuits such as static VAR compensators and high-voltage dc-ac inverters (for use in high-voltage dc (HVDC) transmission) has driven the development of this class of devices, which are typically available in ratings from 5 to 8 kV. The cross section is similar to that shown in Fig. 3.31, showing the photosensitive region and the amplifying gate structures. Light-triggered thyristors (LTTs) may also integrate overvoltage protection.

One of the most recent devices can block 6 kV forward and reverse, conduct 2.5 kA average current, and maintain a di/dt capability of 300 A/μs and a dv/dt capability of 3000 V/μs, with a required trigger power of 10 mW. An integrated light-triggered and light-quenched SITh has been produced that

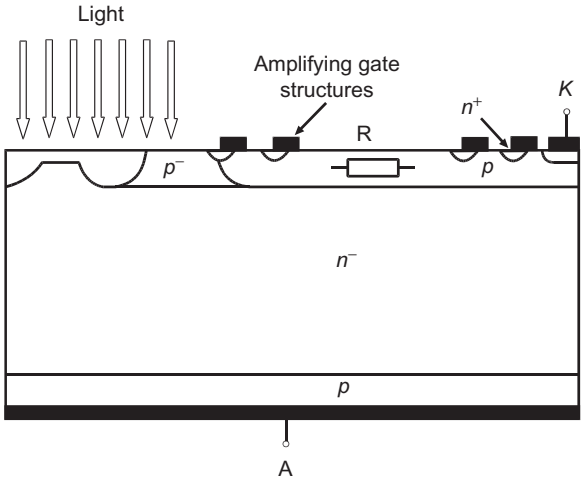


FIG. 3.31 Cross section of a light-triggered thyristors (LTT).

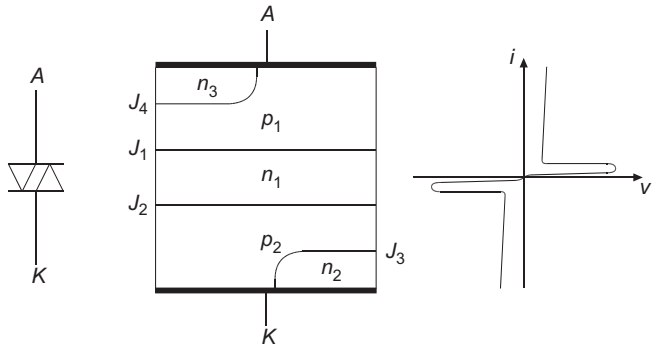


FIG. 3.33 Cross section and *i-v* plot of a diac.

can block 1.2 kV and conduct up to 20 A (at a forward drop of 2.5 V). This device is an integration of a normally off buried-gate static induction photo-thyristor and a normally off *p*-channel darlington surface-gate static induction phototransistor. The optical trigger and quenching power required is less than 5 and 0.2 mW, respectively.

3.6.9 Bi-directional Controlled Thyristors

The BCT is an integrated assembly of two antiparallel thyristors on one Si wafer. The intended applications for this switch are VAR compensators, static switches, soft starters, and motor drives. These devices are rated up to 6.5 kV blocking. Cross talk between the two halves has been minimized. A cross section of the BCT is shown in Fig. 3.32. Note that each surface has a cathode and an anode (opposite devices). The small gate-cathode periphery necessarily restricts the BCT to low-frequency applications because of its *di/dt* limit.

Low-power devices similar to the BCT, but in existence for many years, are the diac and triac. A simplified cross section of a diac is shown in Fig. 3.33. A positive voltage applied to the anode with respect to the cathode forward biases J_1, while reverse biasing J_2. J_4 and J_3 are shorted by the metal contacts. When J_2 is biased to breakdown, a lateral current flows in the p_2 region. This lateral flow forward biases the edge of J_3, causing carrier injection. The result is that the device switches into its thyristor mode and latches. Applying a reverse voltage causes the opposite behavior at each junction, but with the same result. Fig. 3.33 also shows the *i-v* plot for a diac.

The addition of a gate connection, to form a triac, allows the breakover to be controlled at a lower forward voltage. Fig. 3.34 shows the structure for the triac. Unlike the diac, this is not symmetrical, resulting in differing forward and reverse breakover voltages for a given gate voltage. The device is fired by applying a gate pulse of the same polarity relative to MT1 as that of MT2.

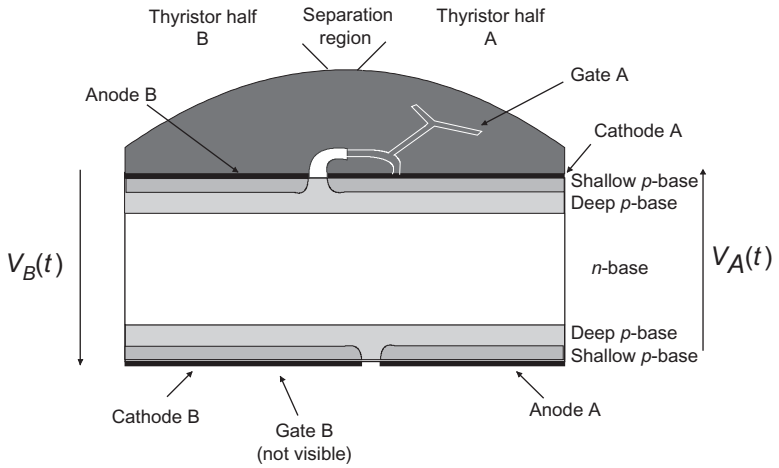


FIG. 3.32 Cross section of a bidirectional control thyristor (BCT).

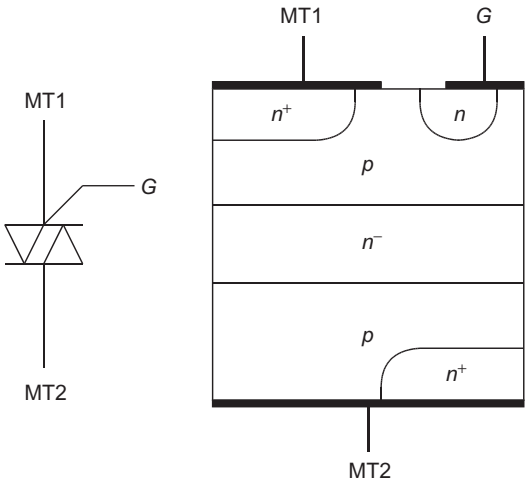


FIG. 3.34 Cross section of a triac.

3.7 Gate Drive Requirements

3.7.1 Snubber Circuits

To protect a thyristor, from a large *di/dt* during turn-on and a large *dv/dt* during turnoff, a snubber circuit is needed. A general snubber topology is shown in Fig. 3.35. The turn-on snubber is made by inductance L_1 (often, L_1 is stray inductance only). This protects the thyristor from a large *di/dt* during the turn-on process. The auxiliary circuit made by R_1 and D_1 allows the discharging of L_1 when the thyristor is turned off. The turn-off snubber is made by resistor R_2 and capacitance C_2. This circuit protects a GTO from large *dv/dt* during the turn-off process. The auxiliary circuit made by D_2 and R_2 allows the discharging of C_2 when the thyristor is turned on. The circuit of capacitance C_2 and inductance L_1 also limits the value of *dv/dt* across the thyristor during forward-blocking. In addition, L_1 protects the thyristor from reverse overcurrents. R_1 and diodes D_1, D_2, are usually omitted in ac circuits with converter-grade thyristors. A similar second set of *L*, *C*, and *R* may be used around this circuit in HVDC applications.

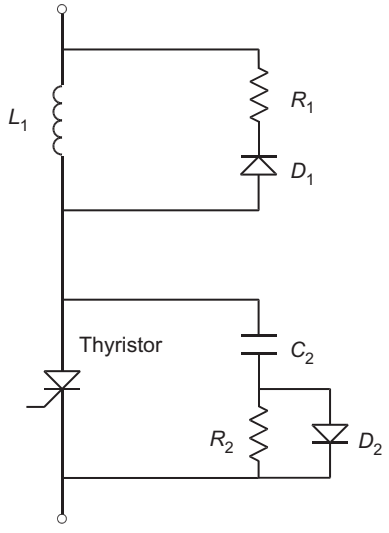


FIG. 3.35 Turn-on (top elements) and turn-off (bottom elements) snubber circuits for thyristors.

3.7.2 Gate Circuits

It is possible to turn on a thyristor by injecting a current pulse into its gate. This process is known as gating, triggering, or firing the thyristor. The most important restrictions are on the maximum peak and duration of the gate pulse current. In order to allow a fast turn-on and a correspondingly large anode *di/dt* during the turn-on process, a large gate current pulse is supplied during the initial turn-on phase with a large di_G/dt. The gate current is kept on, at lower value, for some times after the thyristor turned on in order to avoid unwanted turn-off of the device; this is known as the "back-porch" current. A shaped gate current waveform of this type is shown in Fig. 3.36.

Fig. 3.37 shows typical gate *i-v* characteristics for the maximum and minimum operating temperatures. The dashed line represents the minimum gate current and corresponding gate voltage needed to ensure that the thyristor will be triggered at various operating temperatures. It is also known as the locus of minimum firing points. On the data sheet, it is possible find a line representing the maximum operating power of the thyristor gating internal circuit. The straight line, between V_{GG} and V_{GG}/R_G, represents the current voltage characteristic of the equivalent trigger circuit. If the equivalent trigger circuit line intercepts the two gate *i-v* characteristics for the maximum and minimum operating temperatures between where they intercept the dashed lines (minimum gate current to trigger and maximum gate power dissipation), then the trigger circuit is able to turn-on the thyristor at any operating temperature without destroying or damaging the device.

In order to keep the power circuit and the control circuit electrically unconnected, the gate signal generator and the gate of the thyristor are often connected through a transformer.

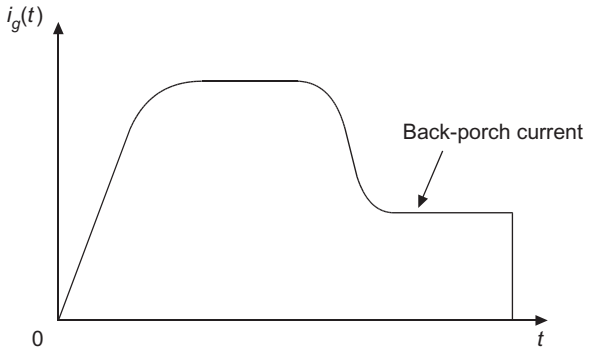


FIG. 3.36 Gate current waveform showing large initial current followed by a suitable back-porch value.

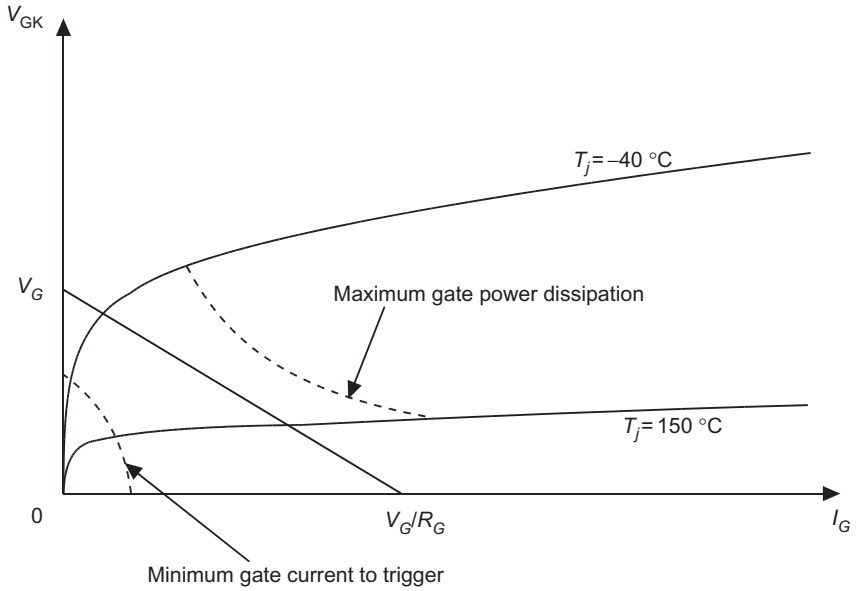


FIG. 3.37 Gate *i-v* curve for a typical thyristor.

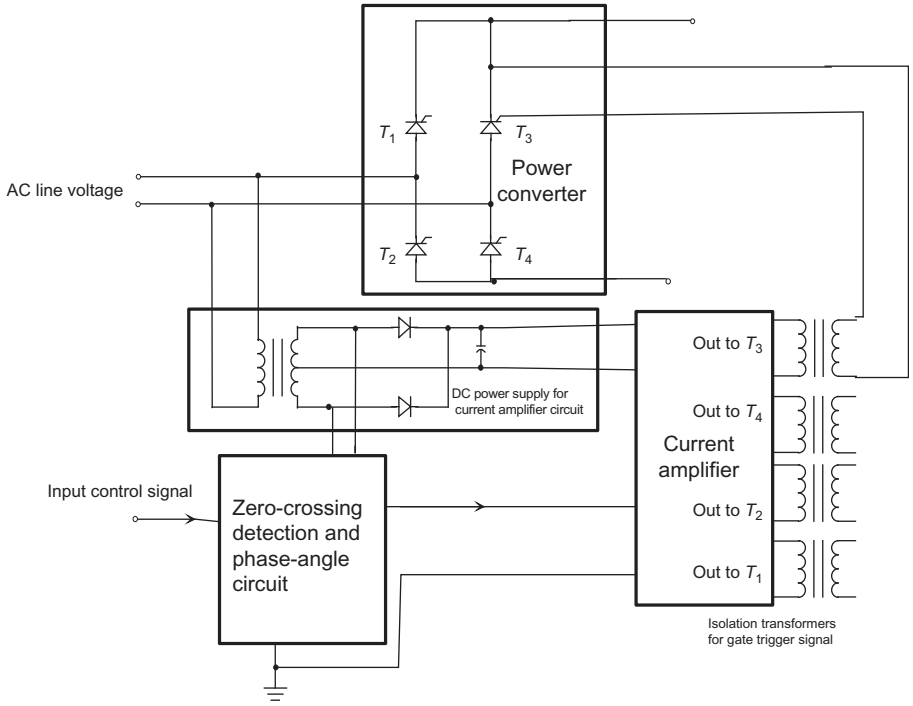


FIG. 3.38 Block diagram of a transformer-isolated gate-drive circuit.

There is a transformer winding for each thyristor, and in this way, unwanted short circuits between devices are avoided. A general block diagram of a thyristor gate trigger circuit is shown in Fig. 3.38. This application is for a standard bridge configuration often used in power converters.

Another problem can arise if the load impedance is high, particularly if the load is inductive and the supply voltage is low. In this situation, the latching current may not be reached during the trigger pulse. A possible solution to this problem could be the use of a longer current pulse. However, such a solution is not attractive because of the presence of the isolation transformer. An alternative solution is the generation of a series of short pulses that last for the same duration as a single long pulse. A single short pulse, a single long pulse, and a series of

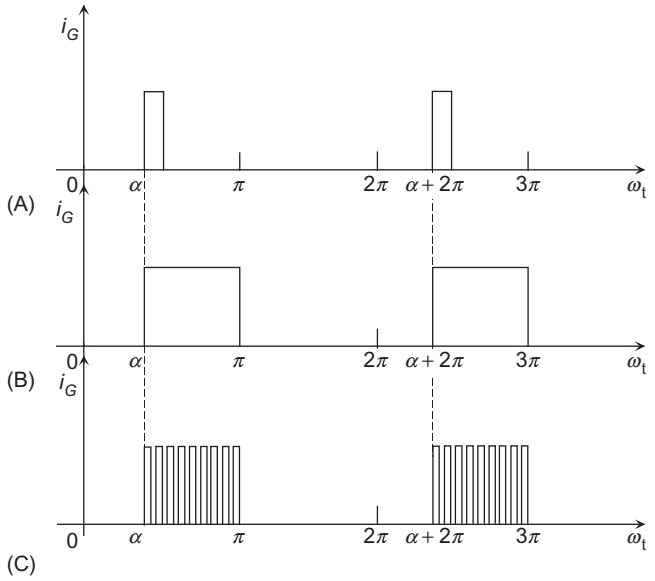


FIG. 3.39 Multiple gate pulses used as an alternative to one long current pulse.

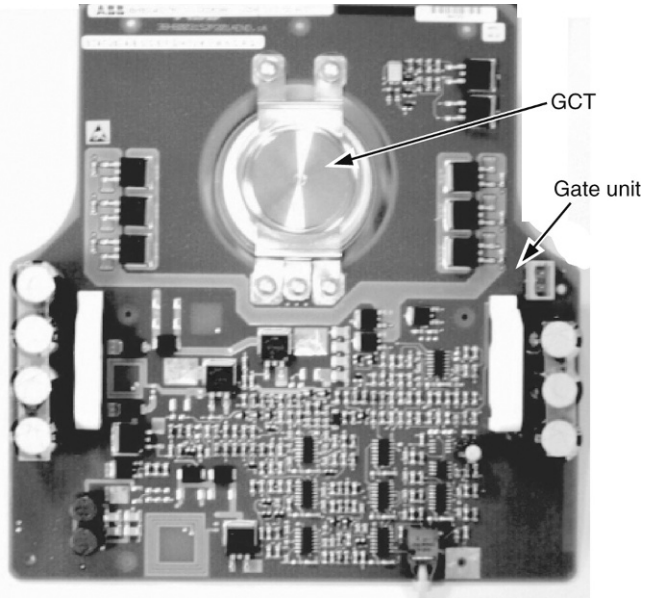


FIG. 3.40 Typical layout of an IGCT gate drive.

short pulses are shown in Fig. 3.39. Reliable gating of the thyristor is essential in many applications.

There are many gate trigger circuits that use optical isolation between the logic-level electronics and a drive stage (typically MOSFETs) configured in a push-pull output. The dc power supply voltage for the drive stage is provided through transformer isolation. Many device manufacturers supply drive circuits available on printed circuit (PC) boards or diagrams of suggested circuits.

IGCT gate drives consist of an integrated module to which the thyristor is connected via a low-inductance mounting; an example is given in Fig. 3.40. Multiple MOSFETs and capacitors connected in parallel may be used to source or sink the necessary currents to turn the device on or off. Logic in the module controls the gate drive from a fiber-optic trigger input and provides diagnostic feedback from a fiber-optic output. A simple power supply connection is also required.

Values for each cell of a multicell GTO model

Model component	Symbol	Value
Delay resistor	R	1 μΩ
Delay capacitor	C	1 nF
Mutual coupling inductance	M	10 nH
Gate contact resistance	R_{GC}	1 mΩ
Cathode contact resistance	R_{KC}	1 mΩ

Other GTO thyristor models have been developed that offer improved accuracy at the expense of increased complexity. The model by Tseng et al. [30] includes charge storage effects in the n^--base, and its application to a multicell model, as in Fig. 3.14, has been demonstrated successfully. Models for the IGCT, based on the lumped-charge approach [31] and the Fourier-based solution of the ambipolar diffusion equation (ADE) [32], have also been developed.

3.8 Applications

The most important application of thyristors is for line-frequency phase-controlled rectifiers. This family includes several topologies, of which one of the most important is used to construct HVDC transmission systems. A single-phase controlled rectifier is shown in Fig. 3.41.

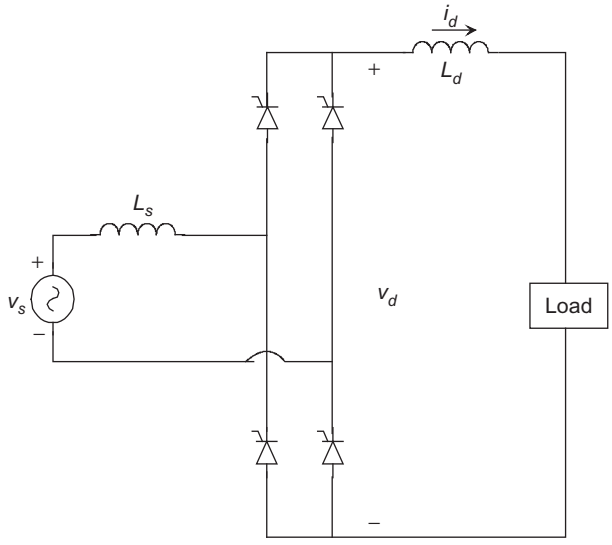


FIG. 3.41 Single-phase controlled rectifier circuit.

The use of thyristors instead of diodes allows the average output voltage to be controlled by appropriate gating of the thyristors. If the gate signals to the thyristors were continuously applied, the thyristors in Fig. 3.41 would behave as diodes. If no gate currents are supplied, they behave as open circuits. Gate current can be applied any time (phase delay) after the forward voltage becomes positive. Using this phase-control feature, it is possible to produce an average dc output voltage less than the average output voltage obtained from an uncontrolled diode rectifier.

3.8.1 DC–AC Utility Inverters

Three-phase converters can be made in different ways, according to the system in which they are employed. The basic circuit used to construct these topologies—the three-phase controlled rectifier—is shown in Fig. 3.42.

Starting from this basic configuration, it is possible to construct more complex circuits in order to obtain high-voltage or high-current outputs or just to reduce the output ripple by constructing a multiphase converter. One of the most important systems using the topology shown in Fig. 3.42 as a basic circuit is the HVDC system represented in Fig. 3.43. This system is made by two converters, a transmission line, and two ac systems. Each converter terminal is made of two poles. Each pole is made by two six-pulse line-frequency converters connected through Δ–Y and Y–Y transformers in order to obtain a 12-pulse converter and a reduced output ripple. The filters are required to reduce the current harmonics generated by the converter.

When a large amount of current and relatively low voltage is required, it is possible to connect in parallel, using a specially designed inductor, two six-pulse line-frequency converters connected through Δ–Y and Y–Y transformers. The special inductor is designed to absorb the voltage between the two converters and to provide a pole to the load. This topology is shown in Fig. 3.44. This configuration is often known as a 12-pulse converter. Higher pulse numbers may also be found.

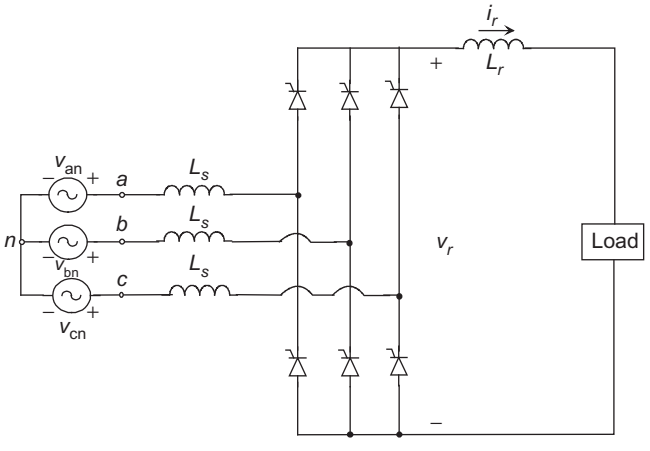


FIG. 3.42 A three-phase controlled bridge circuit used as a basic topology for many converter systems.

3.8.2 Motor Control

Another important application of thyristors is in motor control circuits. Historically, thyristors have been used heavily in traction, although most new designs are now based on IGBTs. Such motor control circuits broadly fall into four types: (i) chopper control of a dc motor from a dc supply, (ii) single- or three-phase converter control of a dc motor from an ac supply, (iii) inverter control of an ac synchronous or induction machine from a dc supply, and (iv) cycloconverter control of an ac machine from an ac supply. An example of a GTO chopper is given in Fig. 3.45. $L_1, R_1, D_1,$ and C_1 are the turn-on snubber; $R_2, D_2,$ and C_2 are the turn-off snubber; finally, R_3 and D_3 form the snubber for the freewheel diode D_3. A thyristor cycloconverter is shown in Fig. 3.46; the waveforms show the fundamental component of the output voltage for one phase. Three double converters are used to produce a three-phase variable-frequency, variable voltage sinusoidal output for driving ac motors. However, the limited frequency range (less than a third of the line frequency) restricts the application to large, low-speed machines at high powers.

A single- or three-phase thyristor converter (controlled rectifier) may be used to provide a variable dc supply for controlling a dc motor. Such a converter may also be used as the front end of a three-phase induction motor drive. The variable voltage, variable-frequency motor drive requires a dc supply, which is supplied by the thyristor converter. The drive may use a square wave or PWM voltage source inverter (VSI) or a current source inverter (CSI). Fig. 3.47 shows a square wave or PWM VSI with a controlled rectifier on the input side. The switch block inverter may be made of thyristors (usually GTOs or IGCTs) for high power, although most new designs now use IGBTs. Low-power motor controllers generally use IGBT inverters.

In motor control, thyristors are also used in CSI topologies. When the motor is controlled by a CSI, a controlled rectifier is also needed on the input side. Fig. 3.48 shows a typical CSI inverter. The capacitors are needed to force the current in the thyristors to zero at each switching event. This is not needed when using GTOs. This inverter topology does not need any additional circuitry to provide the regenerative braking (energy recovery when slowing the motor). Historically, two back-to-back connected line-frequency thyristor converters have been employed to allow bidirectional power flow and thus regenerative braking. Use of antiparallel GTOs with symmetrical blocking capability, or the use of diodes in series with each asymmetrical GTO, reduces the number of power devices needed, but greatly increases the control complexity.

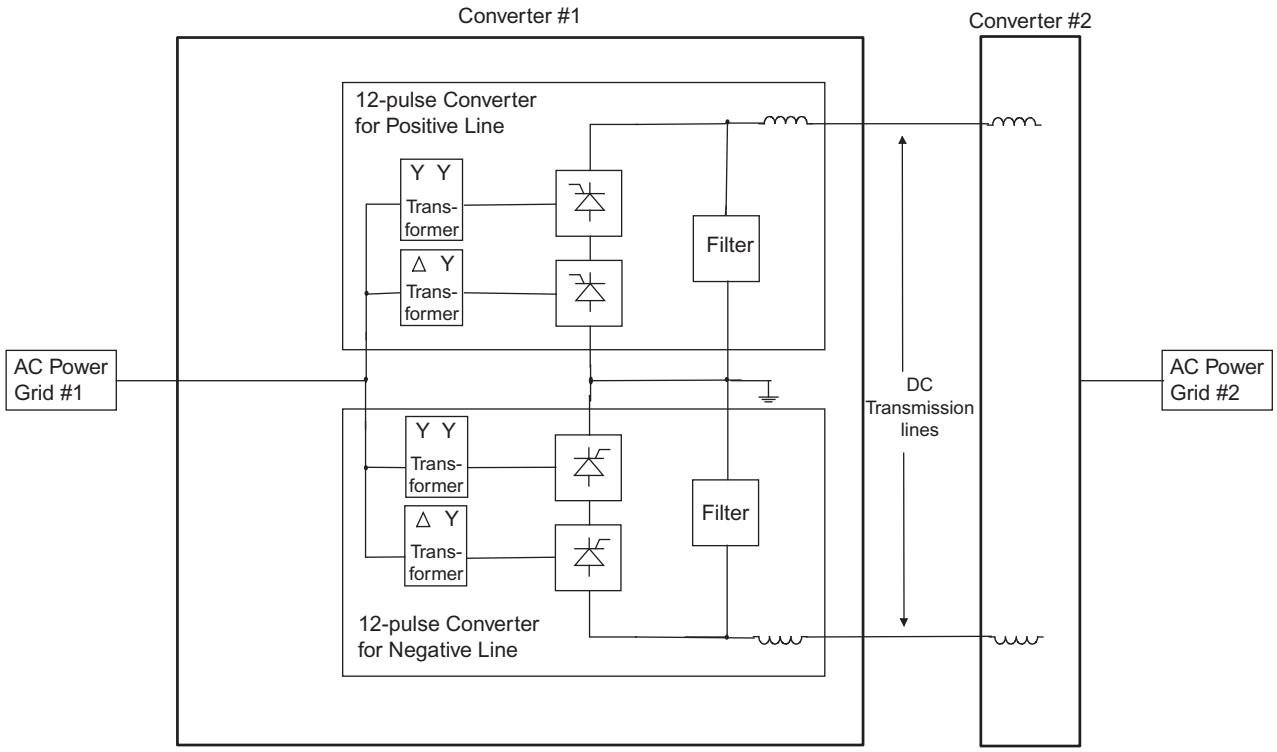


FIG. 3.43 A HVDC transmission system.

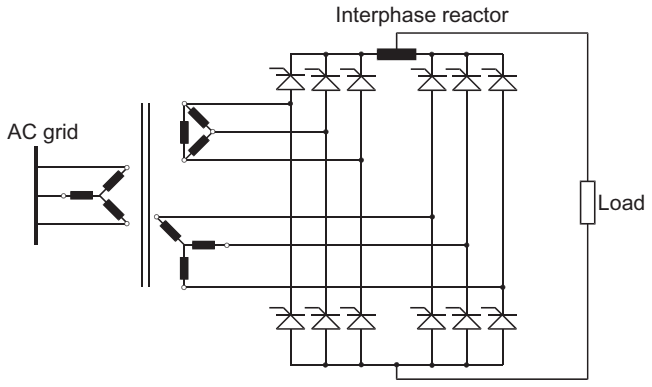


FIG. 3.44 Parallel connection of two six-pulse converters for high current applications.

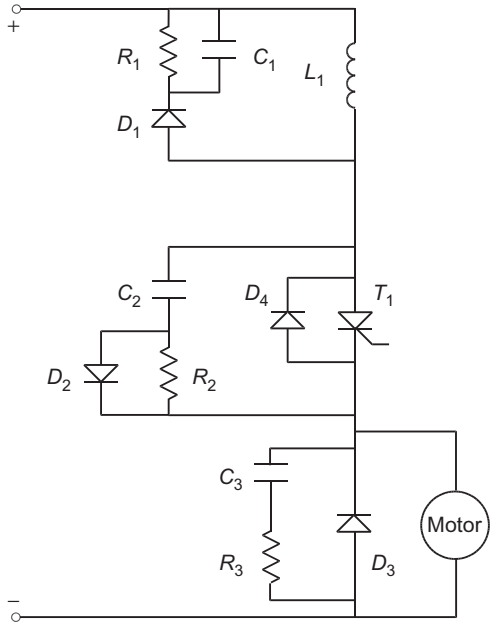


FIG. 3.45 GTO chopper for dc motor control.

3.8.3 VAR Compensators and Static Switching Systems

Thyristors are also used to switch capacitors or inductors in order to control the reactive power in the system. Such arrangements may also be used in phase-balancing circuits for balancing the load fed from a three-phase supply. Examples of these circuits are shown in Fig. 3.49. These circuits act as static VAR controllers. The topology represented on the left of Fig. 3.49 is called a thyristor-controlled inductor (TCI), and it acts as a variable inductor where the inductive VAR supplied can be varied quickly. Because the system may require either inductive or capacitive VAR compensation, it is possible to connect a bank of capacitors in parallel with a TCI. The topology shown on the

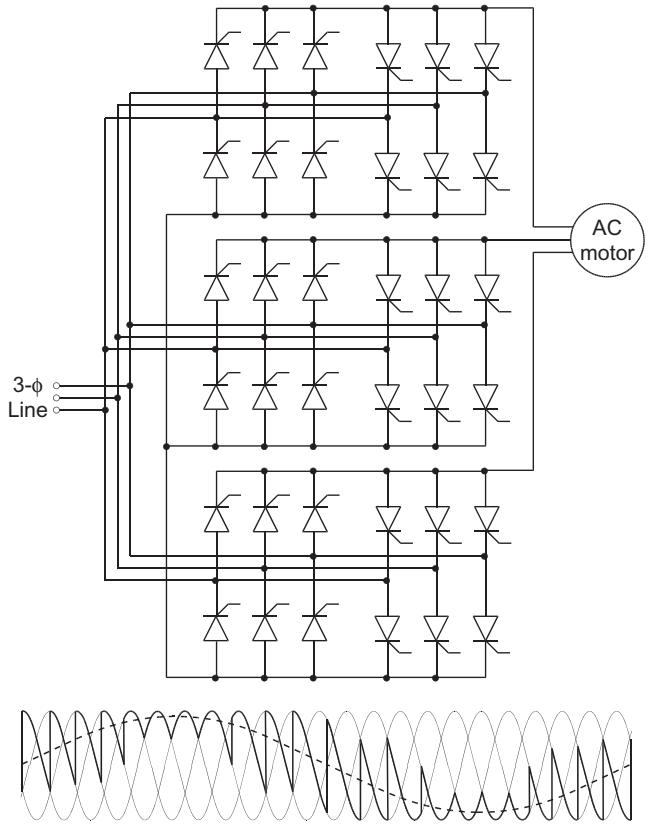


FIG. 3.46 Cycloconverter for control of large ac machines.

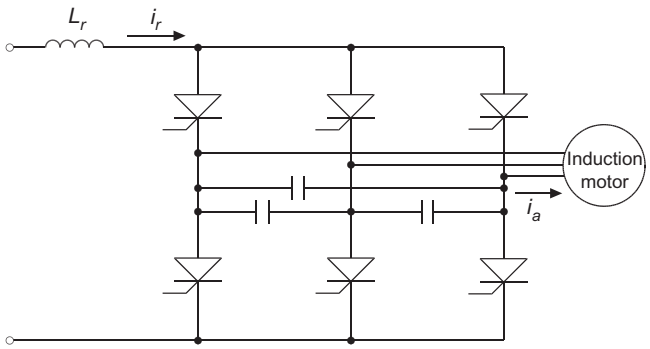


FIG. 3.48 CSI on the output section of a motor drive system using capacitors for power factor correction.

right of Fig. 3.49 is called a thyristor-switched capacitor (TSC). Capacitors can be switched out by blocking the gate pulse of all thyristors in the circuit. The problem of this topology is the voltage across the capacitors at the thyristor turnoff. At turn-on the thyristor must be gated at the instant of the maximum ac voltage to avoid large overcurrents. Many recent SVCs have used GTOs.

A similar application of thyristors is in solid-state fault current limiters and circuit breakers. In normal operation, the thyristors are continuously gated. However, under fault conditions, they are switched rapidly to increase the series impedance in the load and to limit the fault current. Key advantages are the flexibility of the current limiting, which is independent of the location of the fault and the change in load impedance, the reduction in fault level of the supply, and a smaller voltage sag during a short-circuit fault.

A less important application of thyristors is as a static transfer switch, used to improve the reliability of uninterruptible power supplies (UPS) as shown in Fig. 3.50. There are two modes of using the thyristors. The first leaves the load permanently connected to the UPS system and in case of emergency disconnects the load from the UPS and connects it directly to the power line. The second mode is opposite to the first one. Under normal conditions, the load is permanently connected to the power line, and in event of a line outage, the load is disconnected from the power line and connected to the UPS system.

3.8.4 Lighting Control Circuits

An important circuit used in lighting control is the dimmer, based on a triac and shown in Fig. 3.51. The *R-C* network applies a phase shift to the gate voltage, delaying the triggering of the triac. Varying the resistance controls the firing angle of the triac and therefore the voltage across the load. The diac is used to provide symmetrical triggering for the positive and negative half cycles, due to the nonsymmetrical nature of the triac. This ensures symmetrical waveforms and elimination of even harmonics. An *L-C* filter is often used to reduce any remaining harmonics.

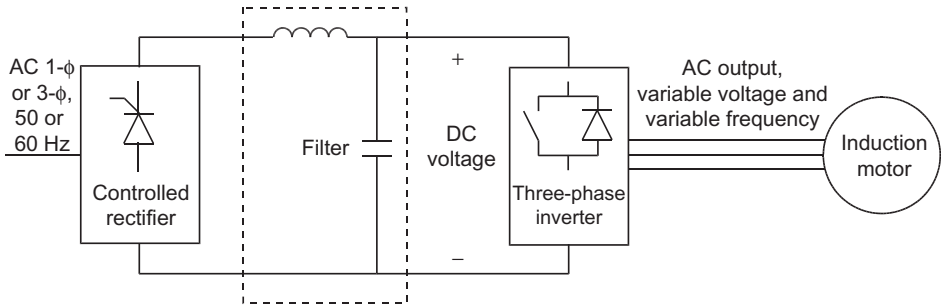


FIG. 3.47 PWM or square wave inverter with a controlled rectifier input.

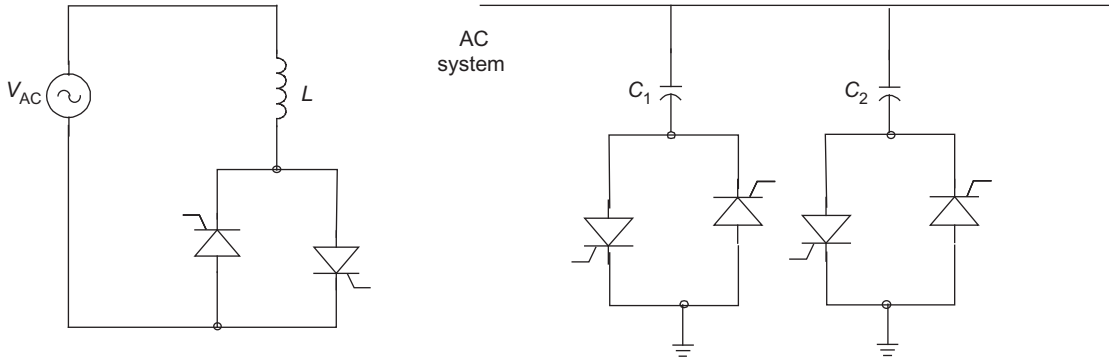


FIG. 3.49 Per phase TCI and TSC system.

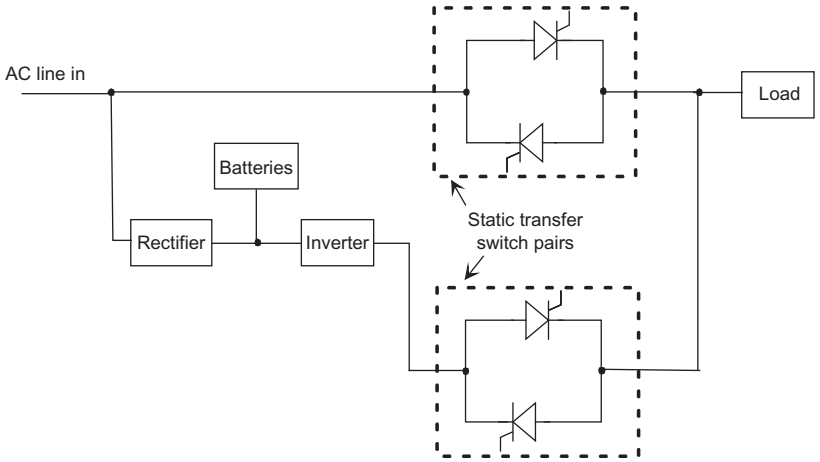


FIG. 3.50 Static transfer switch used in an UPS system.

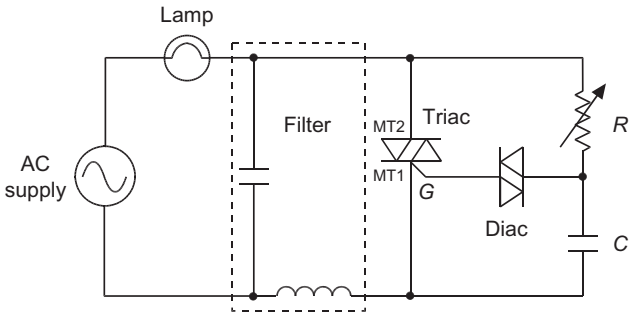


FIG. 3.51 Basic dimmer circuit used in lighting control.

References

[1] S.K. Ghandi, Semiconductor Power Devices—Physics of Operation and Fabrication Technology, John Wiley and Sons, New York, 1977. pp. 63–84.

[2] B.J. Baliga, Power Semiconductor Devices, PWS Publishing, Boston, MA, 1996. pp. 91–110.

[3] B. Beker, J.L. Hudgins, J. Coronati, B. Gillett, S. Shekhawat, Parasitic parameter extraction of PEBB module using VTB technology, IEEE IAS Ann. Mtg. Rec. (1997) 467–471.

[4] C.V. Godbold, V.A. Sankaran, J.L. Hudgins, Thermal analysis of high power modules, IEEE Trans. PEL 12 (1) (1997) 3–11.

[5] J.L. Hudgins, W.M. Portnoy, High *di/dt* pulse switching of thyristors, IEEE Tran. PEL 2 (1987) 143–148.

[6] S.M. Sze, Physics of Semiconductor Devices, second ed., John Wiley and Sons, New York, 1984. pp. 140–147.

[7] V.A. Sankaran, J.L. Hudgins, W.M. Portnoy, Role of the amplifying gate in the turn-on process of involute structure thyristors, IEEE Tran. PEL 5 (2) (1990) 125–132.

[8] S. Menhart, J.L. Hudgins, W.M. Portnoy, The low temperature behavior of thyristors, IEEE Tran. ED 39 (1992) 1011–1013.

[9] A. Herlet, The forward characteristic of silicon power rectifiers at high current densities, Solid-State Electron. 11 (8) (1968) 717–742.

[10] J.L. Hudgins, C.V. Godbold, W.M. Portnoy, O.M. Mueller, Temperature effects on GTO characteristics, IEEE IAS Annual Mtg. Rec. (1994) 1182–1186.

[11] J.L. Hudgins, A review of modern power semiconductor electronic devices, Microelectronics Journal 24 (1993) 41–54.

[12] Dynex semiconductor: Data GTO data-sheets web-site. Available form: http://www.dynexsemi.com/product-area/gto-thyristors.

[13] Data sheet: Anode Shorthed Gate Turn-Off Thyristor Type G1000NC450. Available form: http://www.westcode.com/g1000nc.pdf, Accessed 23 February 2017.

[14] I.M.A. El-Amin, GTO PSPICE model and its applications, in: The Fourth Saudi Engineering Conference, vol. III, November 1995, 1995, pp. 271–277.
[15] P.R. Palmer, B.H. Stark, A PSPICE model of the DG-EST based on the ambipolar diffusion equation, IEEE PESC Rec. (1999) 358–363.
[16] T.M. Jahns, R.W.A.A. De Doncker, J.W.A. Wilson, V.A. K. Temple, D.L. Waltrus, Circuit utilization characteristics of MOS-controlled thyristors, IEEE Trans. Ind. Appl. 27 (3) (1991) 589–597.
[17] Harris Semiconductor, MCT/IGBTs/Diodes Databook, 1995.
[18] P. Holdman, F. Lotuka, SMPS IGBTs—high switching frequencies allow efficient.
[19] D. Quek, Design of Protection and Control Strategies for Low-loss MCT Power Converters, North Dakota State University, 1994. PhD Thesis.
[20] D. Quek, S. Yuvarajan, A novel gate drive for the MCT incorporating overcurrent protection, in: Proceedings of IEEE IAS Annual Meeting, 1994, pp. 1297–1302.
[21] S. Yuvarajan, R. Nelson, D. Quek, A study of the effects of snubber on switching loss and EMI in an MCT converter, in: Proceedings of IEEE IAS Annual Meeting, 1994, pp. 1344–1349.
[22] T.C. Lee, M.E. Elbuluk, D.S. Zinger, Characterization and snubbing of a bidirectional MCT switch in a resonant ac link converter, IEEE Trans. Ind. Electron. 31 (5) (1995) 978–985.
[23] S. Yuvarajan, D. Quek, A PSPICE model for the MOS controlled thyristor, IEEE Trans. Ind. Electron. 42 (5) (1995) 554–558.
[24] G.L. Arsov, L.P. Panovski, An improved PSPICE model for the MOS-Controlled Thyristor, IEEE Trans. Ind. Electron. 46 (2) (1999) 473–477.
[25] P.D. Kendle, V.A.K. Temple, S.D. Arthur, Switching comparison of Generation-1 and Generation-2 P-MCTs and ultrafast N-IGBTs, in: Proceedings of IEEE IAS Annual Meeting, 1993, pp. 1286–1292.
[26] E. Yang, V. Temple, S. Arthur, Switching loss of Gen-1 and Gen-2 P-MCTs in soft-switching circuits, in: Proceedings of IEEE APEC, 1995, pp. 746–754.
[27] Q. Huang, G.A.J. Amaratunga, E.M. Sankara Narayanan, W. I. Milne, Analysis of -channel MOS-controlled thyristors, IEEE Trans. Electron Devices 38 (7) (1991) 1612–1618.
[28] B. Jayant Baliga, Power Semiconductor Devices, PWS Publishing, Boston, MA, 1996.
[29] R. Rodrigues, A. Huang, R. De Doncker, MTO thyristor power switches, in: Proceedings of PCIM'97 Power Electronics Conference, 1997, pp. 4-1–4-12.
[30] K.J. Tseng, P.R. Palmer, Mathematical model of gate-turn-off thyristor for use in circuit simulations, IEE Proc. Electr. Power Appl. 141 (6) (1994) 284–292.
[31] X. Wang, A. Caiafa, J. Hudgins, E. Santi, Temperature effects on IGCT performance. IEEE IAS Annual Mtg. Rec. (2003).
[32] X. Wang, A. Caiafa, J.L. Hudgins, E. Santi, P.R. Palmer. Implementation and validation of a physics-based circuit model for IGCT with full temperature dependencies. IEEE PESC Rec. (2004) 597–603.

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4

Static Induction Devices

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4.1 Introduction

Static induction devices were invented in 1975 by Nishizawa [1], and for many years, Japan was the only country where static induction family devices were successfully fabricated. Static induction transistor (SIT) can be considered as a short channel junction field effect transistor (JFET) device operating in prepunch-through region. The number of devices in this family is growing with time. The SIT can operate with the power over 100 kW at 100 kHz and above 150 W at 3 GHz [2]. These devices may operate up to THz frequencies [3,4]. Static induction transistor logic (SITL) had 100 times smaller switching energy than its I^2L competitor [5,6]. Static induction thyristor has many advantages over the traditional silicon-controlled rectifier (SCR), and static induction diod (SID) exhibits high switching speed, large reverse voltage, and low forward voltage drops [7].

4.2 Theory of Static Induction Devices

The cross section of the SIT is shown in Fig. 4.1, while its characteristics are shown in Fig. 4.2. An induced electrostatically potential barrier controls the current in static induction devices. The derivations of formulas will be done for an n-channel device, but the obtained results, with a little modification, can also be applied to p-channel devices. For a small electric field existing in the vicinity of the potential barrier, the drift and diffusion current can be approximated by

$$J_n = -qn(x)\mu_n \frac{d\varphi(x)}{dx} + qD_n \frac{dn(x)}{dx} \tag{4.1}$$

where $D_n = \mu_n V_T$ and $V_T = kT/q$. By multiplying both sides of the equation by $\exp(-\varphi(x)/V_T)$ and rearranging

$$J_n \exp\left(-\frac{\varphi(x)}{V_T}\right) = qD_n \frac{d}{dx}\left[n(x)\exp\left(-\frac{\varphi(x)}{V_T}\right)\right] \tag{4.2}$$

Integrating from x_1 to x_2, one can obtain

$$J_n = qD_n \frac{n(x_2)\exp(-\varphi(x_2)/V_T) - n(x_1)\exp(-\varphi(x_1)/V_T)}{\int_{x_1}^{x_2} \exp(-\varphi(x)/V_T)dx} \tag{4.3}$$

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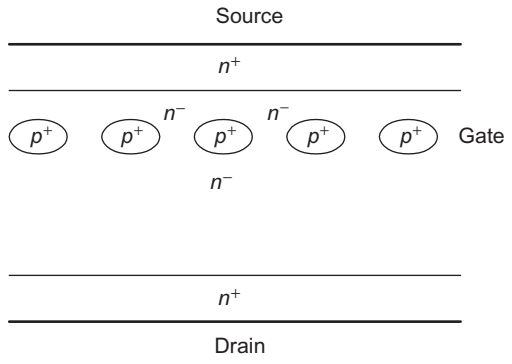


FIG. 4.1 Cross section of the static induction transistor.

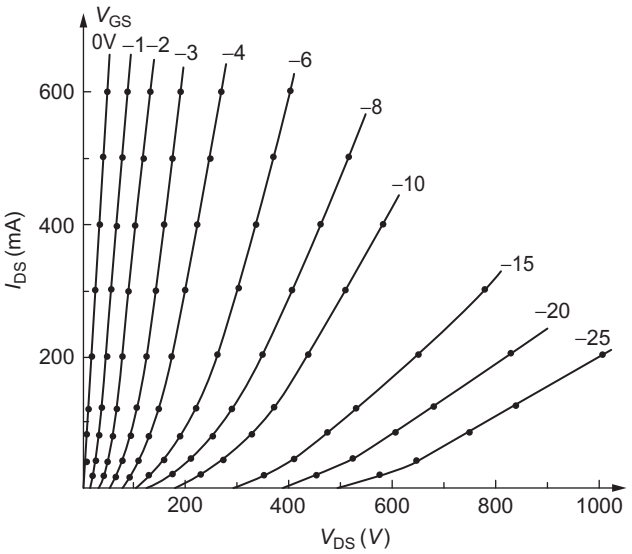


FIG. 4.2 Characteristics of the early SIT design [1].

With the following boundary conditions

$$\varphi(x_1)=0;\ \ n(x_1)=N_S$$
$$\varphi(x_2)=V_D;\ \ n(x_2)N_D \tag{4.4}$$

Eq. (4.3) reduces to

$$J_n=\frac{qD_nN_S}{\int_{x_1}^{x_2}\exp\left(-\varphi(x)/V_T\right)dx} \tag{4.5}$$

Note that the above equations derived for SIT can also be used to find current in any devices controlled by a potential barrier, such as a bipolar transistor, an MOS transistor operation in subthreshold mode, or a Schottky diode.

4.3 Characteristics of SIT

Samples of the potential distribution in the SI devices are shown in Fig. 4.3 [7]. The vicinity of the potential barrier can be approximated using parabolic formulas (Fig. 4.4) along and across the channel [8,9].

$$\varphi(x)=\Phi\left[1-\left(2\frac{x}{L}-1\right)^2\right] \tag{4.6}$$

$$\varphi(y)=\Phi\left[1-\left(2\frac{y}{W}-1\right)^2\right] \tag{4.7}$$

Integrating Eq. (4.5) first along the channel and then across the channel yields a very simple formula for drain currents in n-channel SITs:

$$I_D=qD_pN_SZ\frac{W}{L}\exp\left(\frac{\Phi}{V_T}\right) \tag{4.8}$$

where Φ is the potential barrier height in reference to the source potential, N_S is the electron concentration at the source, W/L ratio describes the shape of the potential saddle in vicinity of the barrier, and Z is the length of the source strip.

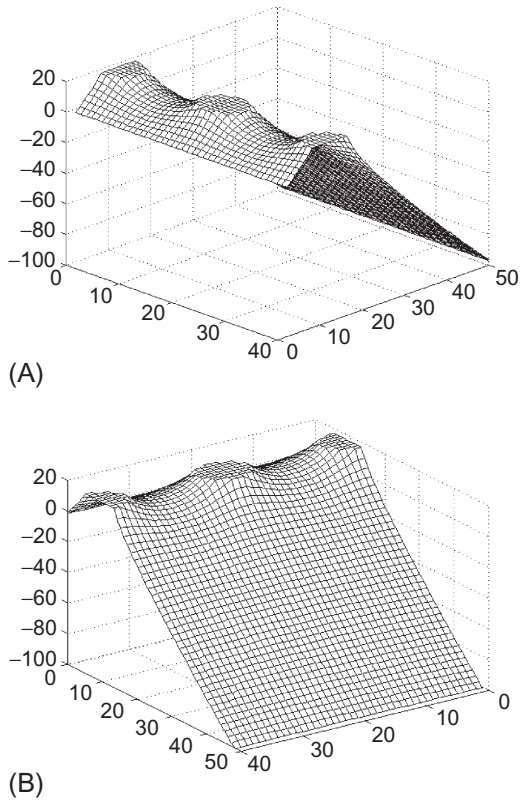


FIG. 4.3 Potential distribution in SIT: (A) view from the source side and (B) view from the drain side.

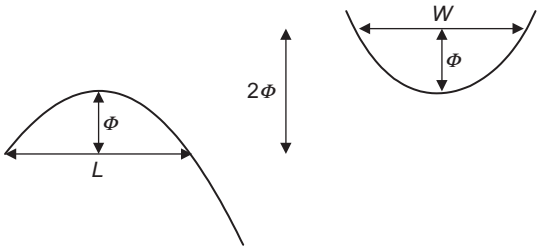


FIG. 4.4 Potential distribution in the vicinity of the barrier approximated by parabolic shapes.

Since barrier height Φ can be a linear function of gate and drain voltages, therefore,

$$I_D = qD_pN_SZ\frac{W}{L}\exp\left(a(V_{GS} + bV_{DS} + \Phi_0)/V_T\right) \tag{4.9}$$

The above equation describes characteristics of SIT for small current range. For large current levels, the device current is controlled by the space charge of moving carriers. In the one-dimensional case, the potential distribution is described by the Poisson equation:

$$\frac{d^2\varphi}{dx_2} = -\frac{\rho(x)}{\varepsilon_{Si}\varepsilon_0} = \frac{I_{DS}}{Av(x)} \tag{4.10}$$

where A is the effective device cross section and $v(x)$ is carrier velocity. For a small electric field, $v(x) = \mu E(x)$, and the solution of Eq. (4.10) is

$$I_{DS} = \frac{9}{8}V_{DS}^2\mu\varepsilon_{Si}\varepsilon_0\frac{A}{L^3} \tag{4.11}$$

and for a large electric field, $v(x) = \text{const}$, and Eq. (4.10) results in

$$I_{DS} = 2V_{DS}v_{sat}\varepsilon_{Si}\varepsilon_0\frac{A}{L^2} \tag{4.12}$$

where L is the channel length and $v_{sat} \asymp 10^{11}$ μm/s is the carrier saturation velocity. In practical devices, the current-voltage relationship is described by an exponential relationship, Eq. (4.9); for small currents, a quadratic relationship, Eq. (4.11); and finally for large voltages by an almost linear relationship, Eq. (4.12). SIT characteristics drawn in linear and logarithmic scales are shown in Figs. 4.5 and 4.6, respectively.

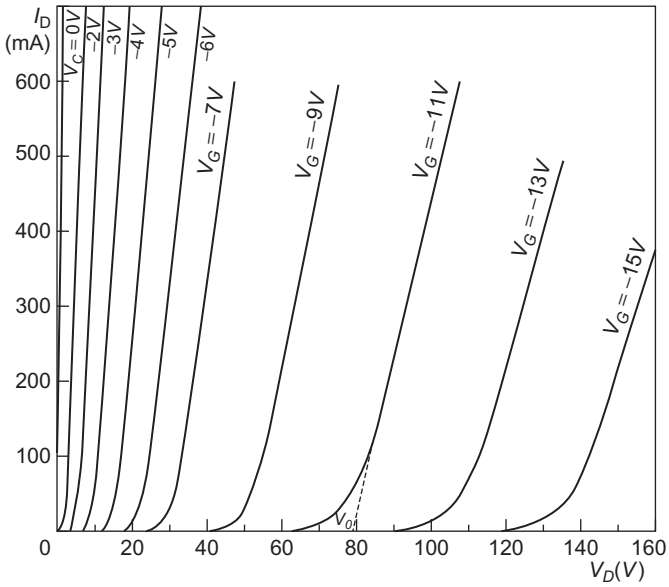


FIG. 4.5 Characteristics of the SIT drawn in a linear scale.

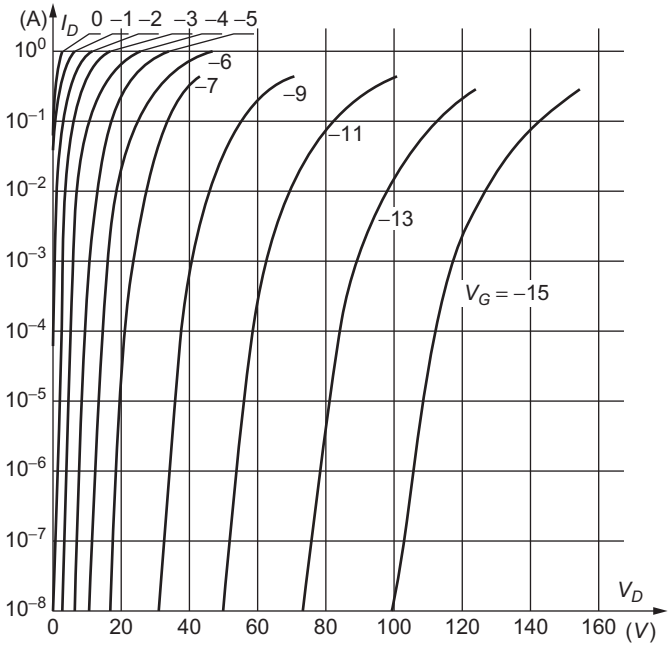


FIG. 4.6 Characteristics of the SIT drawn in a logarithmic scale.

4.4 Bipolar Mode Operation of SI devices (BSIT)

The bipolar mode of operation of SIT was first reported in 1976 by Nishizawa and Wilamowski [5,6]. Several complex theories for the bipolar mode of operation were developed [10–14], but actually, the simple formula given by Eq. (4.5) works well not only for the typical mode of the SIT operation but also for the bipolar mode of the SIT operation. Furthermore, the same formula works very well for the classical bipolar transistors. Typical characteristics of the SI transistor operating in normal and in bipolar modes are shown in Figs. 4.7 and 4.8.

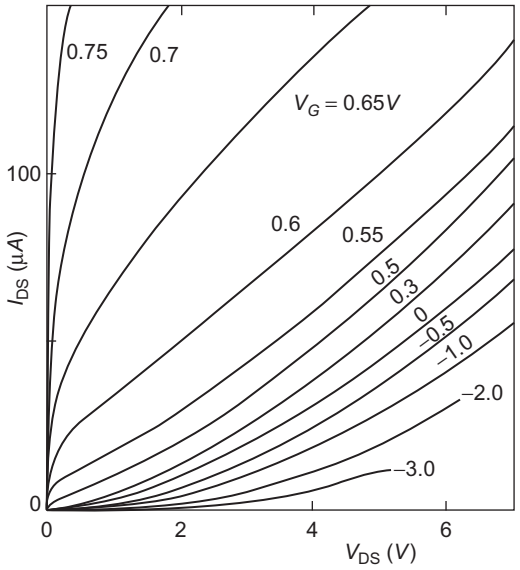


FIG. 4.7 Small-size SIT transistor characteristics, operating in both the normal and bipolar modes, $I_D = f(V_{DS})$ with V_{GS} as a parameter.

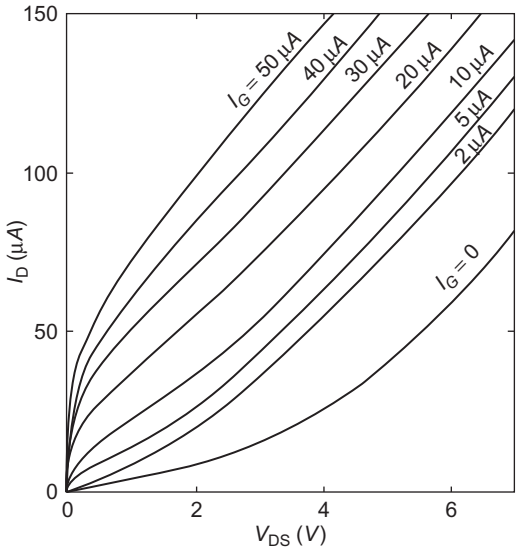


FIG. 4.8 Small-size SIT transistor characteristics, operating in both the normal and bipolar modes, $I_D = f(V_{DS})$ with I_G as a parameter.

A potential barrier controls the current in the SIT, and it is given by

$$J_n = \frac{qD_n N_S}{\int_{x_1}^{x_2} \exp\left(-\frac{\varphi(x)}{V_T}\right) dx} \tag{4.13}$$

where $\phi(x)$ is the profile of the potential barrier along the channel.

For example, in the case of *npn* bipolar transistors, the potential distribution across the base in reference to emitter potential at the reference impurity level $N_E = N_S$ is described by

$$\varphi(x) = V_T \ln\left(\frac{N_B(x)N_S}{n_i^2}\right) \exp\left(-\frac{V_{BE}}{V_T}\right) \tag{4.14}$$

After inserting Eq. (4.14) into Eq. (4.13), one can obtain the well-known equation for electron current injected into the base:

$$J_n = \frac{qD_n n_i^2}{\int_{x_1}^{x_2} N_B(x)dx} \exp\left(\frac{V_{BE}}{V_T}\right) \tag{4.15}$$

If Eq. (4.13) is valid for SIT and BJT, then one may assume that it is also valid for the bipolar mode of operation of the SIT transistor. This is a well-known equation for the collector current in the bipolar transistor, but this time, it was derived using the concept of the current flow through the potential barrier.

4.5 Emitters for Static Induction Devices

One of the disadvantages of the SIT is the relatively flat shape of the potential barrier (Fig. 4.9A). This leads to slow, diffusion-based transport of carriers in the vicinity of the potential barrier. The carrier transit time can be estimated using the formula

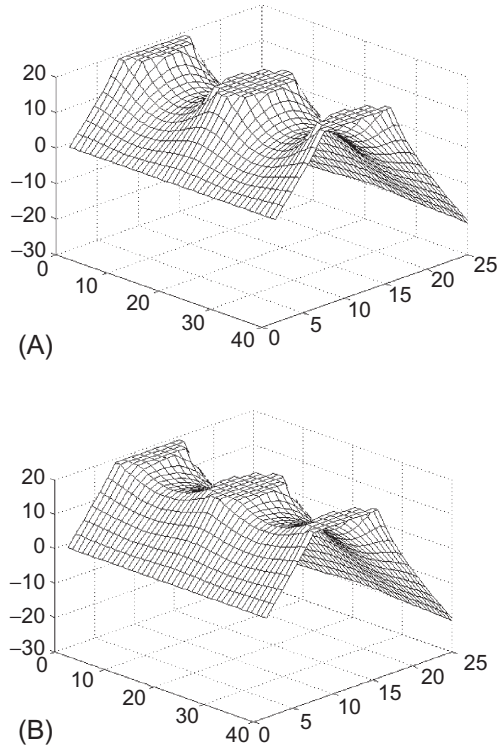


FIG. 4.9 Potential distributions in SIT: (A) traditional and (B) with sharp potential barrier.

$$t_{\text{transit}} = \frac{l_{\text{eff}}^2}{D} \tag{4.16}$$

where l_{eff} is the effective length of the channel and $D = \mu V_T$ is the diffusion constant. In the case of a traditional SIT transistor, this channel length is about 2 μm, while in the case of SIT transistors with sharper barriers (Fig. 4.9B), the channel length is reduced to about 0.2 μm. The corresponding transient times are 2 ns and 20 ps, respectively.

Potential distributions shown in Fig. 4.3 are valid for SIT with an emitter made of a traditional *p-n* junction. A much narrower potential barrier can be obtained when the other type of emitter is being used. There are two well-known emitters, (1) *p-n* junction (Fig. 4.10A) and (2) Schottky junction (Fig. 4.10B). For silicon devices, *p-n* junctions have a forward voltage drop of 0.7–0.8 V, while Schottky emitters have 0.2–0.3 V only. Since the Schottky diode is a majority carrier device, the carrier storage effect is negligible.

Another interesting emitter structure is shown in Fig. 4.10C. This emitter has all the advantages of the Schottky diode, with majority carrier injection, even though it is fabricated out of *p-n* junctions.

The concept of static induction devices can be used independently of the type of emitter shown in Fig. 4.10. With Schottky-type and punch-through-type emitters, the potential barrier is much narrower, and this results in faster response time and larger current gain in the bipolar mode of operation.

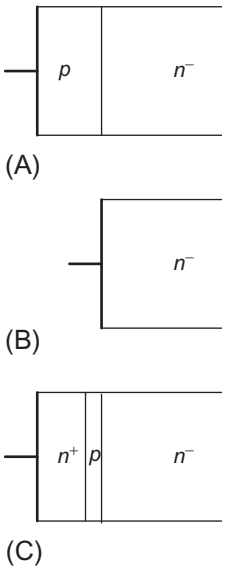


FIG. 4.10 Various structures of emitters: (A) *p-n* junction including heterostructure with SiGe materials, (B) Schottky junction, and (C) punch-through emitter (in normal operation condition, the *p* region is depleted from carriers).

4.6 Static Induction Diode

The bipolar mode of operation of SIT can also be used to obtain diodes with low forward voltage drop and negligible carrier storage effect [10,11,13,15]. A SID can be obtained by shorting a gate to the emitter of the SIT [16,17]. Such diode has all the advantages of the SIT such as thermal stability and short switching time. The cross section of such diode is shown in Fig. 4.11.

The quality of the SID can be further improved with more sophisticated emitters (Fig. 4.10B and C). The SI diode with Schottky emitter was described by Wilamowski in 1983 [18] (Fig. 4.12). A similar structure was later published by Baliga [19].

4.7 Lateral Punch-Through Transistor

Fabrications of SI transistors usually require very sophisticated technology. It is much simpler to fabricate a lateral punch-through transistor (LPTT), which operates on the same principle and has similar characteristics [20] (Fig. 4.13). The cross section of the LPTT is shown in Fig. 4.14.

4.8 Static Induction Transistor Logic

The SITL was proposed by Nishizawa and Wilamowski [5,6]. This logic circuit has almost 100 times better power-delay product than its I^2L competitor. Such drastic improvement of the power-delay product is possible because the SITL structure has a significantly smaller junction parasitic capacitance and also the voltage swing is reduced. Figs. 4.15 and 4.16 illustrate the concept of SITL. Measured characteristics of

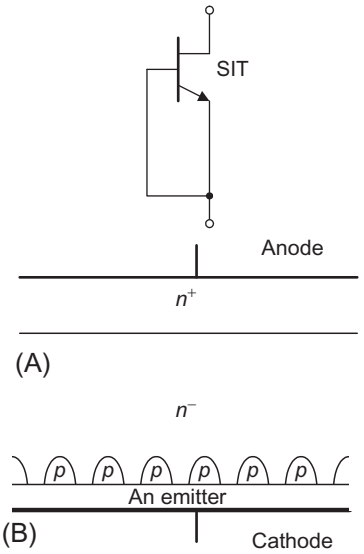


FIG. 4.11 Static induction diode: (A) circuit diagram and (B) cross section.

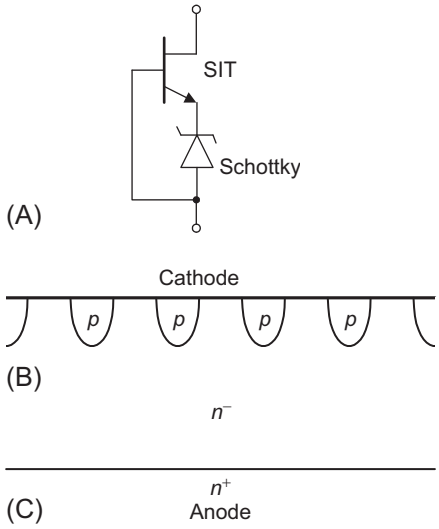


FIG. 4.12 Schottky diode with enlarged breakdown voltages: (A) circuit diagram and (B and C) two cross section of possible implementation.

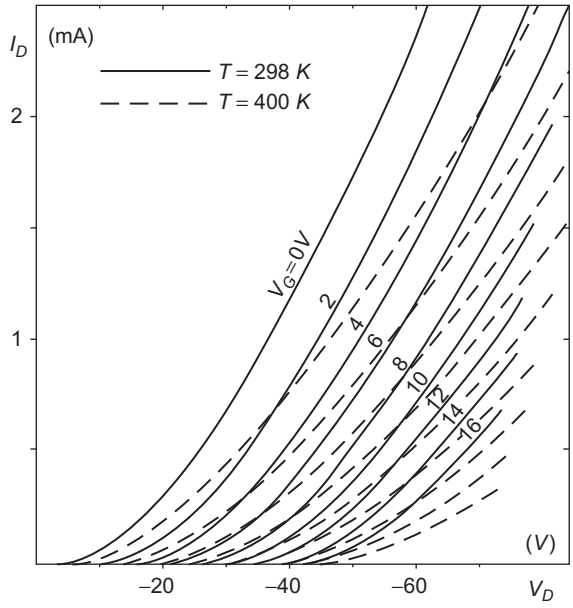


FIG. 4.13 Characteristics of lateral punch-through transistor.

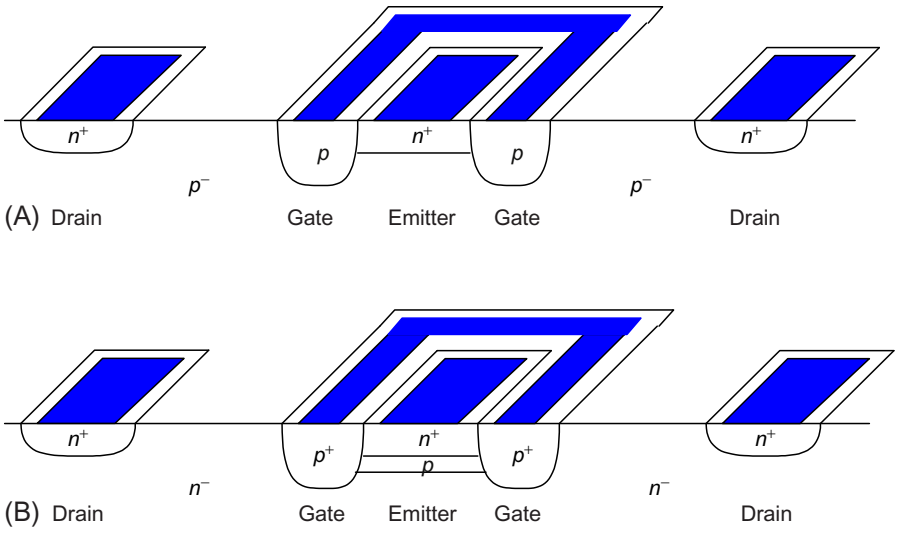


FIG. 4.14 Structures of the lateral punch-through transistors: (A) simple and (B) with sharper potential barrier.

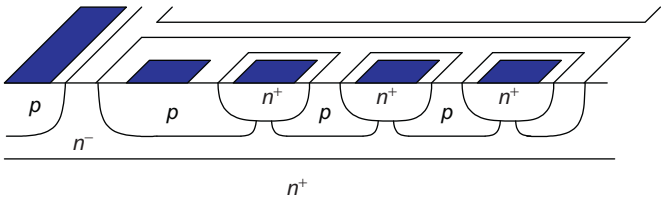


FIG. 4.15 Cross section of SIT logic.

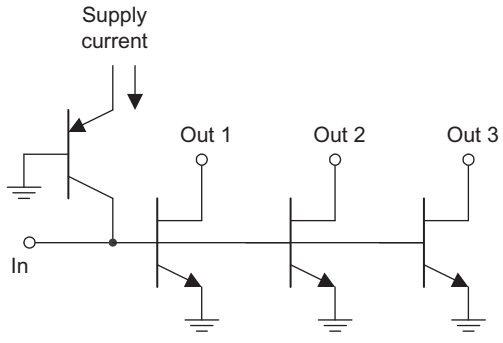


FIG. 4.16 Diagrams of SIT logic.

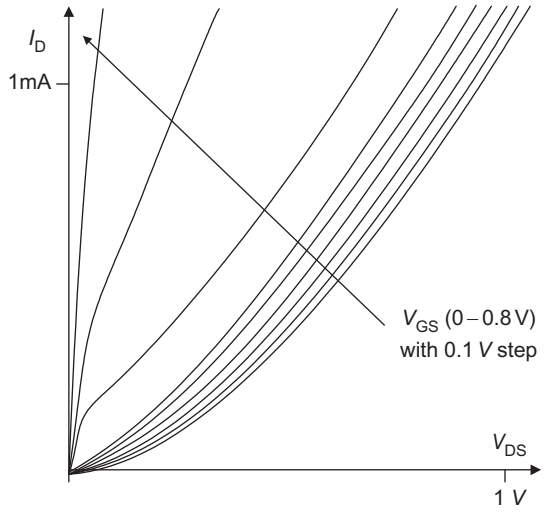


FIG. 4.17 Measured characteristics of *n*-channel transistor of the logic circuit of Fig. 4.16.

n-channel transistor of the static induction logic are shown in Fig. 4.17.

4.9 BJT Saturation Protected by SIT

The SI transistor can also be used instead of a Schottky diode to protect a bipolar junction transistor against saturation [21]. This leads to faster switching time. The concept is shown in Figs. 4.13 and 4.18. Note that this approach is advantageous to the solution with Schottky diode, since it does not require additional area on a chip and it does not introduce additional capacitance between the base and the collector. The base-collector capacitance is always enlarged by the Miller effect, and this leads to slower switching in the case of the solution with the Schottky diode.

4.10 Static Induction MOS Transistor

The punch-through transistor with MOS-controlled gate was described in 1983 [22,23]. In the structure in Fig. 4.19A, current

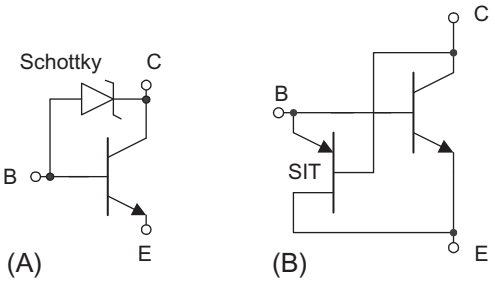


FIG. 4.18 Protection of bipolar transistor against deep saturation: (A) using Schottky diode and (B) using SIT.

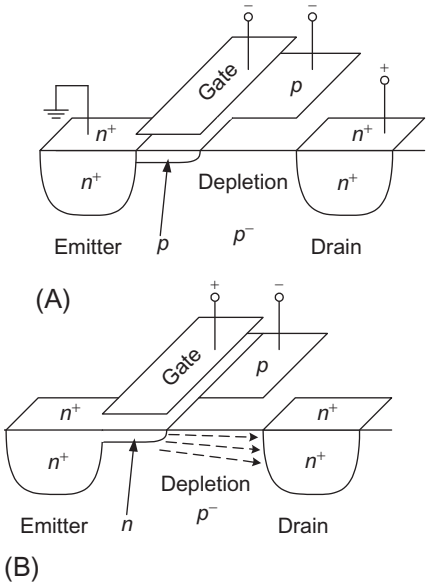


FIG. 4.19 MOS-controlled punch-through transistor: (A) transistor in the punch-through mode for the negative gate potential and (B) transistor in the on-state for the positive gate potential.

can flow in a similar fashion as in the LPTT [20]. In this mode of operation, carriers are moving far from the surface with a velocity close to the saturation velocity. The real advantage of such structure is the very low gate capacitance.

Another implementation of static induction MOS transistor (SIMOS) is shown in Fig. 4.20. The buried p^+ layer is connected to the substrate, which has a large negative potential. As a result, the potential barrier is high, and the emitter-drain current cannot flow. The punch-through current may start to flow

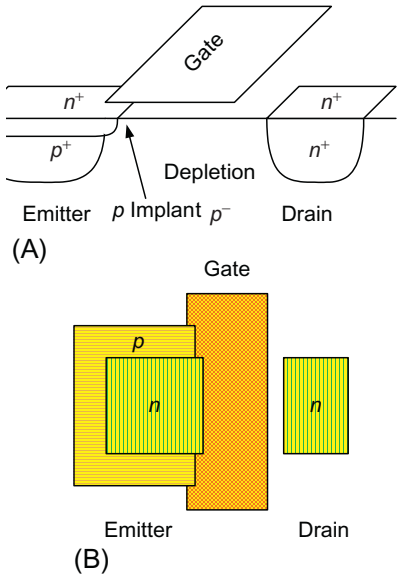


FIG. 4.20 Static induction MOS structure: (A) cross section and (B) top view.

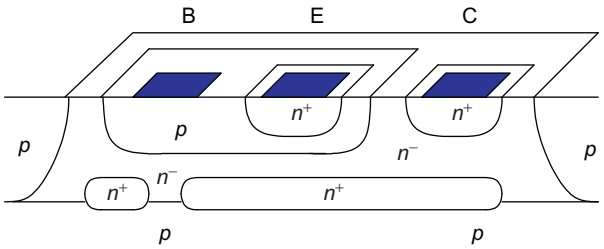


FIG. 4.21 Cross sections of bipolar transistors protected against deep saturation using SIT.

when the positive voltage is applied to the gate, and in this way, the potential barrier is lowered. The *p*-implant layer is depleted, and due to the high horizontal electric field under the gate, there is no charge accumulation under this gate. Such a transistor has several advantages over the traditional MOS transistor (Fig. 4.21).

1. The gate capacitance is very small, since there is no accumulation layer under the gate.
2. Carriers are moving with a velocity close to saturation velocity.
3. Much lower substrate doping and the existing depletion layer lead to much smaller drain capacitance.

The device operates in a similar fashion as MOS transistor in subthreshold conditions, but this process occurs at much higher current levels. Such "bipolar mode" of operation may have many advantages in VLSI applications.

4.11 Space Charge Limiting Load (SCLL)

Using the concept of the space charge-limited current flow, it is possible to fabricate very large resistors on a very small area. Moreover, these resistors have a very small parasitic capacitance. For example, a 50 kΩ resistor requires only several square μm when a 2 μm feature size technology is used [7].

Depending on the value of the electric field, the device current is described by the following two equations. For a small electric field, $v(x) = \mu E(x)$:

$$I_{DS} = \frac{9}{8} V_{DS}^2 \mu \varepsilon_{Si} \varepsilon_0 \frac{A}{L^3} \tag{4.17}$$

For a large electric field, $v(x) = \text{const}$:

$$I_{DS} = 2 V_{DS} v_{sat} \varepsilon_{Si} \varepsilon_0 \frac{A}{L^2} \tag{4.18}$$

Moreover, these resistors, which are based on the space charge limit flow, have a very small parasitic capacitance (Fig. 4.22).

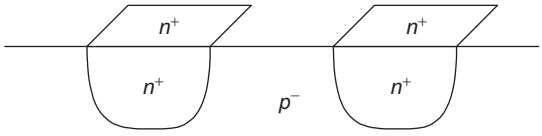


FIG. 4.22 Space charge limiting load (SCLL).

4.12 Power MOS Transistors

Power MOS transistors are being used for fast switching power supplies and for switching power converters. They can be driven with relatively small power, and switching frequencies could be very high. High switching frequencies lead to compact circuit implementations with small inductors and small capacitances. Basically, only two technologies, DMOS and VMOS, are used for power MOS devices as shown in Figs. 4.23 and 4.24.

A more popular structure is the DMOS shown in Fig. 4.24. This structure also uses the SIT concept. Note that for large drain voltages, the *n*-region is depleted from carriers, and statically induced electric field in the vicinity of the virtual drain is significantly reduced. As a result, this transistor may withstand much larger drain voltages, and also the effect of channel length modulation is significantly reduced. The later effect leads to larger output resistances of the transistor. Therefore, the drain current is less sensitive to drain voltage variations. The structure in Fig. 4.24 can be considered as a composition of the MOS transistor and the SIT transistor as is shown in Fig. 4.25.

The major disadvantage of power MOS transistors is relatively large drain series resistance and much smaller

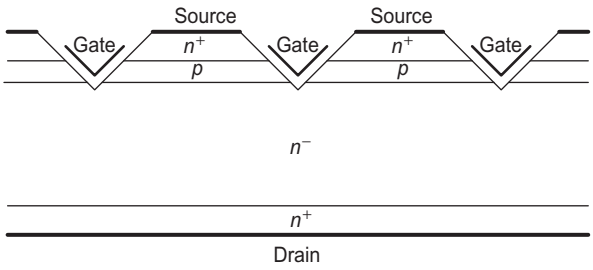


FIG. 4.23 Cross section of the VMOS transistor.

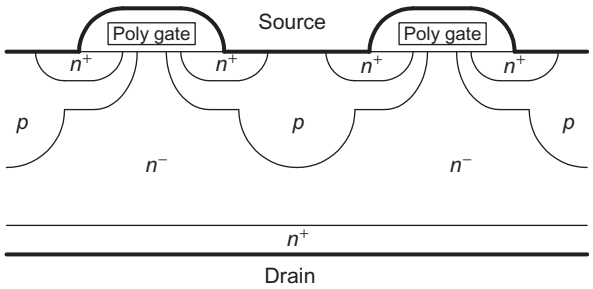


FIG. 4.24 Cross section of the DMOS transistor.

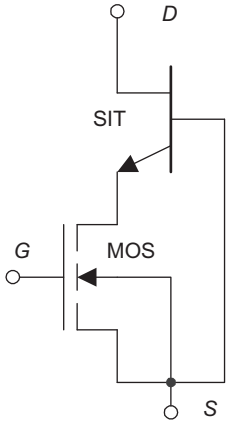


FIG. 4.25 Equivalent diagram with MOS and SIT of the structure of Fig. 4.24.

transconductance in comparison with bipolar transistors. Both of these parameters can be improved dramatically by a simple change of the type of drain, in the case of *n*-channel device from *n*-type to *p*-type drain. This way, the integrated structure is being built where its equivalent diagram consists of MOS transistor integrated with bipolar transistor. Such structure has β times larger transconductance (β is the current gain of bipolar transistor) and much smaller series resistance due to the conductivity modulation effect caused by holes injected into lightly doped drain region. Such device is known as insulated-gate bipolar transistors (IGBT) as shown in Fig. 4.26. Their main disadvantage is large switching time limited primarily by poor switching performance of bipolar transistor. Another difficulty is related to a possible latch-up action of a four-layer $n^+pn^-p^+$ structure. This undesired effect could be suppressed by using heavily doped p^+ region in the base of NPN structure, which leads to significant reduction of the current gain of this parasitic transistor. The gain of other PNP transistor must be kept large, so the transconductance of the entire device is large too. The IGBT transistor has breakdown voltages up to 1500 V; turn off times are in range 0.1–0.5 μs. They may operate with currents above 100 A with a forward voltage drop about 3 V.

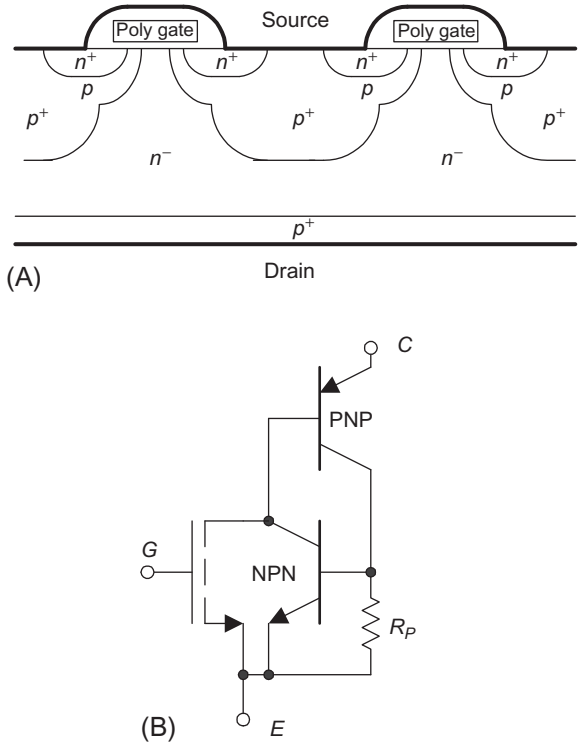


FIG. 4.26 Insulated-gate bipolar transistor (IGBT), (A) cross section and (B) equivalent diagram.

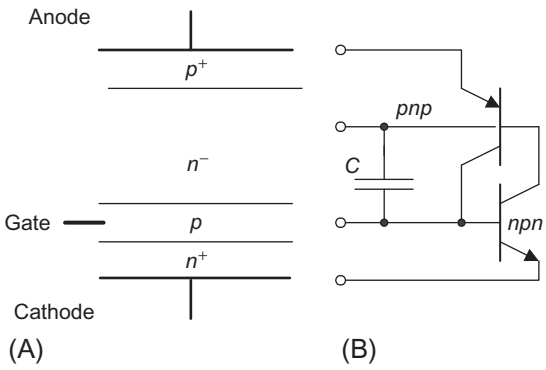


FIG. 4.27 Silicon control rectifier: (A) cross section and (B) equivalent diagram.

4.13 Static Induction Thyristor

There are several special semiconductor devices dedicated to high power applications. The most popular is thyristor known also as silicon control rectifier (SCR). This device has a four-layer structure as shown in Fig. 4.27A, and it can be considered as two transistors *npn* and *pnp* connected as shown in Fig. 4.27B.

In normal mode of operation (anode has positive potential), only one junction is reverse-biased, and it can be represented by capacitance *C*. A spike of anode voltage can therefore get through capacitor *C*, and it can trigger SCR. This behavior is not acceptable in practical application, and therefore, a different device structure is being used as is shown in Fig. 4.28. Note that by shorting gate to cathode by resistor *R*, it is much more difficult to trigger the *npn* transistor by spike of anode voltage. This way, rapid change of anode voltages is not able to trigger thyristor. Therefore, this structure has a very large *dv/dt* parameter.

When NPN transistor is replaced with SI transistor, parameters of a thyristor can be significantly improved. For example, with breaking voltage in the range of 5 kV and current of 600 A,

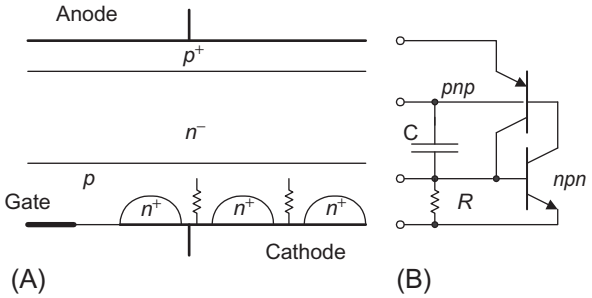


FIG. 4.28 Silicon control rectifier with larger *dv/dt* parameter: (A) cross section and (B) equivalent diagram.

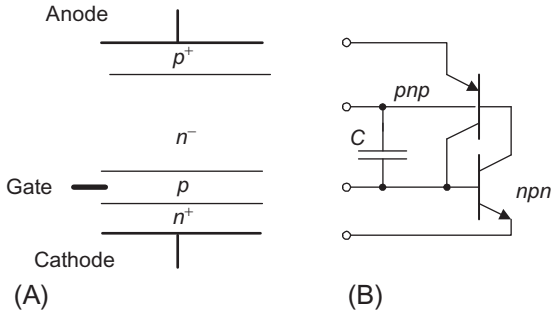


FIG. 4.30 GTO-SIT: (A) cross section and (B) equivalent diagram.

the switching on time can be as short as 100 ns, and *dv/dt* parameter can be as large as 50 kV/s [15,24].

Most of the SCRs sold in the market comprise an integrated structure composed of two or more thyristors. This structure has both large *dv/dt* and *di/dt* parameters. This structure consists of internal thyristor that significantly amplifies the gate signal.

One can notice that the classical thyristor as shown in Fig. 4.27 can be turned off by the gate voltage, while integrated SCR shown in Fig. 4.29 can be only turned off by reducing anode current to zero. Most of the SCRs sold in the market have an integrated structure composed of two or more thyristors. This structure has both large *dv/dt* and *di/dt* parameters.

4.14 Gate Turn Off Thyristor

For the dc operation, it is important to have a thyristor that can be turned off by the gate voltage. Such thyristor has a structure similar to the one shown in Fig. 4.27. It is important, however, to have significantly different current gains β for *pnp* and *npn* transistors. The current gain of *npn* transistor should be as large as possible, and the current gain of *pnp* transistor should be small. The product of β_{npn} and β_{pnp} should be larger than one. This can be easily implemented using SI structure as shown in Fig. 4.30.

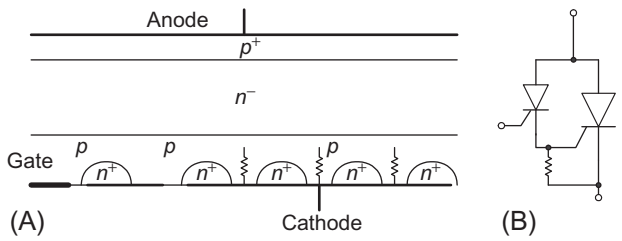


FIG. 4.29 Integrated structure of silicon control rectifier: (A) cross section and (B) equivalent diagram.

References

[1] J. Nishizawa, T. Terasaki, J. Shibata, Field-effect transistor versus analog transistor (static induction transistor), IEEE Trans. Electron Dev. 22 (4) (1975) 185–197.

[2] M. Tatsude, E. Yamanaka, J. Nishizawa, High-frequency high-power static induction transistor, IEEE Ind. Appl. Mag. 1 (2) (1995) 40–45. March/April.

[3] J. Nishizawa, P. Plotka, T. Kurabayashi, Ballistic and tunneling gaas static induction transistors: nano-devices for THz electronics, IEEE Trans. Electron Dev. 49 (7) (2002) 1102–1111.

[4] J. Nishizawa, K. Suto, T. Kurabayashi, Recent advance in tetrahertz wave and material basis, Russ. Phys. J. 46 (6) (2003) 615–622.

[5] J. Nishizawa, B.M. Wilamowski, Integrated logic—state induction transistor logic, in: International Solid State Circuit Conference, Philadelphia USA, 1977, pp. 222–223.

[6] J. Nishizawa, B.M. Wilamowski, Static induction logic—a simple structure with very low switching energy and very high packing density, in: International Conference on Solid State Devices, Tokyo, Japan, 1976, pp. 53–54. Jpn. J. Appl. Phys. 16(1) (1977) 158–162.

[7] B.M. Wilamowski, High speed, high voltage, and energy efficient static induction devices, in: 12 Symposium of Static Induction Devices – SSID'99, (invited speech) Tokyo, Japan, 1994, pp. 23–28.

[8] P. Plotka, B.M. Wilamowski, Interpretation of exponential type drain characteristics of the SIT, Solid State Electron. 23 (1980) 693–694.

[9] P. Plotka, B.M. Wilamowski, Temperature properties of the static induction transistor, Solid State Electron. 24 (1981) 105–107.

[10] C.W. Kim, M. Kimura, K. Yano, A. Tanaka, T. Sukegawa, Bipolar-mode static induction transistor: experiment and two-dimensional analysis, IEEE Trans. Electron Dev. 37 (9) (1990) 2070–2075.

[11] Y. Nakamura, H. Tadano, M. Takigawa, I. Igarashi, J. Nishizawa, Experimental study on current gain of BSIT, IEEE Trans. Electron Dev. 33 (6) (1986) 810–815.

[12] J. Nishizawa, T. Ohmi, H.L. Chen, Analysis of static characteristics of a Bipolar-Mode SIT (BSIT), IEEE Trans. Electron Dev. 29 (8) (1982) 1233–1244.

[13] K. Yano, I. Henmi, M. Kasuga, A. Shimizu, High-power rectifier using the BSIT operation, IEEE Trans. Electron Dev. 45 (2) (1998) 563–565.

[14] K. Yano, M. Masahito, H. Moroshima, J. Morita, M. Kasuga, A. Shimizu, Rectifier characteristics based on Bipolar-Mode SIT Operation, IEEE Electron Dev. Lett. 15 (9) (1994) 321–323.

[15] R. Hironaka, M. Watanabe, E. Hotta, A. Okino, Performance of pulsed power generator using high voltage static induction thyristor, IEEE Trans. Plasma Sci. 28 (5) (2000) 1524–1527.
[16] K. Yano, S. Honarkhah, A. Salama, Lateral SOI static induction rectifiers, in: Proceedings of 2001 International Symposium on Power Semiconductor Devices, Osaka, 2001, pp. 247–250.
[17] K. Yano, N. Hattori, Y. Yamamoto, M. Kasuga, Impacts of channel implantation on performance of static shielding diodes and static induction rectifiers, in: Proceedings of 2001 International Symposium on Power Semiconductor Devices, Osaka, 2001, pp. 219–222.
[18] B.M. Wilamowski, Schottky diodes with high breakdown voltage, Solid State Electron. 26 (5) (1983) 491–493.
[19] B.J. Baliga, The pinch rectifier: a low forward-drop, high-speed power diode, IEEE Electron Dev. Lett. 5 (1984) 194–196.
[20] B.M. Wilamowski, R.C. Jaeger, The lateral punch-through transistor, IEEE Electron Dev. Lett. 3 (10) (1982) 277–280.
[21] B.M. Wilamowski, R.H. Mattson, Z.J. Staszak, The SIT saturation protected bipolar transistor, IEEE Electron Dev. Lett. 5 (1984) 263–265.
[22] B.M. Wilamowski, The punch-through transistor with MOS controlled gate, Phys. Status Solidi (a) 79 (1983) 631–637.
[23] B.M. Wilamowski, R.C. Jaeger, J.N. Fordemwalt, Buried MOS transistor with punch-through, Solid State Electron. 27 (8/9) (1984) 811–815.
[24] N. Shimizu, T. Sekiya, K. Iida, Y. Imanishi, M. Kimura, J. Nishizawa, Over 55 kV/us, dv/dt turnoff characteristics of 4 kV-Static Induction Thyristor for Pulsed Power Applications, in: Proceedings of 2004 International Symposium on Power Semiconductor Devices, Kitakyushu, Japan, 2004, pp. 281–284.

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5

SiC and GaN Power Semiconductor Devices

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5.1 Background

Power semiconductor devices are key components of power electronics technology, used primarily as switches or rectifiers in circuits and systems. Currently, more than 70% of all electric energy consumed is processed by power electronics. The main function of power electronics is to control and transfer the flow of electric energy from one form to another and in a form that is suitable to the user. Semiconductor devices are widespread and can be found in almost every electric and electronic piece of equipment or product. Their power range depends on the application and can be from milliwatts to megawatts. Power devices have a significant impact on the economy as they determine system cost and efficiency.

The invention of the transistor in 1947 by Shockley, Bardeen, and Brattain [1] allowed direct solid-state control of electricity for the first time. However, the application of transistors for controlling electric power was limited until the invention of the thyristor in the late 1950s [2]. Although the thyristor has limited switching capability, it cannot be turned off by external control. Thyristors have been used for the design of different applications, such as control of direct current (DC) motors. The first power bipolar junction transistor (BJT) with substantial power handling capabilities was introduced in the 1960s. The device overcame some of the limitations of the thyristor because it could be switched on or off by applying an external signal.

Further developments of the thyristor led to the realization of a fully controllable switching device, a thyristor that can be turned off using a specialized gate design within the thyristor (GTO) [3]. This enables the GTO to be used in more complex power conversion technology that is capable of controlling power more directly and efficiently. This significant development greatly enhanced power electronics technology.

The metal-oxide-silicon field-effect transistor (MOSFET) was the next major device introduced in the 1970s [4]. It has minimal drive requirements due to its insulated gate. Also, the MOSFET is a voltage-controllable device having high input impedance and fast switching response. MOSFETs are unipolar majority carrier devices that give them a faster switching speed than the BJT or thyristor. On the other hand, the power handling capabilities of the MOSFET are low compared with the thyristor because of high ON-state resistance associated with high blocking voltage.

In the early 1980s, a new process technology was developed allowing MOSFET and BJT technology to be integrated on the same chip [5]. A new device, the insulated-gate bipolar transistor (IGBT), was introduced. IGBTs possess the advantages of both devices: faster switching (inherited from MOSFET) and lower specific ON-state resistance (from the PNP BJT). Improvements in design and technology have made IGBTs popular replacements for BJTs and low- to medium-power

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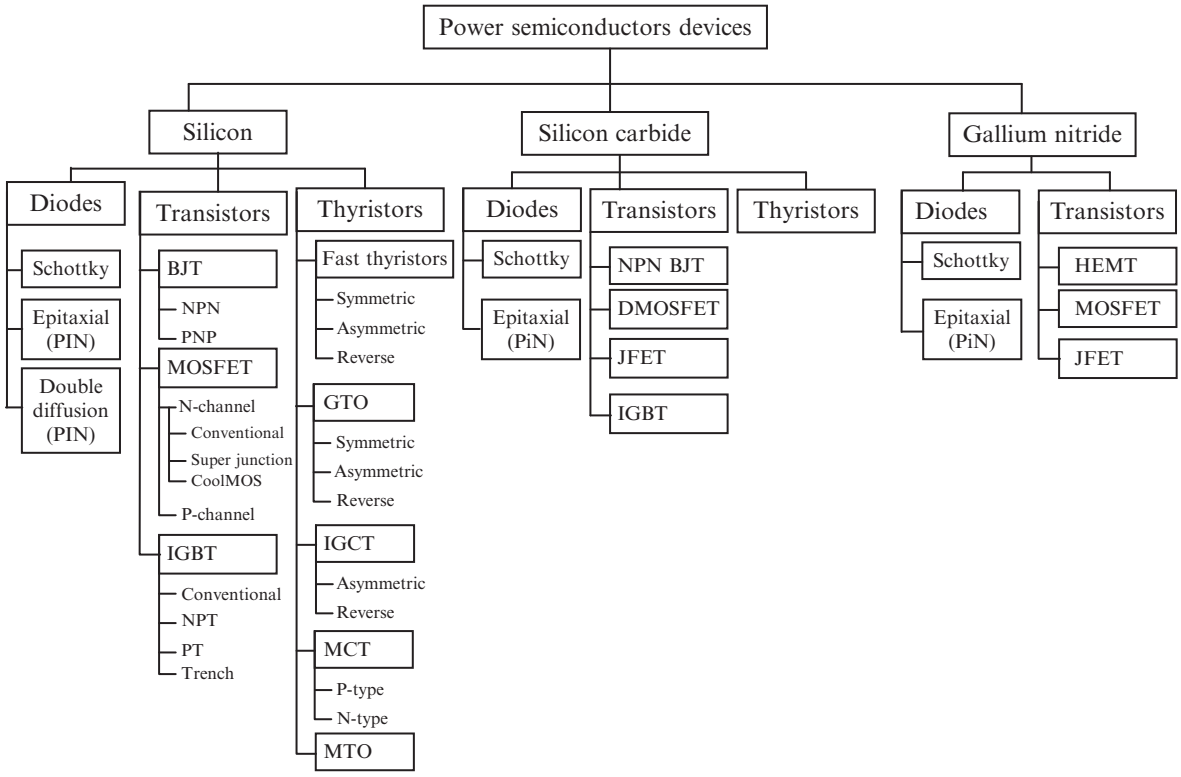


FIG. 5.1 Most important power semiconductor devices on the market along with silicon carbide and gallium nitride power devices that have been developed and studied in recent years.

thyristor technology. The IGBT is presently the dominate semiconductor device for most medium-power applications.

Fig. 5.1 summarizes the most important power silicon (Si) semiconductor devices on the market along with silicon carbide (SiC) and gallium nitride (GaN) power devices that are on the market and others that have been developed and studied in recent years in various semiconductor laboratories. Due to many decades of development, fabrication, and optimization of a large variety of Si devices and a large material abundance, high manufacturing capability, and extremely low cost, Si is still the most used element for production of power semiconductor devices.

Based on their structure, power devices can be classified as diodes, transistors, and thyristors. Si Schottky diodes are typically used for high switching frequencies at low breakdown voltage (BV), $BV \leq 100$ V; the fast switching epitaxial PiN diodes are used for $BV \leq 600 \div 1200$ V, and double-diffused PiN diodes are applied at higher voltages, $BV \geq 1000$ V.

Silicon BJTs have been completely replaced by MOSFETs and IGBTs. By introducing an extra P-doping region in the MOSFET drift region, a high breakdown voltage is achieved with much higher drift doping, which results in a drastic reduction (5–10 times) in specific ON-resistance for the same chip area in a voltage range of $BV = 600$–1000 V.

Large-area Si devices capable of handling thousands of amperes and kilovolts are now available on the market. Metal-oxide-semiconductor (MOS) gate devices, such as IGBTs, are designed using two different structures: punch-through (PT) and nonpunch-through (NPT). Both types of IGBTs can handle voltage up to 3.3 kV and current up to 1.2 kA [6]. IGBT modules for 6.5 kV and 0.6 kA are also available.

Silicon GTOs and thyristors are still widely used for very high-power applications. FMCC group is currently selling asymmetrical GTO thyristors for 4.5 kV and 26 kA [7]. The devices are optimized for low conduction losses, and the switching frequency is in the range of 200–500 Hz for most applications. All GTOs require snubbers for protection during turn-on and turn-off switching. Significant improvement to the GTO structure, including a gate driver, an integrated inverse diode, and better packaging, resulted in a new semiconductor device, the integrated gate-commutated thyristor (IGCT). The IGCTs have much faster turn-off times than GTOs. This allows them to operate at higher frequencies—up to several kilohertz—for very short periods of time. However, the typical IGCT operating frequency is up to 500 Hz due to high switching losses at higher frequencies. Asymmetrical IGCTs, optimized for snubberless turnoff, can operate at 6.5 kV and 4.2 kA. Metal-oxide-semiconductor-controlled thyristors (MCTs) and MOS turn-off thyristors (MTOs) have been proposed, but the market demand for these devices is very low at this time [8].

The need for high-voltage, high-power-density devices operating at high frequencies and junction temperatures higher than 150°C is growing, especially for advanced power electronics. Silicon-based devices are not able to meet these requirements without connecting, in series and in parallel, to a large number of devices using costly active or passive snubbers and expensive cooling systems [9]. For this reason, the limitations of Si material properties for power devices have been debated during the last decade; and wide bandgap semiconductors, such as those made of SiC and GaN, have attracted considerable attention.

Significant research into SiC and GaN as materials for semiconductor devices has been carried out during the last 20 years. Their wide bandgap energy enables the devices to operate at elevated temperatures (600°C) while retaining low leakage current. The higher breakdown strength for a given blocking voltage of SiC and GaN results in smaller drift layers or channel lengths as compared with Si devices. As a result, the storage of the minority carriers or the input and output capacitance and, therefore, the associated switching losses at a given switching frequency are reduced. This leads to an increase of the switching frequency to 0.5–1 MHz with acceptable switching losses, which significantly reduces the size and cost of the passive components in power electronic systems.

Regardless of the advantages that SiC and GaN materials possess, they have not been adopted for manufacturing of the entire family of high-power devices. Difficulty with crystal growth, the presence of crystal defects, such as micropipes and dislocations, and the absence of abundant wafer suppliers have all contributed to a lack of progress in the fabrication of SiC and GaN power devices by the commercial sector [10]. Several industrial research groups and university labs have been working on improving the material properties and development of SiC and GaN power devices. In September 2001, two companies advertised the commercial availability of SiC Schottky diodes: Infineon (from 600 V up to 6 A or from 300 V up to 10 A) and Microsemi (100-200-480 V, 1A) [11]. Five years later, in February 2006, the first commercially available GaN high-electron-mobility transistor (HEMT) products were launched by Eudyna Devices (now Sumitomo Electric Device Innovations USA, Inc.) [12]. Since then, new SiC and GaN devices and new companies have been introduced to the market. In the next sections, the physical properties of SiC and GaN materials are compared with Si material, and the new devices are discussed.

5.2 Silicon Carbide and Gallium Nitride Materials

This chapter includes details on the physical and electric characteristics of SiC and GaN materials and highlights on the advantageous properties of power semiconductor devices fabricated from them.

5.2.1 Silicon Carbide Polytypes

SiC is known as a classical polytypic substance existing in more than 250 polytypes; the common polytypes are 6H, 15R, 4H, and 3C [13]. The letters H, C, and R denote the overall lattice type as being hexagonal, cubic, or rhombohedral, respectively. All polytypes have a hexagonal frame with a carbon (C) atom positioned at the center of the mass of the tetragonal structure outlined by the four neighboring Si atoms, and the distance between a C atom to each of the Si atoms is the same [14].

Polytypes are formed by stacking SiC molecules on top of each other in a certain order. The stacking order between succeeding double layers of C and Si atoms determines the difference between polytypes. During substrate manufacturing for semiconductor devices, it is important that the entire wafer is a single polytype. Growth conditions during substrate production should be stable because any instability in the growing process leads to spontaneous switching from one polytype to another. This will alter the electric properties of the material and act as a nucleation site for defects such as micropipes [15].

Currently, two SiC polytypes are accepted in SiC device research: 6H-SiC and 4H-SiC. Before the introduction of 4H-SiC wafers in 1994, 6H-SiC was the dominant polytype. Since then, both polytypes have been used in research; but recently, 4H-SiC has become the more dominant polytype. This is because the charge-carrier mobilities in 4H-SiC are identical along the two planes of the semiconductor, whereas the 6H-SiC polytype exhibits anisotropy, which means that the mobilities of the material in the two planes are not the same.

5.2.2 Gallium Nitride Crystal Structures

Gallium nitride is found in three crystal structures: wurtzite, zinc blende, and rock salt. At ambient conditions, GaN crystalizes in a wurtzite-type structure [16], while the zinc-blende and rock-salt cubic GaN structures are metastable structures [17] at normal conditions. The zinc-blende GaN structure is formed during a film preparation process [18], while the rock-salt cubic GaN structure is formed under ultrahigh pressure of at least 37 GPa, and when the pressure is completely released, the rock-salt structure transfers back to the wurtzite structure [19]. The zinc-blende GaN structure is not an equilibrium phase, and the growth of it would cost extra energy [20]. The wurtzite crystal structure of GaN material exhibits a variety of material properties, such as spontaneous polarization and piezoelectric polarization effects, which are very important in the design of GaN heterostructure devices [21]. Also, the GaN wurtzite crystal structure has a wider bandgap than the zinc-blende structure [22], which is also an advantage for using the wurtzite structure in the fabrication of power devices.

5.2.2.1 Silicon Carbide and Gallium Nitride Physical and Electrical Properties

Silicon carbide and GaN materials display a wide range of properties, such as high breakdown electric field strength, high

TABLE 5.1 Physical properties for various semiconductors

Material	E_G (eV)	E_C (MV cm^{-1})	n_i (cm^{-3})	ε_r	μ_r (cm^2 V^{-1} s^{-1})	v_{SAT} (10^7 cm s^{-1})	σ_T (W m^{-1} K^{-1})	CTE (ppm K^{-1})
Si	1.1 [23]	0.3 [23]	10^{10} [23]	11.9	1400 [23]	1.02 [23]	130 [23]	2.6 [23]
GaAs	1.424 [23]	0.4 [23]	2.1×10^6	13.1	8500 [23]	2.0 [24]	55 [23]	5.73 [23]
3C-SiC	2.36 [25] [26]	1 [25]	10 [27]		≤800 [25]	2.0	360 [25]	3.8 [25]
4H-SiC	3.23 [25]	3–5 [25]	8.2×10^{-9}	10.1	≤900 [25]	2.0	370 [25]	5.12 [25]
6H-SiC	3.0 [25]	3-5	2.3×10^{-6}	9.66	≤400 [25]	2.0	490 [25]	4.3–4.7 [25]
GaN wurtzite	3.39 [25]	3-5 [25]	1.9×10^{-10}	9	≤1000 [25]	2.2	130 [25]	3.2–5.6 [25]
GaN zinc blende	3.2 [28]							
Diamond	5.45 [29]	5.6 [29]	1.6×10^{-27} [29]	5.5	1900 [29]	2.7 [29]	600–2000 [29]	0.8 [29]

saturated drift velocity, and high thermal stability, which make it attractive for use as a material for semiconductor devices. Table 5.1 summarizes some of these properties for the most popular wide bandgap semiconductors and Si. Some of the properties that benefit power semiconductor devices are strongly dependent on the bandgap. These properties are critical electric field, intrinsic carrier concentration, and to a lesser extent mobility and conductivity.

Silicon carbide is from the IV–IV group semiconductor family and has an indirect bandgap. Every SiC polytype has a different bandgap. Gallium nitride is from the III–V semiconductor family and has a direct bandgap. The bandgaps of 4H-SiC and GaN wurtzite-type structures at room temperature are 3.23 and 3.39 eV [25], which are more than three times higher than the bandgap of Si.

5.2.2.2 Critical Electric Field

The specific ON-state resistance, R_{SP-ON}, is an important device parameter for determining the device conduction losses. It is based on the critical electric field of the material, ε_c. Knowing the energy bandgap of the material, the critical electric field can be calculated. An expression for the critical electric field as a function of the bandgap energy for the indirect bandgap materials, such as SiC, is [30]

$$\varepsilon_c = 2.38 \times 10^5 E_G^2 \tag{5.1}$$

and an expression for the critical electric field for the direct bandgap materials, such as GaN, is [30]

$$\varepsilon_c = 1.73 \times 10^5 E_G^{2.5} \tag{5.2}$$

There is no dependence on the background doping included in these expressions because the voltage blocking capability, during the OFF-state of power electronic devices, depends on the property of the lightly doped drift region [30]. For Si, an expression for a relationship between the critical electric field, ε_c, and the bandgap, E_G, [31] is

$$\varepsilon_c = 1.02 \times 10^7 \sqrt{\frac{q}{\varepsilon_0 \varepsilon_r}} N_{N^-}^{1/8} E_G^{3/4} \tag{5.3}$$

where N_N^- is the doping concentration in the lightly doped drift region, N^- region; q is the unity electric charge ($\cong 1.6 \times 10^{-19}$), $\varepsilon_0 = 8.85 \times 10^{-14}$ F/cm; and ε_r is the Si dielectric constant. Assuming that the doping concentration in the lightly doped drift region, N^- region, is approximately 5×10^{13} cm^{-3}, the electric field can be represented by the formula:

$$\varepsilon_c = 2.5 \times 10^5 E_G^{3/4} \tag{5.4}$$

The critical electric fields of SiC and GaN materials are high as compared with Si because they have wider bandgaps. A wider bandgap of SiC or GaN material indicates that the energy required to break a bond is significantly higher than the energy required for the Si material. This allows a larger electric field to be applied before the avalanche of a multitude of ionized carriers occurs in the semiconductor. A more than 10 times higher critical electric field for SiC and GaN materials compared with Si allows power devices to be designed with thinner, more highly doped drift regions to achieve similar blocking voltages.

The specific ON-resistance can be related to the breakdown voltage, BV; electron mobility, μ_n; relative permittivity, ε_r; and bandgap energy, E_G.

For Si, the specific ON-resistance can be calculated by the following equation [32]:

$$R_{SP-ON} = \frac{1.716 \times 10^{-6} \varepsilon_r BV^{2.5} E_G^{-3}}{\mu_n} \tag{5.5}$$

For SiC, the specific ON-resistance is [33]

$$R_{SP-ON} = \frac{3.351 \times 10^{-3} BV^2 E_G^{-6}}{\varepsilon_r \mu_n} \tag{5.6}$$

For GaN, the specific ON-resistance is [33]

$$R_{SP-ON} = \frac{8.725 \times 10^{-3} BV^2 E_G^{-7.5}}{\varepsilon_r \mu_n} \tag{5.7}$$

Fig. 5.2 presents a theoretical, specific ON-state resistance of blocking regions designed for certain breakdown voltages in Si, 4H-SiC, and GaN under optimum punch-through conditions using Eqs. (5.5)–(5.7).

From Fig. 5.2 and Eqs. (5.5)–(5.7), it can be deduced that, for the same blocking voltage, SiC and GaN devices offer specific ON-resistance that is more than 350 times lower than their Si counterparts. The doping concentration also affects the

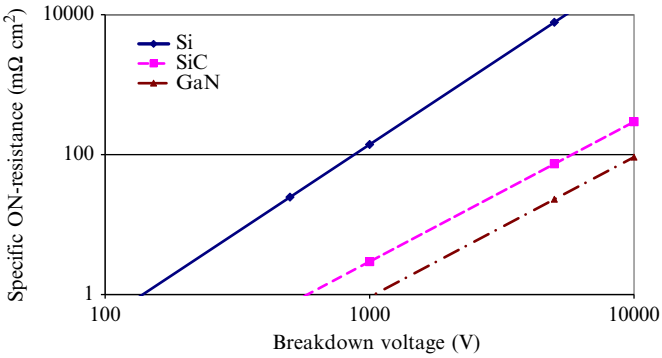


FIG. 5.2 Specific ON-state resistance of the blocking regions in function of the breakdown voltages for Si, 4H-SiC, and GaN.

blocking voltage. For the same blocking voltage, the background doping in a SiC and a GaN device can be 10–100 times higher than that of a Si device. An increase in doping concentration will also lead to a decrease in specific ON-resistance. This is one of the most important advantages of high-voltage SiC and GaN devices because for the same blocking voltage, the ON-resistance is much lower. The fact that the devices can be made thinner and more highly doped means that SiC and GaN devices have the capability of operating at a higher frequency. Thinner devices are faster because the carriers do not have to travel as far through the device and have less volume of stored charge (bipolar devices).

5.2.2.3 Intrinsic Carrier Concentration

The intrinsic carrier concentration of a semiconductor completely free of impurities and defects is the number of excited electrons from the valence band occupying energy-momentum states in the conduction band (and also the number of excited holes in the valence band) per unit volume. It is given by the equation:

$$n_i = (N_C N_V)^{\frac{1}{2}} e^{-\frac{E_G}{2kT}} \tag{5.8}$$

where N_C and N_V are the effective density of states in the conduction and in the valence band, respectively; E_G is the energy bandgap; k is Boltzmann's constant (1.381×10^{-23} J K^{-1}); and T is the absolute temperature in Kelvin, and it is assumed that $kT \leq E_G/5$.

Due to the wide bandgaps of SiC and GaN materials, their room-temperature intrinsic carrier concentrations are very small, $\sim 8.2 \times 10^{-9}$ cm^{-3} for SiC and 1.6×10^{-10} for GaN, while the intrinsic carrier concentration of Si is 1.45×10^{10} cm^{-3}. Wide bandgap semiconductors have the advantage of operating at high temperature and radiation fluxes because degradation effects due to thermally generated carriers are small. As the temperature increases, the electron's thermal energy in the valence band increases leading to a condition where any effects due to impurity doping are negated. This condition at elevated temperatures effectively causes the semiconductor to act as if it were intrinsic (no impurity doping). The temperature at which this condition occurs for Si is about 150°C, while SiC has a wide bandgap, and the valence electrons require more thermal energy to move from valence to conducting band. This intrinsic temperature for SiC is ~900°C.

Radiation energy/particle flux can also excite an electron and make it move to the conducting band. Similar to temperature, a wide bandgap material will require more radiation energy to free an electron from the conducting band.

As a result of a wide bandgap, devices built with SiC and GaN can endure more heat and radiation without losing their designed electric properties. Devices using the wide bandgap materials can theoretically operate in extreme conditions where Si-based devices cannot.

5.2.2.4 Saturated Drift Velocity

The saturated drift velocity is also one of the most important device-related characteristics of a semiconductor because it determines the frequency limits of power devices and, consequently, the range of their most efficient use. The high-frequency capability of a semiconductor material is directly proportional to the material drift velocity. The drift velocity of 4H-SiC (2×10^7 cm s^{-1}) and a GaN wurtzite crystal structure (2.2×10^7 cm s^{-1}) is approximately twice as large as the drift velocity of Si (10^7 cm s^{-1}); hence, it is expected that 4H-SiC- and GaN-based power devices could be switched at significantly higher frequencies as compared with their Si counterparts. In addition, a higher drift velocity allows charge in the depletion region to be removed faster; therefore, the switching losses are smaller since the reverse recovery current is smaller, and the reverse recovery time is shorter.

5.2.2.5 Thermal Stability

As was mentioned previously, one of the advantages of 4H-SiC- and GaN-based semiconductor devices is that they can operate at high temperatures due to the wide bandgap. Besides this, 4H-SiC has another thermal advantage—significantly high thermal conductivity, $\lambda_{SiC} = 4.9$ W cm^{-1} K^{-1}, compared with the conductivity of Si, $\lambda_{Si} = 1.5$ W cm^{-1} K^{-1}. This means that SiC-based devices can operate at higher power densities. The thermal conductivity of GaN, $\lambda_{GaN} = 1.3$ W cm^{-1} K^{-1}, is approximately equal to the thermal conductivity of Si. For low-power-density applications, the losses are not much larger, and the device temperature does not exceed the maximum operating junction temperature. Therefore, GaN devices can be built on Si substrates. Silicon is an important material in these applications because there are high quantities of inexpensive Si substrates available compared, for example, with SiC substrates. Thus, the use of Si as a substrate material is desirable, primarily for cost reasons. However, using Si substrates for GaN devices also introduces a number of critical issues due to the lattice mismatch and the difference in the thermal expansion coefficients, which affect the quality and device reliability [34]. For high-power-density applications, the GaN devices should be grown on a SiC substrate.

The junction-to-case thermal resistance $\left(R_{th-jc}\right)$ of a device is calculated by the following equation:

$$R_{th-jc} = \frac{d}{\lambda A} \tag{5.9}$$

where d is the length (cm), in the direction of the heat flow, and A is the cross-sectional area (cm^2) perpendicular to the direction of heat flow. Since the 4H-SiC thermal conductivity is three times higher as compared with Si, the junction-to-case thermal resistances of 4H-SiC devices are three times lower than their Si counterparts. Lower R_{th-jc} indicates that the heat generated in a 4H-SiC substrate during the operation could more easily flow (diffuse) to the case, to the heat sink, and then to the environment. Therefore, the advantage of 4H-SiC devices or GaN devices on SiC substrate is faster heat dissipation, reducing the requirement for a heavy heat sink and complex thermal packaging. There is also a real benefit in terms of long-term reliability due to potentially lower thermal stresses.

5.2.2.6 Coefficient of Thermal Expansion

All materials change their size when subjected to a temperature change as long as the pressure is held constant. The coefficient of thermal expansion (CTE) describes a change in the size of an object with a change in the temperature. It is the fractional change in the volume of the object per degree change in temperature at a constant pressure. During the design of high-power semiconductor devices, it is necessary for the semiconductor CTE to closely match the package substrate CTE to minimize shear stresses at material interfaces.

The CTE of 4H-SiC is 5.2 ppm K^{-1}, and the CTE of GaN is from 3.2 to 5.6 ppm K^{-1} [25]. The two coefficients are significantly larger than the CTE of Si (2.6 ppm K^{-1}). The CTE of most package materials is higher than 4.5 ppm K^{-1}. The best matches of the package materials and 4H-SiC and GaN are AlN substrate (4.5 ppm K^{-1}), beryllia (BeO) substrate (6.1 ppm K^{-1}), and alumina (Al_2O_3) substrate (6.5 ppm K^{-1}).

5.2.2.7 Figure of Merit

To compare the performance of power semiconductor technologies and devices, two groups of figures of merit (FOMs) are used. The first group includes FOMs that are functions of the intrinsic material parameters, and they are used to compare technologies or materials. A larger FOM number, for the first group, represents better performance. The second group includes FOMs that are functions of the device parameters. They are used to compare device performance in a power system. A smaller FOM number, for the second group, means better device performance.

FOM for materials and technology

The Baliga high-frequency figure of merit (BHFFOM) is derived to compare the performance of power semiconductor devices operating at high frequencies. Baliga relates the power losses of the devices to the intrinsic material parameters and shows that the switching loss of a power semiconductor device depends on the electron mobility, μ_n, and the critical electric field, ε_C. The BHFFOM is given by the following equation [35]:

$$\text{BHFFOM} = \mu_n \varepsilon_c^2 \sqrt{\frac{V_G}{4BV^3}} \tag{5.10}$$

where V_G is gate drive voltage. For high-frequency operation, the power losses can be reduced by using semiconductors with a larger mobility and critical electric field for breakdown [35]. The FOMs for 4H-SiC and a GaN wurtzite crystal structure normalized to Si are given in Table 5.2. For calculation of BHFFOMs, it is assumed that the gate drive voltage, V_G, and the breakdown voltage, BV, are the same for Si, 4H-SiC, and GaN devices. The results show an 81.6 times bigger BHFFOM for 4H-SiC compared with Si and a 197.1 bigger BHFFOM for GaN compared with Si. Therefore, significant performance improvement for high-frequency operation can be achieved by replacing Si with SiC and GaN.

Johnson's figure of merit (JFOM) shows that the performance limits and power-frequency limits of a power device are set by the intrinsic material parameters, such as the critical electric field, ε_c, and its electron saturation velocity [36]:

$$\text{JFOM} = \frac{\varepsilon_C^2 v_{sat}^2}{4\pi^2} \tag{5.11}$$

For high-power and high-frequency operation, the devices should be based on semiconductor materials with both large breakdown voltage and high electron velocity. Therefore, wide bandgap materials, like GaN and SiC, are having higher critical electric fields and electron saturation velocities and, therefore, higher JFOM. Table 5.2 provides calculated JFOM results for 4H-SiC and GaN wurtzite crystal structure normalized to Si, which confirms that 4H-SiC and GaN have 488 and 1284 times higher JFOM, respectively, compared with Si.

In Ref. [37], JFOM is also presented as a function of the cut-off frequency, f_T, which is related to the effective saturation velocity and the breakdown voltage, BV, that can be related to the critical electric field.

$$\text{JFOM} = \frac{2}{\alpha} f_T BV \tag{5.12}$$

TABLE 5.2 Figures of merit for 4H-SiC and a GaN wurtzite crystal structure normalized to Si

FOM	Si	4H-SiC	GaN
BHFFOM	1	81.6	197
JFOM	1	488	1284
BFOM	1	6.15	8.97

The FOMs discussed above are connected to the switching losses of power devices. Power losses of semiconductor devices also include static or ON-state losses, which depend on the specific ON-resistance of the devices. Baliga related the specific ON-resistance to the breakdown voltage, BV; electron mobility, μ_n; relative permittivity ε_r; and critical electric field, ε_c, by the following equation [38]:

$$R_{SP-ON} = \frac{4BV^2}{\varepsilon_r \mu_n \varepsilon_c} \tag{5.13}$$

The denominator of Eq. (5.13) is known as the Baliga figure of merit (BFOM) for resistivity or ON-losses:

$$\text{BFOM} = \varepsilon_r \mu_n \varepsilon_c \tag{5.14}$$

Table 5.2 also gives the calculated results for the BFOM for 4H-SiC and a GaN wurtzite crystal structure normalized to Si. The results confirm that 4H-SiC and GaN have better FOM indexes, that is, 6.15 and 8.97 times higher, respectively, compared with Si.

The ability of GaN to form heterojunctions makes it superior compared with SiC for transistors, although the two materials have similar breakdown fields and saturation electron velocities. GaN can be used to fabricate HEMTs, whereas SiC is currently only used to fabricate metal-semiconductor field-effect transistors (MESFETs) and power MOSFETs. Significantly high mobility (2500 $\text{cm}^2\,\text{Vs}^{-1}$ [39]) in the two-dimensional electron gas (2DEG) and high carrier concentration for HEMTs leads to low channel resistance, which is especially important for high-frequency operation in power switching applications .

FOM for devices

Designers of power electronic systems are using FOMs that are related to the device's parameters. The lower the index value of these FOMs, the better the device performance. Two devices with the same value perform the same in a given application.

The switching losses figure of merit (SLFOM) is used to evaluate the switching performance of field-effect transistors (FETs). SLFOM is a product of the specific ON-resistance of a device, R_{SP-ON}, and its gate to drain charge, Q_{GD}, [40]:

$$\text{SLFOM} = R_{SP-ON} Q_{GD} \tag{5.15}$$

The gate-to-drain charge, Q_{GD}, of an FET is a main parameter of the turn-on loss of a FET. Some companies, for example, provide the gate-to-drain charge, Q_{GD}, and gate-to-source charge, Q_{GS} [41]. In this case, a more accurate value of SLFOM can be obtained [42]:

$$\text{SLFOM} = R_{SP-ON} Q_{SW} \tag{5.16}$$

where Q_{SW} is known as the switching charge, and it is equal to the sum of Q_{GD} and Q_{GS}. The charge Q_{GS} is the portion of the gate-to-source charge from the device threshold voltage to the gate plateau voltage, which controls the current rise and fall of the device. Since SiC and GaN have a bigger bandgap than Si, their channel width is smaller, and, therefore, their gate-to-drain and gate-to-source capacitance are smaller. Consequently, their gate-to-drain charge and gate-to-source, Q_{GD} and Q_{GS}, are smaller. Also, as mentioned above, R_{SP-ON} of SiC and GaN devices is smaller than R_{SP-ON} of Si devices. Therefore, the SLFOMs of SiC and GaN devices are smaller than the SLFOM of a Si device.

The conduction loss figure of merit (CLFOM) is used to evaluate a FETs' performance. CLFOM is a product of ON-state resistance, R_{SP-ON}, and total gate charge, Q_G [43]:

$$\text{CLFOM} = R_{SP-ON} Q_G \tag{5.17}$$

For a given MOSFET technology, both parameters, R_{SP-ON} and Q_G, are opposite of each other. A device with a lower ON-state resistance has a higher gate charge and vice versa [44]. The ON-state resistance, total gate charge, and switching charge are not constants. The ON-state resistance and total gate charge values depend on the gate-source voltage, V_{GS}, and are also influenced by the junction temperature, T_J. Furthermore, the ON-state resistance of a MOSFET depends on the drain current, I_D, while the total gate charge depends on the drain-source voltage, V_{DS}. The switching charge, Q_{SW}, also depends on the drain-source voltage, V_{DS}.

A proper comparison of devices using SLFOM and CLFOMs is possible when it is made under the same conditions [44]. The more proper CLFOM is given in [43] and [44]:

$$\begin{aligned}\text{SLFOM}(V_{GS}, T_J, I_D, V_{DS}) = {} & R_{SP-ON}(V_{GS}, T_J, I_D) \\ & \times Q_{SW}(V_{GS}, T_J, V_{DS})\end{aligned} \tag{5.18}$$

$$\begin{aligned}\text{CLFOM}(V_{GS}, T_J, I_D, V_{DS}) = {} & R_{SP-ON}(V_{GS}, T_J, I_D) \\ & \times Q_G(V_{GS}, T_J, V_{DS})\end{aligned} \tag{5.19}$$

The SLFOM and CLFOM for Si, SiC, and GaN devices on the market are given in Table 5.3. Although a fair comparison between the devices cannot be done because for the same blocking voltage, they are designed for different drain currents; the SiC and GaN devices have better FOMs than the Si device. A device with a higher drain current will have a bigger area and, therefore, a higher gate-to-source and gate-to-drain capacitance and a high switching charge. It will also have smaller ON-resistance. For breaking voltage equal to 650 V, the smallest figure of merit has the GaN Systems GaN device. The two Cree devices, C3M0065090J and CPM2-1700-0045B, are designed for 900 and 1700 V, correspondingly, but the 900 V device has higher ON-resistance, 65 Ω, compared with the 1700 V device with an ON-resistance of 45 Ω. The low ON-resistance of the 1700 V device can be due to the higher design's drain current than the 900 V device. Also, the 1700 V device is more mature. The maturation of the SiC and GaN technology will result in new devices with smaller FOMs, which will be more attractive for power electronic applications.

TABLE 5.3 Parameters and FOMs for Si, SiC, and GaN devices

Material	Part number	Company (reference)	VB (V)	I_D (A)	R_{SP_ON} (mΩ)	Q_{SW} (nC)	Q_G (nC)	SLFOM	CLFOM
Si	IPB65R045C7	Infineon [45]	650	46	45	53	93	2385	4185
SIC	SCT3017AL	ROHM [46]	650	118	17	110	172	1870	2924
SiC	C3M0065090J	Cree [47]	900	35	65	18.7	30	1215.5	1950
SiC	CPM2-1700-0045B	Cree [48]	1700	72	45	101	188	4545	8460
GaN	GS66508B	GaN Systems [49]	650	30	50	4	5.8	200	290
GaN	PGA26E19BA	Panasonic [50]	600	10	140	3.3	NA	462	NA

5.3 SiC Power Devices

5.3.1 Introduction

Due to the significant improvements in SiC material growth technology, SiC-based power devices are available for high-power, high-temperature, and high-frequency applications. Three types of SiC power devices, diodes, transistors, and thyristors, have been designed, modeled, and characterized during the last two decades. Some of them are on the market, and others are in a development stage. Designers are trying to improve the performance of these devices and optimize their FOM parameters to obtain the best ratio between conduction and switching losses, resulting in higher system efficiency [51]. The physics and important parameters of SiC power devices are discussed in this chapter.

5.3.2 SiC Power Diodes

The power diodes are the key components used in power electronic applications. A power diode is often used as a parallel diode to the switch body diode for decreasing the switching losses. Basically, SiC power diodes can be classified into three types: (1) SiC Schottky diode; (2) SiC PiN diode; and (3) SiC merged PN-Schottky diode (MPS), also called a junction barrier Schottky (JBS) diode.

5.3.2.1 SiC Schottky Diode

The SiC Schottky diode was the first SiC device on the market by Infineon Technologies (from 600 V up to 6 A or from 300 V up to 10 A) and Microsemi (100-200-480 V, 1 A) [11]. Now, 15 years later, from 1700 V up to 50 A with zero reverse recovery, zero forward recovery, high-frequency operation, temperature-independent switching behavior, extremely fast switching, and positive temperature coefficient on the forward voltage, V_F, diodes are available [52]. The commercially available Si Schottky diodes are usually rated at maximum breakdown voltages of <100 V [53]. Beyond this limit, Si Schottky diodes cannot compete with Si PiN diodes due to the unacceptably large ON-state resistance of Schottky diodes and the voltage blocking limit due to barrier lowering.

An advantage of high-power SiC Schottky diodes is that they have zero reverse recovery charge since they are majority carrier devices. The reverse recovery current peak is very small compared with a fast Si PiN diode leading to significantly lower turn-OFF losses. The reverse recovery current is due to the displacement current from the junction capacitance. Since the dynamic characteristic of a Schottky diode is capacitive in nature, the reverse recovery characteristic of a SiC Schottky diode is independent from forward current, di/dt, and device junction temperature [54].

A power SiC Schottky diode is formed by the junction of a semiconductor (SiC) with a metal (titanium (Ti), nickel (Ni), gold (Au), or platinum (Pt)) that forms a Schottky barrier. The semiconductor is grown on a substrate that forms an ohmic contact with another metal, as shown in Fig. 5.3.

A Schottky diode is a unipolar device, which means that the current conduction is governed only by majority carriers (electrons). Similar to a Si Schottky diode, the forward voltage of SiC, V_F, is one of the important parameters when selecting a Schottky diode. It is a function of temperature, Schottky barrier height, and drift region resistance. A dependence of the voltage drop and the current density, J_F, is given by the following equation:

$$V_F = \frac{nkT}{q} \ln\left(\frac{J_F}{A^* T^2}\right) + \phi_B/q + R_{SP_ON} J_F \tag{5.20}$$

where n is the ideality factor. For an ideal device, n is equal to one, while for a real device, n is larger than 1 and can be assumed to be between 1 and 1.3. Boltzmann's constant is k, q is the electron charge, T is the absolute temperature, and A^* is Richardson's constant with theoretical values of 146 A cm^{-2}K^{-2} for 4H-SiC [55] and 110 A cm^{-2}K^{-2} for Si. For the same current density and at room temperature (300 K), the voltage of the first member of the right side of Eq. (5.20) for SiC will be 7 mV smaller.

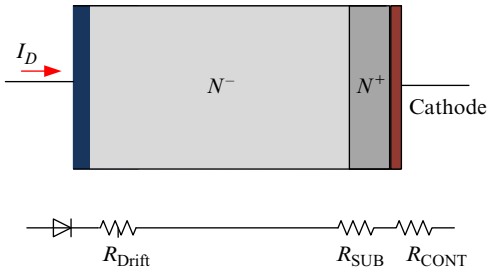


FIG. 5.3 Schottky diode structure and simple model.

The potential barrier at the metal-semiconductor interface, ϕ_B, given in Eq. (5.20), is known as the Schottky barrier height. It can be calculated by the equation:

$$\phi_B = \phi_m - \chi \tag{5.21}$$

where ϕ_m is the work function of the metal and χ is the material's electron affinity. The measured and calculated barrier heights for selected metal/4H-SiC junctions are listed in Table 5.4 [56,57]. Titanium/silicon carbide has the smallest barrier height. The measured barrier heights depend on the surface polarity of SiC (Si- and C-face) and often differ from the calculated values.

The Schottky barrier heights for selected metal/Si junction [58] are provided in Table 5.5. The maximum barrier heights of a Si device are significantly small compared with the minimum barrier heights of a SiC device. The difference between the barrier height of Ti/SiC and Ti/Si is larger than 0.56 V. Due to the high barrier height of a SiC device, the contribution of the barrier height to the forward voltage drop is higher, though the contribution from the specific on-resistance is lower. However, barrier height lowering will occur at high applied electric fields and result in a device design change for SiC diodes, just as in Si diodes, to PiN structures.

In Eq. (5.20), R_{SP_ON} is the total specific resistance. It is a sum of the ohmic contact resistance, R_{CONT}; the substrate resistance, R_{SUB}; and the drift region resistance, R_{Drift} [59]:

$$R_{SP_ON} = R_{CONT} + R_{SUB} + R_{Drift} \tag{5.22}$$

For silicon carbide devices, the substrate has higher resistance, and R_{SUB} must be included in the analysis. The new SiC devices are fabricated with a thin substrate for a lower forward voltage and improved thermal performance [54]; therefore, the resistance will be smaller. The ohmic contact resistance, R_{CONT}, is the resistance between the contact of the drift region and the cathode. It may also make a substantial contribution to the ON-state voltage drop. The drift region resistance, R_{Drift}, can be determined by the drift layer thickness and doping concentration, W_D and N_D, and the electron mobility, μ_n, according to the following equation:

$$R_{Drift} = \frac{W_D}{q\mu_n N_D} \tag{5.23}$$

The drift region resistance, R_{Drift}, can also be given as an expression in terms of the designed blocking voltage, V_B, and critical electric field, E_C:

$$R_{Drift} = \frac{4V_B^2}{2qE_C^3} \tag{5.24}$$

The drift region resistance increases quadratically with blocking voltage; therefore, the ON-state losses will increase significantly with an increase of the blocking voltage. Since conductivity modulation effects are not inherent to Schottky diodes, the drift region resistance will be significantly high for high-voltage diodes. In [60], a 3 kV 4H-SiC Schottky diode with a diameter of 1 mm and ON-resistance of 34 mΩ cm^{-2} (1.08 Ω) is reported, which is significantly high. For high blocking voltage, a PiN diode is preferred.

Another important parameter of a Schottky diode is the reverse leakage current. If the reverse leakage current is high when the reverse voltage is high, the power dissipated by it leads to an increase in the diode temperature. Since the reverse leakage current is sensitive to the junction temperature, increasing the limits of the power dissipation initiates a positive feedback for the temperature leading to permanent damage of the device [61]. Therefore, optimizing the diode parameters to obtain low leakage current is an important concern for a device designer.

Two mechanisms significantly contribute to the reverse leakage current operating at a high reverse voltage: the thermionic emission over the potential barrier and quantum mechanical tunneling of the carriers through a potential barrier. When reverse voltage, V_R, is applied, the leakage current due to the thermionic effect is

$$I_L = AA^*T^2 e^{-\frac{q\phi_B}{kT}}\left(e^{-\frac{qV_R}{kT}} - 1\right) \tag{5.25}$$

where A is the Schottky diode cross-sectional area and other parameters are as previously described. Increasing the reverse voltage higher than $3kT/q$ for moderately doped semiconductors decreases the Schottky barrier and causes the reverse leakage current to increase. Therefore, for a reverse voltage higher than $3kT/q$, the leakage current equation should include the barrier lowering $\Delta\phi_B$:

$$I_L = AA^*T^2 e^{-\frac{q\phi_B}{kT}} e^{-\frac{q\Delta\phi_B}{kT}}\left(e^{-\frac{qV_R}{kT}} - 1\right) \tag{5.26}$$

The barrier lowering depends on the maximum electric field, E_M, at the metal-semiconductor interface and the semiconductor relative permittivity [61]:

TABLE 5.4 Measured and calculated values of barrier heights for selected metal/4H-SiC junctions

Metals		Ti	Ni	Au
Measured	ϕ_B/q (Si-face), V	1.12	1.69	1.81
	ϕ_B/q (C-face), V	1.25	1.87	2.07
Calculated	ϕ_B/q, V	1.06	1.63	1.69

TABLE 5.5 Schottky barrier heights for selected metal/Si junctions

Metal	Mg	Ti	Cr	W	Mo	Pd	Au	Pt
ϕ_B/q, V	0.4	0.5	0.61	0.67	0.68	0.77	0.88	0.9

$$\Delta\phi_B = \sqrt{\frac{qE_M}{4\pi\varepsilon_r}} \tag{5.27}$$

For a one-dimensional Schottky junction, the maximum electric field, E_M, is related to the applied reverse bias voltage, V_R, by the following equation:

$$E_M = \sqrt{\frac{2qN_D}{\varepsilon_r}(V_R - V_{bi})} \tag{5.28}$$

Since the barrier lowering increases as the reverse bias voltage increases, the leakage current also increases. The second mechanism that contributes to the increase of the leaking current is the tunneling current. Since SiC has a wide bandgap and, therefore, a high critical electric field, the SiC Schottky diodes are designed to stand significantly higher electric fields on the metal-semiconductor interface compared with Si diodes. The SiC Schottky diodes can experience very high electric fields, higher than 2 MV cm^{-1}, which will contribute to a significant increase of the leakage current. A more rapid increase in leakage current observed in SiC Schottky diodes can be expressed with the thermionic emission model [59]:

$$I_L = A^*T^2 e^{-\frac{q\phi_B}{kT}} e^{-\frac{q\Delta\phi_B}{kT}} e^{C_T E_M^2}\left(e^{-\frac{qV_R}{kT}} - 1\right) \tag{5.29}$$

where C_T is a tunneling coefficient. Since the forward voltage drop of a SiC Schottky diode and the leakage current increase as the design breakdown voltage increases, PiN and merged PN-Schottky diodes should be used for applications using higher-voltage SiC.

5.3.2.2 SiC PiN Diode

The advantage of a SiC PiN diode is low specific resistance R_{SP_ON}, during high current conduction, due to high-level injection of minority carriers in the lightly doped drift region resulting in conductivity modulation. However, conductivity modulation causes significant reverse recovery current during switching, which is undesirable because it causes additional turn-ON loss in the active switch. At voltage ratings from 10 to 20 kV, 4H-SiC PiN diodes offer the best trade-off between ON-state voltage drop, switching losses, and high-temperature performance as compared with Si PiN and SiC Schottky/JBS diodes [62].

Different research groups have worked on designing, fabricating, and characterizing SiC PiN diodes, but the maturity of PiN diodes is not sufficient enough to be marketable. In 2001, a high-voltage PiN diode in SiC with a blocking voltage of over 19 kV was reported [63]. It has a forward voltage drop of 6.5 V at 100 A cm^{-2}. Also in 2002, the design, fabrication, and high-temperature characteristics of 4H-SiC PiN rectifiers with 5, 6, and 10 kV blocking voltage were reported [64]. For the 10 kV rectifier, a forward voltage drop of <4.8 V was observed at 100 A cm^{-2} in the entire 25–200°C temperature range. Also in [62], 12.9 kV SiC PiN diodes with ultralow ON-state voltage drop and differential ON-resistance of 3.75 V and 3.3 mΩ cm^{-2} at 100 A cm^{-2}, respectively, were reported. It has also been reported in the literature that Schottky and PiN SiC diodes have significantly less reverse current than the conventional fast or ultrafast Si diode [65].

SiC PiN diodes consist of a highly doped N-type substrate, a lightly doped N-type epitaxial layer, known as the drift region, and a highly doped P-type region for the anode, which is shown in Fig. 5.4. The most important parameter for a power SiC PiN diode is the voltage drop, V_{AK}, across it during the conduction state. It is composed of five components, including the voltages across the junctions, J_1 and J_2, the voltage across the two depletion regions, V_{d1} and V_{d2}, and the voltage across the drift region, V_{N^-}.

$$V_{AK} = V_{j1} + V_{j2} - V_{d1} - V_{d2} + V_{N^-} \tag{5.30}$$

Different models have been used to calculate the voltage drop across the diode and the current passing through it. A level-3 model for modeling a power diode using a Fourier-based solution for the ambipolar diffusion equation (ADE) of the lightly doped N^- drift region is given in [66]. In their model, the PiN diode is divided into three regions, and the basic equations governing the behavior of semiconductor devices are used to analyze the operation of the diode. The diode current, I_D, and the electron, hole, and displacement currents at junctions J_1 and J_2 (I_{n1}, I_{p1}, I_{disp1} and I_{n2}, I_{p2}, I_{disp2}) and their direction are shown in Fig. 5.4. The P^+ and N^+ emitters are assumed to be minority sinks.

Since the P^+ emitter region is highly doped, high-level injection exists during the ON-state, and therefore, there is a significant electron concentration adjacent to the P^+N^- junction. As a result of this high concentration, electrons flow into the P^+ emitter and recombine with the holes. The resulting electron current due to the emitter recombination is

$$I_{n1} = qAh_p p_{x1}^2 \tag{5.31}$$

where p_{x1} is the hole concentration at the junction, J_1. The recombination parameter, h_p, is calculated by the following equation:

$$h_P = \frac{1}{N_P}\sqrt{\frac{D_{n_P}}{\tau_{n_P}}} \tag{5.32}$$

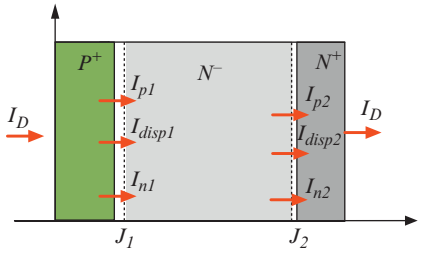


FIG. 5.4 Schematic structure of a $P^+N^-N^+$ power diode.

where N_P is the emitter doping concentration and D_{nP} and τ_{nP} are the electron diffusivities and lifetime. The current continuity at junction J_1 (Fig. 5.4) requires that

$$I_D = I_{n1} + I_{p1} + I_{dis1} \tag{5.33}$$

The junction voltage of junction J_1 is [32]

$$V_{j1} = V_T \ln\left(\frac{p_{x1} N_{N^-}}{n_i^2}\right) \tag{5.34}$$

where V_T is the thermal voltage (kT/q).

A high-power diode has a thick, lightly doped drift region for supporting high blocking voltage. A simple charge control modeling approach cannot be applied for the drift region, since the transient duration is comparable with or shorter than the transient time of the charge carriers. In this case, the charge dynamics in the drift region can be described by the continuity and the transport equations. To simplify the analysis, the charge profile in the thick, lightly doped drift region is assumed to be one-dimensional for more than 90% of its volume. Also, high-level injection in the drift region during most of the time of the transient and ON-state can be assumed. Under these assumptions and quasineutrality, the one-dimensional ADE describing the carrier dynamics in the majority of this region is given by the equation:

$$D_{N^-}\frac{\partial^2 p(x,t)}{\partial x^2} = \frac{p(x,t)}{\tau_{N^-}} + \frac{\partial p(x,t)}{\partial t} \tag{5.35}$$

where D_{N^-} is the ambipolar diffusion coefficient, τ_{N^-} is the high-level carrier lifetime within the drift region, and $p(x,t)$ is the excess carrier concentration. Different methods can be used to solve the ADE. In [66], Fourier analysis is used to solve the ADE. The basic idea of the Fourier-based solution is to separate excess carrier concentration $p(x,t)$into its space and time functions. According to Leturcq [67], the excess carrier concentration, $p(x,t)$, can be represented as a discrete cosine Fourier series:

$$p(x,t) = p_0(t) + \sum_{k=1}^{\infty} p_k(t)\cos\left[\frac{k\pi(x-x_1)}{x_2-x_1}\right] \tag{5.36}$$

where the Fourier series coefficients $p_k(t)$ are

$$\begin{aligned} p_0(t) &= \frac{1}{x_2-x_1}\int_{x_1}^{x_2} p(x,t)dx \\ p_k(t) &= \frac{2}{x_2-x_1}\int_{x_1}^{x_2} p(x,t)\cos\left(\frac{k\pi(x-x_1)}{x_2-x_1}\right)dx \end{aligned} \tag{5.37}$$

By substituting the carrier concentration in the Fourier series from Eq. (5.37) into the ADE, Eq. (5.35), the amplitude of the Fourier series $p_k(t)$ can be determined in a group of first-order differential equations. This requires employing the boundary conditions at the edges of the drift region. The required boundary conditions are the boundaries of the regions (x_1 and x_2), their differentials (dx_1/dt and dx_2/dt), and the carrier density gradients at x_1 and x_2 given by the equations:

$$\left.\frac{\partial p}{\partial x}\right|_{X_1} = \frac{1}{2qA}\left(\frac{I_n}{D_n} - \frac{I_p}{D_p}\right)\Bigg|_{X_1} \text{ and } \left.\frac{\partial p}{\partial x}\right|_{X_2} = \frac{1}{2Aq}\left(\frac{I_n}{D_n} - \frac{I_p}{D_p}\right)\Bigg|_{X_2} \tag{5.38}$$

where D_n and D_p are electron and hole diffusivities, I_n and I_p are electron and hole currents, and A is the active device area. The solution to the ADE is given by the following differential equations as each of them refers to a harmonic, p_k, of the carrier charge density, $p(x)$:

For $k > 0$

$$\begin{aligned} &D_{N^-}\left[\left.\frac{\partial p(x,t)}{\partial x}\right|_{x2}(-1)^k - \left.\frac{\partial p(x,t)}{\partial x}\right|_{x1}\right] \\ &= \frac{x_2-x_1}{2}\left(\frac{dp_k(t)}{dt} + \left[\frac{1}{\tau} + \frac{D_{N^-}k^2\pi^2}{(x_2-x_1)^2}\right]p_k(t)\right) \\ &+ \left(\sum_{\substack{n=1 \\ n\neq k}}^{\infty}\frac{n^2}{n^2-k^2}\left[\frac{dx_1}{dt} - (-1)^{n+k}\frac{dx_2}{dt}\right]p_n(t) + \frac{p_k(t)}{4}\left(\frac{dx_1}{dt} - \frac{dx_2}{dt}\right)\right) \end{aligned}$$

For $k = 0$,

$$\begin{aligned} D_{N^-}\left[\left.\frac{\partial p(x,t)}{\partial x}\right|_{x_2} - \left.\frac{\partial p(x,t)}{\partial x}\right|_{x_1}\right] &= (x_2-x_1)\left(\frac{dp_0(t)}{dt} + \frac{p_0(t)}{\tau}\right) \\ &+ \sum_{n=1}^{\infty}\left[\frac{dx_1}{dt} - (-1)^n\frac{dx_2}{dt}\right]p_n(t) \end{aligned} \tag{5.39}$$

At the boundary, x_1 and x_2, the carrier densities, p_{x1} and p_{x2}, are calculated using Eqs. (5.40), (5.41), respectively:

$$p_{x1} = \sum_{k=1}^{n}(-1)^k p_k \tag{5.40}$$

$$p_{x2} = \sum_{k=1}^{n} p_k \tag{5.41}$$

The current continuity equation at junction J_2 is

$$I_{n2} = I_D - I_{p2} - I_{disp2} \tag{5.42}$$

Assuming that

$$\frac{1}{D_n} + \frac{1}{D_p} = \frac{D_n + D_p}{D_n D_p} = \frac{2}{D_{N^-}} \text{ and } D\left(\frac{1}{D_n} - \frac{1}{D_p}\right) = \frac{D_n - D_p}{D_n + D_p} = D_{diff} \tag{5.43}$$

and using the current continuity equations at junctions J_1, Eq. (5.33), and J_2, Eq. (5.42), the left side of Eq. (5.39), for even and odd numbers of k, can be calculated by the following equations:

$$I_{even} = D\left(\left.\frac{\partial p}{\partial x}\right|_{x_2} - \left.\frac{\partial p}{\partial x}\right|_{x_1}\right) = \frac{1}{2qA}\begin{vmatrix} I_D \\ I_{p2} \\ I_{n1} \\ I_{disp1} \\ I_{disp2} \end{vmatrix}\begin{vmatrix} 2 & -2 & -2 & -\frac{D}{D_p} & -\frac{D}{D_n} \end{vmatrix}$$

$$I_{odd} = D\left(\left.\frac{\partial p}{\partial x}\right|_{x_2} - \left.\frac{\partial p}{\partial x}\right|_{x_1}\right) = \frac{1}{2qA}\begin{vmatrix} I_D \\ I_{p2} \\ I_{n1} \\ I_{disp1} \\ I_{disp2} \end{vmatrix}\begin{vmatrix} -2D_{diff} & 2 & 2 & -\frac{D}{D_p} & \frac{D}{D_n} \end{vmatrix} \tag{5.44}$$

The depletion layer voltages, V_{d1} and V_{d2}, across the P^+N^- and N^- N depletion layers are derived using a feedback from the boundary carrier densities, p_{x1} and p_{x2}:

$$V_{d1} = \begin{cases} 0 & \text{if } p_{x1} > 0, \\ -K_{FV}p_{x1} & \text{otherwise.} \end{cases}$$
$$V_{d2} = \begin{cases} 0 & \text{if } p_{x2} > 0, \\ -K_{FV}p_{x2} & \text{otherwise.} \end{cases} \tag{5.45}$$

The feedback constant, K_{FV}, is set to 10^{-12}, which gives good convergence and minimal error. The same value of K_{FV} is used to calculate the depletion layer voltages of a diode and an IGBT in [68].

The depletion widths, W_{d1} and W_{d2}, are

$$W_{d1} = \sqrt{\frac{2\varepsilon V_{d1}}{qN_{N^-} + \frac{|I_{p1}|}{Av_{sat}}}}$$
$$W_{d2} = \sqrt{\frac{2\varepsilon V_{d2}}{qN_{N^-} + \frac{|I_{n2}|}{Av_{sat}}}} \tag{5.46}$$

The boundary positions, x_1 and x_2, are

$$x_1 = W_{d1}$$
$$x_2 = W_{N^-} - W_{d2} \tag{5.47}$$

The displacement currents, I_{disp1} and I_{disp2}, at junctions J_1 and J_2 are

$$I_{disp1} = C_{J1}\frac{dV_{d1}}{dt} = \varepsilon A\frac{1}{W_{d1}}\frac{dV_{d1}}{dt}$$
$$I_{disp2} = C_{J2}\frac{dV_{d2}}{dt} = \varepsilon A\frac{1}{W_{d2}}\frac{dV_{d2}}{dt} \tag{5.48}$$

The voltage drop in the lightly doped drift region, V_{N^-}, can be calculated based on electron and hole currents passing through it. The current transport equations are

$$J_n = q\mu_n n\mathcal{E} + q\mu_n \nabla n \tag{5.49}$$

$$J_p = q\mu_n n\mathcal{E} - q\mu p\nabla p \tag{5.50}$$

Due to conductivity modulation, it can be assumed that the concentration of the electrons in the drift region is

$$n = p + N_{N^-} \tag{5.51}$$

Including the doping concentration, N_{N^-} is necessary, especially during the switching when the drift region has low conductivity due to the low-level injection.

Summing the current transport equations and including the Einstein relation ($D_p/\mu_p = kT/q$) and Eq. (5.51), the total current density is

$$J = qE\left(p\left(\mu_n + \mu_p\right) + \mu_n N_{N^-}\right) + qV_T\left(\mu_n - \mu_p\right)\frac{\partial p}{\partial x} \tag{5.52}$$

The electric field, $\mathcal{E}$, is

$$\mathcal{E} = \frac{J}{q\left(p\left(\mu_n + \mu_p\right) + \mu_n N_{N^-}\right)} - \frac{V_T\left(\mu_n - \mu_p\right)}{p\left(\mu_n + \mu_p\right) + \mu_n N_{N^-}}\frac{\partial p}{\partial x} \tag{5.53}$$

The drift region voltage drop is calculated by integrating the electric field between the two boundaries, x_1 and x_2:

$$V_{N^-} = \frac{J}{q}\int_{x_1}^{x_2}\frac{dx}{p\left(\mu_n + \mu_p\right) + \mu_n N_{N^-}} - \int_{p_{x1}}^{p_{x2}}\frac{V_T\left(\mu_n - \mu_p\right)}{p\left(\mu_n + \mu_p\right) + \mu_n N_{N^-}}\partial p \tag{5.54}$$

The voltage drop in the lightly doped drift region, V_{N^-}, is composed of two components: a resistive voltage drop due to the resistivity of the lightly doped drift region and voltage due to the diffusion across the drift region. The first integral of Eq. (5.54) cannot be solved analytically from the Fourier series relation because the carrier densities must be calculated for each point along the drift region and then substituted in Eq. (5.54). Instead, the drift region is divided into segments of equal width. It is desirable that the number of segments, M, be equal to the number of the terms in the Fourier series used to calculate the carrier densities. The width of a segment is calculated by the equation:

$$\Delta x = \frac{x_2 - x_1}{M - 1} \tag{5.55}$$

The carrier distribution in every point is calculated by the inverse Fourier transformation. The carrier distribution between two points is assumed to be a linear approximation (Fig. 5.5):

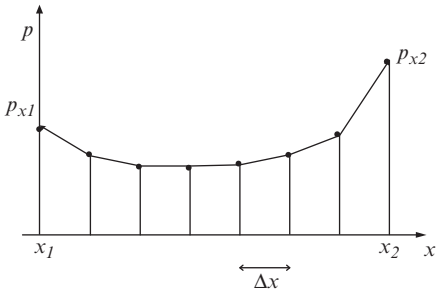


FIG. 5.5 The carrier distribution in the drift region during the ON-state.

$$p_T = p_{T1} + (p_{T2} - p_{T1})\frac{x}{\Delta x} \tag{5.56}$$

The resistive voltage drop for every segment, V_{seg}, is calculated by

$$V_{seg} = \frac{J}{q\left(\mu_n + \mu_p\right)} \int_0^{\Delta x} \frac{dx}{p_T} = \frac{J}{q\left(\mu_n + \mu_p\right)} \frac{\Delta x}{p_{T2} - p_{T1}} \ln\left(\frac{p_{T2}}{p_{T1}}\right) \tag{5.57}$$

For $p_{T1} = p_{T2} = p_T$, Eq. (5.57) is not defined. Using L'Hôpital's rule for this case, the voltage drop of the segment is

$$V_{seg} = \frac{J}{q\left(\mu_n + \mu_p\right)} \frac{\Delta x}{p_T} \tag{5.58}$$

These two cases for calculating V_{seg} are generalized in [68] as follows:

$$V_{seg} = \begin{cases} \dfrac{J}{q\left(\mu_n + \mu_p\right)} \dfrac{\Delta x}{p_{T2} - p_{T1}} \ln\left(\dfrac{p_{T2}}{p_{T1}}\right) & \text{if } |p_{T2} - p_{T1}| \\ & \geq 0.00005(p_{T2} - p_{T1}), \\ \dfrac{J}{q\left(\mu_n + \mu_p\right)} \dfrac{\Delta x}{p_T} & \text{otherwise.} \end{cases} \tag{5.59}$$

and the voltage drop, V_{N^-}, of the silicon rectifier is

$$V_{N^-} \approx \frac{I}{qA\left(\mu_n + \mu_p\right)} \frac{x_2 - x_1}{M-1} \sum_{k=0}^{M-1} \left[\frac{1}{p_{T(k)} - p_{T(k-1)}} \ln\left(\frac{p_{T(k)}}{p_{T(k-1)}}\right)\right] - V_T\left(\frac{\mu_n - \mu_p}{\mu_n + \mu_p}\right) \ln\left(\frac{p_{x2}}{p_{x1}}\right) \tag{5.60}$$

where I is the current passing through the drift region, A is its cross-sectional area, and M is the number of terms of the Fourier series, and the carrier distribution, $p_{T(k)}$, is calculated by

$$p_{T(k)} = p\left(x_1 + \frac{k(x_2 - x_1)}{M-1}\right) + \frac{\mu_n N_B}{\mu_n + \mu_p} \tag{5.61}$$

The N^+ emitter region, shown in Fig. 5.4, has a high doping concentration, and therefore, there is a significant hole concentration adjacent to the N^- N^+ junction. Due to the high-level injection during the ON-state, electrons from the N^+ region are injected into the lightly doped drift region, and high concentration holes flow into the highly doped N^+ emitter region. The holes recombine with the electrons, and the resulting hole current due to the emitter recombination is

$$I_{p2} = qAh_n p_{x2}^2 \tag{5.62}$$

The recombination parameter, h_n, depends on the emitter doping levels, N_{N^+}; the minority carrier diffusivities, $D_{p_{N^+}}$; and the holes' lifetime, $\tau_{p_{N^+}}$ [69]; and it is calculated by the equation:

$$h_n = \frac{1}{N_{N^+}} \sqrt{\frac{D_{p_{N^+}}}{\tau_{p_{N^+}}}} \tag{5.63}$$

The junction voltage, V_{J2}, is [32]

$$V_{j2} = V_T \ln\left(\frac{p_{x2}}{N_{N^-}}\right) \tag{5.64}$$

Summing the two junction voltages from Eqs. (5.34), (5.64), the total junction voltage, $V_{j12,}$ is

$$V_{j12} = V_T \ln\frac{p_{x1}p_{x2}}{n_i^2} = V_T \ln p_{x1}p_{x2} - 2V_T \ln(n_i) \tag{5.65}$$

The total junction voltage, V_{j12}, does not directly depend on the doping concentration of the lightly doped drift region, N_{N^-}. However, there is a dependency between the boundary values of the excess charge concentrations, p_{x1} and p_{x2}, and the impurity doping level that then determines junction voltage values. To obtain the minimum forward voltage drop during conduction, V_F, the minimum width of the drift region, corresponding to the minimum doping concentration, should be used. However, the results from the simulation given in [70] do not agree with this simple assertion from Eq. (5.65). The simulation results show that increasing the doping concentration, N_{N^-}, for the same breakdown voltage leads to a decrease of V_{AK} to a minimum value, after which further increases in the doping concentration cause an increase in the forward voltage drop. Higher doping concentrations, N_{N^-}, lead to reduced injection efficiencies of the higher doped P^+ and N^+ emitters into the drift region and, therefore, decrease the values of the carrier densities, p_{x1} and p_{x2}, at the region boundaries. It can be seen, from Eq. (5.65), that as the boundary charge concentrations are reduced, the contribution of the junction voltages to the total forward drop tend to cause a reduction in V_{AK}. Also, the total junction voltage, V_{j12}, depends on the intrinsic carrier concentration. Since the intrinsic carrier concentration of Si is $\sim 10^{10}$ cm^{-3}, the second member of Eq. (5.65) is $2V_T \ln(n_i) \approx 20V_T \ln(10)$ and will be subtracted to calculate the total junction voltage of a Si diode. The intrinsic carrier concentration of

SiC is $\sim 10^{-10}$ cm^{-3}, and the second member of Eq. (5.65) is $2V_T \ln(n_i) \approx -20V_T \ln(10)$ and will be added to calculate the total junction voltage of a SiC diode. For the same carrier densities, p_{x1} and p_{x2}, the total junction voltage of SiC will be approximately 2.38 V due to a lower intrinsic carrier concentration as compared with Si, which explains the experimental results of the IV characteristics of Si and SiC diodes. The forward voltage drop for a high-voltage Si diode is no more than 1.5 V, while for a SiC diode, the voltage drop is higher than 3 V. In [71], it is shown that for low-voltage devices (<6.5 kV), the forward voltage drop will be smaller for Si, as compared with SiC devices, while for high-voltage devices, the opposite is true.

Since for the same blocking voltage, the lightly doped drift region of a SiC diode is thinner than the lightly doped drift region of a Si diode, the stored charge will be smaller, the reverse recovery current will be smaller, and consequently, the switching losses will be smaller. Therefore, the power application designer should carefully calculate the losses and choose the best diode for the application.

5.3.2.3 SiC Junction Barrier Schottky Diode

As mentioned above, a SiC PiN diode has a large forward voltage drop (about 3 V) due to the wide bandgap energy. For low- and medium-voltage applications, 600–6000 V, the forward drop becomes a significant part of ON-state losses in SiC PiN diodes. On the other hand, when using a Si Schottky diode as a rectifier, the forward voltage drop is in the range of 1–1.5 V. Reverse leakage current depends on the blocking voltage, and for the same blocking voltage, the leakage current is significantly higher than that of a SiC PiN diode.

The JBS diode combines the benefits of the Schottky and PiN diode. It was first demonstrated in silicon [72] as a Schottky structure with a P$^+$N junction grid integrated into its drift region. As of 2016, JBCs can be found on the market for 600, 1200, and 1700 V reverse-blocking ratings.

Schematic cross sections of a JBS structure are shown in Fig. 5.6. It combines Schottky and PiN diodes, as illustrated, with P$^+$-well embedded in the N- epilayer. During the forward conduction mode, JBS behaves as a Schottky diode. The current flows from the anode to cathode due to the majority carriers (electrons) flowing through the multiple conductive channels under the Schottky contact. In normal operation, the Schottky current dominates, and the analysis for the forward current can be based on thermionic emission theory for Schottky junctions.

The forward voltage drop in the function of current density is determined by the metal-semiconductor Schottky barrier height. The expression for the current density has to be modified to allow for the area taken up by the P$^+$ regions in the structure [32]:

$$V_{FS} = \frac{nkT}{q} \ln\left(\frac{J_F}{A^* T^2}\right) + \phi_B + R_{SP_ON} J_{FS} \tag{5.66}$$

where J_{FS} is the current density across the Schottky barrier calculated by the following equation:

$$J_{FS} = \frac{m+s}{2d} J_{FC} \tag{5.67}$$

where s is the diffusion width of the P^+ regions, m is the masked regions (spacing between P^+ regions), and $2d$ is the actual area of the Schottky diode. The simulation results given in [73] show that the smallest spacing between P$^+$ regions results in the lowest electric field and the lowest forward voltage drop. For calculating the ON-state resistance, R_{SP_ON}, of a JBS diode, it should be taken into account that the current will pass through a different area. The equation for the ON-state resistance, R_{SP_ON}, is based on current spreading from the top $2d$ to the bottom $(m+s)$ [32]:

$$R_{SP_ON} = \rho \frac{(x_j + W)(m+s)}{m+s-2d} \ln\left(\frac{m+s}{2d}\right) \tag{5.68}$$

In Eq. (5.68), ρ is the resistivity of the epilayer, x_j is the P^+ region thickness, and W is the depletion layer width:

$$W = \sqrt{\frac{2\varepsilon_r}{N_D}(V_{bi} - V_F)} \tag{5.69}$$

The reverse leakage current has two components: one that is due to the injection of carriers across the Schottky barrier and another that is due to space-charge generation and diffusion currents [32]. The first expression is derived by modifying Eq. (5.26) to allow for the area taken up by the P$^+$ regions in the structure:

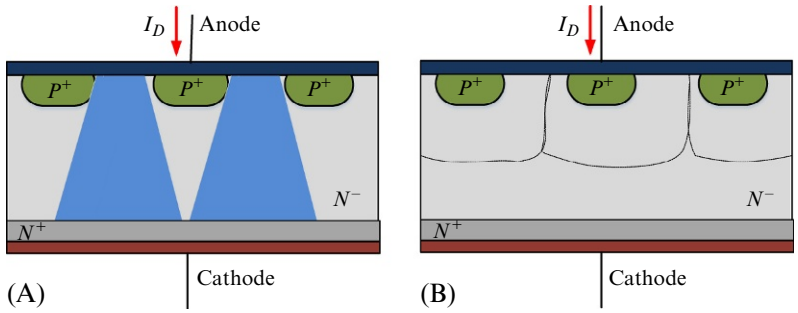


FIG. 5.6 Structure of a power JBS diode under (A) forward and (B) reverse bias.

$$I_{L_{SCH}} = \frac{2d}{m+s} A^* T^2 e^{-\frac{q\phi_B}{kT}} e^{-\frac{q\Delta\phi_B}{kT}} \left(e^{-\frac{qV_R}{kT}} - 1 \right) \tag{5.70}$$

The barrier lowering, $\Delta\phi_B$, is calculated by Eq. (5.27) where E_M is the electric field at the Schottky barrier. Applying negative voltage to a JBS causes its P^+N junctions to become reverse-biased, and the depletion layers spread into the channel. Increasing the negative voltage leads to pinch-off of the Schottky barrier and forms a potential barrier that limits the electric field at the Schottky contact, while the drift region supports further increase in voltage. The electric field is approximately constant once the channel potential barrier forms and pinch-off occurs. Further increases in reverse voltage are not reflected in the electric field; therefore, the electric field can be expressed by the pinch-off voltage, V_p:

$$E_M = \sqrt{\frac{2qN_D}{\varepsilon_r}(V_P + V_{bi})} \tag{5.71}$$

The size of the spacing between the P^+ regions should be optimized so that pinch-off is reached before the electric field at the Schottky contact increases to the point where excessive leakage currents occur due to tunneling currents and ON-resistance is not so big [73].

The second component of the leakage current is due to the P^+N junction:

$$I_{L_{P^+N}} = q\sqrt{\frac{D_p}{\tau_p}}\frac{n_i^2}{N_D} + q\frac{n_i W}{\tau_P} \tag{5.72}$$

where D_p and τ_p are hole diffusivity and lifetime in the N region with a width and doping concentration of W and N_D. Since the intrinsic carrier concentration of SiC (10^{-10}) is small compared with Si (10^{10} cm^{-3}), the leakage current of a SiC JBS due to the P^+N junction is significantly smaller and can be neglected. The presence of P^+ implanted regions improves the current surge capability and dv/dt and di/dt ratings for JBS diodes [73].

When a SiC JBS is designed to block high voltage, the N region is significantly thick and lightly doped; therefore, the forward voltage drop will be significantly large, especially for high current. The high-voltage JBS operates at two operation modes: JBS and MPS, depending on the forward-bias voltage level. When the bias voltage is not high enough to turn on the inherent PiN diode ($V_F < 3$ V), only the Schottky part is conducting. As the forward bias increases ($V_F > 3$ V), the minority carriers start to be injected into the N- layer from the P^+-well and modulate the conductivity of the epilayer resulting in a low resistance in series with the Schottky region. As a result, the ON-state current density in the high-voltage JBS during the MPS mode becomes ever larger than that for a PiN diode. The storage charge during the MPS mode is significantly smaller than that in the PiN diode, and therefore, the reverse recovery behavior of the high-voltage JBSs will be significantly superior to those for PiN diodes. The peak reverse current will be smaller, and therefore, the switching losses, and the stresses in the switch controlling the reverse recovery will be smaller.

If the high-voltage JBS is designed so that the space between the PN junctions within the cell is significantly small, a potential barrier under the Schottky region can be formed. The leakage current will be small since the lowering effect of the Schottky barrier will not be observed.

5.3.3 SiC MOSFET

For Si power MOSFETs (breakdown voltage higher than 200 V), the ON-resistance becomes dominated by the drift region resistance leading to an increase in the ON-state voltage drop and conducting losses. Novel Si structures have allowed the breakdown voltage to extend to 600 V, but the specific on-resistance is still reasonably large, which limits high-frequency operation. Theoretically, the much lower drift region resistance in SiC would allow development of power MOSFETs with higher breakdown voltages and smaller switching and conducting losses.

Since the introduction of the first SiC power double diffusion MOSFET (DMOSFET) in 1996 [74], different devices have been designed, characterized, and studied to improve their performance. Some SiC MOSFETs developed since that time are provided in Table 5.6. Since 1996, blocking voltages have increased from 0.76 to 14 kV. For a long period of time, the power MOSFET structures developed in Si could not be directly employed for SiC devices due to the following reasons.

The first is that in low-voltage devices, the ON-resistance is caused by the low mobility of inversion electrons at the SiO_2/4H-SiC interface. It was found, however, that the electric quality of the interface can be improved dramatically by postoxidation annealing in nitric oxide (NO) that leads to an increase in the inversion layer electron mobility and a corresponding reduction in channel resistivity [91]. Also, the introduction of a

TABLE 5.6 Parameters of SiC MOSFETs developed in the past few years

BV (kV)	R_{SP_ON} (mΩ cm^2)	Reference
0.76	66	[74]
0.95	220	[75]
0.95	8.7	[76]
1	6.95	[77]
1.1	74@100°C	[78]
1.3	7	[79]
1.4	313	[80]
1.6	27	[81]
1.8	8	[82]
2	10.3	[83]
2.6	200	[84]
3.06	121	[85]
3.36	199	[85]
10	236	[86]
10	133	[87]
10	123	[88]
10	111	[89]
14	228	[90]

self-aligned process reduces the channel resistance, and therefore, the specific ON-resistance of a well-fabricated power device is no longer limited by the channel resistance [92].

The second reason is that a high electric field in the insulator, silicon dioxide (SiO_2) of a silicon carbide MOSFET, can cause the device to fail during the blocking mode. The problem is aggravated at the trench corners leading to rupture of the gate oxide at higher drain voltages [93], thus restricting the maximum operating voltage. It can be prevented by using a buried P^+ layer to shield the channel region [94]. As a result, the electric field in the gate oxide is reduced, increasing the reliability of the SiC MOSFETs.

The third reason is that the injection of electrons into the oxide can take place when the electrons in the semiconductor gain sufficient energy to surmount the potential barrier between the SiC and SiO_2. This can cause shifting of the threshold voltage of the MOSFET leading to reliability problems.

Many companies have invested extensively in research and development of SiC MOSFETS, and most of the problems have been solved. Now, 1700 V devices can be found on the market [46]. At the ECCE 2011 Phoenix conference, Cree Inc. presented a new 12 kV SiC MOSFET ready for production.

A common structure for a SiC MOSFET is the double diffused or DMOSFET (Fig. 5.7), which has high switching speed and durability. It is a vertical device with a planar gate. The name is taken from the fabrication technique that involves double diffusion through the same opening: one for creating the P region and the other for the N source. DMOSFET has a very short channel length, L_{CH}, for achieving high transconductance and gain and also for high frequency response [95]. The current capability of a device can be improved by increasing the device aspect ratio L_{CH}/W_{CH}, where W_{CH} is the channel width. The voltage capability can be improved by decreasing the doping concentration or the thickness of the lightly doped drift region.

Applying a positive voltage to the gate higher than the threshold voltage, V_{th}, creates an inversion layer (channel) on the top of the P-base region connecting the source to the junction field-effect transistor (JFET) region. An accumulation layer under the gate oxide at the top of the JFET region is also formed, providing current that spreads from the channel into the JFET region. The electron current flows through the channel and then continues to the path with the smallest resistance, that is, through the accumulation layer. After leaving the accumulation layer, the current flows downward and sideways toward the drain electrode [95].

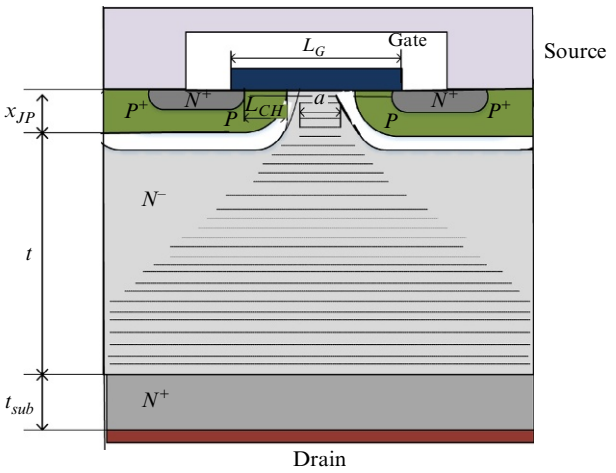


FIG. 5.7 Structure of a power DMOSFET.

For small values of the channel voltage, $V_{CH} < V_{CHsat}$, the DMOSFET has an approximately constant ON-state resistance with a value that is the sum of the channel and drift region resistance. The drain current, I_D, is

$$I_D = \frac{\mu_{CH} C_{OX} W_{CH}}{2L_{CH}} \left[2(V_{GS} - V_{th}) V_{CH} - V_{CH}^2\right] \tag{5.73}$$

where μ_{CH} is the inversion layer mobility (channel mobility), C_{OX} is the oxide capacitance per unit area, and V_{GS} is the gate-source voltage. The channel voltage, V_{CH}, is calculated by the equation:

$$V_{CH} = V_{DS} - I_D\left(R_{JFET} + R_{Drift}\right) \tag{5.74}$$

where R_{JFET} and R_{Drift} are JFET resistance and drift region resistances, respectively. The JFET resistance, R_{JFET}, is the resistance of the lightly doped N region that is under the accumulation layer formed under the gate electrode. The cross-sectional area of the JFET region through which the current flow increases slightly with distance, but for simplicity of analysis, a uniform cross section for the current flow can be assumed. If the JFET region is assumed to extend from the gate to the bottom of the P-base junction, x_{JP}, (P-region thickness), the resistance of the JFET region can be calculated by Eq. (5.75) [38]:

$$R_{JFET} = \frac{\rho_{JFET} x_{JP}}{Z\, a} \tag{5.75}$$

where Z is the length of the cell in the orthogonal direction to the cross section shown in Fig. 5.7, ρ_{JFET} is the resistivity of the JFET region depending on the doping concentration of the JFET region and calculated by

$$\rho_{JFET} = \frac{1}{q Z N_{JEFT}} \tag{5.76}$$

and a in Eq. (5.75) is the width of the channel flow. The width can be related to the device structural parameters gate width, W_G, and the width of the P-base L_{CH} by the equation:

$$a = W_G - 2L_{CH} - 2W_0 \tag{5.77}$$

where W_0 is the zero-bias depletion region width:

$$W_0 = \sqrt{\frac{2\varepsilon_{SiC} N_P V_{bi}}{q N_{JEFT}(N_{JEFT} + N_P)}} \tag{5.78}$$

Since $N_{JEFT} \ll N_P$, the equation for the zero-bias depletion region width can be simplified to

$$W_0 = \sqrt{\frac{2\varepsilon_{SiC} V_{bi}}{q N_{JEFT}}} \tag{5.79}$$

The built-in voltage depends on the doping concentration of both sides of the PN junction:

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_P N_{JFET}}{n_i^2}\right) \tag{5.80}$$

The intrinsic carrier concentration for SiC is significantly small compared with Si; therefore, the built-in voltage and drift region resistance will be larger. The parameter P-region thickness can be used to optimize the JFET region.

The drift region is under the JFET region. Since there is no depletion region to restrict the current in the drift region from spreading, it will spread, and therefore, the cross-sectional area will increase. If it is assumed that the cross-sectional width, X_D, for current flow increases by an angle of 45 degrees, and this width is smaller than the width of the cell, W_{Cell}; the drift region resistance can be calculated by the following equation:

$$R_{JFET} = \frac{\rho_{Drift}}{2Z} \ln\left(\frac{a+2t}{a}\right) \tag{5.81}$$

where ρ_{drift} is the resistivity of the drift region and t is the thickness of the drift region. For the same breakdown voltage, the drift region thickness of a Si device is big as compared with a SiC device. The SiC device can also be highly doped; therefore, the drift region resistance for a SiC device will be small as compared with the drift region of a Si device.

At high drain-source voltage, $V_{DS} > V_{DSsat} = V_{GS} - V_{th}$, the saturation of the current is observed. At least three mechanisms of current saturation in a DMOSFET occur: channel pinch-off, carrier saturation velocity in the high-electric-field regions, and the so-called parasitic JFET effect [96] that prevents the current from flowing uniformly in the JFET region. During saturation, the current is constrained to flow in a narrow JFET channel. The drain current can be calculated by the following equation:

$$I_D = \frac{\mu_{CH} C_{OX} W_{CH}}{2L_{CH}} V_{CHsat}^2 \tag{5.82}$$

where the channel resistance, R_{CH}, and the accumulation layer resistance, R_A, should be included in the calculation of the saturation voltage. The channel resistance depends on the inversion layer mobility, μ_{CH} and can be calculated by

$$R_{CH} = \frac{L_{CH}}{\mu_{CH} C_{OX}(V_{GS-} V_{th})} \tag{5.83}$$

The accumulation layer resistance, R_A, depends on the accumulation layer length, L_A, and the electron mobility in the accumulation layer, μ_A:

$$R_A = \frac{L_A}{\mu_A C_{OX}(V_{GS-} V_{th})} \tag{5.84}$$

The accumulation layer length, L_A, is

$$L_A = \frac{L_G}{2} - x_{JP} \tag{5.85}$$

where L_G is the gate length. For modeling the dynamic characteristics of a power SiC DMOSFET, the nonlinear gate-to-drain capacitance, C_{GD}, should be calculated as follows:

$$C_{GD} = \frac{C_{OX} C_{Dep}}{C_{OX} + C_{Dep}} \tag{5.86}$$

where C_{Dep} is the depletion region capacitance that is formed under the gate oxide.

$$C_{Dep} = \frac{\varepsilon_{SiC} Z(L_G - 2x_{JP})}{W_{Dep}} \tag{5.87}$$

where the depletion width, $W_{Dep,}$ depends on the drain bias, V_D, and can be calculated by the following equation:

$$W_{Dep} = \frac{\varepsilon_{SiC}}{C_{OX}} \left(\sqrt{1 + \frac{2V_D C_{OX}^2}{q\varepsilon_{SiC} N_{JFET}}} - 1\right) \tag{5.88}$$

From Eqs. (5.87), (5.88), the depletion capacitance, C_{Dep}, decreases as the drain bias voltage V_D, increases.

5.3.4 SiC JFET

The SiC JFET has some benefits, such as a resistive forward characteristic in the first and third quadrants and a monolithic integrated body diode. It is comparable with available SiC Schottky diodes in terms of stored charge, low output capacitance, low gate charge, and low switching losses that makes it attractive for use.

The first commercialized SiC transistor was normally the ON JFET from SemiSouth Laboratories and SiCED Electronics Development. They were easy to implement as there were no reliability issues with gate oxide as with SiC MOSFETs. The JFETs are only depletion-mode, normally ON-type devices that conduct current at zero gate voltage and are fully blocked when the gate voltage is below the pinch-off voltage. The most successful JFET type, in terms of voltage and current ratings, has been the lateral channel JFET (LCJFET), shown in Fig. 5.8 The LCJFET allows optimization of the channel parameters and is easy to fabricate. Due to the combined lateral-vertical channel design, the LCJFET has significantly reduced Miller capacitance. A parasitic diode formed with the buried P region and the N drift region can be used as a freewheeling diode without an external antiparallel diode. Also, the current through the channels can flow in the reverse direction when enough gate-source voltage is applied; therefore, the LCJFET can work in synchronous rectification circuits.

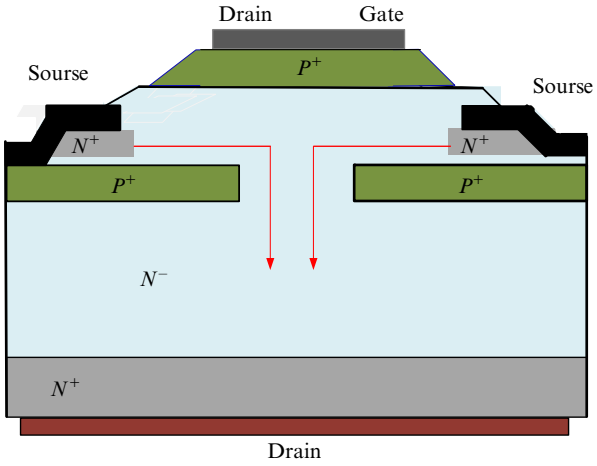


FIG. 5.8 Lateral channel SiC JFET.

When JFETs are ON, they exhibit constant resistance that can be minimized by increasing the gate voltage slightly higher than zero. A normally-ON device is not easy to use in a power application because losing the control can cause undesired conduction of the switch and, consequently, can lead to shoot-through current damaging the circuit [97].

A cascode configuration, shown in Fig. 5.9, composed of a SiC JFET and a series-connected low-voltage Si MOSFET, can overcome the problem and make a normally-ON JFET behave similarly to a conventional MOSFET. Typically, a 30 V MOSFET with very low ON-resistance controls the JFET conduction. When the two devices are conducting, the conduction losses of the MOSFET will be insignificant. When the Si MOSFET is turned on, the gate-source voltage of the JFET becomes zero, allowing current to pass from the drain to the source. The forward characteristics of a cascode configuration are determined by the gate-source voltage applied to the MOSFET.

During the OFF-state, the cascode exhibits a rugged avalanche behavior. Since in a cascode configuration the control device is a low-voltage Si MOSFET, it is easy to replace a power device with a cascode configuration packed as one device, because the control is made with the same voltage levels. The temperature coefficient of the ON-resistance of a SiC JFET is positive, which naturally protects the device from overshooting during high-temperature operation. However, there are some limitations with a cascode configuration. The maximum operating temperature in a cascode configuration is limited by the Si MOSFET, the Si MOSFET internal body diode shows a low dv/dt rating, limiting the switching frequency of the JFET, and the conduction losses are higher since the two devices are connected in series [98].

To overcome these limitations, gate drivers that can block a JFET have been designed. The driver output voltage swings from zero to negative voltage. The negative voltage level is less than the maximum pinch-off voltage of the device and, therefore, could cause a gate avalanche condition. In order to limit uncontrolled avalanche current, a parallel circuit, that includes a resistor, capacitor, and diode connected in series to the JFET gate, can be used. This parallel circuit is capable of limiting the avalanche current but supplying the high gate current peaks required for fast switching [99]. A disadvantage of using a special JFET driver is that a negative supply voltage should be provided to the drive circuit that complicates the control circuit of the device. Also, replacing a power device with a JFET in a power application is more complicated because the driver and the control are also affected.

In 2011, normally OFF vertical channel JFETs (VCJFETs) compatible with standard gate drive circuitry and featuring a positive temperature coefficient for ease in paralleling were commercially available. VCJFETs were based on a patented vertical channel trench structure from SemiSouth Laboratories, Inc. A typical high-voltage VCJFET is shown in Fig. 5.10.

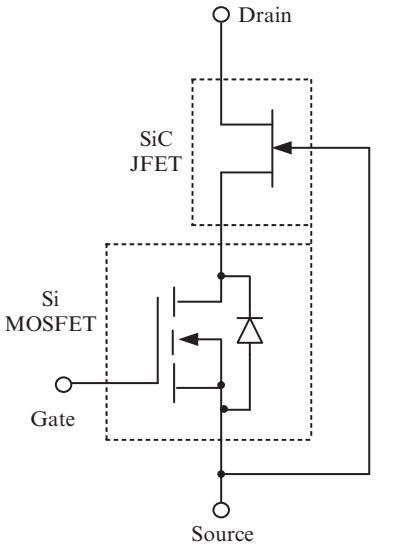


FIG. 5.9 SiC JFET/Si low-voltage MOSFET cascode configuration.

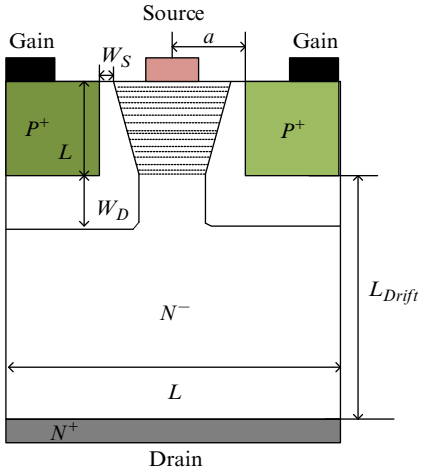


FIG. 5.10 SiC VCJFET cross section.

When the channel voltage is smaller ($V_{CH} < V_{CHsat}$), a VCJFET works in the linear region and has an approximately constant ON-state resistance; the value of which is the sum of the channel and drift region resistance. The drain current, I_D, can be calculated by the following equation [100]:

$$I_D = I_P \left[\frac{3V_{CH}}{V_P} - \frac{2}{V_P^{3/2}} \left[(V_{CH} - V_{GS} + V_{bi})^{3/2} - (V_{bi} - V_{GS})^{3/2} \right] \right] \tag{5.89}$$

where I_P is the pinch-off current depending on the channel parameters, such as electron mobility, μ_n; doping concentration, N_{CH}; VCJFET thickness, Z; half of the width of the channel region, a; and the effective length of the channel. The pinch-off current is calculated by the following equation:

$$I_P = \frac{q^2 \mu_n N_{CH}^2 Z a^3}{3\varepsilon_{SiC} L_{eff}} \tag{5.90}$$

Since the drift region of a high-voltage SiC VCJFET is designed to support high voltage, the drift region is thick and lightly doped. Hence, the drift resistance will be significantly higher than other resistance through which the drain current is flowing. Therefore, the drift resistance should be included for calculating the channel voltage, V_{CH}:

$$V_{CH} = V_{DS} - I_D R_{Drift} \tag{5.91}$$

where R_{Drift} is the drift resistance. To simplify the expression for calculating the drift resistance, the current spreading effect of the current coming from the channel can be neglected; then, the drift resistance can be calculated as the resistance of the rectangular area in the drift region under the channel:

$$R_{Drift} = \frac{L_{Drift} - W_D}{q\mu_n N_{Drift} Z W_{Drift}} \tag{5.92}$$

where L_{Drift} and W_{Drift} are the drift region thickness and the width and N_{Drift} is the doping concentration of the lightly doped drift region.

The pinch-off voltage depends on the channel parameters and can be calculated by the equation:

$$V_P = \frac{qN_{CH}a^2}{2\varepsilon_{SiC}} \tag{5.93}$$

The built-in voltage is

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_{CH}N_P}{n_i^2}\right) \tag{5.94}$$

where N_P is the doping concentration of the gate.

When the channel voltage is increased so that $V_{CH} > V_{CHsat}$, the drain current saturates. The saturation current is defined by the following equation:

$$V_{CHsat} = V_P - V_{GS} + V_{bi} \tag{5.95}$$

There are two reasons for the drain current to saturate. One reason is that the depletion region becomes progressively wider toward the drain side causing a reduction of channel width and an increase of channel resistance. The other reason is that due to the presence of a high electric field in the channel, the carrier velocity saturates. The saturated drain current, I_{DSAT}, can be calculated by the equation [100]:

$$I_{DSAT} = I_P \left[1 - 3\frac{V_{bi} - V_{GS}}{V_P} + 2\left(\frac{V_{bi} - V_{GS}}{V_P}\right)^{3/2} [1 + \lambda(V_{CH} - V_{CHSAT})] \right] \tag{5.96}$$

The multiplication term $[1 + \lambda(V_{CH} - V_{CHSAT})]$ in Eq. (5.96) is used to account for the channel modulation effect.

A benefit of a VCJFET is that it can be used in directions, forward and reverse, in a converter circuit. The reverse I–V characteristics do not saturate as do the forward I–V characteristics. The reason for this is that when the drain current is in the reverse direction, $V_{GD} > V_{GS}$, the channel closes so the drain side will be wide open. As a result, as V_{SD} increases, the channel is never pinched off when $V_{GS} > V_{th}$, while when $V_{GS} < V_{th}$, the channel is always pinched off on the side of the source and wide open on the drain side. Therefore, it is possible for a VCJFET to be used for freewheeling, although no parasitic diode is formed between the source and the drain [101].

In order to model the switching losses of a VCJFET, the capacitance between gate and source, C_{GS}, and the capacitance between gate and drain, C_{GD}, should be known. The gate-source capacitance is

$$C_{GS} = \frac{K_{GS}\varepsilon_{SiC}A_{GS}}{W_S} \tag{5.97}$$

where K_{GS} is the coupling area, the coefficient of the gate and source; A_{GS} is the coupling area between gate and source; and W_S is the depletion width between the gate and source. The depletion width can be calculated by

$$W_S = \sqrt{\frac{2\varepsilon_{SiC}}{qN_{CH}}}(V_{bi} - V_{GS}) \tag{5.98}$$

The gate-to-drain capacitance is

$$C_{GD} = \frac{\varepsilon_{SiC}A_{GD}}{W_D} \tag{5.99}$$

where the width of the depletion region between the gate and the drain is

$$W_D = \sqrt{\frac{2\varepsilon_{SiC}}{qN_{CH}}}(V_{CH} + V_{bi} - V_{GS}) \tag{5.100}$$

TABLE 5.7 Parameters and FOMs for 1200 V SiC devices

Type	Part number	Company	I_D (A)	R_{SP-ON} (mΩ)	Q_{SW} (nC)	Q_G (nC)	SLFOM	CLFOM
JFET	IJW120R100T1 [102]	Infineon	26	100	48	72	4800	7200
MOSFET	SCT3017AL [103]	Cree	40	52	65	115	3380	5980

Some of the parameters of SiC JFETs and MOSFETs are presented in Table 5.7 as their switching losses FOM (SLFOM) and conduction losses FOM (CLFOM). The MOSFET FOMs are smaller although the MOSFET current is higher. In 2009, it was stated that a SiC MOSFET would be the device of choice as soon as the SiO_2/SiC interface and reliability issues were resolved [104]. The two companies that were producing JFETs no longer exist. Infineon Technologies discontinued their JFET products. Other SiC companies are more interested in production and development of SiC MOSFETs; therefore, the future of the SiC JFET is still unknown.

5.3.5 SiC BJT

Power BJTs in SiC are very attractive for power switching applications due to their very low specific ON-resistance and high-temperature operation with high power densities [105]. The common-emitter gain, β; the specific on-resistance, R_{SP_ON}; and the open-base breakdown voltage, BV_{CEO}, are important parameters that should be accounted for in choosing a device for a power application. The current gain should be high enough to reduce the base current that controls the BJT. Considerable work has been done to improve device performance. One of the main challenges is to increase the current gain of 4H-SiC BJTs [106] that is limited by the surface recombination [105]. Reducing the surface recombination current by optimizing the surface passivation improves the current gain [107]. Also, the common-emitter current gain can be improved by increasing the minority carrier lifetime in the base and emitter regions [108]. The maximum current gain for high-voltage SiC BJTs that has been reported in the literature is 335 for a 600 V device [109].

To increase the blocking voltage, the growth of high-purity SiC homoepitaxial thin films on SiC single-crystal wafers is required to form N^-N^+ wafer structures [110]. The maximum open-base breakdown voltage, BV_{CEO}, for a SiC BJT was reported to be 6 kV, but the gain was only 3 [111]. Further work is necessary to improve the design and to develop a new processing technology so that an increase in BV_{CEO} can be achieved without sacrificing the current gain of the transistor. Also, the conduction and switching power losses should be minimized. The conduction losses depend on the collector-emitter voltage and the collector current.

The voltage drop, V_{CE}, across the high-power SiC BJT is composed of six components, including the voltages across the junctions, J_0, J_1, and pseudojunction, J_2; the voltage across the two depletion regions, V_{d1} and V_{d2}; and the voltage across the carrier storage region (CSR), V_{N^-}:

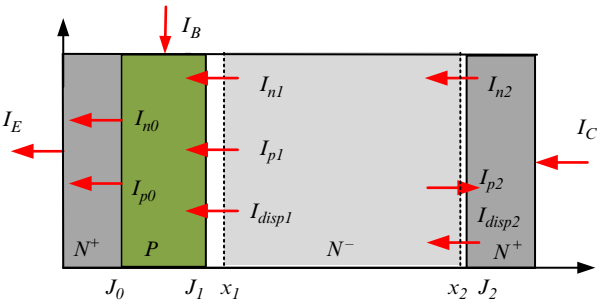


FIG. 5.11 One-dimensional cross section of a power BJT showing the hole and electron currents in each region.

$$V_{CE} = V_{j0} + V_{j1} + V_{j2} - V_{d1} - V_{d2} + V_{N^-} \tag{5.101}$$

A basic one-dimensional structure of a power BJT is illustrated in Fig. 5.11. The BJT is divided into four regions: N^+ emitter, P base, N^- drift, and N^+ collector. The external (emitter base and collector currents, I_E, I_B, and I_C) and internal electron and hole and displacement currents (at junctions J_0—I_{n0}, I_{p0}; J_1—I_{n1}, I_p, and I_{disp1}; and J_2—I_{n2}, I_{p2}, and I_{disp2}) are indicated for each region.

The N^+ emitter layer of a power BJT can be simply characterized as a hole sink. The hole current at the junction, J_0, is obtained by the following equation:

$$I_{p0} = qAh_n n_{B0} P_B \tag{5.102}$$

where n_{B0} is the electron concentration at junction J_0 and P_B is the base doping concentration. The N^+ emitter recombination parameter, h_n, depends on emitter properties, such as doping level (N_E), hole diffusivity (D_p), and hole minority lifetime (τ_p). The electron current component at junction J_0 is determined by

$$I_{n0} = I_C - I_{p0} \tag{5.103}$$

and the voltage drop across junction J_0 is

$$V_{j0} = V_T \ln\left(\frac{n_{B0}(n_{B0} + P_B)}{n_i^2}\right) \tag{5.104}$$

The equation for the P-base region can be used to derive the boundary current at junction J_1. The lumped-charge method is used to model the behavior in the base region due to its moderate doping level and comparatively narrow base width. The injected carrier distribution in the base region during conduction is shown in Fig. 5.12.

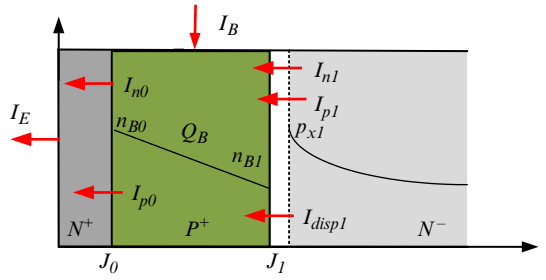


FIG. 5.12 Charge distribution and boundary current components in P base.

Using the continuity equation for the base region, the injected minority carrier charge is described by the relation:

$$\frac{dQ_B}{dt}+\frac{Q_B}{\tau_{BHL}}=I_{n0}-I_{n1}=I_B+I_{p1}+I_{disp1}-I_{p0} \tag{5.105}$$

where τ_{BHL} is the high-level lifetime in the P-base region.

The total electron charge in the base is expressed as

$$Q_B=\frac{n_{B0}+n_{B1}}{2}qAW_B \tag{5.106}$$

where W_B is the base width. The electron concentration at the base region boundary on the collector side, n_{B1}, is related to the excess carrier concentration, p_{x1}, by the doping concentration of the base, P_B, by the equation:

$$n_{B1}=\frac{p_{x1}^2}{P_B} \tag{5.107}$$

Since the diffusion length in the base region is much greater than the base width, the gradient of the electron concentration is approximately linear, giving the electron current at the base-collector junction, J_1, as

$$I_{n1}=qD_nA\frac{n_{B0}-n_{B1}}{W_B} \tag{5.108}$$

The base-emitter voltage V_{BE} is calculated by the equation:

$$V_{BE}=V_T\ln\left(\frac{n_{B0}P_B}{n_i^2}+1\right) \tag{5.109}$$

The voltage drop in N^- drift region is calculated during the ON-state in a manner similar to that of a PiN diode. The injected excess carrier concentration is determined by the ADE. As for all power switches, high-level injection and quasi-neutral conditions exist. Under high-level injection conditions, the ADE for the lightly doped drift describes the carrier dynamics of the majority carriers:

$$D\frac{\partial^2p(x,t)}{\partial x^2}=\frac{p(x,t)}{\tau}+\frac{\partial p(x,t)}{\partial t} \tag{5.110}$$

where D is the ambipolar diffusion coefficient, τ is the high-level carrier lifetime within the drift region, and $p(x, t)$ is the excess carrier concentration. The Fourier series solution of the ADE is given by the following first-order differential equations as each of them refers to a harmonic, $p_k(t)$, of the total minority carrier density, $p(x,t)$:

For $k>0$

$$\begin{aligned}&D\left[\left.\frac{\partial p(x,t)}{\partial x}\right|_{x_2}(-1)^k-\left.\frac{\partial p(x,t)}{\partial x}\right|_{x_1}\right]\\&=\frac{x_2-x_1}{2}\left(\frac{dp_k(t)}{dt}+\left[\frac{1}{\tau}+\frac{Dk^2\pi^2}{(x_2-x_1)^2}\right]p_k(t)\right)\\&+\left(\sum_{\substack{n=1\\n\neq k}}^{\infty}\frac{n^2}{n^2-k^2}\left[\frac{dx_1}{dt}-(-1)^{n+k}\frac{dx_2}{dt}\right]p_n(t)+\frac{p_k}{4}\left(\frac{dx_1}{dt}-\frac{dx_2}{dt}\right)\right)\end{aligned} \tag{5.111}$$

for $k=0$

$$\begin{aligned}D\left[\left.\frac{\partial p(x,t)}{\partial x}\right|_{x_2}-\left.\frac{\partial p(x,t)}{\partial x}\right|_{x_1}\right]&=(x_2-x_1)\frac{dp_0(t)}{dt}+\frac{p_0(t)}{\tau}\\&+\sum_{n=1}^{\infty}\left[\frac{dx_1}{dt}-(-1)^n\frac{dx_2}{dt}\right]p_n(t)\end{aligned}$$

The solution to the ADE is determined by using the boundary conditions at the edges of the charge storage region. The representation requires the width of the undepleted region and the hole and electron currents at the boundaries of the drift region, which give the gradients of the carrier concentrations at x_1 and x_2, respectively. For the given direction of the currents (Fig. 5.13), the required boundary conditions are given by the equations:

$$\left.\frac{\partial p}{\partial x}\right|_{x_1}=\frac{1}{2q}\left(\frac{J_n}{D_n}+\frac{J_p}{D_p}\right)\Bigg|_{x_1}\text{ and }\left.\frac{\partial p}{\partial x}\right|_{x_2}=\frac{1}{2q}\left(\frac{J_n}{D_n}+\frac{J_p}{D_p}\right)\Bigg|_{x_2} \tag{5.112}$$

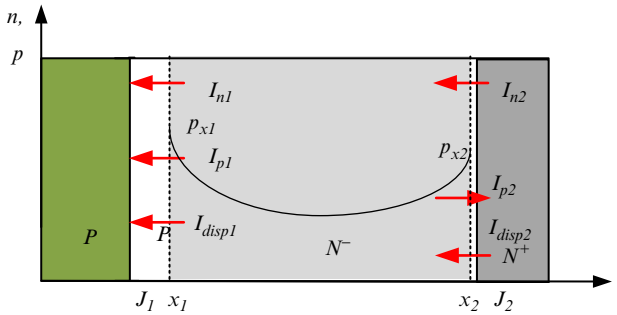


FIG. 5.13 Charge distribution and boundary current components in N^- collector.

Using the boundary condition Equation (5.112), the left side of Eq. (5.111), for even and odd numbers of k, can be calculated by the following equations:

$$I_{even} = D\left(\left.\frac{\partial p}{\partial x}\right|_{x_2} - \left.\frac{\partial p}{\partial x}\right|_{x_1}\right) = \frac{1}{2qA}\begin{vmatrix} I_{n1} \\ I_{p1} \\ I_{n2} \\ I_{p2} \end{vmatrix}\begin{vmatrix} -\frac{D}{D_n} - \frac{D}{D_p} + \frac{D}{D_n} + \frac{D}{D_p} \end{vmatrix} \tag{5.113}$$

$$I_{odd} = D\left(\left.\frac{\partial p}{\partial x}\right|_{x_2} - \left.\frac{\partial p}{\partial x}\right|_{x_1}\right) = -\frac{1}{2qA}\begin{vmatrix} I_{n1} \\ I_{p1} \\ I_{n2} \\ I_{p2} \end{vmatrix}\begin{vmatrix} \frac{D}{D_n} & \frac{D}{D_p} & \frac{D}{D_n} & \frac{D}{D_p} \end{vmatrix} \tag{5.114}$$

The boundary carrier densities, p_{x1} and p_{x2}, at the boundaries, x_1 and x_2, are calculated using the equations:

$$p_{x_1} = \sum_{k=1}^{n} p_k \text{ and } p_{x_2} = \sum_{k=1}^{n} (-1)^k p_k \tag{5.115}$$

The voltages across the N^-N^+ and N^-P^+ depletion layers, V_{d1} and V_{d2}, are calculated by the following equations:

$$\begin{aligned} V_{d1} &= \begin{cases} 0 & \text{if } p_{x1} > 0, \\ -K_{FV} p_{x1} & \text{otherwise.} \end{cases} \\ V_{d2} &= \begin{cases} 0 & \text{if } p_{x1} > 0, \\ -K_{FV} p_{x2} & \text{otherwise.} \end{cases} \end{aligned} \tag{5.116}$$

The feedback constant, K_{FV}, is set to 10^{-12}, which gives good convergence and minimal error [68]. The associated depletion widths, W_{d1} and W_{d2}, are calculated using a step doping concentration change on each side of the junction:

$$\begin{aligned} W_{d1} &= \sqrt{\frac{2\varepsilon V_{d1}}{qN_{N^-} + \frac{|I_c|}{A v_{sat}}}} \\ W_{d2} &= \sqrt{\frac{2\varepsilon V_{d2}}{qN_{N^-} + \frac{|I_c|}{A v_{sat}}}} \end{aligned} \tag{5.117}$$

The boundary positions, x_1 and x_2, are calculated by

$$\begin{aligned} x_1 &= W_{d1} \\ x_2 &= W_{N^-} - W_{d2} \end{aligned} \tag{5.118}$$

The displacement currents, I_{disp1} and I_{disp2}, are due to the changing depletion widths at junctions J_1 and J_2:

$$\begin{aligned} I_{disp1} &= C_{J1}\frac{dV_{d1}}{dt} = \varepsilon A \frac{1}{W_{d1}}\frac{dV_{d1}}{dt} \\ I_{disp2} &= C_{J2}\frac{dV_{d2}}{dt} = \varepsilon A \frac{1}{W_{d2}}\frac{dV_{d2}}{dt} \end{aligned} \tag{5.119}$$

The voltages across junctions J_1 and J_2 are

$$\begin{aligned} V_{j1} &= 2V_T \ln\left(\frac{p_1}{n_i}\right) \\ V_{j2} &= V_T \ln\left(\frac{p_{x2}}{N_C}\right) \end{aligned} \tag{5.120}$$

The voltage drop across the carrier storage region, V_{N^-}, is calculated based on the injected carrier concentration discussed in Section 5.3.2.2.

$$\begin{aligned} V_{N^-} \approx & \frac{I_C}{qA\left(\mu_n + \mu_p\right)} \frac{x_2 - x_1}{M-1} \sum_{\kappa=0}^{M-1} \left[\frac{1}{p_{T(k)} - p_{T(k-1)}} \ln\left(\frac{p_{T(k)}}{p_{T(k-1)}}\right)\right] \\ & + V_T \left(\frac{\mu_n - \mu_p}{\mu_n + \mu_p}\right) \ln\left(\frac{p_{x2}}{p_{x1}}\right) \end{aligned} \tag{5.121}$$

where the carrier distribution, $p_{T(k)}$, is calculated as

$$p_{T(k)} = p\left(x_1 + \frac{k(x_2 - x_1)}{M-1}\right) + \frac{\mu_n N_{N^-}}{\mu_n + \mu_p} \tag{5.122}$$

The N^+ collector region has similar properties to the N^+ emitter region as it also can be presented as a hole sink. The hole current at junction J_2 is obtained by the equation:

$$I_{p2} = qAh_n p_{x2}^2 \tag{5.123}$$

The electron current at junction J_2 is

$$I_{n2} = I_c + I_{p2} - I_{disp2} \tag{5.124}$$

During the ON-state, the voltages across the N^-N^+ and N^-P^+ depletion layers, V_{d1} and V_{d2}, are equal to zero, and the collector-emitter voltage is

$$V_{CE} = V_{j0} + V_{j1} + V_{j2} + V_{N^-} \tag{5.125}$$

Substituting the junctions' voltages from Eqs. (5.104), (5.120) in Eq. (5.125) and simplifying, the following equation will be obtained:

$$V_{CE} = V_T \ln\left(n_{B0}(n_{B0} + P_B)p_{x1}^2 \frac{p_{x2}}{N_C}\right) + 4V_T \ln\left(\frac{1}{n_i}\right) + V_{N^-} \tag{5.126}$$

Since the thickness of the lightly doped drift region of a SiC BJT is smaller than the lightly doped drift region of a Si device, their boundary carrier densities, p_{x1} and p_{x2}, at the boundaries, x_1 and x_2, are bigger [71]. Therefore, for the same doping concentration of the four regions of a power SiC BJT and a power Si BJT, the first term of Eq. (5.126) for a SiC device is big compared with a Si one. Also, if it is assumed that the intrinsic carrier concentrations of Si and SiC are 10^{10} and 10^{-10} cm^{-3} and

the thermal voltage, $V_T = 0.256$, the second term of a Si device is a negative number (approximately −2.36 V) that will subtract from the first term and make collector-emitter voltage smaller, while for a SiC BJT, the second term is a positive number (∼2.36 V) that will add to the first term and make the collector-emitter voltage bigger. Only the voltage drop in the lightly doped drift region for SiC will be small compared with a Si one, since the thickness in Si is significantly larger and the doping concentration in Si is lower. To have benefits of conductivity modulation and therefore small ON-resistance, SiC BJTs similar to SiC PiN diode should be designed for higher than 4 kV [112]. Also, the BJT is a bipolar device having minority and majority carrier flowing during operation; therefore, the drift region stores charge that decreases the device switching speed and thus can only operate at switching frequencies less than can be obtained with a MOSFET structure.

5.3.6 SiC IGBT

As previously mentioned, the rapid improvement in 4H-SiC material quality and the maturing of SiC device processing in recent years have enabled the development of high-voltage SiC power devices (MOSFETs and JFETs). However, the ON-resistance of SiC MOSFETs and JFETs rapidly increases as the blocking voltage and operating junction temperature increase because they are unipolar devices and conductivity modulation is not happening in the lightly doped drift region. This makes the conduction loss of the unipolar devices unacceptable for applications with a blocking voltage higher than 10 kV. For these applications, bipolar devices are preferred because they have been shown to have a small voltage drop due to strong conductivity modulation in their drift regions [113].

Simple gate drive interfaces make 4H-SiC IGBTs attractive devices. Chronologically, the first fabricated and characterized IGBTs were *P*-channel because there was a practical limitation in producing the low resistivity P^+-type SiC substrate required for fabricating *N*-channel IGBTs [114]. But with the advantages of the SiC technology, *N*-channel IGBTs have been built. Both *N*- and *P*-channel SiC IGBTs have demonstrated high blocking voltage capability, as the first IGBT fabricated in 2006 had a blocking voltage of 5.8 kV. Since then, different IGBTs have been built; for example, 12 kV *P*-channel IGBTs with 14 mΩ cm^2 ON-resistance [115], 13 kV *N*-channel IGBTs with 22 mΩ cm^2 ON-resistance [116], and 20 kV self-aligned *P*-channel DMOS-IGBTs have been reported [117]. The 20 kV *P*-channel IGBT has a less than 15 times a smaller voltage drop at 31 A cm^{-2} current density compared with a theoretical MOSFET with the same blocking voltage [117]. The last reported IGBT with ultrahigh blocking voltage of 27 kV was reported in 2015 [118].

Different SiC device research groups have been working on optimizing the IGBT parameters and fabricating and characterizing devices so that soon IGBTs will be on the market. For a given blocking voltage, a trade-off between conduction and switching loses should be made to optimize the IGBT parameters. A reason for this is that there is a huge amount of charge stored in the IGBT lightly doped drift region during the ON-state and that has to be removed during turn-OFF [119].

In [120], the device group from Cree Inc. has fabricated a 10 kV MOSFET and an *N*-type IGBT capable of flowing 10 and 4 A, respectively. Both devices were processed identically through the device fabrication process each as a MOS part where the lightly doped drift region had the same length and doping concentration. The only difference between the two devices is that the *N*-channel IGBTs have a moderately doped *N* field-stop (FS) buffer layer and a heavily doped P^+ injector, while the MOSFET has an N^+ substrate. The DC characteristics of the devices were measured, and it was observed that the forward voltage drops of the two structures were the same, ∼5 V.

The switching results indicated that both devices were much faster than the highest voltage, commercially available Si IGBT. The MOSFET turn-OFF transient time was faster than the IGBT turn-OFF time of 140 and 400 ns, respectively. A reason for slow turn-OFF time is that the IGBT is a bipolar device and stores minority and majority charges in the lightly doped drift region that are removed slowly, while the MOSFET is a unipolar device and is not dependent on carrier recombination during turn-OFF. The IGBT turn-OFF transient can be improved by reducing gate resistance and optimizing the internal capacitance and increasing the high-level lifetime.

Seven years later, the Cree Inc. group demonstrated a 20.7 kV *N*-channel IGBT with a forward voltage drop of 6.4 V at a collector current of 20 A and a 17 kV *N*-channel IGBT with a forward voltage drop of 5.7 V at a collector current of 20 A [121]. The two IGBTs were fabricated with the same mask sets and identical fabrication process. Although the lightly doped drift region for the 20.7 kV IGBT was significantly increased in width to support higher voltage, the voltage drop did not increase significantly, which can be attributed to conductivity modulation that takes place during the conduction state of the IGBT. Similar to a SiC PiN diode and a BJT, as an IGBT is a bipolar device, the junction voltage drops are dominant in determining the forward voltage drop with a blocking voltage smaller than 20 kV. The ON-resistance for an IGBT will be dominated by the parasitic resistance, such as channel resistance and the contact resistance, while the resistance of the lightly doped drift region will not be much larger due to high-level injection in the lightly doped drift region leading to conductivity modulation.

Results of a comparison of *N*-channel and *P*-channel SiC IGBTs have shown comparable static characteristics that can be explained by the fact that during the ON-state, an IGBT is operating at high-level injection. Regardless of the structure of an IGBT, the behavior of the carriers in the lightly doped drift region is governed by the ADE:

$$D\frac{\partial^2 p(x,t)}{\partial x^2} = \frac{p(x,t)}{\tau} + \frac{\partial p(x,t)}{\partial t} \tag{5.127}$$

Operating at high-level injection means that the injected carriers in the lightly doped drift region have significantly higher values than the background impurity doping concentration. The electron and hole concentrations in the drift region during the ON-state are equal:

$$p(x,t) = n(x,t) \tag{5.128}$$

Their concentrations depend on the boundary conditions at each end of the drift region, the minority charge-carrier lifetime, and the drift region width. Assuming that *N*-channel and *P*-channel IGBTs are processed identically through the device fabrication process and the gate-source voltage and collector current are the same, then the carrier concentration in the drift region of the two devices will be equal, and therefore, the voltage drop across the drift regions will be the same. The IGBT junction voltages are functions of the doping concentrations, and they will be the same for the identically processed *N*- and *P*-channel IGBTs. Therefore, the total voltage drop for identically processed *N*-channel and *P*-channel SiC IGBTs will be significantly the same when the devices are subjected to the same conditions: gate-source voltage, collector current, and temperature.

On the other hand, *N*-channel IGBTs offer far superior switching characteristics over *P*-channel IGBTs. In Ref. [122], the simulation results of the switching characteristics of *N*-channel and *P*-channel 15 kV SiC IGBTs are given that support this fact. The rate of increase in the collector-emitter voltage of an *N*-channel IGBT is 40 V ns^{-1} and for a *P*-channel IGBT is 5 V ns^{-1}. The current decay for the *N*-channel IGBT is also faster than the current decay for the *P*-channel IGBT. A physical explanation for this is that in the beginning of the turn-OFF process, the collector-emitter voltage, V_{CE}, rises from the forward voltage, V_F, to the DC supply voltage, V_{DC}, and the rate of change of the V_{CE} depends on the rate of removal of the stored charge through the emitter side. During this time, the recombination and displacement currents are significantly smaller than the minority carrier current and can be neglected. The minority current is responsible for the charge removal. As the V_{CE} rises, the depletion region expands toward the collector junction. The minority carriers are swept out through the depletion region, and the majority of carriers are pushed toward the collector where most of them will recombine in the P^+ injector layer for an *N*-channel IGBT or N^+ injector layer for a *P*-channel IGBT [119]. Due to the large rate of change in the minority carrier current, the depletion region expends faster in an *N*-channel IGBT than in a *P*-channel IGBT, and therefore, the collector voltage for *N*-channel an IGBT rises at a faster rate. During the second phase of the turn-OFF process, after the collector-emitter voltage, V_{CE}, reaches the DC supply voltage, V_{DC}, the freewheeling diode is turned ON that allows the collector current to fall down to a value depending on the remaining storage charge. During this time, the V_{CE} overshoots due to the energy stored in the stray inductance in the collector-emitter loop. After that, the collector current depends only on the remaining storage charge, and the recombination rate depends on the high-level carrier lifetime [123]. Since the holes' lifetime is smaller than the electrons' lifetime, the tailing current phase is shorter for an *N*-channel IGBT compared with a *P*-channel IGBT. Also, an *N*-channel IGBT has faster charge extraction due to the large ionization energy of acceptors in 4H-SiC [122]. Since the total losses for an *N*-channel IGBT are smaller compared with a *P*-channel IGBT, further developments in IGBT should be focused on an *N*-channel IGBT [118].

Similar to other power devices, IGBTs consist a thick lightly doped drift region that is required to support high voltage and prevent an avalanche breakdown. The drift region thickness, the doping concentration, and the minority carrier lifetime are important IGBT design parameters. Their values are optimized so that the sum of the conduction and switching losses is minimized for a desired blocking voltage. The drift region thickness and doping concentration are optimized to obtain minimum conduction loses (forward voltage drop) for the same blocking voltage. Increasing the doping concentration requires a thicker drift region to sustain the high voltage and prevent an avalanche breakdown. The minority lifetime effects the conducting and switching losses. An increase in the lifetime enhances the conductivity modulation, and therefore, the forward voltage drop is reduced, while the recombination process becomes slower and results in high switching losses. A compromise between conduction and switching losses should be made to optimize the carrier lifetime in the drift region.

To decrease the drift region thickness for the same IGBT blocking voltage, an FS layer adjacent to the lightly doped drift region is used, making the IGBT an asymmetrical device. In [124], it is shown that a 15 kV *N*-channel symmetrical IGBT does not have an FS layer and the thickness of the drift region is 247 μm, while for an asymmetrical *N*-channel IGBT, the thickness is 150 μm. Therefore, the voltage drop in the lightly doped drift region is significantly smaller for an asymmetrical device. Also, due to the FS layer, the depletion width starts to expand across the whole drift region when an IGBT is switched OFF and a punch-through effect is observed. Therefore, the depletion width that is equal to the drift region thickness should be designed first. The punch-through effect benefits the switching characteristics of an IGBT. After the punch-through, the sweep-out of the excess carriers practically stops, and the charge removal is performed mostly due to the recombination process in the FS layer. Therefore, the current tail disappears under the punch-through condition. The punch-through effect has some disadvantages also. During punch-through, the parasitic capacitance associated with increasing of the V_{CE} turns into a much smaller capacitance instead of a large diffusion capacitance [121]. This capacitance resonates with the parasitic stray inductance in the collector-emitter loop resulting in voltage overshooting and a ringing phenomenon,

which should be carefully considered. The thickness of the FS layer is an important device parameter. Increasing the FS layer thickness results in superior turn-OFF speed but slightly increases the forward voltage drop, while decreasing the FS layer thickness slows down the turn-OFF speed but offers superior conduction capability [125].

To reduce the ON-state resistance of the lightly doped drift region of an N-channel IGBT, some power device designers have inserted a thin, heavily doped N^+ current spreading layer (CSL) beneath the P-type base region, forming a JFET layer between the two P bases. An CSL helps to distribute the electron flow more uniformly, minimizing the current crowding at the top of the drift region and reducing the drift layer resistance. Both regions, CSL and JFET, are formed as N-type epitaxial layers having higher doping concentration than the drift layer. Increasing the doping concentration in the JFET region helps to reduce the ON-state resistance; however, it causes an increase in the electric field at the SiC-SiO_2 interface during the blocking state. Simulation results have shown that for a drift region width higher than 1.6 μm, the oxide field reaches 4 MV cm^{-1} prior to the avalanche breakdown in SiC. Decreasing the JFET width increases the resistance since it pinches off the current path but reduces the cell area; consequently, the effect of the specific ON-resistance is negligible [77]. An optimum width of the JFET region can be determined. When an IGBT has an optimum width, its blocking voltage is limited by the avalanche breakdown for the entire range of the lightly doped drift region. In [126], it is shown that for their design, the optimum width is 1 μm.

To optimize the parameters of a PT IGBT, a physics-based model, given in [127], can be used. For this purpose, the device is divided into five regions, as shown in Fig. 5.14: P emitter (collector terminal), N^+ field-stop layer, N^- drift region, P well, and N^+ emitter. Fig. 5.14 also shows the external currents (emitter and collector currents I_E and I_C), the internal electron and hole currents (at junctions J_0 I_{n0} and I_{p0}, J_1 I_{n_1} and I_{p_1}, and J_2 I_{n_2} and I_{p_2}), and the capacitive currents from the displacement layers (I_{disp_2} and I_{CG}). The IGBT is a gate-controlled device and is used as a controllable switch in power electronic applications. Given its P-N-P-N structure, the IGBT is a voltage bidirectional switch, that is, it can conduct current in one direction only, but it can block the voltage of both polarities. The reverse-blocking capability is rarely used in conventional power converter configurations.

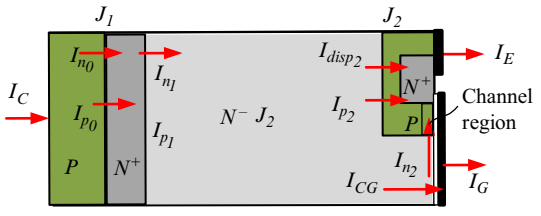


FIG. 5.14 One-dimensional cross section used for modeling of PT IGBT showing the currents in each region.

Frequently, an antiparallel diode is added as a separate chip to accommodate converter configurations, such as the voltage source inverter, which require a current bidirectional switch. In the normal forward blocking operation of the IGBT, a depletion layer is formed at the MOS end of the drift region (at the N^- drift region/P-well junction), while in a reverse-blocking operation, it is formed at the P emitter/drift region junction. In forward blocking, a depletion layer is never formed at the P emitter. For this reason, no displacement current for junction J_0 is included. The model can be easily extended to reverse-blocking IGBTs by allowing a depletion layer at the junction J_0.

The hole and electron currents in the P-emitter layer end of a power IGBT at junctions, J_0, I_{p0}, and I_{n0}, depend on the process happening in the FS layer. The sum of them is equal to the IGBT collector current:

$$I_C = I_{p0} + I_{n0} \tag{5.129}$$

where N_N is the doping concentration of the FS layer.

Adding an FS layer allows a reduction in the drift region thickness for the same blocking voltage and also speeds up the IGBT turn-off process but creates two junctions, J_0 and J_1. Due to electron reverse injection into the P^+ emitter, there is a small electron current I_{n0} at junction J_0. These electrons travel through the buffer layer from the drift region. The hole current, I_{p0}, injected from the P^+ emitter, travels mostly by diffusion through the FS layer. Since the layer is typically quite thin in comparison with the hole diffusion length, L_{p_N}, there is little recombination, and most of the holes reach the drift region. This hole current is I_{p1} and represents the hole injection from the buffer layer into the drift region.

The difference between the two hole currents at junctions J_1 and J_0 is due to the recombination, and it is compensated for by an increase in the electron current, so that the electron current I_{n1} at junction J_1 can be presented by a sum of the recombination component plus the reverse injection electron current I_{n0}. Static conditions are assumed up to now, while under dynamic conditions, an additional hole current component due to variations in the stored charge in the buffer layer should be considered.

Assuming a quasistatic state, the continuity equation of the holes in the buffer layer is then expressed by

$$D_{pN}\frac{d^2p(x)}{dt^2} = \frac{p(x)}{\tau_{pN}} \tag{5.130}$$

where τ_{pN} is the minority lifetime and D_{pN} is the hole diffusivity in the field-stop layer. The solution for the excess hole concentration in the buffer layer is given by

$$p(x) = \frac{\left[p_{N0}\sinh\left(\frac{W_N - x}{L_{pN}}\right) + p_{NW}\sinh\left(\frac{x}{L_{pN}}\right)\right]}{\sinh\left(\frac{W_N}{L_{pN}}\right)} \tag{5.131}$$

where W_N is the width of the buffer layer, p_{N0} and p_{NW} are the hole concentrations at the two edges of the field-stop layer (junctions J_0 and J_1), and L_{pN} is the hole diffusion length.

Under the low-level injection, the minority hole current is mostly diffusion current, so it is expressed as

$$I_p = qAD_{pN}\frac{dp}{dx} \tag{5.132}$$

Thus, the hole current at the junction J_0 is obtained substituting the derivative of Eq. (5.131) for $x = 0$ into Eq. (5.132):

$$I_{p0} = qAD_{pN}\left.\frac{dp}{dx}\right|_{x=0} = \frac{qAD_{pN}}{L_{pN}\sinh\left(\frac{W_N}{L_{pN}}\right)}\left[p_{N0}\cosh\left(\frac{W_N}{L_{pN}}\right) - p_{NW}\right] \tag{5.133}$$

Assuming quasiequilibrium, the reverse injection current I_{n0} at junction J_0 is given by

$$I_{n0} = \frac{AI_{sne}N_N p_{N0}}{n_i^2} \tag{5.134}$$

where I_{sne} is the emitter electron saturation current.

The current continuity at the boundaries of the buffer layer requires that

$$I_C = I_{n0} + I_{p0} = I_{n1} + I_{p1} + I_{dis1} \tag{5.135}$$

Then, the hole concentration at the junction J_1 is obtained by substituting Eqs. (5.133), (5.134) into Eq. (5.135) and then reorganizing the equation to the form:

$$p_{N0} = \left[\frac{AI_{sne}N_N}{n_i^2} + \frac{qAD_{pN}}{L_{pN}\sinh\left(\frac{W_N}{L_{pN}}\right)}\right]^{-1}\left[I_C + \frac{qAD_{pN}}{L_{pN}\sinh\left(\frac{W_N}{L_{pN}}\right)}p_{NW}\right] \tag{5.136}$$

The hole current I_{p1} at junction J_1 is obtained similar to I_{p0}, only $x = W_N$:

$$I_{p1} = qAD_{pN}\left.\frac{dp}{dx}\right|_{x=W_N} = \frac{qAD_{pN}}{L_{pN}\sinh\left(\frac{W_N}{L_{pN}}\right)}\left[p_{N0} - p_{NW}\cosh\left(\frac{W_N}{L_{pN}}\right)\right] + I_{QN} \tag{5.137}$$

The current, I_{QN}, represents the capacitive current due to the variation in the charge Q_N stored in the buffer region:

$$I_{QN} = -\frac{dQ_N}{dt} \tag{5.138}$$

The charge Q_N can be approximated as

$$Q_N = qAW_N\frac{p_{N0} + p_{NW}}{2} \tag{5.139}$$

The hole concentration, p_{NW}, at the boundary between the buffer layer and the drift region is obtained by applying the Boltzmann relationship for the junction J_2 under the assumption of high-level injection in the drift region ($p_{N^-0} >> N_{N^-}$):

$$p_{NW} = \frac{p_{N^-0}(p_{N^-0} + N_{N^-})}{N_N} = \frac{p_{N^-0}^2}{N_N} \tag{5.140}$$

where p_{N^-0} is the hole concentration in the beginning and N_{N^-} is the doping concentration of the N^- drift region.

The voltages across the junctions J_0 and J_1 are

$$V_{J0} = V_T\ln\left(\frac{p_{N0}N_N}{n_i^2}\right) \tag{5.141}$$

$$V_{J1} = V_T\ln\left(\frac{N_{N^-}}{p_{N^-0}}\right) \tag{5.142}$$

The voltage drop in the N^- drift region is calculated during the ON-state. The charge distribution and the boundary current components in the N^- region are shown in Fig. 5.15. The injected excess carrier concentration is determined by the ADE. As for all bipolar power switches, high-level injection and quasineutral conditions exist. Under high-level injection conditions, the ADE (Eq. 5.35) describes the carrier dynamics.

It was mentioned that, during forward blocking of an IGBT, no depletion layer forms at junction J_1; therefore, its thickness, x_1, can be approximated as zero. Therefore, the charge storage region, which operates under high-level injection and is described by the ADE, Eq. (5.35), has $x_1 \equiv 0$ and $\frac{dx_1}{dt} \equiv 0$. The Fourier series solution of the ADE, given by Eq. (5.39), can be simplified to

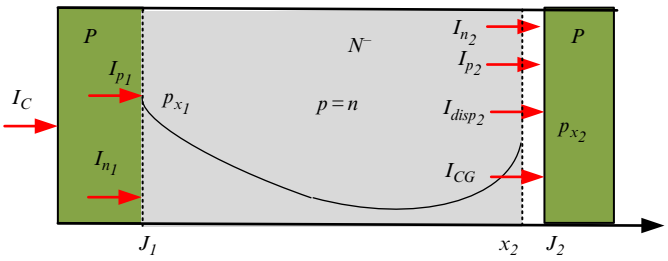


FIG. 5.15 Charge distribution and boundary current components in the N^- region of PT IGBT.

For $k > 0$

$$D_{N^-}\left[\left.\frac{\partial p(x,t)}{\partial x}\right|_{x2}(-1)^k - \left.\frac{\partial p(x,t)}{\partial x}\right|_{x1}\right] = \frac{x_2}{2}\left(\frac{dp_k(t)}{dt} + \left[\frac{1}{\tau} + \frac{D_{N^-}k^2\pi^2}{x_2^2}\right]p_k(t)\right) + \left(\sum_{\substack{n=1 \\ n\neq k}}^{\infty}\frac{n^2}{n^2-k^2}\left[(-1)^{n+k}\frac{dx_2}{dt}\right]p_n(t) + \frac{p_k(t)}{4}\left(\frac{dx_2}{dt}\right)\right) \quad (5.143)$$

For $k = 0$

$$D\left[\left.\frac{\partial p(x,t)}{\partial x}\right|_{x_2} - \left.\frac{\partial p(x,t)}{\partial x}\right|_{x1}\right] = x_2\left(\frac{dp_0(t)}{dt} + \frac{p_0(t)}{\tau}\right) - \sum_{n=1}^{\infty}\left[(-1)^n\frac{dx_2}{dt}\right]p_n(t)$$

The solution to the ADE is determined by using the boundary conditions at the edges of the charge storage region:

$$\left.\frac{\partial p}{\partial x}\right|_{x_1} = \frac{1}{2q}\left(\frac{J_n}{D_n} - \frac{J_p}{D_p}\right)\Bigg|_{x_1} \quad \text{and} \quad \left.\frac{\partial p}{\partial x}\right|_{x_2} = \frac{1}{2q}\left(\frac{J_n}{D_n} - \frac{J_p}{D_p}\right)\Bigg|_{x_2} \quad (5.144)$$

The current continuity equation at junction J_2 is determined by

$$I_C = I_{n_2} + I_{p_2} + I_{disp_2} + I_{CG} \quad (5.145)$$

The electron current at junction J_2 is the MOS channel current:

$$I_{n_2} = I_{mos} \quad (5.146)$$

Substituting Eqs. (5.146) in (5.145) and then in Eq. (5.143), the left side of the solution of the ADE (Eq. 5.143), for even and odd numbers of k, can be calculated by the following equations:

$$I_{odd} = -D\left(\left.\frac{\partial p}{\partial x}\right|_{x_2} + \left.\frac{\partial p}{\partial x}\right|_{x_1}\right) = \begin{vmatrix} I_{n_1} \\ I_{mos} \\ I_C \\ I_{disp_2} \\ I_{CG} \end{vmatrix} \frac{1}{2qA}\begin{vmatrix} 2 & -2 & \frac{2D}{D_p} & -\frac{D}{D_p} & -\frac{D}{D_p} \end{vmatrix}$$

$$I_{even} = D\left(\left.\frac{\partial p}{\partial x}\right|_{x_2} - \left.\frac{\partial p}{\partial x}\right|_{x_1}\right) = \frac{1}{2qA}\begin{vmatrix} I_{n1} \\ I_{mos} \\ I_C \\ I_{disp2} \\ I_{CG} \end{vmatrix} \begin{vmatrix} -2 & +2 & 0 & +\frac{D}{D_p} & +\frac{D}{D_p} \end{vmatrix} \quad (5.147)$$

The boundary carrier densities p_{x1} and p_{x2} at the boundaries x_1 and x_2 are calculated using the equations:

$$p_{x_1} = \sum_{k=0}^{M-1} p_k \quad \text{and} \quad p_{x_2} = \sum_{k=0}^{M-1}(-1)^k p_k \quad (5.148)$$

The voltage across the N^-P depletion layer, V_{d_2}, is calculated by the following equation:

$$V_{d_2} = \begin{cases} 0 & \text{if } p_{x_1} > 0, \\ -K_{FV}p_{x_2} & \text{otherwise.} \end{cases} \quad (5.149)$$

The associated depletion width, W_{d_2}, is calculated using a step doping concentration change on each side of the junction:

$$W_{d_2} = \sqrt{\frac{2\varepsilon V_{d_2}}{qN_{N^-} + \frac{|I_C|}{Av_{sat}}}} \quad (5.150)$$

The boundary position x_2 is calculated by

$$x_2 = W_{N^-} - W_{d_2} \quad (5.151)$$

The displacement current at x_2 is composed of two components: I_{disp_2} flowing into the P well and I_{CG} associated with Miller capacitance and accumulation layer charge. The P-well displacement current is given by

$$I_{disp_2} = C_{J_2}\frac{dV_{d2}}{dt} = \varepsilon A\frac{1}{W_{d_2}}\frac{dV_{d_2}}{dt} \quad (5.152)$$

To calculate the Miller capacitance, it is assumed that the depletion layer extends under the gate from P well and only extends downward through the drift region once the accumulation layer has been removed from the gate in the center of the intercell region. Therefore, the width of the Miller capacitance, W, is

$$W = W_{d2} - l_m - l_1 \quad (5.153)$$

where l_m is an intercell half width and l_1 is a width due to voltage V_{GE}:

$$l_1 = \sqrt{\frac{2\varepsilon V_{GE}}{qN_{N^-}}} \quad (5.154)$$

The Miller capacitance is given by the series combination of the oxide capacitance $C_{ox}Aa_i$ and the depletion capacitance $\frac{\varepsilon Aa_i}{W}$:

$$C_{CG} = \frac{C_{ox}Aa_i}{1 + \frac{C_{ox}}{\varepsilon}W} \quad (5.155)$$

where a_i is the ratio of intercell area to the total die area.

Due to Miller capacitance, the current I_{CG} is

$$I_{CG} = C_{CG}\left(\frac{dV_{d2}}{dt} - \frac{dV_{GE}}{dt}\right) \quad (5.156)$$

where

$$\frac{dV_{GE}}{dt}=\frac{1}{C_{GE}+C_{GC}}\left(I_G+C_{CG}\frac{dV_{d2}}{dt}\right) \tag{5.157}$$

The voltage drop in the carrier storage region V_{N^-} is calculated based on the injected carrier concentration:

$$V_{N^-}\approx\frac{I_C}{qA\left(\mu_n+\mu_p\right)}\frac{x_2-x_1}{M-1}\sum_{\kappa=0}^{M-1}\left[\frac{1}{p_{T(k)}-p_{T(k-1)}}\ln\left(\frac{p_{T(k)}}{p_{T(k-1)}}\right)\right]+V_T\left(\frac{\mu_n-\mu_p}{\mu_n+\mu_p}\right)\ln\left(\frac{p_{x2}}{p_{x1}}\right) \tag{5.158}$$

where the carrier distribution $p_{T(k)}$ is calculated as

$$p_{T(k)}=p\left(x_1+\frac{k(x_2-x_1)}{M-1}\right)+\frac{\mu_n N_{N^-}}{\mu_n+\mu_p} \tag{5.159}$$

IGBTs are used as switches, operating mainly in two stages: ON and OFF. The MOS region can be modeled as a simple MOSFET. During the ON-state, the MOSFET operates either in the triode region or in the saturation region, while during the OFF-state, it operates in cut-OFF. Therefore, during the OFF-state, the gate-source voltage is smaller than the threshold voltage ($V_{GS}<V_{TH}$), and current I_{mos} is zero. During the ON-state, the gate-source voltage is larger than the threshold voltage ($V_{GS}>V_{TH}$), and current I_{mos} is calculated by

$$I_{mos}=\begin{cases}\frac{K_p}{2}\left[2V_{DS}(V_{GS}-V_{TH})-V_{DS}^2\right] & \text{if } V_{DS}\le V_{GS}-V_{TH}\\ \frac{K_p}{2}(V_{GS}-V_{TH})^2 & \text{otherwise}\end{cases} \tag{5.160}$$

The voltage drop V_{CE} across PT IGBT is composed of three components: voltages across the junction J_1, voltage across the two depletion regions V_{d2}, and voltage across the carrier storage region V_{N^-}.

$$V_{CE}=V_{j_1}+V_{d_2}+V_{N^-} \tag{5.161}$$

5.3.7 SiC Thyristor

As the trend of power electronics industry is moving toward high voltage, high current, and high frequency, the conduction and switching losses of the power semiconductor devices should be at an acceptable level. Up to now, SCRs are still the most powerful devices currently available in pulse power applications. A single SCR can block 8 kV and conduct 4 kA, and a GTO can block 6 kV and conduct 6 kA [128]. However, due to the high switching losses of SCRs and GTOs, their maximum operation frequency is limited to 1 kHz. Because of their switching and driving characteristics, the device paralleling for high-power applications is impossible. SCRs and Si GTOs have a positive temperature coefficient and their operating temperature is limited to 100°C junction temperature, since the leakage current increases significantly above that temperature. Typically, this requires expensive active liquid cooling to maintain safe operation conditions. The leakage current of a SiC GTO is extremely small at 300°C and only requires forced air cooling.

SiC GTOs and IGBTs are two devices that can soon be utilized in utility-based power handling equipment, such as flexible AC transmission systems (FACTS) and high-voltage DC transmissions (HVDCT). A 4H-SiC thyristor is a better candidate because it is capable of higher current densities than a SiC IGBT, since the physical mechanism for conductivity modulation is more effective in the thyristor than the IGBT. Also, SiC IGBTs are limited to 150°C junction temperature due to a limitation of the gate oxide reliability.

In the near future, large-area SiC GTOs will be utilized in FACTS and HVDCT due to three main advantages: a smaller number of devices connected in series since they have higher blocking capability (20–30 kV with the present technology), low current leakage, and reduced cooling requirements due to the ability of SiC GTOs to operate at higher junction temperatures (300°C if the packaging issues are solved). However, the thyristor requires more complex external circuitry as it is a current-controlled device.

The first SiC symmetrical thyristors (700 V with a rated current of 6 A and a forward drop of 3.9 V) were demonstrated by Cree, Inc. [129]. Since then, scientists from Cree and other institutions have designed and fabricated different asymmetrical *NPNP* devices. The limitations of the epilayer thickness and device footprint have been the main obstacles for increasing the blocking voltage and the current capability of the devices, but different scientific groups have worked in the last two decades to improve design, fabrication, and characterization of different power semiconductor devices that were used for an evaluation of SiC GTOs from 1.77 kV blocking voltage with 4 V voltage drop at 100 A and 200°C [130] demonstrated in 2005 to a 22 kV blocking voltage with approximately 6.5 V voltage drop at 100 A and 150°C reported 10 years later. The most important developments of this evaluation were increasing the wafer diameter to 5.9″ (150 mm) [131]; the electrically active defects, such as dislocations, point defects, and silicon inclusion, have been drastically reduced; the problem of the foreword voltage drop, V_F, drift due to high density of the basal plane dislocation has been solved by improving the epitaxial growth; and improving the life time of the minority carrier concentration in the lightly doped drift region.

Due to very high blocking voltage (>20 kV) for SiC GTOs, they have a low-doped thick drift region that has high resistivity. In order to obtain significantly low ON-state losses, the ambipolar diffusion length of the minority carriers in the drift region should be significantly large, that is, the minority carrier

lifetime must be made as long as possible. For an *N*-type SiC epilayer, a significant improvement of carrier lifetime has been achieved from 0.69 to 9.5 μs by reducing the $Z_{1/2}$ center via two-step thermal treatment (thermal oxidation and Ar annealing) for a 148 μm N-type epilayer [132]. However, there is some difficulty for enhancement of the carrier lifetimes in *p*-type epilayers [133]. In [134], the lifetime in *P*-type SiC epilayer was improved from 1 to 4 μs by oxidation at 1300°C for 5 h prior to the metal contact processing; however, the carrier lifetime was not uniform across the chip area. The lifetime uniformity can be enhanced by controlling the point defects in SiC by low-energy electron irradiation [132].

Currently, the thyristors are made on N^+ 4H-SiC substrates, because P^+ substrates have higher resistance than the N^+ substrates. Recently, a significant improvement in N^+ 4H-SiC substrate quality has been reported. An IGBT with an ultrahigh blocking voltage of 27 kV was built on N^+ 4H-SiC substrate [118]. For a Si power thyristor to minimize power losses, the epilayer is N^- type. Therefore, in the future, power thyristors will build on P^+ substrate with an N^- epilayer.

To optimize the parameters of the transistor, a physics-based model for GTOs employing a Fourier-based solution for the ambipolar diffusion equation of the N^- lightly doped drift region and a lumped-charge method for the P-base region can be used. A new level-3 physics-based model for GTOs employs a Fourier-based solution for the ambipolar diffusion equation of the lightly doped N^- drift region, and a lumped-charge method for the *P*-base region is provided below. In addition to the external electric characteristics, the model can also provide internal physical and electric information, such as junction voltages, and the charge distribution in the buffer layer and the base regions. Fig. 5.16 shows the schematic structure of a SiC high-power thyristor with the direction of the flowing currents.

A major difficulty in analyzing and modeling the performance of bipolar power devices is due to the different carrier density distribution in the different regions. The behavior of the GTO is modeled by dividing the device into different regions.

The P^+ and N^+ emitter regions have high doping concentration, and therefore, there is a significant electron concentration adjacent to the P^+N junction and a significant hole concentration adjacent to the PN^+ junction due to the equal concentrations of holes and electrons. As a result of these high concentrations, minority carriers flow into the highly doped P^+ and N^+ emitter regions, where they recombine with holes and electrons, respectively. The process is known as emitter recombination. The resulting electron and hole currents due to the recombination are

$$I_{n0} = qAh_p p_{N0}^2 \tag{5.162}$$

$$I_{p3} = qAh_n n_{PW}^2 \tag{5.163}$$

where p_{N0} and n_{PW} are the hole and the electron concentrations at junctions J_0 and J_3, respectively. The recombination parameters, h_p and h_n, calculated by Eqs. (5.32), (5.63), depend on the emitter properties, such as doping level (N_{P^+} and N_{N^+}), electron and hole diffusivities (D_n and D_p), and electron and hole lifetime (τ_n and τ_p). The hole and emitter currents in the P^+ and N^+ emitter regions are

$$I_{p0} = I_A - I_{n0} \tag{5.164}$$

$$I_{n3} = I_A - I_{p3} \tag{5.165}$$

Adding a buffer layer allows a reduction of the drift region thickness for the same blocking voltage and speeds up the thyristor turn-off process, but it creates two junctions, J_1 and J_2. Due to electron reverse injection into the P^+ emitter, there is a small electron current, I_{n0}, at junction J_0. These electrons travel through the buffer layer coming from the drift region. The hole current, I_{p0}, injected from the P^+ emitter travels mostly by diffusion through the buffer layer. Since the buffer layer is typically quite thin in comparison with the diffusion length in the buffer layer, L_{p_N}, there is little recombination in the buffer layer, and most of the hole current reaches the drift region. This current, I_{p1}, presents the hole injection from the buffer layer into the drift region.

The difference between the two hole currents at the junction J_1 and J_0 is due to the recombination, and it is compensated by an increase in the electron current, so that the electron current I_{n1} at junction J_1 can be presented by a sum of the

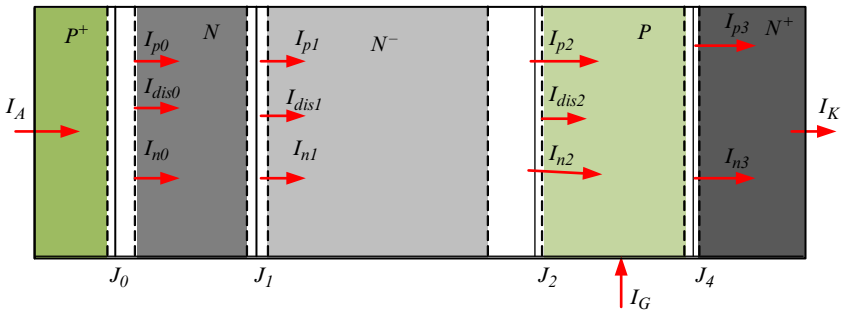


FIG. 5.16 Schematic structure of SiC high-power thyristor.

recombination component plus the reverse injection electron current I_{n0}. Static conditions are assumed up to now, while under the dynamic condition an additional hole current component due to variations in the stored charge in the buffer layer should be consider.

Assuming a quasistatic state, the continuity equation of the holes in the buffer layer is then expressed by

$$D_{pN}\frac{d^2p(x)}{dt^2}=\frac{p(x)}{\tau_{pN}} \tag{5.166}$$

where τ_{pN} is the minority lifetime and D_{pN} is the hole diffusivity in the buffer layer. The solution for the excess hole concentration in the buffer layer is given by

$$p(x)=\frac{\left[p_{N0}\sinh\left(\frac{W_N-x}{L_{pN}}\right)+p_{NW}\sinh\left(\frac{x}{L_{pN}}\right)\right]}{\sinh\left(\frac{W_N}{L_{pN}}\right)} \tag{5.167}$$

where W_N is the width of the buffer layer, p_{N0} and p_{NW} are the hole concentrations at the two edges of the buffer layer (junctions J_0 and J_1), and L_{pN} is the diffusion length of the holes.

Under the low-level injection, the minority hole current is mostly diffusion current, so it is expressed as

$$I_p=qAD_{pN}\frac{dp}{dx} \tag{5.168}$$

Thus, the hole current at the junction J_0 is obtained by substituting the derivative of Eq. (5.167) for $x=0$ into Eq. (5.168):

$$I_{p1}=qAD_{pN}\left.\frac{dp}{dx}\right|_{x=0}=\frac{qAD_{pN}}{L_{pN}\sinh\left(\frac{W_N}{L_{pN}}\right)}\left[p_{N0}\cosh\left(\frac{W_N}{L_{pN}}\right)-p_{NW}\right] \tag{5.169}$$

Assuming quasiequilibrium, the reverse injection current I_{n0}, at junction J_0 is given by

$$I_{n1}=\frac{I_{sne}N_Np_{N0}}{n_i^2} \tag{5.170}$$

where I_{sne} is the emitter electron saturation current, which is usually small, and N_N is the doping concentration of the buffer layer.

The current continuity at the boundaries of the buffer layer requires that

$$I_A=I_{n0}+I_{p0}=I_{n1}+I_{p1}+I_{dis1} \tag{5.171}$$

Then, the hole concentration at the junction J_1 is obtained by substituting Eqs. (5.169), (5.170) into Eq. (5.171) and then reorganizing to the form:

$$p_{N0}=\left[\frac{AI_{sne}N_N}{n_i^2}+\frac{qAD_{pN}}{L_{pN}\sinh\left(\frac{W_N}{L_{pN}}\right)}\right]^{-1}\left[I_A+\frac{qAD_{pN}}{L_{pN}\sinh\left(\frac{W_N}{L_{pN}}\right)}p_{NW}\right] \tag{5.172}$$

The hole current, I_{p1}, at junction J_1 is obtained similar to I_{p0}, only $x=W_N$:

$$I_{p1}=qAD_{pN}\left.\frac{dp}{dx}\right|_{x=W_N}=\frac{qAD_{pN}}{L_{pN}\sinh\left(\frac{W_N}{L_{pN}}\right)}\left[p_{N0}-p_{NW}\cosh\left(\frac{W_N}{L_{pN}}\right)\right]+I_{QN} \tag{5.173}$$

The current, I_{QN}, represents the capacitive current due to the variation in the charge, Q_N, stored in the buffer region.

$$I_{QN}=-\frac{dQ_N}{dt} \tag{5.174}$$

The charge, Q_N, can be approximated as

$$Q_N=qAW_N\frac{p_{N0}+p_{NW}}{2} \tag{5.175}$$

The hole concentration, p_{NW}, at the boundary between the buffer layer and the drift region, is obtained by applying the Boltzmann relationship for the junction J_1 under the assumption of high-level injection in the drift region ($p_{N^-0}>>N_{N^-}$):

$$p_{NW}=\frac{p_{N^-0}(p_{N^-0}+N_{N^-})}{N_N}=\frac{p_{N^-0}^2}{N_N} \tag{5.176}$$

where p_{N^-0} is the hole concentration in the beginning and N_{N^-} is the doping concentration of the N^- drift region that is denoted below as p_{x1}.

The voltages across the junctions, J_0 and J_1, are

$$V_{J1}=V_T\ln\left(\frac{p_{N0}N_N}{n_i^2}\right) \tag{5.177}$$

$$V_{J2}=V_T\ln\left(\frac{N_{N^-}}{p_{N^-0}}\right) \tag{5.178}$$

The GTO thyristor requires a thick drift region to support a high blocking voltage. A simple charge control modeling approach cannot be applied for the drift region because the transient duration compares with or is shorter than the transient time of the charge carriers. In this case, the charge dynamics in the drift region can be described by the continuity and the transport equations. The charge profile in the thick drift region can be assumed as one-dimensional over more than 90% of the volume, which makes the analysis simple. Also, high-level

injection conditions can be assumed during the time of the transient and static state. Under this assumption and quasineutrality, the one-dimensional ambipolar diffusion equation that describes the carrier dynamics in the majority of this region is given by Eq. (5.35). The equations from Section 5.3.2.2 for SiC PiN diodes in Eqs. (5.35)–(5.61) are the same for a power GTO, so it will not be repeated.

The junction voltage V_{J2} between the lightly doped drift region N^- and the P base is

$$V_{J2} = 2V_T \ln\left(\frac{p_{x2}}{n_i}\right) \tag{5.179}$$

The lumped-charge method can be used to model the charge behavior in the base region due to high doping level and comparatively narrow base width. Using the continuity equation for the base region, the injected minority carrier charge can be described by the relation below:

$$\frac{dQ_P}{dt} + \frac{Q_P}{\tau_{PHL}} = I_{n3} - I_{n2} = I_{p2} + I_G + I_{disp2} - I_{p3} \tag{5.180}$$

where τ_{PHL} is the high-level lifetime in the P-base region. The electron concentration at the P-base region boundary, n_{P0}, is related to p_{x2} by the doping concentration of the base, N_P, by the equation:

$$n_{P0} = \frac{p_{x2}^2}{N_P} \tag{5.181}$$

The total electron charge in the base can be expressed as

$$Q_P = \frac{n_{P0} + n_{PW}}{2} qAW_P \tag{5.182}$$

where n_{PW} is the electron concentration at the base region boundary from the N^+ emitter side and W_P is the base width. Since the diffusion length in the P-base region is much greater than the base width, the gradient of the electron concentration may be approximated linearly. Then, the electron current at junction, J_3, is

$$I_{n3} = qD_nA\frac{n_{PW} - n_{P0}}{W_P} \tag{5.183}$$

The junction voltage V_{J3} between the P-base and the N^+ emitter can be calculated by the equation:

$$V_{J2} = V_T \ln\left(\frac{n_{PW}(n_{PW} + N_P)}{n_i^2}\right) \tag{5.184}$$

The voltage drop V_{AK} across the SiC thyristor is composed of seven components including voltages across junctions J_0, J_1, J_2, and J_3, the voltage across the two depletion regions, V_{d1} and V_{d2}, and the voltage across the drift region, V_{N^-}:

$$V_{AK} = V_{J0} + V_{J1} + V_{J2} + V_{J3} + V_{d1} + V_{d2} + V_{N^-} \tag{5.185}$$

5.4 GaN Power Devices

Due to the significant improvements in GaN material growth technology, engineers have utilized different GaN-based power devices in high-frequency and power applications. The device designers are trying to improve performance and reliability and optimize their FOM parameters to obtain high system efficiency. GaN HEMT devices ranging up to 650 V are available on the market. The physics and important parameters of GaN power devices are discussed below.

5.4.1 Lateral GaN Schottky Barrier Diodes

To achieve a high-efficiency, high-density power conversion system, the high-voltage diodes used in a system should have low turn-ON voltage, V_T, low ON-resistance, R_{ON}, low leakage current, and short reverse recovery time. Due to the wide bandgap of GaN and high electron mobility in the 2DEG, AlGaN-/GaN-based lateral Schottky barrier diodes (SBDs) on a Si, sapphire, or SiC substrate have demonstrated superior performance over rectifiers made in other material systems, such as gallium arsenide (GaAs)-based devices. The advantages of lateral GaN-based devices are that they have a very low ON-resistance because of the extremely high electron concentrations in the 2DEG, up to 10–20 times higher that GaAs-based devices. Lateral SBDs have a small junction capacitance compared with conventional Schottky diodes and, therefore, low reverse recovery times. Also, a lateral design approach enables the standard GaN HEMT process flow to be used for integrating a Schottky diode with a high-voltage transistor [135].

A cross section of a typical lateral AlGaN/GaN heterostructure Schottky diode is shown in Fig. 5.17. The epitaxial layers are grown by metal-organic chemical vapor deposition on a substrate, and then, two types of contacts, ohmic and Schottky, are formed.

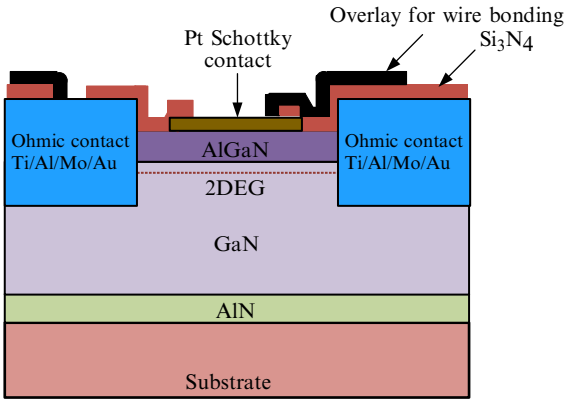


FIG. 5.17 Cross section of a lateral AlGaN/GaN heterostructure Schottky diode (substrate, AlN buffer layer, GaN, and AlGaN).

The quality of the epitaxial GaN depends on the quality of the substrate. Si, sapphire, SiC, and GaN can be used for the substrate. Si substrates have good quality, are significantly large in size, and are inexpensive. They can be used for GaN devices for low-power-density applications, where the losses are not high and the device temperature does not exceed the maximum operating junction temperature. Using a Si substrate for GaN devices introduces a number of critical issues due to the lattice mismatch and the difference in the thermal expansion coefficients, which affects the quality and device reliability [34]. Sapphire substrates are cost-effective and widely used for electronic devices with high power density and high-pulsed-output power densities, but it has a high lattice mismatch to GaN and poor thermal conductivity. Therefore, it is difficult to remove heat produced during operation. For high-power-density applications, the GaN devices should be grown on a SiC substrate since the SiC thermal conductivity is three times higher than Si, which leads to improved heat dissipation. The qualities of SiC substrates have improved significantly in the last few years, but they are still not widely available at low cost. GaN substrates have only recently been developed and used for power devices, although they are most important for optical applications. By using GaN substrates, the lattice mismatch is fully eliminated, but the cost of these substrates is high, and large diameters are not available. GaN layers grown on GaN substrates have low defect densities compared with layers grown on other types of substrate. Therefore, for devices of the same physical dimensions, devices utilizing GaN substrates will exhibit better OFF-state and ON-state characteristics.

Growth of GaN onto a Si or a sapphire substrate offers the very attractive potential for incorporating GaN devices. However, because of the large difference in lattice constant, crystal structure, and thermal expansion coefficient, it is difficult to epitaxially grow GaN. To solve this problem, a buffer layer that minimizes the mismatch between the substrate and GaN allows growth with a quality equal to GaN. Several buffer layer types have been used to grow GaN on Si, for example, SiC [136], AlN [137], GaAs [138] and silicon nitride (Si_3N_4) [139]. An AlN buffer layer is one of the best candidates for obtaining high-quality GaN on a Si substrate. It was found in [140] that a thicker AlN buffer layer resulted in higher crystalline quality of consequently grown GaN film.

The heterostructure consisting of undoped GaN and undoped zinc blende (cubic) ($Al_{0.3}Ga_{0.7}N$) is grown on the AlN buffer layer. Due to spontaneous and piezoelectric polarization, a 2DEG is created in the channel at the AlGaN/GaN interface [141]. The sheet electron density and the mobility in the channel are significantly high, $\sim 10^{13}\,\text{cm}^{-2}$ and $1500\,\text{cm}^2\,(\text{V s})^{-1}$, respectively, which result in low ON-state resistance.

Two types of contacts are formed in a lateral SBD. Metals or alloys such as palladium (Pd), platinum (Pt), indium-platinum (IrPt), palladium-silver (PdAg), and nickel/gold (Ni/Au) that have higher work functions than GaN can be used to form a Schottky barrier to the channel. The Schottky barrier is formed to the AlGaN interfacial layer of an AlGaN/GaN heterostructure. Since the channel has a high electron concentration, the depletion length is significantly shorter than in conventional diodes, although the lateral SBDs have a greater barrier height.

The ohmic contacts of a GaN power device (diodes and transistors), in most cases, represent a metal stack that is formed by thermal evaporation of different metals in multilayers following by rapid thermal annealing. The devices should be optimized to have low specific conduction resistance, and they should also be thermally stable. For *N*-type GaN, metal stacks such as titanium/aluminum/molybdenum/gold (Ti/Al/Mo/Au) and titanium/aluminum/platinum/gold (Ti/Al/Pt/Au) can be used to form ohmic contacts because of their excellent characteristics. A specific contact resistivity as low as $4.7 \times 10^{-7}\,\Omega\,\text{cm}^{-2}$ was obtained by rapid thermal annealing of evaporated Ti/Al/Mo/Au [142]. Also, Ti/Al/Pt/Au contacts on GaN have shown a minimum contact resistivity of $8.4 \times 10^{-5}\,\Omega\,\text{cm}^{-2}$ after annealing [143].

Applying a positive bias, higher than the turn-ON voltage, V_T, to the anode, causes electrons to flow from cathode to the anode. For an applied anode to cathode voltage, V_{AC}, higher than $3kT/q$, the current through the diode is

$$I_A = AA^*T^2 e^{-\frac{q\phi_B}{kT}}\left(e^{-\frac{qV_{AC}}{kT}} - 1\right) \tag{5.186}$$

where A is the Schottky contact area and A^* is the Richardson constant ($26.4\,\text{A cm}^{-2}\text{K}^{-2}$), and the potential barrier at the metal-semiconductor interface, ϕ_B, depends on the work function of the metal or alloy used for the Schottky contact.

As a negative bias is applied to the Schottky contact, a depletion layer between the Schottky contact and the 2DEG is formed. Increasing the negative voltage, the depletion layer expands and the junction capacitance decreases, resulting in a nonlinear capacitance-voltage characteristic [144]. A simple equivalent circuit model of a Schottky/2DEG diode is shown in Fig. 5.18. It consist of a voltage-dependent junction capacitance, C_j, series resistance, R_s, and a shunt capacitance, C_{sh}, [144].

The junction capacitance, C_j, is

$$C_j(V_{AC}) = \frac{W\varepsilon}{\pi} A \ln\left(\frac{\left(R^2 + d_{dep}^2\right)^{1/2} + R}{\left(R^2 + d_{dep}^2\right)^{1/2} - R}\right) \tag{5.187}$$

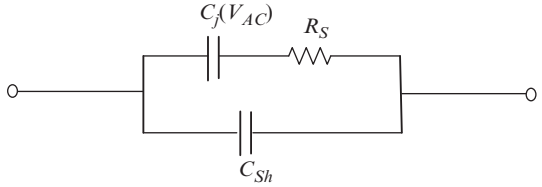


FIG. 5.18 A simple equivalent circuit model of a Schottky diode.

where W is the Schottky contact width and R is the half height of the Schottky metallization. The depletion width d_{dep} is

$$d_{dep}(V_{AC}) = \frac{2\varepsilon(V_{bi} - V_{AC})}{qn_s} \tag{5.188}$$

where V_{bi} is the built-in voltage, V_{AC} is the reverse bias applied voltage, and n_s is the 2DEG sheet charge density. The series resistance, R_s, is a sum of the undepleted channel resistance, R_{CH}, and the ohmic contact resistance, R_{OC}:

$$R_s = R_{CH} + R_{OC} \tag{5.189}$$

The undepleted channel resistance, R_{CH}, is

$$R_{CH} = \frac{L_{AC} - d_{dep}}{q\mu_n n_s W} \tag{5.190}$$

where L_{AC} is the distance between anode and cathode (channel length) and μ_n is the electron mobility in 2DEG. The ohmic contact resistance, R_{OC}, is

$$R_{OC} = \frac{r_{sp}}{W} \tag{5.191}$$

where r_{sp} is the specific contact resistivity. The shunt capacitance, C_{sh}, includes the ohmic contact (pad-to-pad) capacitance and Schottky contact-to-ohmic pad capacitance.

For high-voltage SBDs, the device channels are significantly long. Therefore, it can be assumed that the junction breakdown is caused either by impact ionization or by tunneling. The channel length, L_{AC}, is a very important device parameter for a lateral SBD. By increasing the distance, L_{AC}, larger breakdown voltages can be obtained, but the ON-resistance and, therefore, the conduction losses will be higher.

Different technologies have been studied to improve SBD performance. One of them uses an anode composed of two metals with different work functions. In this case, two types of contacts are formed: a Schottky and an ohmic, as shown in Fig. 5.19.

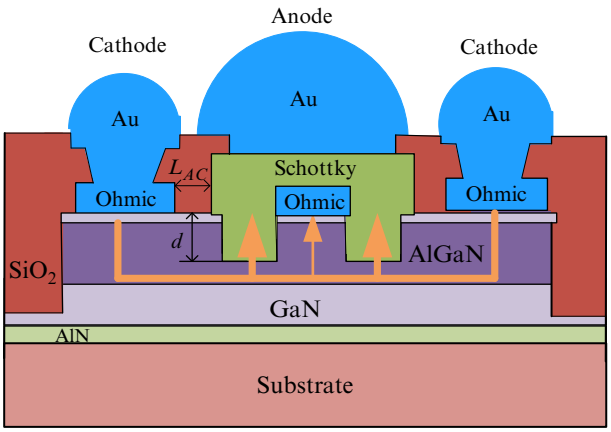


FIG. 5.19 A Schottky diode with recessed dual anode metal.

The low work function metal reduces the turn-ON voltage, V_T, and the high work function metal at the edge of the anode reduces the reverse leakage current and maintains the breakdown voltage. In [145], it is shown that the turn-ON voltage of the SBD is reduced from 1.47 to 0.57 V by employing the dual metal anode, and the breakdown voltages are virtually unaffected.

Another technology that can be used to reduce the turn-on voltage, V_T, without an increase in the leakage current is recess etching in the anode region of an SBD. The etching process must be well controlled because uneven etched surface morphologies can result in an increase in the surface leakage current [146]. A combination of an ohmic anode and a recessed Schottky gate, as shown in Fig. 5.19, is responsible for the low turn-ON voltage and an increase in the forward current. No breakdown-voltage degradation has been observed. In comparison with a conventional SBD, the forward current at 1.5 V is increased by two to three times in the SBD with a recessed dual anode metal, resulting in a breakdown voltage of 1440 V. The reason for this is that when a small positive voltage is applied to the anode, electrons flow from the cathode to the anode ohmic metal. Increasing the anode voltage so that the Schottky contact under the recessed anode region is turned on causes electrons to also flow through the Schottky metal. Additional electrons passing through the anode ohmic contact lead to very low turn-ON voltage, V_T, and high forward current.

The recess depth, d, is an important design parameter for a Schottky GaN device. For devices with a higher value than the optimum recessed depth, the electrons tend to flow through the Schottky metal instead of through the anode ohmic metal so that the electrons flowing to the anode ohmic metal are suppressed. The blocking voltage is not affected by the recess depth. In [146], it is reported that an AlGaN/GaN on Si SBD with dual metal and 16 nm recess depth with 0.34 V turn-ON voltage, V_T, has an anode current, I_A, (at 1.5 V) equal to 1.63 A. A SBD with a maximum breakdown voltage of 1.9 kV was reported by [147].

Researchers have reaped the benefits of GaN lateral Schottky diodes, such as low turn-ON voltage, V_T; low ON-resistance, R_{ON}; low leakage current; and low reverse recovery times. Improvements in the reliability of the GaN lateral Schottky diodes will make them the best candidates for high-power applications.

5.4.2 Vertical GaN PiN Diodes

GaN vertical devices have been studied extensively because of their potential to sustain high breakdown voltage without enlarging the chip area [148] and hence increasing the number of dies on a wafer. Also, vertical GaN devices have the potential to achieve a higher power at high temperature (150°C) than the lateral devices, especially for higher breakdown voltages and higher scaling level designs [149]. Vertical devices have high current capability and do not suffer from the thermal management issues associated with thin-film surfaces [150].

The reliability and performance of GaN-based devices depends on the defect density. GaN layers grown on foreign substrates (e.g., Si or SiC) create difficulties for realizing vertical devices because of higher defect densities ($>10^8$–10^9 cm^{-2}) created. For fabricating devices with high breakdown-voltage capability, low leakage current, and high reliability, it is very important that the epitaxial layers have a low defect density. GaN layers grown on a GaN bulk substrate have significantly low defect densities ($<10^6$ cm^{-2}), but the bulk GaN substrates are too expensive and currently have small diameters, which are the main challenges for the commercialization of the GaN vertical devices, although they have shown high performance. Scientists from different universities and companies are conducting ongoing research into improving the quality and increasing the size of the GaN substrates. The research is mostly driven by the optoelectronics industry in two directions: scalability and price reduction. Since there are already multiple suppliers of bulk GaN substrates, the development of GaN vertical power devices will increase soon.

In Fig. 5.20, a cross section of a vertical GaN PiN diode is shown. Similar to Si and SiC PiN diodes, a GaN PiN diode consists of a heavily doped N^+ region, a lightly doped drift region, and a heavily doped P^+ region. When a GaN vertical diode is built on GaN substrate, the substrate has a high electron concentration (1.5–2×10^{18} cm^{-3}) and plays a role as a heavily doped N^+ region. Some researchers have built a GaN vertical diode on a Si substrate. In this case, due to the lattice mismatch and differences in the thermal expansion coefficients between Si and GaN, a buffer layer of AlN/GaN or AlGaN is grown between the substrate and the epitaxial layer. The buffer layer improves the quality of the epitaxial layer grown on top of it. Then, a heavily Si-doped N-GaN layer (2×10^{18} cm^{-3}) is grown.

As mentioned earlier for N-type GaN, metal stacks, such as Ti/Al/Mo/Au, Ti/Al/Pt/Au, and others, can be used to form low-resistivity stable ohmic contacts because of their excellent characteristics. Obtaining stable contacts with low resistivity for P-type GaN is more difficult due to the wide bandgap of GaN. Since the work function of P-type semiconductors is larger and for a wide bandgap it will be pronounced, a metal with a larger work function [151] is required to align the metal and semiconductor Fermi levels. Metal stacks, such as Ni/Au, Pd/Au, Ni/Pd/Au, and others, can be used for these ohmic contacts. An alloy of Ni/Pd/Au is reported to have good ohmic contact with a low specific resistance of 4.5×10^{-6} Ω cm^2 [152].

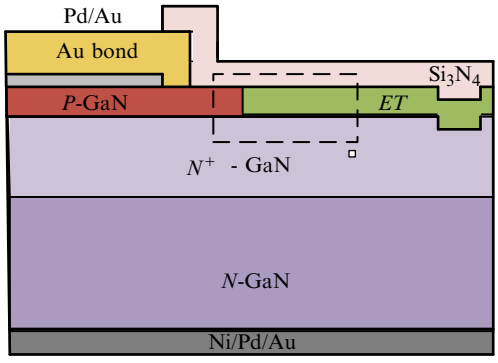


FIG. 5.20 A cross section of a vertical GaN PiN diode.

For the same breakdown voltage, the thickness of the lightly doped drift region N^- of a GaN vertical PiN diode is smaller than the thickness of Si and SiC PiN diodes, while GaN PiN diodes can have a higher doping concentration in the lightly doped drift region than SiC and Si. Shown in Fig. 5.21 are the calculated results for the minimum width of the lightly doped drift region as a function of the doping concentration for a PiN structure for different applied voltages and different

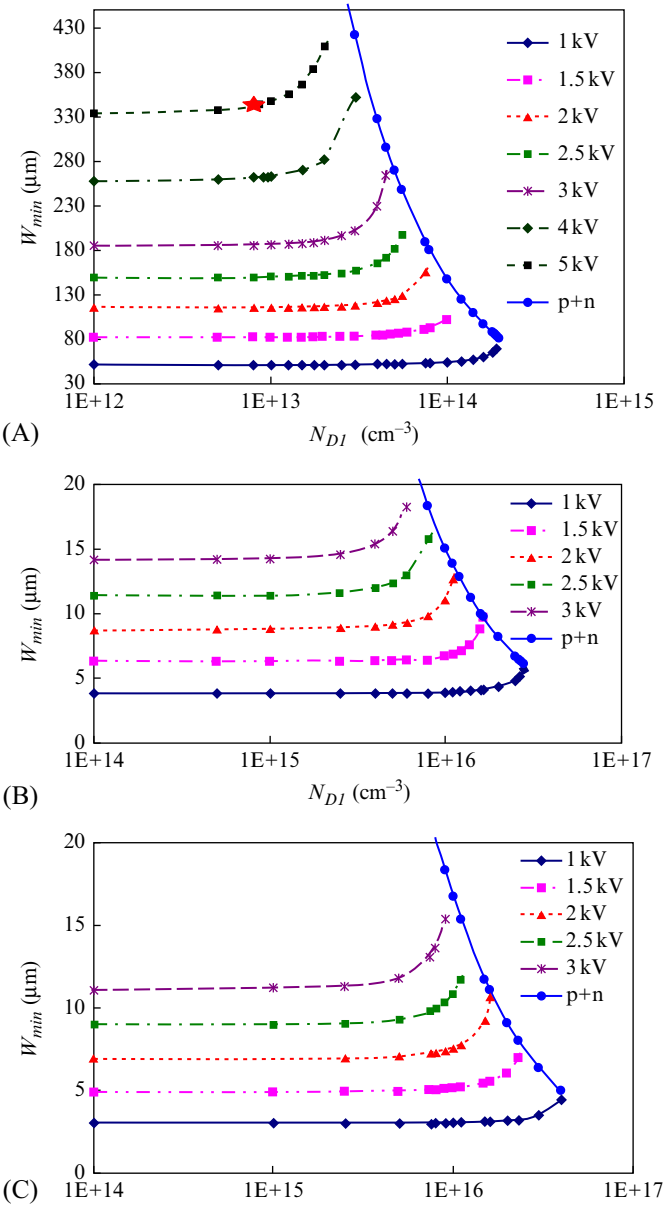


FIG. 5.21 The minimum width of the lightly doped drift region (W_{min}) as a function of doping concentration (N_{D1}) for a P^+N diode and a $P^+N^-N^+$ structure for different applied voltages and different semiconductor materials: (A) Si, (B) 4H-SiC, and (C) GaN.

semiconductor materials: Si, 4H-SiC, and GaN [153]. For a 3 kV GaN diode, the thickness of the lightly doped drift region is ~12 μm, and the doping concentration for this thickness is $\sim 10^{16}$ cm^{-3}. For a SiC device, the thickness and the doping concentration for a 3 kV device are 15 μm and $\sim 7 \times 10^{15}$ cm^{-3}, while for a Si device the thickness and the doping concentration for a 3 kV device are 200 μm and $\sim 8 \times 10^{13}$ cm^{-3}. In [154], a vertical GaN 2.6 kV power diode is described with a lightly doped drift region width and doping concentration of 15 μm and $\sim 8 \times 10^{13}$ cm^{-3}, which support the calculated results given in [153]. On the drift region, a heavily magnesium (Mg)-doped P^+-type GaN layer is grown. The layer's impurity concentration is higher than 2×10^{17} cm^{-3}, depending on the diode design.

A level-3 model introduced in Section 5.3.2.2 can be used for modeling a GaN PiN power diode. The most important parameter for a power GaN PiN diode is the voltage drop, V_{AK}, across it during the conduction state. It is composed of five components, including the voltages across the junctions, J_1 and J_2; the voltage across the two depletion regions, V_{d1} and V_{d2}; and the voltage across the drift region, V_{N^-}:

$$V_{AK} = V_{j1} + V_{j2} - V_{d1} - V_{d2} + V_{N^-} \tag{5.192}$$

Although the lightly doped drift region of a GaN PiN diode is significantly thinner than the lightly doped drift region of a Si PiN diode and the carrier concentration in the drift region is considerably higher in a GaN device, the voltage drop across a 5 kV GaN device, at a current smaller than 50 A, is larger than the voltage drop of a Si diode. The published data for the turn-ON voltage at room temperature of a GaN diode are larger than 3 V [150,155–157]. The reason for the higher turn-ON voltage of a GaN PiN diode is similar to the reason for that in a SiC PiN diode. SiC and GaN are wide bandgap materials, and their intrinsic carrier concentration, n_i, at room temperature is significantly smaller than the carrier concentration of Si. The junction voltage of junction J_1 is a dominant term in Eq. (5.192), especially for the diodes with a breakdown voltage smaller than 5 kV. The junction voltage of junction J_1 is

$$V_{j1} = V_T \mathrm{In}\left(\frac{p_{x1} N_{N^-}}{n_i^2}\right) \tag{5.193}$$

where V_T is the thermal voltage (kT/q), p_{x1} is the excess carrier concentration of the lightly doped drift region at the junction J_1, and N_{N^-} is the doping concentration of the lightly doped drift region. The total junction voltage V_{j12}, which is a sum of the voltages of the junctions J_1 and J_2, V_{j1} and V_{j2}:

$$V_{j12} = V_T \ln\left(\frac{p_{x1} p_{x2}}{n_i^2}\right) \tag{5.194}$$

The total junction voltage, Vj_{12}, does not directly depend on the doping concentration of the lightly doped drift region, N_{N^-}. However, there is a dependency between the boundary values of the excess charge concentrations, p_{x1} and p_{x2}, and the impurity doping level that determines the junction voltage values. Also, the excess carrier concentrations, p_{x1} and p_{x2}, depend on the emitter recombination parameters that can be assumed as constants for calculating the total forward voltage drop.

To obtain the minimum forward voltage drop, V_{AK}, during conduction time, the minimum width of the drift region, corresponding to the minimum doping concentration, should be used. However, the results from the simulation given in [153] do not agree with this simple assertion. Increasing the doping concentration, $\boldsymbol{N_{N^-}}$,for the same breakdown voltage leads to a decrease of V_{AK} to a minimum value, after which further increases in the doping concentration cause an increase in the forward voltage drop. A higher doping concentration, $\boldsymbol{N_{N^-}}$, reduces the injection efficiencies of the higher doped P^+ and N^+ emitters into the drift region and, therefore, decreases the values of the excess carrier densities, p_{x1} and p_{x2}, at the region boundaries. From Eq. (5.194), it can be seen that as the boundary charge concentrations are reduced, the total junction voltage, Vj_{12}, also reduces, as shown in Fig. 5.22.

Although higher doping concentrations, N_{N^-}, lead to a decrease in the values of the excess carrier densities, p_{x1} and p_{x2}, the voltage drop across the drift region, V_{N^-}, has a minimum value. The forward voltage drop, V_{AK}, also has a minimum.

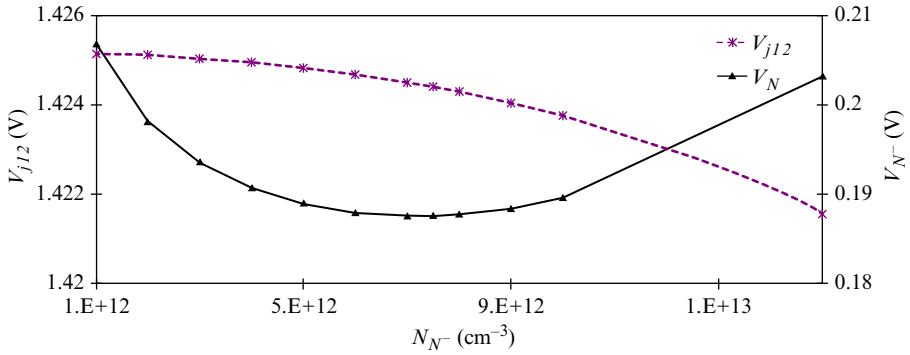


FIG. 5.22 The simulation results of a Si PiN structure for a designed breakdown voltage of 5 kV, given in [148]: the total junction voltage, Vj_{12}, and the voltage drop across the drift region, V_{N^-}, as a function of the doping concentration of the lightly doped drift region, $\boldsymbol{N_{N^-}}$.

The simulation results for optimizing the doping concentration to minimize the forward voltage drop, V_{AK}, of a 5 kV Si PiN diode would lead to a reduction in the forward drop of more than 12%, while for SiC and GaN PiN diodes the reduction in the forward voltage drop for a concentration below 10^{15} cm^{-3} is <1% [153]. Hence, the optimization of the concentration of the lightly doped drift region for SiC and GaN is not necessary.

Fabricating GaN devices with high breakdown voltages requires a low-doped drift region and edge-termination (ET) structures that do not limit device performance. ET plays a key role in determining the device breakdown voltage. The purpose of the ET structures is to spread out the electric field at the edge of the junction such that there is no region with a very high electric field that can damage the device. The lack of good ET reduces the breakdown voltage significantly below the ideal limits due to field crowding at the edges that leads to an avalanche breakdown. To improve device performance, the electric field crowding at the edges should be minimized. Different ET techniques have been used for different types of GaN devices. One of them is smoothing of the equipotential contours at the edge of the device resulting in a manageable electric field [158]. A field-plate structure consisting of a SiN_x passivation layer and a Ti/Au bilayer can be used for the ET [159]. When the metal contact is extended over a surface dielectric layer, for example, SiO_2, the depletion region boundary is extended, and therefore, the electric field crowding is reduced [160]. Another ET technique for reducing electric field crowding is the formation of a P^+ floating ring or guard ring [160]. In [161], a simple ET technique is used to achieve nearly ideal parallel plane breakdown voltage for GaN devices. The technique involves implanting a neutral species on the edges of devices to form a highly resistive, amorphous layer. ET is obtained by using argon implantation, increasing the breakdown voltage of GaN Schottky barrier diodes from 300 V for unterminated diodes to 1650 V after ET.

Improving the quality and the size of the GaN substrate, improving the quality of the epitaxial layers, and choosing the right ET technique will help the device designer to fabricate a high-voltage GaN PiN diode (>10 kV) that will switch quickly and have a smaller forward voltage drop than the Si PiN diode.

5.4.3 GaN JFET

The breakdown voltage of a lateral transistor depends mainly on the channel parameters. In order to maintain low ON-resistance, R_{ON}, the device width and the space between the gate and the drain should be increased, which limits the breakdown voltage to 1 kV and increases the need for more sophisticated device structures for managing the electric field and also increases the device capacitance. In a vertical device, the breakdown voltage depends on the deposition region parameters, and it is easier to scale up for high current and voltage. Vertical devices allow greater power density, lower capacitance, and generally better performance.

Two types of JFETs are considered in this book: a vertical JFET (VJEFT) and a lateral channel JFET with a vertical drift region (LC-VJFET).

5.4.3.1 Vertical JFET

Two cross sections of vertical GaN JFETs are depicted in Fig. 5.23. The first one has a rectangular channel, and the second has trapezoidal channels. Depending on the doping levels and physical dimensions of a VJFET, the transistor can be designed to operate as a normally-ON or normally-OFF device. A normally-OFF device is preferable because it will prevent current from flowing when no voltage is applied to the gate, and therefore, it can be easily utilized in power applications.

A cascode circuit, shown in Fig. 5.24, includes a high-voltage, normally-ON GaN JFET with a low-voltage MOSFET that can operate as a normally-OFF high-voltage device. The high-voltage GaN VJFET is a normally-ON device and has a negative threshold voltage, and the low-voltage MOSFET is capable of blocking ~30 V with a standard power MOSFET threshold voltage. The cascode circuit has the gate-driving characteristics

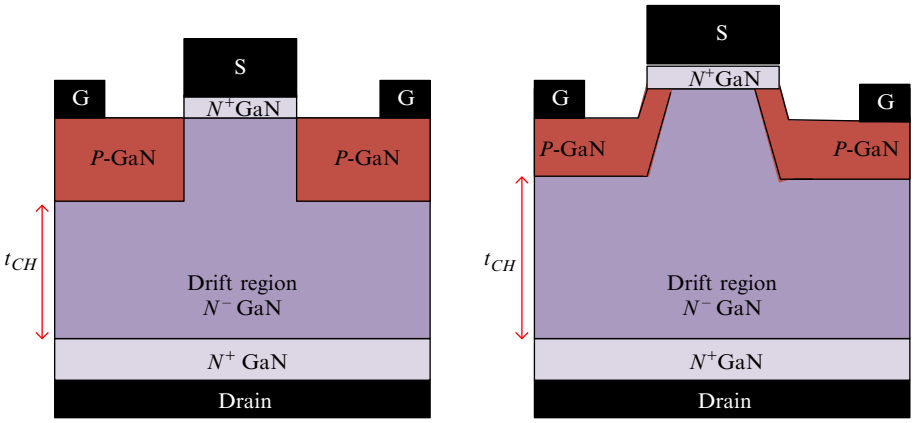


FIG. 5.23 A cross section of a vertical JFET with rectangular and trapezoidal channels.

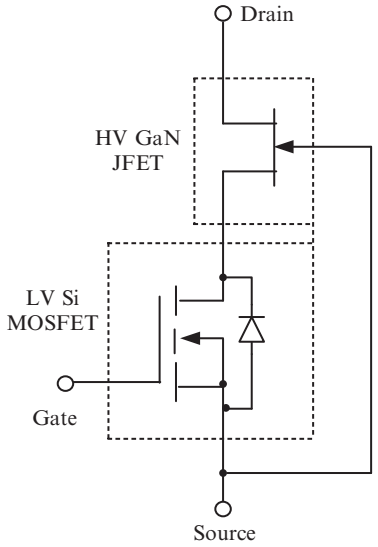


FIG. 5.24 A cascode circuit including a high-voltage JFET and low-voltage MOSFET.

of the standard power MOSFET and the current/voltage capability of the high-voltage GaN VJFET. Since the MOSFET is a low-voltage device, its ON-resistance, R_{DS_ON}, is significantly smaller than in the GaN JFET, and the associated losses will be insignificant.

A VJFET consists of a heavily doped N^+ region, a lightly doped N^- drift region, and a channel region that is formed between two heavily doped P^+ regions. On the top of the channel region is the heavily doped N^+ region. For a normally-OFF device and with no voltage applied to the gates ($V_{GS}=0$), the channel is fully depleted of carriers due to a significantly high doping concentration of the heavily doped P^+ regions and the significantly low doping concentration in the channel. The depletion region width depends on the doping concentrations of the channel and heavily doped P^+ region, N_{CH} and N_P; GaN permittivity, ε; built-in voltage, V_{bi}; and gate-source voltage, V_{GS}:

$$W \approx \frac{\varepsilon}{q}\frac{N_{CH}N_P}{N_{CH}+N_P}(V_{bi}-V_{GS}) \tag{5.195}$$

The built-in voltage is calculated by the equation:

$$V_{bi}=\frac{kT}{q}ln\left(\frac{N_{CH}N_P}{n_i^2}\right) \tag{5.196}$$

where k *is* Boltzmann's constant, T is the temperature in Kelvin, q is unit electric charge, and n_i is the GaN intrinsic carrier concentration. If a positive voltage is applied to the gates, the depletion region width decreases, creating no resistive path for the current, and the current passes through the channel from the drain to the source.

For a normally-ON device and no voltage applied to the gates ($V_{GS}=0$), the channel is not depleted, and the current passes through the channel from the drain to the source. When a negative voltage, with a magnitude higher than the threshold voltage, is applied to the gate, the depletion region is extended and prevents current from passing through the channel.

When a GaN VJFET is built on GaN substrate, the substrate has high electron concentration and plays the role as a heavily doped N^+ region. Other substrates, such as Si or SiC, can be used for building of a GaN VJFET.

Epitaxial layers are grown on the top of the GaN substrate or the buffer layer for devices made with other substrates. The VJFET GaN epitaxial layers can have nonuniform doping concentration as a function of the thickness of the different layers, which can be used for optimizing a device's performance [162]. The drift region thickness and the doping concentration are designed to carry the majority of the drain-source voltage, V_{DS}. The drift region concentration can be in the range of 10^{14}–10^{16} cm^{-3}. The gates are formed on the top of the heavily doped P^+ regions, whose thickness, t_{CH}, determines the channel thickness. The doping concentration in the channel can be equal to or less than the doping concentration of the drift region. The doping concentration in the channel depends on the desired threshold voltage of the VJFET.

In Fig. 5.23, the channel has a rectangular shape. There are JFETs where the channels can be designed to have a trapezoidal shape. The trapezoidal-shaped channel can improve the performance by enabling better control of the electric field near the location where the channel sidewall and the upper surface meet [162]. The width of the channel, W_{CH}, for a rectangular channel or the bottom base for a trapezoidal-shaped channel can vary depending on numerous factors, such as desired functionality (normally-ON or normally-OFF device) and the channel doping concentration. The width and the thickness of the channel, W_{CH} and t_{CH}, should be optimized so that a very small leakage current flows from the source to the drain while maintaining a low ON-state resistance, R_{ON}.

Simulation results given in [163] showed that the ON-state resistance, R_{ON}, can be reduced by increasing the channel doping concentration and width, but in this case, the breakdown voltage is reduced, a positive threshold voltage is compromised, and a normally-OFF operation is hard to achieve. The threshold voltage, V_T, is very sensitive to the channel width, W_{CH}. In order to achieve a positive threshold voltage, V_T, the channel width should be smaller than 1 μm, which leads to a high ON-state resistance, R_{ON}. To obtain a better trade-off between the threshold voltage, V_T, and ON-state resistance, R_{ON}, a lateral channel JFET with a vertical drift region is proposed.

5.4.3.2 Lateral Channel JFET With Vertical Drift Region

A cross section of a lateral channel GaN JFET with a vertical drift region (LC VJFET) is shown in Fig. 5.25. Similar to VJFET, the doping levels and physical dimensions of an LC VJFET determine the transistor functionality to operate as a normally-ON or normally-OFF device. A normally-OFF device

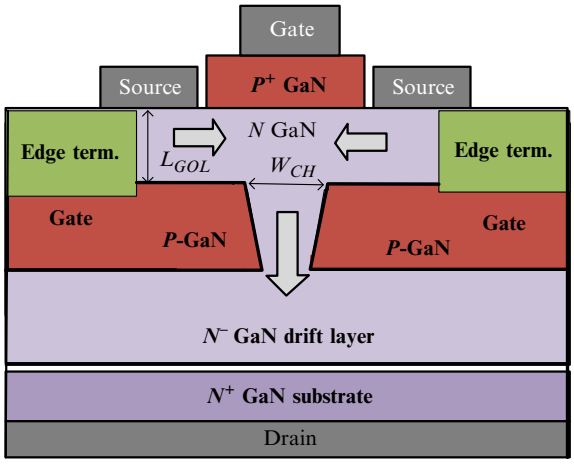


FIG. 5.25 A cross section of a lateral channel JFET with a vertical drift region.

is preferable, but the cascode configuration shown in Fig. 5.24 has the gate-driving characteristic of the low-voltage MOSFET and the current/voltage capability of the high-voltage LC VJFET, which can be used for a normally-ON device.

The LC VJFET has three regions of interest. First is the core of the device, which includes the device channel and the gate region. The second region includes the lightly doped drift region and the substrate, and the third region is the edge termination and the isolation region.

A GaN LC VJFET can be built on a heavily doped GaN substrate, but other substrates, such as Si or SiC, can also be used. However, in this case, a buffer layer from AlN/GaN, AlGaN, or other suitable materials should be grown between the substrate and the epitaxial layer to improve the quality of the epitaxial layer grown on top of it. The breakdown voltage of an LC VJFET is determined by the doping concentration and thickness of the lightly doped drift region and also the proper edge-termination techniques. For a kV-rated device, the doping concentration of the lightly doped drift region is in the range of 10^{15}–10^{16} cm^{-3}. The lightly doped drift region provides a region through which current flows from the drain to source during the ON-state, but during the OFF-state, the drift region provides a region for supporting the electric field by the voltage gradient between the source or gate and the drain [164].

The channel of the LC-VJFET is composed of two parts: a vertical and a lateral conductive region. A blocking *P*-type GaN layer, with a significantly high impurity concentration in the range of 10^{17}–10^{19} cm^{-3}, is used to form the two regions. The blocking layer supports the vertical electric field and causes the current to flow in the lateral area of the channel. The length of the overlap, L_{GOL}, between the gate and the blocking layer is an important parameter. This is exactly the effective gate that modulates the lateral channel width and changes the conductivity of the channel. When the length of the overlap, L_{GOL}, is smaller than the optimum value, leakage current in the device increases as the channel is not fully pinched OFF, and some electrons flow from the source to the drain. But increasing the length of the overlap, L_{GOL}, more than the optimum value causes the ON-state resistance of the device to increase [163].

The vertical channel region is a continuation of the lightly doped drift region. The vertical channel thickness and doping concentration should be optimized with two constraints: minimizing the LC-VJFET ON-resistance when the device is turned ON and providing proper pinch-OFF so that no current passes through the channel when the device is turned OFF. The channel width, W_{CH}, is also an important design parameter that determines the functionality of the device as a normally-ON or normally-OFF design. If the channel width, W_{CH}, is significantly large, the path of the current from the drain to the source will be low resistance, but in this circumstance, pinch-OFF of the channel is more difficult to achieve.

On the top of the channel, a heavily doped P^+-type GaN layer is deposited and patterned to form the gate. The blocking *P*-type GaN layer, together with the gate, can control the device by the PN junctions formed with the *N*-type channel. In some designs, the gate and the blocking layer are electrically tied to form a buried *P*-type gate.

The edge-termination scheme used in the transistors is similar to those schemes used in PiN junction diodes. The potential applied to the top metal is spread over a distance that is typically greater than the thickness of the lightly doped drift region. For this purpose, two separate implant steps are used. Smoothing the equipotential contours at the device edges results in better management of the electric field on the device surface and prevents the device from breaking down prematurely [165]. In this case, if a breakdown occurs, it will be due to an avalanche breakdown.

The operation of an LC-VJFET depends on the design. For a normally-OFF device, where no voltage is applied to the gates ($V_{GS}=0$), the channel is fully depleted of carriers due to a significantly high doping concentration of the heavily doped P^+ gate and the blocking *P*-type GaN layer from one side and a significantly low doping concentration in the channel from the other side. Two depletion regions are formed: one from the *PN* junction of the P^+ gate and the *N*-channel and the second one from the blocking *P*-type GaN layer and the *N*-channel. The two depletion widths can be calculated using Eq. (5.195) by substituting the corresponding doped concentrations. The total depletion width, *W*, is a sum of the depletion width of the two junctions. When a positive voltage is applied to the gates, the depletion width, *W*, decreases, and current passes through the channel from the drain to the source. For a normally-ON device with no voltage applied to the gates ($V_{GS}=0$), the channel is not depleted, and the current flows through the channel from the drain to the source. When a negative voltage, with a magnitude higher than the threshold voltage, is applied to the gate, the two depletion regions are expanded and prevent current from passing through the channel.

The simulation results given in [163] show that there is a higher degree of coupling between the ON-resistance, R_{ON}, and the threshold voltage, V_T, in the LC VJFET than in the VJFET. Therefore, a low ON-state resistance can be obtained with a thinner and more highly doped *N*-GaN channel.

5.4.4 GaN MOSFET

In the last 10 years, research on the design, fabrication, and characterization of high-voltage GaN MOSFETs has been based on both lateral and vertical structures: the fabrication process for a lateral high-voltage MOSFET is simpler than the vertical MOSFET since a thick, lightly doped drift region is necessary for a vertical structure. For the same breakdown voltage, a lateral device has a larger area than a vertical device. Therefore, the chip size of a lateral MOSFET is bigger. However, a Si substrate can be used for growth of lateral devices, which are larger and cheaper, while GaN substrates are normally used for vertical MOSFETs, which are smaller and more expensive. Other substrates, such as Si or SiC can also be used for vertical devices, but a buffer layer should be grown between the substrate and the epitaxial layer to improve the quality of the epitaxial layer, which increases the device cost.

5.4.4.1 Vertical Trench MOSFET

Fig. 5.26 shows a cross section of a high-voltage GaN vertical trench MOSFET. Most of the vertical GaN high-voltage MOSFETs are built on a low-defect-density GaN substrate, which is the MOSFET drain. The substrate doping concentration is higher than 10^{18} cm^{-3}. A lightly doped N^- drift region is grown on the top of the substrate by metal-organic vapor deposition. The doping concentration of the drift region is in the range of 10^{14}–10^{16} cm^{-3}, and its thickness depends on the desired breakdown voltage. The area of the drift region depends on its thickness. It should be chosen to allow spreading of the current in the drift region, thereby decreasing the drift region ON-resistance. The value of the thickness and the doping concentration of the lightly doped drift region can be optimized so that the sum of the conduction and the switching losses of the device can be minimized.

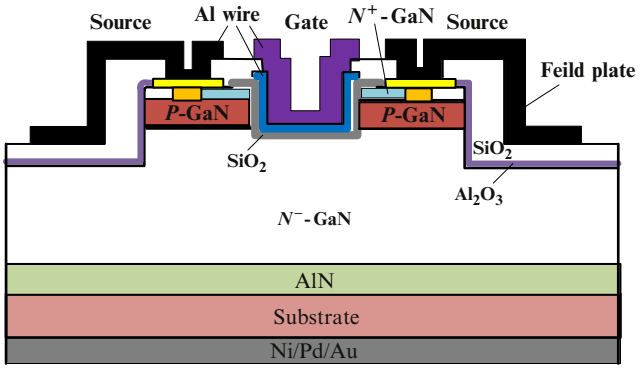


FIG. 5.26 A cross section of a vertical trench MOSFET.

A *P*-type base layer with a thickness smaller than 1 μm is grown on the top of the drift region. The thickness of the *P*-layer is the channel length of the device or the effective gate of the device. The doping concentration of the base is higher than the drift region, and it is in the range of 10^{17}–10^{19} cm^{-3}. On the top of the base layer, a selective area regrowth of a heavily doped N^+-type layer is grown to form the MOSFET source. SiO_2 can be used as the regrowth mask. The doping concentration of the N^+-type layer is higher than 3×10^{18} cm^{-3}, and the thickness is smaller than 0.5 μm. Usually for GaN devices, Si is used as the dopant for the formation of *N*-type layers, and Mg is used for *P*-type.

The gate trench is then formed by etching part of the two MOSFET layers, *P* base and N^+ source. A SiO_2 layer, as a dielectric interlayer, is deposited on the sidewall and the bottom of the trench by plasma-enhanced chemical vapor deposition, and then, the metal is deposited to form the gate electrode. The vertical sidewall of the trench should be well smoothed and cleaned to achieve high inversion layer mobility and, therefore, low resistivity of the channel [38]. Also, the trench bottom plays a crucial role in achieving superior electric performance and highly reliable operation. Therefore, the trench bottom should be a little bit rounded, which will reduce the P-well pinching effect, and as a result, the pinching resistance under the gate-drain area is decreased [166].

To improve the OFF-state characteristic, such as the breakdown voltage of a trench MOSFET, a field-plate edge-termination technique can be used to reduce the electric field at the edge of the *PN* junction around the isolation mesa periphery [167]. The field plate consists of the extended wiring electrode for the source electrode. The field-plate electrode completely overlaps the *PN* junction from the side, and therefore, the potential crowding at the edge of the *PN* junction is effectively reduced. While an improvement of the ON-state characteristic, such as the ON-resistance can be achieved by reducing the cell pitch size, improving the dielectric/semiconductor interface quality, and optimizing the drift layer growth condition which will enhance the electron mobility.

The operation of a high-voltage GaN trench MOSFET is similar to the operation of Si and SiC trench MOSFETs. When a positive voltage higher than the threshold voltage is applied between the gate and the source of the device, an *N*-channel region is formed on the surface of the *P* base that provides a conducting path between the source and drain terminals. If the gate to source voltage is below the threshold voltage, the transistor is turned off, and only a very small leakage current is passing from the drain to the source of the transistor. In theory, the threshold voltage of a MOSFET is defined as the voltage applied between the gate and source that creates an inversion layer of minority carriers with a concentration higher than the base. According to [168], the threshold voltage is

$$V_{th} = \Phi_S + \frac{\varepsilon_{GaN}}{\varepsilon_{SiO_2}} t_{SiO_2} \sqrt{\frac{2qN_P}{\varepsilon_{GaN}\varepsilon_0}\Phi_S} \tag{5.197}$$

where ε_{GaN} and ε_{SiO_2} are the permittivity of GaN and SiO_2, respectively; t_{SiO_2} is the thickness of the SiO_2; and N_P is the doping concentration of the base. The surface potential at the P base is Φ_S. At the deposition-inversion transition point, the surface potential is

$$\Phi_S = 2\Phi_F = \frac{2kT}{q} \ln\left(\frac{N_P}{n_i}\right) \tag{5.198}$$

For the same doping concentration of the P base and SiO_2 layer thickness, the calculated threshold voltage for a GaN device should be larger than the threshold voltages of SiC and Si devices because of the significantly low intrinsic carrier concentration of GaN. The simulation result for the threshold voltage of a trench GaN MOSFET (P-base doping concentration 3×10^{19} cm^{-3}) obtained from a one-dimensional, self-consistent Schrödinger-Poisson solver is 26 V, while the experimental result for the same device is significantly lower at 8 V [169]. Other researchers, [170–172], have also reported low experimental threshold voltage values compared with theoretical values. Differences between the simulation and experimental results can be due to the sidewall etch damage of the P base, which can cause nitrogen vacancies to form and behave as donors [169]. Research about decreasing the sidewall etch damage, better smoothing, and cleaning after sidewall etching is being conducted, which will increase the threshold voltage and provide better noise immunity to prevent false turn-on.

In 2016, at the 28th International Symposium on Power Semiconductor Devices and ICs, a state-of-the-art GaN trench MOSFET, with a breakdown voltage of 1.6 kV and a high current operation exceeding 10 A for a single-cell device, was reported [167]. The breakdown voltage of the device was improved from 1.2 to 1.6 kV by applying a field-plate edge-termination technique around the isolation mesa of the transistor. The specific ON-resistance, R_{ON}, of the single cell, measured when a gate-source voltage, V_{GS}, of 40 V was applied, was 2.7 mΩ cm^2. The threshold voltage of the trench MOSFET was reported to be 3.5 V. The authors also showed the switching characteristics for a double-pulse switching experiment (see Fig. 5.27). From the switching characteristics, the rise and fall time, t_r and t_f, were determined to be 19 and 10 ns, respectively, when the supply voltage, V_{DD}, was 400 V and the drain current, I_D, was around 10–14 A. Also, the turn-on and turn-off switching losses were calculated to be 90 and 12 μJ, respectively, which suggests that the fabricated vertical GaN trench MOSFETs are suitable for use in high-power applications with high-frequency switching.

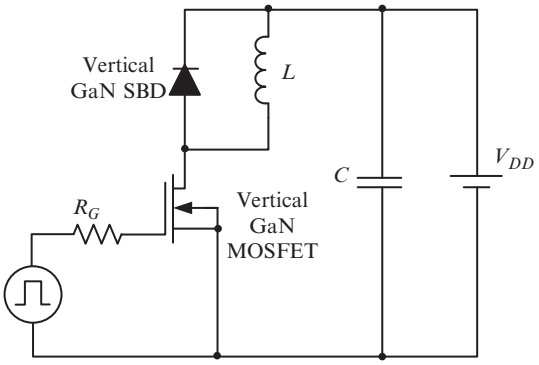


FIG. 5.27 Schematic circuit diagram for double-pulse switching measurement using the fabricated vertical GaN MOSFET and the internally developed vertical GaN SBD [162].

5.4.4.2 Lateral MOSFET

Lateral MOSFETs have a significantly simpler structure than the vertical ones because during fabrication, no heavy etching is used for the gate and no thick, lightly doped drift region is grown. Also, the three terminals, the source, gate, and drain, are placed on the top surface, which is suitable for power-integrated circuits where the power transistor is monolithically integrated with control circuits on the same chip. However, for the same blocking voltage, the length of the channel of a lateral MOSFET is longer, and therefore, the area of the device is larger than the area of a vertical trench MOSFET. Similar to the vertical MOSFET, the lateral MOSFET is normally an OFF device.

A cross section of a GaN lateral MOSFET is shown in Fig. 5.28. Different substrates, such as sapphire, SiC, and GaN, have been used for fabricating lateral MOSFETs. A P-type Mg-doped GaN layer is grown by metal-organic chemical vapor deposition on top of the substrate. For better growth of the P-doped layer, a buffer layer between the substrate and the P layer is grown. A SiO_2 thin layer is grown on top of the P layer to form the MOS structure of the transistor and to suppress any damage or pollution due to ion

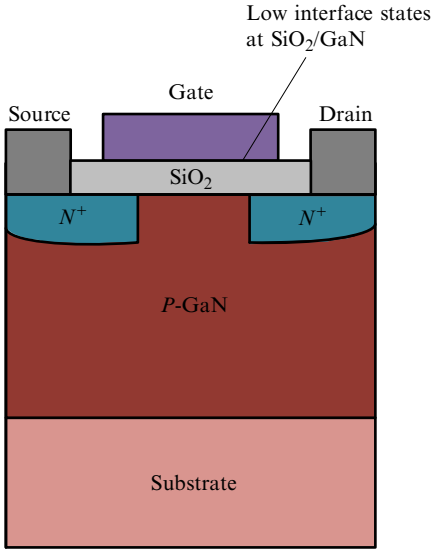


FIG. 5.28 A cross section of a GaN lateral MOSFET.

implantation. The ion implantation is used to place Si ions in the P layer and to form heavily doped N^+ source and drain regions. In the end, low-resistance contact layers are formed on the drain, source, and the gate.

The breakdown of a lateral MOSFET is mainly determined by the thickness of the SiO_2 layer. Since the drain has a high doping concentration, the voltage drop of the drain region is significantly smaller. Therefore, the potential of the region of the drain under the gate is approximately equal to the applied voltage on the drain. When the gate-source voltage is smaller than the threshold voltage and the drain-source voltage is significantly high, a breakdown can occur in the gate oxide. A schematic of a lateral GaN MOSFET during the OFF-state and its potential and electric field in function of the position is shown in Fig. 5.29. During the OFF-state, the gate and source are connected to the ground, and high voltage is applied to the drain with respect to the source. The electric field between the drain and the gate is significantly high because of the small thickness of the SiO_2 layer, while the channel length is significantly larger. Therefore, the electric field between the drain and source is smaller. Also, the resistance of the SiO_2 layer is larger than the channel resistance. For these reasons, almost all of the electric field is concentrated on the gate oxide, a result of the breakdown near point 1 in Fig. 5.29 [173].

The electric field in the region between the gate and the drain is significantly higher and, therefore, limits the voltage applied between the drain and the source. To spread the electric field and decrease its value in the region between the gate and the drain, a lightly doped N^- layer, known as the reduced surface field (RESURF) layer, is used by different scientific groups to increase the breakdown voltage of a lateral device. The RESURF concept was introduced by Appels and Vaes for the first time [174]. A RESURF layer increases the breakdown voltage of lateral MOSFETs and increases the ON-state resistance since the layer should be long and lightly doped. Another aspect of a long, lateral drift layer is the additional required chip area, which increases the cost of the devices. For a given breakdown voltage, the optimal parameters of a RESURF layer, the length and doping concentration, should be determined. A trade-off between blocking voltage and ON-state resistance should be found.

A lateral GaN MOSFET with a RESURF layer during the OFF-state and its potential and electric field as a function of the position is shown in Fig. 5.30. During the OFF-state, a big part of the electric field of the MOSFET with a RESURF layer is concentrated on the two sides of the RESURF layer, and some part is in the RESURF layer. Therefore, for the same breakdown voltage, the electric field in the gate oxide layer for a MOSFET with a RESURF layer will be significantly smaller than the electric field in the gate oxide layer for a conventional MOSFET. To ensure long-term reliability of a MOSFET, the electric field in the gate oxide layer should be kept below 3 MV cm^{-1}. A lateral GaN MOSFET with RESURF, with a high blocking capability of 1550 V and an operation current of 2.5 A, is reported in [172]. To further reduce the surface electric field and maintain a high breakdown voltage, two RESURF regions are required. A lateral GaN with two RESURF regions is shown in Fig. 5.31. The RESURF1 region is near the gate and has a low implant dose. Lowering the implant dose in RESURF1 will reduce the electric field of the oxide near to the gate. The RESURF2 region is near the drain and has a high implant dose. The higher implant dose in the RESURF2 region will support high breakdown voltage. In [175], an enhancement mode N-channel lateral GaN high-voltage MOSFET with two RESURF regions is presented, with a breakdown voltage of 2.5 kV and a specific on-resistance of 30 mΩ cm^{-2}. Further

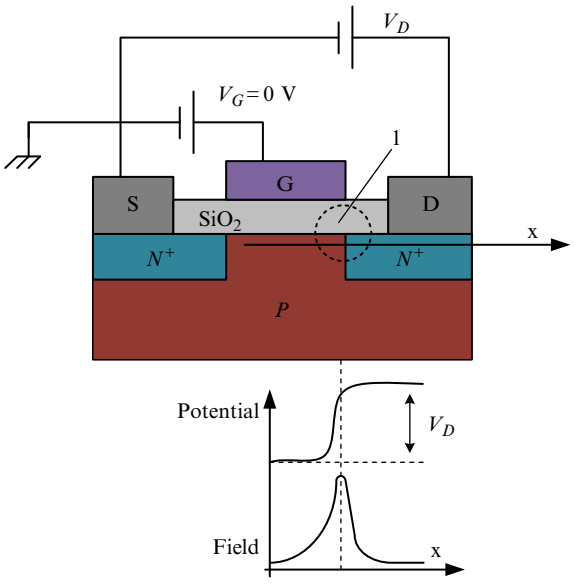


FIG. 5.29 A schematic of a lateral GaN MOSFET, the potential and electric field during the OFF-state.

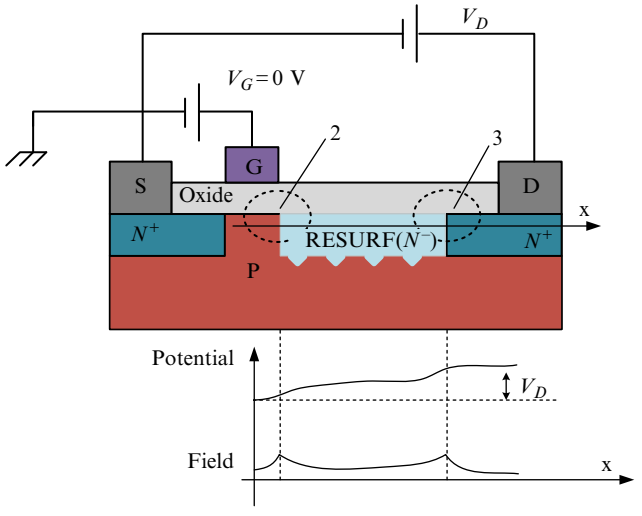


FIG. 5.30 A schematic of a GaN lateral MOSFET with a RESURF layer, the potential and electric field during the OFF-state.

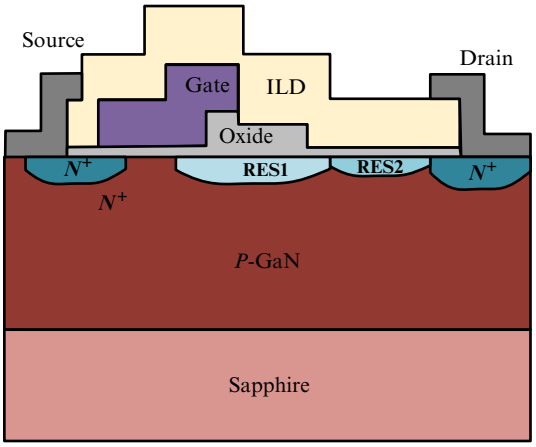


FIG. 5.31 A cross section of a GaN lateral MOSFET with two RESURF regions.

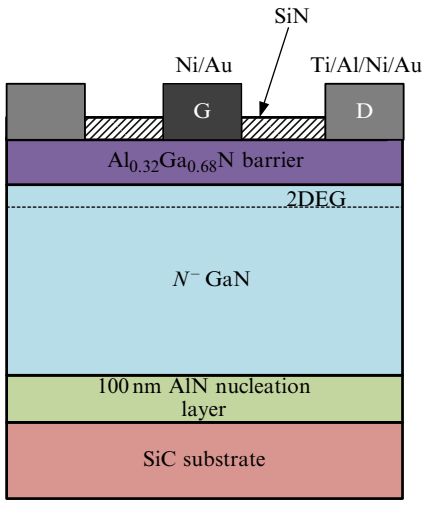


FIG. 5.32 A cross section of a conventional GaN HEMT.

improvement of lateral GaN MOSFETs can be accomplished by improving the quality of the SiO_2/GaN interface and reducing the resistance of the contacts. If the SiO_2/GaN interface has poor quality, the electrons passing through the channel are captured at interface states leading to a decrease in electron mobility and, therefore, an increase in channel resistance. Annealing at temperatures higher than 900°C after depositing SiO_2 has been used to decrease interface state density [173,176,177].

Simulation results for GaN MOSFET devices of similar dimension with a RESURF region (field-plate structure) and a GaN HEMT are given in [177]. From the simulation results, it is concluded that both devices are capable of producing similar ON-state modes of operation and achieve similar effective mobility at equivalently larger electric fields. However, during subthreshold operation, the GaN MOSFET is shown to contain a much lower carrier concentration than the GaN heterostructure field-effect transistor (HFET). As a result, the breakdown avalanche effect in the GaN MOSFET is roughly five times larger than the GaN HFET for devices of similar dimensions, 3500 and 600 V, respectively. Therefore, implementing the MOS structure with the high quality of the SiO_2/GaN interface can potentially resolve fundamental constraints for high-voltage power applications caused by current device architects.

5.4.5 GaN HEMT

5.4.5.1 GaN HEMT Structure

A GaN HEMT is a field-effect transistor in which two layers of different bandgaps and polarizations (GaN and AlGaN) are grown upon one another forming a heterojunction. As a consequence, in the vicinity of the heterojunction, positive charge is induced at the interface due to both spontaneous and piezoelectric type of polarization. Free electrons are transferred from the AlGaN layer, having higher conduction band energy, to the GaN layer, where the conduction band energy is lower, thus occupying a lower energy state and compensating for the induced positive charge [178]. The number of electrons is larger, especially if AlGaN is doped with impurities. Accumulated electrons along the heterojunction in a quantum well are usually referred to as two-dimensional electron gas (2DEG). The 2DEG is located in the channel of the HEMT, where current flows between the drain and the source controlled by the gate.

A cross section of a conventional GaN HEMT is shown in Fig. 5.32. HEMTs have been successfully grown on Si [179], sapphire [180], SiC [181], and GaN [182] substrates. SiC and sapphire substrates were the first used for HEMTs because of the existing experience in the light-emitting diode (LED) industry. However, successful growth of GaN HEMTs on Si substrates with parameters similar to HEMTs on SiC substrate has been reported lately. This is attractive to industry since Si substrates are available in large sizes and at low cost. Since SiC has three times the thermal conductivity of Si, HEMT transistors for low-power applications can be built on Si substrates, while for high-power applications, SiC substrates are preferred. The epitaxial layer grown on GaN substrates will not have a mismatch problem, but these substrates are extremely costly and small in size.

For HEMTs grown on foreign substrates, an intermediate, nucleation, or buffer layer is essential to the growth of quality GaN on the substrate. The morphology and crystal quality of a buffer layer play a critical role in determining the quality of epitaxial growth [183]. Aluminum nitride can be used as a nucleation layer. Metal-organic chemical vapor deposition and metal-organic molecular beam epitaxy methods can be used to form the AlN buffer layer. In [184], it is shown that there is no distinct difference between the GaN grown on a buffer layer obtained by the two methods.

The GaN epilayer grown on the top of the buffer layer is known as a channel layer because a channel is formed within.

The channel layer is grown mostly by metal-organic chemical vapor deposition along the [0001] direction to benefit from the spontaneous polarization within the GaN wurtzite crystal. The temperature for growing the GaN epilayer is also important to the quality of the layer. As the temperature increases, the defect density and surface roughness decreases, which may be attributed to the improvement in the surface mobility and activities of source spaces on the substrate [184].

On the top of the channel layer, a barrier layer with a higher bandgap and lower electron affinity, compared with the GaN channel layer, is grown. The buffer layer can be fabricated with a group-III nitride material, such as $Al_xGa_yIn_{1-x-y}N$, where $0 \leqq x \leqq 1$, $0 \leqq y \leqq 1$ and $x+y \leqq 1$ [185]. The thickness of the AlGaN barrier layer and the aluminum composition can be optimized so that a significant carrier concentration is induced and a 2DEG can be formed.

A passivation layer is deposited on the top of the barrier layer between the gate and the source and the second passivation layer between the drain and the gate. The layers may be initially formed as a single layer that is subsequently etched through to form the gate [185]. Different dielectric materials can be used, such as SiN, SiO_2, Si, Ge, MgO_x, MgN_x, ZnO, SiN_X, and SiO_x, but usually, SiN is used. The deposition temperature and post-annealing temperature of the passivation layer are important for controlling dynamic ON-state resistance degradation. The results given in [186] indicate that the SiN/AlGaN interface trap density is reduced by increasing the deposition temperature and also by increasing the postannealing temperature. Therefore, the current collapse in terms of dynamic ON-state resistance is also reduced.

As illustrated in Fig. 5.32, a conventional AlGaN/GaN HEMT has typically been fabricated with coplanar metal contacts. The source and drain electrodes are ohmic contacts providing low resistance and nonrectifying behavior, while the gate contact is intended to be a nonohmic Schottky barrier contact that controls the carrier concentration in the channel and blocks the current at large reverse voltages. Since the Schottky gate electrode and the 2DEG are separated by the AlGaN layer, the gate leakage current should be suppressed, but a relatively large gate leakage current is usually observed in the devices due to the defects near or at the surface of the AlGaN layer. The defects are formed during the epitaxial layer growth and by interface reaction between the metal and AlGaN layers interacting due to thermal treatments during the fabrication processes. Different materials have been used to create Schottky gate electrodes: Ni, Cu, Pt, and W. Pure metals have poor thermal stability on the AlGaN layer, while using electrodes with compound nitrides, such as TiN, the gate leakage current and the current collapse are suppressed to some extent. A characterization and comparison of poly-Si and TiN gate electrodes have shown advantages in reducing the leakage current and robustness against reverse-bias stressing of the poly-Si gate electrode [187].

Forming all three contacts on the same epitaxial layer may result in compromises between these characteristics. Therefore, there is a trade-off in device design, when selecting the doping and composition of the AlGaN barrier layer, between optimizing the source and drain ohmic contacts while optimizing the nonohmic gate contact [185]. Furthermore, high-power HEMTs should be optimized to provide as much current-carrying capability as possible to the region under the gate electrode while allowing the gate to block as high voltage as possible. Hence, it may be useful to have differences in the regions between the source and gate, under the gate, and between the gate and drain in order to modify the amount of energy band bending. Modifying the band bending will change the amount of the sheet region charge and the electric field profile within the device.

To improve electric performance together with reliability, new advanced structures have been designed and characterized. Introducing a field plate between the gate and drain electrodes enables electric field modulation. As a result, the electric field profile is reshaped, and the electric field is spread along the device's channel. Under the field plate, a depletion zone is formed so that the maximum peak value of the electric field at the drain side of the gate edge is reduced. Therefore, using a field-plate structure increases the device breakdown voltage, since the maximum electric field is distributed across the region among the gate and drain [188].

The phenomenon known as current collapse is associated with surface states in GaN-based HEMTs. It is caused by electrons trapped by defects in the GaN layer and the interface between the passivation film and the AlGaN barrier layer. Since, the electric field at the gate edge has a maximum value, it strongly affects the current collapse due to the acceleration of the electrons in the channel. The ON-resistance increase caused by the current collapse phenomena strongly depends on the gate-edge electric field. The results given in [189] show that the ON-state resistance increase caused by the current collapse phenomena is dramatically reduced by a field plate since the gate-edge electric field is reduced by the field-plate electrode.

The electron mobility in the 2DEG of an AlGaN/GaN heterostructure is an important transport parameter that characterizes the quality of the structure and determines the HEMT performance [190]. The 2DEG mobility is limited by a combination of various scattering mechanisms such as background impurities, polarization effects, degeneracy, interface roughness scattering, dislocations, scattering by acoustic and optical phonons, remote modulation doping scattering, and alloy disorder [191] and [192].

The electron mobility in the 2DEG is a function of the sheet electron density, N_S, at the heterointerface over a wide temperature range. It increases with an increase in the sheet electron density, N_s, up to a maximum value and decreases with further increases in the density, N_S. At a high sheet electron density in AlGaN/GaN heterostructures, the electrons spill from the quantum well near the heterointerface and occupy the delocalized states in the channel, leading to a reduction of the electron mobility. In this case, less effective screening and more

pronounced ionized impurity scattering were observed when electrons occupied a much wider doped region near the heterointerface [193].

The sheet electron density near the AlGaN/GaN heterointerface is mainly contributed by the electrons induced by the doped AlGaN barrier and from the electrons generated by the piezoelectric effect. The sheet density of 2DEG is expressed as [194]:

$$N_S = \frac{1}{q}\left(\sigma_{AlGaN} - \frac{\varepsilon_{AlGaN}}{d_{AlGaN}}\Delta V_{AlGaN}\right) \tag{5.199}$$

where σ_{AlGaN} is the sheet charge density that is induced by AlGaN polarization, q is the electron charge, and ε_{AlGaN} and d_{AlGaN} are the dielectric constant and the thickness of the AlGaN barrier. The potential drop, $\Delta V_{AlGaN,}$ can be calculated as

$$\Delta V_{AlGaN} = q\Phi_b - E_F - \Delta E_C \tag{5.200}$$

where Φ_b is the surface barrier height, E_F is the Fermi level position with respect to the GaN conduction band edge at the AlGaN/GaN interface, and ΔE_C is the conduction band discontinuity between GaN and AlGaN, as shown in Fig. 5.33.

To decrease the sheet electron density, N_s, and improve the performance of the HEMT, a GaN capping layer placed between the barrier layer of AlGaN and the passivation layer of SiN is deposited as shown in Fig. 5.34. Strong polarization-induced electric fields are present in the AlGaN buffer layer and in the GaN capping layer that affect the 2DEC sheet density, depending on the thickness of the GaN capping layer. Experimental results given in [195] and the simulation results given in [196] show that the presence of a GaN capping layer results in a monotonic decrease of the sheet electron density with increases in the capping layer thickness. Decreasing the 2DEG sheet density results in modification of the electron scattering mechanisms and, therefore, modification in the mobility too. The experimental and simulation results show that as the thickness of the GaN capping layer increases, the electron mobility increases monotonically to a maximum point, where further increases in the capping layer thickness will cause the mobility to decrease slightly and eventually saturate [195] and [196].

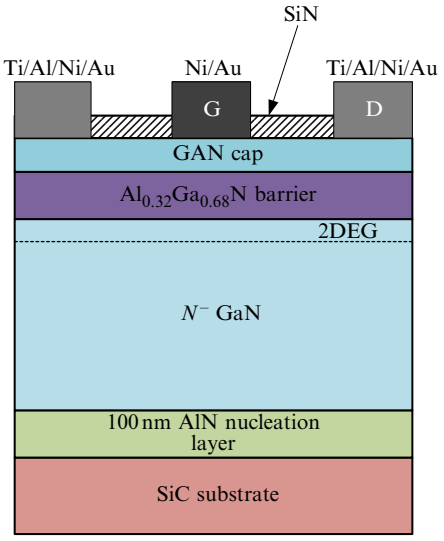


FIG. 5.34 A cross section of an advanced GaN HEMT structure.

The 2DEG sheet resistance of the GaN/AlGaN/GaN structure can be calculated by the following equation [194]:

$$N_S = \frac{d_{GaN}\sigma_{GaN} + d_{AlGaN}\sigma_{AlGaN}}{q(d_{GaN} + d_{AlGaN})} - \frac{\varepsilon_{GaN}}{q}(q\Phi_b + E_F) \tag{5.201}$$

where σ_{GaN} is the sheet charge density that is induced by the GaN polarization and ε_{GaN} and d_{GaN} are dielectric constant and the thickness of the GaN capping layer, respectively. The surface barrier height, $\Phi_{b,}$ and the Fermi level position, $E_{F,}$ are shown in Fig. 5.35.

To achieve better HEMT performance, a thin AlN (~1 nm) interlayer at the AlGaN/GaN interface is added in some advanced structures. The insertion of the thin AlN interlayer suppresses the penetration of the wave function into the barrier and effectively removes alloy scattering and pushes out most of

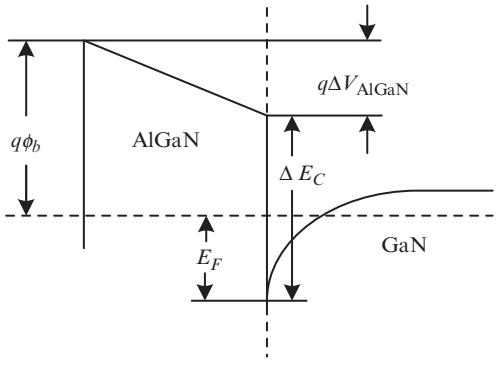


FIG. 5.33 Conduction band diagram of an AlGaN/GaN heterostructure [195].

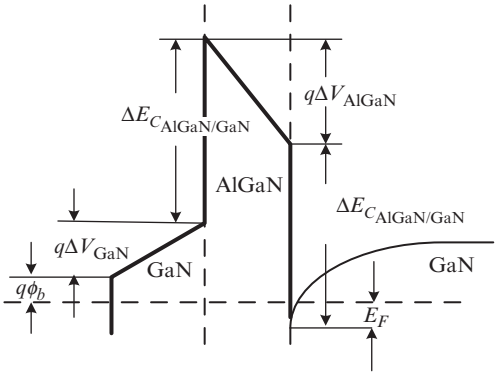


FIG. 5.35 Conduction band diagram of a GaN/AlGaN/GaN heterostructure [195].

the 2DEG from the barrier. The small finite part that still penetrates the barrier is not affected by the allow scattering [197]. Also, additional polarization due to the AlN interlayer is observed. As a result, the sheet charge density and mobility are improved as compared with the conventional AlGaN/GaN heterostructure having equivalent AlGaN parameters.

At small drain bias, V_{DS}, the conductivity between the source and drain, known as 2DEG conductivity, is proportional to the product of channel mobility, μ, and the sheet electron density, N_S:

$$g_{SD} = \frac{I_D}{V_{DS}} = q\mu N_S \frac{L}{W} \tag{5.202}$$

where I_D is the drain current and L and W are the length and width of the gate. Therefore, insertion of an AlN layer increases the conductivity. In [198], it is reported that introduction of an AlN interlayer improved the ON-state resistance and current, R_{ON} and I_{ON}, by 10 %.

The 2DEG sheet resistance of GaN/AlN/AlGaN structure can be calculated by the following equation according to [194]:

$$N_S = \frac{d_{AlGaN}\sigma_{AlGaN} + d_{AlN}\sigma_{AlN}}{q(d_{AlGaN} + d_{AlN})} - \frac{\varepsilon}{q}\left(q\Phi_b + E_F - \Delta E_{C\,\frac{AlN}{GaN}} + \Delta E_{C\,\frac{AlGaN}{GaN}}\right) \tag{5.203}$$

where σ_{AlN} is the sheet charge density that is induced by AlN polarization and ε_{AlN} and d_{AlN} are the dielectric constant and thickness of the AlN capping layer, respectively. The surface barrier height, $\Phi_{b,}$ and the Fermi level position, $E_{F,}$ of the GaN/AlN/AlGaN structure are shown in Fig. 5.36.

A critical requirement of the power switch is that it has low ON-resistance, R_{ON}, immediately after switching from OFF-state to ON-state. The ON-resistance, R_{ON}, of a HEMT is expressed by the following equation:

$$R_{ON} = 2R_C + R_S + R_D + R_{CH} \tag{5.204}$$

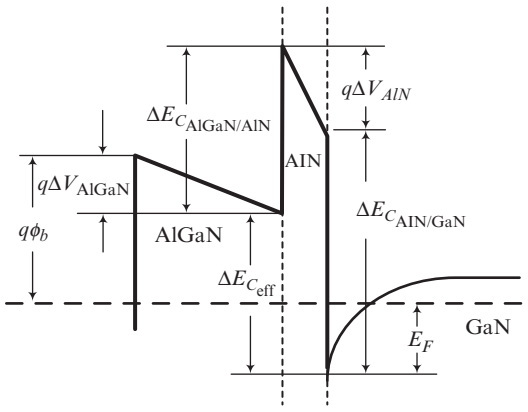


FIG. 5.36 Conduction band diagram of a GaN/AlN/AlGaN heterostructure [195].

where R_C is the source and drain contact resistance, R_S, is the parasitic source resistance, R_D, is the parasitic drain resistance, and R_{CH} is the channel resistance. The carrier trapping at the surface and the buffer traps degrade the device performance. In a GaN HEMT, the parasitic charge moving in and out of the traps affects the density of the 2DEG and causes ON-resistance degradation. To characterize the dynamic ON-resistance of a HEMT, a switching test should be performed using Fig. 5.37. The gate source of the device is connected to a pulsed generator that can switch the device from OFF- to ON-state. During the OFF-state, high-voltage V_{DD} is applied to the device. The load resistance, R_L, is connected in series with the device under test, and it is adjusted so that the ON-state resistance is measured in the linear region. The turn-ON and turn-OFF time are fixed during the experiment. Turn-OFF time should be long enough, typically larger than 10 ms, so the device under test cools down and its temperature does not affect the results. The ON-time is larger than the time at which the dynamic resistance is measured or the time at which the drain current, I_D, saturates.

The transient drain current through the device, $i_D(t)$, and the drain-source voltage, $v_{DS(t)}$, are recorded, and the resistance is calculated for different times by the equation:

$$R_{ON_{Dyn}}(t) = \frac{v_{DS(t)}}{i_D(t)} \tag{5.205}$$

The static ON-resistance, $R_{ONstatic,}$ is calculated by the same equation; only the saturated values for the current and the voltage are used. The experiment and calculation can be repeated for different values of the load resistance (i.e., different drain current). In Fig. 5.38A is a sketch of the gate-source voltage applied to the device under test, the drain-source voltage and the drain current. While in Fig. 5.38B showed a sketch of the dependency of drain current I_D, as a function of drain-source voltage, V_{DS}, for times t_1 and $_{t2}$ and different values of the load resistance.

The current collapse can be defined as a normalized dynamic ON-resistance (i.e., a ratio of the dynamic resistance value to its static value). The ratio can be used to compare the performances of HEMTs.

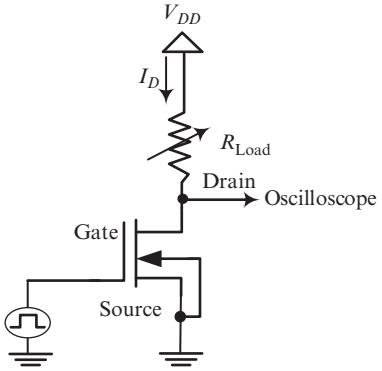


FIG. 5.37 Pulsed test circuit for dynamic ON-resistance measurement.

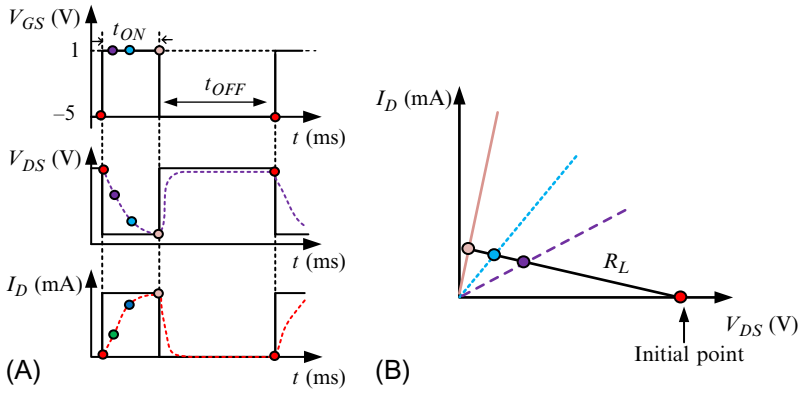


FIG. 5.38 Pulsed test for calculating dynamic ON-resistance. (A) Gate source voltage applied to the device under test, the drain-source voltage and the drain current in function of time. (B) Dependency of drain current I_D, as a function of drain-source voltage, V_{DS}, for times t_1 and t_2 and different values of the load resistance.

5.4.5.2 GaN HEMT DC Characteristics

The current-voltage characteristics of a HEMT are related to the density variation of the 2DEG where 2DEG depends on the gate-source voltage, V_{GS}, applied to the HEMT. Moreover, any changes of V_{GS} have an effect on the electron mobility in the channel. A HEMT has three modes of operation: linear, saturation, and cut-OFF. For power applications and the linear mode of operation, the low-field mobility of the electrons in 2DEG, μ_n, is used to calculate the drain current, while when the drain-source voltage increases, the mobility of the electrons in the 2DEG decreases. In this case, a simple model for high field mobility, μ_n^{HV}, based on the geometry of the HEMT structure is used:

$$\mu_n^{HV} = \frac{\mu_n}{1 + \dfrac{\mu_n V_{DS}}{L_{CH} v_{sat}}} \tag{5.206}$$

where L_{CH} is the channel length and v_{sat} is the saturation velocity. The drain current, i_D, is proportional to the density of electrons in the channel [199]:

$$i_D(x) = \frac{W}{L_{CH}} \mu_n C_{GS} \frac{dv}{dx} \tag{5.207}$$

where W is the channel width. The drain current can be obtained by integrating the current along the channel. If the source and drain contact resistances are neglected and the boundary conditions are used,

$$v_{x=0} = 0 \text{ and } v_{x=L_{CH}} = V_{DS} \tag{5.208}$$

then the drain current in the linear regime of operation is

$$I_D = \frac{W}{L_{CH}} \mu_n C_{GS} \left[(V_{GS} - V_{th}) V_{DS} - V_{DS}^2 \right] \tag{5.209}$$

where C_{GS} is the gate-to-source capacitance and V_{th} is the threshold voltage. In the saturation regime of operation, the drain current is

$$I_D = \frac{W}{L_{CH}} \mu_n C_{GS} (V_{GS} - V_{th})^2 \tag{5.210}$$

5.4.5.3 GaN HEMT Design Considerations

To improve the performance and also protect GaN HEMTs from damage, the designer should take into account some very important concerns and benefits.

The threshold voltages of GaN HEMTs are low compared with the Si and SiC MOSFETs. Some of the HEMT devices start to conduct current at significantly low gate-source voltage (1.4 V) that makes it difficult to ensure that the device turns OFF, especially at low temperatures (the threshold voltage decreases as the temperature drops). Negative voltage should be used in this case to ensure turn-OFF of the device. This behavior indicates that the threshold voltage has a positive temperature coefficient. HEMTs are unipolar devices (i.e., no minority carriers are involved during conduction). Therefore, there is no reverse recovery charge and thus very small reverse recovery losses.

As it can be seen in Figs. 5.32 and 5.34, GaN HEMTs do not have an intrinsic body diode as in Si and SiC MOSFETs. However, they have a so-called "body-diode" effect that makes the device conduct under applied reverse voltages. The mechanism for an enhancement GaN HEMT to behave as a diode during turn-OFF is as follows [200]. When the gate-source voltage is zero and the drain-source voltage is positive, no channel is created, and therefore, current is not flowing. As the drain-source voltage starts to become negative, a positive bias on the gate relative to the drift region is formed, injecting electrons under the gate. The gate-to-drain voltage starts to increase, and when it reaches the threshold voltage, there will be a significant amount of electrons under the gate to form a conduction channel.

The temperature coefficient of the ON-state resistance, R_{ON}, of a GaN HEMT is positive, similar to Si and SiC MOSFETs, but the magnitude is small compared with a Si MOSFET and approximately in the same range as a SiC MOSFET.

Since GaN HEMTs have high switching speed, the voltage slew rate may be more than ten to hundreds of volts per nanosecond, and the current slew rate may be more than 10 A s^{-1}. Such a high slew rate may lead to the so-called Miller effect (i.e., undesirable or parasitic turn-ON of the power transistor and that creates a short circuit that will cause significant damage resulting in destruction of the HEMT).

Shown in Fig. 5.39A is a synchronous buck converter. If the upper HEMT is switched ON, the lower one has to be OFF in order to avoid a shoot-through condition and, therefore, possible failure of the HEMT due to overcurrent.

The mechanism of the parasitic switching for the synchronous buck can be explained with the capacitive voltage divider formed between the gate to drain and gate to source of the low-side transistor (Fig. 5.39B). The gate-source voltage of the low-side transistor is

$$V_{GS} = \frac{C_{GD}}{C_{GD} + C_{GS}} V_{SW} \tag{5.211}$$

where C_{GD} and C_{GS} are the gate-drain and gate-source capacitances, respectively, and V_{SW} is the switching node voltage. Although the gate of the low HEMT is set to zero by the driver circuit, there is a possibility that the low-side HEMT turns ON because of the fast change in the switching voltage. The rate of change of the voltage at the switching node, V_{SW}, is approximately V_{in}/t_r, where V_{in} is the converter input voltage and t_r is the rise time. The voltage slew causes a current to flow through gate-to-drain capacitance of the low-side HEMT:

$$i_{C_{GD}} = C_{GD} \frac{dV_{SW}}{dt} \tag{5.212}$$

This current flows into the equivalent impedance of driver pull-down resistance in series with the gate resistance and both of them in parallel to the gate-source capacitance of the low HEMT. If the gate-source voltage during the rise time of the high side transistor is higher than the threshold voltage, the low HEMT will turn ON parasitically. One way to prevent this from happening is to split the gate pull-up and pull-down connection in the driver and allowing for the insertion of discrete resistors, if needed. The low (OFF-state) pull-down resistance should be a lower resistance value than the pull-up resistance value. If the driver does not support a separate turn-OFF resistor, a diode in parallel can be used, as shown in Fig. 5.40.

The high slew rate may also cause ringing and, in some cases, damage if the common source inductance, L_S, is not minimized. The source current, i_S, is the sum of the drain and the gate currents. Any voltage induced on the common source inductance $\left(L_S \frac{di_S}{dt}\right)$ will show up as ringing in the gate-source voltage. To address this issue, one company developed packages with exceptionally low internal inductance by implementing source-sense or Kelvin connection, but the external inductance that contributes to the ringing should also be minimized. Shown in Fig. 5.41 is a Kelvin connection at the source of a HEMT where the ground return of the gate driver is connected directly to the source on the die internal to the package by a star-point connection. In this case, the external parasitic inductances and resistances in the gate loop will be minimized, and the high slew rate of the drain current during turn-ON switching cannot influence the gate current loop.

However, the (PCB) layout should be carefully considered to minimize the effect of the parasitic inductance. For this purpose, the designers should keep the connection from the output of the driver to the HEMT gate and from the Kelvin connection

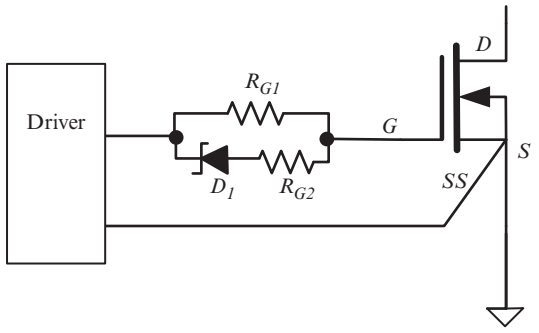


FIG. 5.40 Separate turn-ON and turn-OFF resistors to control parasitic turn-on of low-side HEMT.

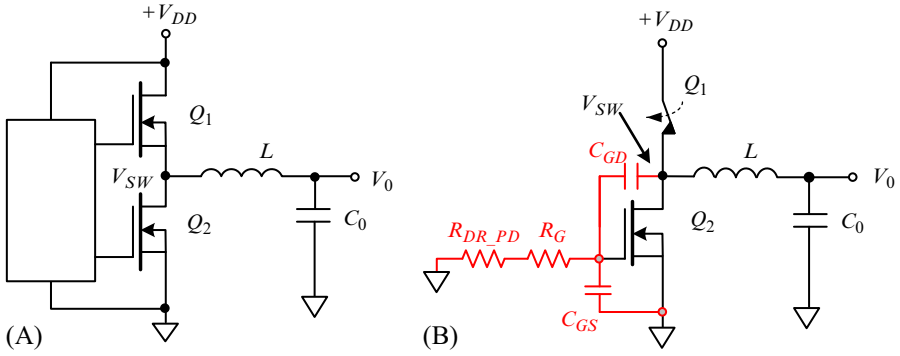


FIG. 5.39 Synchronous buck converter (A) idea and (B) parasitic resistance and capacitance included.

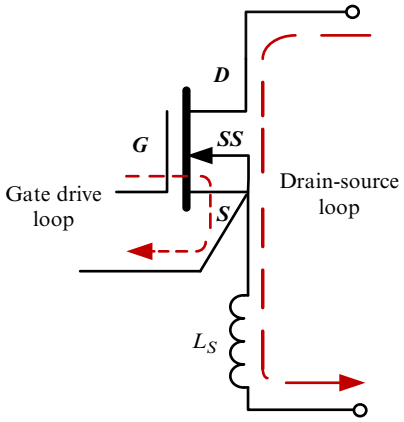


FIG. 5.41 Source-sense or Kelvin connection at the HEMT source.

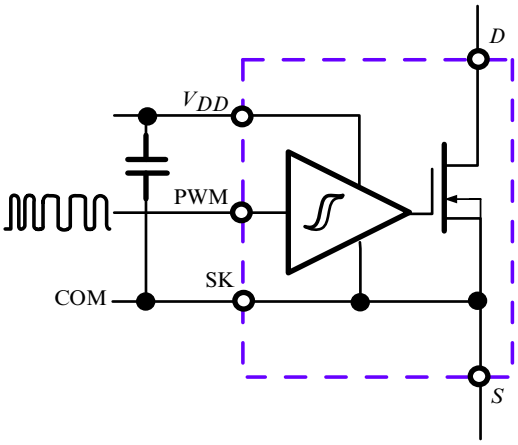


FIG. 5.43 Gate drive and logic circuits with GaN power FETs on a single chip.

to the gate return path of the driver as short as possible. To reduce the wire parasitic inductance, the two paths should be on separate board layers physically over each other. In this case, the magnetic flux generated by two current flows will cancel each other and will lower the parasitic inductance. Also, the connection for the decoupling capacitor of the driver power supply should be short.

During the fast switching transition, the Miller capacitance combined with parasitic inductance in the gate-source loop may induce over- or undershoot voltage spikes that could possibly exceed the maximum gate-source voltage rating of the device. This can be avoided by optimizing the PCB layout, but if the spikes still remain after overvoltage clamping a Zener diode and a capacitor in parallel is included as it shown in Fig. 5.42A can be used [201]. If a negative gate-source voltage is used to turn OFF the HEMT, the overvoltage clamp will have two Zener diodes connected back to back as shown in Fig. 5.42B. For effective clamping, the diode and the capacitor should be placed as close to the device gate as possible.

To enable high switching, high power density, and low system cost, some companies are fabricating a gate drive and logic circuit with GaN power FETs on a single chip, as shown in Fig. 5.43. The advantages of this type of arrangement are that there is no gate-loop parasitic inductance and, therefore, the output signal will be absent of ringing; has a fast rise-time gate signal; and the ability to have rail-to-rail gate signal values. Plus, it offers high-frequency operation with minimal propagation delay [202].

Unlike many conventional Si MOSFETs, the GaN HEMTs are not avalanche rated at the breakdown at the drain-source junction. Therefore, in order to maintain reliability, the maximum drain-source voltage, V_{DS}, should be guaranteed by design. For some topologies, Si MOSFETs can be directly substituted for GaN HEMTs with the same breakdown voltage. An example of this type of topology is a full bridge converter controlled as a dual synchronous buck, as shown in Fig. 5.44 [203].

While for some resonance topologies, Si MOSFETs cannot be replaced with GaN HEMTs that have the same breakdown voltage. Shown in Fig. 5.45 is a resonant-reset forward converter.

After the switch turns OFF, the magnetizing current reverses in a sinusoidal fashion set by the magnetizing inductance, L_m,

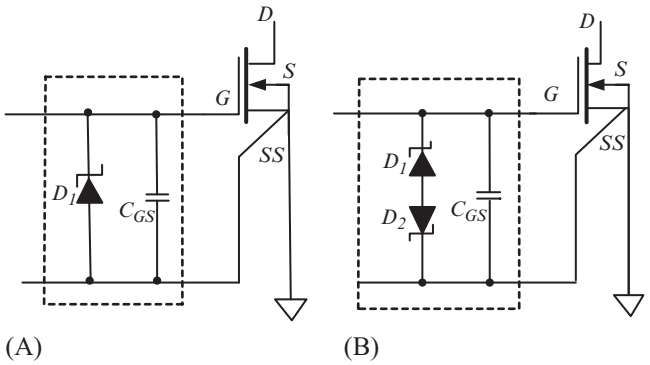


FIG. 5.42 Gate overvoltage clamping using Zener diodes and capacitor: (A) zero voltage is applied to turn OFF the HEMT, (B) negative voltage is applied to turn OFF the HEMT.

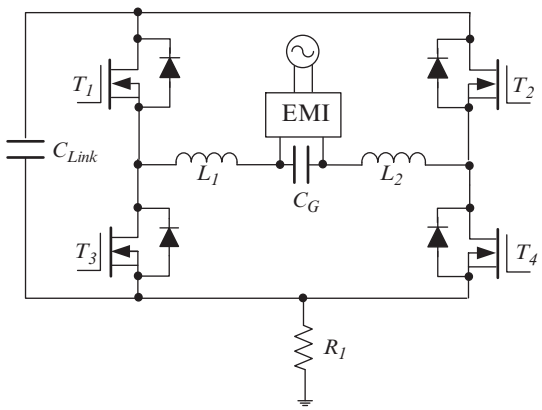


FIG. 5.44 A dual synchronous buck converter.

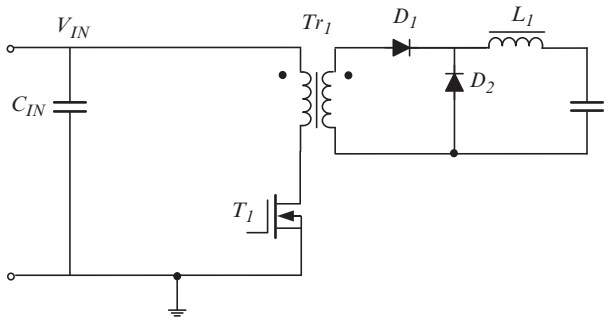


FIG. 5.45 A resonant-reset forward converter.

and the resonance capacitance, C_R. The resonance capacitance, C_R, is a sum of all capacitances across the primary winding of the transformer including the reflected diode capacitance, C_D:

$$C_R = C_D\left(\frac{N_S}{N_P}\right)^2 + C_{DS} + C_T \tag{5.213}$$

where C_{DS} is the switch drain-source capacitance, C_T is transformer primary windings capacitance, and N_S/N_P is the transformer winding ratio. The drain-source capacitance, C_{DS}, is dominant in this expression. The drain-source peak voltage, V_{DSpeak}, of the switch depends on the characteristic impedance $\sqrt{L_m/C_R}$ and can be calculated by the equation:

$$V_{DSpeak} = V_{in} + V_P = V_{in} + I_{Ppeak}\sqrt{\frac{L_m}{C_R}} \tag{5.214}$$

where the peak primary current is

$$I_{Ppeak} = \frac{1}{2}\frac{V_{in}t_{ON}}{L_m} \tag{5.215}$$

From the last three equations, it can be concluded that if only switches are different in the circuit shown in Fig. 5.45, the maximum drain-to-source voltage that will be applied to the switch depends on the drain-source capacitance, C_{DS}. Since GaN HEMTs have significantly smaller capacitance, the peak voltage, V_P, will be significantly larger, and therefore, the peak drain-source voltage will correspondingly be larger. In order to maintain maximum reliability, GaN HEMTs should be rated for higher voltages than the Si MOSFETs in any particular application.

Although GaN high-power HEMTs have significantly low switching and conduction power losses, compared with MOSFETs in Si or SiC, during high-power and high-frequency operation, their temperature is increased. Thermal management is another very important consideration for designers. The current fabrication methodology of HEMT structures implies that the gate, drain, and source connections must be made on the same side of the die. For this reason, necessary isolation gaps must be included between these contacts as this mounting technique results in a higher thermal resistance. To improve the thermal resistance, the package of HEMTs has a thermal pad on the bottom side that is connected to the substrate through high-density microvias with copper providing the low thermal resistance path. To optimize the device performance, the thermal pad must always be connected to the source. For most effective cooling, a heat sink can be attached to the PCB bottom copper pad with the recommended thermally conductive interface pad or film between the heat sink and the bottom copper pad. Also, the top copper layer should be a 2 oz or thicker layer. A PCB with four or more internal layers is desirable. To improve the heat transfer is to add plated, through-hole thermal vias between conductive layers, but no vias should be placed under the solder bars unless they are microvias and completely filled with copper [200]. Vias with holes located directly under the gate, source, or drain solder bars will reduce the transistor's temperature cycling performance. In Fig. 5.46, a cross-sectional view of the GaN HEMT package and thermal dissipation path through the PCB, vias, and the heat sink is shown [204].

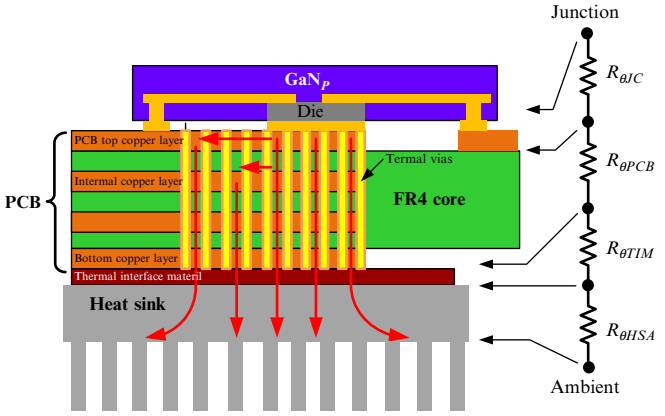


FIG. 5.46 A cross-sectional view of a GaN HEMT package and thermal dissipation path [203].

Appendix Lightly Doped Drift Region Thickness

One of the requirements for choosing a proper power electronic device for a converter is that it must possess a low specific ON-resistance. The specific ON-resistance of a bipolar device is related to the width and doping concentration of the lightly doped drift region (N^- base). This means that the doping concentration and the width of the low-doped base region in a bipolar device must be carefully considered to achieve a desired avalanche breakdown voltage and ON-resistance (conduction characteristics).

The avalanche breakdown voltage, V_{BD}, for an abrupt parallel plate junction, is a function of the background doping and the semiconductor properties, such as dielectric constant,

energy bandgap, and impact ionization coefficient. Breakdown occurs when the carrier multiplication becomes greater than unity. Impact ionization coefficients empirically describe the exponential relationship of the applied electric field and associated charge-carrier creation. The impact ionization coefficients for electrons and holes have different values, and values for semiconductor materials of interest are obtained empirically. The general ionization coefficient has been determined to have a theoretical form that is exponential and represented by [205]:

$$\alpha_i = A_i e^{-\left(\frac{b_i}{\mathcal{E}}\right)^{m_i}} \tag{A.1}$$

where $\mathcal{E}$ is the electric field (V cm^{-1}), A_i is the amplitude parameter (cm^{-1}), b_i is the ionization energy parameter related to the mean free path between collisions (V cm^{-1}), and m_i is an additional fit parameter for use with a multitude of semiconductor materials [205,206]. These parameter values depend on the semiconductor material, and they are different for electrons or holes. For Si, 6H-SiC, and GaN, m_i has been determined to be 1 for both electrons and holes [205,206].

Near the breakdown condition, a small error is introduced by equating the impact ionization coefficients of electrons and holes to an effective ionization coefficient, α_{eff}. In this case, the breakdown voltage is defined as the applied voltage at which the summed effects described by the ionization coefficient acting over the depletion width, W, create more free charge carriers. The boundary at breakdown is when the integral Eq. (A.2) achieves a value of unity [207]. The associated breakdown condition in terms of the effective ionization coefficient is:

$$\int_0^W \alpha_{eff}\, dx = 1 \tag{A.2}$$

Evaluation of this integral using Eq. (A.1) is very difficult; and no analytical expressions result, thus limiting its usefulness for device design. However, a simplified (and purely empirical) polynomial expression for the ionization coefficient in terms of the electric field is widely used [207]:

$$\alpha_{eff} = K\mathcal{E}^7 \tag{A.3}$$

The two previous fit parameters, A_i and b_i, are absorbed into the prefactor, K. The coefficient, K, is expressed in terms of new parameters, A, b, and m, that are averages of the previous A_i, b_i, and m_i values, expressed in Eq. (A.1) for holes and electrons [206]:

$$K = 9 \times 10^{-38} \frac{A 216^m}{b^{0.85} E_G^{15}} \tag{A.4}$$

where E_G is the bandgap energy (eV) for the semiconductor material of interest.

For a one-sided abrupt P^+-N junction, the electric field and the voltage across the lightly doped region are functions of the depletion distance and depend on the impurity doping concentration, N_{D1}, in the lightly doped N-base and the depleted N-base width, W. The electric field and voltage relations are presented in Eqs. (A.5), (A.6), respectively.

$$\mathcal{E}(x) = \frac{q}{\varepsilon} N_{D1}(W - x) \tag{A.5}$$

$$V(x) = \frac{q}{2\varepsilon} N_{D1}(W - x)^2 \tag{A.6}$$

The maximum electric field is observed at junction ($x = 0$). Using this and substituting Eq. (A.5) in Eq. (A.3) and then substituting into the integral Eq. (A.2), one can obtain the minimum width of the depletion layer, $W_{\min}$, at breakdown [206].

$$W_{\min} = \left(\frac{K}{8}\frac{q^7}{\varepsilon^7} N_{D1}^7\right)^{-\frac{1}{8}} \tag{A.7}$$

The corresponding breakdown voltage can then be determined from Eq. (A.6) as

$$V_{BD} = \left(2K\frac{q^3}{\varepsilon^3} {N_{D1}}^3\right)^{-1/4} \tag{A.8}$$

It should be noted that the permittivity is correctly placed in the denominator in Eq. (A.8), not in the numerator as was presented in the expressions from [206].

To reduce the lightly doped region width and maintain the same breakdown voltage requires the addition of a highly doped N^+ buffer layer at the end of the drift (N-base) region to create a $P^+N^-N^+$ structure. This will modify the expressions for the minimum width of the depletion layer, $W_{\min}$, and the corresponding breakdown voltage, V_{BD}. Reducing the width of the base region will decrease the effective on-resistance during conduction and reduce the volume of stored charge, thus decreasing the turn-OFF (and turn-ON) time.

To reduce the thickness of the drift region for the same blocking voltage, a heavily doped N^+-type buffer layer should be added to the end of the drift region to create a $P^+N^-N^+$ structure Fig. A.1B. Due to the high doping level in the buffer layer, the gradient of the electric field will be steep and positive, in the same way as in the P-type region. The electric field has maximum value at the P^+N^- junction. The electric field in the drift region will decrease gradually with no requirement for an excessive depletion layer width. The phenomenon that occurs when the depletion layer extends across the entire drift region is known as punch-through.

Consider a two-dimensional $P^+N^-N^+$ structure under equilibrium conditions with the doping profile sketched in Fig. A.1. The electric field in the different regions can be obtained by substituting the charge densities into Poisson's equations and then integrating:

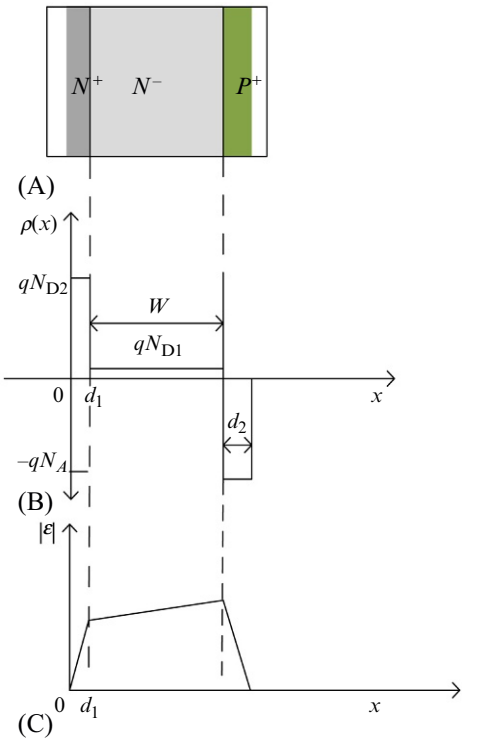


FIG. A.1 (A) A $P^+N^-N^+$ structure highlighting the depleting region under a large reverse applied voltage, (B) doping profile of the $P^+N^-N^+$ structure with charge density as a function of position, and (C) electric field as a function of position.

$$\mathcal{E}=\begin{cases}(q/\varepsilon)N_{D2}x & 0\le x\le d_1\\ (q/\varepsilon)(N_{D1}x+d_1(N_{D2}-N_{D1})) & d_1\le x\le d_1+W\\ (q/\varepsilon)N_A(d_1+W+d_2-x) & d_1+W\le x\le d_1+W+d_2\\ 0 & x\le 0 \text{ and } d_1+W+d_2\le x\end{cases} \tag{A.9}$$

where the respective impurity doping concentrations for the $N^+N^-P^+$ regions are N_{D2}, N_{D1}, and N_A. The corresponding depletion region thicknesses of each section are d_1, W, and d_2.

The maximum electric field of the $P^+N^-N^+$ structure will be at the N^-P^+ junction $(x=d_1+W)$. Charge neutrality from Eq. (A.9) gives the depletion thickness, d_2 of the P^+ region as

$$d_2=(N_{D1}W+N_{D2}d_1)/N_A \tag{A.10}$$

Since $\mathcal{E}=-dV/dx$, the electric potential applied to the structure is obtained by integrating the electric field from 0 to d_1+W+d_2 resulting in

$$V_{appl}=\frac{q}{\varepsilon}\left[\frac{N_{D2}^2+N_{D2}N_A}{2N_A}d_1^2+\left(\frac{N_{D1}N_{D2}}{N_A}+N_{D2}\right)d_1W+\left(\frac{N_{D1}^2+N_AN_{D1}}{2N_A}\right)W^2\right] \tag{A.11}$$

Substituting Eqs. (A.11) into (A.10) and using the result to calculate the ionization coefficient Eq. (A.3), we can reevaluate the ionization integral Eq. (A.2) as

$$N_{D2}^7d_1^8+\frac{N_{D2}^8d_1^8}{N_A}+\left(\frac{N_{D1}}{N_A}+1\right)(8N_{D2}^7d_1^7W+28N_{D1}N_{D2}^6d_1^6W^2+56N_{D1}^2N_{D2}^5d_1^5W^3+70N_{D1}^3N_{D2}^4d_1^4W^4+56N_{D1}^4N_{D2}^3d_1^3W^5+28N_{D1}^5N_{D2}^2d_1^2W^6+8N_{D1}^6N_{D2}d_1W^7+N_{D1}^7W^8)=\frac{8\varepsilon^7}{Kq^7} \tag{A.12}$$

For a given breakdown voltage, BV, the thicknesses of the drift region, W, can be calculated numerically using Eqs. (A.11), (A.12).

Nomenclature

a	Width of channel flow, cm
a_i	Ratio of intercell area to total die area
A	Cross-sectional active device area, cm^2
A*	Richardson's constant
A_{GS}	Coupling area between gate and source, cm^2
A_i, b_i, and m_i	Amplitude parameter (cm^{-1}), ionization energy parameter ($V\ cm^{-1}$), and fit parameter
BV	Breakdown voltage, kV
BV_{CEO}	Maximum open-base breakdown voltage of BJT, kV
C, C_n, and C_p	Auger coefficients, $cm^6\ s^{-1}$
C_{Dep}	Depletion region capacitance, F
C_j	Junction capacitance, F
C_{GD}	Gate-to-drain capacitance, F
C_{OX}	Oxide capacitance per unit area, $F\ cm^{-2}$
C_{SH}	Shunt capacitance, F
C_T	Tunneling coefficient
d	Length from junction to case, cm
d	Recess depth, cm
d_{dep}	Depletion width, cm
d_1, W, and d_2	Depletion region thicknesses of each section of $N^+N^-P^+$ regions, respectively, cm
D	Ambipolar diffusivity, cm^2s^{-1}
D_n and D_p	Electron and hole diffusivities, cm^2s^{-1}
D_{N^-}	Ambipolar diffusion coefficient in N^- region, cm^2s^{-1}
D_{pN}	Hole diffusivity in field-stop N layer, cm^2s^{-1}
D_{pN+}	Minority carrier diffusivities in N^- region, cm^2s^{-1}
E_C	Critical electric field, $V\ cm^{-1}$
E_G	Bandgap energy, eV
E_M	Electric field at Schottky barrier, $V\ cm^{-1}$
E_M	Maximum electric field, $V\ cm^{-1}$
f_T	Cutoff frequency, Hz
h_n and h_p	Electron and hole recombination parameters, $cm^{-4}s^{-1}$
I	Current passing through drift region, A
I_{CG}	Displacement layer, A

I_D	Drain current, A
I_D	Diode current, A
I_{disp1} and I_{disp2}	Displacement currents, A
I_E, I_B, I_C	Emitter, base, and collector currents, A
I_{mos}	MOS current, A
I_n and I_p	Electron and hole currents, A
I_{n0}, I_{n1}, and I_{n2}	Electron current at junctions J_0, J_1, and J_2, A
I_{p0}, I_{p1}, and I_{p2}	Electron current at junctions J_0, J_1, and J_2, A
I_{QN}	Capacitive current, A
I_{sne}	Emitter electron saturation current, A
Ip	Pinch-off current, A
J_0, J_1, J_2, J_3	Junctions
J_F	Current density, A cm^{-2}
J_{FS}	Current density across the Schottky barrier, A cm^{-2}
$J_{n((N^+N^-)}$, $J_{n((PN^-)}$	Electron carrier densities at the N^+N^- and PN^- junctions, A cm^{-2}
k and n	Harmonic indexes for CSR carrier density of Fourier series representation
k	Boltzmann's constant (1.381×10^{-23} J K^{-1})
K	Coefficient
K_{FV}	Feedback constant
K_{GS}	Coupling area coefficient between gate and source
L_A	Accumulation layer length, cm
L_{CH}	DMOSFET channel length, cm
L_{DRIFT}	Drift region thickness, cm
L_{PN}	Hole diffusion length, cm
l_m	Intercell half width, cm
l_1	Width due to voltage V_{GE}, cm
M	Number of the terms of the Fourier series
M	Number of segments
N^-	Drift region
N^+	Field-stop layer
N^+	Emitter
N_A	Acceptor doping concentration, cm^{-3}
N_{B0}	Electron concentration at junction J_0, cm^{-3}
N_C	Effective density of state in conduction band, cm^{-3}
N_{CH}	Channel doping concentration, cm^{-3}
N_D	Donor doping concentration, cm^{-3}
N_{DRIFT}	Doping concentration of lightly doped drift region, cm^{-3}
N_{D1}	Doping concentration in the lightly doped N-base, cm^{-3}
N_{D2}, N_{D1} , N_A	Doping concentration in the $N^+N^-P^+$ regions, respectively, cm^{-3}
N_E	Emitter doping concentration, cm^{-3}
N_{JEFT}	Doping concentration in the *JFET* region, cm^{-3}
N_N	Doping concentration of buffer layer, cm^{-3}
N_N^-	Doping concentration in the N^- region, cm^{-3}
N_p	Emitter doping concentration, cm^{-3}
N_p	Doping concentration of gate, cm^{-3}
N_S	Number of effectively available states per unit volume, cm^{-3}
N_V	Effective density of state in valence band, cm^{-3}
n	Electron carrier concentration, cm^{-3}
N_{B1}	Electron concentration base-region boundary, cm^{-3}
n	Ideality factor
n_i	Intrinsic carrier concentration, cm^{-3}
n_{PO}	Electron concentration P-base region boundary, cm^{-3}
n_0 … n_7	Nodes in lumped-charge model, cm^{-3}
n_{pw}	Electron concentration at junction J_3, cm^{-3}
n_{pw}	Electron concentration at base region boundary from N^- emitter side, cm^{-3}
n_s	2DEG sheet charge density, cm^{-3}
P	P emitter
P	P well
P_B	Base doping concentration, cm^{-3}
p	Hole carrier concentration, cm^{-3}
P_{DRIFT}	Hole concentration of drift region, cm^{-3}
$p(x)$	Ambipolar carrier density as a function of position, cm^{-3}
$p(x,t)$	Excess carrier concentration, cm^{-3}
$p(x,t)$	Ambipolar carrier density as a function of position and time, cm^{-3}
$p_0(t)$	DC Fourier series component of the carrier storage region (CSR), cm^{-3}
P_{JFET}	Doping concentration of JFET region, cm^{-3}
$p_k(t)$, $p_n(t)$—k- or $n^{-\text{th}}$	Fourier series component of CSR carrier density profile, cm^{-3}
P_{N-}	Hole concentration in N^- region, cm^{-3}
p_{NO}	Hole concentration at the boundary between buffer layer and drift region, cm^{-3}
p_{NO}, p_{NW}	Hole concentrations at two edges of field-stop layer, cm^{-3}
$p_{T(k)}$	Carrier distribution, cm^{-3}
p_{T1}, p_{T2}, and p_{T1}	Carrier densities of the two points of a segment and the carrier density of the segment, cm^{-3}
p_{x1} and p_{x2}	Excess carrier concentrations at the two boundaries of the drift region, junctions J_1 and J_2, cm^{-3}
q	Unit electric charge (≅1.6×10−19C)
R	Half height of Schottky metallization, cm
R_A	Accumulation layer resistance, Ω
R_{AUG}	Auger recombination rate, cm^{-3}s^{-1}
R_{CH}	Channel resistance, Ω
R_{CONT}	Ohmic contact resistance, Ω
R_{DRIFT}	Drift region resistance, Ω
R_{JFET}	Junction field-effect transistor resistance, Ω
R_{OC}	Ohmic contact resistance, Ω
R_{ON}	ON-resistance, Ω
R_s	Series resistance, Ω
r_{sp}	Specific contact resistivity, mΩ cm^2
R_{SP_ON}	Specific ON-resistance, mΩ cm^2
R_{SRH}	Shockley-Read-Hall carrier recombination rate, cm^{-3}s^{-1}
$R_{(th-jc)}$	Junction-to-case thermal resistance, K kW^{-1}
T	Absolute temperature, K
T_j	Junction temperature, K
V_{AC}	Anode cathode voltage, V
V_{AK}	Voltage drop during conduction state, V
V_B	Blocking voltage, V
V_{BE}	Base-emitter voltage, V
V_{bi}	Built-in voltage, V
V_{CE}	Collector-emitter voltage, V

V_{CH}	Channel voltage, V
V_{d1} and V_{d2}	Depletion layer voltages, V
V_D	Drain bias, V
V_{DC}	DC supply voltage, V
V_{DS}	Drain-source voltage, V
V_F	Forward voltage drop, V
V_G	Gate drive voltage, V
V_{GE}	Gate emitter voltage, V
V_{GS}	Gate-source voltage, V
V_{N^-}	Carrier storage region voltage, V
V_{N^-}	Drift region voltage drop, V
V_{j0}, V_{j1}, and V_{j2}	Voltage drop at junctions J_0, J_1, and J_2, V
V_{j12}	Total junction voltage, V
V_R	Reverse voltage, V
v_{sat}	Saturation velocity, cm s^{-1}
V_{seg}	Resistive voltage drop of a segment, V
V_T	Thermal voltage, V
V_{th}	Threshold voltage, V
W	Depletion layer width, cm
W	Miller capacitance width, cm
W	Schottky contact width, cm
W_B	Base width, cm
W_{CH}	DMOSFET channel width, cm
W_D	Drift layer thickness, cm
W_{d1} and W_{d2}	Depletion widths, cm
W_{DEP}	Depletion region width, cm
W_{DRIFT}	Drift region width, cm
W_g	Gate width, cm
W_I	Intrinsic layer width, cm
W_{min}	Minimum width of the depletion layer of *N*-base, cm
W_N	Width of buffer layer, cm
W_P	Base region width, cm
W_S	Depletion width between gate and source, cm
W_0	Zero bias depletion region width, cm
W_1, W_2, W	Widths of the depletion region on the N^- and P sides of the junction and total depletion layer, cm
χ	SiC electron affinity, eV
x_D	Cross-sectional width, cm
x_j	P^+ region thickness, cm
x_{JP}	P-base junction thickness, cm
x_1	Thickness, cm
x_1 and x_2	Boundary positions of the carrier storage region, cm
z	Length of cell in the orthogonal direction to the cross section
z	Width in vertical to paper direction, cm
α_i, and α_{eff}	General ionization coefficient, effective ionization coefficient, cm^{-1}
β	Common-emitter gain
ε	Electric field strength, V cm^{-1}
ε_C	Critical electric field strength, V cm^{-1}
ε_r	*Si* Dielectric constant
ε_r	Relative permittivity
ε	Material permittivity, Fcm^{-1}
λ	Thermal conductivity, W cm^{-1} K^{-1}
μ_{CH}	Inversion layer mobility, $cm^2V^{-1}s^{-1}$
μ_n and μ_p	Electron and hole mobilities, $cm^2V^{-1}s^{-1}$
τ	High-level carrier lifetime, s
τ_n, τ_p, and τ_{HL}	Electron, hole, and high-level injection lifetimes, s
τ_{PHL}	High-level lifetime in P-base region, s
τ_{pN}	Minority lifetime in *N* region, s
τ_{N^-}	Electron lifetime in N^- region, s
ψ	Potential, V
ρ	Resistivity of the epilayer, Ω cm^{-2}
Q_G	Total gate charge, C
Q_{GD}	Gate-to-drain charge, C
Q_{GS}	Gate-to-source charge, C
Q_{GS}	Charge in buffer region, C
Q_N	Charge in buffer region, C
Q_{SW}	Switching charge, C
ϕ_m	Work function of the metal, eV

Acronyms/Initialisms

ac	Alternating current
ADE	Ambipolar diffusion equation
AlN	Aluminum nitride
AlGaN	Aluminum gallium nitride
Al_2O_3	Alumina
Au	Gold
BeO	Beryllia
BHFFOM	Baliga high-frequency figure of merit
BJT	Bipolar junction transistor
C	Carbon
C	Cubic
CLFOM	Conduction loss figure of merit
CS	Carrier storage
CSL	Current spreading layer
CSR	Carrier storage region
CTE	Coefficient of thermal expansion
DC	Direct current
DMOSFET	Double diffusion metal-oxide-semiconductor field-effect transistor
ET	Edge termination
FACTS	Flexible AC transmission systems
FET	Field-effect transistor
FOM	Figure of merit
FS	Field stop
GaN	Gallium nitride
GaAs	Gallium arsenide
Ge	Germanium
GTO	Gate turn-off thyristor
H	Hexagonal
HEMT	High-electron-mobility transistor
HFET	Heterostructure field-effect transistor
HVDCT	High-voltage DC transmission
ICM	Integral charge control model
IGBT	Insulated-gate bipolar transistor
IGCT	Integrated gate-commutated thyristor
IrPt	Indium-platinum
JBS	Junction barrier Schottky diode
JFET	Junction field-effect transistor
JFOM	Johnson's figure of merit
LC-JFET	Lateral channel junction field-effect transistor

LED	Light-emitting diode
MCT	MOS-controlled thyristors
MESFET	Metal-semiconductor field-effect transistor
Mg	Magnesium
Mo	Molybdenum
MOS	Metal-oxide-semiconductor
MOSFET	Metal-oxide-semiconductor field-effect transistor
MPS	Merged PN-Schottky diode
MTO	MOS turn-off thyristor
Ni	Nickel
Ni/Au	Nickel/gold
NO	Nitric oxide
NPT	Nonpunch-through
PCB	Printed circuit board
PiN	*P*, intrinsic and *N*-doped regions
Pd	Palladium
PdAg	Palladium-silver
Pt	Platinum
PNP	*P*-, *N*-, and *P*-doped regions
PT	Punch-through
R	Rhombohedral
RC	Resistor-capacitor
RESURF	Reduced surface field
SBD	Schottky barrier diode
SCR	Silicon-controlled rectifier
Si	Silicon
SiC	Silicon carbide
Si_3N_4	Silicon nitride
SiO_2	Silicon dioxide
SLFOM	Switching losses figure of merit
SRH	Shockley-Read-Hall
T	Titanium
2DEG	Two-dimensional electron gas
VCJFET	Vertical channel junction field-effect transistor
VJFET	Vertical junction gate field-effect transistors

References

[1] J. Bardeen, W.H. Brittain, The transistor, a semiconductor triode, Phys. Rev. (1948) 230.

[2] J.M. Goldey, I.M. Mackintosh, I.M. Ross, Turn-off gain in p-n-p-n switches, Solid State Electron. 3 (1961) 119.

[3] J.M. Goldey, I.M. Makintosh, I.M. Ross, Turn-off gain in p-n-p-n transistor triodes, Solid State Electron. 3 (1961) 119.

[4] V.A.K. Temple, R.P. Love, A 600V MOSFET with near ideal onresistance, IEDM Tech. Dig. (1978) 664.

[5] B.J. Baliga, Fast-switching insulated gate transistors, IEEE Electron Device Lett. 4 (12) (1983) 452–454.

[6] http://www.pwrx.com/summary/IGBT/IGBT.aspx.

[7] http://fmccgroup.com/products/semiconductors/gto.

[8] S. Bernet, Recent developments of high power converters for industry and traction applications, IEEE Trans. Power Electron. 15 (6) (2000) 1102–1117.

[9] A. Elasser, Silicon carbide benefits and advantages for power electronics circuits and systems, Proc. IEEE 90 (6) (2002) 969–986.

[10] C.M. Johnson, N.G. Wright, S. Ortolland, D. Morrison, K. Adachi, A.O. O'Neill, Silicon carbide power devices: hopeful or hopeless? in: Proc. IEE Colloq. Recent Advances in Power Devices, 1999, pp. 10/1–10/5.

[11] B. Ozpineci, L.M. Tolbert, S.K. Islam, M. Hasanuzzaman, Effects of silicon carbide (SiC) power devices on HEV PWM inverter losses, in: 27 Annual Conference of the IEEE Industrial Electronics Society (IECON'01), Denver, Colorado: s.n., Nov 29 to Dec 2, 2001.

[12] S. Pearton, GaN and ZnO-based Materials and Devices, Springer Science & Business Media, 2012. s.l.

[13] M. Dudleyt, W. Huangt, S. Wangt, J.A.P. Neudeckt, C. Fazis, White-beam synchrotron topographic analysis of multi-polytype SiC device configurations, J. Phys. D. Appl. Phys. 28 (1995) A56–A62.

[14] http://staff.csc.fi/~raback/sic/thesis/node6.html.

[15] M. Shur, S. Rumyantsev, M. Levinshtein (Eds.), SiC Materials and Devices, Selected Topics in Electronics and Systems, 43, World Scientific Publishing Co. Pte. Ltd, 2007, p. 8. s.l.

[16] M. Ueno, M. Yoshida, A. Onodera, O. Shimomura, K. Takemura, Stability of the wurtzite-type structure under high pressure: GaN and InN, Phys. Rev. B 49 (14) (1994). s.l.

[17] E. Dirote, Nanotechnology at the Leading Edge, Nova Science Publisher, Inc., New York, 2006.

[18] N. Kuwano, K. Kobayashi, K. Oki, S. Miyoshi, H. Yaguchi, K. Onabe, Y. Shiraki, Formation of cubic GaN on (111)B GaAs by metal-organic vapor-phase epitaxy with dimethylhydrazine, Jpn. Soc. Appl. Phys. 33 (1) (1994) 3415–3417.

[19] G. Karas, New Developments in Crystal Growth Research, Nova Science Publishers, Inc., New York, 2005.

[20] B. Shi, M. Xie, H. Wu, Transition between wurtzite and zinc-blende GaN: an effect of deposition, Appl. Phys. Lett. 89 (2006). http://aip.scitation.org/doi/10.1063/1.2360916. s.l.

[21] M. Lei, Gallium Nitride Heterogeneous Source Drain MOSFET, ProQuest, Ann Arbor, 2007.

[22] M. Levinshtein, S. Rumyantsev, M. Shur, Properties of Advanced SemiconductorMaterials GaN, AlN, InN, BN, SiC, SiGe, John Wiley & Sons, Inc., New York, 2001.

[23] M. Levinshtein, S. Rumyantsev, M. Shurr (Eds.), Semiconductor Parameters, 1, World Scientific, River Edge, NJ, 1996.

[24] S. Adachi, Properties of Group-IV, III-V and II-VI Semiconductors, John Wiley and Sons, 2005. http://onlinelibrary.wiley.com/book/10.1002/0470090340. s.l.

[25] M.E. Levinshtein, S.L. Rumyantsev, M.S. Shur (Eds.), Properties of Advanced Semiconductor Materials: GaN, AlN, InN, BN, SiC, SiGe, John Wiley & Sons, Ins, New York, 2001.

[26] M.E. Levinshtein, S.L. Rtmlyantsev, M.S. Shur, Properties of Advanced Semiconductor Materials: GaN, AlN, InN, BN, SiC, SiGe, John Wiley & Sons, Inc, New York, 2001.

[27] P.G. Neudeck, Silicon carbide technology, in: The VLSI Handbook, second ed., CRC Press, 2006 (Chapter 5).

[28] M. Suzuki, T. Uenoyama, A. Yanase, First-principles calculations of effective-mass parameters of AlN and GaN, Phys. Rev. B 52 (11) (1995) 8132–8139. s.l.

[29] M. Levinshtein, S. Rumyantsev, M. Shur, Semiconductor Parameters, world Scientific, River Edge, 1996, pp. 1–211.

[30] J.L. Hudgins, Wide and narrow bandgap semiconductors for power electronics: a new valuation, J. Electron. Mater. 32 (6) (2003) 471–477.

[31] B. Baliga, Semiconductors for high-voltage, vertical channel field-effect transistors, J. Appl. Phys. 53 (1982) 1759–1764.

[32] B.J. Baliga, Power Semiconductor Devices, PWS Pub. Co., Boston, MA, 1996. s.l.

[33] J.L. Hudgins, G.S. Simin, E. Santi, M.A. Khan, An assessment of wide bandgap semiconductors for power devices, IEEE Trans. Power Electron 18 (3) (2003) 907–914. s.l.

[34] J. Johnson, E. Piner, A. Vescan, R. Therrien, J. Rajagopal, J. Roberts, J. Brown, J. Brown, K. Linthicum, 12 W/mm AlGaN–GaN HFETs on silicon substrates, IEEE Electron Device Lett. 25 (7) (2004). s.l.
[35] B.J. Baliga, Power semiconductor device figure of merit for high-frequency applications, IEEE Electron Device Lett 10 (10) (1989). s.l.
[36] E. Johnson, Physical Limitations on Frequency and Power Parameters of Transistors, IRE International Convention Record, New York, NY, 1966.
[37] F.A. Marino, N. Faralli, D.K. Ferry, S.M. Goodnick, M. Saraniti, Figures of merit in high-frequency and high-power GaN, J. Phys. Conf. Ser. 193 (2009).
[38] B.J. Baliga, Fundamentals of Power Semiconductor Devices, Springer Science + Business Media, LLC, New York, 2008.
[39] C. Skierbiszewski, K. Dybko, W. Knap, M. Siekacz, W. Krupczyński, G. Nowak, M. Boćkowski, J. Łusakowski, Z.R. Wasilewski, D. Maude, T. Suski, S. Porowski, High mobility two-dimensional electron gas in AlGaN/GaNAlGaN/GaN heterostructures grown on bulk GaN by plasma assisted molecular beam epitaxy, Appl. Phys. Lett. 86 (10) (2005). s.l.
[40] A.Q. Huang, New unipolar switching power device figures of merit, IEEE Electron Device Lett. 25 (5) (2004). s.l.
[41] C2M0025120D Silicon Carbide Power MOSFET Z-FET. s.l.: Cree Datasheet, 2014.
[42] M. Frivaldsky, P. Spanik, B. Kozacek, M. Piri, Evaluation of power transistors figure of merit for hard switching commutation mode through experimental analysis, in: Progress In Electromagnetics Research Symposium Proceedings, Prague, Czech Republic, 2015.
[43] E. Niculescu, O. Purcaru, M. Maria, M. Cristian, A laboratory exercise to estimate the figure of merit index of power MOSFET, in: Proceedings of the 5th WSEAS/IASME International Conference on Educational Technologies, La Laguna, Spain, 2009.
[44] J. Ejury, How to Compare the Figure of Merit (FOM) of MOSFETs Application Note, Infineon Technologies Inc, 2003. s.l.
[45] DataSheet 650VCoolMOS™C7PowerTransistor IPB65R045C7, InfineonTechnologiesAG, München, Germany, 2013.
[46] Data Sheet CPM2-1700-0045B N-Channel SiC MOSFET. s.l. : ROHM Co. Ltd, 2016.
[47] Data Sheet C3M0065090J Silicon Carbide Power MOSFET C3M MOSFET Technology N-Channel Enhancement Mode, Cree INC, Durham, NC, 2016.
[48] Data Sheet CPM2-1700-0045B Silicon Carbide Power MOSFET C3M MOSFET Technology, Cree Inc., Durham, NC, 2016.
[49] Preliminary Datasheet GS66508B Bottom-side cooled 650 V E-mode GaN transistor. s.l. : GaN System, 2016.
[50] PGA26E19BA Preliminary Datasheet, Panasonic Semiconductor Solutions Co., Ltd., Newark, NJ, 2015.
[51] V. Scarpa, O. Harmon, 120 0 V Co o lSi C™ S ch o ttk y D i od e, Gen er a ti o n 5, Infineon Technologies AG, Munich, Germany, 2016.
[52] CPW5-1700-Z050B Silicon Carbide Schottky Diode Chip Z-RecTM Rectifier, Cree, Inc., Durham, NC, 2013.
[53] H.A. Mantooth, K. Peng, E. Santi, J.L. Hudgins, Modeling of wide bandgap power semiconductor devices—Part I, IEEE Trans. Electron Dev. 62 (2) (2015).
[54] O. Harmon, T. Basler, F. Björk, Design, Advantages of the 1200 V SiC Schottky Diode with MPS, Bodo's Power Systems, 2015. https://www.infineon.com/dgdl/Infineon-Article_Advantages_of_the_1200V_SiC_Schottky_Diode_with_MPS_Design-ART-v01_00-EN.pdf?fileId=5546d46250cc1fdf0151674981861d76, s.l.
[55] Z.C. Feng, SiC Power Materials: Devices and Applications, Springer Science & Business Media, Heidelberg, Germany, 2013. s.l.
[56] D. Defives, O. Durand, F. Wyczisk, O. Noblanc, C. Brylinski, F. Meyer, Barrier height analysis of metal/4H-SiC schottky contacts, Microelectron. Eng. 55 (1–4) (2001).
[57] D. Schroede, Modeling of Interface Carrier Transport for Device Simulation, Springer-Verlag, Wien, 1994.
[58] C. Hu, Semiconductor Devices for Integrated Circuits, Pearson, Delhi, India, 2010. s.l.
[59] B.J. Baliga, Advanced Power Rectifier Concepts, Springer Science + Business Media, New York, 2009. s.l.
[60] Q. Wahab, T. Kimoto, A. Ellison, C. Hallin, M. Tuominen, R. Yakimova, A. Henry, J.P. Bergman, E. Janzén, A 3 kV Schottky barrier diode in 4H-SiC, Appl. Phys. Lett. 72 (1998) 445–448.
[61] J. Zhao, K. Sheng, R.C. Lebron-Velilla, Silicone Carbide Schottky barrier diode, Int. J. High Speed Electron. Syst. 15 (4) (2005) 821–866.
[62] S.G. Sundaresan, C. Sturdevant, M. Marripelly, E. Lieser, R. Singh, 12.9 kV SiC PiN diodes with low on-state drops and high carrier lifetimes, Mater. Sci. Forum 717–720 (2012) 949–952.
[63] Y. Sugawara, D. Takayama, K. Asano, R. Singh, J. Palmour, T. Hayashi, 12-19kV 4H-SiC p–i–n diodes with low power loss, in: 13th Int. Symp. Power Semiconductor Devices and ICs. s.n.: Osaka, Japan, 2001, pp. 27–30.
[64] R. Singh, K.G. Irvine, D.C. Capell, J.T. Richmond, D. Berning, A.R. Hefner, Large area, ultra-high voltage 4H-SiC p-i-n rectifiers, IEEE Trans. Electron Dev. 49 (12) (2002) 2308–2316.
[65] A. Elasser, M. Kheraluwala, M. Ghezzo, R. Steigerwald, N. Evers, J. Kretchmer, T.P. Chow, A comparative evaluation of new silicon carbide diodes and state-of-the-art silicon diodes for power electronic applications, IEEE Trans. Ind. Appl. (2003) 915–921.
[66] T.K. Gachovska, J.L. Hudgins, E. Santi, A. Bryan, P.R. Palmer, Modeling Bipolar Power Semiconductor Devices, Morgan & Claypool Publishers, 2013. http://www.morganclaypool.com/doi/suppl/10.2200/S00483ED1V01Y201302PEL005/suppl_file/Gachovska_Ch1.pdf, s.l.
[67] P. Leturcq, O. Berraies, J.L. Debrie, P. Gillet, M. Kallala, J. L. Massol, Bipolar Semiconductor Device Models for Computed-Aided Design in Power Electronics, EPE, 1995, pp. 1222–1227.
[68] A. Braynt, Simulation and Optimization of Diode and IGBT Interaction in a Chopper Cell (Ph.D. dissertation), University of Cambridge, 2005. s.l.
[69] H.S. levels, W. Gerlach, On the effective carrier lifetime in p-s-n rectifiers at high injection, Solid State Electron. 12 (1969) 267–275.
[70] J.L. Hudgins, T.K. Gachovska, Optimization of Forward Voltage Drop for Si, SiC, and GaN High Voltage Diode, Consum. Electron. Times 2 (4) (2013).
[71] J.L. Hudgins, T. Gachovska, Comparison of the forward voltage drop of Si and SiC high voltage diodes, ECS Trans. 64 (7) (2014).
[72] B.M. Wilamowski, Schottky diodes with high breakdown voltages, Solid State Electron. 26 (5) (1983) 491–493.
[73] C. Severt, A. Agarwal, R. Singh, S.H. Ryu, Design of dual use, high efficiency, 4H-SiC Schottky and MPS diodes, in: Energy Conversion Engineering Conference and Exhibit, 2000. (IECEC) 35th Intersociety, Las Vegas, NV, 2000.
[74] J.N. Shenoy, J.A. Cooper, M.R. Melloch, High-voltage double implanted power MOSFETs in 6H-SiC, IEEE Electron Device Lett. 18 (3) (1997) 93–95.

[75] A. Alok, E. Arnold, R. Egloff, J. Barone, J. Murphy, R. Conrad, J. Burke, 4H-SiC RF power MOSFET, IEEE Electron Device Lett. 22 (12) (2001) 557–558.
[76] S. Ryu, C. Jonas, B. Heath, J. Richmond, A. Agarwal, J. Palmour, 950V, 8.7mohm-cm2 high speed 4H-SiC power DMOSFETs, in: Material Research Society Spring Meeting, San Francisco: s.n, 2006, pp. 391–400.
[77] A. Saha, J.A. Cooper, A 1-kV 4H-SiC power DMOSFET optimized for low on-resistance, IEEE Trans. Electron Dev. 54 (10) (2007) 2786–2791.
[78] A.K. Agarwal, J.B. Casady, L.B. Rowland, W.F. Valek, M.H. White, C.D. Brandt, 1.1kV 4H-SiC power UMOSFET's, IEEE Electron Device Lett. 18 (12) (1997) 586–588.
[79] K. Fujihira, N. Miura, T. Watanabe, Y. Nakao, N. Yutani, K. Ohtsuka, M. Imaizumi, T. Takami, T. Oomori, Realization of low on-resistance 4H-SiC power MOSFETs by using retrograde profile in P-body, Mater. Sci. Forum 556–557 (2007) 827–830.
[80] Y. Sugawara, L. Asano, 1.4 kV 4H-SiC UMOSFET with low specific on-resistance, in: 10th International Symposium on Power Semiconductor Devices and ICs, Kyoto, 1998, pp. 119–122. s.n.
[81] S.H. Ryu, A. Agarwal, J. Richmond, J. Palmour, N. Saks, J. Williams, 27 mΩ-cm2, 1.6 kV power DiMOSFETs in 4H-SiC, in: 14th International Symposium on Power Semiconductor Devices and ICs, Santa Fe, 2002, pp. 65–68. s.n.
[82] S.H. Ryu, S. Krishnaswami, B. Hull, B. Heath, M. Das, J. Richmond, A. Agarwal, J. Palmour, J. Scofield, Development of 8 mΩ − cm2, 1.8 kV 4H-SiC DMOSFETs, Mater. Sci. Forum 527–529 (2) (2006) 1261–1264.
[83] S.H. Ryu, S. Krishnaswami, M. Das, B. Hull, J. Richmond, B. Heath, A. Agarwal, J. Palmour, J. Richmond, 10.3 mohm-cm2, 2 kV power DMOSFETs in 4H-SiC, in: 17th Int. Symp. Power Semicond. Devices &IC's, 2005, pp. 275–278.
[84] J. Spitz, M.R. Melloch, J.A. Cooper Jr., M.A. Capano, 2.6 kV 4H-Sic lateral DMOSFET's, IEEE Electron Device Lett. 19 (4) (1988) 100–102.
[85] Y. Li, J.A. Cooper, M.A. Capano, High-voltage (3 kV) UMOSFETs in 4H-SiC, IEEE Trans. Electron Dev. 49 (6) (2002) 972–975.
[86] S.H. Ryu, S. Krishnaswami, A. Agarwal, J. Richmond, J. Palmour, Development of 10 kV 4H-SiC power DMOSFETs, Mater. Sci. Forum 457–460 (2004) 1385–1388.
[87] H. Robert, S. Buchoff, S. Van Campen, T. McNutt, A. Ezis, B. Bettina, C. Kirby, M. Sherwin, R. Clarke, R. Singh, A 10-kV large-area 4H-SiC power DMOSFET with stable subthreshold behavior independent of temperature, IEEE Trans. Electron Dev. 55 (8) (2008) 1807–1815.
[88] S.H. Ryu, S. Krishnaswami, M. Das, J. Richmond, A. Agarwal, J. Palmour, J. Scofield, 10 kV 123 mΩ − cm2 4H-SiC power DMOSFETs, IEEE Electron Device Lett. 25 (8) (2004) 556–558.
[89] S.H. Ryu, S. Krishnaswami, B. Hull, J. Richmond, A. Agarwal, A. Hefner, 10 kV, 5A 411-SiC Power DMOSFET, in: 18th International Symposium on Power Semiconductor Devices & IC's, Naples, Italy: s.n, 2006.
[90] Y. Sui, T. Tsuji, J.A. Cooper Jr., On-state characteristics of SiC power UMOSFETs on 115-μm drift Layers, IEEE Electron Device Lett. 26 (4) (2005) 255–257.
[91] C.Y. Lu, J.A. Cooper Jr., T. Tsuji, G. Chung, J.R. Williams, K. McDonald, L.C. Feldman, Effect of process variations and ambient temperature on electron mobility at SiO2/4H-SiC interface, IEEE Trans. Electron Dev. 50 (7) (2003) 1582–1588.
[92] M. Matin, A. Saha, J.A. Cooper Jr., A self-aligned process for high voltage, short-channel vertical DMOSFETs in 4H-SiC, IEEE Trans. Electron Dev. 51 (10) (2004) 1721–1725.
[93] A.K. Agarwal, R.R. Siergeij, S. Seshadri, M.H. White, P.G. Mcmullin, A. A. Burk, L.B. Rowland, C.D. Brandt, R.H. Hopkins, Critical materials, device design, performance and reliability issues in 4H-SiC power UMOSFET structures, Mat. Res. Soc. Symp. Proc. 423 (1996) 87–92.
[94] P.M. Shenoy, B.J. Baliga, The planar 6H-SiC ACCUFET: a new high-voltage power MOSFET structure, IEEE Electron. Dev. Lett. 18 (1997) 589–591.
[95] A. Blicher, Field_Effect and Bipolar Power Transistor Physics, Academic Press, New York, 1981.
[96] R. Fu, A. Grekov, J. Hudgins, A. Mantooth, E. Santi, Power SiC DMOSFET Model accounting for nonuniform current distribution in JFET region, IEEE Trans. Ind. Appl. 48 (1) (2012) 181–190.
[97] H. Choi. Overview of Silicon Carbide Power Devices. s.l.: Fairchild Semiconductor, https://www.fairchildsemi.co.kr/Assets/zSystem/documents-archive/collateral/technicalArticle/Overview-of-Silicon-Carbide-Power-Devices.pdf.
[98] K. Mino, S. Herold, J.W. Kolar, A gate drive circuit for silicon carbide JFET, in: Industrial Electronics Society, 2003, IECON '03. The 29th Annual Conference of the IEEE, 2003.
[99] S. Round, M. Heldwein, J. Kolar, I. Hofsajer, P. Friedrichs, A SiC JFET driver for a 5 kW, 150 kHz three-phase PWM converter, in: Conference Record of the 2005 Industry Applications Conference, Fourtieth IAS Annual Meeting, 2005.
[100] E. Platania, Z. Chen, F. Chimento, L. Lu, E. Santi, A. Raciti, J. Hudgins, A. Mantooth, D. Sheridan, J. Cassady, A physics-based model for a SiC JFET device accounting for the mobility dependence on temperature and electric field, in: Industry Applications Society Annual Meeting. IAS '08. IEEE, Edmonton, 2008.
[101] C. Cai, W. Zhou, K. Sheng, Characteristics and application of normally-Off SiC-JFETs in converters without antiparallel diodes, EEE Trans. Power Electr. 28 (2013) 4850–4860.
[102] Final Datasheet Silicon Carbide- Junction Field Effect Transistor 1200 V CoolSiC™ Power Transistor IJW120R100T1. s.l.: Infineon Technologies AG, Vol. 2013.
[103] Datasheet C2M0040120D silicon carbide power MOSFET C2M MOSFET Technology, Cree, Inc., Durham, 2014.
[104] M. Bakowski, Prospects and development of vertical normally-off JFETs in SiC, J. Telecommun. Inform. Technol. 4 (2009) 25–36.
[105] S.-H. Ryu, A.K. Agarwal, R. Singh, J.W. Palmour, 1800 V NPN bipolar junction transistors in 4H-SiC, IEEE Electron Device Lett. 22 (3) (2001) 124–126.
[106] H.S. Lee, M. Östling, 1200-V 5.2-mΩ • cm2 4H-SiC BJTs with a high common-emitter current gain, IEEE Electron Device Lett. 28 (11) (2007) 1007–1009.
[107] M. Domeij, H.-S. Lee, E. Danielsson, C.-M. Zetterling, M. Östling, A. Schöner, Geometrical effects in high current gain 1100-V 4HSiC BJTs, IEEE Electron Device Lett 26 (10) (2005) 743–745.
[108] A.K. Agarwal, S. Krishnaswami, J. Richmond, C. Capell, S.-H. Ryu, J. Palmour, S. Balachandran, T.P. Chow, S. Bayne, B. Geil, C. Scozzie, Evolution of the 1600 V, 20 A SiC bipolar junction transistors, in: 17 International Symposium on Power Semiconductor Devices & IC's, Santa Barbara, CA: s.n., 2005, pp. 271–274.
[109] H. Miyake, T. Kimoto, J. Suda, 4H-SiC bipolar junction transistors with record current gains of 257 on (0001) and 335 on (000–1), in: IEEE 23rd International Symposium on Power Semiconductor Devices and ICs, San Diego, 2011.

[110] N. Ohtani, Recent progress in SiC single crystal wafer technology, in: The 5th International Symposium on Advanced Science and Technology of Silicon Materials (JSPS Si Symposium), Kona, Hawaii, USA: s.n., 2008.
[111] S. Balachandran, C. Li, P.A. Losee, I.B. Bhat, T.P. Chow, 6 kV 4H-SiC BJTs with specific on-resistance below the unipolar limit using a selectively grown base contact process, in: The 19th International Symposium on Power Semiconductor Devices and ICs, Jeju Island: s.n., 2007, pp. 293–296.
[112] T. Hudgins, J.L. Gachovskaa, Comparison of the forward voltage drop of Si and SiC high voltage diodes, ECS Trans. 64 (7) (2014) 223–236.
[113] J. Wang, A.Q. Huang, B.J. Baliga, RBSOA study of high voltage SiC bipolar devices, in: 21st International Symposium on Power Semiconductor Devices & IC's, 2 ISPSD, 2009, pp. 263–266.
[114] Q. Zhang, C. Jonas, S. Ryu, A. Agarwal, J. Palmour, Design and fabrications of high voltage IGBTs on 4H-SiC, in: IEEE International Symposium on Power Semiconductor Devices and IC's, 2006.
[115] Q. Zhang, C. Jonas, J. Sumakeris, A. Agarwal, J. Palmour, 12 kV 4H-SiC p-IGBTs with record low specific on-resistance, in: Int. Conf. Silicon Carbide and Related Materials (ICSCRM), Otsu, Japan: s.n., 2007.
[116] M. Das, Q. Zhang, R. Callanan, C. Capell, J. Claytou, M. Donfrio, S. Haney, F. Husna, C. Jonas, J. Richmond, J.J. Sumakeris, A 13 kV 4H-SiC N-channel IGBT with lowRdiff, on and fast switching, in: Int. Conf. Silicon Carbide and Related Materials (ICSCRM), Otsu, Japan: s.n., 2007.
[117] Y. Sui, X. Wang, J.A. Cooper, High-voltage self-aligned p-channel DMOS-IGBTs in 4H-SiC, IEEE Electron Device Lett 28 (8) (2007) 728–730.
[118] E. van Brunt, L. Cheng, M.J. O'Loughlin, J. Richmond, V. Pala, J. Palmour, C.W. Tipton, C. Scozzie, 27 kV, 20 A 4H-SiC n-IGBTs, Mater. Sci. Forum 821–823 (2015) 847–850.
[119] K. Sheng, F. Udrea, G.A.J. Amaratunga, Optimum carrier distribution of the IGBT, Solid State Electron. 44 (9) (2000) 1573–1583.
[120] M.K. Das, R. Callanan, D.C. Capell, B. Hull, F. Husna, J. Richmond, M. O'loughlin, M.J. Paisley, A. Powell, Q. Zhang, 20th International Sympo … Help Working with Abstracts, in: 20th International Symposium on Power Semiconductor Devices and IC's, Browse Conference Publications, Orlando, 2008.
[121] S. Ryu, C. Capel, l.C. Jonas, Y. Lemma, M. O'Loughlin, J. Clayton, E. Van Brunt, K. Lam, J. Richmond, A. Burk, D. Grider, S. Allen, J. Palmour, A. Agarwal, A. Kadavelugu, S. Bhattacharya, Ultra high voltage IGBTs in 4H-SiC, in: Wide Bandgap Power Devices and Applications (WiPDA), IEEE Workshop on, Columbus, 2013.
[122] S. Chowdhury, T.P. Chow, Performance tradeoffs for ultra-high voltage (15 kV to 25 kV) 4H-SiC n-channel and p-channel IGBTs, in: Power Semiconductor Devices and ICs (ISPSD), 28th International Symposium, 2016.
[123] A. Bryant, S. Yang, P. Mawby, D. Xiang, L. Ran, P. Tavner, P.R. Palmer, Investigation into IGBT dV/dt during turn-off and its temperature dependence, IEEE Trans. Power Electron 26 (10) (2011) 3019–3031.
[124] W. Sung, J. Wang, A. Huang, B. Baliga, Design and investigation of frequency capability of 15kV 4H-SiC IGBT, in: 21st International Symposium on Power Semiconductor Devices & IC's, 2009.
[125] S. Ryu, C. Capell, C. Jonas, L. Cheng, M. O'Loughlin, A. Burk, A. Agarwal, J. Palmour, A. Hefner, Ultra high voltage (>12 kV), high performance 4H-SiC IGBTs, in: 24th International Symposium on Power Semiconductor Devices and ICs, 2014.
[126] T. Tamaki, G.G. Walden, Y. Sui, J.A. Cooper, Optimization of on-state and switching performances for 15–20-kV 4H-SiC IGBTs, IEEE Trans. Electron Dev. 5 (8) (2008) 1920–1927.
[127] X. Kang, A. Caiafa, E. Santi, J.L. Hudgins, P.R. Palmer, Characterization and modeling of high-voltage field-stop IGBTs, IEEE Trans. Ind. Appl. 39 (4) (2003) 922–928.
[128] L.L. Lai, Power system restructuring and deregulation: trading, performance and information technology, John Wiley & Sons, Ltd, New York, 2001. s.l.
[129] A.K. Agarwal, J.B. Casady, L.B. Rowland, S. Seshadri, R.R. Siergiej, W.F. Valek, C.D. Brandt, 700-V asymmetrical 4H-SiC gate turn-off thyristors (GTOs), IEEE Electron Device Lett. 18 (1997) 518.
[130] A.K. Agarwal, B. Damsky, J. Richmond, S. Krishnaswami, C. Capell, S.H. Ryu, J.W. Palmour, The first demonstration of the 1 cm x 1 cm SiC thyristor chip, in: The 17 International Symposium on Power Semiconductor Devices & IC's, Santa Barbara: s.n., 2005, pp. 195–198.
[131] CREE, Cree Silicon Carbide Substrates and Epitaxy, Product Specifications, Cree. INC, Durham, NC, 2013.
[132] T. Kimoto, T. Hiyoshi, T. Hayashi, J. Suda, Impacts of recombination at the surface and in the substrate on carrier lifetimes of n-type 4H–SiC epilayers, J. Appl. Phys. 108 (8) (2010). s.l.
[133] T. Hayashi, K. Asano, J. Suda, T. Kimoto, Impacts of reduction of deep levels and surface passivation on carrier lifetimes in p-type 4H-SiC epilayers, 109 (2011) 114502–114504.
[134] L. Cheng, A.K. Agarwal, C. Capell, M. O'Loughlin, E.V. Brunt, K. Lam, J. Richmond, A. Burk, J.W. Palmour, H. O'Brien, A. Ogunniyi, C. Scozzie, 20 kV, 2 cm2, 4H-SiC gate turn-off thyristors for advanced pulsed power applications, in: Plasma Science (ICOPS), Abstracts IEEE International Conference on, San Francisco, 2013.
[135] T. Boles, C. Varmazis, D. Carlson, L. Xia, D. Jin, T. Palacios, G. W. Turner, R.J. Molnar, High-voltage GaN-on-silicon Schottky diodes, CS MSNTECH, New Orleans, 2013. May 13th–16th.
[136] T. Takeuchi, H. Amano, K. Hiramatsu, N. Sawaki, I. Akasaki, Growth of single crystalline GaN film on Si substrate using 3C-SiC as an intermediate layer, J. Cryst. Growth 115 (1991) 1–4. s.l.
[137] A. Watanabe, T. Takeuchi, K. Hirosawa, H. Amano, K. Hiramatsu, I. Akasaki, The growth of single crystalline GaN on a Si substrate using AIN as an intermediate layer, J. Cryst. Growth 128 (1993) 1–4. s.l.
[138] J.W. Yang, C.J. Sun, Q. Chen, M.Z. Anwar, M.S. Khan, S. A. Nikishin, G.A. Seryogin, A.V. Osinsky, L. Chernyak, H. Temkin, C. Hu, S. Mahajan, High quality GaN–InGaN heterostructures grown on (111) silicon substrates, Appl. Phys. Lett. 96 (1996). s.l.
[139] Y. Nakakda, I. Aksenov, H. Okumura, GaN heteroepitaxial growth on silicon nitride buffer layers formed on Si (111) surfaces by plasma-assisted molecular beam epitaxy, Appl. Phys. Lett. 73 (1998) 827–829. s.l.
[140] Z. Keyan, W. Lianshan, C.S. Jin, C.V. Thompson, Evolution of AlN buffer layers on silicon and the effect on the property of the expitaxial GaN film, 2003. s.l.: http://hdl.handle.net/1721.1/3713.
[141] J. Songa, W. Lua, J.S. Flynnb, G.R. Brandes, AlGaN/GaN Schottky diode hydrogen sensor performance at high temperatures with different catalytic metals, Solid State Electron. 49 (2005) 1330–1334.

[142] V. Kumar, L. Zhou, D. Selvanathan, I. Adesida, Thermally-stable low-resistance Ti/Al/Mo/Au multilayer ohmic contacts on n–GaN, Appl. Phys. 92 (2002) 1712–1714.
[143] Z.M. Zhao, R.L. Jiang, P. Chen, D.J. Xi, H.Q. Yu, B. Shen, R. Zhang, Y. Shi, S.L. Gu, Y.D. Zheng, Ti/Al/Pt/Au and Al ohmic contacts on Si-substrated GaN, Appl. Phys. Lett. 79 (218) (2001) 218–221. s.l.
[144] W.C.B. Peatman, T.W. Crowe, M. Shur, B. Gelmont, A Schottky/2-DEG Varactor Diode for Millimeter and Submillimeter Wave Multiplier Applications, in: Third International Symposium on Space Terahertz Technology, Michigan, 1992.
[145] T.F. Changa, C.F. Huanga, T.Y. Yangb, C.W. Chiub, T.Y. Huangb, K.Y. Leec, F. Zhao, Low Turn-on voltage dual metal AlGaN/GaN Schottky barrier diode, Solid State Electron. 105 (2015) 12–15.
[146] H.S. Lee, D.Y. Jung, Y. Park, J. Na, H.G. Jang, H.S. Lee, C.H. Jun, J. Park, S.O. Ryu, S.C. Ko, E.S. Nam, 0.34 VT AlGaN/GaN-on-Si large Schottky barrier diode with recessed dual anode metal, IEEE Electron Device Lett. 36 (11) (2015) 1132–1134.
[147] H. Zhu, N. Zongyang, Y. Kazuki, C. Xiaodong, J. Yu, K. Wayne, J. Erhard, X. Debdeep, G. Huili, 1.9 kV AlGaN/GaN lateral Schottky barrier diodes on silicon, IEEE Electron Device Lett. 34 (2015) 375–377. s.l.
[148] T. Kachi, T. Uesugi, Which are the future GaN power devices for automotive applications, lateral structures or vertical structures? in: CS MANTECH Conference, Palm Springs, California, 2011.
[149] Y. Zhang, M. Sun, Z. Liu, T. Palacios, Electrothermal simulation and thermal performance study of gan vertical and lateral power transistors, IEEE Trans. Electron Dev. 60 (7) (2013) 2224–2230.
[150] I.C. Kizilyalli, A.P. Edwards, H. Nie, D.P. Bour, 400-A (Pulsed) vertical GaN p-n diode with breakdown voltage of 700 V, IEEE Electron Device Lett. 35 (6) (2014) 654–656.
[151] H. Morkoç, Handbook of Nitride Semiconductors and Devices: Electronic and Optical Processes in Nitrides, Wiley-VCH Verlag GmbH, Weinheim, Germany, 2008.
[152] C. Chu, C.C. Yu, Y.K. Wang, J.Y. Tsai, F.I. Lai, S.C. Wang, Low-resistance ohmic contacts on p-type GaN using Ni/Pd/Au metallization, Appl. Phys. Lett. 77 (21) (2000) 3423–3426.
[153] T.K. Gachovska, Consumer Electronics Times, Optimization of forward voltage drop for Si, SiC, and GaN high voltage diode, Consum. Electron. Times 2 (4) (2013).
[154] J.R. Dickerson, et al., Vertical GaN power diodes with a bilayer edge termination, IEEE Trans. Electron Dev. 63 (1) (2016) 419–425.
[155] X. Zou, X. Zhang, X. Lu, C.W. Tang, K.M. Lau, Breakdown ruggedness of quasi-vertical GaN-based p-i-n diodes on Si substrates, IEEE Electron Device Lett. 37 (9) (2016) 1158–1161.
[156] Y. Zhang, M. Sun, D. Piedra, M. Azize, X. Zhang, T. Fujishima, T. Palacios, GaN-on-Si vertical Schottky and p-n diodes, IEEE Electron Device Lett. 35 (6) (2014) 618–620.
[157] I.C. Kizilyalli, T. Prunty, O. Aktas, 4-kV and 2.8-mΩ-cm2 vertical GaN p-n diodes with low leakage currents, IEEE Electron Device Lett. 36 (10) (2015). s.l.
[158] I.C. Kizilyalli, A.P. Edwards, O. Aktas, T. Prunty, D. Bour, Vertical power p-n diodes based on bulk GaN, IEEE Trans. Electron Dev. 62 (2) (2015). s.l.
[159] Y. Zhang, et al., Origin and Control of OFF-State Leakage Current in GaN-on-Si Vertical Diodes, IEEE Trans. Electron Dev. 62 (7) (2015). s.l.
[160] K. Ip, K.H. Baik, B. Luo, F. Ren, S.J. Pearton, S.S. Park, Y.J. Park, A. P. Zhang, High current bulk GaN Schottky rectifiers, Solid State Electron. 46 (7) (2002). s.l.
[161] A.M. Baliga, B.J. Ozbek, Planar nearly ideal edge-termination technique for GaN devices, IEEE Electron Device Lett. 32 (3) (2011). s.l.
[162] I. C. Kizilyalli, H. Nie, A. P. Edwards, L. Romano, D. P. Bour, R. J. Brown, T. R. Prunty. Method and System for Gan Vertical JFET Utilizing a Regrown Gate. s.l.: US20160190351 A1, 2016.
[163] S. Chowdhury, D. Ji, Design of 1.2 kV power switches with low RON using GaN-based vertical JFET, IEEE Trans. Electron Dev. 62 (8) (2015). s.l.
[164] H. Nie, A. Edwards, I. Kizilyalli, D. Bour, T.R. Prunty, Region, Lateral GaN JFET With Vertical Drift. s.l.: United States Patent Application Publication, Vol. US20140131721 A1, 2014.
[165] I.C. Aktas, O. Kizilyalli, Characterization of vertical GaN p–n diodes and junction field-effect transistors on bulk GaN down to cryogenic temperatures, 30, Semiconductor Science and Technology, 2015. http://iopscience.iop.org/article/10.1088/0268-1242/30/12/124001, s.l.
[166] J. Zeng, G. Dolny, C. Kocon, R. Stokes, N. Kraft, L. Brush, T. Grebs, J. Hao, R. Ridley, J. Benjamin, L. Skurkey, S. Benczkowski, D. Semple, P. Wodarczyk, C. Rexer, An ultra dense trench-gated power MOSFET technology using a self-aligned process, Proceedings of the 13th International Symposium on Power Semiconductor Devices and ICs, Osaka, 2001.
[167] T. Oka, T. Ina, Y. Ueno, J. Nishii, Over 10 a operation with switching characteristics of 1.2 kV-class vertical GaN trench MOSFETs on a bulk GaN substrate, 28th International Symposium on Power Semiconductor Devices and ICs, Prague, 2016.
[168] R. Pierret, Semiconductor Device Fundamentals, Addison-Wesley Publishing ompany, Inc, Boston, MA, 1996.
[169] C. Gupta, S.H. Chan, Y. Enatsu, A. Agarwal, S. Keller, U.K. Mishra, OG-FET: An in-situ Oxide, GaN interlayer based vertical trench MOSFET, s.l.: IEEE Electron Device Lett 99 (2016) 1601–1604.
[170] H. Otake, S. Egami, H. Ohta, Y. Nanishi, H. Takasu, GaN-based trench gate metal oxide semiconductor field effect transistors with over 100 cm2/(V-s) channel mobility, Jpn. J. Appl. Phys. 46 (25) (2007). s.l.
[171] M. Kodama, M. Sugimoto, E. Hayashi, N. Soejima, O. Ishiguro, M. Kanechika, K. Itoh, H. Ueda, T. Uesugi, T. Kachi, GaN-based trench gate metal oxide semiconductor field-effect transistor fabricated with novel wet etching, Appl. Phys. Express 1 (2) (2008). s.l.
[172] H. Otake, K. Chikamatsu, A. Yamaguchi, T. Fujishima, H. Ohta, Vertical GaN-based trench gate metal oxide semiconductor field-effect transistors on GaN bulk substrates, Appl. Phys. Express 1 (1) (2008). s.l.
[173] Y. Niiyama, T. Shinagawa, S. Ootomo, H. Kambayashi, T. Nomura, S. Kato, High-power operation of normally-off GaN MOSFETs, Furukawa Rev. 36 (2009). s.l.
[174] H.M.J. Vaes, J.A. Appels, HV thin layer devices (RESURF Devices), in: Intlernational Electron Devices Meeting, Washington, DC, 1979.
[175] W. Huang, T.P. Chow, Y. Niiyama, T. Nomura, S. Yoshida, Lateral implanted RESURF GaN MOSFETs with BV up to 2.5 kV, in: Proceedings of the 20th International Symposium on Power Semiconductor Devices & IC's, Orlando, 2008.
[176] W. Huang, T.P. Chow, Y. Niiyama, T. Nomura, S. Yoshida, 730V, 34mΩ-cm2 lateral epilayer RESURF GaN MOSFET, in: 21st International Symposium on Power Semiconductor Devices & IC's, Barselona, 2009.
[177] W. Huang, T. Khan, T.P. Chow, Enhancement-mode n-channel GaN MOSFETs on p and n-GaN/Sapphire Substrates, IEEE Electron Device Lett. 27 (10) (2006). s.l.

[178] O. Ambacher, J. Smart, J.R. Shealy, N.G. Weimann, K. Chu, M. Murphy, W.J. Schaff, L.F. Eastman, R. Dimitrov, L. Wittmer, M. Stutzmann, W. Rieger, J. Hilsenbeck, wo-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures, J. Appl. Phys. 85 (6) (1999). s.l.

[179] T.E. Kazior, R. Chelakara, W. Hoke, J. Bettencourt, T. Palacios, H. S. Lee, High performance mixed signal and rf circuits enabled by the direct monolithic heterogeneous integration of GaN HEMTs and Si CMOS on a silicon substrate, in: Compound Semiconductor Integrated Circuit Symposium (CSICS), 2011 IEEE, 2011.

[180] W. Saito, T. Nitta, Y. Kakiuchi, Y. Saito, K. Tsuda, I. Omura, M. Yamaguchi, On-resistance modulation of high voltage GaN HEMT on sapphire substrate under high applied voltage, IEEE Electron Device Lett. 28 (8) (2007). s.l.

[181] S.T. Sheppard, K. Doverspike, W.L. Pribble, S.T. Allen, J. W. Palmour, L.T. Kehias, T.J. Jenkins, High-power microwave GaN/AlGaN HEMTs on semi-insulating, IEEE Electron Device Lett. 20 (4) (1999). s.l.

[182] K.K. Chu, P.C. Chao, M.T. Pizzella, R. Actis, D.E. Meharry, K. B. Nichols, R.P. Vaudo, X. Xu, J.S. Flynn, J. Dion, G.R. Brandes, 9.4 W/mm power density AlGaN-GaN HEMTs on free-standing GaN substrates, IEEE Electron Device Lett. 25 (9) (2004). s.l.

[183] K. Lorenz, M. Gonsalves, W. Kim, V. Narayanan, S. Mahajan, Comparative study of GaN and AlN nucleation layers and their role in growth of GaN on sapphire by metalorganic chemical vapor deposition, Appl. Phys. Lett. 77 (2000). s.l.

[184] J.W. Leea, S.H. Junga, H.Y. Shina, I.H. Leeb, C.W. Yanga, S.H. Leea, J.B. Yooa, Effect of buffer layer on the growth of GaN on Si substrate, J. Cryst. Growth 237-239 (2002). 2. s.l.

[185] Y. Wu, P. Parikh, U. Mishra, High Voltage Gan Transistor. US20120223366 A1 September 6, 2012.

[186] M.T. Hasan, T. Kojima, H. Tokuda, M. Kuzuhara, Effect of sputtered SiN passivation on current collapse of AlGaN/GaN HEMTs, in: CS MANTECH Conference, New Orleans, Louisiana, USA, 2013.

[187] J. Chen, H. Wakabayashi, K. Tsutsui, H. Iwai, K. Kakushima, Poly-Si gate electrodes for AlGaN/GaN HEMT with high reliability and low gate leakage current, Microelectron. Reliab. 63 (2016). s.l.

[188] G. Vacca, GaN-based HEMT improvement using advanced structures, Semiconductor Today Compounds Advanced Silicon 7 (7) (2013). s.l.

[189] W. Saito, Y. Kakiuchi, T. Nitta, Y. Saito, T. Noda, H. Fujimoto, A. Yoshioka, T. Ohno, M. Yamaguchi, Field-plate structure dependence of current collapse phenomena in high-voltage GaN-HEMTs, IEEE Electron Device Lett. 31 (7) (2010). s.l.

[190] T.H. Brennan, K.F. Yu, Theoretical study of the two-dimensional electron mobility in strained III-nitride heterostructures, J. Appl. Phys. 89 (2001). s.l.

[191] L. Hsu, W. Walukiewicz, Electron mobility in AlxGa1 − xN/GaN heterostructures, Phys. Rev. B 56 (1997). s.l.

[192] T. Li, R.P. Joshi, C. Fazi, Monte Carlo evaluations of degeneracy and interface roughness effects on electron transport in AlGaN-GaN heterostructures, J. Appl. Phys. 88 (2000). s.l.

[193] R. Gaska, M.S. Shur, A.D. Bykhovski, A.O. Orlov, G.L. Snider, Electron mobility in modulation-doped AlGaN–GaN heterostructures, Appl. Phys. Lett. 74 (1999). s.l.

[194] H.X. Guang, Z.D. Gang, J. De-Sheng, Formation of two-dimensional electron gas at AlGaN/GaN heterostructure and the derivation of its sheet density expression, Chin. Phys. B 24 (6) (2015). s.l.

[195] S. Heikman, S. Keller, Y. Wu, J.S. Speck, S.P. DenBaars, U.K. Mishra, Polarization effects in AlGaN/GaN and GaN/AlGaN/GaN heterostructures, J. Appl. Phys. 93 (2003). s.l.

[196] A. Asgari, M. Kalafi, L. Faraone, The effects of GaN capping layer thickness on two-dimensional electron mobility in GaN/AlGaN/GaN heterostructures, Phys. E. 25 (2005). s.l.

[197] D. Jena, Polarization Induced Electron Populations in III-V Nitride Semiconductors Transport, Growth, and Device Applications, University of California, Santa Barbara, 2003.

[198] S. Kolluri, S. Keller, D. Brown, G. Gupta, S. Rajan, S.P. DenBaars, U. K. Mishra, Influence of AlN interlayer on the anisotropic electron mobility and the device characteristics of N-polar AlGaN/GaN metal-insulator-semiconductor-high electron mobility transistors grown on vicinal substrates, J. Appl. Phys. 108 (2010).

[199] M. Charfeddine, H. Belmabrouk, M. Ali Zaidi, H. Maaref, 2-D theoretical model for current-voltage characteristics in AlGaN/GaN HEMT's, J. Mod. Phys. 3 (2012).

[200] A. Lidow, J. Strydom, M. de Rooij, D. Reusch, GaN Transistors for Efficient Power Conversion, Wiley, Chichester, United Kingdom, 2014. s.l.

[201] Note, GaN Systems Application. How to Drive GaN Enhancement Mode Power Switching Transistors, s.l. : GaN Systems.Inc., 2014.

[202] A. Bindra, Startup Unveils Plan to Build GaN Power ICs, Electronics 360 Powered by IEE Global Spec, 2016. s.l.

[203] T.K. Gachovska, C. Gerolami, Comparison of Si and GaN-FETs in a VAR compensation application, in: Electrical Power and Energy Conference, Ottawa, 2016.

[204] PCB Thermal Design Guide for GaN Enhancement Mode Power Transistors, Note, GaN System Inc. Application, 2016, http://www.ecomal.com/fileadmin/Datenblaetter/GaN_Systems/App_Notes/GN005_App_Note-PCB_Thermal_Design_Guide_for_GaN_Enhancement_Mode_Power_Transistors.pdf.

[205] S.M. Sze, G. Gibbons, Avalanche breakdown voltages of abrupt and linearly graded p-n Junctions in Ge, Si, GaAs, and GaP, Appl. Phys. Lett. 8 (1967) 111–113.

[206] M. Trivedi, K. Shenai, Performance evaluation of high power wide band-gap semiconductor rectifiers, J. Appl. Phys. 85 (9) (1999) 6889–6897.

[207] W. Fulopa, Calculation of avalanche breakdown voltages of silicon p-n junctions, Solid State Electron. 10 (1) (1967) 39–43.

Further Reading

[1] W.B. Shockley, Circuit element utilizing semiconductor material. US patent 2,569,347, 1948.

[2] B.J. Baliga, M.S. Adler, R.P. Love, P.V. Gray, N.D. Zommer, The insulated gate transistor: A new three-terminal MOS-controlled bipolar power device, IEEE Trans. Electron Dev. 31 (6) (1984) 821–828.

[3] http://www.cree.com/products/pdf/1700V%20Sales%20Sheet.pdf.

[4] Y. Luo, J. Zhang, P. Alexandrov, L. Fursin, J.H. Zhao, T. Burke, High voltage (>1 kV) and high current gain (32) 4H-SiC power BJTs using Al-free ohmic contact to the base, IEEE Electron Device Lett. 24 (11) (2003) 695–697.

[5] V.C. Huang, J.A. Cooper Jr., 4H-SiC NPN bipolar junction transistors with BVCEO >3200, in: 14th International Symposium on Power Semiconductor Devices and ICs, 2002, pp. 57–60.

[6] J.H. Zhao, J. Zhang, P. Alexandrov, X. Li, T. Burke, A high voltage (1,750V) and high current gain (β = 24.8) 4H-SiC bipolar junction transistor using a thin (12 μm) drift layer, Mater. Sci. Forum 457–460 (2004) 1173–1176.

[7] S. Krishnaswami, A. Agarwal, J. Richmond, C. Capell, S.-H. Ryu, J. Palmour, B. Geil, D. Katsis, C. Scozzie, High temperature characterization of 4H-SiC bipolar junction transistors, Mater. Sci. Forum 527–529 (2006) 1437–1440.
[8] Q.J. Zhang, A. Agarwal, A. Burk, B. Geil, C. Scozzie, 4H–SiC BJTs with current gain of 110, Solid State Electron. 52 (2008) 1008–1010.
[9] H. Lee, M. Domeij, R. Ghandi, C.M. Zetterling, M. Östling, High-current-gain SiC BJTs with regrown extrinsic base and etched JTE, IEEE Trans. Electron Dev. 55 (8) (2008) 1894–1898.
[10] J. Zhang, Y. Luo, P. Alexandrov, L. Fursin, J.H. Zhao, A high current gain 4H-SiC NPN power bipolar junction transistor, IEEE Electron Device Lett. 24 (2003) 327–329.
[11] J. Zhang, P. Alexandrov, T. Burke, J.H. Zhao, 4H-SiC power bipolar junction transistor with a very low specific on-resistance of 2.9 mΩ • cm2, IEEE Electron Device Lett. 27 (5) (2006) 368–370.
[12] J. Zhang, P. Alexandrov, J.H. Zhao, High Power(500V-70A) and high gain(44-47) 4H-SiC bipolar junction transistors, Mater. Sci. Forum 457–460 (2004) 1149–1152.
[13] S. Round, M. Heldwein, J. Kolar, I. Hofsajer, P. Friedrichs, A SiC JFET driver for a 5 kW, 150 kHz three-phase PWM converter, in: Fourtieth IAS Annual Meeting - Industry Applications Conference, Vol. 1, 2005, pp. 410–416.
[14] http://www.semiconductor-today.com/news_items/2009/OCT/SEMISOUTH_051009.htm October 5, 2009.
[15] P. Friedrichs, H. Mitlehner, R. Schorner, K.O. Dohnke, R. Elpelt, D. Stephani, The vertical silicon carbide JFET—a fast and low loss solid state power switching device, EPE, Graz, Austria, 2001. s.n.
[16] P. Friedrichs, H. Mitlehner, R. Schorner, K.O. Dohnke, R. Elpelt, D. Stephani, Stacked High Voltage Switch Based on Sic VJFETs, ISPSD, Cambridge, UK, 2003, pp. 139–142.
[17] K. Asano, Y. Sugawara, T. Hayashi, S. Ryu, R. Singh, J. Palmour, D. Takayama, 5kV 4H-SiC SEJFET with Low RonS of 69m12cm2, in: ISPSD'02, Santa Fe, 2002, pp. 61–64.
[18] J. Wua, J. Hua, J.H. Zhao, X. Wang, X. Li, L. Fursin, T. Burke, Normally-off 4H-SiC trench-gate MOSFETs with high mobility, Solid State Electron. 52 (6) (2008) 909–913.
[19] P. Friedrichs, H. Mitlehner, R. Schorner, K.O. Dohnke, R. Elpelt, D. Stephani, High voltage, modular switch based on Sic VJFETs – first results for a fast 4,5kV/1.2 Ohm configuration, in: ECSCRM2002, Linkiiping, 2002.
[20] Q. Zhang, H.R. Chang, M. Gomez, C. Bui, E. Hanna, J.A. Higgins, T. I. Smith, J.R. Williams, 10 kV trench gate IGBTs on 4H-SiC, in: The 17th International Symposium on Power Semiconductor Devices and ICs, 2005, pp. 303–306.
[21] A.K. Agarwal, S.H. Ryu, R. Singh, O. Kordina, J.W. Palmourl, 2600 V, 12 A, 4H-SiC, asymmetricalgate turn-off (GTO) thyristor development, Mater. Sci. Forum 338–342 (2000) 1387–1390.
[22] S.V. Campen, A. Ezis, J. Zingaro, G. Storaska, R.C. Clarke, V. Temple, M. Thompson, T. Hansen, 7 kV 4H-SiC GTO Thyristors, in: MRS Proceedings, 742, 2002. K7.7.
[23] J. Wang, A.Q. Huang, Design and Characterization of High-Voltage Silicon Carbide Emitter Turn-off Thyristor, IEEE Trans. Power Electron. 24 (5) (2009) 1189–1197.
[24] Y. Sugawara, D. Takayama, K. Asano, A. Agarwal, S. Ryu, J. Palmour, S. Ogata, 12.7 kV ultra high voltage SiC commutated gate turn-off thyristor: SICGT, in: Intemational Symposium on Power Semiconductor Devices & ICs, Kitakyushu, 2004, pp. 365–368.
[25] G. Paques, S. Scharnholz, N. Dheilly, D. Planson, R.W. De Doncker, High-voltage 4H-SiC thyristors with a graded etched junction termination extension, IEEE Electron Device Lett. 32 (10) (2011) 1421–1423.
[26] V. Anantharam, K.N. Bhat, Analytical solutions for the breakdown voltages of punched-through diodes having curved junction boundaries at the edges, IEEE Trans. Electron Dev. 27 (5) (1980) 939–945.
[27] E. Santi, J.L. Hudgins, H.A. Mantooth, Variable model levels for power semiconductor devices, in: The 2007 Summer Computer Simulation Conference, San Diego, 2007, pp. 276–283.
[28] C.L. Ma, P.O. Lauritzen, P.Y. Lin, I. Budihardjo, A systematic approach to modeling of power semiconductor devices based on charge control principles, in: IEEE PESC Rec, Taipei, 1994, pp. 31–37.
[29] N. Talwalkar, P.O. Lauritzen, B. Fatemizadeh, D. Perlman, C.L. Ma, A power BJT model for circuit simulation, in: 27th Annual IEEE Power Electronics Specialists Conference, Baveno, Italy, vol. 1, 1996, pp. 50–55.
[30] C.L. Ma, P.O. Lauritzen, A physics-based GTO model for circuit simulation, in: Power Electronics Specialists Conference, Atlanta, vol. 2, 1995, pp. 872–878.
[31] Z. Hossain, K.J. Olejniczak, H.A. Mantooth, E.X. Yang, C.L. Ma, A physics-based MCT circuit model using the lumped-charge modeling approach, IEEE Trans. Power Electron. 16 (2) (2001) 264–272.
[32] I. Budihardjo, P.O. Lauritzen, C. Xu, Simulation of high frequency PWM and Quasi-resonant converters using the lumped-charge power MOSFET model, in: Applied Power Electronics Conference and Exposition, APEC '94, vol. 2, 1994, pp. 1042–1048.
[33] H.K. Gummel, H.C. Poon, An integral charge-control model of bipolar transistors, Bell Syst. Tech. J. 49 (1970) 827–852.
[34] G. Massobrio, P. Antognetti, Semiconductor Device Modeling With SPICE, McGraw-Hill, Inc., New York, NY, USA, 1993. s.l.
[35] G.M. Kull, L.W. Nagel, S.W. Lee, P. Lloyd, E.J. Prendergast, H. Dirks, A unified circuit model for bipolar transistors including quasi-saturation effects, IEEE Trans. Electron Dev. 32 (1985) 1103–1113.
[36] M. Pong, R. Jackson, Simulation of power transistor in its circuit environment, in: IEEE Industry Applications Society Annual Meeting Conference Record, Toronto, Canada: s.n., 1985, pp. 894–899.
[37] H. Jeong, J. Fossum, A charge-based large signal bipolar transistor model for device and circuit simulation, IEEE Trans. Electron Dev. 36 (1) (1987) 124–131.
[38] D. Roulston, J. Quoirin, Simulation of highvoltage power switching transistors under forced gain and inductive load turn-off conditions, Solid State Electron Dev. 135 (1) (1988) 7–12.
[39] H. Goebel, R. Kraus, H.J. Mattausch, A Hybrid method for modeling semiconductor power devices, in: Power Electronics Specialists Conference, Seattle: s.n., 1993, pp. 45–52.
[40] H.Z. Fardi, Modeling dc gain performance of 4H-SiC BJTs, Int. J. Comput. Math. Electr. Electron. Eng. 26 (5) (2007) 1236–1246.
[41] J.J. Ebers, J.L. Moll, Large-signal behavior of junction transistors, Proc. IRE 42 (1954) 1761–1772.
[42] G. Brezeanu, Silicon carbide (SiC): a short history. An analytical approach for SiC power device design, Semiconductor Conference, 2005. CAS 2005 International, 2 (2005) 345–348.
[43] S.E. Saddow, A. Agarwal (Eds.), Advances in Siliconl Carbide Processing an Applications, Artech House Inc, Boston, 2004.

[44] H.J. Round, A note on carborundum, Electr. World 19 (1907) 309–310.
[45] H. Baumhauer, Über die Kristalle des Carborundums, Z. Kristallogr. 50 (1912) 33–39.
[46] J.A. Lely, Silidum carbide von Art und Mendge der eingebeunten verunreininungen, Ber. Dt. Keram. Ges. 32 (1955) 229–231.
[47] Y.M. Tairov, V.F. Tsvetkov, Investigation of growth processes of ingots of silicon carbide single crystals, J. Cryst. Growth 43 (1978) 209–212.
[48] J. Zhang, T. Burke, Implantation-free 4H-SiC bipolar junction transistors with double base epilayers, IEEE Electron Device Lett 29 (5) (2008) 471–473.
[49] B.J. Baliga, Silicone Carbide Power Devices, World Scientific Co. Pte. Ltd, 2005. s.l.
[50] C. Xu, D. Schroeder, A power bipolar junction transistor model describing static and dynamic behaviour, IEEE Trans. Power Electron. 7 (4) (1992) 734–740.
[51] C.L. Ma, P.O. Lauritzen, P. Türkes, H.J. Mattausch, A physically-based Lumped-charge SCR Model, in: Power Electronics Specialists Conference, Seattle: s.n., 1993, pp. 53–59.
[52] H. Matsunami, S. Nishino, H. Ono, IVA-8 heteroepitaxial growth of cubic silicon carbide on foreign substrates, IEEE Trans. Electron Dev. 28 (1981) 1235–1236.
[53] Bridgestone Develops 5-Inch Semi-Conductor Wafer, http://rubbermarketnews.net/2011/08/bridgestone-develops-5-inch-semiconductor-wafer/ August 29, 2011. (Cited: October 17, 2011).
[54] H. Föll, Ramsdell Notation for SiC Polytypes, http://www.tf.uni-kiel.de/matwis/amat/semi_en/kap_a/basics/ba_1_1.html (Online 2008). (Cited: October 17, 2011).
[55] T.T. Han, Y. Fu, H. Ågren, P. Han, Z. Qin, R. Zhang, Room-temperature photoluminescence of doped 4H-SiC film grown on AlN/Si(100), Appl. Phys. A Mater. Sci. Process. 86 (2007) 145–149.
[56] V. Veliadis, T. McNutt, M.S. nook, H. Hearne, P. Potyraj, J. Junghans, C. Scozzie, Large area silicon carbide vertical JFETs for 1200 V cascode switch operation, Int. J. Power Manag. Electron. 2008 (2008) 523721, 8.
[57] P.R. Palmer, E. Santi, J.L. Hudgins, X. Kang, J.C. Joyce, P.Y. Eng, Circuit simulator models for the diode and IGBT with full temperature dependent features, IEEE Trans. Power Electron. 18 (5) (2003) 1220–1229.
[58] A.T. Bryant, P.R. Palmer, E. Santi, J.L. Hudgins, A compact diode model for the simulation of fast power diodes including the effects of avalanche and carrier lifetime zoning, in: Power Electronics Specialists Conference, PESC '05. IEEE 36th, 2005, pp. 2042–2048.
[59] X. Wang, A. Caiafa, J.L. Hudgins, E. Santi, P.R. Palmer, Implementation and Validation of a Physics-based Circuit Model forIGCT with Full Temperature Dependencies, Implementation and Validation of a Physics-based Circuit Model for, Aachen, Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual, Germany, 2004. s.n.
[60] W.S. Loh, B.K. Ng, J.S. Ng, S.I. Soloviev, C.H. Young, P.M. Sandvik, C.M. Johnson, J.P.R. David, Impact ionization coefficients in 4H-SiC, IEEE Trans. Electron Dev. 55 (8) (2008) 1984–1990.
[61] L.F. Shampine, M.W. Reichelt, The MATLAB ODE suite, SIAM J. Sci. Comput. 18 (1) (1997) 1–22.
[62] P.B. Klein, J.A. Freitas Jr., S.C. Binari, A.E. Wickenden, Observation of deep traps responsible for current collapse in GaN metal semiconductor field effect transistors, Appl. Phys. Lett. 75 (1999) 4016–4018.
[63] P.B. Klein, J.A. Freitas Jr., S.C. Binari, A.E. Wickenden, Observation of deep traps responsible for current collapse in GaN metal–semiconductor field-effect transistors, Appl. Phys. Lett. 75 (1999) 4016–4018.
[64] General Properties of Silicon Carbide. https://www.ifm.liu.se/semicond/local_info/popular/Chapter2.html (Cited: February 20, 2012).
[65] H. Föll, Siliconcarbide—Materials Aspects. http://www.tf.uni-kiel.de/matwis/amat/semi_en/kap_a/backbone/ra_1_1.html (Cited: February 20, 2012).
[66] http://www.tf.uni-kiel.de/matwis/amat/semi_en/kap_a/backbone/ra_1_1.html.
[67] A. Elasser, M. Kheraluwala, M. Ghezzo, R. Steigerwald, N. Evers, J. Kretchmer, T.P. Chow, A comparative evaluation of new silicon carbide diodes and state-of-the-art silicon diodes for power electronic applications, IEEE Trans. Ind. Appl. 39 (4) (2003) 915–921.
[68] A. Bryant, K. Xiaosong, E. Santi, P. Palmer, J. Hudgins, Two-step parameter extraction procedure with formal optimization for physics-based circuit simulator IGBT and p-i-n diode models, IEEE Trans. Power Electron. 21 (2) (2006) 295–309.
[69] V. Bougrov, M.E. Levinshtein, S.L. Rumyantsev, A. Zubrilov, in: M.E. Levinshtein, S.L. Rumyantsev, M.S. Shur (Eds.), Properties of Advanced Semiconductor Materials GaN, AlN, InN, BN, SiC, SiG, John Wiley & Sons, Inc., New York, 2001.
[70] M. Bayer, R. Kraus, K. Hoffman, A precise model for the DC and transient characteristics of BJT's, in: Power Electronics Specialists Conference, 1994, pp. 64–68.
[71] T.K. Hudgins, J.L. Gachovska, Optimization of forward voltage drop for Si, SiC, and GaN High voltage diode, Consum. Electron. Times 2 (2013) 4. s.l.
[72] X. Song, A. Huang, M. Lee, C. Peng, L. Cheng, H. O'Brien, A. Ogunniyi, C. Scozzie, J. Palmour, 22 kV SiC Emitter turn-off (ETO) thyristor and its dynamic performance including SOA, in: 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD), Hong Kong, 2015.
[73] T. Gachovska, J.L. Hudgins, Comparison of the forward voltage drop of Si and SiC high voltage diodes, ECS Trans 64 (7) (2014). s.l.
[74] C. Gupta, S.H. Chan, Y. Enatsu, A. Agarwal, S. Keller, U.K. Mishra, s.l.: IEEE Electron Device Lett., 37 (12) (2016) 1601–1604.
[75] K.M. Bothe, D.W. Barlage, Underlying design advantages for GaN MOSFETs compared with GaN HFETs for power applications, J. Comput. Electron. 13 (1) (2014). s.l.
[76] E. Mitani, H. Haematsu, S. Yokogawa, J. Nikaido, Y. Tateno, Mass-production of high-voltage GaAs and GaN devices, in: CS MANTECH 2006, Vancouver, British Columbia, Canada, 2006.

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6

Power Electronic Modules

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6.1 Introduction

A power electronic module or power module is an assembly containing several power components, mostly power semiconductor devices, properly internally interconnected to perform a power conversion function. It is an integrated building block for the realization of a power converter with a reduced number of external components required. Control electronics such as gate drivers, sensing, and protection functions may be included inside the power module package. In this case, the term intelligent power module (IPM) is commonly used. From the electric standpoint, the power module reduces parasitic elements in the interconnection of the power semiconductor devices due to the tight physical integration. From the thermal standpoint, the power module usually has a thermally conductive baseplate that can be bolted to a heat sink or a cold plate to remove the loss heat generated as a result of power converter operation. From the mechanical standpoint, it provides a robust mechanical package for the power components inside. In conclusion, a power module is an electro-thermo-mechanical device optimized for power converter operation. Using a power module may simplify the design of a power converter because the power module design provides a robust mechanical structure and guarantees proper operation from an electric and thermal point of view as long as the module datasheet specifications and guidelines are followed. Power modules are typically used at higher power levels, where a discrete component implementation would require paralleling of several power semiconductor devices.

Advantages of power modules are tight integration of multiple power semiconductor devices, high current and power ratings because multiple power semiconductor dies can be paralleled inside the module, good thermal management, and mechanical robustness. Probably, the biggest advantage is the reduction of parasitic elements, in particular parasitic inductances, due to the tight integration. These parasitic elements cause additional losses and overshoot and ringing during converter operation, which cause electromagnetic interference (EMI) issues. The parasitic element reduction allows switching converter operation at higher frequency, which reduces passive

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filtering element size, and may provide additional system-level advantages, such as quiet converter operation at switching frequencies above the audible range.

The main disadvantage of power modules is probably a higher cost compared with discrete devices. A second disadvantage is that a specific application may require characteristics not available in commercial modules on the market.

In this article, power electronic modules will be described mostly from the point of view of a power module user, somebody who wants to use a power module to realize a power converter rather than the point of view of the designer of a power module.

In Section 6.2, the differences between discrete devices and modules are discussed. Section 6.3 gives an example of a power module. Section 6.4 briefly describes the manufacturing process of power modules. Section 6.5 describes various types of modules and the types of power semiconductor devices used in them. Section 6.6 discusses thermal management and Section 6.7 module reliability. Finally, Section 6.8 provides design guidelines and considerations for the use of power modules.

6.2 Discrete Power Devices Versus Power Modules

Fig. 6.1 shows a photo of two discrete semiconductor components—a power metal-oxide-semiconductor field-effect transistor (MOSFET) and a diode—and a power module. The power module is a half-bridge configuration realized with silicon insulated-gate bipolar transistors (IGBTs). The module ratings are from 1200 V to 100 A. Notice that the power module has multiple power and control connections. The module of Fig. 6.1 has three large screw-type power connections for the power terminals and four smaller pin-type connections on top for the IGBT gate terminals. The bottom of the module has a metal baseplate that can be bolted to a heat sink for thermal management. Two of the baseplate holes for heat sink mount can be clearly seen at the bottom. Notice that a discrete component contains a single power semiconductor device in an individual package, whereas the power module contains multiple power semiconductor devices. A second difference is that for discrete devices, the metal plate for heat sink connection, if provided like in the discrete MOSFET of Fig. 6.1, is typically nonisolated, whereas in the power module, all semiconductor devices are thermally coupled to the baseplate but are electrically isolated from it. In the TO220 discrete MOSFET, the metal tab is electrically connected to the drain of the MOSFET, and electric isolation must be provided as part of the heat sink mount.

6.3 An Example of Power Module

In this section, an example of an IGBT half-bridge power module is described. The physical structure of the power module with labeled terminal connections is shown in Fig. 6.2.

The equivalent circuit of the module is shown in Fig. 6.3 with labeled terminals. The top IGBT, called IGBT1, has collector terminal C1 and emitter terminal E1. The gate and emitter Kelvin terminals are called G1K and E1K, respectively (Kelvin contacts are discussed in Section 6.8.3). Labeling is similar for IGBT2, the bottom IGBT. Note that the module contains four distinct semiconductor devices, two IGBTs and

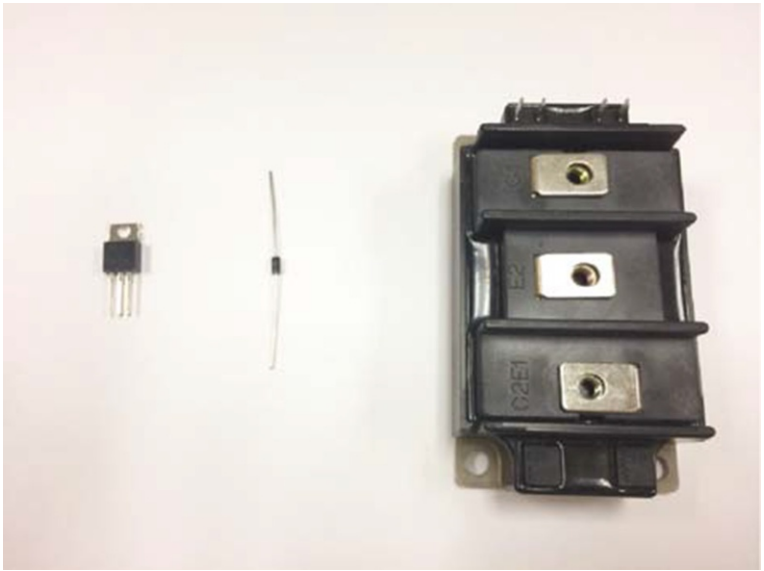


FIG. 6.1 From left to right: photo of a discrete power MOSFET in TO220 package, a discrete leaded diode, and a power electronic module (Toshiba MG100Q2YS1).



FIG. 6.2 Photo of Toshiba MG100Q2YS1 IGBT half-bridge power module with labeled terminals.

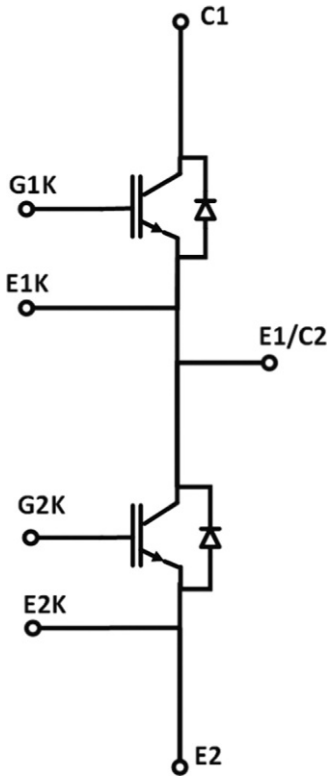


FIG. 6.3 Equivalent circuit of Toshiba MG100Q2YS1 power module.

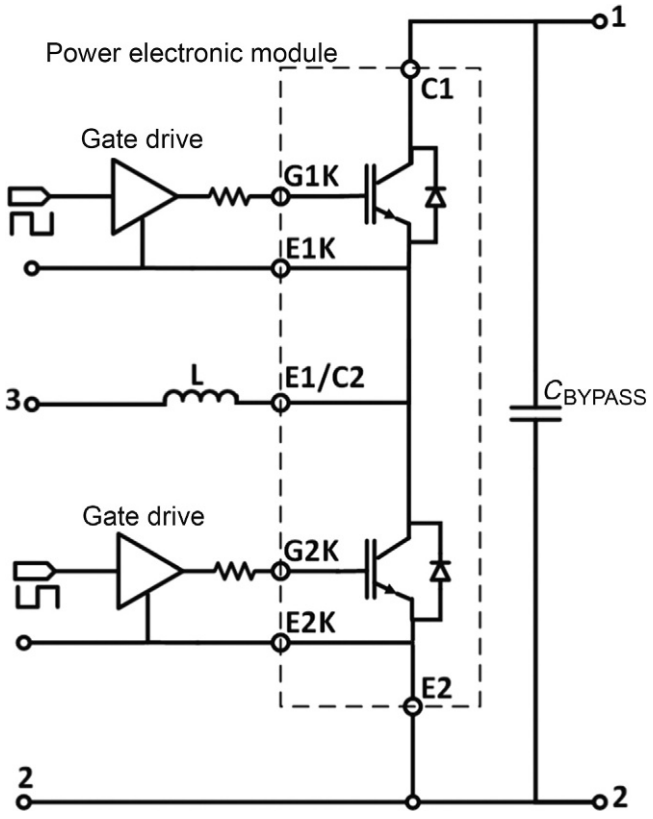


FIG. 6.4 Equivalent circuit of power electronic module with some of the external components needed for switching converter realization.

two diodes. Each of these may consist of a single die or multiple dies connected in parallel to achieve higher current capability.

The IGBT half-bridge power module can be used to realize different switching power converters such as a bidirectional DC-DC converter (buck type in one direction and boost type in the other direction) or a single-phase two-level inverter. Three modules could be combined to create a three-phase inverter, but in that case, using a single three-phase module may be more convenient. Some of the external components required to realize a switching power converter are shown in Fig. 6.4. First of all, gate drivers are required to control the IGBTs. In a switching converter, the two IGBTs are turned on in a complementary fashion, so that, when one IGBT is on, the other one is off. The gate driver controls should introduce a short dead time during which both switches are off to prevent shoot-through, that is, shorting capacitor C_{BYPASS}. Second, a bypass capacitor C_{BYPASS} is required to filter the square-

wave current at the switching frequency drawn by the power module during operation. As will be described later, capacitor C_{BYPASS} should be a high-frequency capacitor and should be placed physically close to the module to minimize interconnection parasitic inductance, which causes overshoot and ringing during switching operation. Finally, an inductor L is required to filter the square-wave voltage at the switching frequency created at node E1/C2 by the switching action. Sources and loads can then be connected to the 1-2 and 3-2 ports.

6.4 Manufacturing Process

As mentioned above, power modules contain multiple power devices internally interconnected to realize a specific power processing function, such as the IGBT half-bridge module package shown in Fig. 6.2. As shown in the equivalent circuit of Fig. 6.3, this module contains multiple IGBT and diode chips interconnected to form a half-bridge topology. Physically, a power module is an integration of semiconductor chips, wire bonds, direct bonded copper (DBC) substrate, solder, baseplate, silicone gel, terminals, housing, and so on as shown in Fig. 6.5. The manufacturing process includes attaching chips on the DBC substrate, bonding wires, attaching the DBC substrate to the baseplate, placing the top housing, and filling it with silicone gel. Each element of the generic power module of Fig. 6.5 has a specific function, and its selection depends on many factors. The semiconductor chips are selected to provide the required voltage and current ratings. The DBC substrate provides electric isolation but good thermal coupling between the chips and the baseplate, so that heat generated on the chips can be efficiently conducted to the baseplate. The top copper layer provides the required electric connections among the bottom terminals of the chips. Wire bonds provide the required electric connections for the top terminals of the chips and connections to the module terminals. The baseplate provides mechanical support for the module and can be connected to a heat sink for heat removal. These elements and the techniques used for power module assembly will be described more in detail in the following subsections.

6.4.1 Semiconductor Chips

The semiconductor chips form the core of a power electronic module. Fig. 6.6 shows the interior of a power electronic module with semiconductor chips mounted on a DBC substrate and interconnected with wire bonds. Semiconductor chips determine the voltage, current, and power ratings of the power module. Power modules with different internal interconnections of semiconductor chips are available to realize different power converter topologies such as half bridge and full bridge. To achieve high-current capability, multiple semiconductor chips can be paralleled inside the module. The performance of power modules in terms of on-resistance, switching speed, and power loss is critically dependent on the semiconductor chip characteristics.

6.4.2 Die Attach

Die attach is the process of attaching a die/chip to a substrate or package. For example, in the power module of Fig. 6.5, the IGBT chip and the diode chip are attached to the top copper layer of the DBC substrate. Note that in case of vertical chip devices, the device power terminals are on opposite sides of the chip, and therefore, the chip current flows through the die attach joint. Die attach is usually accomplished by using one of the following processes: (1) eutectic, (2) solder, (3) adhesive, (4) glass or silver glass:

1) A *eutectic bond* is formed by melting a preform consisting of a mixture or alloy of two or more dissimilar metals in the joint between the die and substrate. The preform has a melting point that is lower than the melting point of its base materials. For example, considering a typical

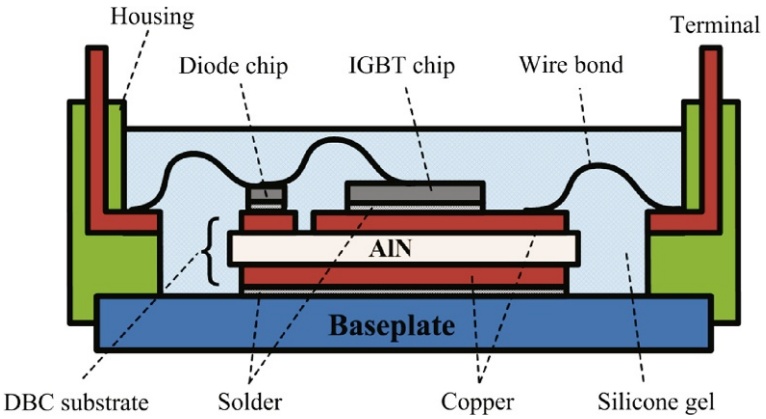


FIG. 6.5 Cross section of IGBT power electronic module.

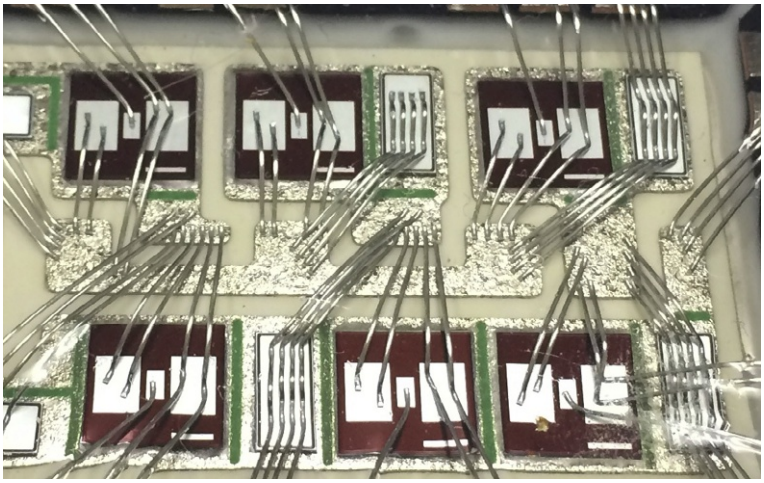


FIG. 6.6 Top view of power module interior showing semiconductor chips mounted on DBC substrate with wire bond interconnections.

preform composed of gold and silicon, the melting point of gold is 1640°C, and the melting point of silicon is 1414°C. However, when the materials are combined in a preform, the melting point drops to 363°C [1].

2) *Solder* is an attaching method commonly used in the semiconductor industry. Solder attach provides good mechanical strength, high thermal conductivity, and good electric conductivity. Lead-based solder has been popular for a long time with advantages of good performance, proved technology, and low cost. However, environmental concerns about the toxic properties of lead have recently arisen. As a result, lead-free solder is gradually replacing lead-based solder in many applications.
3) An *adhesive* bond is formed by attaching the die to the substrate using some type of adhesive material. It can be electrically insulating or conductive depending on the adhesive material used. An advantage of adhesive bonding is that it is performed at room temperature and does not require high temperatures.
4) A *glass bond* is formed by attaching the die to the substrate using glass in paste form. The glass paste may also contain silver particles that enhance thermal and electric conductivity (this is called silver-glass die bonding). The glass bonding process is similar to adhesive bonding. The differences are the material used and the need for heat. Glass bonds are heated to 350–450°C that melts the glass into a low viscosity liquid. The glass hardens as it cools, thereby making the bond [1].

6.4.3 Wire Bonds

The electric connections between the top connections of semiconductor chips and module terminals are realized by wire bonding (shown in Figs. 6.5 and 6.6). Conventional wire bonding materials include aluminum (Al), copper (Cu), and gold (Au). Aluminum is the most common material for power modules because of its low cost and convenient process, especially to form thick wires for high-current capability. Gold has the lowest resistivity and good high-frequency performance and is usually used for integrated circuit and high-frequency devices. Due to limited improvement of resistance in power module and high cost, gold is not commonly used in power modules. The electric properties of copper are intermediate between those of Al and Au, whereas the cost of aluminum is significantly lower than copper. Consequently, Al wire bonds are most common with copper used in special cases.

To satisfy high-current requirements, heavy wire bonding (Fig. 6.7) has been developed. Traditional wire size is smaller than 10 mils (1 mil = 1/1000 in.) in diameter, whereas heavy wire bonding is significantly thicker and can save space on the bonding pad. An alternative solution is ribbon bonding (Fig. 6.8), which has the added advantage of better high-frequency performance [2]. Ribbon bonding is a form of wedge bonding using flat ribbon to replace the round wire. Compared with round wire, ribbon wire can carry higher current at high frequency, where skin effect is the limiting factor, and has smaller effective inductance and less signal cross talk [3].

6.4.4 DBC Substrate

The DBC substrate is an important interface between the electric components in the power module and the external cooling system [4]. It consists of a ceramic insulator layer with copper bonded to one or both sides by a high-temperature melting and diffusion process. DBC substrates provide electric conduction on the top copper layer, electric isolation from top to bottom thanks to the ceramic insulator layer, and outstanding thermal conduction from top to bottom. The top copper layer is etched

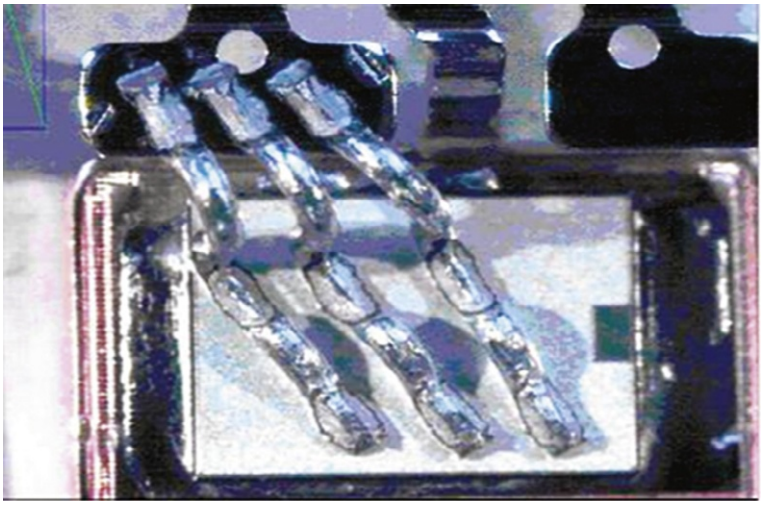


FIG. 6.7 Heavy wire bonding.

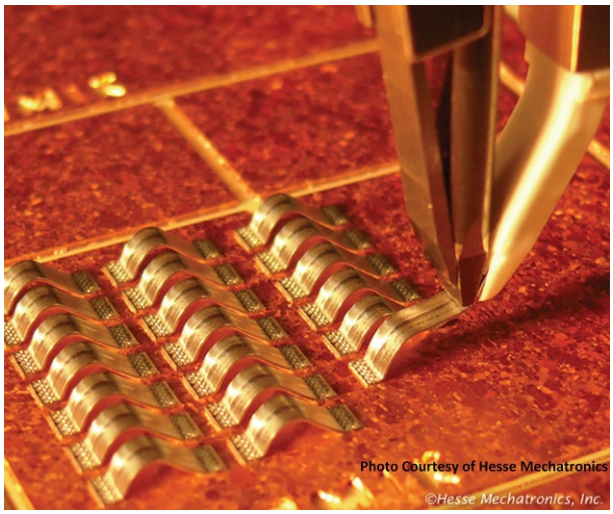


FIG. 6.8 Ribbon bonding.

to form the required electric interconnections and is electrically connected to the backside electrodes of semiconductor chips using one of the die attach techniques described above, most commonly by soldering. The excellent electric isolation is provided by the ceramic material. The two most common choices are alumina (Al_2O_3) and aluminum nitride (AlN). Al_2O_3 is inexpensive and widely used; however, it has the disadvantages of having relatively low thermal conductivity (24–28 W/m K) and of being brittle. Compared with Al_2O_3, AlN is more expensive, but it has better mechanical and thermal performance (thermal conductivity larger than 150 W/m K) and therefore has become popular in high-temperature applications [5]. The bottom copper layer is usually not patterned and is soldered to the baseplate to achieve heat spreading from top to bottom. One important thermal characteristic of DBC substrates is a low coefficient of thermal expansion (CTE), which is close to that of silicon. This ensures good thermal cycling performance and higher reliability.

6.4.5 Baseplate

One of the main functions of the baseplate is to provide mechanical support for the electric components and the DBC substrate. At the same time, it must propagate the heat generated by the semiconductor chips to the external heat sink effectively. A high degree of surface smoothness is also required to guarantee no voids between the baseplate and the DBC substrate, because voids can cause hot spots that will eventually lead to cracking and poor reliability [4]. In order to reduce the thermal resistance of the interface between the baseplate and the heatsink, a thin layer of thermal grease (also called thermal paste or heatsink compound) is applied between the baseplate and the heat sink. The purpose of

the thermal grease is to fill up voids due to interface surface imperfections, because air in these voids acts as an excellent thermal insulator. However, thermal grease is not a good thermal conductor, so a thick layer of thermal grease may actually *increase* the thermal resistance between the baseplate and the heat sink.

CTE mismatch is a key consideration in power module design and needs to be addressed in each connection and attachment between two different materials inside the power module. To improve power module mechanical reliability, adjacent materials should have closely matched CTEs, so that, when the module heats up and cools down during operation, the adjacent materials expand and contract in a similar way, avoiding the development of mechanical stress, which can cause joint failure due to mechanical fatigue. This is particularly important for large-area connections, which may develop larger mechanical stress during thermal cycling. Therefore, the baseplate material should be thermally compatible with the DBC substrate material, and mechanical, chemical, and other factors also need to be considered.

The housing and silicone gel are used to insulate the electric components on the top of the module and prevent contamination. In modern IPMs, thermal sensors are attached to the DBC close to the chips, to measure the real-time junction temperature, which is very useful for device condition monitoring.

6.5 Types of Power Electronic Modules

There are several different types of power electronic modules available on the market today. They come in different shapes and sizes and can be categorized either by the power processing topology used or by the power semiconductor devices used.

6.5.1 A Survey of Power Electronic Module Topologies

A brief survey of power electronic module topologies is now given:

Diode rectifier or thyristor rectifier: Four (or more) diodes or thyristors are connected in a bridge circuit configuration that converts an AC input (typically either single phase or three phase) into a DC output. A full-bridge and a three-phase bridge diode rectifier are shown in Fig. 6.9. For an example of a three-phase module, see Ref. [6].

- Half-bridge, full-bridge, or three-phase (six-pack) power module: Generally, these power modules, shown in Fig. 6.10, are implemented with either power MOSFETs or IGBTs (insulated-gate bipolar transistors). Typically, IGBTs can achieve much higher current and voltage ratings, allowing them to operate at higher power levels with reduced conduction losses, whereas MOSFETs can operate at much higher switching frequencies, making them suitable for application where fast switching and high power density are required. A half-bridge configuration can be used to implement a DC-DC power-bidirectional converter or a single-phase inverter. A full-bridge configuration can be used to implement a full-bridge converter or a three-level single-phase inverter. A six-pack power module can be used to implement a three-phase inverter or a three-phase-controlled rectifier. Note that since all switches are controllable, all these converter topologies are power bidirectional, that is, power can flow in both directions. For an example of a six-pack power module, see Ref. [7].
- Converter-inverter-brake (CIB) module: The module, shown in Fig. 6.11, contains a single-phase or three-phase uncontrolled or half-controlled bridge rectifier (C) plus an inverter (I) and a brake chopper (B). This module contains all power semiconductor devices required to implement a three-phase variable motor drive fed by three-phase power. The three-phase diode rectifier can be used to create a DC bus voltage that supplies the three-phase inverter connected to the three-phase motor. The chopper circuit allows to pulse-width modulate a braking resistor to dissipate energy during regenerative braking. See Ref. [8] for more information about regeneration in motor drives.

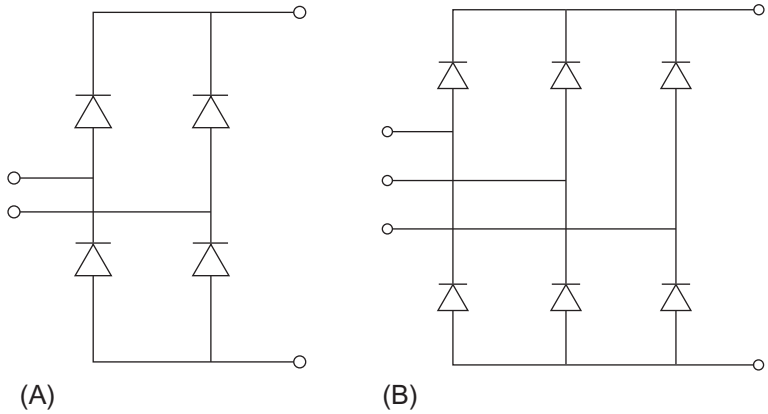


FIG. 6.9 Diode rectifier: single-phase full-bridge (A) and three-phase (B) configuration.

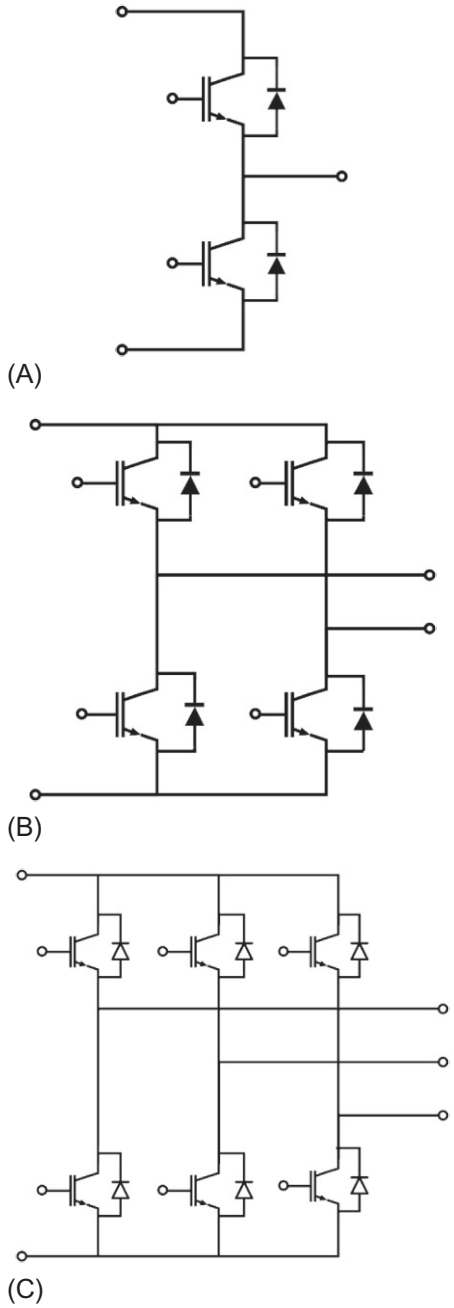


FIG. 6.10 Circuit diagram of a half-bridge (A), full-bridge (B), and a three-phase six-pack power module (C).

- Neutral-point-clamped (NPC) module: Each leg has four power switches connected in series. The applied voltage on the power switch is one-half that of a two-level converter. The NPC topology can allow operation at voltages larger than the voltage rating of a single power device. In addition, NPC converter can achieve lower output current ripples and improve the total harmonic distortion (THD) of the output.
- Power factor correction (PFC) module: PFC module combines a rectifying function and a PFC function in order to reduce the harmonics of the input current and improve power factor.

6.5.2 Power Semiconductor Devices Used in Power Electronic Modules

The most common power semiconductor devices used in power electronic modules are diodes, MOSFETs, IGBTs, and thyristors. Power bipolar junction transistors (BJTs) are less common and are briefly mentioned for completeness.

1. Power diode:

   Power diodes provide uncontrolled rectification of power and are used in applications such as AC-DC converters and variable-frequency drives. Typically, the power diode can be either a P-i-N diode or a Schottky diode.

   The P-i-N diode is a bipolar device having a so-called P-i-N structure, that is, it is a p-n junction with a wide, undoped intrinsic semiconductor layer (i-layer) in the middle to sustain a reverse blocking voltage. Frequently, the midlayer, rather than being intrinsic, has low N-doping and is therefore called N- (N minus) layer. Fig. 6.12 shows the basic structure of a P-i-N diode. In the forward-biased conduction, the diode has a forward conduction drop, which causes conduction loss, and the diode can be modeled as a junction voltage source, equal to the threshold voltage, and a series equivalent resistance that represents the increasing slope in the diode I-V characteristics. In the reverse-biased condition, a small reverse leakage current flows, which increases gradually with the applied reverse voltage. If the applied reverse voltage exceeds a certain voltage, called breakdown voltage, the reverse current becomes very large due to avalanche breakdown, and the diode may be destroyed due to large power dissipation in the device. The advantage of a P-i-N diode is low on-state voltage drop in high-current conduction, due to the minority carrier injection in epitaxial drift region resulting in conductivity modulation. However, the minority carrier injection during conduction causes a large reverse recovery current during diode turnoff, which is not desirable, because it causes additional turn-on loss in the active switch.

   The Schottky diode is a very attractive unipolar device, formed by an electrically nonlinear contact between a metal and a semiconductor bulk region shown in Fig. 6.13. It has low on-state voltage drop, almost zero reverse recovery charge, and extremely high switching

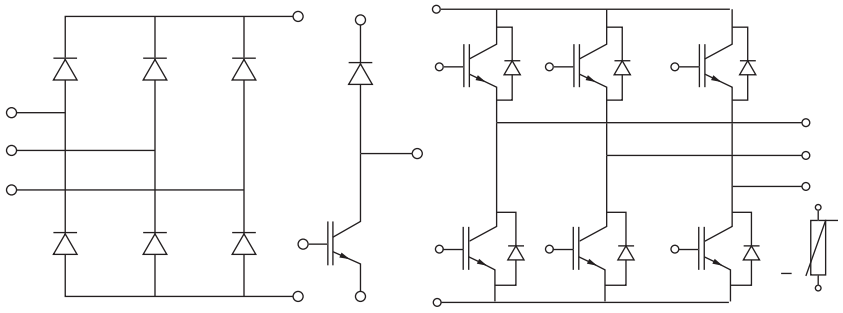


FIG. 6.11 CIB module including a three-phase uncontrolled rectifier, a brake chopper, and a three-phase IGBT inverter. A temperature-sensing thermistor is also included.

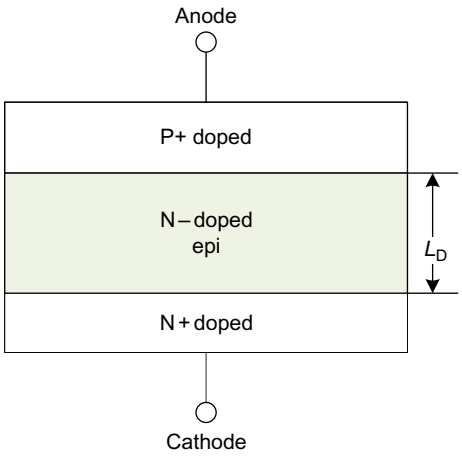


FIG. 6.12 Basic structure of a P-i-N diode.

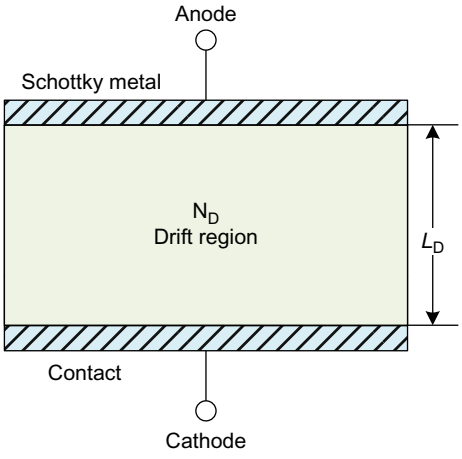


FIG. 6.13 Basic structure of a Schottky diode.

speed, but its reverse leakage current is large especially at high temperature due to its lower built-in potential barrier. Additionally, the breakdown voltage of Schottky diode is limited by the increase of drift region resistance without any conductivity modulation effect.

2. Power MOSFET

The power metal-oxide-semiconductor field-effect transistor (MOSFET) is a unipolar, majority carrier, and voltage-controlled device. It is one of the most commonly used power devices due to its easy gate driving, fast switching speed, and low loss dissipation. Most power MOSFETs feature a vertical structure (a structure of alternating p-type and n-type doping) shown in Fig. 6.14. In most power MOSFETs, the N+ source and P-well junction are shorted to prevent the parasitic bipolar transistor from turning on accidentally. When no gate voltage is applied, the power MOSFET is capable of supporting a drain-source blocking voltage through the reverse-biased P-well and N-epi junction. In high-voltage devices, most of the blocking voltage is supported by the lightly doped N-epi layer.

Generally speaking, the power MOSFET can operate in two different quadrants of its *I-V* characteristics:

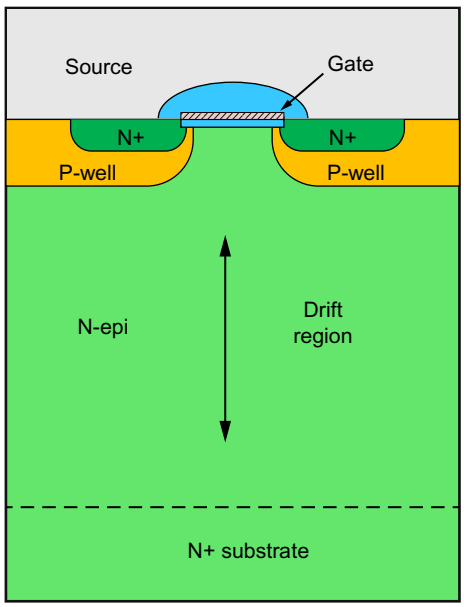


FIG. 6.14 Basic structure of a power MOSFET.

the first quadrant operation and the third quadrant operation. As the gate voltage (V_G) increases above a threshold voltage (V_{th}), the MOSFET starts to conduct current. When the gate voltage V_G is much larger than the threshold voltage V_{th}, the output *I-V* curve appears linear, and the MOSFET channel is fully turned on. Under low gate overdrive, the drain current reaches a saturation value when the MOSFET channel is pinched off.

The MOSFET's switching behavior is highly dependent on the parasitic capacitances gate-to-source C_{gs}, gate-to-drain C_{gd}, and drain-to-source C_{ds}. Gate-to-drain capacitance C_{gd} and drain-to-source C_{ds} are nonlinear and a function of bias voltages.

3. Power IGBT

   The insulated-gate bipolar transistor (IGBT) is a minority carrier device with high input impedance and large current-carrying capability. The IGBT combines the advantages of both power MOSFET and BJT, and it has MOS input characteristics and bipolar output characteristics. The basic structure of a power IGBT is shown in Fig. 6.15.

   The IGBT is widely used in many applications of power electronics, such as motor drives, uninterruptible power supplies (UPS), and power modules, because of the following advantages:
   - A very low on-state voltage drop due to conductivity modulation and very small conduction loss
   - A simple gate driver circuit design due to the MOS gate structure
   - A very large current-carrying capability and smaller chip size for a given conduction current
   - Good forward and reverse voltage blocking capability

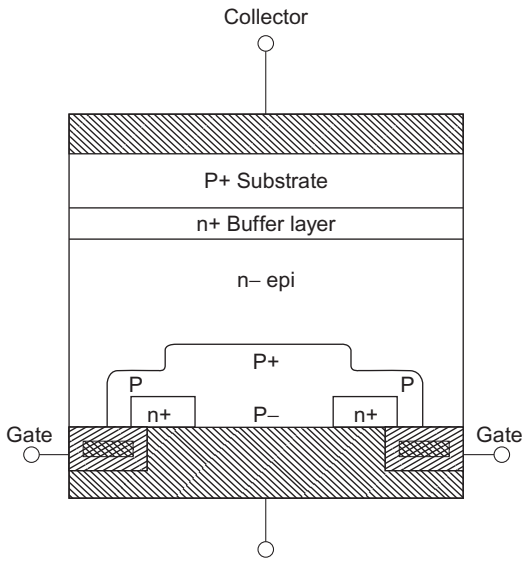


FIG. 6.15 Basic structure of a power IGBT.

   However, the IGBT has some drawbacks, compared with power MOSFET:
   - Slow switching speed, current tailing due to carrier combination
   - Latch-up issue due to the parasitic thyristor structure

   The IGBT is viewed as a serial connection of a MOSFET and a P-i-N diode, and sometimes it is modeled as a wide base PNP transistor driven by a MOSFET in Darlington configuration. In the output I-V characteristics of a power IGBT, the conduction current starts flowing when the gate voltage exceeds the threshold voltage, and collector-source voltage is approximately above 0.7 V.

4. Power Thyristor

   A thyristor is a power device with four alternating layers of p-type and n-type doping and can be turned on by the gate terminal but cannot be turned off by the gate [9]. It has the largest power-handling capability.

5. Power BJT

   The power bipolar transistors (BJT) are conceptually the same as the small-signal BJTs. The main difference is that the active area of power BJT device is much larger resulting in a much higher current handling capability. Power BJTs also have a thick and lightly doped collector region. Such collector regions result in a large blocking voltage.

6.5.3 SiC Power Semiconductor Devices in Power Modules

In recent times, power semiconductor devices using silicon carbide (SiC), a wide bandgap material, rather than silicon have become commercially available. The SiC material has superior material properties for power electronic applications. SiC devices are starting to be used in power modules. In particular, SiC-merged barrier Schottky diodes are used to replace high-voltage P-i-N diodes. The advantage is that, unlike P-i-N diodes, SiC Schottky diodes are majority carrier devices and do not exhibit reverse recovery at turnoff. SiC MOSFETs are also being introduced in modules. Presently, the higher cost of SiC devices limits their adoption.

6.6 Thermal Management of Power Modules

6.6.1 The Purpose of Thermal Management

For a variety of system-level reasons, modern power electronic applications require compact and high-power density power converters. In order to achieve this required miniaturization, higher integration of components and higher switching frequencies, which reduce passive filtering element size, are required. The increase in switching frequency leads to increased power losses and the physical integration makes it harder to remove the loss heat generated. This creates a significant design challenge that requires careful thermal

management. Additionally, in power modules, the power dissipation is concentrated inside the small power semiconductor chips, making heat removal particularly difficult. Power module datasheets specify a maximum allowable junction temperature, that is, temperature at the semiconductor chips inside the module. Exceeding this temperature will lead to module failure. Moreover, lower operating junction temperatures lead to markedly improved module reliability. The maximum junction temperature for current commercially available silicon-based power modules is around 150°C.

Another thermal concern affecting module reliability is thermal cycling, that is, the alternate heating and cooling of the module as a result of varying operating conditions. Excessive thermal cycling leads to aging and early failure of the module. In order to avoid overheating and to improve reliability, a common recommendation is that junction temperature should not exceed 125°C. Therefore, thermal management of power module is necessary to satisfy the thermal requirements described above.

6.6.2 Equivalent Thermal Network of Power Module

Fig. 6.16 shows a cross section of a power electronic module. Power dissipation occurs at the silicon chip due to conduction and switching losses. The heat is conducted through several material layers inside the module until it reaches the baseplate. Fig. 6.16 shows that the heat flows from top to bottom through the top solder layer, the top copper layer, the ceramic substrate, the bottom copper layer, the bottom solder layer, and the baseplate. From the baseplate, the heat exits the module, crosses the thermal grease layer, and reaches the heat sink. In case of air cooling, the heat then transfers by convection to the air surrounding the heat sink. Usually, the heat flow is modeled as being unidimensional with the lateral heat spreading modeled as a spreading angle that increases the heat flow cross section. It should be kept in mind that this approximation introduces a certain error [10]. Each material layer has a certain thermal resistance and thermal capacitance. The temperature gradient across each layer drives the conductive heat transfer. Consequently, the temperature gradually decreases from junction temperature at the silicon chip to ambient temperature T_{AMB}.

The junction temperature in the power module can be estimated by the equivalent Cauer *RC* thermal network shown in Fig. 6.17. In this equivalent model, voltage represents temperature, and current represents heat flow. An *RC* cell represents a specific material layer [11]. The thermal resistance R_i of the *i*th layer is given by

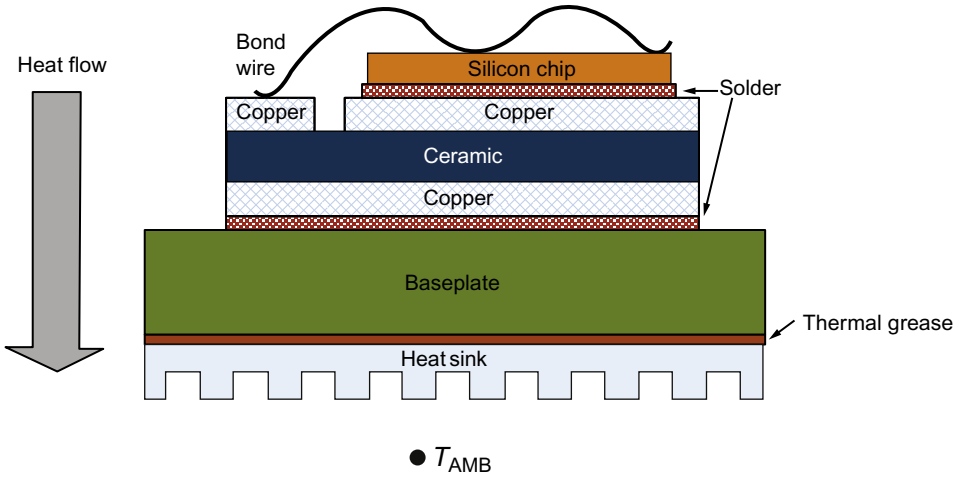


FIG. 6.16 Cross section of power electronic module showing heat flow.

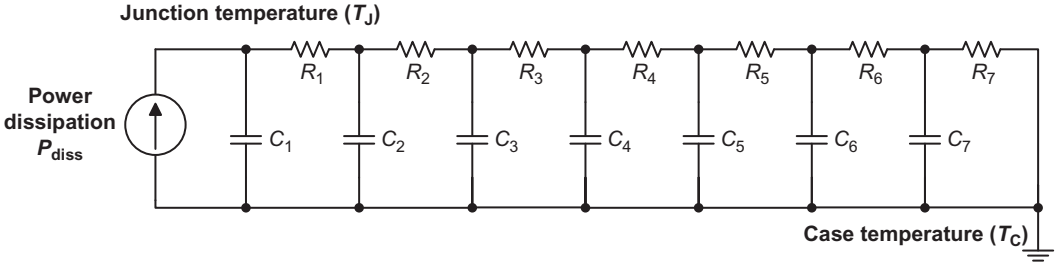


FIG. 6.17 Equivalent Cauer RC thermal network of the power module from junction to case.

$$R_i = \frac{d_i}{k_i A_i} \tag{6.1}$$

where d_i is the ith layer thickness; A_i is the effective cross-sectional area, including a spreading angle for conductors; and k_i is the thermal conductivity of the ith layer.

Thermal capacitance C_i of the ith layer is given by the equation

$$C_i = (c \times \rho \times V)_i \tag{6.2}$$

where c is the constant pressure-specific heat capacity, ρ is the mass density, and V is the effective volume of the ith layer.

According to the equivalent thermal network, the junction temperature T_J is numerically equal to the top left node voltage (the top node of the input current source), while the case temperature T_C represents the reference node voltage of the network. The power module datasheets provide a numerical value for the junction-to-case thermal resistance $R_{th(JC)}$. The term "case" indicates the bottom of the baseplate, where the heat sink is attached. In the equivalent model of Fig. 6.17, $R_{th(JC)}$ is equal to the sum of all thermal resistances R_1 through R_7. The relationship between T_J and T_C is given by the following equation [12]:

$$T_J = T_C + P_{diss} \cdot R_{th(JC)} \tag{6.3}$$

This thermal resistance directly provides the temperature difference between junction and case. To calculate the absolute temperature, it is necessary to calculate the case temperature T_C. This temperature can be calculated based on the selected heat sink, air flow, and ambient temperature T_{AMB}.

As previously mentioned, power modules frequently have a thermal sensor mounted in close proximity of the chips. This gives experimental access to junction temperature in real time [13]. Note that this method can only measure the junction temperature in steady state or for slowly varying thermal transients, because the measured value is accurate only at thermal equilibrium.

According to the thermal network, the junction temperature can be controlled in an acceptable range by applying external cooling to the case of the module.

6.6.3 Cooling Solutions for Power Module

6.6.3.1 Air Cooling

The fin heat sink is a common air cooling solution used in industry, as shown in Fig. 6.18.

For low-power application, a fin heat sink with natural convection is a good choice because no additional device is needed. When the dissipated power is larger, forced convection cooling using an electric fan can be used. However, when the dissipated power density exceeds 100 W/cm^2, the heat sink will not satisfy the cooling requirement, and a more effective cooling method is needed, such as liquid cooling.

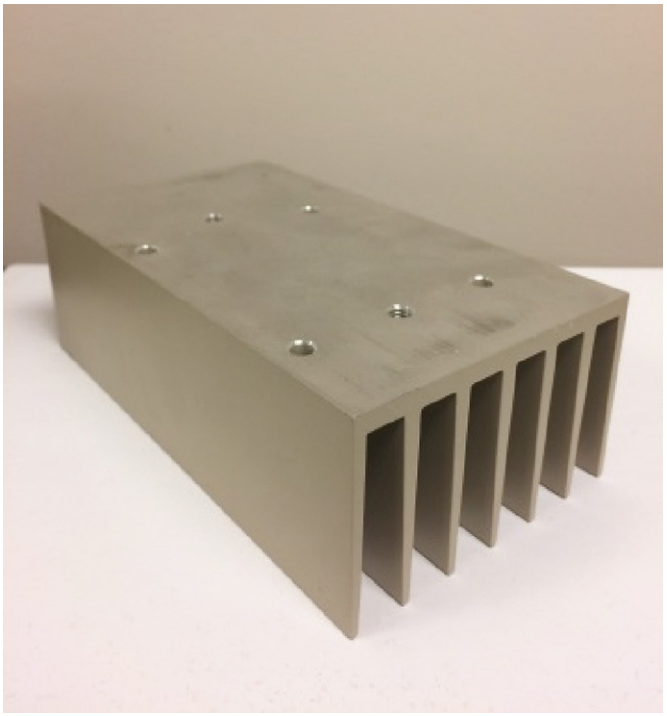


FIG. 6.18 Structure of fin heat sink for power electronics.

6.6.3.2 Liquid Cooling

Liquid cooling has higher thermal transfer efficiency than air cooling and is used in high-power modules. The power module baseplate is thermally connected to a so-called cold plate, which is liquid-cooled. A liquid cooling system is required, as shown in Fig. 6.19. The cooling liquid in the system, such as water, is pumped into the inlet of the cold plate, is heated by the heat flow from the module, flows out from the outlet, and transfers the heat to the cooling radiator. The cold water is gathered in the coolant tank and recirculated. Liquid cooling provides superior thermal performance compared with air cooling, but it incurs additional cost and may affect reliability due to possible coolant leaks.

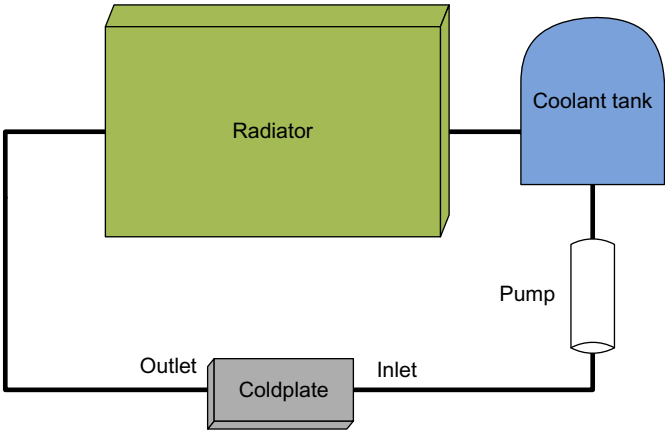


FIG. 6.19 Schematic cold plate and liquid cooling system.

6.6.3.3 Double-Sided Cooling

An approach to increase cooling performance is to remove heat from both sides of the semiconductor dies, instead of removing it from one side only. This approach cannot be used effectively in case of the wire bond package of Fig. 6.16, because the wire bonds prevent heat removal from the top. Consequently, double-sided cooling can be applied only to wire-bond-free power modules. Wire-bond-free packaging techniques include low-temperature attach using double-sided DBC, flip chip solder balls interconnection technology, and press-pack technology. Design complexity, cooling efficiency, electric isolation, and power density must be considered for each case when interfacing the device package with advanced double-sided cooling schemes. The cooling methods are different and depend on the packaging technology used. The double-sided cooling methods are now briefly discussed for the double-sided DBC structure and for the press-pack structure.

6.6.3.4 Double-Sided Cooling Using the DBC Structure

Low-temperature attach techniques have been used to connect IGBT devices to DBC on both sides in order to achieve double-sided liquid cooling. This technique increases cooling performance, but electric isolation via DBC adds thermal resistance. Fig. 6.20 shows a cross section of the double-sided cooling structure with power semiconductors. This package design gave a thermal resistance of 0.087°C/W for a flow rate of 1.6 gal/min [14].

Flip chip solder ball interconnection technology can be used to eliminate cooling interface issues related to wire bonds, but electric isolation requirements limit the efficiency of the cooling system also in this case. Microchannels are integrated directly in the package to provide double-sided cooling. The interface between the device and DBC via solder balls as well as the use of DBC as isolation between the device and heat sinks somewhat reduces the heat transfer from the chip. This cooling and package configuration provides a thermal resistance of 0.09–0.12°C/W for a flow rate range of 0.2–2 gal/min [14]. Fig. 6.21 shows a cross section of the structure.

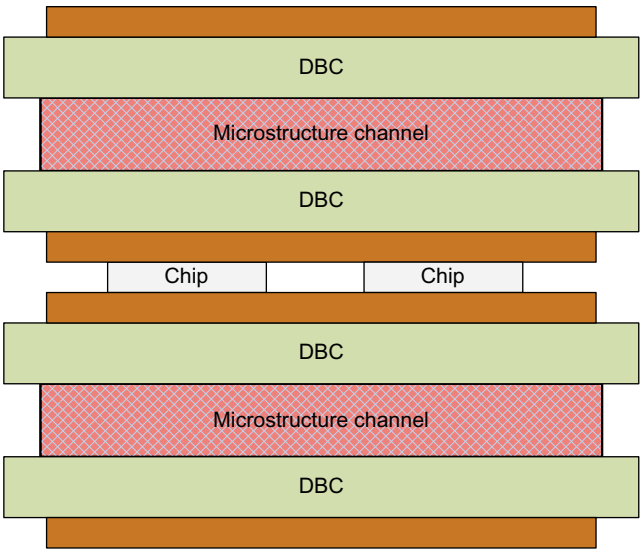


FIG. 6.20 Cross section of the double-sided cooling structure with low temperature joining techniques.

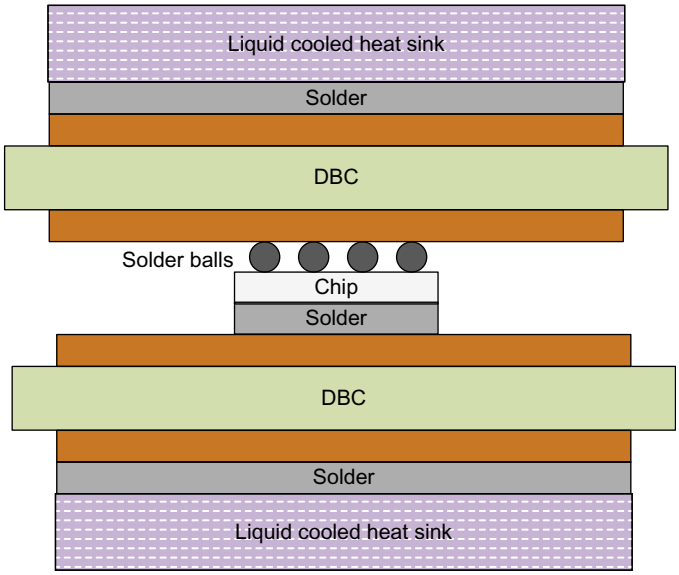


FIG. 6.21 Cross section of the double-sided cooling structure with flip chip solder.

6.6.3.5 Double-Sided Cooling Using the Press-Pack Structure

Press-pack semiconductor packaging technology can also allow advanced double-side cooling schemes. This example uses evaporators on both sides of the semiconductors. This method is promising for applications that use press-pack technology. Fig. 6.22 shows the cross section of the press-pack and double-sided multiphase cooling structure.

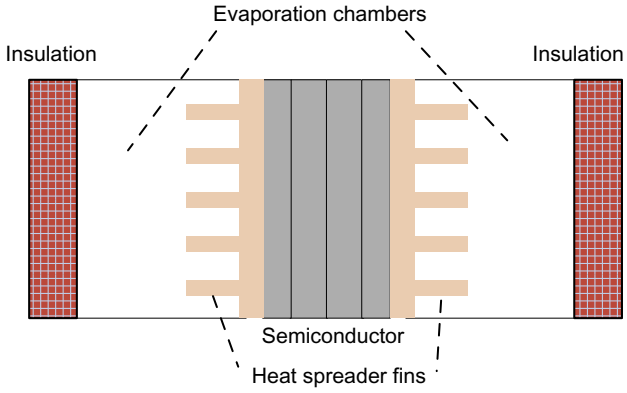


FIG. 6.22 Cross section of the double-sided cooling structure for press pack.

6.7 Reliability of Power Modules

For power electronic applications, reliability of power modules is an important issue. The reliability of power electronics has been improving over the years. As an example, power module failure rate in traction has decreased from 1000 FITs in 1995 to 20 FITs in 2000 (1 FIT = one failure per 10^9 device hours). In recent years, many failure-detecting tests have been proposed or improved, such as solder cracking and bond wire lift-off tests [15].

Thermomechanical stress on power module packaging materials is the most common reason for module failure due to mismatch in the coefficients of thermal expansion (CTE) between different adjacent materials inside the power module package. The structure of a power module, shown in Fig. 6.5, has been described earlier. The most common module failures are due to wire bond lifting, that is, the wire bond detaching from the surface it was bonded to, and solder cracking.

Bond wire lifting is one of the main reasons for power electronic module failures: a crack is formed and grows at the junction between the chip and the bond wire due to mismatch between the CTEs as a result of temperature variations. The difference in the CTEs causes strain at the interface. The strain initiates the crack that grows as a result of successive stress cycles during operation. This is shown in Fig. 6.23. The bond wire lifting failures can be examined by microstructural testing. A discussion of reliability in power modules can be found in [16].

Cracks usually grow from the two end sides during thermal cycles, and the bond wire lifts up when the crack reaches the center. A contributing factor to bond wire failures is magnetic forces induced on the wire bonds by inductive coupling among bond wires.

The second most common failure is related to solder fatigue at a solder joint inside the power module. For example, a failure may occur in the solder joint between a silicon die and the copper substrate, as shown in Fig. 6.24. The failure occurs because of CTE mismatch between the die chip and the substrate, which results in mechanical stress that shifts the solder layers laterally in relation to each other and eventually creates voids.

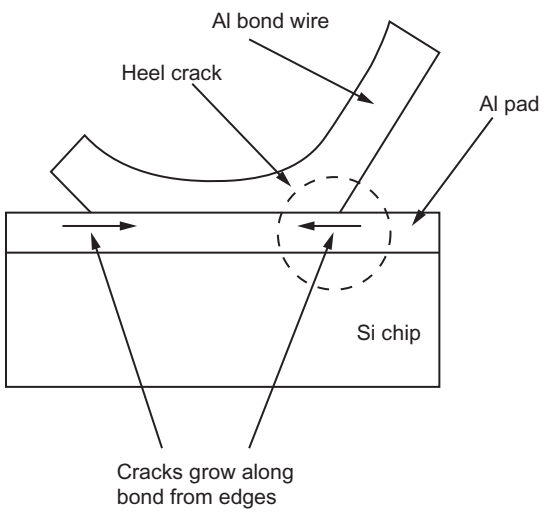


FIG. 6.23 Bond wire lifting resulting from crack propagation.

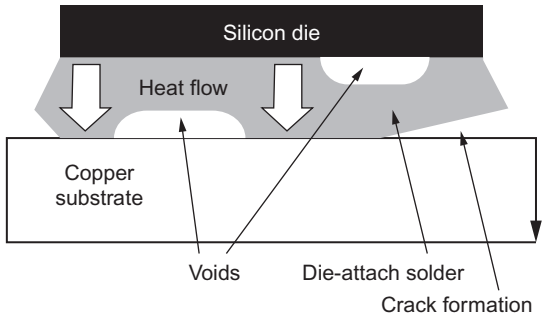


FIG. 6.24 Void and crack formation between die and substrate.

As shown in Fig. 6.24, the voids are a barrier to heat conduction from die to substrate and cause a nonuniform heat distribution. This in turn increases the thermal resistance between die and substrate and damages the die. The stress on the interfaces depends on temperature and increases as temperature increases.

Two different types of thermal stress can be identified, power cycling and thermal cycling. Power cycling refers to temperature variations caused by varying power loss in the devices due to a variation of operating conditions. Thermal cycling is the effect of temperature variations in the environment around the power module.

Power converters usually undergo both types of temperature cycling but with different levels of temperature variation and frequency [16].

6.7.1 Reliability Tests [17]

A power module is exposed to active temperature cycles due to its operation and to passive temperature cycles due to variation of the surrounding environment. Thermal cycling and power cycling tests can be performed to represent these conditions and evaluate reliability:

6.7.1.1 Thermal Cycling Test

In this test, the temperature of the power module is changed as a result of a change in case temperature or of variation of ambient temperature (TST, thermal shock test). No electric stress is applied. This test evaluates lifetime of the solder joints and ability of the device to survive sudden temperature variation.

6.7.1.2 Power Cycling Test

In this test, the ruggedness of semiconductor devices such as IGBTs and MOSFETs is evaluated under thermomechanical stress due to power loss cycling in the internal semiconductor

dies. The variation of temperature is due to periodic variations of load current. This test evaluates reliability under high-temperature operation.

The equivalent test cycles can be evaluated by converting the thermal stress on solder and bond joints due to active and passive thermal stress into reliability test data.

6.8 Design Guidelines and Considerations

In order to utilize a commercially available power module to realize a switching converter for a specific application, the following steps should be followed:

1. *Power module selection based on switching converter specifications*. A power module of the desired topology with the appropriate voltage and current rating should be selected. The type (IGBT, MOSFET, and so on) and characteristics of the power semiconductor devices in the module determine achievable switching frequency. From the manufacturer's datasheets, conduction and switching losses can be estimated.
2. *Electric design*. Referring to Fig. 6.4, the external components required to realize the converter need to be designed. These include bypass capacitor C_{BYPASS}, gate drivers (unless they are already integrated inside the module), power inductor L, and converter control. Some special considerations regarding the first two items, which are specific to power modules, will be discussed below.
3. *Thermal design*. Based on the estimated losses, the thermal design must be completed. The cooling method—natural convection, forced convection, or liquid cooling—is selected and the thermal circuit designed to achieve a desired maximum junction temperature under worst-case conditions.

For a successful design, it is critical to follow the specifications and recommendations in the manufacturer's datasheets. Manufacturers also provide additional design support, such as application notes, technical papers, and online loss calculation software tools for their products.

6.8.1 Bypass Capacitor Considerations

Besides component selection, as is frequently the case in power electronics, proper physical layout is critical. As shown in Fig. 6.25, for the case of a half-bridge converter, the switching loop should be minimized in physical size in order to reduce overshoot and ringing during switching. The objective is to reduce the distributed parasitic inductance of the switching loop, shown as lumped inductance L_{SWITCH} in the figure.

As shown in Fig. 6.4, the switching loop is partially inside the power module, but it is completed by the external capacitor

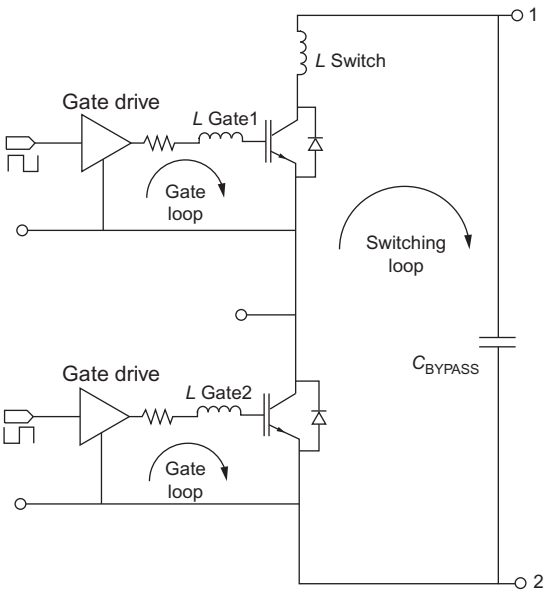


FIG. 6.25 Half-bridge module schematic showing the switching loop and the gate loops that should be minimized for proper converter operation.

C_{BYPASS}. This capacitor should absorb the square-wave current at the switching frequency resulting from switching converter operation. It is critical to use a high-frequency high-current-ripple capacitor. Ceramic or metal film capacitors are appropriate. Polypropylene capacitors are a popular choice. It is critical to mount the bypass capacitor physically close to the module. A laminated bus bar is recommended to reduce parasitic inductance by having closely spaced flat conductors conducting opposite polarity currents.

6.8.2 Gate Driver Design Considerations

The gate driver design is similar to what is commonly done for discrete power semiconductor devices. Based on the total gate charge Q_G from the datasheets and on the desired gate voltage rise and fall time, a gate driver with adequate current capability is selected. The choice of gate resistor is a trade-off: a smaller gate resistor gives faster switching speed with lower switching losses and with increased gate noise immunity, whereas a larger gate resistor gives slower switching speed with reduced switching noise and reduced diode reverse recovery. It should be kept in mind that power modules frequently have internal gate resistances in case of multiple paralleled dies as shown in Fig. 6.26. Resistances R_g are internal to the module and are needed to ensure dynamic current balance. If a single gate resistor was used, there could be an LC oscillation caused by the input capacitances of the two IGBTs resonating with the parasitic inductance of the gate connection. In the case of Fig. 6.26, this resonant path has a $2R_g$ series damping resistance. The module

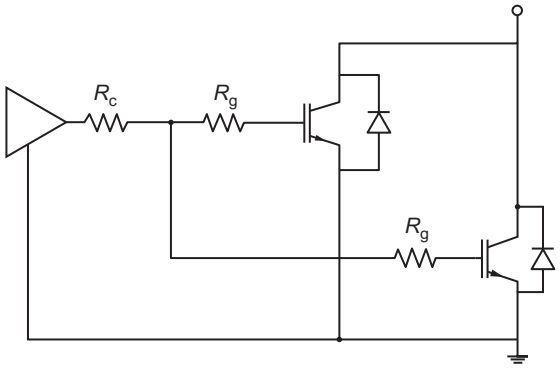


FIG. 6.26 Schematic of bottom switch of power module consisting of two paralleled IGBTs with internal resistances R_g.

datasheets usually provide a recommended external gate resistor range of values.

Regarding layout, it is important to minimize the gate loops shown in Fig. 6.25. A large gate loop causes a large parasitic inductance L_{GATE} that resonates with the IGBT input capacitance causing gate voltage ringing, which may cause spurious IGBT switching. The power module gate contacts should be directly connected to the gate driver printed circuit board if possible.

6.8.3 Gate Kelvin Contacts

Power modules typically have gate Kelvin contacts. It is essential that they be used for the gate drive as shown in Fig. 6.4 in order to have an effective dynamic gate voltage control. Fig. 6.27 shows the case of no emitter Kelvin contact. As a result, there is a parasitic emitter inductance L_E that is part of both the switching

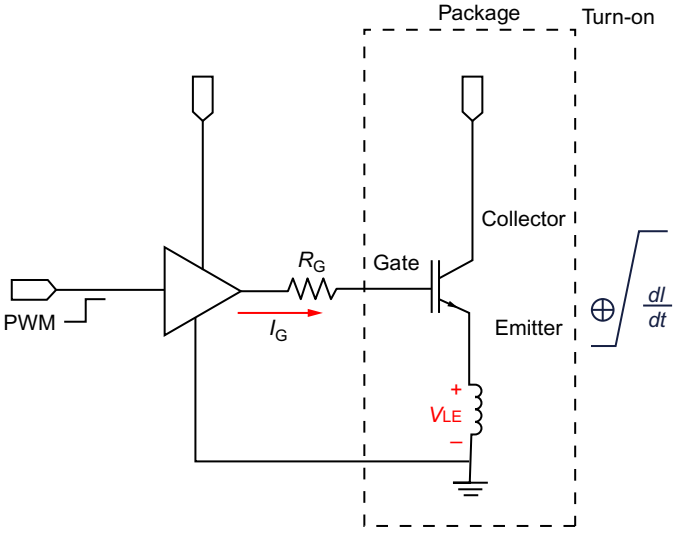


FIG. 6.27 Packaged IGBT without emitter Kelvin contact.

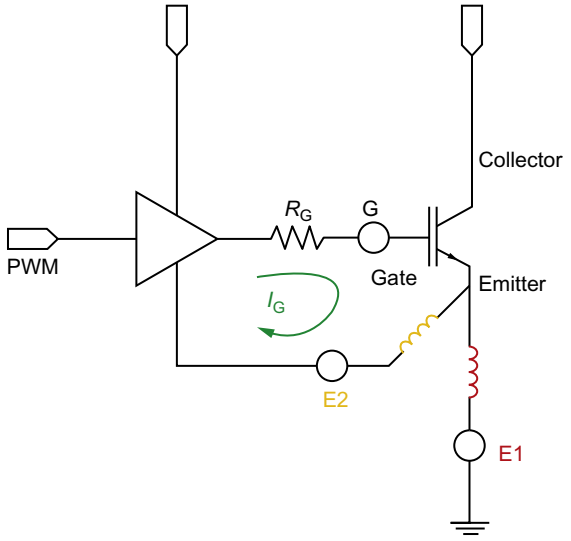


FIG. 6.28 Emitter Kelvin contact E2 is separate from emitter power contact E1.

loop and the gate loop (refer to Fig. 6.25). This inductance conducts the full collector current. During turn-on, the gate drive voltage increases, and the IGBT gradually turns on. The increasing collector current induces a positive voltage v_{LE} on the parasitic emitter inductance that subtracts from the gate driver voltage and slows down the gate-emitter voltage rise. This negative feedback effect is undesirable because it slows down the switching transition and causes the gate driver to have less dynamic control of the actual gate-emitter voltage. A similar negative feedback effect occurs at turnoff, slowing down this transition as well. This problem can be solved by providing a separate emitter Kelvin contact as shown in Fig. 6.28. The power contact emitter inductance (in red) is not part of the gate loop, and the negative feedback effect is eliminated.

Fig. 6.29 shows the inside of a six-pack IGBT power module. On the bottom left side, one can see the power emitter pin and the Kelvin emitter pin. Notice that dedicated wire bonds go from the IGBT chip to the Kelvin emitter pin. These wire bonds conduct only the gate driver current and not the collector current and represent the E2 connection of Fig. 6.28. The figure also shows the IGBT and diode dies, the IGBT gate and emitter pads, the wire bonds, the top copper layer, the ceramic substrate, and the thermistor.

6.8.4 Other Design Considerations

In order to realize a switching converter, other design aspects must be considered, such as protection, sensing, and control implementation. The gate driver may include protections, such as short circuit protection. Current sensing may be implemented for protection and for current mode programming control.

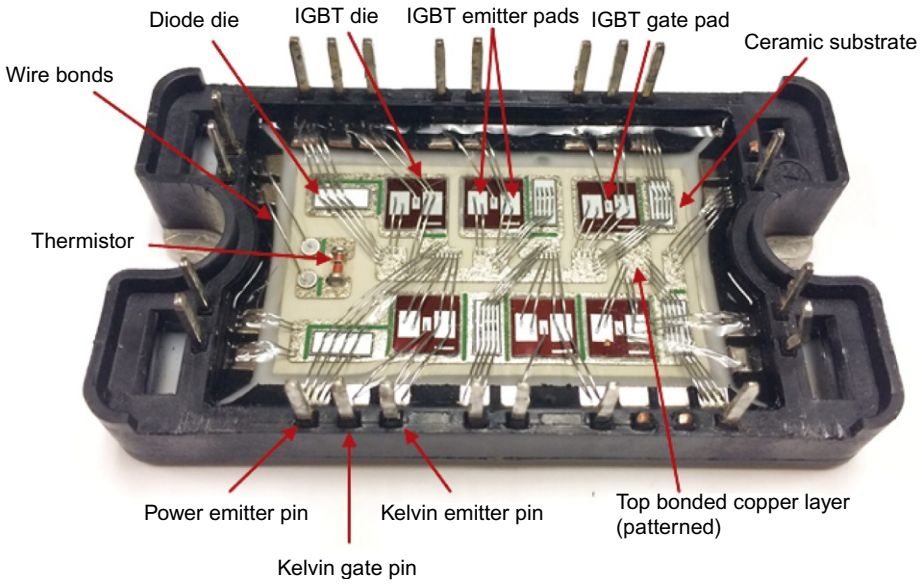


FIG. 6.29 Photo of opened Microsemi APTGF50X60T3G six-pack IGBT power module (from 600 V to 50 A) with several internal features labeled.

Voltage sensing is typically required for control. Either an analog or a digital controller can be used. Snubbers and clamps may be required to reduce switching waveform overshoot and ringing. EMI filters may be required.

References

[1] Online resource, www.HYBOND.com (Accessed 23 February 2017).
[2] Online resource, www.hesse-mechatronics.com (Accessed 23 February 2017).
[3] I. Wei Qin, P. Reid, R.E. Werner, D. Doerr, Automatic wedge bonding with ribbon wire for high frequency applications, in: IEMT, 2002, pp. 97–101.
[4] W.W. Sheng, R.P. Colino, Power Electronic Modules Design and Manufacture, CRC Press, Boca Raton, Florida, 2005.
[5] L. Xingsheng, Processing and Reliability Assessment of Solder Joint Interconnection for Power Chips, (Virginia Tech Dissertation) (2001).
[6] Powerex three-phase diode bridge module RM75TPM-2H, http://www.pwrx.com/pwrx/docs/rm75tpm-2 h.pdf (Accessed 23 February 2017).
[7] Infineon power IGBT module FS100R07PE4, http://www.infineon.com/dgdl/Infineon-FS100R07PE4-DS-v02_00-en_de.pdf?fileId=db3a304333227b5e013359531e9908c6 (Accessed 23 February 2017).
[8] Allen Bradley, What is regeneration? http://www.ab.com/support/abdrives/documentation/techpapers/RegenOverview01.pdf (Accessed 23 February 2017).
[9] B. Jayant Baliga, Fundamentals of Power Semiconductor Devices, Springer, New York, 2008.
[10] C. Van Godbold, V.A. Sankaran, J.L. Hudgins, Thermal analysis of high-power modules, IEEE Trans. Power Electron. 12 (1) (1997) 3–11.
[11] T.K. Gachovska, B. Tian, J. Hudgins, W. Qiao, A real-time thermal model for monitoring of power semiconductor devices, IEEE Trans. Ind. Appl. 51 (4) (2015) 3361–3367.
[12] B. Tian, W. Qiao, Z. Wang, T.K. Gachovska, J. Hudgins, Monitoring IGBT's health condition via junction temperature variations, in: APEC, 2014, , pp. 2550–2555.
[13] Infineon application note, http://www.infineon.com/dgdl/Infineon-AN2009_10_Using_the_NTC-AN-v1.0-en.pdf (Accessed 23 February 2017).
[14] B.C. Charboneau, Double-sided liquid cooling for power semiconductor devices using embedded power technology, Virginia Polytechnic Institute, Blacksburg, VA, 2005.
[15] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, P. Tavner, An industry-based survey of reliability in power electronic converters, IEEE Trans. Ind. Appl. 47 (3) (2011) 1441–1451.
[16] S. Yang, D. Xiang, A. Bryant, P. Mawby, L. Ran, P. Tavner, Condition monitoring for device reliability in power electronic converters: A review, IEEE Trans. Power Electron. 25 (11) (2010) 2734–2752.
[17] A. Christmann, M. Thoben, K. Mainka, Reliability of power modules in hybrid vehicles, in: PCIM Europe International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management Proceedings, 2009, pp. 1–7.

Further Reading

[18] Y.S. Sun, J.C. Driscoll, A new hybrid power technique utilizing a direct copper to ceramic bond, IEEE Trans. Electron Devices 23 (8) (1976) 961–967.

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Section II

Power Conversion

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7

Diode Rectifiers

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7.1 Introduction

This chapter describes the application and design of diode rectifier circuits. It covers single-phase rectifier circuits, three-phase rectifier circuits, polyphase rectifier circuits, and high-frequency rectifier circuits. The objectives of this chapter are the following:

- To enable the readers to understand the operation of typical rectifier circuits
- To enable the readers to appreciate the different qualities of rectifiers required for different applications
- To enable the reader to design practical rectifier circuits

The high-frequency rectifier waveforms given are obtained from PSpice simulations, which take into account the secondary effects of stray and parasitic components. In this way, the waveforms can closely resemble the real ones. These waveforms are particularly useful to help designers determine the practical voltage, current, and other ratings of high-frequency rectifiers.

7.2 Single-Phase Diode Rectifiers

There are two types of single-phase diode rectifier that convert a single-phase ac supply into a dc voltage, namely, single-phase half-wave rectifiers and single-phase full-wave rectifiers. In the following subsections, the operations of these rectifier circuits are examined, and their performances are analyzed and compared in a tabulated form. For the sake of simplicity, the diodes are considered to be ideal, that is, they have zero forward voltage drop and reverse recovery time. This assumption is generally valid for the case of diode rectifiers that use the mains, a low-frequency source, as the input and when the forward voltage drop is small compared with the peak voltage of the mains. Furthermore, it is assumed that the load is purely resistive such that the load voltage and the load current have similar waveforms. In Section 7.5, Filtering Systems in Rectifiers Circuits, the effects of inductive load and capacitive load on a diode rectifier are considered in detail.

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7.2.1 Single-Phase Half-Wave Rectifiers

The simplest single-phase diode rectifier is the single-phase half-wave rectifier. A single-phase half-wave rectifier with resistive load is shown in Fig. 7.1. The circuit consists of only one diode that is usually fed with a secondary transformer as shown. During the positive half cycle of the transformer secondary voltage, diode D conducts. During the negative half cycle, diode D stops conducting. Assuming that the transformer has zero internal impedance and provides perfect sinusoidal voltage on its secondary winding, the voltage and current waveforms of resistive load R and the voltage waveform of diode D are shown in Fig. 7.2.

By observing the voltage waveform of diode D in Fig. 7.2, it is clear that the peak inverse voltage (PIV) of diode D is equal to V_m during the negative half cycle of the transformer secondary voltage. Hence, the peak repetitive reverse voltage (V_{RRM}) rating of diode D must be chosen to be higher than V_m to avoid reverse breakdown. In the positive half cycle of the transformer secondary voltage, diode D has a forward current that is equal to the load current; therefore, the peak repetitive forward current (I_{FRM}) rating of diode D must be chosen to be higher than the peak load current, V_m/R, in practice. In addition, the transformer has to carry a dc current that may result in a dc saturation problem of the transformer core.

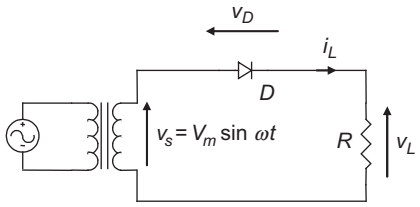


FIG. 7.1 A single-phase half-wave rectifier with resistive load.

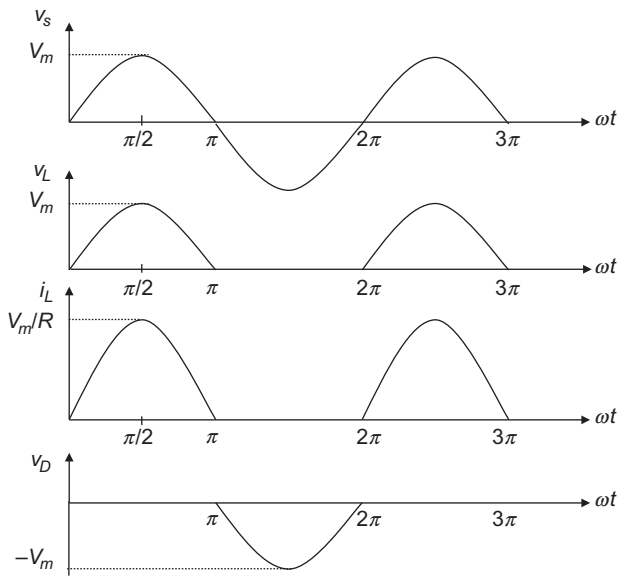


FIG. 7.2 Voltage and current waveforms of the half-wave rectifier with resistive load.

7.2.2 Single-Phase Full-Wave Rectifiers

There are two types of single-phase full-wave rectifier, namely, full-wave rectifiers with center-tapped transformer and bridge rectifiers. A full-wave rectifier with a center-tapped transformer is shown in Fig. 7.3. It is clear that each diode, together with the associated half of the transformer, acts as a half-wave rectifier. The outputs of the two half-wave rectifiers are combined to produce full-wave rectification in the load. As far as the transformer is concerned, the dc currents of the two half-wave rectifiers are equal and opposite, such that there is no dc current for creating a transformer core saturation problem. The voltage and current waveforms of the full-wave rectifier are shown in Fig. 7.4. By observing diode voltage waveforms v_{D_1} and v_{D_2} in Fig. 7.4, it is clear that the PIV of the diodes is equal to $2V_m$ during their blocking state. Hence, the V_{RRM} rating of the diodes must be chosen to be higher than $2V_m$ to avoid reverse breakdown. (Note that, compared with the half-wave rectifier shown in Fig. 7.1, the full-wave rectifier has twice the dc output voltage, as shown in Section 7.2.4.) During its conducting state, each diode has a forward current which is equal to the load current; therefore, the I_{FRM} rating of these diodes must be chosen to be higher than the peak load current, V_m/R, in practice.

Employing four diodes instead of two, a bridge rectifier as shown in Fig. 7.5 can provide full-wave rectification without using a center-tapped transformer. During the positive half cycle of the transformer secondary voltage, the current flows to the load through diodes D_1 and D_2. During the negative half cycle, D_3 and D_4 conduct. The voltage and current waveforms of the bridge rectifier are shown in Fig. 7.6. As with the full-wave rectifier with center-tapped transformer, the I_{FRM} rating of the employed diodes must be chosen to be higher than the peak load current, V_m/R. However, the PIV of the diodes is reduced from $2V_m$ to V_m during their blocking state.

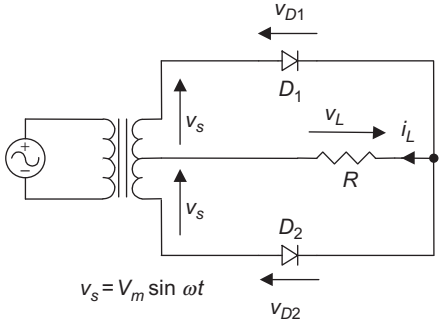


FIG. 7.3 Full-wave rectifier with center-tapped transformer.

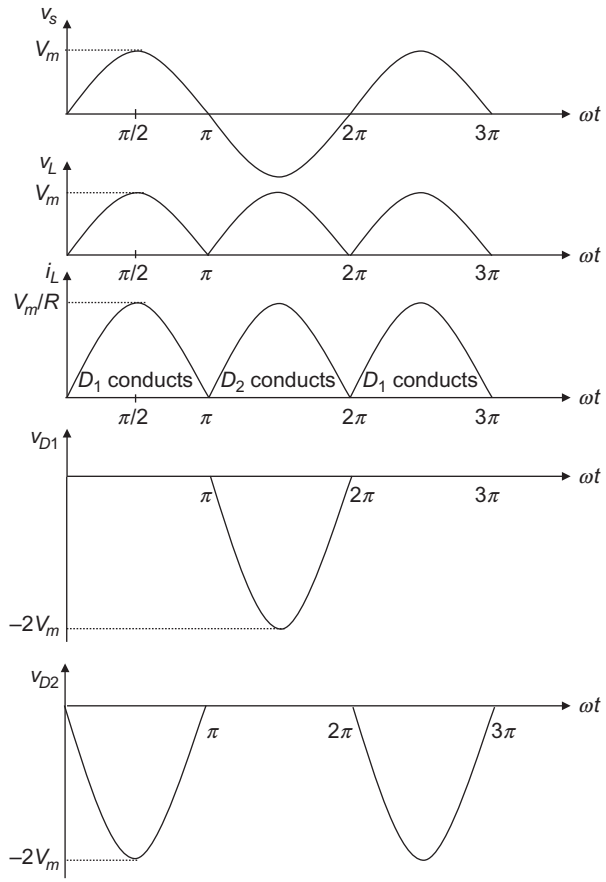


FIG. 7.4 Voltage and current waveforms of the full-wave rectifier with center-tapped transformer.

7.2.3 Performance Parameters

In this subsection, the performance of the rectifiers mentioned above will be evaluated in terms of the following parameters.

7.2.3.1 Voltage Relationships

The average value of the load voltage v_L is V_{dc} and it is defined as

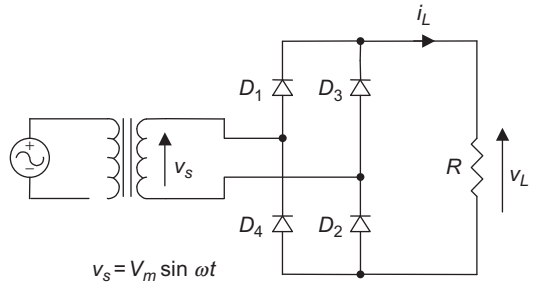


FIG. 7.5 Bridge rectifier.

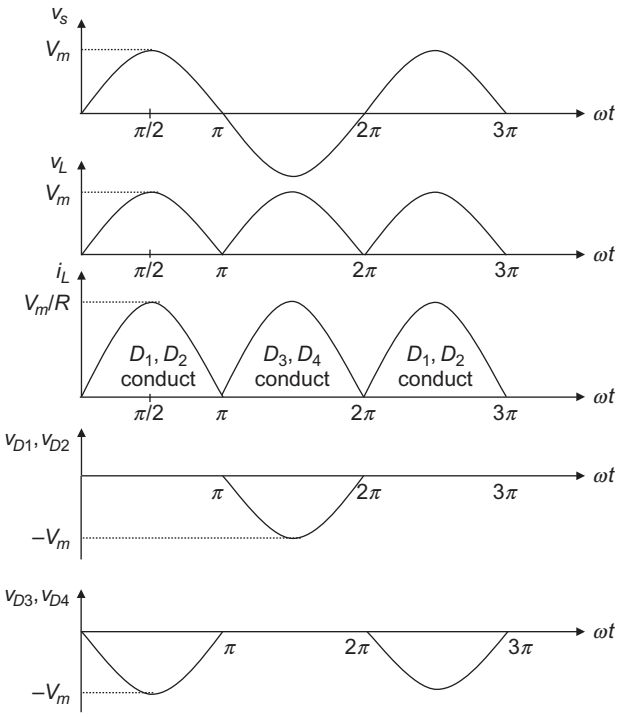


FIG. 7.6 Voltage and current waveforms of the bridge rectifier.

$$V_{dc} = \frac{1}{T}\int_0^T v_L(t)\,dt \tag{7.1}$$

In the case of a half-wave rectifier, Fig. 7.2 indicates that load voltage $v_L(t) = 0$ for the negative half cycle. Note that the angular frequency of the source $\omega = 2\pi/T$, and Eq. (7.1) can be rewritten as

$$V_{dc} = \frac{1}{2\pi}\int_0^{\pi} V_m \sin\omega t\, d(\omega t) \tag{7.2}$$

Therefore,

$$\text{Half-wave} \quad V_{dc} = \frac{V_m}{\pi} = 0.318\ V_m \tag{7.3}$$

In the case of a full-wave rectifier, Figs. 7.4 and 7.6 indicate that $v_L(t) = V_m|\sin\omega t|$ for both the positive and negative half cycles. Hence, Eq. (7.1) can be rewritten as

$$V_{dc} = \frac{1}{\pi}\int_0^{\pi} V_m \sin\omega t\, d(\omega t) \tag{7.4}$$

Therefore,

$$\text{Full-wave} \quad V_{dc} = \frac{2V_m}{\pi} = 0.636\ V_m \tag{7.5}$$

The root-mean-square (rms) value of load voltage v_L is V_L, which is defined as

$$V_L = \left[\frac{1}{T}\int_0^T v_L^2(t)dt\right]^{1/2} \tag{7.6}$$

In the case of a half-wave rectifier, $v_L(t) = 0$ for the negative half cycle; therefore, Eq. (7.6) can be rewritten as

$$V_L = \sqrt{\frac{1}{2\pi}\int_0^{\pi}(V_m \sin\omega t)^2 d(\omega t)} \tag{7.7}$$

or

$$\text{Half-wave} \quad V_L = \frac{V_m}{2} = 0.5V_m \tag{7.8}$$

In the case of a full-wave rectifier, $v_L(t) = V_m|\sin\omega t|$ for both the positive and negative half cycles. Hence, Eq. (7.6) can be rewritten as

$$V_L = \sqrt{\frac{1}{\pi}\int_0^{\pi}(V_m \sin\omega t)^2 d(\omega t)} \tag{7.9}$$

or

$$\text{Full-wave} \quad V_L = \frac{V_m}{\sqrt{2}} = 0.707V_m \tag{7.10}$$

The result of Eq. (7.10) is as expected because the rms value of a full-wave rectified voltage should be equal to that of the original ac voltage.

7.2.3.2 Current Relationships

The average value of load current i_L is I_{dc}, and because load R is purely resistive, it can be found as

$$I_{dc} = \frac{V_{dc}}{R} \tag{7.11}$$

The rms value of load current i_L is I_L, and it can be found as

$$I_L = \frac{V_L}{R} \tag{7.12}$$

In the case of a half-wave rectifier, from Eq. (7.3),

$$\text{Half-wave} \quad I_{dc} = \frac{0.318V_m}{R} \tag{7.13}$$

and from Eq. (7.8),

$$\text{Half-wave} \quad I_L = \frac{0.5V_m}{R} \tag{7.14}$$

In the case of a full-wave rectifier, from Eq. (7.5),

$$\text{Full-wave} \quad I_{dc} = \frac{0.636V_m}{R} \tag{7.15}$$

and from Eq. (7.10),

$$\text{Full-wave} \quad I_L = \frac{0.707V_m}{R} \tag{7.16}$$

7.2.3.3 Rectification Ratio

The rectification ratio, which is a figure of merit for comparing the effectiveness of rectification, is defined as

$$\sigma = \frac{P_{dc}}{P_L} = \frac{V_{dc}T_{dc}}{V_L I_L} \tag{7.17}$$

In the case of a half-wave diode rectifier, the rectification ratio can be determined by substituting Eqs. (7.3), (7.13), (7.8), and (7.14) into Eq. (7.17):

$$\text{Half-wave} \quad \sigma = \frac{(0.318V_m)^2}{(0.5V_m)^2} = 40.5\% \tag{7.18}$$

In the case of a full-wave rectifier, the rectification ratio is obtained by substituting Eqs. (7.5), (7.15), (7.10), and (7.16) into Eq. (7.17):

$$\text{Full-wave} \quad \sigma = \frac{(0.636V_m)^2}{(0.707V_m)^2} = 81\% \tag{7.19}$$

7.2.3.4 Form Factor

The form factor (FF) is defined as the ratio of the root-mean-square value (heating component) of a voltage or current to its average value:

$$\text{FF} = \frac{V_L}{V_{dc}} \quad \text{or} \quad \frac{I_L}{I_{dc}} \tag{7.20}$$

$$\text{Half-wave} \quad \text{FF} = \frac{0.5V_m}{0.318V_m} = 1.57 \tag{7.21}$$

In the case of a full-wave rectifier, the FF can be found by substituting Eqs. (7.16) and (7.15) into Eq. (7.20):

$$\text{Full-wave} \quad \text{FF} = \frac{0.707V_m}{0.636V_m} = 1.11 \tag{7.22}$$

7.2.3.5 Ripple Factor

The ripple factor (RF), which is a measure of the ripple content, is defined as

$$\text{RF} = \frac{V_{ac}}{V_{dc}} \tag{7.23}$$

where V_{ac} is the effective (rms) value of the ac component of load voltage v_L:

$$V_{ac} = \sqrt{V_L^2 - V_{dc}^2} \tag{7.24}$$

Substituting Eq. (7.24) into Eq. (7.23), the RF can be expressed as

$$\text{RF} = \sqrt{\left(\frac{V_L}{V_{dc}}\right)^2 - 1} = \sqrt{\text{FF}^2 - 1} \tag{7.25}$$

In the case of a half-wave rectifier,

$$\text{Half-wave} \quad \text{RF} = \sqrt{1.57^2 - 1} = 1.21 \tag{7.26}$$

In the case of a full-wave rectifier,

$$\text{Full-wave} \quad \text{RF} = \sqrt{1.11^2 - 1} = 0.482 \tag{7.27}$$

7.2.3.6 Transformer Utilization Factor

The transformer utilization factor (TUF), which is a measure of the merit of a rectifier circuit, is defined as the ratio of the dc output power to the transformer volt-ampere (VA) rating required by the secondary winding:

$$\text{TUF} = \frac{P_{dc}}{V_s I_s} = \frac{V_{dc} I_{dc}}{V_s I_s} \tag{7.28}$$

where V_s and I_s are the rms voltage and rms current ratings of the secondary transformer:

$$V_s = \frac{V_m}{\sqrt{2}} = 0.707 V_m \tag{7.29}$$

The rms value of the transformer secondary current I_s is the same as that of the load current I_L. For a half-wave rectifier, I_s can be found from Eq. (7.14):

$$\text{Half-wave} \quad I_s = \frac{0.5 V_m}{R} \tag{7.30}$$

For a full-wave rectifier, I_s is found from Eq. (7.16):

$$\text{Full-wave} \quad I_s = \frac{0.707 V_m}{R} \tag{7.31}$$

Therefore, the TUF of a half-wave rectifier can be obtained by substituting Eqs. (7.3), (7.13), (7.29), and (7.30) into Eq. (7.28):

$$\text{Half-wave} \quad \text{TUF} = \frac{0.318^2}{0.707 \times 0.5} = 0.286 \tag{7.32}$$

The poor TUF of a half-wave rectifier signifies that the transformer employed must have a 3.496 (1/0.286) VA rating in order to deliver 1 W dc output power to the load. In addition, the transformer secondary winding has to carry a dc current that may cause magnetic core saturation. As a result, half-wave rectifiers are used only when the current requirement is small.

In the case of a full-wave rectifier with center-tapped transformer, the circuit can be treated as two half-wave rectifiers operating together. Therefore, the transformer secondary VA rating, $V_s I_s$, is double that of a half-wave rectifier, but the output dc power is increased by a factor of four due to higher rectification ratio as indicated by Eqs. (7.5) and (7.15). Therefore, the TUF of a full-wave rectifier with center-tapped transformer can be found from Eq. (7.32):

$$\text{Full-wave} \quad \text{TUF} = \frac{4 \times 0.318^2}{2 \times 0.707 \times 0.5} = 0.572 \tag{7.33}$$

In the case of a bridge rectifier, it has the highest TUF in single-phase rectifier circuits because the currents flowing in both the primary and secondary windings are continuous sinewaves. By substituting Eqs. (7.5), (7.15), (7.29), and (7.31) into Eq. (7.28), the TUF of a bridge rectifier can be found:

$$\text{Bridge} \quad \text{TUF} = \frac{0.636^2}{(0.707)^2} = 0.81 \tag{7.34}$$

The transformer primary VA rating of a full-wave rectifier is equal to that of a bridge rectifier since the current flowing in the primary winding is also a continuous sinewave.

7.2.3.7 Harmonics

Full-wave rectifier circuits with resistive load do not produce harmonic currents in their transformers. In half-wave rectifiers, harmonic currents are generated. The amplitudes of the harmonic currents of a half-wave rectifier with resistive load, relative to the fundamental, are given in Table 7.1. The extra loss caused by the harmonics in the resistive loaded rectifier circuits is often neglected because it is not high compared with other losses. However, with nonlinear loads, harmonics can cause appreciable loss and other problems such as poor power factor and interference.

7.2.4 Design Considerations

In a practical design, the goal is to achieve a given dc output voltage. Therefore, it is more convenient to put all the design parameters in terms of V_{dc}. For example, the rating and turn ratio of the transformer in a rectifier circuit can be easily determined if the rms input voltage to the rectifier is in terms of the required output voltage V_{dc}.

Denote the rms value of the input voltage to the rectifier as V_s, which is equal to $0.707 V_m$. Based on this relation and Eq. (7.3), the rms input voltage to a half-wave rectifier is found as

$$\text{Half-wave} \quad V_s = 2.22 V_{dc} \tag{7.35}$$

TABLE 7.1 Harmonic percentages of a half-wave rectifier with resistive load

Harmonic	Second	Third	Fourth	Fifth	Sixth	Seventh	Eighth
%	21.2	0	4.2	0	1.8	0	1.01

Similarly, from Eqs. (7.5) and (7.29), the rms input voltage per secondary winding of a full-wave rectifier is found as

$$\text{Full-wave} \quad V_s = 1.11 V_{dc} \tag{7.36}$$

Another important design parameter is the V_{RRM} rating of the diodes employed.

In the case of a half-wave rectifier, from Eq. (7.3),

$$\text{Half-wave} \quad V_{RRM} = V_m = \frac{V_{dc}}{0.318} = 3.14 V_{dc} \tag{7.37}$$

In the case of a full-wave rectifier with center-tapped transformer, from Eq. (7.5),

$$\text{Full-wave} \quad V_{RRM} = 2V_m = \frac{2V_{dc}}{0.636} = 3.14 V_{dc} \tag{7.38}$$

In the case of a bridge rectifier, also from Eq. (7.5),

$$\text{Bridge} \quad V_{RRM} = V_m = \frac{V_{dc}}{0.636} = 1.57 V_{dc} \tag{7.39}$$

It is important to evaluate the I_{FRM} rating of the employed diodes in rectifier circuits.

In the case of a half-wave rectifier, from Eq. (7.13),

$$\text{Half-wave} \quad I_{FRM} = \frac{V_m}{R} = \frac{I_{dc}}{0.318} = 3.41 I_{dc} \tag{7.40}$$

In the case of full-wave rectifiers, from Eq. (7.15),

$$\text{Full-wave} \quad I_{FRM} = \frac{V_m}{R} = \frac{I_{dc}}{0.636} = 1.57 I_{dc} \tag{7.41}$$

The important design parameters of basic single-phase rectifier circuits with resistive loads are summarized in Table 7.2.

7.3 Three-Phase Diode Rectifiers

It has been shown in Section 7.2 that single-phase diode rectifiers require a rather high transformer VA rating for a given dc output power. Therefore, these rectifiers are suitable only for low-to-medium power applications. For power output higher than 15 kW, three-phase or polyphase diode rectifiers should be employed. There are two types of three-phase diode rectifier that convert a three-phase ac supply into a dc voltage, namely, star rectifiers and bridge rectifiers. In the following subsections, the operations of these rectifiers are examined, and their performances are analyzed and compared in tabulated form. For the sake of simplicity, the diodes and the transformers are considered to be ideal, that is, the diodes have zero forward voltage drop and reverse current and the transformers possess no resistance and no leakage inductance. Furthermore, it is assumed that the load is purely resistive, such that the load voltage and the load current have similar waveforms. In Section 7.5, Filtering Systems in Rectifier Circuits, the effects of inductive load and capacitive load on a diode rectifier are considered in detail.

7.3.1 Three-Phase Star Rectifiers

7.3.1.1 Basic Three-Phase Star Rectifier Circuit

A basic three-phase star rectifier circuit is shown in Fig. 7.7. This circuit can be considered as three single-phase half-wave rectifiers combined together. Therefore, it is sometimes referred to as a three-phase half-wave rectifier. The diode in a particular phase conducts during the period when the voltage on that phase is higher than that on the other two phases. The

TABLE 7.2 Important design parameters of basic single-phase rectifier circuits with resistive load

	Half-wave rectifier	Full-wave rectifier with center-tapped transformer	Full-wave bridge rectifier
Peak repetitive reverse voltage V_{RRM}	$3.14V_{dc}$	$3.14V_{dc}$	$1.57V_{dc}$
RMS input voltage per transformer leg V_s	$2.22V_{dc}$	$1.11V_{dc}$	$1.11V_{dc}$
Diode average current $I_{F(AV)}$	$1.00I_{dc}$	$0.50I_{dc}$	$0.50I_{dc}$
Peak repetitive forward current I_{FRM}	$3.14I_{F(AV)}$	$1.57I_{F(AV)}$	$1.57I_{F(AV)}$
Diode rms current $I_{F(RMS)}$	$1.57I_{dc}$	$0.785I_{dc}$	$0.785I_{dc}$
Form factor of diode current $I_{F(RMS)}/I_{F(AV)}$	1.57	1.57	1.57
Rectification ratio	0.405	0.81	0.81
Form factor	1.57	1.11	1.11
Ripple factor	1.21	0.482	0.482
Transformer rating primary VA	$2.69P_{dc}$	$1.23P_{dc}$	$1.23P_{dc}$
Transformer rating secondary VA	$3.49P_{dc}$	$1.75P_{dc}$	$1.23P_{dc}$
Output ripple frequency f_r	$1f_i$	$2f_i$	$2f_i$

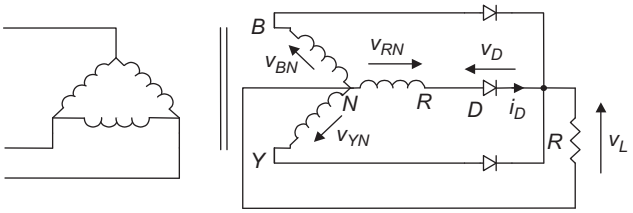


FIG. 7.7 Three-phase star rectifier.

voltage waveforms of each phase and the load are shown in Fig. 7.8. It is clear that, unlike the single-phase rectifier circuit, the conduction angle of each diode is $2\pi/3$, instead of π. This circuit finds uses where the required dc output voltage is relatively low, and the required output current is too large for a practical single-phase system.

Taking phase R as an example, diode D conducts from $\pi/6$ to $5\pi/6$. Therefore, using Eq. (7.1), the average value of the output can be found as

$$V_{dc} = \frac{3}{2\pi}\int_{\pi/6}^{5\pi/6} V_m \sin\theta d\theta \tag{7.42}$$

or

$$V_{dc} = V_m \frac{3}{\pi}\frac{\sqrt{3}}{2} = 0.827V_m \tag{7.43}$$

Similarly, using Eq. (7.6), the rms value of the output voltage can be found as

$$V_L = \sqrt{\frac{3}{2\pi}\int_{\pi/6}^{5\pi/6} (V_m \sin\theta)^2 d\theta} \tag{7.44}$$

or

$$V_L = V_m\sqrt{\frac{3}{2\pi}\left(\frac{\pi}{3} + \frac{\sqrt{3}}{4}\right)} = 0.84V_m \tag{7.45}$$

In addition, the rms current in each transformer secondary winding can also be found as

$$I_s = I_m\sqrt{\frac{1}{2\pi}\left(\frac{\pi}{3} + \frac{\sqrt{3}}{4}\right)} = 0.485I_m \tag{7.46}$$

where $I_m = V_m/R$.

Based on the relationships stated in Eqs. (7.43), (7.45), (7.46), all the important design parameters of the three-phase star rectifier can be evaluated, as listed in Table 7.3, which is given at the end of Section 7.3.2. Note that, as with a single-phase half-wave rectifier, the three-phase star rectifier shown in Fig. 7.7 has direct currents in the secondary windings that can cause a transformer core saturation problem. In addition, the currents in the primary do not sum to zero. Therefore, it is preferable not to have star-connected primary windings.

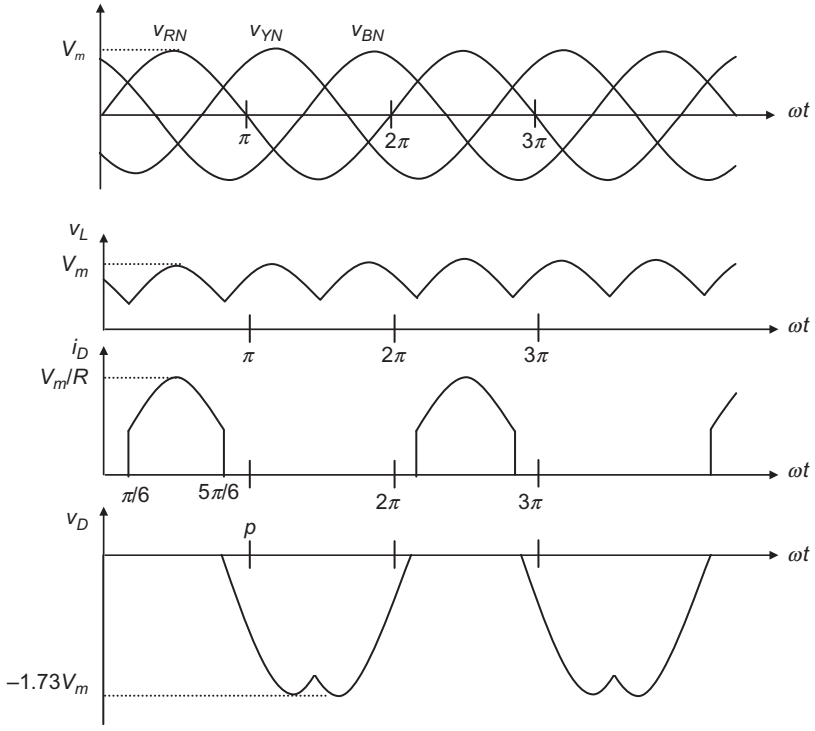


FIG. 7.8 Waveforms of voltage and current of the three-phase star rectifier shown in Fig. 7.7.

TABLE 7.3 Important design parameters of the three-phase rectifier circuits with the resistive load

	Three-phase star rectifier	Three-phase double-star rectifier with interphase transformer	Three-phase bridge rectifier
Peak repetitive reverse voltage V_{RRM}	$2.092V_{dc}$	$1.06V_{dc}$	$1.05V_{dc}$
RMS input voltage per transformer leg V_s	$0.855V_{dc}$	$0.855V_{dc}$	$0.428V_{dc}$
Diode average current $I_{F(AV)}$	$0.333I_{dc}$	$0.167I_{dc}$	$0.333I_{dc}$
Peak repetitive forward current I_{FRM}	$3.63I_{F(AV)}$	$3.15I_{F(AV)}$	$3.14I_{F(AV)}$
Diode rms current $I_{F(RMS)}$	$0.587I_{dc}$	$0.293I_{dc}$	$0.579I_{dc}$
Form factor of diode current $I_{F(RMS)}/I_{F(AV)}$	1.76	1.76	1.74
Rectification ratio	0.968	0.998	0.998
Form factor	1.0165	1.0009	1.0009
Ripple factor	0.182	0.042	0.042
Transformer rating primary VA	$1.23P_{dc}$	$1.06P_{dc}$	$1.05P_{dc}$
Transformer rating secondary VA	$1.51P_{dc}$	$1.49P_{dc}$	$1.05P_{dc}$
Output ripple frequency f_r	$3f_i$	$6f_i$	$6f_i$

7.3.1.2 Three-Phase Interstar Rectifier Circuit

The transformer core saturation problem in the three-phase star rectifier can be avoided by a special arrangement in its secondary windings, known as zigzag connection. The modified circuit is called the three-phase interstar or zigzag rectifier circuit, as shown in Fig. 7.9. Each secondary-phase voltage is obtained from two equal-voltage secondary windings (with a phase displacement of $\pi/3$) connected in series so that the dc magnetizing forces due to the two secondary windings on any limb are equal and opposite. At the expense of extra secondary windings (increasing the transformer secondary rating factor from 1.51 to 1.74 VA/W), this circuit connection eliminates the effects of core saturation and reduces the transformer primary rating factor to the minimum of 1.05 VA/W. Apart from transformer ratings, all the design parameters of this circuit are the same as those of a three-phase star rectifier (therefore not separately listed in Table 7.3). Furthermore, a star-connected primary winding with no neutral connection is equally permissible because the sum of all primary phase currents is zero at all times.

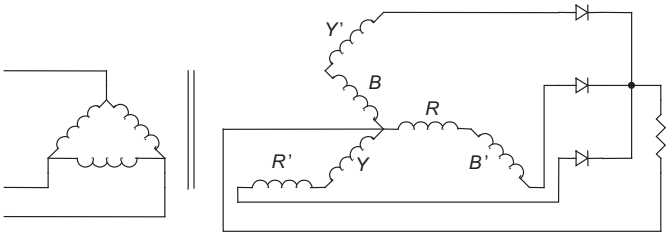


FIG. 7.9 Three-phase interstar rectifier.

7.3.1.3 Three-Phase Double-Star Rectifier With Interphase Transformer

This circuit consists essentially of two three-phase star rectifiers with their neutral points interconnected through an interphase transformer or reactor (Fig. 7.10). The polarities of the corresponding secondary windings in the two interconnected systems are reversed with respect to each other, so that the rectifier output voltage of one three-phase unit is at a minimum when the rectifier output voltage of the other unit is at a maximum as shown in Fig. 7.11. The function of the interphase transformer is to cause the output voltage v_L to be the average of the rectified voltages $v1$ and $v2$ as shown in Fig. 7.11. In addition, the ripple frequency of the output voltage is now six times that of the mains, and therefore, the component size of the filter (if there is any) becomes smaller. In a balanced circuit, the

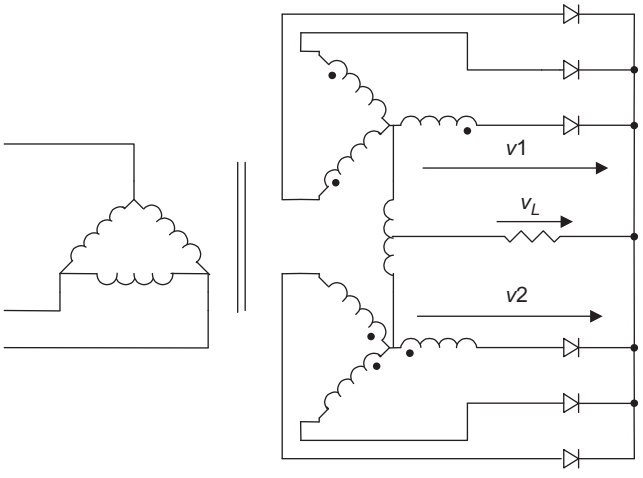


FIG. 7.10 Three-phase double-star rectifier with interphase transformer.

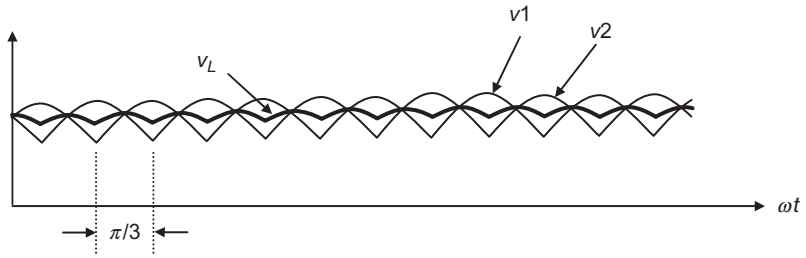


FIG. 7.11 Voltage waveforms of the three-phase double-star rectifier.

output currents of two three-phase units flowing in opposite directions in the interphase transformer winding will produce no dc magnetization current. Similarly, the dc magnetization currents in the secondary windings of two three-phase units cancel each other out.

By virtue of the symmetry of the secondary circuits, the three primary currents add up to zero at all times. Therefore, a star primary winding with no neutral connection would be equally permissible.

7.3.2 Three-Phase Bridge Rectifiers

Three-phase bridge rectifiers are commonly used for high-power applications because they have the highest possible transformer utilization factor for a three-phase system. The circuit of a three-phase bridge rectifier is shown in Fig. 7.12. The diodes are numbered in the order of conduction sequences, and the conduction angle of each diode is $2\pi/3$.

The conduction sequence for diodes is 12, 23, 34, 45, 56, and 61. The voltage and the current waveforms of the three-phase bridge rectifier are shown in Fig. 7.13. The line voltage is 1.73 times the phase voltage of a three-phase star-connected source. It is permissible to use any combination of star- or delta-connected primary and secondary windings because the currents associated with the secondary windings are symmetrical.

Using Eq. (7.1), the average value of the output can be found as

$$V_{dc} = \frac{6}{2\pi}\int_{\pi/3}^{2\pi/3} \sqrt{3}V_m \sin\theta d\theta \tag{7.47}$$

or

$$V_{dc} = V_m \frac{3\sqrt{3}}{\pi} = 1.654V_m \tag{7.48}$$

Similarly, using Eq. (7.6), the rms value of the output voltage can be found as

$$V_L = \sqrt{\frac{9}{\pi}\int_{\pi/3}^{2\pi/3} (V_m \sin\theta)^2 d\theta} \tag{7.49}$$

or

$$V_L = V_m \sqrt{\frac{3}{2} + \frac{9\sqrt{3}}{4\pi}} = 1.655V_m \tag{7.50}$$

In addition, the rms current in each transformer secondary winding can also be found as

$$I_s = I_m \sqrt{\frac{2}{\pi}\left(\frac{\pi}{6} + \frac{\sqrt{3}}{4}\right)} = 0.78I_m \tag{7.51}$$

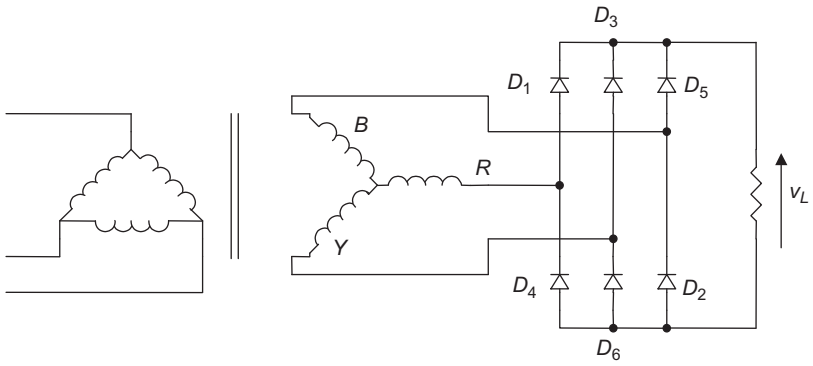


FIG. 7.12 Three-phase bridge rectifier.

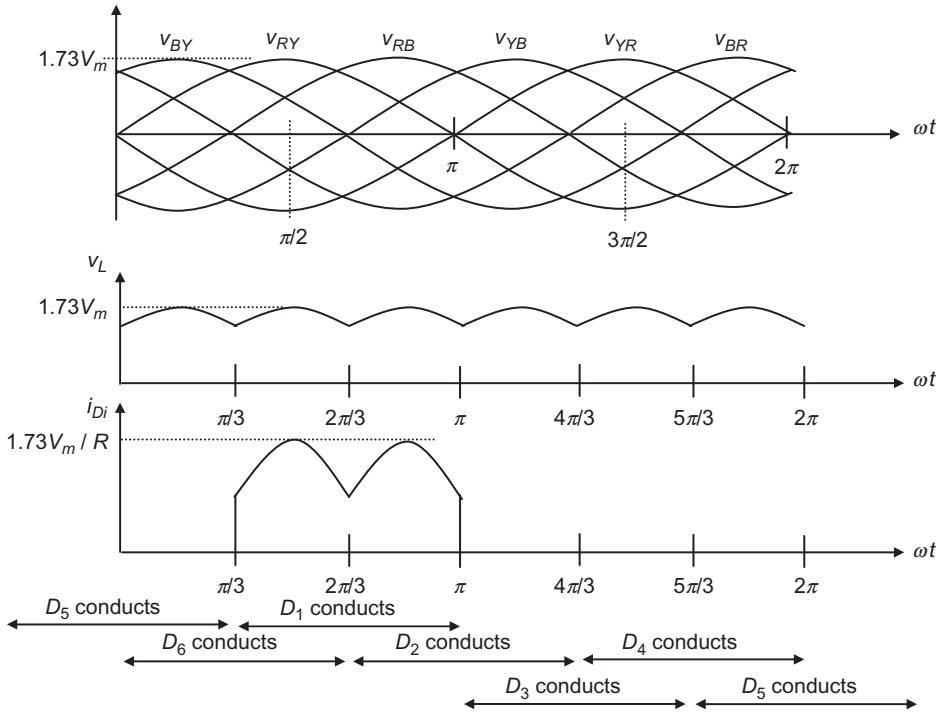


FIG. 7.13 Voltage and current waveforms of the three-phase bridge rectifier.

and the rms current through a diode is

$$I_D = I_m \sqrt{\frac{1}{\pi}\left(\frac{\pi}{6} + \frac{\sqrt{3}}{4}\right)} = 0.552 I_m \tag{7.52}$$

where $I_m = 1.73 V_m / R$.

Based on Eqs. (7.48), (7.50), (7.51), (7.52), all the important design parameters of the three-phase star rectifier can be evaluated, as listed in Table 7.3. The dc output voltage is slightly lower than the peak line voltage or 2.34 times the rms phase voltage. The V_{RRM} rating of the employed diodes is 1.05 times the dc output voltage, and the I_{FRM} rating of the employed diodes is 0.579 times the dc output current. Therefore, this three-phase bridge rectifier is very efficient and popular wherever both dc voltage and current requirements are high. In many applications, no additional filter is required because the output ripple voltage is only 4.2%. Even if a filter is required, the size of the filter is relatively small because the ripple frequency is increased to six times the input frequency.

7.3.3 Operation of Rectifiers With Finite Source Inductance

It has been assumed in the preceding sections that the commutation of current from one diode to the next takes place instantaneously when the interphase voltage assumes the necessary polarity. In practice, this is hardly possible because there are finite inductances associated with the source. For the purpose of discussing the effects of the finite source inductance, a three-phase star rectifier with transformer leakage inductances is shown in Fig. 7.14, where l_1, l_2, and l_3 denote the leakage inductances associated with the transformer secondary windings.

Refer to Fig. 7.15. At the time when v_{YN} is about to become larger than v_{RN}, due to leakage inductance l_1, the current in D_1 cannot fall to zero immediately. Similarly, due to the leakage inductance l_2, the current in D_2 cannot increase immediately to the full value. The result is that both the diodes conduct for a certain period, which is called the overlap (or commutation) angle. The overlap reduces the rectified voltage v_L as shown in the upper voltage waveform of Fig. 7.15. If all the leakage inductances are equal, that is, $l_1 = l_2 = l_3 = l_c$, then the amount of reduction of dc output voltage can be estimated as $mf_i l_c I_{dc}$, where m is the ratio of the lowest ripple frequency to the input frequency.

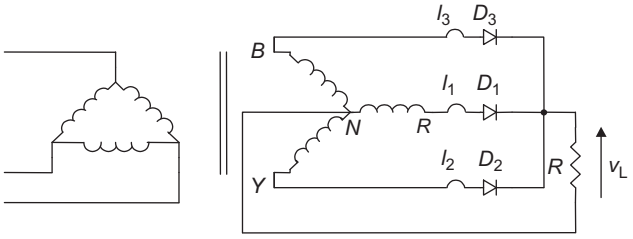


FIG. 7.14 Three-phase star rectifier with the transformer leakage inductances.

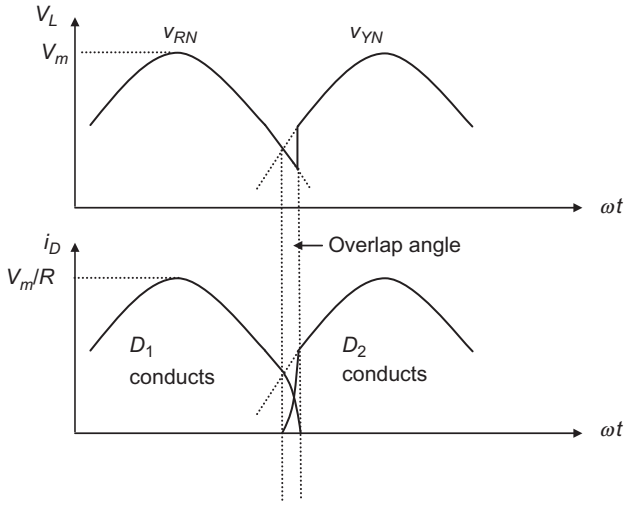


FIG. 7.15 Waveforms during commutation in Fig. 7.14.

For example, for a three-phase star rectifier operating from a 60 Hz supply with an average load current of 50 A, the amount of reduction of the dc output voltage is 2.7 V if the leakage inductance in each secondary winding is 300 μH.

7.4 Poly-Phase Diode Rectifiers

7.4.1 Six-Phase Star Rectifier

A basic six-phase star rectifier circuit is shown in Fig. 7.16. The six-phase voltages on the secondary are obtained by means of a center-tapped arrangement on a star-connected three-phase winding. Therefore, it is sometimes referred to as a three-phase full-wave rectifier. The diode in a particular phase conducts during the period when the voltage on that phase is higher than that on the other phases. The voltage waveforms

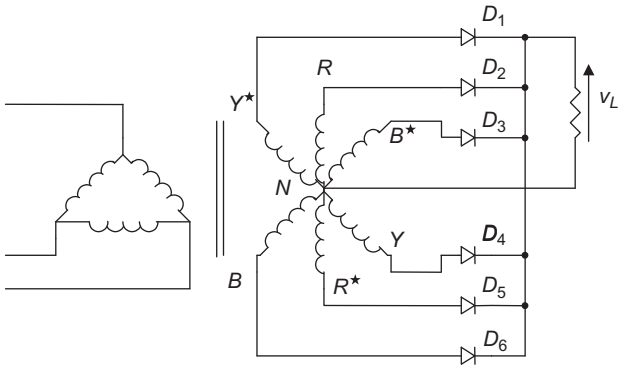


FIG. 7.16 Six-phase star rectifier.

of each phase and the load are shown in Fig. 7.17. It is clear that, unlike the three-phase star rectifier circuit, the conduction angle of each diode is $\pi/3$, instead of $2\pi/3$. Currents flow in only one rectifying element at a time, resulting in a low average current, but a high peak to an average current ratio in the diodes and poor transformer secondary utilization. Nevertheless, the dc currents in the secondary of the six-phase star rectifier cancel in the secondary windings like a full-wave rectifier and, therefore, core saturation is not encountered. This six-phase star circuit is attractive in applications that require a low ripple factor and a common cathode or anode for the rectifiers.

By considering the output voltage provided by v_{RN} between $\pi/3$ and $2\pi/3$, the average value of the output voltage can be found as

$$V_{dc} = \frac{6}{2\pi}\int_{\pi/3}^{2\pi/3} V_m \sin\theta d\theta \tag{7.53}$$

or

$$V_{dc} = V_m \frac{6}{\pi}\frac{1}{2} = 0.955 V_m \tag{7.54}$$

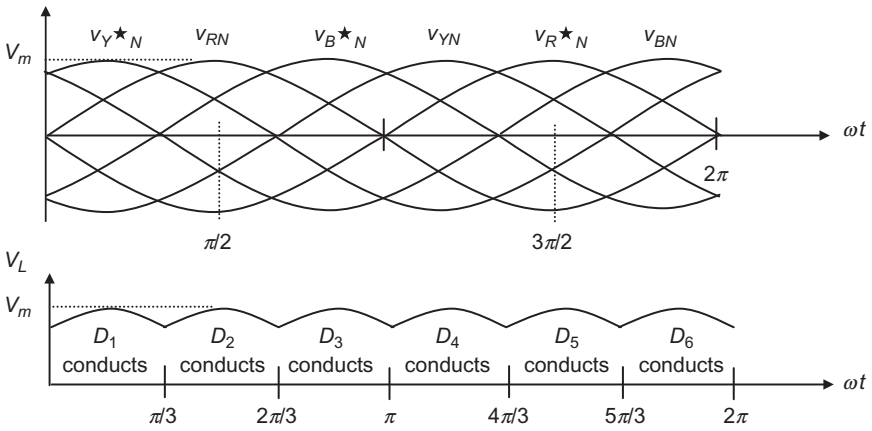


FIG. 7.17 Voltage waveforms of the six-phase star rectifier.

Similarly, the rms value of the output voltage can be found as

$$V_L = \sqrt{\frac{6}{2\pi}\int_{\pi/3}^{2\pi/3} (V_m \sin\theta)^2 d\theta} \tag{7.55}$$

or

$$V_L = V_m\sqrt{\frac{6}{2\pi}\left(\frac{\pi}{6}+\frac{\sqrt{3}}{4}\right)} = 0.956V_m \tag{7.56}$$

In addition, the rms current in each transformer secondary winding can also be found as

$$I_s = I_m\sqrt{\frac{1}{2\pi}\left(\frac{\pi}{6}+\frac{\sqrt{3}}{4}\right)} = 0.39I_m \tag{7.57}$$

where $I_m = V_m/R$.

Based on the relationships stated in Eqs. (7.55)–(7.57), all the important design parameters of the six-phase star rectifier can be evaluated, as listed in Table 7.4 (given at the end of Section 7.4.3).

7.4.2 Six-Phase Series Bridge Rectifier

The star- and delta-connected secondaries have an inherent $\pi/6$-phase displacement between their output voltages. When a star- and a delta-connected bridge rectifier are connected in series as shown in Fig. 7.18, the combined output voltage will have a doubled ripple frequency (12 times that of the mains). The ripple of the combined output voltage will also be reduced from 4.2% (for each individual bridge rectifier) to 1%. The combined bridge rectifier is referred to as a six-phase series bridge rectifier.

In the six-phase series bridge rectifier shown in Fig. 7.18, let V_m^* be the peak voltage of the delta-connected secondary. The peak voltage between the lines of the star-connected secondary is also V_m^*. The peak voltage across the load, denoted as V_m, is equal to $2V_m^* \times \cos(\pi/12)$ or $1.932V_m^*$ because there is $\pi/6$-phase displacement between the secondaries. The ripple frequency is twelve times the mains frequency. The average value of the output voltage can be found as

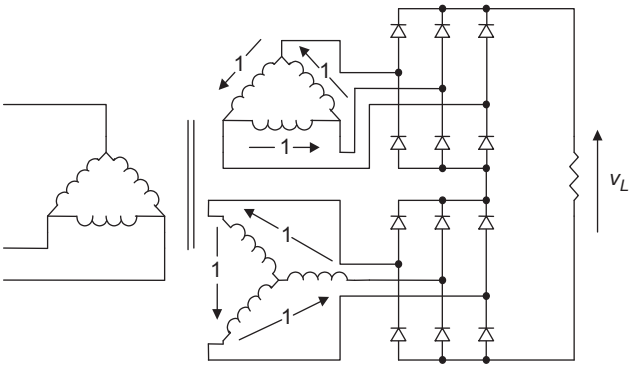


FIG. 7.18 Six-phase series bridge rectifier.

$$V_{dc} = \frac{12}{2\pi}\int_{5\pi/12}^{7\pi/12} V_m \sin\theta d\theta \tag{7.58}$$

or

$$V_{dc} = V_m\frac{12}{\pi}\frac{\sqrt{3}-1}{2\sqrt{2}} = 0.98862V_m \tag{7.59}$$

The rms value of the output voltage can be found as

$$V_L = \sqrt{\frac{12}{2\pi}\int_{5\pi/12}^{7\pi/12} (V_m \sin\theta)^2 d\theta} \tag{7.60}$$

or

$$V_L = V_m\sqrt{\frac{12}{2\pi}\left(\frac{\pi}{12}+\frac{1}{4}\right)} = 0.98867V_m \tag{7.61}$$

TABLE 7.4 Important design parameters of the six-phase rectifier circuits with resistive load

	Six-phase star rectifier	Six-phase series bridge rectifier	Six-phase parallel bridge rectifier (with interphase transformer)
Peak repetitive reverse voltage V_{RRM}	$2.09V_{dc}$	$0.524V_{dc}$	$1.05V_{dc}$
RMS input voltage per transformer leg V_s	$0.74V_{dc}$	$0.37V_{dc}$	$0.715V_{dc}$
Diode average current $I_{F(AV)}$	$0.167I_{dc}$	$0.333I_{dc}$	$0.167I_{dc}$
Peak repetitive forward current I_{FRM}	$6.28I_{F(AV)}$	$3.033I_{F(AV)}$	$3.14I_{F(AV)}$
Diode rms current $I_{F(RMS)}$	$0.409I_{dc}$	$0.576I_{dc}$	$0.409I_{dc}$
Form factor of diode current $I_{F(RMS)}/I_{F(AV)}$	2.45	1.73	2.45
Rectification ratio	0.998	1.00	1.00
Form factor	1.0009	1.00005	1.00005
Ripple factor	0.042	0.01	0.01
Transformer rating primary VA	$1.28P_{dc}$	$1.01P_{dc}$	$1.01P_{dc}$
Transformer rating secondary VA	$1.81P_{dc}$	$1.05P_{dc}$	$1.05P_{dc}$
Output ripple frequency f_r	$6f_i$	$12f_i$	$12f_i$

The rms current in each transformer secondary winding is

$$I_s = I_m\sqrt{\frac{4}{\pi}\left(\frac{\pi}{12}+\frac{1}{4}\right)} = 0.807I_m \tag{7.62}$$

The rms current through a diode is

$$I_s = I_m\sqrt{\frac{2}{\pi}\left(\frac{\pi}{12}+\frac{1}{4}\right)} = 0.57I_m \tag{7.63}$$

where $I_m = V_m/R$.

Based on Eqs. (7.59), (7.61), (7.62), (7.63), all the important design parameters of the six-phase series bridge rectifier can be evaluated, as listed in Table 7.4 (given at the end of Section 7.4.3).

7.4.3 Six-Phase Parallel Bridge Rectifier

The six-phase series bridge rectifier described above is useful for high-output voltage applications. However, for high-output current applications, the six-phase parallel bridge rectifier (with an interphase transformer) shown in Fig. 7.19 should be used.

The function of the interphase transformer is to cause the output voltage v_L to be the average of the rectified voltages $v1$ and $v2$ as shown in Fig. 7.20. As with the six-phase series bridge rectifier, the output ripple frequency of the six-phase parallel bridge rectifier is also 12 times that of the mains. Further filtering on the output voltage is usually not required. Assuming a balanced circuit, the output currents of two three-phase units (flowing in opposite directions in the interphase transformer winding) produce no dc magnetization current.

All the important design parameters of the six-phase parallel rectifiers with interphase transformer are also listed in Table 7.4.

7.5 Filtering Systems in Rectifier Circuits

Filters are commonly employed in rectifier circuits for smoothing out the dc output voltage of the load. They are classified as inductor-input dc filters and capacitor-input dc filters. Inductor-input dc filters are preferred in high-power applications because more efficient transformer operation is obtained due to the reduction in the form factor of the rectifier current. Capacitor-input dc filters can provide volumetrically efficient

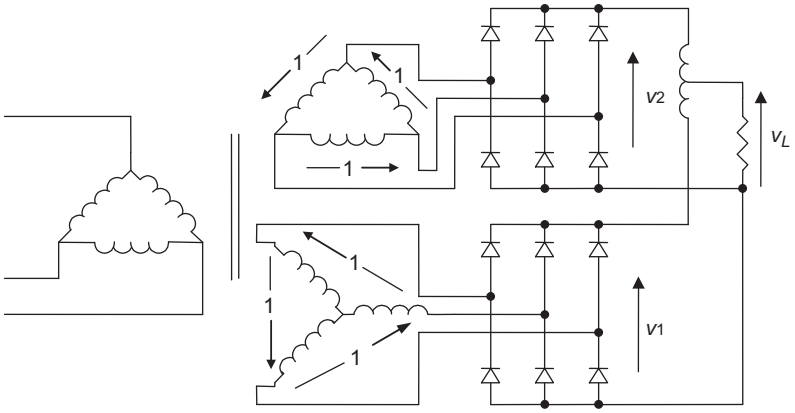


FIG. 7.19 Six-phase parallel bridge rectifier.

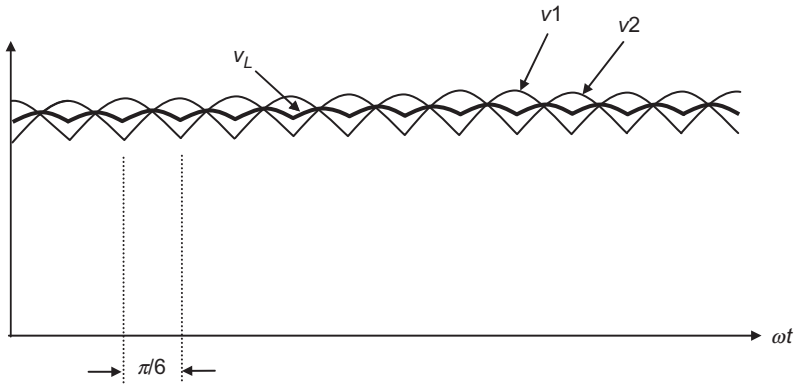


FIG. 7.20 Voltage waveforms of the six-phase bridge rectifier with interphase transformer.

operation, but they demand excessive turn-on and repetitive surge currents. Therefore, capacitor-input dc filters are suitable only for lower-power systems where close regulation is usually achieved by an electronic regulator cascaded with the rectifier.

7.5.1 Inductive-Input DC Filters

The simplest inductive-input dc filter is shown in Fig. 7.21A. The output current of the rectifier can be maintained at a steady value if the inductance of L_f is sufficiently large $(\omega L_f \gg R)$. The filtering action is more effective in heavy load conditions than in light load conditions. If the ripple attenuation is not sufficient even with large values of inductance, an L-section filter as shown in Fig. 7.21B can be used for further filtering. In practice, multiple L-section filters can also be employed if the requirement on the output ripple is very stringent.

For a simple inductive-input dc filter shown in Fig. 7.21A the ripple is reduced by the factor

$$\frac{v_o}{v_L} = \frac{R}{\sqrt{R^2 + (2\pi f_r L_f)^2}} \tag{7.64}$$

where v_L is the ripple voltage before filtering, v_o is the ripple voltage after filtering, and f_r is the ripple frequency.

For the inductive-input dc filter shown in Fig. 7.21B, the amount of reduction in the ripple voltage can be estimated as

$$\frac{v_o}{v_L} = \left| \frac{1}{1 - (2\pi f_r)^2 L_f C_f} \right| \tag{7.65}$$

where f_r is the ripple frequency, if $R \gg 1/2\pi f_r C_f$.

7.5.1.1 Voltage and Current Waveforms of Full-Wave Rectifier With Inductor-Input DC Filter

Fig. 7.22 shows a single-phase full-wave rectifier with an inductor-input dc filter. The voltage and current waveforms are illustrated in Fig. 7.23.

When the inductance of L_f is infinite, the current through the inductor and the output voltage are constant. When inductor L_f is finite, the current through the inductor has a ripple component, as shown by the dotted lines in Fig. 7.23. If the input inductance is too small, the current decreases to zero (becoming discontinuous) during a portion of the time between the peaks of the rectifier output voltage. The minimum value of inductance required to maintain a continuous current is known as the critical inductance L_C.

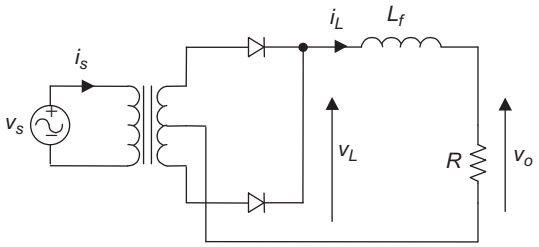


FIG. 7.22 A full-wave rectifier with inductor-input dc filter.

7.5.1.2 Critical Inductance L_C

In the case of single-phase full-wave rectifiers, the critical inductance can be found as

$$\text{Full-wave} \quad L_C = \frac{R}{6\pi f_i} \tag{7.66}$$

where f_i is the input mains frequency.

In the case of polyphase rectifiers, the critical inductance can be found as

$$\text{Poly-phase} \quad L_C = \frac{R}{3\pi m(m^2 - 1) f_i} \tag{7.67}$$

where m is ratio of the lowest ripple frequency to the input frequency, for example, $m = 6$ for a three-phase bridge rectifier.

7.5.1.3 Determining the Input Inductance for a Given Ripple Factor

In practice, the choice of the input inductance depends on the required ripple factor of the output voltage. The ripple voltage of a rectifier without filtering can be found by means of Fourier analysis. For example, the coefficient of the nth harmonic component of the rectified voltage v_L shown in Fig. 7.22 can be expressed as

$$v_{L_n} = \frac{-4V_m}{\pi(n^2 - 1)} \tag{7.68}$$

where $n = 2, 4, 8, \ldots$, etc.

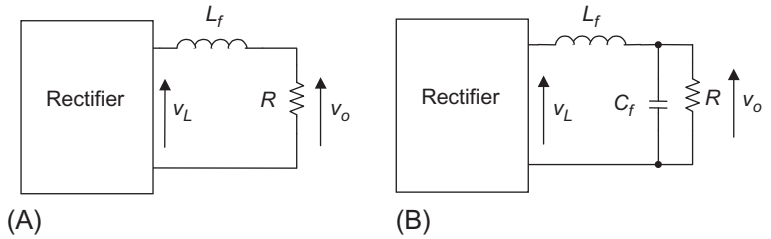


FIG. 7.21 Inductive-input dc filters. (A) Simple inductive-input dc filter. (B) L-section filter.

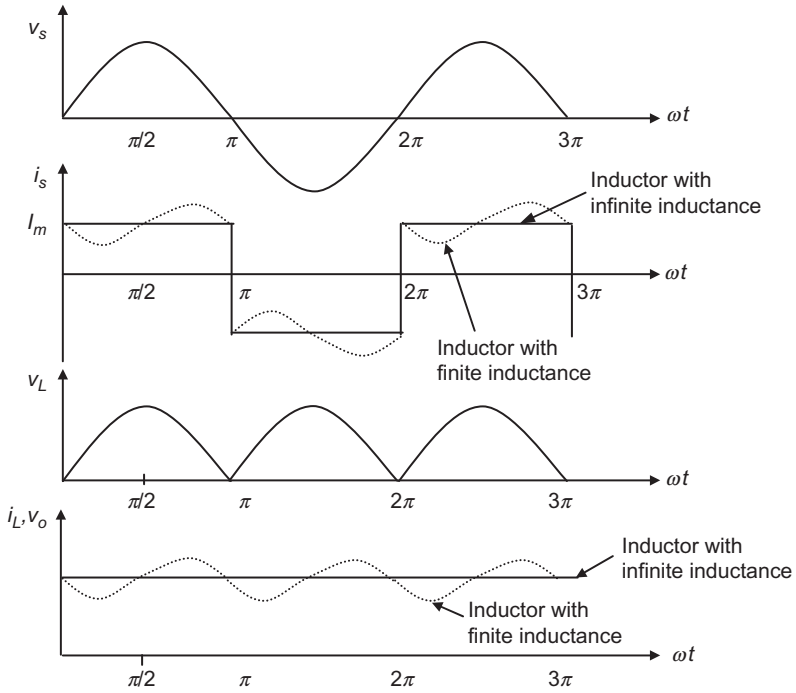


FIG. 7.23 Voltage and current waveforms of full-wave rectifier with inductor-input dc filter.

The dc component of the rectifier voltage is given by Eq. (7.5). Therefore, in addition to Eq. (7.27), the ripple factor can also be expressed as

$$\text{RF} = \sqrt{2 \sum_{n=2,4,8,} \left(\frac{1}{n^2-1}\right)^2} \tag{7.69}$$

Considering only the lowest-order harmonic ($n = 2$), the output ripple factor of a simple inductor-input dc filter (without C_f) can be found, from Eqs. (7.64) and (7.69), as

$$\text{Filtered RF} = \frac{0.4714}{\sqrt{1 + \left(4\pi f_i L_f / R\right)^2}} \tag{7.70}$$

7.5.1.4 Harmonics of the Input Current

In general, the total harmonic distortion (THD) of an input current is defined as

$$\text{THD} = \sqrt{\left(\frac{I_s}{I_{s1}}\right)^2 - 1} \tag{7.71}$$

where I_s is the rms value of the input current and I_{s1} and the rms value of the fundamental component of the input current. The THD can also be expressed as

$$\text{THD} = \sqrt{\sum_{n=2,3,4,} \left(\frac{I_{sn}}{I_{s1}}\right)^2} \tag{7.72}$$

where I_{sn} is the rms value of the nth harmonic component of the input current.

Moreover, the input power factor is defined as

$$\text{PF} = \frac{I_{s1}}{I_s} \cos\phi \tag{7.73}$$

where ϕ is the displacement angle between the fundamental components of the input current and voltage.

Assume that inductor L_f of the circuit shown in Fig. 7.22 has an infinitely large inductance. The input current is then a square wave. This input current contains undesirable higher harmonics that reduce the input power factor of the system. The input current can be easily expressed as

$$i_s = \frac{4I_m}{\pi} \sum_{n=1,3,5,} \frac{1}{n} \sin 2n\pi f_i t \tag{7.74}$$

The rms values of the input current and its fundamental component are I_m and $4I_m/\left(\pi\sqrt{2}\right)$, respectively. Therefore, the THD of the input current of this circuit is 0.484. Since the displacement angle is $\phi = 0$, the power factor is $4/\left(\pi\sqrt{2}\right) = 0.9$.

The power factor of the circuit shown in Fig. 7.22 can be improved by installing an ac filter between the source and the rectifier, as shown in Fig. 7.24.

Considering only the harmonic components, the equivalent circuit of the rectifier given in Fig. 7.24 can be found as shown in Fig. 7.25. The rms value of the nth harmonic current appearing in the supply can then be obtained using the current divider rule:

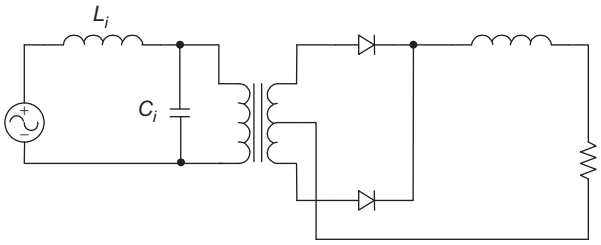


FIG. 7.24 Rectifier with input ac filter.

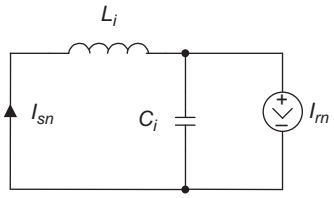


FIG. 7.25 Equivalent circuit for input ac filter.

$$I_{sn} = \left| \frac{1}{1 - (2n\pi f_i)^2 L_i C_i} \right| I_{rn} \tag{7.75}$$

where I_{rn} is the rms value of the nth harmonic current of the rectifier.

Applying Eq. (7.73) and knowing $I_{rn}/I_{r1} = 1/n$ from Eq. (7.74), the THD of the rectifier with input filter shown in Fig. 7.24 can be found as

$$\text{Filtered THD} = \sqrt{\sum_{n=3,5} \frac{1}{n^2} \left| \frac{1}{1 - (2n\pi f_i)^2 L_i C_i} \right|^2} \tag{7.76}$$

The important design parameters of typical single-phase and three-phase rectifiers with inductor-input dc filter are listed in Table 7.5. Note that, in a single-phase half-wave rectifier, a freewheeling diode is required to be connected across the input of the dc filters such that the flow of load current can be maintained during the negative half cycle of the supply voltage.

7.5.2 Capacitive-Input DC Filters

Fig. 7.26 shows a full-wave rectifier with capacitor-input dc filter. The voltage and current waveforms of this rectifier are shown in Fig. 7.27. When the instantaneous voltage of the secondary winding v_s is higher than the instantaneous value of capacitor voltage v_L, either D_1 or D_2 conducts, and the capacitor C is charged up from the transformer. When the instantaneous voltage of the secondary winding v_s falls below the instantaneous value of capacitor voltage v_L, both the diodes are reverse biased and the capacitor C is discharged through load resistance R. The resulting capacitor voltage v_L varies between a maximum value of V_m and a minimum value of $V_m - V_{r(pp)}$ as shown in Fig. 7.27. ($V_{r(pp)}$ is the peak-to-peak ripple voltage.) As shown in Fig. 7.27, the conduction angle θ_c of the diodes becomes smaller when the output ripple voltage decreases. Consequently, the power supply and the diodes suffer from high repetitive surge currents. An LC ac filter, as shown in Fig. 7.24, may be required to improve the input power factor of the rectifier.

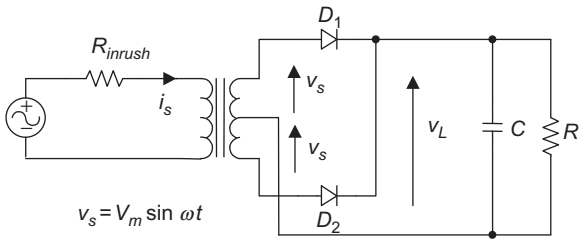


FIG. 7.26 Full-wave rectifier with capacitor-input dc filter.

TABLE 7.5 Important design parameters of typical rectifier circuits with inductor-input dc filter

	Full-wave rectifier with center-tapped transformer	Full-wave bridge rectifier	Three-phase star rectifier	Three-phase bridge rectifier	Three-phase double-star rectifier with interphase transformer
Peak repetitive reverse voltage V_{RRM}	$3.14V_{dc}$	$1.57V_{dc}$	$2.09V_{dc}$	$1.05V_{dc}$	$2.42V_{dc}$
RMS input voltage per transformer leg V_s	$1.11V_{dc}$	$1.11V_{dc}$	$0.885V_{dc}$	$0.428V_{dc}$	$0.885V_{dc}$
Diode average current $I_{F(AV)}$	$0.5I_{dc}$	$0.5I_{dc}$	$0.333I_{dc}$	$0.333I_{dc}$	$0.167I_{dc}$
Peak repetitive forward current I_{FRM}	$2.00I_{F(AV)}$	$2.00I_{F(AV)}$	$3.00I_{F(AV)}$	$3.00I_{F(AV)}$	$3.00I_{F(AV)}$
Diode rms current $I_{F(RMS)}$	$0.707I_{dc}$	$0.707I_{dc}$	$0.577I_{dc}$	$0.577I_{dc}$	$0.289I_{dc}$
Form factor of diode current $I_{F(RMS)}/I_{F(AV)}$	1.414	1.414	1.73	1.73	1.73
Transformer rating primary VA	$1.11P_{dc}$	$1.11P_{dc}$	$1.21P_{dc}$	$1.05P_{dc}$	$1.05P_{dc}$
Transformer rating secondary VA	$1.57P_{dc}$	$1.11P_{dc}$	$1.48P_{dc}$	$1.05P_{dc}$	$1.48P_{dc}$
Output ripple frequency f_r	$2f_i$	$2f_i$	$3f_i$	$6f_i$	$6f_i$
Ripple component V_r at					
(a) Fundamental	$0.667V_{dc}$	$0.667V_{dc}$	$0.250V_{dc}$	$0.057V_{dc}$	$0.057V_{dc}$
(b) Second harmonic	$0.133V_{dc}$	$0.133V_{dc}$	$0.057V_{dc}$	$0.014V_{dc}$	$0.014V_{dc}$
(c) Third harmonic of the ripple frequency	$0.057V_{dc}$	$0.057V_{dc}$	$0.025V_{dc}$	$0.006V_{dc}$	$0.006V_{dc}$

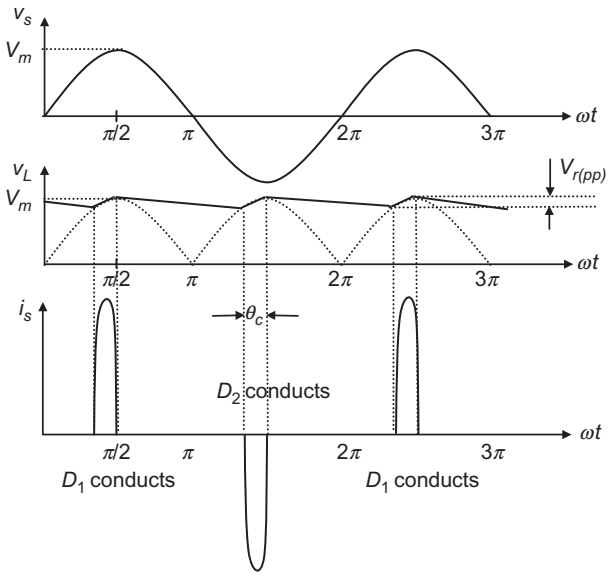


FIG. 7.27 Voltage and current waveforms of the full-wave rectifier with capacitor-input dc filter.

In practice, if the peak-to-peak ripple voltage is small, it can be approximated as

$$V_{r(pp)} = \frac{V_m}{f_r RC} \tag{7.77}$$

where f_r is the output ripple frequency of the rectifier.

Therefore, the average output voltage V_{dc} is given by

$$V_{dc} = V_m\left(1 - \frac{1}{2f_r RC}\right) \tag{7.78}$$

The rms output ripple voltage V_{ac} is approximately given by

$$V_{ac} = \frac{V_m}{2\sqrt{2} f_r RC} \tag{7.79}$$

The ripple factor RF can be found from

$$\text{RF} = \frac{1}{\sqrt{2}(2f_r RC - 1)} \tag{7.80}$$

7.5.2.1 Inrush Current

The resistor R_{inrush} in Fig. 7.26 is used to limit the inrush current imposed on the diodes during the instant when the rectifier is being connected to the supply. The inrush current can be very large because capacitor C has zero charge initially. The worst case occurs when the rectifier is connected to the supply at its maximum voltage. The worst-case inrush current can be estimated from

$$I_{inrush} = \frac{V_m}{R_{sec} + R_{ESR}} \tag{7.81}$$

where R_{sec} is the equivalent resistance looking from the secondary transformer and R_{ESR} is the equivalent series resistance (ESR) of the filtering capacitor. Hence, the employed diode should be able to withstand the inrush current for a half cycle of the input voltage. In other words, the *maximum allowable surge current* (I_{FSM}) rating of the employed diodes must be higher than the inrush current. The equivalent resistance associated with the transformer windings and the filtering capacitor is usually sufficient to limit the inrush current to an acceptable level. However, in cases where the transformer is omitted, for example, the rectifier of an off-line switch-mode supply, resistor R_{inrush} must be added for controlling the inrush current.

Consider as an example, a single-phase bridge rectifier, which is to be connected to a 120 V to 60 Hz source (without transformer). Assume that the I_{FSM} rating of the diodes is 150 A for an interval of 8.3 ms. If the ESR of the filtering capacitor is zero, the value of the resistor for limiting inrush current resistance can be estimated to be 1.13 Ω using Eq. (7.81).

7.6 High-Frequency Diode Rectifier Circuits

In high-frequency converters, diodes perform various functions, such as rectifying, flywheeling, and clamping. One special quality a high-frequency diode must possess is a fast switching speed. In technical terms, it must have a short reverse recovery time and a short forward recovery time.

The reverse recovery time of a diode may be understood as the time a forwardly conducting diode takes to recover to a blocking state when the voltage across it is suddenly reversed (which is known as forced turnoff). The temporary short circuit during the reverse recovery period may result in large reverse current, excessive ringing, and large power dissipation, all of which are highly undesirable.

The forward recovery time of a diode may be understood as the time a nonconducting diode takes to change to the fully on state when a forward current is suddenly forced into it (which is known as forced turn-on). Before the diode reaches the fully on state, the forward voltage drop during the forward recovery time can be significantly higher than the normal on-state voltage drop. This may cause voltage spikes in the circuit.

It should be interesting to note that, as far as circuit operation is concerned, a diode with a long reverse recovery time is similar to a diode with a large parasitic capacitance. A diode with a long forward recovery time is similar to a diode with a large parasitic inductance. (Spikes caused by the slow forward recovery of diodes are often wrongly thought to be caused by leakage inductance.) Comparatively, the adverse effect of a long reverse recovery time is much worse than that of a long forward recovery time.

Among commonly used diodes, the Schottky diode has the shortest forward and reverse recovery times. Schottky diodes

are therefore most suitable for high-frequency applications. However, Schottky diodes have relatively low reverse breakdown voltage (normally lower than 200 V) and large leakage current. If, due to these limitations, Schottky diodes cannot be used, ultrafast diodes should be used in high-frequency converter circuits.

Using the example of a forward converter, the operations of a forward rectifier diode, a flywheel diode, and a clamping diode will be studied in Section 7.6.1. Because of the difficulties encountered in the full analyses taking into account parasitic/stray/leakage components, PSpice simulations are extensively used here to study the following:

- The idealized operation of the converter
- The adverse effects of relatively slow rectifiers (e.g., the so-called ultrafast diodes, which are actually much slower than Schottky diodes)
- The improvement achievable by using high-speed rectifiers (Schottky diodes)
- The effects of leakage inductance of the transformer
- The use of snubber circuits to reduce ringing
- The operation of a practical converter with snubber circuits

Using the example of a flyback converter, the operations of a flyback rectifier diode and a clamping diode will also be studied in Section 7.6.2.

The design considerations for high-frequency diode rectifier circuits will be discussed in Section 7.6.3. Some precautions that must be taken in the interpretation of computer simulation results are briefed in Section 7.6.4.

7.6.1 Forward Rectifier Diode, Flywheel Diode, and Magnetic-Reset Clamping Diode in a Forward Converter

7.6.1.1 Ideal Circuit

Fig. 7.28 shows the basic circuit of a forward converter. Fig. 7.29 shows the idealized steady-state waveforms for continuous-mode operation (the current in L_1 being continuous). These waveforms are obtained from PSpice simulations, based on the following assumptions:

- Rectifier diode D_R, flywheel diode D_F, and magnetic-reset clamping diode D_M are ideal diodes with infinitely fast switching speed.
- Electronic switch $M1$ is an idealized MOS switch with infinitely fast switching speed and

$$\text{On-state resistance} = 0.067\ \Omega$$
$$\text{Off-state resistance} = 1\ \text{M}\Omega$$

  It should be noted that PSpice does not allow a switch to have zero on-state resistance and infinite off-state resistance.
- Transformer T_1 has a coupling coefficient of 0.99999999. PSpice does not accept a coupling coefficient of 1.
- The switching operation of the converter has reached a steady state.

Referring to the circuit shown in Fig. 7.28 and the waveforms shown in Fig. 7.29, the operation of the converter can be explained as follows:

1. For $0 < t < DT$ (D is the duty cycle of the MOS switch M_1 and T is the switching period of the converter. M_1 is turned on when $V1$ (VPULSE) is 15 V and turned off when $V1$(VPULSE) is 0 V).

   The switch M_1 is turned on at $t = 0$.

   The voltage at node 3, denoted as $V(3)$, is

$$V(3) = 0 \quad \text{for} \quad 0 < t < DT \tag{7.82}$$

   The voltage induced at node 6 of the secondary winding L_S is

$$V(6) = V_{IN}\left(N_s/N_p\right) \tag{7.83}$$

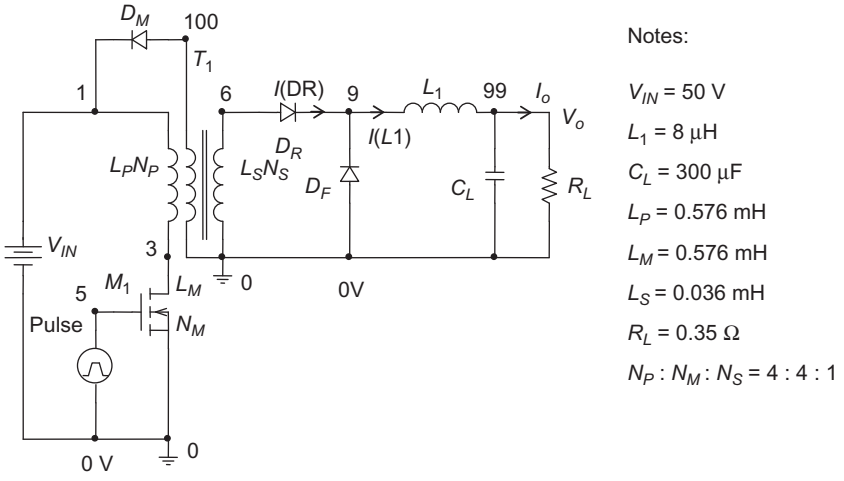


FIG. 7.28 Basic circuit of forward converter.

This voltage drives a current $I(DR)$ (current through rectifier diode D_R) into the output circuit to produce the output voltage V_o. The rate of increase of $I(DR)$ is given by

$$\frac{dI(DR)}{dt} = \left[V_{IN}\frac{N_S}{N_P} - V_o\right]\frac{1}{L_1} \tag{7.84}$$

where V_o is the dc output voltage of the converter.

The flywheel diode D_F is reversely biased by $V(9)$, the voltage at node 9:

$$V(9) = V_{IN}(N_S/N_P) \quad \text{for} \quad 0 < t < DT \tag{7.85}$$

The magnetic-reset clamping diode D_M is reversely biased by the negative voltage at node 100. Assuming that L_M and L_P have the same number of turns, we have

$$V(100) = -V_{IN} \quad \text{for } 0 < t < DT \tag{7.86}$$

A magnetizing current builds up linearly in L_P. This magnetizing current reaches the maximum value of $(V_{IN}DT)/L_P$ at $t = DT$.

2. For $DT < t < 2DT$

The switch M_1 is turned off at $t = DT$.

The collapse of magnetic flux induces a back emf in L_M, which is equal to L_P, to turn-on the clamping diode D_M. The magnetizing current in L_M drops (from the maximum value of $(V_{IN}\ DT)/L_P$, as mentioned above) at the rate of V_{IN}/L_P. It reaches zero at $t = 2DT$.

The back emf induced across L_P is equal to V_{IN}. The voltage at node 3 is

$$V(3) = 2V_{IN} \quad \text{for } DT < t < 2DT \tag{7.87}$$

The back emf across L_S forces D_R to stop conducting.

The inductive current in L_1 forces the flywheel diode D_F to conduct. $I(L1)$ (current through L_1) falls at the rate of

$$\frac{dI(L1)}{dt} = \frac{-V_o}{L_1} \tag{7.88}$$

The voltage across D_R, denoted as $V(6,9)$ (the voltage at node 6 with respect to node 9), is

$$\begin{aligned} V(DR) &= V(6,9) \\ &= -V_{IN}(N_S/N_P) \quad \text{for } DT < t < 2DT \end{aligned} \tag{7.89}$$

3. For $2DT < t < T$

D_M stops conducting at $t = 2DT$. The voltage across L_M then falls to zero.

The voltage across L_P is zero:

$$V(3) = V_{IN} \tag{7.90}$$

The voltage across L_S is also zero:

$$V(6) = 0 \tag{7.91}$$

Inductive current $I(L1)$ continues to fall at the rate of

$$\frac{dI(L1)}{dt} = \frac{-V_o}{L_1} \tag{7.92}$$

The switching cycle restarts when the switch M_1 is turned on again at $t = T$.

From the waveforms shown in Fig. 7.29, the following useful information (for continuous-mode operation) can be found:

- The output voltage V_o is equal to the average value of $V(9)$:

$$V_o = \mathrm{D}\frac{N_S}{N_P}V_{IN} \tag{7.93}$$

- The maximum current in the forward rectifying diode D_R and flywheel diode D_F is

$$\begin{aligned} I(DR)_{max} &= I(DF)_{max} \\ &= I_o + \frac{1}{2}\frac{V_o}{L_1}(1-D)T \end{aligned} \tag{7.94}$$

where $V_o = \mathrm{D}V_{IN}(N_S/N_P)$ and I_o is the output loading current.

- The maximum reverse voltage of D_R and D_F is

$$\begin{aligned} V(DR)_{max} &= V(DF)_{max} \\ &= V(6,9)_{max} = V_{IN}\frac{N_S}{N_P} \end{aligned} \tag{7.95}$$

- The maximum reverse voltage of D_M is

$$V(DM)_{max} = V_{IN} \tag{7.96}$$

- The maximum current in D_M is

$$I(DM)_{max} = DT\frac{V_{IN}}{L_P} \tag{7.97}$$

- The maximum current in the switch $M1$, denoted as $ID(M1)$, is

$$\begin{aligned} ID(M1)_{max} &= \frac{N_S}{N_P}I(DR)_{max} + I(DM)_{max} \\ &= \frac{N_S}{N_P}\left[I_o + \frac{1}{2}\frac{V_o}{L_1}(1-D)T\right] + DT\frac{V_{IN}}{L_P} \end{aligned} \tag{7.98}$$

It should, however, be understood that, due to the nonideal characteristics of practical components, the idealized waveforms shown in Fig. 7.29 cannot actually be achieved in the real world. In the following, the effects of nonideal diodes and transformers will be examined.

7.6.1.2 Circuit Using Ultra-Fast Diodes

Fig. 7.30 shows the waveforms of the forward converter (circuit given in Fig. 7.28) when ultrafast diodes are used as D_M, D_R, and D_F. (Note that ultrafast diodes are actually much slower than Schottky diodes.) The waveforms are obtained by PSpice simulations, based on the following assumptions:

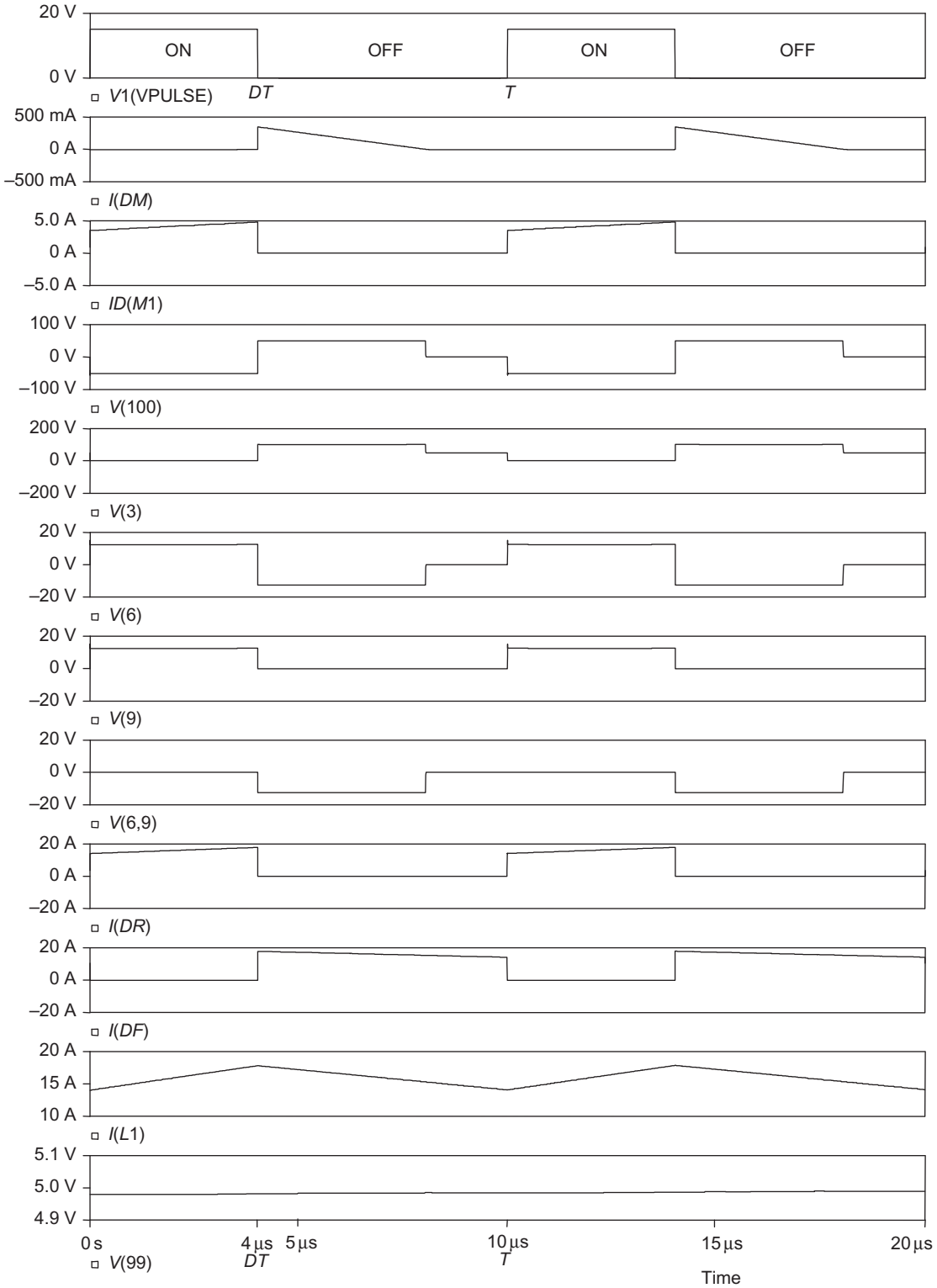


FIG. 7.29 Idealized steady-state waveforms of forward converter for continuous-mode operation.

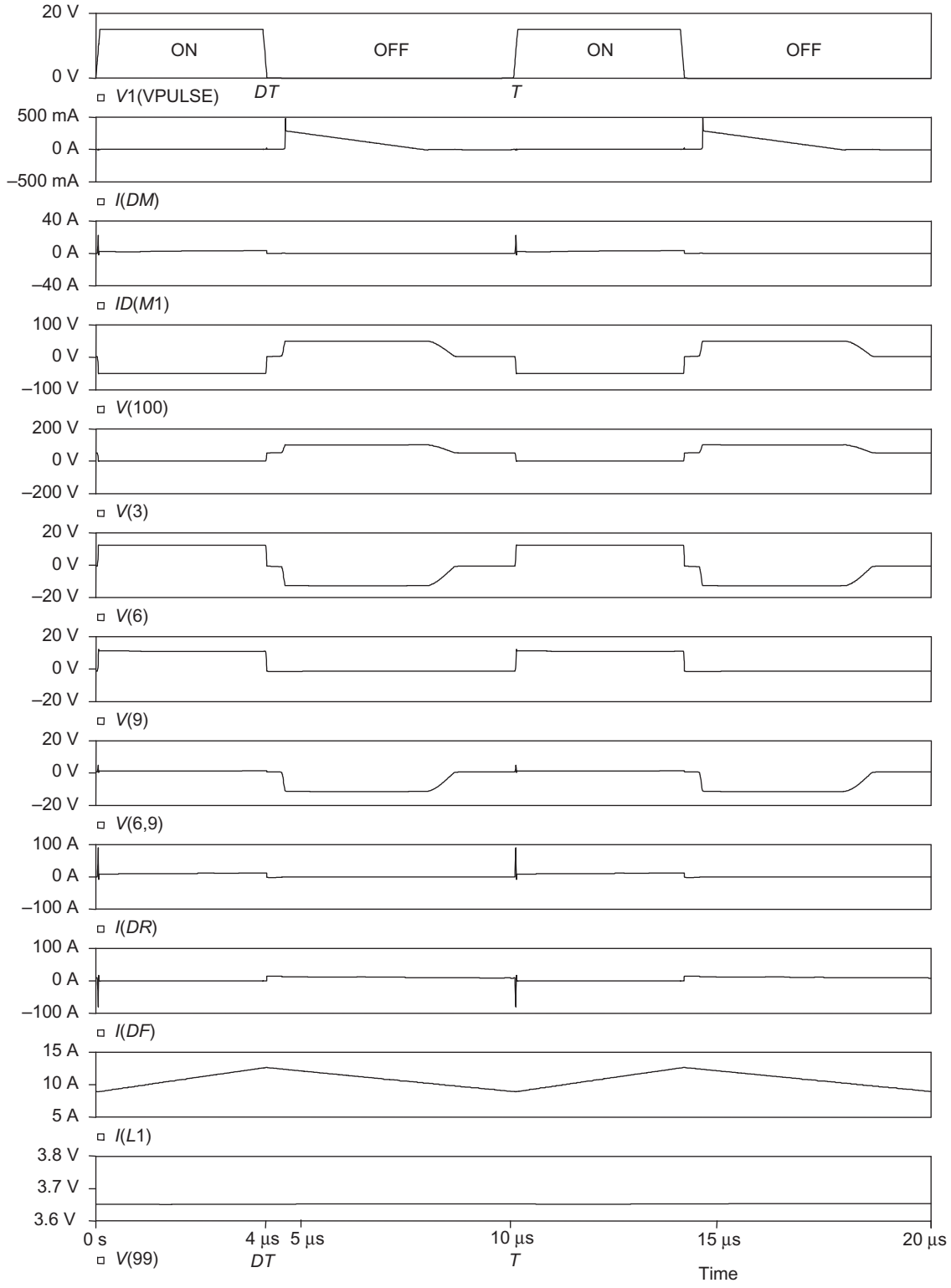


FIG. 7.30 Waveforms of forward converter using "ultrafast" diodes (which are actually much slower than Schottky diodes).

- D_M is an MUR460 ultrafast diode. D_R and D_F are MUR1560 ultrafast diodes.
- M_1 is an IRF640 MOS transistor.
- Transformer T_1 has a coupling coefficient of 0.99999999 (which may be assumed to be 1).
- The switching operation of the converter has reached a steady state.

It is observed that a large spike appears in the current waveforms of diodes D_R and D_F (denoted as *I(DR)* and *I(DF)* in Fig. 7.30) whenever the MOS transistor M_1 is turned on. This is due to the relatively slow reverse recovery of the flywheel diode D_F. During the reverse recovery time, the positive voltage suddenly appearing across L_S (which is equal to $V_{IN}(N_S/N_P)$) drives a large transient current through D_R and D_F. This current spike results in large current stress and power dissipation in D_R, D_F, and M_1.

A method of reducing the current spikes is to use Schottky diodes as D_R and D_F, as described below.

7.6.1.3 Circuit Using Schottky Diodes

In order to reduce the current spikes caused by the slow reverse recovery of rectifiers, Schottky diodes are now used as D_R and D_F. The assumptions made here are (referring to the circuit shown in Fig. 7.28) the following:

- D_R and D_F are MBR2540 Schottky diodes.
- D_M is an MUR460 ultrafast diode.
- M_1 is an IRF640 MOS transistor.
- Transformer T_1 has a coupling coefficient of 0.99999999.
- The switching operation of the converter has reached a steady state.

The new simulated waveforms are given in Fig. 7.31. It is found that, by employing Schottky diodes as D_R and D_F, the amplitudes of the current spikes in *ID(M1)*, *I(DR)*, and *I(DF)* can be reduced to practically zero. This solves the slow-speed problem of ultrafast diodes.

7.6.1.4 Circuit With Practical Transformer

The simulation results given above in Figs. 7.29–7.31 (for the forward converter circuit shown in Fig. 7.28) are based on the assumption that transformer *T*1 has effectively no leakage inductance (with coupling coefficient $K = 0.99999999$). It is, however, found that when a practical transformer (having a slightly lower *K*) is used, severe ringings occur. Fig. 7.32 shows some simulation results to demonstrate this phenomenon, where the following assumptions are made:

- D_R and D_F are MBR2540 Schottky diodes. D_M is an MUR460 ultrafast diode.
- M_1 is an IRF640 MOS transistor.
- Transformer T_1 has a practical coupling coefficient of 0.996.
- The effective winding resistance of L_P is 0.1 Ω. The effective winding resistance of L_M is 0.4 Ω. The effective winding resistance of L_S is 0.01 Ω.
- The effective series resistance of the output filtering capacitor is 0.05 Ω.
- The switching operation of the converter has reached a steady state.

The resultant waveforms shown in Fig. 7.32 indicate that there are large voltage and current ringings in the circuit. These ringings are caused by the resonant circuits formed by the leakage inductance of the transformer and the parasitic capacitances of diodes and transistor.

A practical converter may therefore need snubber circuits to damp these ringings, as described below.

7.6.1.5 Circuit With Snubber Across The Transformer

In order to suppress the ringing voltage caused by the resonant circuit formed by transformer leakage inductance and the parasitic capacitance of the MOS switch, a snubber circuit, shown as R_1 and C_1 in Fig. 7.33, is now connected across the primary winding of transformer T_1. The new waveforms are shown in Fig. 7.34. Here, the drain-to-source voltage waveform of the MOS transistor, *V*(3), is found to be acceptable. However, there are still large ringing voltages across the output rectifiers (*V*(6,9) and *V*(9)).

In order to damp the ringing voltages across the output rectifiers, additional snubber circuits across the rectifiers may therefore also be required in a practical circuit, as described below.

7.6.1.6 Practical Circuit

Fig. 7.35 shows a practical forward converter with snubber circuits added also to rectifiers (R_2C_2 for D_R and R_3C_3 for D_F) to reduce the voltage ringing. Figs. 7.36 and 7.37 show the resultant voltage and current waveforms. Fig. 7.36 is for continuous-mode operation ($R_L = 0.35\Omega$), where *I(L1)* (current in L_1) is continuous. Fig. 7.37 is for discontinuous-mode operation ($R_L = 10\Omega$), where *I(L1)* becomes discontinuous due to an increased value of R_L. These waveforms are considered to be acceptable.

The design considerations of diode rectifier circuits in high-frequency converters will be discussed later in Section 7.6.3.

7.6.2 Flyback Rectifier Diode and Clamping Diode in a Flyback Converter

7.6.2.1 Ideal Circuit

Fig. 7.38 shows the basic circuit of a flyback converter. Due to its simple circuit, this type of converter is widely used in low-cost low-power applications. Discontinuous-mode operation (meaning that the magnetizing current in the transformer falls to zero before the end of each switching cycle) is often used because it offers the advantages of easy control and low diode reverse recovery loss. Fig. 7.39 shows the idealized steady-state waveforms for discontinuous-mode operation.

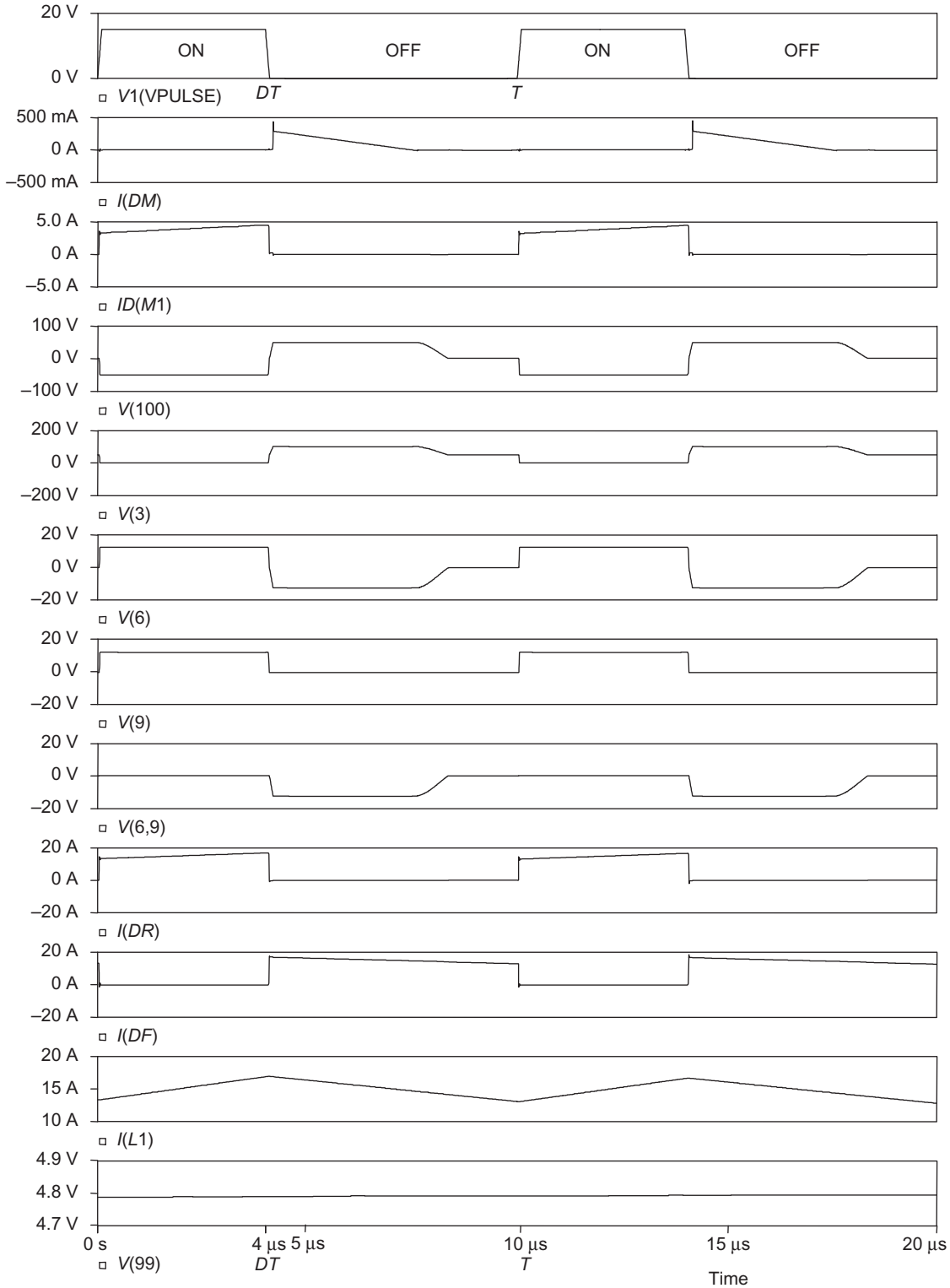


FIG. 7.31 Waveforms of forward converter using Schottky (fast-speed) diodes as output rectifiers.

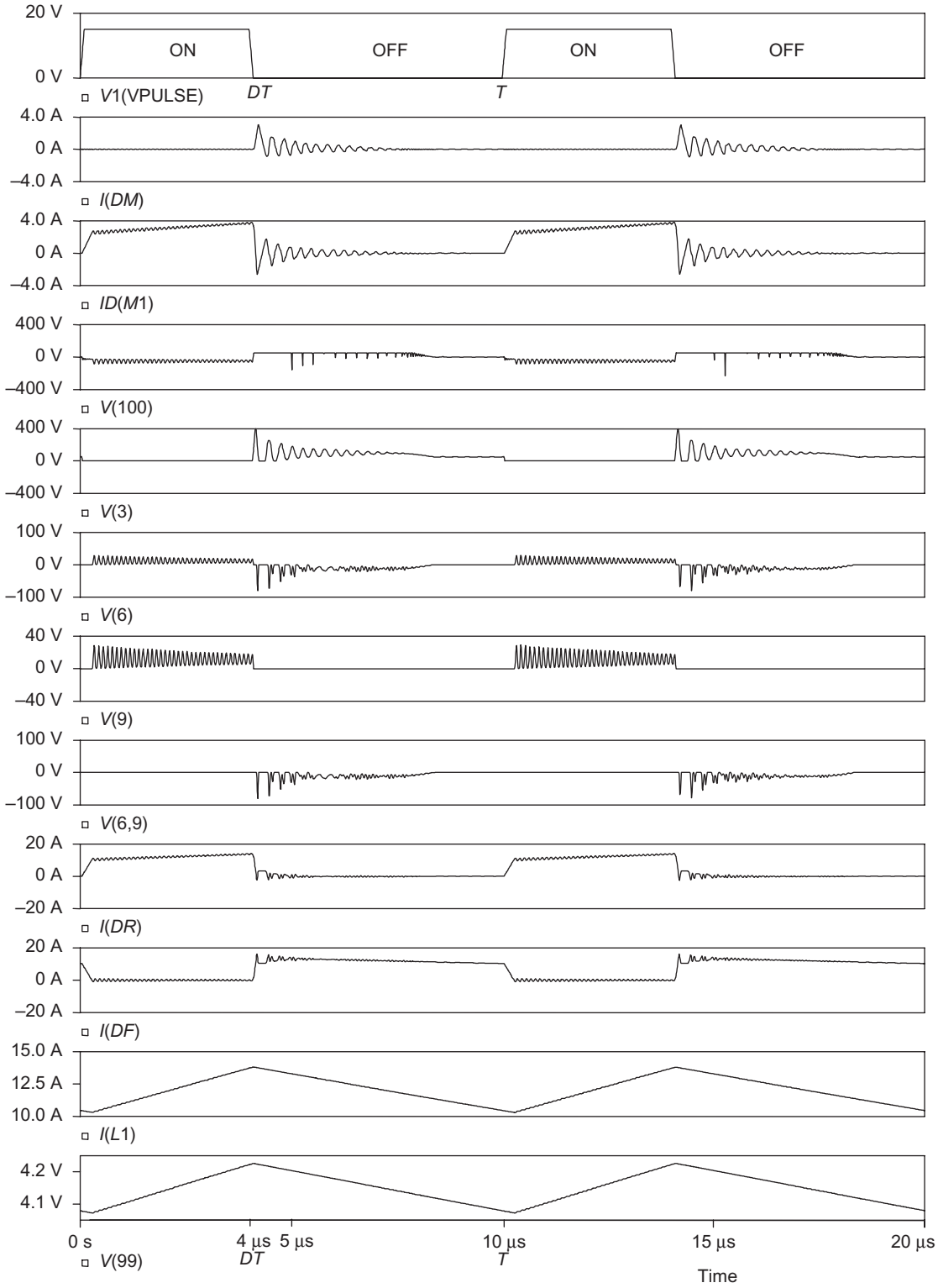
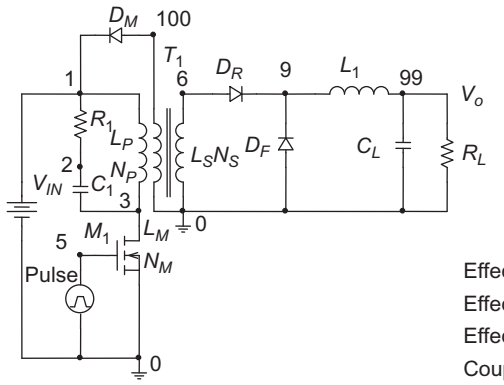


FIG. 7.32 Waveforms of forward converter with practical transformer and output filtering capacitor having nonzero series effective resistance.



V_{IN} = 50 V, D_M = MUR460
D_R = MBR2540, D_F = MBR2540
M_1 = IRF640, R_1 = 24 Ω
C_1 = 3000 pF, C_L = 3500 μF
ESR of C_L = 0.05 Ω, L_1 = 8 μH
L_P = 0.576 mH, L_M = 0.576 mH
L_S = 0.036 mH, $N_P : N_M : N_S$ = 4 : 4 : 1
R_L = 0.35 Ω
Effective winding resistance of L_P =0.1 Ω
Effective winding resistance of L_M =0.4 Ω
Effective winding resistance of L_S = 0.01 Ω
Coupling coefficient K = 0.996

FIG. 7.33 Forward converter with snubber circuit (R_1C_1) across transformer.

These waveforms are obtained from PSpice simulations, based on the following assumptions:

- D_R is an idealized rectifier diode with infinitely fast switching speed.
- M_1 is an idealized MOS switch with infinitely fast switching speed and

$$\text{On-stateresistance} = 0.067\ \Omega$$
$$\text{Off-stateresistance} = 1\ \text{M}\Omega$$

- Transformer T_1 has a coupling coefficient of 0.99999999.
- The switching operation of the converter has reached a steady state.

Referring to the circuit shown in Fig. 7.38 and the waveforms shown in Fig. 7.39, the operation of the converter can be explained as follows:

1. For $0 < t < DT$

   The switch M_1 is turned on at $t = 0$:

$$V(3) = 0 \quad \text{for } 0 < t < DT$$

   The current in M_1, denoted as $ID(M1)$, increases at the rate of

$$\frac{dID(M1)}{dt} = \frac{V_{IN}}{L_P} \tag{7.99}$$

   The output rectifier D_R is reversely biased.
2. For $DT < t < (D + D_2)T$

   The switching M_1 is turned off at $t = DT$.

   The collapse of magnetic flux induces a back emf in L_S to turn-on the output rectifier D_R. The initial amplitude of the rectifier current $I(DR)$, which is also denoted as $I(LS)$, can be found by equating the energy stored in the primary winding current $I(LP)$ just before $t = DT$ to the energy stored in the secondary winding current $I(LS)$ just after $t = DT$:

$$\frac{1}{2}L_P[I(LP)]^2 = \frac{1}{2}L_S[I(LS)]^2 \tag{7.100}$$

$$\frac{1}{2}L_P\left[\frac{V_{IN}}{L_P}DT\right]^2 = \frac{1}{2}L_S[I(LS)]^2 \tag{7.101}$$

$$I(LS) = \sqrt{\frac{L_P}{L_S}}\frac{V_{IN}}{L_P}DT \tag{7.102}$$

$$I(LS) = \frac{N_P}{N_S}\frac{V_{IN}}{L_P}DT \tag{7.103}$$

   The amplitude of $I(LS)$ falls at the rate of

$$\frac{dI(LS)}{dt} = \frac{-V_o}{L_S} \tag{7.104}$$

   and $I(LS)$ falls to zero at $t = (D + D_2)T$. Since $D_2V_o = V_{IN}(N_S/N_P)D$,

$$D_2 = \frac{V_{IN}}{V_o}\frac{N_S}{N_P}D \tag{7.105}$$

   D_2 is effectively the duty cycle of the output rectifier D_R.
3. For $(D + D_2)T < t < T$

   The output rectifier D_R is off.

   The output capacitor C_L provides the output current to the load R_L.

   The switching cycle restarts when the switch M_1 is turned on again at $t = T$.

From the waveforms shown in Fig. 7.39, the following information (for discontinuous-mode operation) can be obtained:

- The maximum value of the current in the switch M_1 is

$$ID(M1)_{max} = \frac{V_{IN}}{L_P}DT \tag{7.106}$$

- The maximum value of the current in the output rectifier D_R is

$$I(DR)_{max} = \frac{N_P}{N_S}\frac{V_{IN}}{L_P}DT \tag{7.107}$$

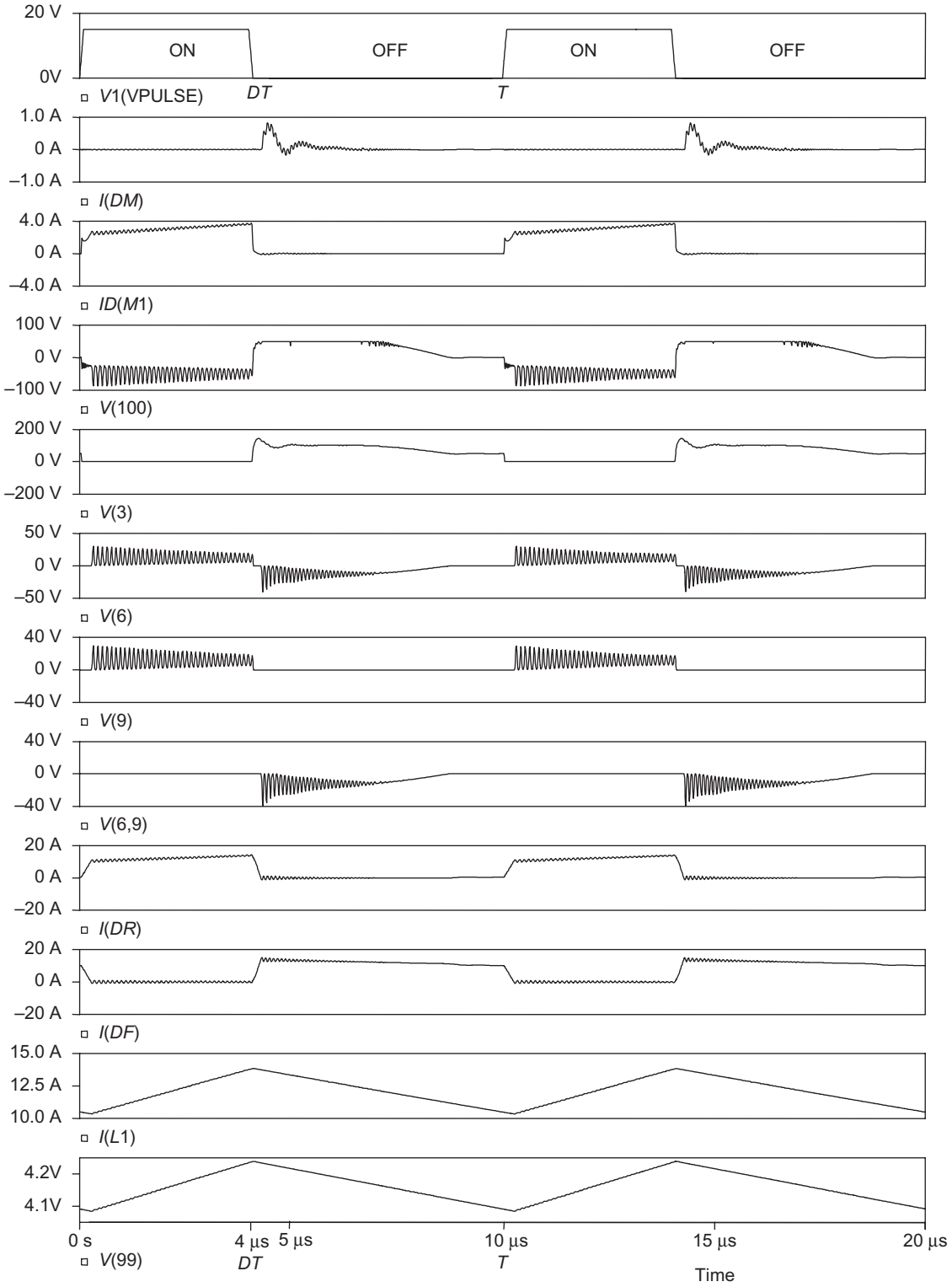


FIG. 7.34 Waveforms of forward converter with snubber circuit across the transformer.

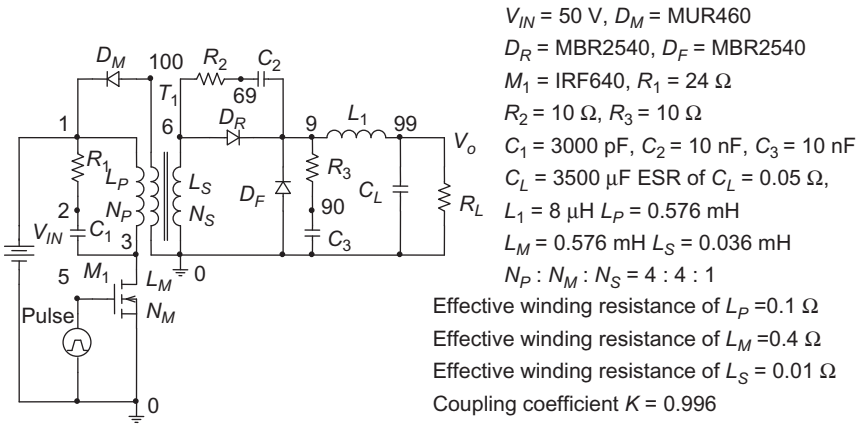


FIG. 7.35 Practical forward converter with snubber circuits across the transformer and rectifiers.

- The output voltage V_o can be found by equating the input energy to the output energy within a switching cycle.

$$V_{IN} \times [\text{Charge taken from } V_{IN} \text{ in a switching cycle}] = \frac{V_o^2}{R_L} T$$

$$V_{IN}\left[\frac{1}{2} DT \frac{DT}{L_P} V_{IN}\right] = \frac{V_o^2}{R_L} T \tag{7.108}$$

$$V_o = \sqrt{\frac{R_L T}{2L_P}} D V_{IN} \tag{7.109}$$

- The maximum reverse voltage of D_R, $V(6,9)$ (which is the voltage at node 6 with respect to node 9), is

$$V(DR)_{max} = V(6,9)_{max} = V_{IN} \frac{N_S}{N_P} + V_o \tag{7.110}$$

7.6.2.2 Practical Circuit

When a practical transformer (with leakage inductance) is used in the flyback converter circuit shown in Fig. 7.38, there will be large ringings. In order to reduce these ringings to practically acceptable levels, snubber and clamping circuits have to be added. Fig. 7.40 shows a practical flyback converter circuit where a resistor-capacitor snubber (R_2C_2) is used to damp the ringing voltage across the output rectifier D_R and a resistor-capacitor-diode clamping ($R_1C_1D_S$) is used to clamp the ringing voltage across the switch M_1. What the diode D_S does here is to allow the energy stored by the current in the leakage inductance to be converted to the form of a dc voltage across the clamping capacitor C_1. The energy transferred to C_1 is then dissipated slowly in the parallel resistor R_1, without ringing problems.

The simulated waveforms of the flyback converter (circuit given in Fig. 7.40) for discontinuous-mode operation are shown in Fig. 7.41, where the following assumptions are made:

- D_R and D_S are MUR460 ultrafast diodes.
- M_1 is an IRF640 MOS transistor.
- Transformer T_1 has a practical coupling coefficient of 0.992.
- The effective winding resistance of L_P is 0.025 Ω. The effective winding resistance of L_S is 0.1 Ω.
- The effective series resistance of the output filtering capacitor C_L is 0.05 Ω.
- The switching operation of the converter has reached a steady state.

The waveforms shown in Fig. 7.40 are considered to be acceptable.

7.6.3 Design Considerations

In the design of rectifier circuits, it is necessary for the designer to determine the voltage and current ratings of the diodes. The idealized waveforms and expressions for the maximum diode voltages and currents given under the heading of "Ideal Circuit" above (for both forward and flyback converters) are a good starting point. However, when parasitic/stray components are also considered, the simulation results given under "Practical Circuit" are much more useful for the determination of the voltage and current ratings of the high-frequency rectifier diodes.

Assuming that the voltage and current ratings have been determined, proper diodes can be selected to meet the requirements. The following are some general guidelines on the selection of diodes:

- For low-voltage applications, Schottky diodes should be used because they have very fast switching speed and low forward voltage drop. If Schottky diodes cannot be used, either because of their low reverse breakdown voltage or because of their large leakage current (when reversely biased), ultrafast diodes should be used.
- The reverse breakdown voltage rating of the diode should be reasonably higher (e.g., 10% or 20% higher) than the maximum reverse voltage, the diode is expected to encounter under the worst-case condition. However, an

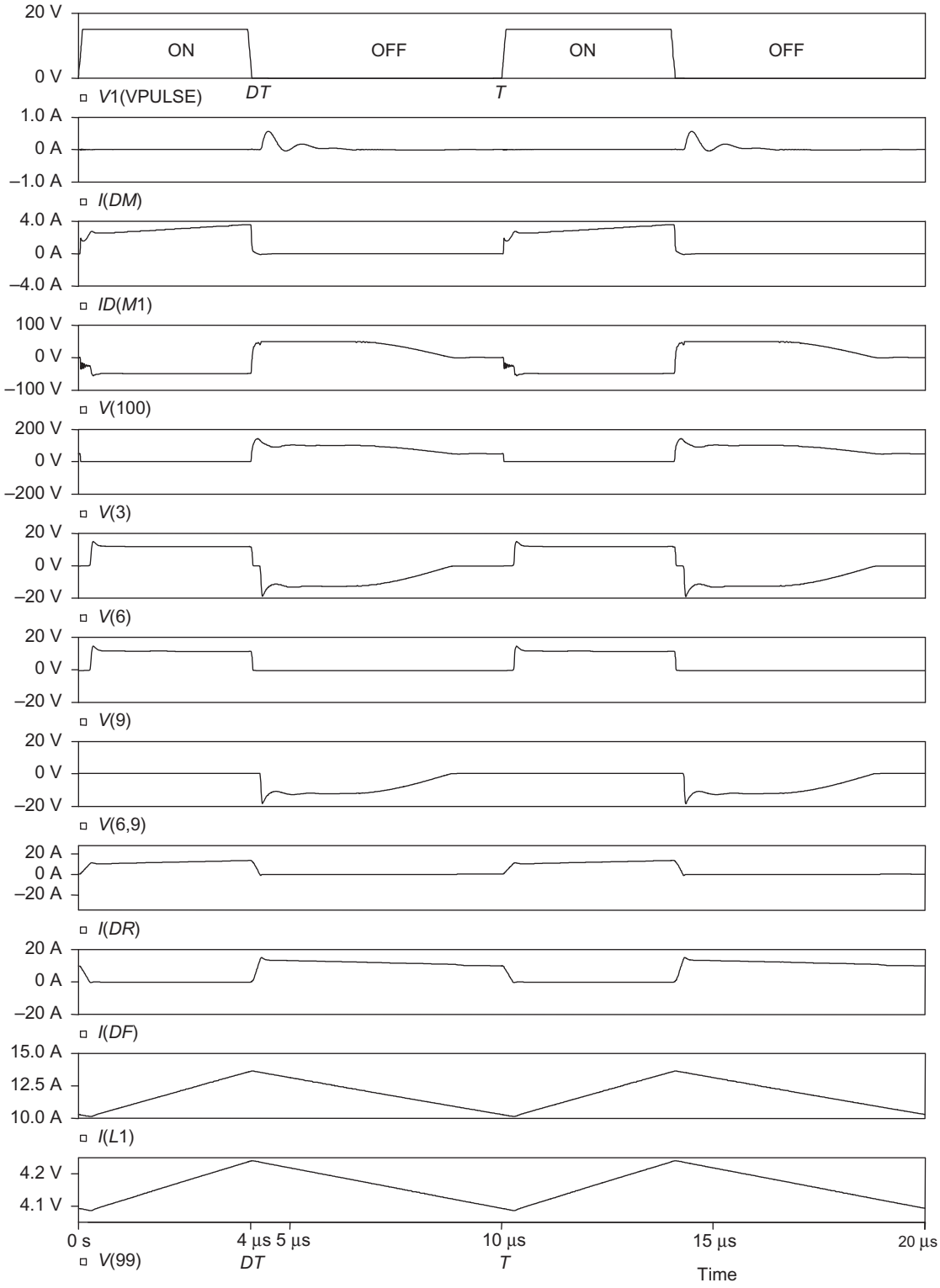


FIG. 7.36 Waveforms of practical forward converter for continuous-mode operation.

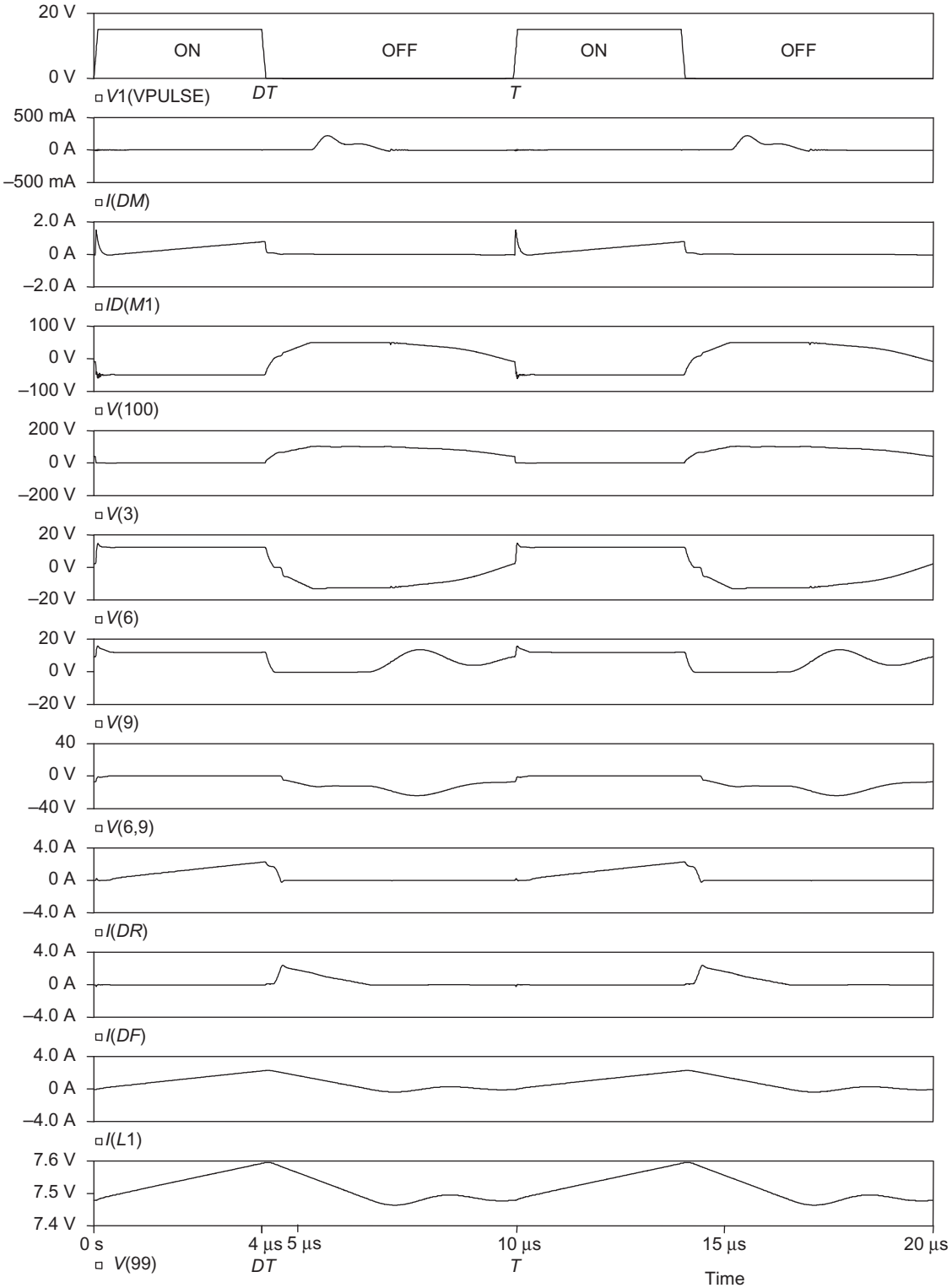


FIG. 7.37 Waveforms of practical forward converter for discontinuous-mode operation.

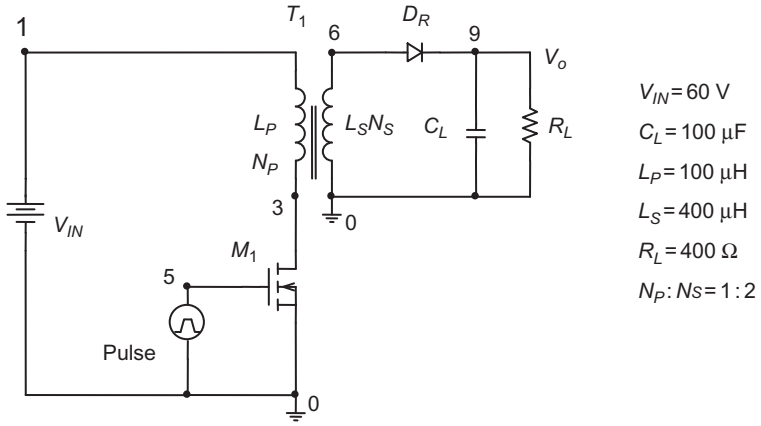


FIG. 7.38 Basic circuit of flyback converter.

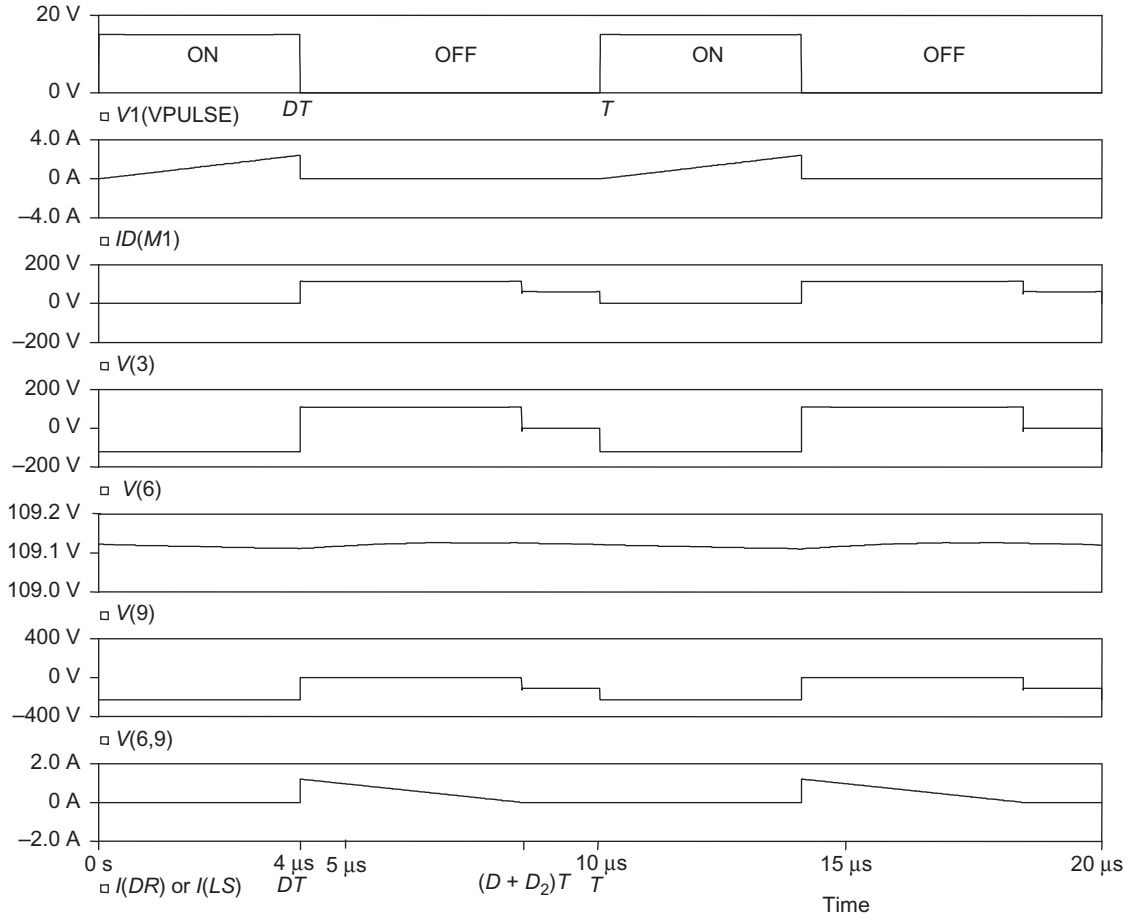


FIG. 7.39 Idealized steady-state waveforms of flyback converter for discontinuous-mode operation.

overly conservative design (using a diode with much higher breakdown voltage than necessary) would result in a lower rectifier efficiency, because a diode having a higher reverse voltage rating would normally have a larger voltage drop when it is conducting.

- The current rating of the diode should be substantially higher than the maximum current the diode is expected to carry during normal operation. Using a diode with a relatively large current rating has the following advantages:

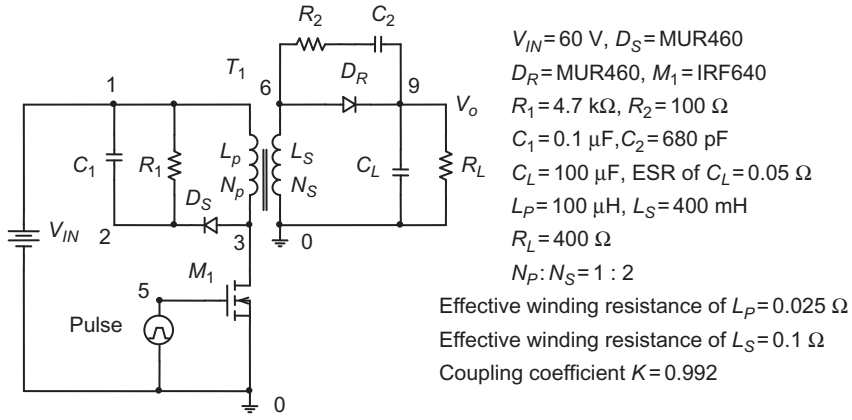


FIG. 7.40 Practical flyback converter circuit.

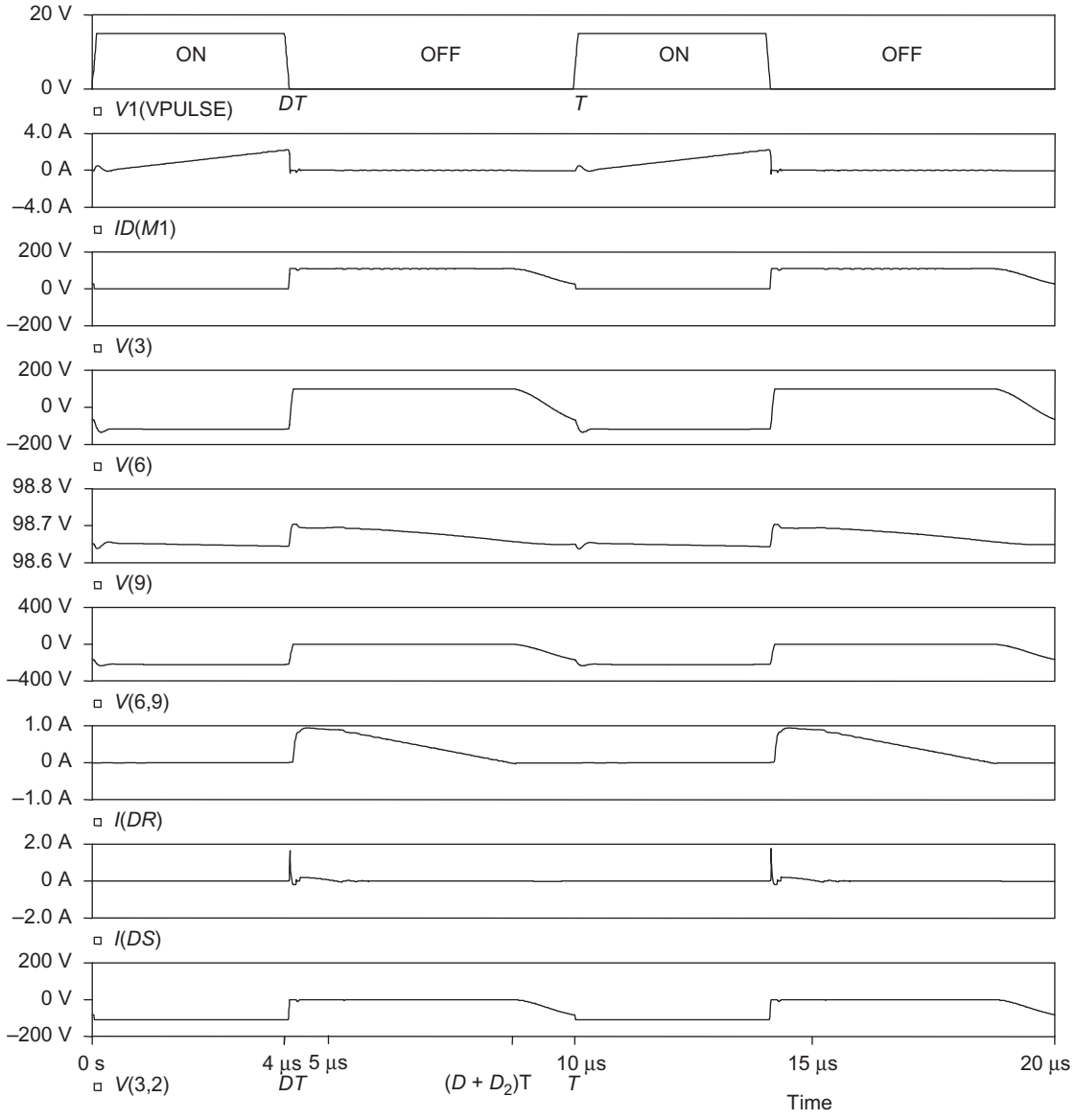


FIG. 7.41 Waveforms of practical flyback converter for discontinuous-mode operation.

- It reduces the possibility of damage due to transients caused by start-up, accidental short circuit, or random turning on and off of the converter.
- It reduces the forward voltage drop because the diode is operated in the lower current region of the *V-I* characteristic.

In some of the "high-efficiency" converter circuits, the current rating of the output rectifier can be many times larger than the actual current expected in the rectifier. In this way, a higher efficiency is achieved at the expense of a larger silicon area.

In the design of *R-C* snubber circuits for rectifiers, it should be understood that a larger *C* (and a smaller *R*) will give better damping. However, a large *C* (and a small *R*) will result in a large switching loss (which is equal to 0.5 CV^2f). As a guideline, a capacitor with five to ten times the junction capacitance of the rectifier may be used as a starting point for iterations. The value of the resistor should be chosen to provide a slightly underdamped operating condition.

7.6.4 Precautions in Interpreting Simulation Results

In using the simulated waveforms as references for design purposes, attention should be paid to the following:

- The voltage/current spikes that appear in the practically measured waveforms may not appear in the simulated waveforms. This is due to the lack of a model in the computer simulation to simulate unwanted coupling among the practical components.
- Most of the computer models of diodes, including those used in the simulations given above, do not take into account the effects of the forward recovery time. (The forward recovery time is not even mentioned in most manufacturers' data sheets.) However, it is also interesting to note that in most cases, the effect of the forward recovery time of a diode is masked by that of the effective inductance in series with the diode (e.g., the leakage inductance of a transformer).

Further Reading

[1] Rectifier Applications Handbook, third ed., Motorola, Inc, Phoenix, AZ, 1993.
[2] M.H. Rashid, Power Electronics: Circuits, Devices, and Applications, second ed., Prentice Hall, Inc., Englewood Cliffs, NJ, 1993
[3] Y.-S. Lee, Computer-Aided Analysis and Design of Switch-Mode Power Supplies, Marcel Dekker, Inc., New York, 1993
[4] J.W. Nilsson, Introduction to PSpice Manual, Electric Circuits Using OrCAD Release 9.1, fourth ed., Prentice Hall, Inc., Upper Saddle River, NJ, 2000
[5] J. Keown, OrCAD PSpice and Circuit Analysis, fourth ed., Prentice Hall, Inc., Upper Saddle River, NJ., 2001

8

Single-Phase Controlled Rectifiers

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8.1 Introduction

This chapter is dedicated to single-phase controlled rectifiers, which are used in a wide range of applications. As shown in Fig. 8.1, single-phase rectifiers can be classified into two big categories:

(i) Topologies working with low switching frequency, also known as line-commutated or phase controlled rectifiers
(ii) Circuits working with high switching frequency, also known as power factor correctors (PFCs), synchronous rectifiers

Line-commutated rectifiers with diodes, covered in a previous chapter of this handbook, do not allow the control of power being converted from ac to dc. This control can be achieved with the use of thyristors. These controlled rectifiers are addressed in the first part of this chapter.

In the last years, increasing attention has been paid to the control of current harmonics present at the input side of the rectifiers, originating from a very important development in the so-called PFCs and synchronous rectifiers. These circuits use power transistors working with high switching frequency to improve the waveform quality of the input current, increasing the power factor. High-power-factor rectifiers can be classified in regenerative and nonregenerative topologies. The synchronous rectification (SR) uses MOSFETs to achieve the rectification function typically performed by diodes. SR improves efficiency, thermal performance, power density, manufacturability, and reliability and decreases the overall system cost of power supply systems. New topology of control rectifier using the single-phase matrix converter is also covered in the second part of this chapter.

8.2 Line-Commutated Single-Phase Controlled Rectifiers

8.2.1 Single-Phase Half-Wave Rectifier

The single-phase half-wave rectifier uses a single thyristor to control the load voltage as shown in Fig. 8.2. The thyristor will conduct, on-state, when the voltage v_T is positive and a firing current pulse i_G is applied to the gate terminal. The control of the load voltage is performed by delaying the firing pulse by an angle α. The firing angle α is measured from the position where a diode would naturally conduct. In case of Fig. 8.2, the angle α is measured from the zero-crossing point of the supply voltage v_s. The load in Fig. 8.2 is resistive, and therefore, the current i_d has the same waveform of the load voltage. The thyristor goes to the nonconducting condition, off-state, when the load voltage and consequently the current reach a negative value.

The load average voltage is given by [1]

$$V_{d\alpha} = \frac{1}{2\pi}\int_{\alpha}^{\pi} V_{max}\sin(\omega t)d(\omega t) = \frac{V_{max}}{2\pi}(1+\cos\alpha) \qquad (8.1)$$

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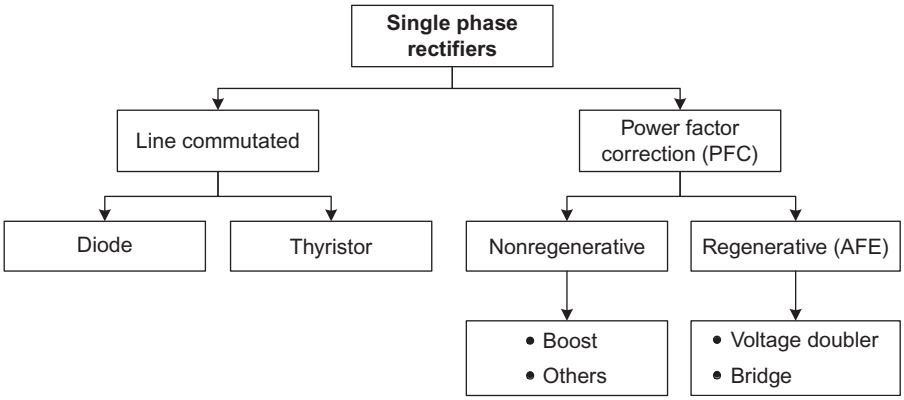


FIG. 8.1 Single-phase rectifier classification.

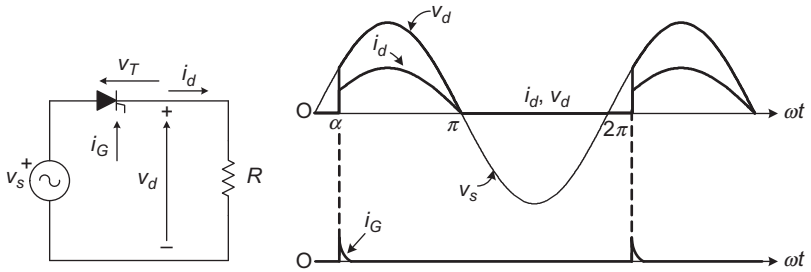


FIG. 8.2 Single-thyristor rectifier with resistive load.

where V_{max} is the supply peak voltage. Hence, it can be seen from Eq. (8.1) that changing the firing angle α controls both the load average voltage and the amount of transferred power.

Fig. 8.3A shows the rectifier waveforms for an *R-L* load. When the thyristor is turned on, the voltage across the inductance is

$$v_L = v_s - v_R = L\frac{di_d}{dt} \tag{8.2}$$

where v_R is the voltage in the resistance *R*, given by $v_R = R \cdot i_d$. If $v_s - v_R > 0$, from Eq. (8.2) holds that the load current increases its value. On the other hand, i_d decreases its value when $v_s - v_R < 0$. The load current is given by

$$i_d(\omega t) = \frac{1}{\omega L}\int_{\alpha}^{\omega t} v_L d\theta \tag{8.3}$$

Graphically, Eq. (8.3) means that the load current i_d is equal to zero when $A_1 = A_2$, maintaining the thyristor in conduction state even when $v_s < 0$.

When an inductive-active load is connected to the rectifier, as illustrated in Fig. 8.3B, the thyristor will be turned on if the firing pulse is applied to the gate when $v_s > E_d$. Again, the thyristor will remain in the on-state until $A_1 = A_2$. When the thyristor is turned off, the load voltage will be $v_d = E_d$.

8.2.2 Bi-Phase Half-Wave Rectifier

The biphase half-wave rectifier, shown in Fig. 8.4, uses a center-tapped transformer to provide two voltages v_1 and v_2. These two voltages are 180 degrees out of phase with respect to the midpoint neutral *N*. In this scheme, the load is fed via thyristors T_1 and T_2 during each positive cycle of voltages v_1 and v_2, respectively, while the load current returns via the neutral *N*.

As illustrated in Fig. 8.4, thyristor T_1 can be fired into the on-state at any time, while voltage $v_{T_1} > 0$. The firing pulses are delayed by an angle α with respect to the instant where diodes would conduct. Also the current paths for each conduction state are presented in Fig. 8.4. Thyristor T_1 remains in the on-state until the load current tends to a negative value. Thyristor T_2 is fired into the on-state when $v_{T_2} > 0$, which corresponds in Fig. 8.4 to the condition when $v_2 > 0$.

The mean value of the load voltage with resistive load is determined by

$$V_{di\alpha} = \frac{1}{\pi}\int_{\alpha}^{\pi} V_{max}\sin(\omega t)d(\omega t) = \frac{V_{max}}{\pi}(1+\cos\alpha) \tag{8.4}$$

The ac supply current is equal to $i_{T_1}\left(N^2/N^1\right)$ when T_1 is in the on-state and $-i_{T_2}\left(N^2/N^1\right)$ when T_2 is in the on-state, where N_2/N_1 is the transformer turns ratio.

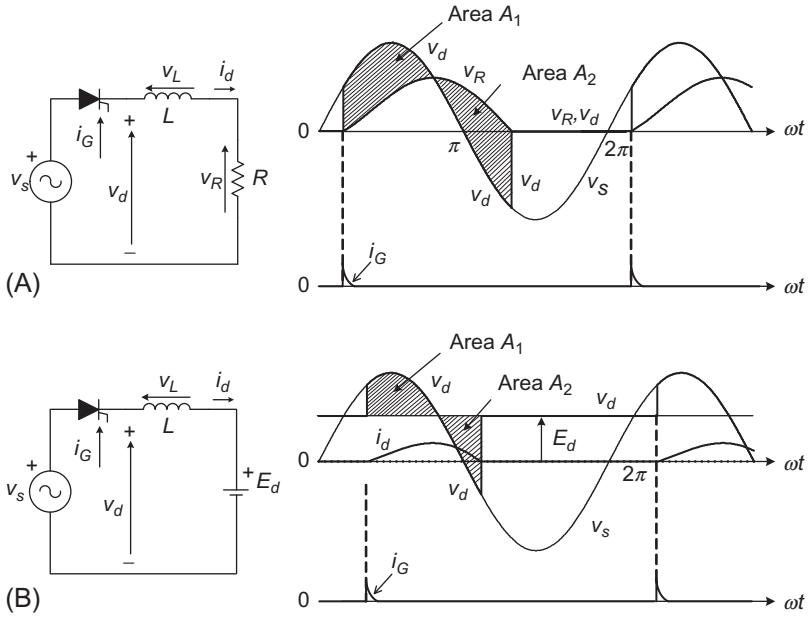


FIG. 8.3 Single-thyristor rectifier with (A) resistive-inductive load and (B) active load.

The effect of the load time constant $T_L = L/R$ on the normalized load current $i_d(t)/\hat{i}_R(t)$ for a firing angle $\alpha = 0$ degrees is shown in Fig. 8.5. The ripple in the load current reduces as the load inductance increases. If the load inductance $L \to \infty$, then the current is perfectly filtered.

8.2.3 Single-Phase Bridge Rectifier

Fig. 8.6A shows a fully controlled bridge rectifier, which uses four thyristors to control the average load voltage. In addition, Fig. 8.6B shows the half-controlled bridge rectifier that uses two thyristors and two diodes.

The voltage and current waveforms of the fully controlled bridge rectifier for a resistive load are illustrated in Fig. 8.7. Thyristors T_1 and T_2 must be fired on simultaneously during the positive half wave of the source voltage v_s, to allow the conduction of current. Alternatively, thyristors T_3 and T_4 must be fired simultaneously during the negative half wave of the source voltage. To ensure simultaneous firing, thyristors T_1 and T_2 use the same firing signal. The load voltage is similar to the voltage obtained with the biphase half-wave rectifier. The input current is given by

$$i_S = i_{T_1} - i_{T_4} \tag{8.5}$$

and its waveform is shown in Fig. 8.7.

Fig. 8.8 presents the behavior of the fully controlled rectifier with resistive-inductive load (with $L \to \infty$) [2] . The high load inductance generates a perfectly filtered current, and the rectifier behaves like a current source. With continuous load current, thyristors T_1 and T_2 remain in the on-state beyond the positive half wave of the source voltage v_s. For this reason, the load voltage v_d can have a negative instantaneous value. The firing of thyristors T_3 and T_4 has two effects:

(i) They turn off thyristors T_1 and T_2.
(ii) After the commutation, they conduct the load current.

This is the main reason why this type of converters is called "naturally commutated" or "line-commutated" rectifiers. The supply current i_S has the square waveform, as shown in Fig. 8.9, for continuous conduction. In this case, the average load voltage is given by

$$V_{di\alpha} = \frac{1}{\pi}\int_{\alpha}^{\pi+\alpha} V_{max}\sin(\omega t)d(\omega t) = \frac{2V_{max}}{\pi}\cos\alpha \tag{8.6}$$

8.2.4 Analysis of the Input Current

Considering a very high inductive load, the input current in a bridge-controlled rectifier is filtered and presents a square waveform. In addition, the input current i_s is shifted by the firing angle α with respect to the input voltage v_s, as shown in Fig. 8.9A. The input current can be expressed as a Fourier series, where the amplitude of the different harmonics is

$$I_{smax,\,n} = \frac{4I_d}{\pi n} \quad (n = 1,3,5,\ldots) \tag{8.7}$$

where n is the harmonic order. The root mean square (rms) value of each harmonic can be expressed as

$$I_{sn} = \frac{I_{smax,\,n}}{\sqrt{2}} = \frac{2\sqrt{2}I_d}{\pi\, n} \tag{8.8}$$

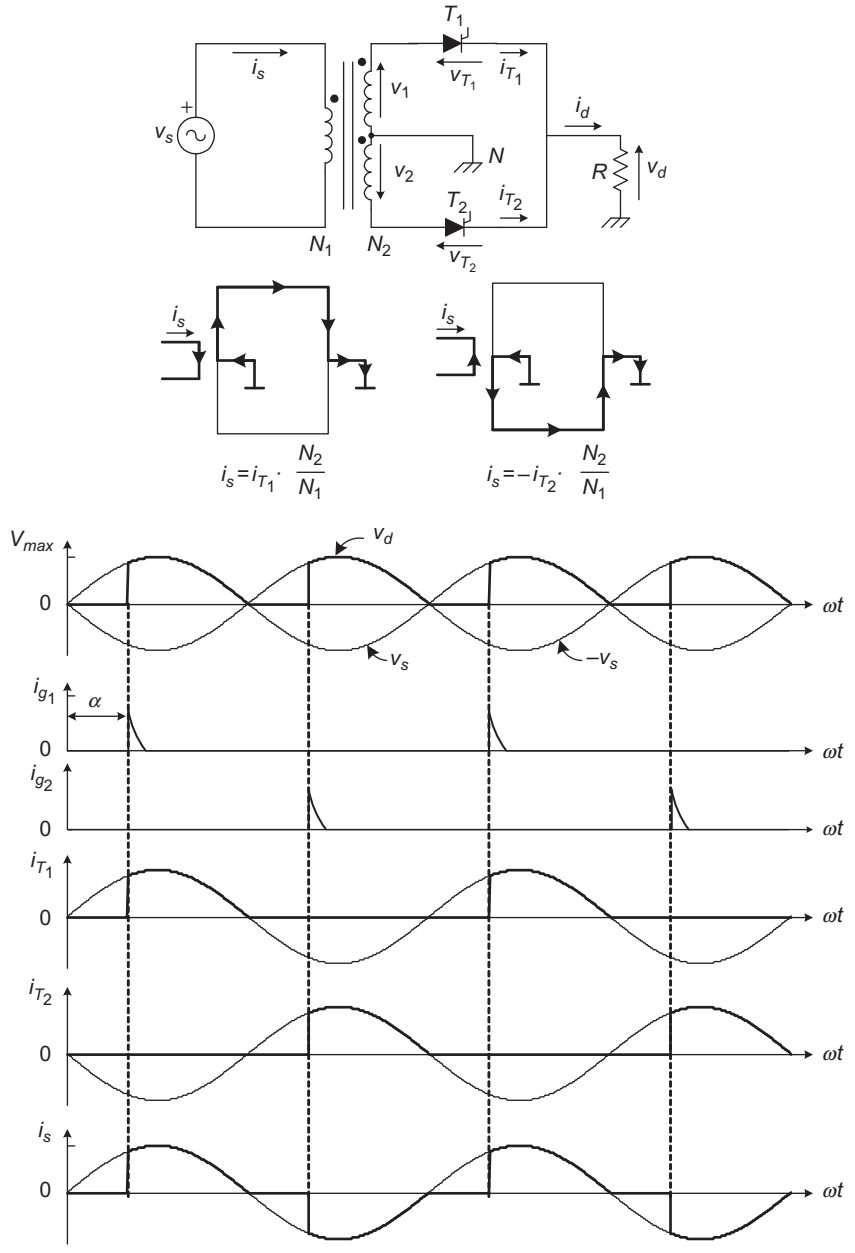


FIG. 8.4 Biphase half-wave rectifier.

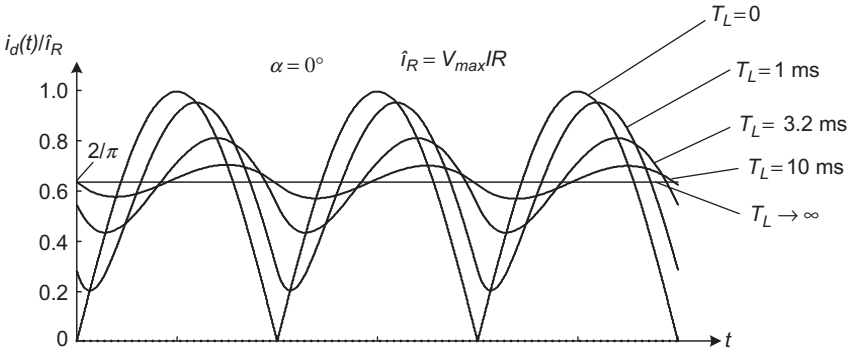


FIG. 8.5 Effect of the load time constant over the current ripple.

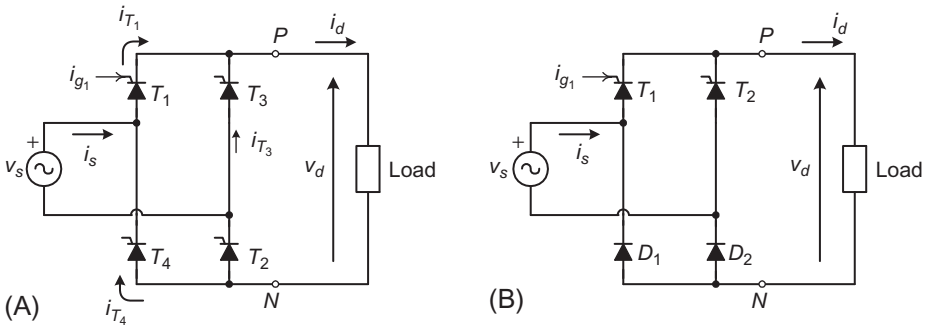


FIG. 8.6 Single-phase bridge rectifier, (A) fully controlled and (B) half-controlled.

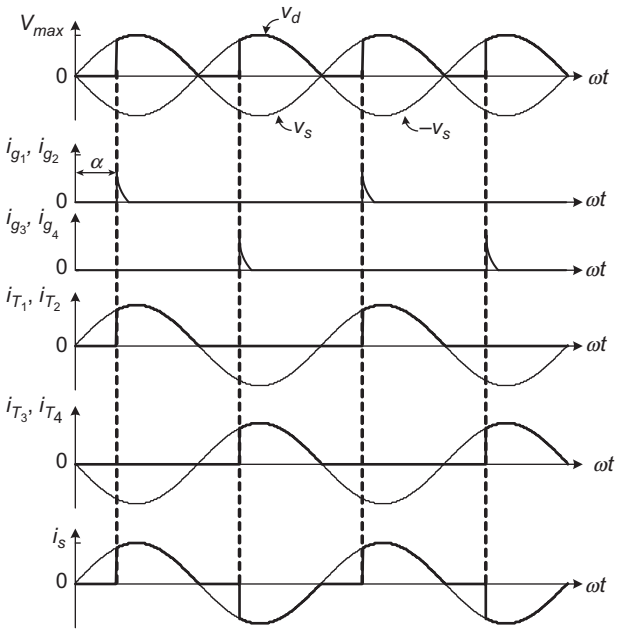


FIG. 8.7 Waveforms of a fully controlled bridge rectifier with resistive load.

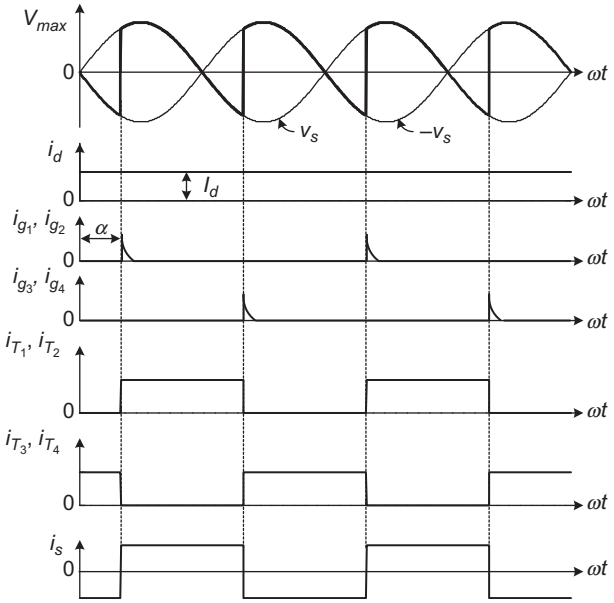


FIG. 8.8 Waveforms of a fully controlled bridge rectifier with resistive-inductive load ($L \rightarrow \infty$).

Thus, the rms value of the fundamental current i_{s1} is

$$I_{s1} = \frac{2\sqrt{2}}{\pi} I_d = 0.9 I_d \tag{8.9}$$

It can be observed from Fig. 8.9A that the displacement angle ϕ_1 of the fundamental current i_{s1} corresponds to the firing angle α. Fig. 8.9B shows that in the harmonic spectrum of the input current, only odd harmonics are present with decreasing amplitude while the frequency increases. Finally, the rms value of the input current i_s is

$$I_s = I_d \tag{8.10}$$

The total harmonic distortion (THD) of the input current can be determined by [3]

$$\text{THD} = \frac{\sqrt{I_s^2 - I_{s1}^2}}{I_{s1}} 100 = 48.4\% \tag{8.11}$$

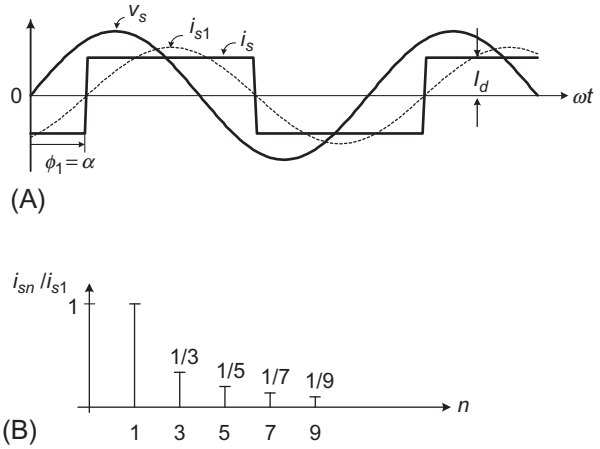


FIG. 8.9 Input current of the single-phase controlled rectifier in bridge connection, (A) waveforms and (B) harmonics spectrum.

8.2.5 Power Factor of the Rectifier

The displacement factor of the fundamental current, obtained from Fig. 8.9A, is

$$\cos\phi_1 = \cos\alpha \tag{8.12}$$

In the case of nonsinusoidal currents, the active power delivered by the sinusoidal single-phase supply is

$$P = \frac{1}{T}\int_0^T v_s(t) i_s(t) dt = V_s I_{s1} \cos\phi_1 \tag{8.13}$$

where V_s is the rms value of the single-phase voltage v_s.

The apparent power is given by

$$S = V_s I_s \tag{8.14}$$

The power factor (PF) is defined by

$$\text{PF} = \frac{P}{S} \tag{8.15}$$

Substitution from Eqs. (8.12), (8.13), and (8.14) in Eq. (8.15) yields

$$\text{PF} = \frac{I_{s1}}{I_s}\cos\alpha \tag{8.16}$$

This equation shows clearly that due to the nonsinusoidal waveform of the input current, the power factor of the rectifier is negatively affected both by the firing angle α and by the distortion of the input current. In effect, an increase in the distortion of the current produces an increase in the value of I_s in Eq. (8.16), which deteriorates the power factor.

8.2.6 The Commutation of the Thyristors

Until now, the current commutation between thyristors has been considered to be instantaneous. This condition is not valid in real cases due to the presence of the line inductance L, as shown in Fig. 8.10A. During the commutation, the current through the thyristors cannot change instantaneously, and for this reason, during the commutation angle μ, all four thyristors are conducting simultaneously. Therefore, during the commutation, the following relationship for the load voltage holds

$$v_d = 0 \quad \alpha \le \omega t \le \alpha + \mu \tag{8.17}$$

The effect of the commutation on the supply current, the voltage waveforms, and the thyristor current waveforms can be observed in Fig. 8.10B.

During the commutation, the following expression holds

$$L\frac{di_s}{dt} = v_s = V_{max}\sin(\omega t) \quad \alpha \le \omega t \le \alpha + \mu \tag{8.18}$$

Integrating Eq. (8.18) over the commutation interval yields

$$\int_{-I_d}^{I_d} di_s = \frac{V_{max}}{L}\int_{\alpha/\omega}^{\alpha+\mu/\omega} \sin(\omega t) dt \tag{8.19}$$

From Eq. (8.19), the following relationship for the commutation angle μ is obtained:

$$\cos(\alpha+\mu) = \cos\alpha - \frac{2\omega L}{V_{max}} I_d \tag{8.20}$$

Eq. (8.20) shows that an increase of the line inductance L or an increase of the load current I_d increases the commutation angle μ. In addition, the commutation angle is affected by the firing angle α. In effect, Eq. (8.18) shows that with different values of α, the supply voltage v_s has a different instantaneous value, which produces different di_s/dt, thereby affecting the duration of the commutation.

Eq. (8.17) and the waveform of Fig. 8.10B show that the commutation process reduces the average load voltage $V_{d\alpha}$. When the commutation is considered, the expression for the average load voltage is given by

$$V_{d\alpha} = \frac{1}{\pi}\int_{\alpha+\mu}^{\pi+\alpha} \sin(\omega t) d(\omega t) = \frac{V_{max}}{\pi}[\cos(\alpha+\mu) + \cos\alpha] \tag{8.21}$$

Substituting Eq. (8.20) into Eq. (8.21) yields

$$V_{d\alpha} = \frac{2}{\pi}V_{max}\cos\alpha - \frac{2\omega L}{\pi} I_d \tag{8.22}$$

8.2.7 Operation in the Inverting Mode

When the angle $\alpha > 90$ degrees, it is possible to obtain a negative average load voltage. In this condition, the power is fed back to the single-phase supply from the load. This operating mode is called inverter or inverting mode, because the energy is transferred from the dc to the ac side. In practical cases, this operating mode is obtained when the load configuration is as shown in Fig. 8.11A. It must be noticed that this rectifier allows unidirectional load current flow. Fig. 8.11B shows the waveform of the load voltage with the rectifier in the inverting mode, neglecting the source inductance L.

Section 8.2.6 described how supply inductance increases the conduction interval of the thyristors by the angle μ. As shown in Fig. 8.11C, the thyristor voltage v_{T_1} has a negative value during the extinction angle γ, defined by

$$\gamma = 180 - (\alpha + \mu) \tag{8.23}$$

To ensure that the outgoing thyristor will recover its blocking capability after the commutation, the extinction angle should satisfy the following restriction:

$$\gamma > \omega t_q \tag{8.24}$$

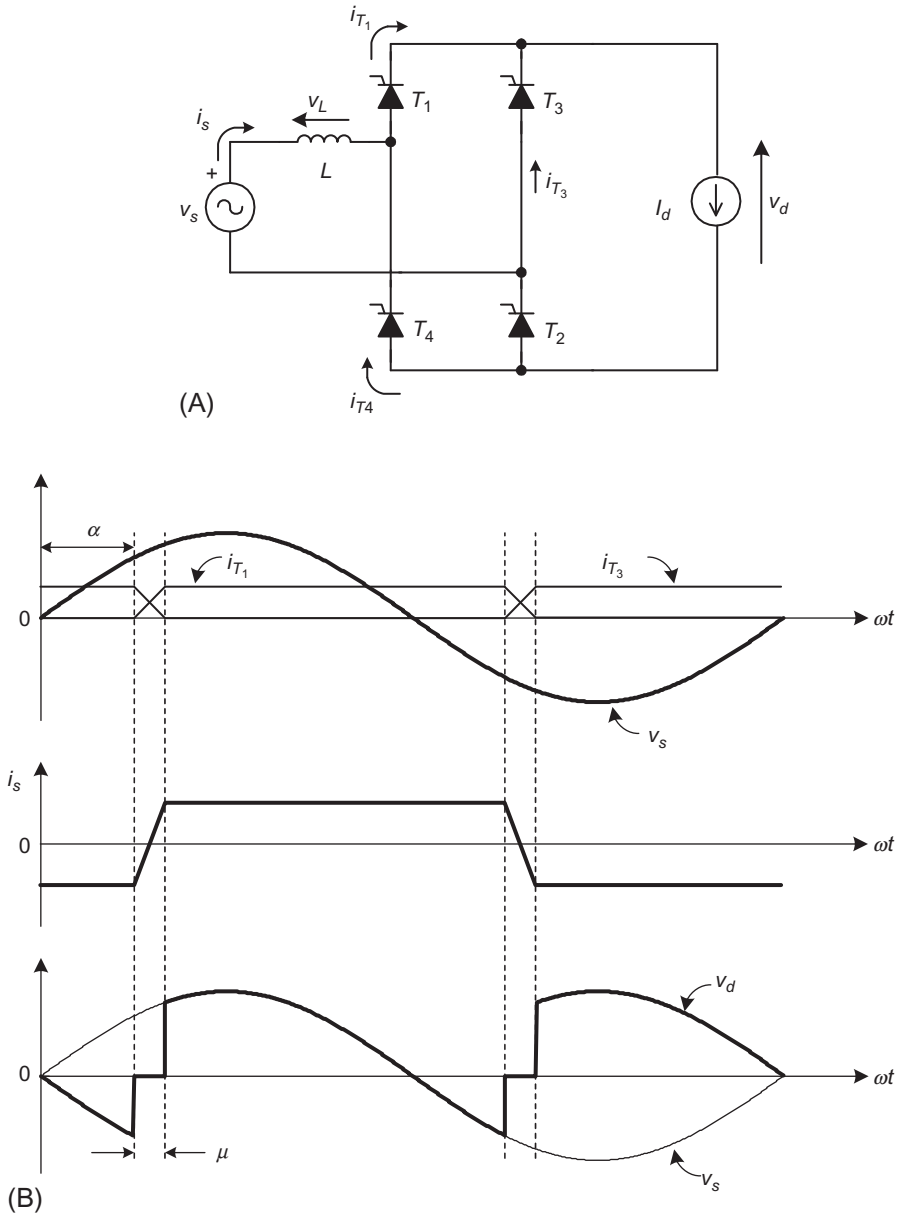


FIG. 8.10 The commutation process, (A) circuit and (B) waveforms.

where ω is the supply frequency and t_q is the thyristor turn-off time. Considering Eqs. (8.23) and (8.24), the maximum firing angle is, in practice,

$$\alpha_{max} = 180 - \mu - \gamma \tag{8.25}$$

If the condition of Eq. (8.25) is not satisfied, the commutation process will fail, originating destructive currents.

8.2.8 Applications

Important application areas of controlled rectifiers include uninterruptible power supplies (UPS), for feeding critical loads. Fig. 8.12 shows a simplified diagram of a single-phase UPS configuration, typically rated for <10 kVA. A fully controlled or half-controlled rectifier is used to generate the dc voltage for the inverter. In addition, the input rectifier acts as a battery charger. The output of the inverter is filtered before it is fed to the load. The operating modes of UPS are best explained in Ref. [4]. The control of low-power dc motors is another interesting application of controlled single-phase rectifiers. In the circuit of Fig. 8.13, the controlled rectifier regulates the armature voltage and consequently controls the motor current i_d in order to produce a required torque.

This configuration allows only positive current flow in the load. However, the load voltage can be both positive and

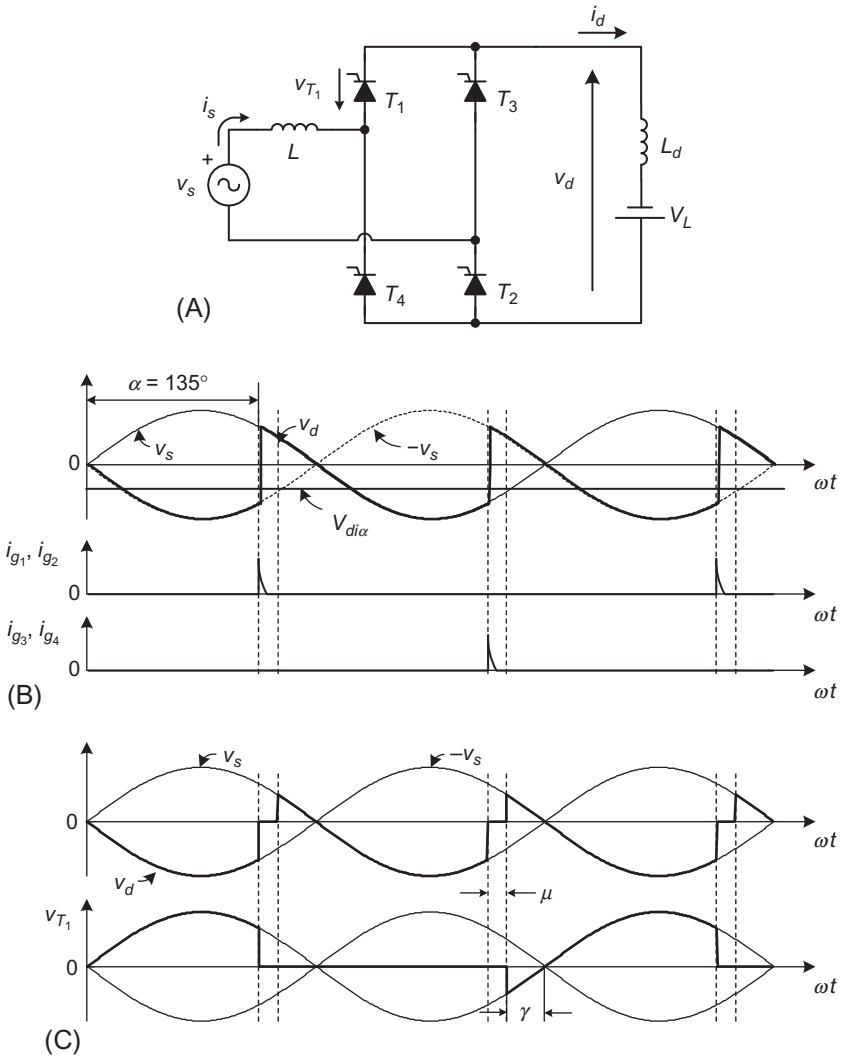


FIG. 8.11 Rectifier in the inverting mode: (A) circuit, (B) waveforms neglecting source inductance L, and (C) waveforms considering L.

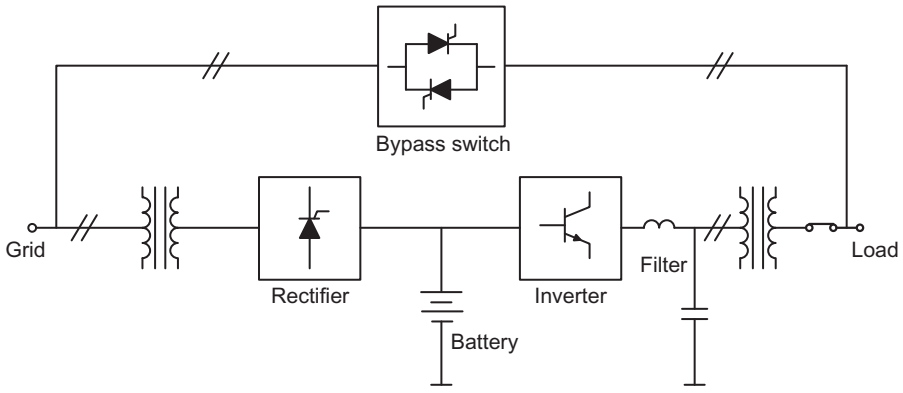


FIG. 8.12 Application of a rectifier in single-phase UPS.

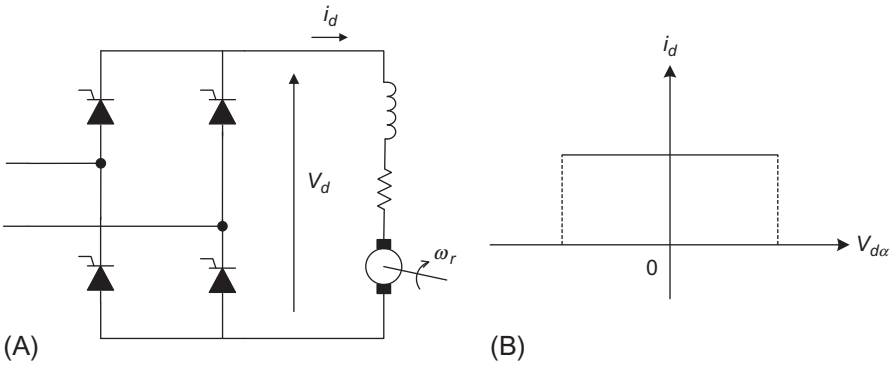


FIG. 8.13 Two-quadrant dc drive, (A) circuit and (B) quadrants of operation.

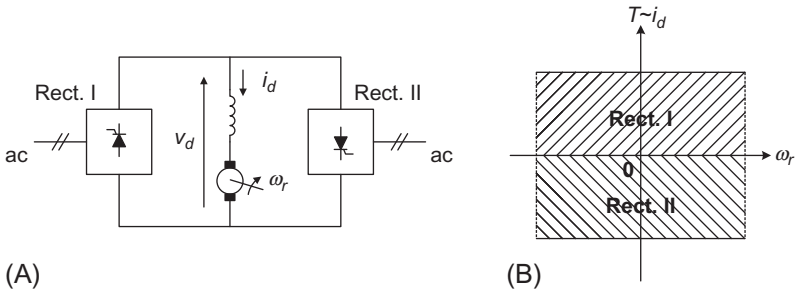


FIG. 8.14 Single-phase dual-converter drive, (A) connection and (B) four-quadrant operation.

negative. For this reason, this converter works in the two-quadrant mode of operation in the plane i_d vs $V_{d\alpha}$.

A better performance can be obtained with two rectifiers in back-to-back connection at the dc terminals, as shown in Fig. 8.14A. This arrangement, known as a dual-converter configuration, allows four-quadrant operation of the drive. Rectifier I provides positive load current i_d, while rectifier II provides negative load current. The motor can work in forward powering, forward braking (regenerating), reverse powering, and reverse braking (regenerating). These operating modes are shown in Fig. 8.14B, where the torque T vs the rotor speed ω_r is illustrated.

8.3 Unity Power Factor Single-Phase Rectifiers

8.3.1 The Problem of Power Factor in Single-Phase Line-Commutated Rectifiers

The main disadvantages of the classical line-commutated rectifiers are that (i) they produce a lagging displacement factor with respect to the voltage of the utility and (ii) they generate an important amount of input current harmonics. These aspects have a negative influence on both power factor and power quality. In the last several years, the massive use of single-phase power converters has increased the problems of power quality in electric systems. In effect, modern commercial buildings have 50% and even up to 90% of the demand, originated by nonlinear loads, which are composed mainly of rectifiers [5,6]. Today, it is not unusual to find rectifiers with total harmonic distortion of the current $\text{THD}_i > 40\%$, originating severe overloads in conductors and transformers.

Fig. 8.15A shows a single-phase rectifier with a capacitive filter, used in much of today's low-power equipment. The input current produced by this rectifier is illustrated in Fig. 8.15B; it appears highly distorted due to the presence of the filter capacitor. This current has a harmonic content shown in Fig. 8.16 and Table 8.1, with a $\text{THD}_i = 197\%$.

The rectifier in Fig. 8.15 has a very low power factor of $\text{PF} = 0.45$, due mainly to its large harmonic content.

8.3.2 Standards for Harmonics in Single-Phase Rectifiers

The relevance of the problems originated by harmonics in single-phase line-commutated rectifiers has motivated some agencies to introduce restrictions to these converters. The IEC 61000-3-2 [7], Class D International Standard, establishes limits to all low-power single-phase equipment having an input current with a "special wave shape" and an active input power $P \leq 600$ W. Class D equipment has an input current with a special wave shape contained within the envelope given in Fig. 8.15B. This class of equipment must satisfy certain

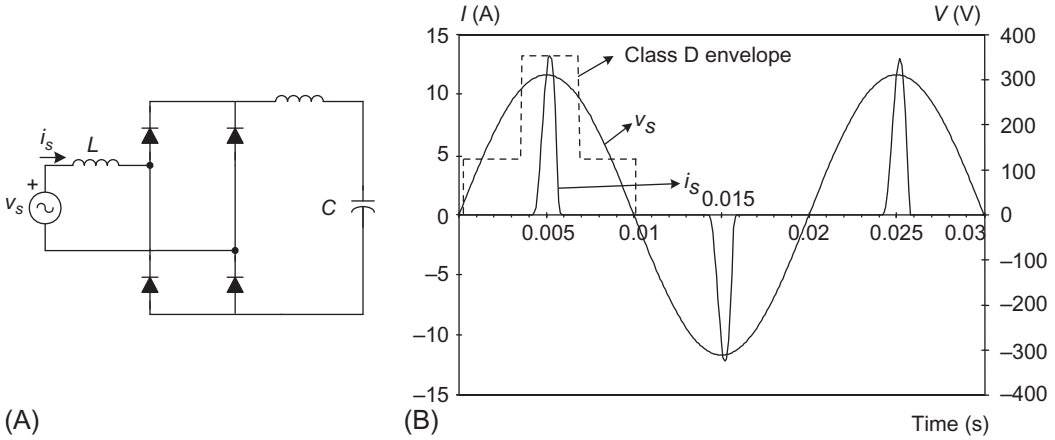


FIG. 8.15 Single-phase rectifier, (A) circuit and (B) waveforms of the input voltage and current.

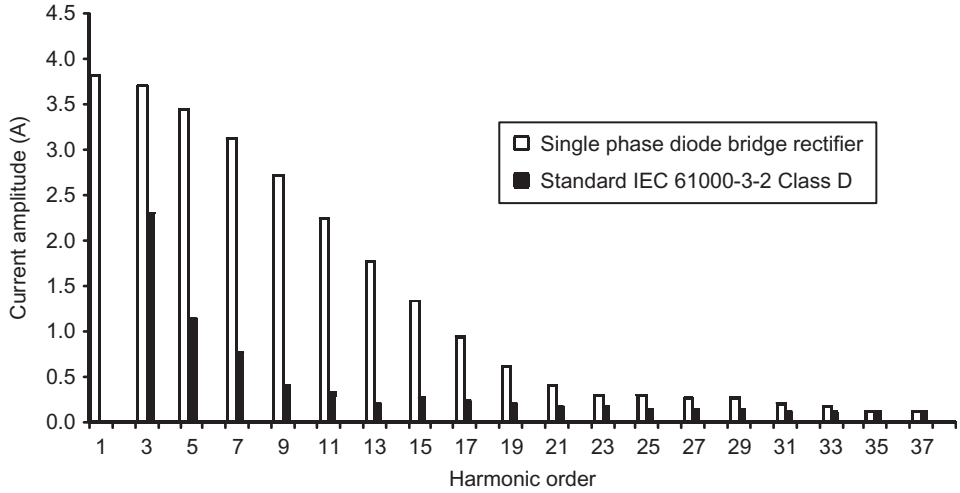


FIG. 8.16 Input current harmonics produced by a single-phase diode bridge rectifier.

TABLE 8.1 Harmonic Content of the Current of Fig. 8.15

n	3	5	7	9	11	13	15	17	19	21
I_n/I_1 (%)	96.8	90.5	81.7	71.0	59.3	47.3	35.7	25.4	16.8	10.6

harmonic limits, shown in Fig. 8.16. It is clear that a single-phase line-commutated rectifier with the parameters shown in Fig. 8.15A is not able to comply with the standard IEC 61000-3-2 Class D. The standard can be satisfied only by adding huge passive filters, which increases the size, weight, and cost of the rectifier. This standard has been the motivation for the development of active methods to improve the quality of the input current and, consequently, the power factor.

8.3.3 The Single-Phase Boost Rectifier

One of the most important high-power-factor rectifiers, from a theoretical and conceptual point of view, is the so-called single-phase boost rectifier, shown in Fig. 8.17A, which is obtained from a classical noncontrolled bridge rectifier, with the addition of transistor T, diode D, and inductor L.

8.3.3.1 Working Principle, Basic Concepts

In boost rectifiers, the input current $i_s(t)$ is controlled by changing the conduction state of transistor T. When transistor T is in the on-state, the single-phase power supply is short-circuited through the inductance L, as shown in Fig. 8.17B; the diode D avoids the discharge of the filter capacitor C through the transistor. The current of the inductance i_L is given by the following equation:

$$\frac{di_L}{dt} = \frac{v_L}{L} = \frac{|v_s|}{L} \tag{8.26}$$

Due to the fact that $|v_s| > 0$, the on-state of transistor T always produces an increase in the inductance current i_L and consequently an increase in the absolute value of the source current i_s.

When transistor T is turned off, the inductor current i_L cannot be interrupted abruptly and flows through diode D,

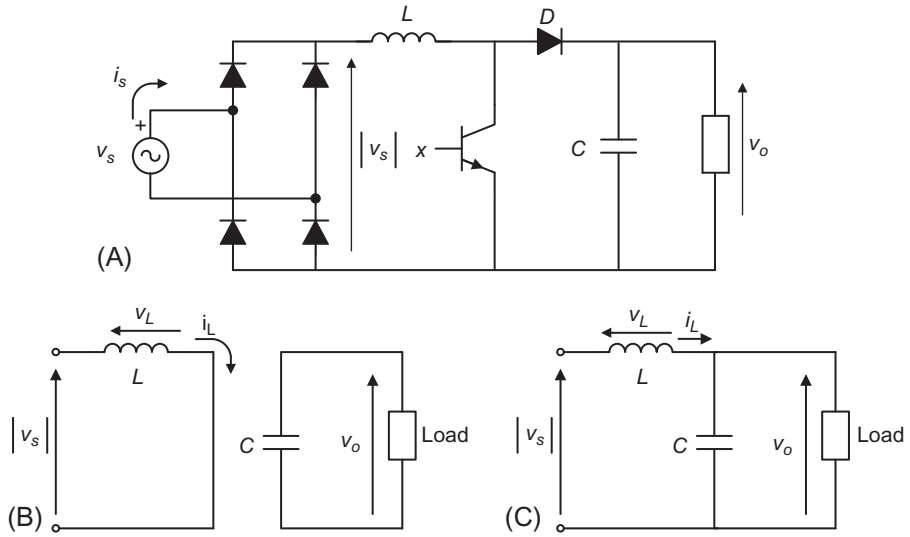


FIG. 8.17 Single-phase boost rectifier, (A) power circuit and equivalent circuit for transistor T in the (B) on-state and (C) off-state.

charging capacitor *C*. This is observed in the equivalent circuit of Fig. 8.17C. In this condition, the behavior of the inductor current is described by

$$\frac{di_L}{dt} = \frac{v_L}{L} = \frac{|v_s| - v_o}{L} \tag{8.27}$$

If $v_o > |v_s|$, which is an important condition for the correct behavior of the rectifier, then $|v_s| - v_o < 0$, and this means that in the off-state the inductor current decreases its instantaneous value.

8.3.3.2 Continuous Conduction Mode (CCM)

When an appropriate firing pulse sequence is applied to transistor T, the waveform of the input current i_s can be controlled to follow a sinusoidal reference, as can be observed in the positive half wave of i_s in Fig. 8.18. This figure shows the reference inductor current $i_{L_{ref}}$, the inductor current i_L, and the gate drive signal x for transistor T. Transistor T is on when $x = 1$, and it is off when $x = 0$.

Fig. 8.18 clearly shows that the on(off)-state of transistor T produces an increase (decrease) in the inductor current i_L. Note that for low values of v_s, the inductor does not have enough energy to increase the current value and, for this reason, it presents a distortion in their current waveform as shown in Fig. 8.18A.

Fig. 8.19 presents a block diagram of the control system for the boost rectifier, which includes a proportional-integral (PI) controller, to regulate the output voltage v_o. The reference value $i_{L_{ref}}$ for the inner current control loop is obtained from the multiplication between the output of the voltage controller and the absolute value $|v_s(t)|$. A hysteresis controller provides a fast control for the inductor current i_L, resulting in a practically sinusoidal input current i_s.

Typically, the output voltage v_o should be at least 10% higher than the peak value of the source voltage $v_s(t)$, in order to assure good dynamic control of the current. The control works with the following strategy: a step increase in the reference voltage $v_{o_{ref}}$ will produce an increase in the voltage error $v_{o_{ref}} - v_o$ and an increase of the output of the PI controller, which originates an increase in the amplitude of the reference current $i_{L_{ref}}$. The current controller will follow this new reference and will increase the amplitude of the sinusoidal input current i_s, which will increase the active power delivered by the single-phase power supply, producing finally an increase in the output voltage v_o.

Fig. 8.20A shows the waveform of the input current i_s and the source voltage v_s. The ripple of the input current can be reduced by shortening the hysteresis width δ. The trade-off for this improvement is an increase in the switching frequency, which is proportional to the commutation losses of the transistors. For a given hysteresis width δ, a reduction of inductance L also produces an increase in the switching frequency. As can be seen, the input current presents a third-harmonic component. This harmonic is generated by the second-harmonic component present in v_o, which is fed back through the voltage (PI) controller and multiplied by the sinusoidal waveform, generating a third-harmonic component on $i_{L_{ref}}$. This harmonic contamination can be avoided by filtering the v_o measurement with a low-pass filter or a band-stop filter around $2\omega_s$. The input current obtained using the measurement filter is shown in Fig. 8.20B. Fig. 8.20D confirms the reduction of the third-harmonic component.

However, in both cases, a drastic reduction in the harmonic content of the input current i_s can be observed in the frequency spectrum of Fig. 8.20C and D. This current fulfills the restrictions established by standard IEC 61000-3-2. The total harmonic

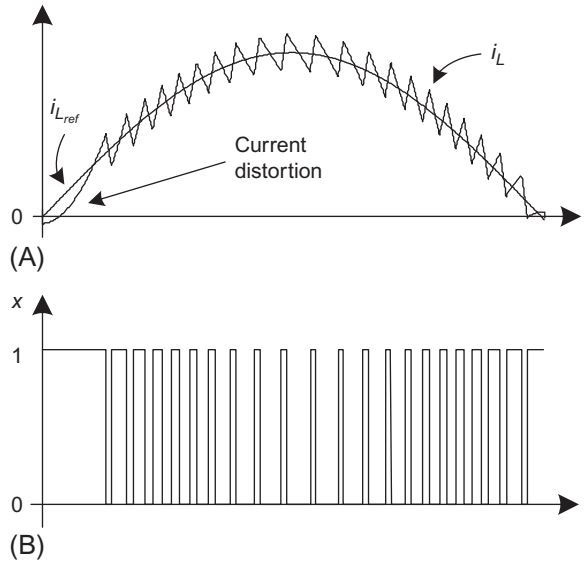


FIG. 8.18 Behavior of the inductor current i_L, (A) waveforms and (B) transistor T gate drive signal x.

distortion of the current in Fig. 8.20A is THD = 7.46%, while the THD of the current of Fig. 8.20B is 4.83%; in both cases, a very high power factor, over 0.99, is reached.

Fig. 8.21 shows the dc voltage control loop dynamic behavior for step changes in the load. An increase in the load, at $t = 0.3$ (s), produces an initial reduction of the output voltage v_o, which is compensated by an increase in the input current i_s. At $t = 0.6$ (s), a step decrease in the load is applied. The dc voltage controller again adjusts the supply current in order to balance the active power.

8.3.3.3 Discontinuous Conduction Mode (DCM)

This PFC method is based on an active current waveform-shaping principle. There are two different approaches considering fixed and variable switching frequency, both operating principles are illustrated in Fig. 8.22.

(a) DCM with fixed switching frequency

The current shaping strategy is achieved by combining three different conduction modes, performed over a

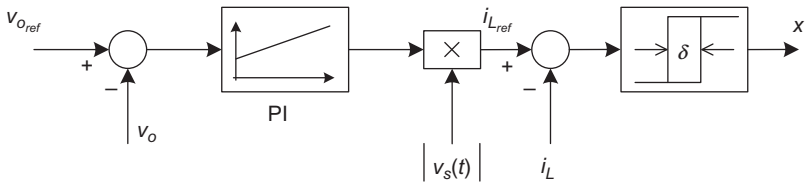


FIG. 8.19 Control system of the boost rectifier.

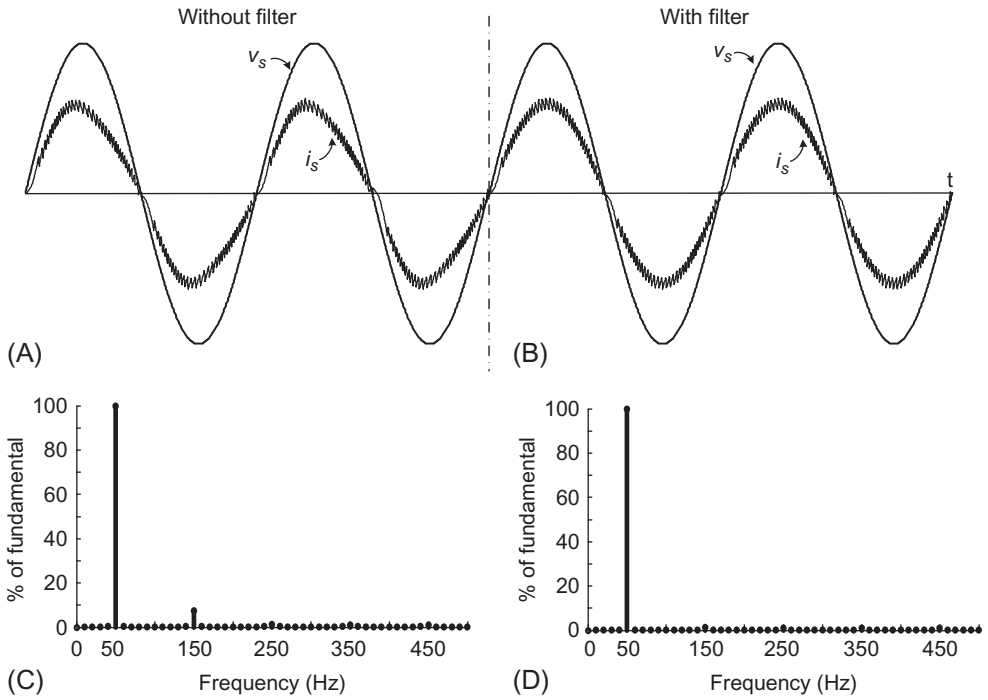


FIG. 8.20 Input current and voltage of the single-phase boost rectifier: (A) without a filter on v_o measurement; (B) with a filter on v_o measurement, frequency spectrum; (C) without filter; and (D) with filter.

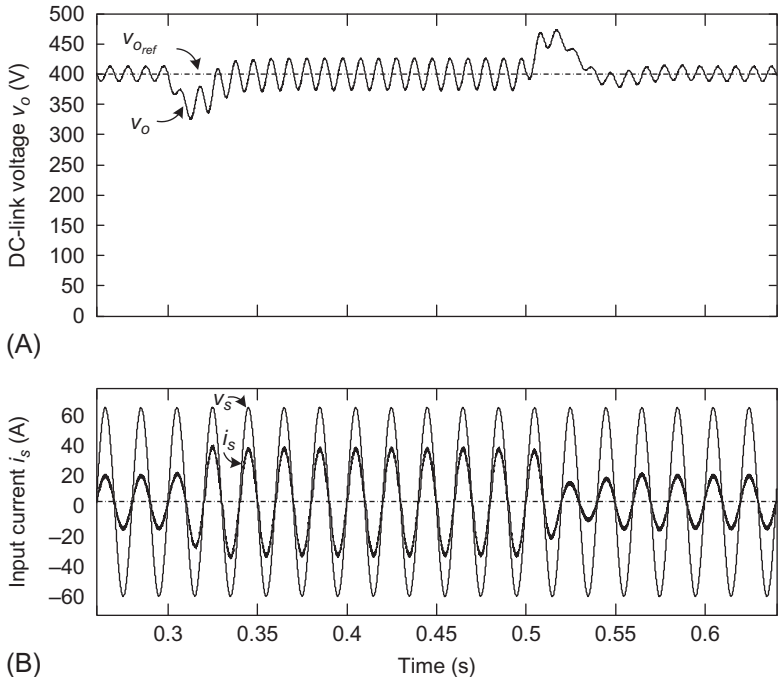


FIG. 8.21 Response to a change in the load, (A) output voltage v_o and (B) input current i_s.

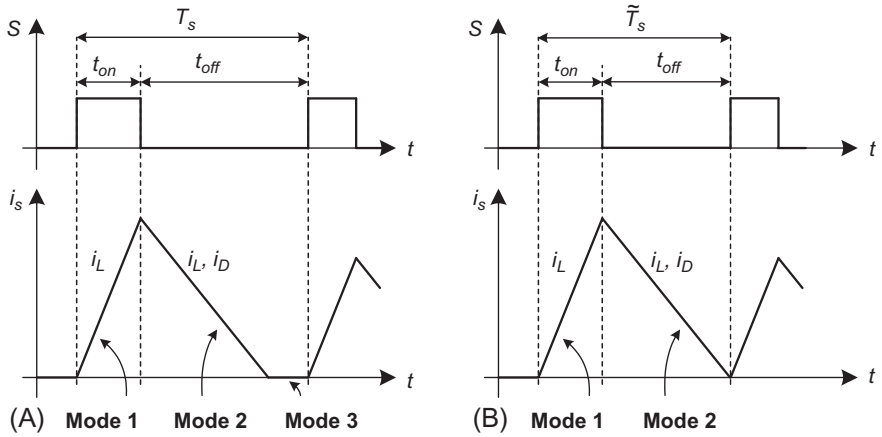


FIG. 8.22 Boost DCM operating principle, (A) with fixed switching frequency and (B) with variable switching frequency.

fixed switching period T_s. At the beginning of each period, the power semiconductor is turned on. During the on-state, shown in Fig. 8.23A, the power supply is short-circuited through the rectifier diodes, the inductor L, and the boost switch T. Hence, the inductor current i_L increases at a rate proportional to the instantaneous value of the supply voltage. As a result, during the on-state, the average supply current i_s is proportional to the supply voltage v_s, which yields to power factor correction.

When the switch is turned off, the current flows to the load trough diode D, as shown in Fig. 8.23B. The instantaneous current value decreases (since the load voltage v_o is higher than the supply peak voltage) at a rate proportional to the difference between the supply and load voltage. Finally, the last mode, illustrated in Fig. 8.23C, corresponds to the time in which the current reaches zero value, completing the switching period T_s. Therefore, the supply current is not proportional to the voltage source during the whole control period, introducing distortion and undesirable EMI in comparison with CCM.

The duty cycle $D = t_{on}/T_s$ is determined by the control loop, in order to obtain the desired output power and to ensure operation in DCM, that is, to reach zero current before the new switching cycle starts. The

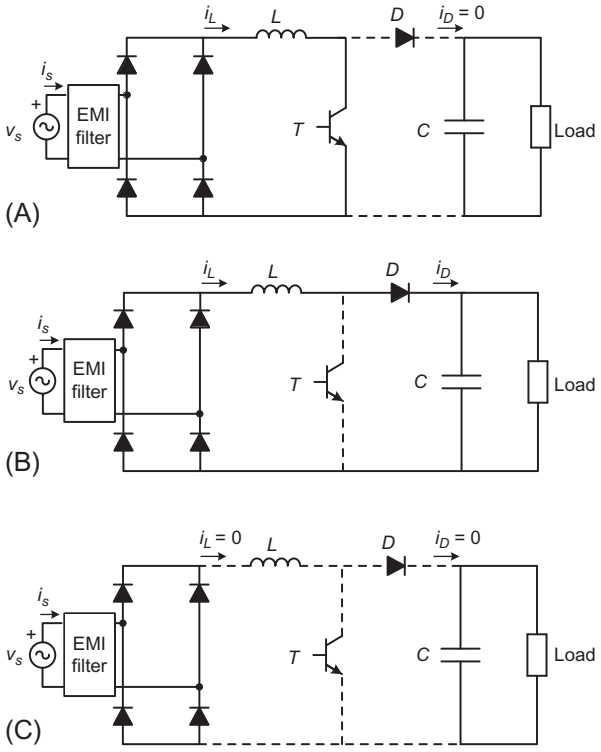


FIG. 8.23 Boost DCM equivalent circuits: (A) mode 1, transistor on, inductor current increasing; (B) mode 2, transistor off, inductor current decreasing; and (C) mode 3, transistor off, inductor current reaches zero. (Insert figure from the third edition).

control strategy can be implemented with analog circuitry as shown in Fig. 8.24, or digitally with modern computing devices. Generally, the duty cycle is controlled with a slow control loop, maintaining the output voltage and duty cycle constant over a half-source cycle.

A qualitative example of the supply voltage and current obtained using DCM is illustrated in Fig. 8.25.

(b) DCM with variable switching frequency

The operating principle is similar to the one used in the previous case, the main difference is that mode 3 is avoided by switching the transistor again to the on-state, immediately after the inductor current reaches zero value. This reduces the current distortion, with the trade-off of introducing variable switching frequency (T_s is variable) and consequently lower-order harmonic content.

Both CCM and DCM achieve an improvement in the power factor. The DCM is more efficient since reverse-recovery losses of the boost diode are eliminated; however, this mode introduces high-current ripple and considerable distortion, and usually, an important fifth-order harmonic is obtained. Therefore, boost DCM applications are limited to 300 W power levels, to meet standards and regulations. The DCM with variable switching frequency reduces this harmonic content, at expends of a wide distributed current spectrum and all related design problems.

8.3.3.4 Resonant Structures for the Boost Rectifiers

An important issue in power electronics is the power losses in power semiconductors. These losses can be classified in two groups: conduction losses and switching losses, as shown in Fig. 8.26.

The conduction losses are produced by the current through the semiconductor juncture, so these losses are unavoidable. However, the switching losses, which are produced while the power semiconductors work in linear state during the transition from on- to off-state or from off- to on-state, can be reduced or even eliminated, if the switch (transition) occurs when (a) the current across the power semiconductor is zero or (b) the voltage between the power terminals of the power semiconductor is zero.

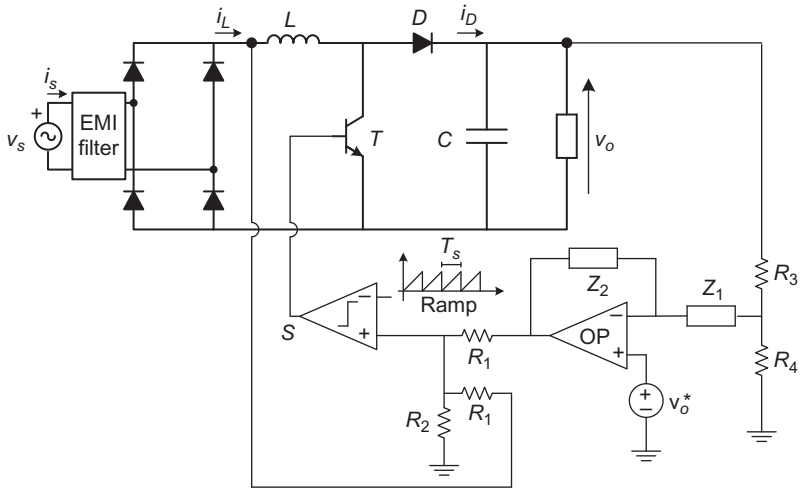


FIG. 8.24 Boost DCM control circuit with fixed switching frequency.

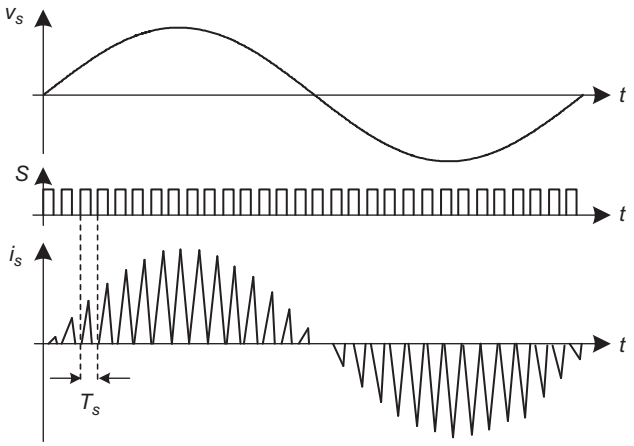


FIG. 8.25 Boost DCM waveforms: supply voltage, transistor control signal, and supply current.

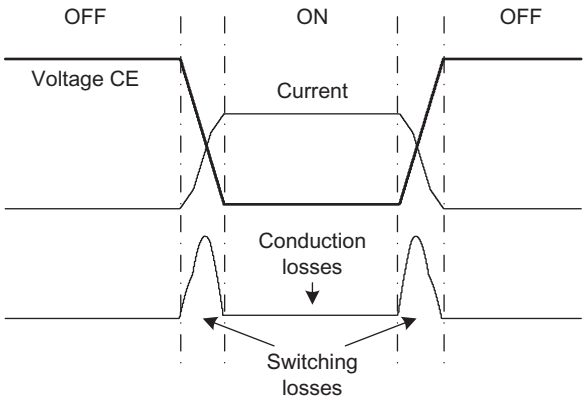


FIG. 8.26 Conduction and switching losses on a power switch.

This operation mode is used in the so-called *resonant* or *soft-switched* converters, which are discussed in detail in a different chapter of this handbook. Resonant operation can also be used with the boost converter topology. In order to produce this condition, topology of Fig. 8.17 needs to be modified, by including reactive components and additional semiconductors.

In Fig. 8.27, a resonant structure for zero-current switching (ZCS) [8] is shown. As can be seen, additional resonant inductors (L_{r_1} and L_{r_2}), capacitors (C_r), diodes (D_{r_1} and D_{r_2}), and power switch (S_r) have been included.

In a similar way, in Fig. 8.28, a resonant structure for zero-voltage switching (ZVS) [9] is shown. Once again, additional inductance (L_r), capacitor (C_r), and power switch (S_r) are added; note, however, that diode D has been replaced by two "resonant diodes," D_{r_1} and D_{r_2}. In both cases, the ZVS or ZCS condition is reached through a proper control of S_r. Other resonant topologies are described in the literature [10–12] with similar behavior.

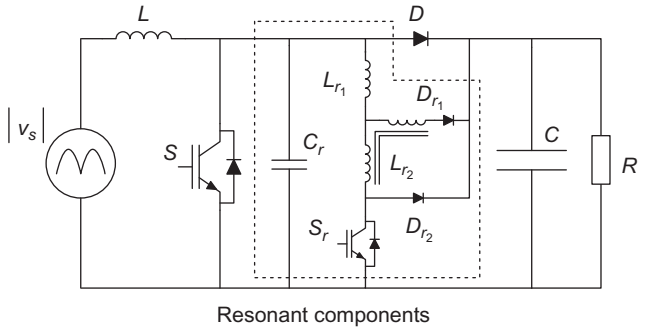


FIG. 8.27 Boost rectifier with ZCS.

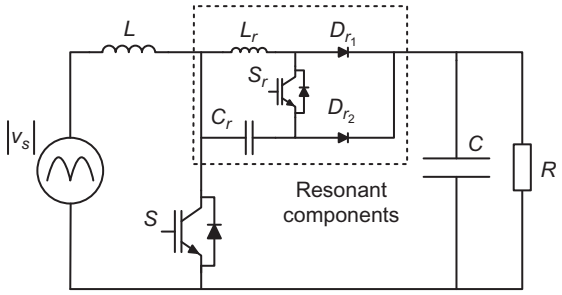


FIG. 8.28 Boost rectifier with ZVS.

8.3.3.5 Bridgeless Boost Rectifier

The bridgeless boost rectifier [13] is shown in Fig. 8.29A. This rectifier replaces the input diode rectifier by a combination of two boost rectifiers that work alternately: (a) When v_s is positive, T_1 and D_1 operate as boost rectifier 1 (Fig. 8.29B), and (b) when v_s is negative, T_2 and D_2 operate as boost rectifier 2 (Fig. 8.29C).

This topology reduces the conduction losses of the rectifier [14,15] but requires a slightly more complex control scheme; also EMI and EMC aspects must be considered.

8.3.4 Voltage Doubler PWM Rectifier

Fig. 8.30A shows the power circuit of the voltage-doubler pulse-width-modulated (PWM) rectifier, which uses two transistors T_1 and T_2 and two filter capacitors C_1 and C_2. The transistors are switched complementary to control the waveform of the input current i_s and the output dc voltage v_o. Capacitor voltages V_{C1} and V_{C2} must be higher than the peak value of the input voltage v_s to ensure the control of the input current.

The equivalent circuit of this rectifier with transistor T_1 in the on-state is shown in Fig. 8.30B. For this case, the inductor voltage dynamic equation is 10.5:

$$v_L = L\frac{di_s}{dt} = v_s(t) - V_{C1} < 0 \tag{8.28}$$

Eq. (8.28) means that under this conduction state, current $i_s(t)$ decreases its value.

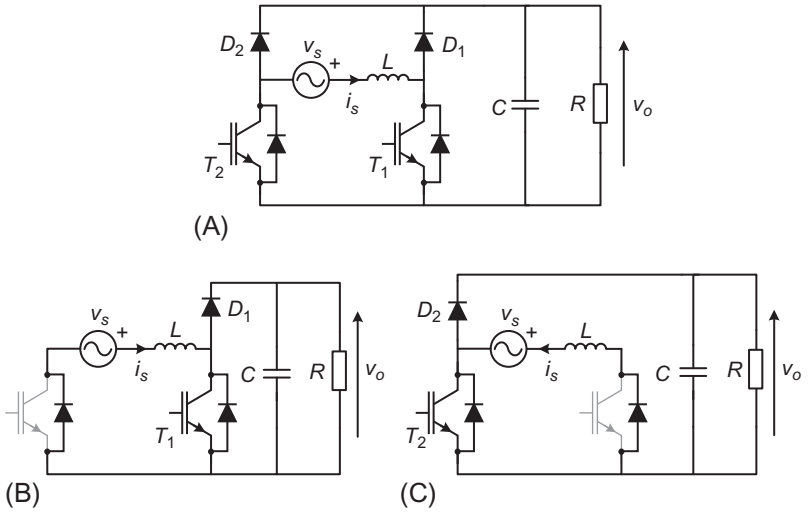


FIG. 8.29 (A) Power circuit of bridgeless boost rectifier; equivalent circuit when (B) $v_s > 0$ and (C) $v_s < 0$.

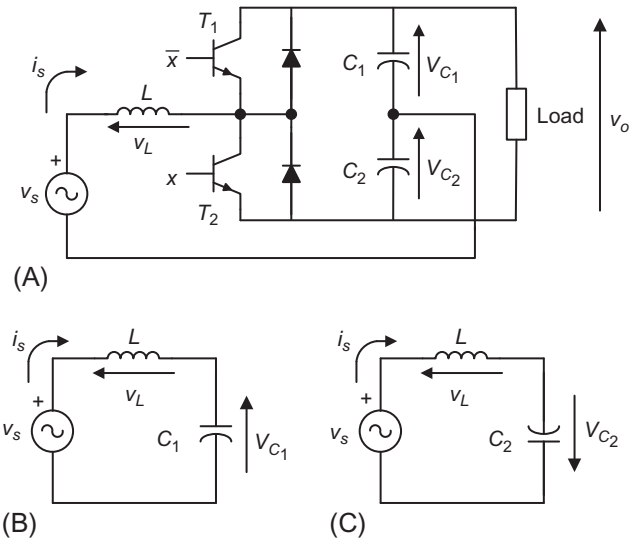


FIG. 8.30 Voltage-doubler rectifier: (A) power circuit, (B) equivalent circuit with T_1 on, and (C) equivalent circuit with T_2 on.

On the other hand, the equivalent circuit of Fig. 8.30C is valid when transistor T_2 is in the conduction state, resulting in the following expression for the inductor voltage

$$v_L = L\frac{di_s}{dt} = v_s(t) + V_{C2} > 0 \tag{8.29}$$

Hence, for this condition, the input current $i_s(t)$ increases.

Therefore, the waveform of the input current can be controlled by switching appropriately transistors T_1 and T_2 in a similar way as shown in Fig. 8.18A for the single-phase boost converter. Fig. 8.31 shows a block diagram of the control system for the voltage-doubler rectifier, which is very similar to the control scheme of the boost rectifier. This topology can present an unbalance in the capacitor voltages V_{C1} and V_{C2}, which will affect the quality of the control. This problem is solved by adding to the actual current value i_s an offset signal proportional to the capacitor's voltage difference.

Fig. 8.32 shows the waveform of the input current. The ripple amplitude of this current can be reduced by decreasing the hysteresis width of the controller.

8.3.5 The PWM Rectifier in Bridge Connection

Fig. 8.33A shows the power circuit of the fully controlled single-phase PWM rectifier in bridge connection, which uses four transistors with antiparallel diodes to produce a controlled dc voltage v_o. Using a bipolar PWM switching strategy, this converter may have two conduction states: (i) transistors T_1 and T_4 in the on-state and T_2 and T_3 in the off-state and (ii) transistors T_2 and T_3 in the on-state and T_1 and T_4 in the off-state.

In this topology, the output voltage v_o must be higher than the peak value of the ac source voltage v_s, to ensure a proper control of the input current.

Fig. 8.33B shows the equivalent circuit with transistors T_1 and T_4 on. In this case, the inductor voltage is given by

$$v_L = L\frac{di_s}{dt} = v_s(t) - V_0 < 0 \tag{8.30}$$

Therefore, in this condition, a reduction of the inductor current i_s is produced.

Fig. 8.33C shows the equivalent circuit with transistors T_2 and T_3 on. Here, the inductor voltage has the following expression:

$$v_L = L\frac{di_s}{dt} = v_s(t) + V_0 > 0 \tag{8.31}$$

which means an increase in the instantaneous value of the input current i_s.

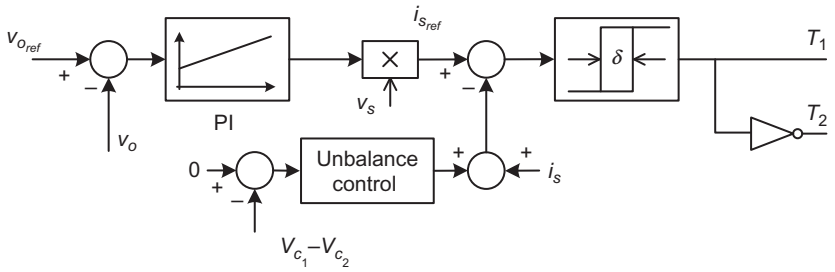


FIG. 8.31 Control system of the voltage-doubler rectifier.

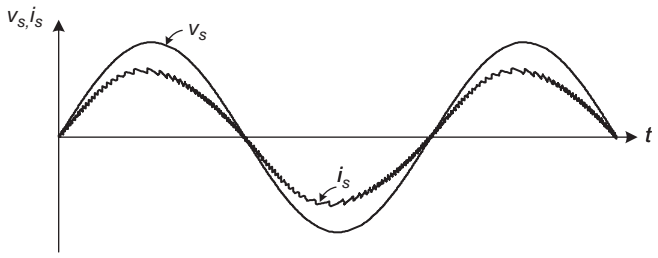


FIG. 8.32 Waveform of the input current in the voltage-doubler rectifier.

Finally, Fig. 8.33D shows the equivalent circuit with transistors T_1 and T_3 or T_2 and T_4 are in the on-state. In this case, the input voltage source is short-circuited through inductor L, which yields

$$v_L = L\frac{di_s}{dt} = v_s(t) + V_0 > 0 \tag{8.32}$$

Eq. (8.32) implies that the current value will depend on the sign of v_s.

The waveform of the input current i_s can be controlled by appropriately switching transistors T_1–T_4 or T_2–T_3, originating a similar shape to the one shown in Fig. 8.18A for the single-phase boost rectifier.

The control strategy for the rectifier is similar to the one illustrated in Fig. 8.31, for the voltage-doubler topology. The quality of the input current obtained with this rectifier is the same as presented in Fig. 8.32 for the voltage-doubler configuration.

The input current waveform can be slightly improved if the state of Fig. 8.33D is used. This can be done by replacing the hysteresis current control with a more complex linear control plus a three-level PWM modulator. This method reduces the semiconductor switching frequency and provides a more defined current spectrum.

Finally, it must be said that one of the most attractive characteristics of the fully controlled PWM converter in bridge connection and the voltage doubler is their regeneration capability. In effect, these rectifiers can deliver power from the load to the single-phase supply, operating with sinusoidal current and a high power factor of PF > 0.99. Fig. 8.33E shows that during regeneration, the input current i_s is 180 degrees out of phase with respect to the supply voltage v_s, which means operation with power factor PF ≈ −1 (PF is approximately 1 because of the small harmonic content in the input current).

8.3.6 Applications of Unity Power Factor Rectifiers

8.3.6.1 Boost Rectifier Applications

The single-phase boost rectifier has become the most popular topology for power factor correction (PFC) in general-purpose power supplies. To reduce the costs, the complete control system shown in Fig. 8.19 and the gate drive circuit of the power transistor have been included in a single integrated circuit (IC), like the UC3854 [16] or MC33262, shown in Fig. 8.34.

Today, there is increased interest in developing high-frequency electronic ballasts to replace the classical electromagnetic ballast present in fluorescent lamps. These electronic ballasts require an ac-dc converter. To satisfy the harmonic current injection from electronic equipment and to maintain a high power quality, a high-power-factor rectifier can be used, as shown in Fig. 8.35 [17].

8.3.6.2 Voltage Doubler PWM Rectifier

The development of low-cost compact motor drive systems is a very relevant topic, particularly in the low-power range. Fig. 8.36 shows a low-cost converter for low-power induction motor drives. In this configuration, a three-phase induction motor is fed through the converter from a single-phase power supply. Transistors T_1 and T_2 and capacitors C_1 and C_2 constitute the voltage-doubler single-phase rectifier, which controls the dc link voltage and generates sinusoidal input current, working with close-to-unity power factor [18]. On the other hand, transistors T_3, T_4, T_5, and T_6 and capacitors C_1 and C_2 constitute the power circuit of an asymmetrical inverter that supplies the motor. An important characteristic of the power circuit shown in Fig. 8.36 is the capability of regenerating power to the single-phase mains.

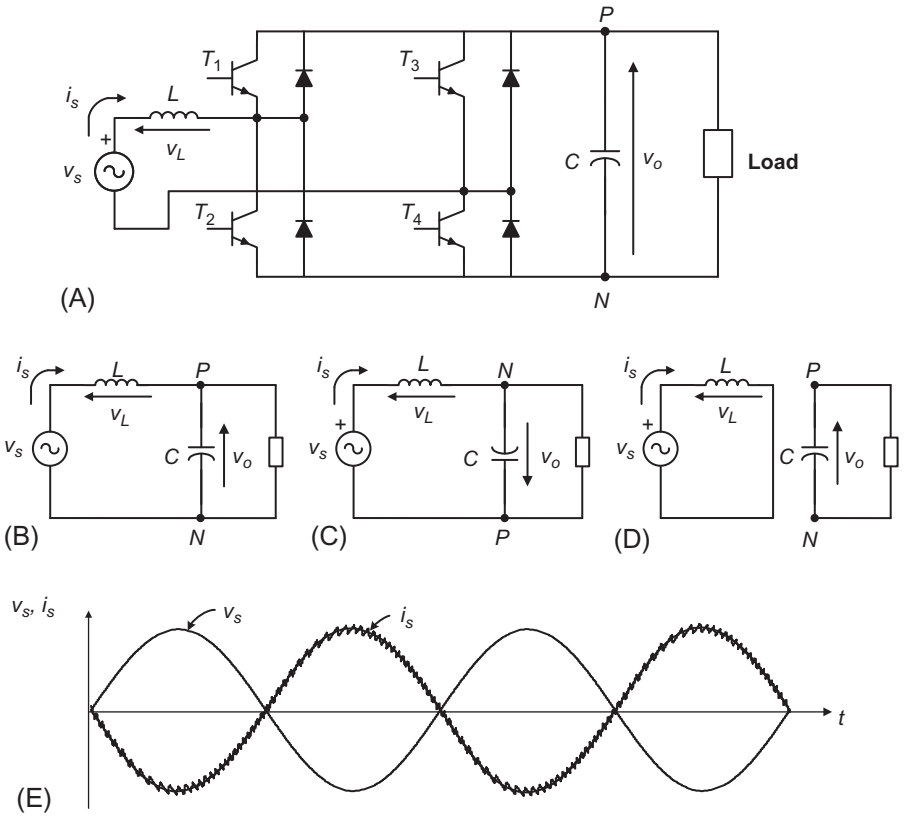


FIG. 8.33 Single-phase PWM rectifier in bridge connection: (A) power circuit, (B) equivalent circuit with T_1 and T_4 on, (C) equivalent circuit with T_2 and T_3 on, (D) equivalent circuit with T_1 and T_3 or T_2 and T_4 on, and (E) waveform of the input current during regeneration.

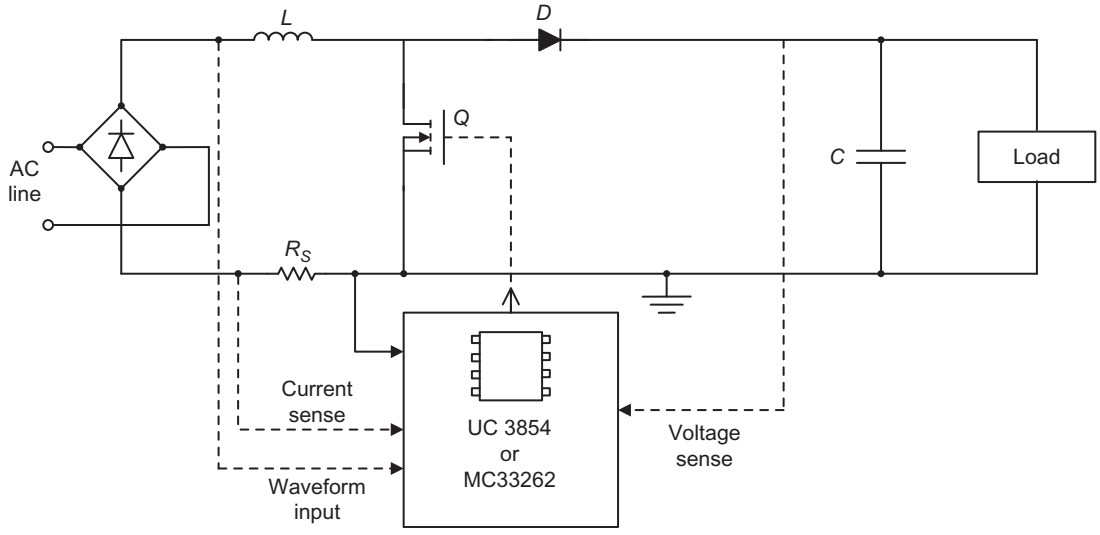


FIG. 8.34 Simplified circuit of a power factor corrector with control integrated circuit.

8.3.6.3 PWM Rectifier in Bridge Connection

Distortion of the input current in the line-commutated rectifiers with capacitive filtering is particularly critical in the UPS fed from motor-generator sets. In effect, due to the higher value of the generator impedance, the current distortion can originate an unacceptable distortion on the ac voltage, which affects the behavior of the whole system. For this reason, it is very attractive to use rectifiers with low distortion in the input current.

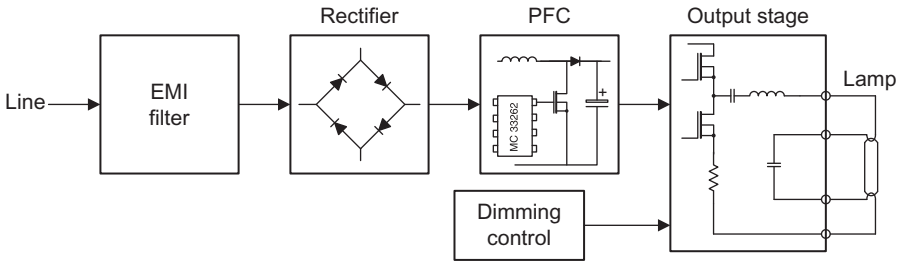


FIG. 8.35 Functional block diagram of electronic ballast with power factor correction.

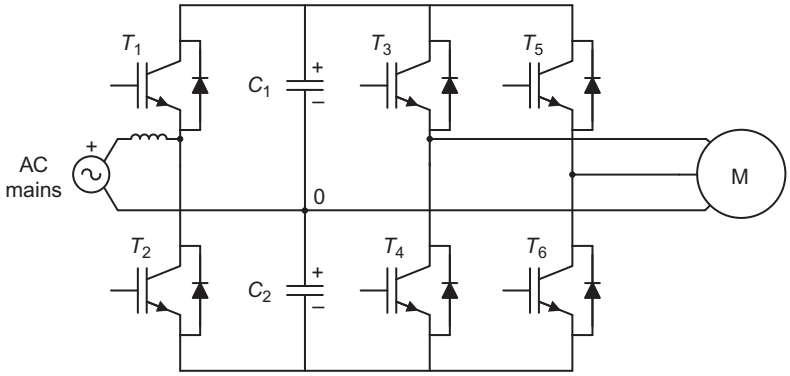


FIG. 8.36 Low-cost induction motor drive.

Fig. 8.37 shows the power circuit of a single-phase UPS, which has a PWM rectifier in bridge connection at the input side. This rectifier generates a sinusoidal input current and controls the charge of the battery [19].

Perhaps the most typical and widely accepted area of application of high-power-factor single-phase rectifiers is in locomotive drives [20]. An essential prerequisite for proper operation of voltage-source three-phase inverter drives in modern locomotives is the use of four-quadrant line-side converters, which ensure motoring and braking of the drive, with reduced harmonics in the input current. Fig. 8.38 shows a simplified power circuit of a typical drive for a locomotive connected to a single-phase power supply [20], which includes a high-power-factor rectifier at the input.

Finally, Fig. 8.39 shows the main circuit diagram of the 300 series Shinkansen train [21]. In this application, ac power from the overhead catenary is transmitted through a transformer to single-phase PWM rectifiers, which provide the dc voltage for the inverters. The rectifiers are capable of controlling the input ac current in an approximate sine waveform and in phase with the voltage, achieving power factor close to unity on powering and on regenerative braking. Regenerative braking produces energy savings and an important operational flexibility.

8.3.7 Synchronous Rectifier

The synchronous rectifier (SR) also known as active rectifier is able to reduce the losses, which lead to improvement in efficiency. The conduction loss contributes a significant role in the overall power loss of diode rectifier, especially in low-output-voltage applications. In the diode rectifier, conduction loss of diode

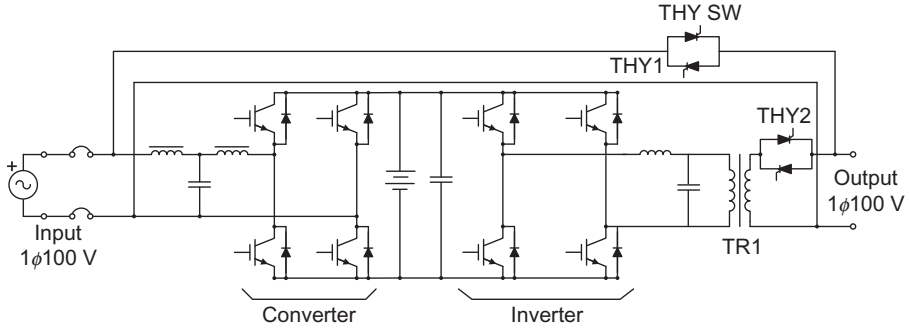


FIG. 8.37 Single-phase UPS with PWM rectifier.

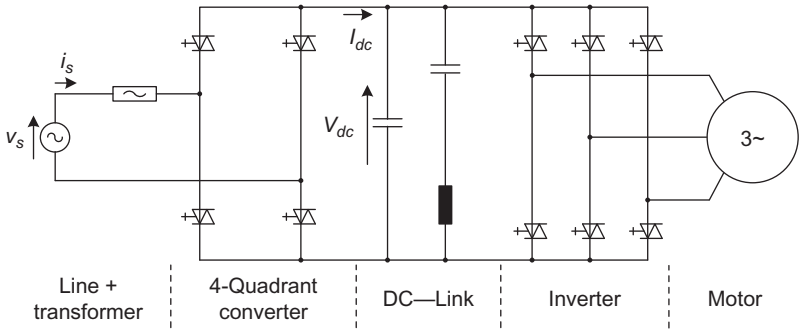


FIG. 8.38 Typical power circuit of an ac drive for locomotive.

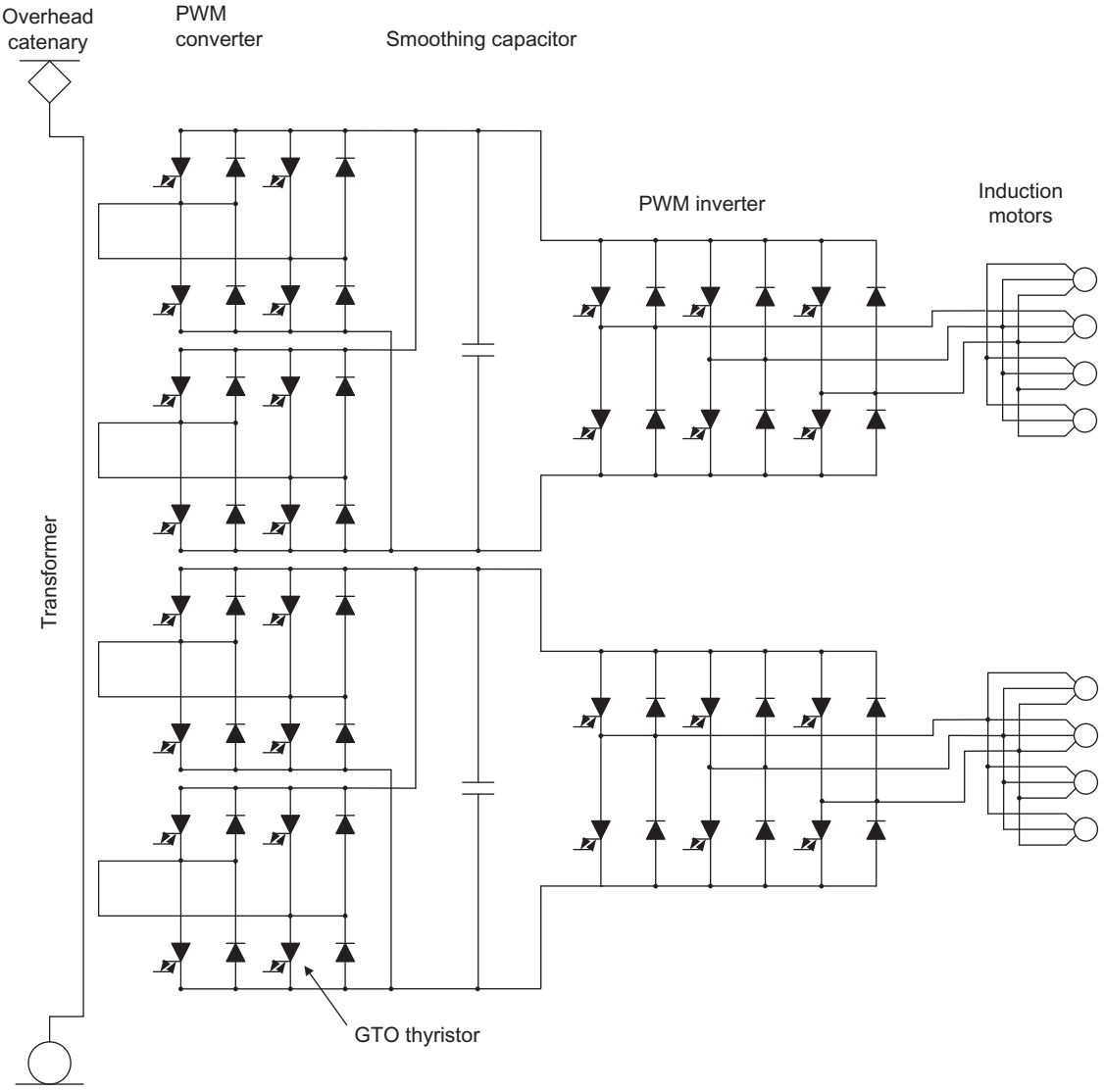


FIG. 8.39 Main circuit diagram of 300 series Shinkansen locomotives.

depends on the forward voltage drop, diode resistance, and the magnitude of current that passes through the devices, while in the SR, MOSFET conduction loss depends on the on resistance ($R_{DS,on}$) of the MOSFET and the current that passes through the devices. Moreover, driving loss is also a part of conduction losses in MOSFET, but it has a very less significant role as compared with total power loss. Therefore, the SR has been widely adopted in low-output-voltage applications with reducing the conduction loss of the output rectifier to improve the efficiency.

The advantages of using SR in high-performance, high-power converters include better efficiency, lower power dissipation, better thermal performance, and inherently optimal current sharing when synchronous MOSFETs are paralleled. The number of MOSFETs can be paralleled to handle higher output currents and results in less equivalent effective $R_{DS,on}$. Moreover, $R_{DS,on}$ has a positive temperature coefficient so the MOSFETs will automatically tend to share current equally, facilitating optimal thermal distribution among the SR devices. This improves the ability to remove heat from the components and the PCB, directly improving the thermal performance of the design. Other potential benefits from SR include smaller form factors, higher ambient operating temperatures, and higher power densities. As discussed above, the downside to SRs is that they require control circuitry to ensure the devices turn on or off synchronously, that is, at the right time. Circuitry required for the control of the SR normally includes voltage and current detectors and drive circuitry for the active devices.

8.3.7.1 Operating Principle

Fig. 8.40 shows the circuit diagram of SR that consists an inductor and four transistors with their body diodes. The transistor used in the circuit must be the MOSFET that can conduct in both the direction. The operating principle of SR is based on the modes of technique to generate the gate signal. The current-driven SR has been used to generate the gate signal for the devices as this method is suitable for all types of topologies and offered number of advantages over voltage-driven method. The current-driven method senses the current flowing through the SR to turn on and turn off the SR properly. The current sensor is used to sense the input current that must flow through the devices. However, for positive half cycle of supply voltage, the current will flow (source to rectifier direction) through the MOSFETs S_1 and S_2, and for negative cycle of supply voltage, current will flow (rectifier to source direction) through MOSFETs S_3 and S_4.

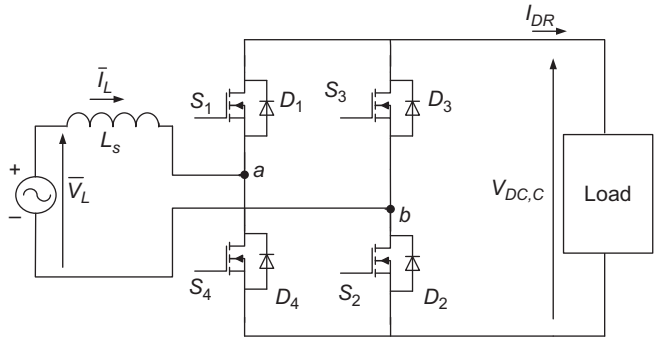


FIG. 8.40 Schematic of synchronous rectifier.

The waveforms of gate signal and dead time are shown in Fig. 8.41. At the beginning of the sinusoidal cycle, the current starts flowing in the body diode, generating a negative V_{DS} across the MOSFET; at that point, turn-on signal is provided to the MOSFET. The dropout voltage across the device falls to much lower voltage, and MOSFET turned on as soft switching that helps to reduce the power losses and results in increasing the system efficiency. Once the MOSFET is on, it must remain in this position until the rectified current will decrease to almost zero; closer is better for the losses point of view. Therefore, a zero-crossing comparator can be used to understand when the drain-source voltage reaches the zero-voltage condition. For this purposes, the value of threshold voltage to turn off the devices must be negative and close to zero, to avoid cross conduction and reduce the body-diode conduction interval at the tail of the semisinusoid.

Let us assume that there are two situations that occur: (a) Current has a spike, and (b) current has multiple zero crossing as shown in Figs. 8.42 and 8.43, respectively. When current has a spike, sensor detects zero current, and MOSFETs S_1 and S_2 are turned off, and negative current flows through the body diodes. Again, current crosses the zero crossing and becomes positive, and body diodes D_1 and D_2 start conducting for the dead-time C as shown in Fig. 8.43. After the dead-time C, again MOSFETs. Moreover, in the case of multiple zero crossing, when the current passes from positive to negative (i.e., at point z_1), sensor detects zero current, and MOSFETs S_1 and S_2 are

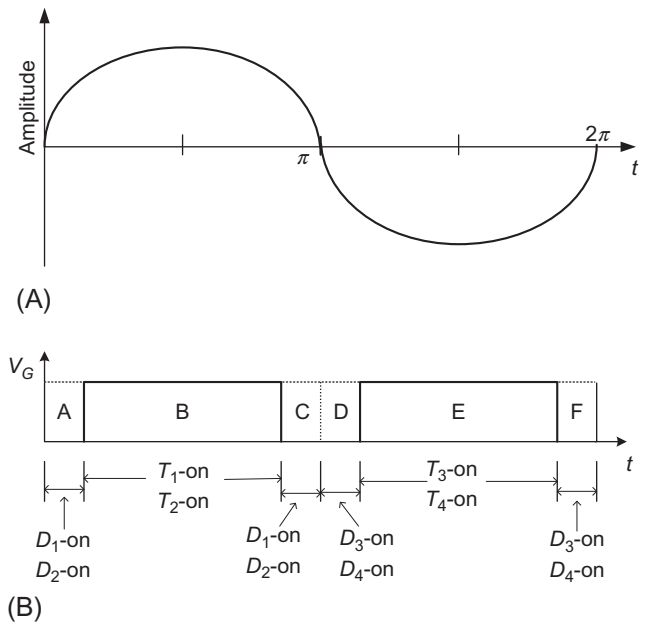


FIG. 8.41 Schematic diagram of (A) current signal and (B) turn-on and turn-off period [22].

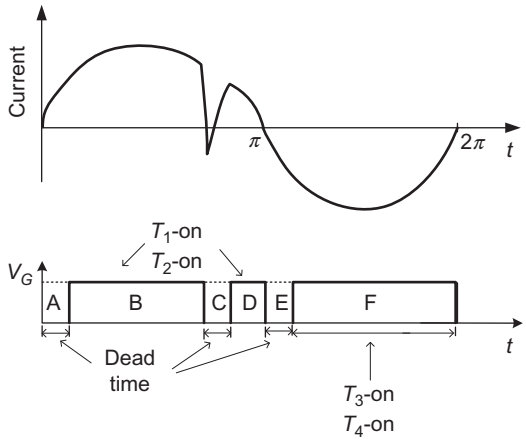


FIG. 8.42 Waveform of current spike.

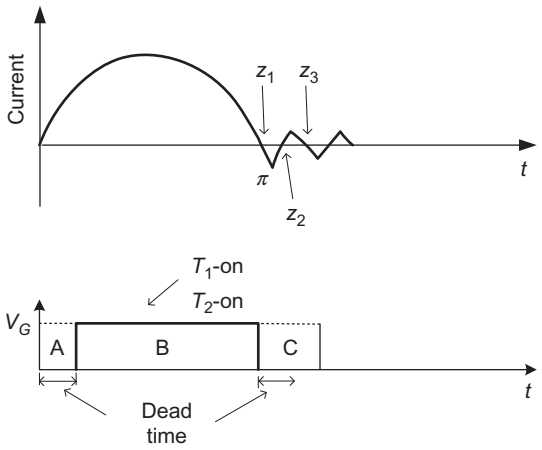


FIG. 8.43 Waveform of current with multiple zero crossing.

turned off. The negative current flows through the body diodes D_3 and D_4, and again, current changes the direction, crosses the zero crossing (i.e., at point z_2), and becomes positive. Then, body diodes D_1 and D_2 start conducting, and again, current changes the direction, crosses the zero crossing (i. e. at point z_3), becomes negative, and flows through the body diodes D_3 and D_4, and process will have continued. In multiple zero crossing, the conduction period of body diodes either D_1 and D_2 or D_3 and D_4 is larger than dead time; then, respective MOSFETs (for instance, for diodes D_1 and D_2, MOSFETs S_1 and S_2 will conduct) will turn on, and they will conduct till the next zero crossing.

8.3.8 Controlled Rectifier Using Single Phase Matrix Converter (SPMC)—Boost Rectifier Operation

The commutation problem is the use of inductive loads where the commutation occurs during the pair of switches turn "off" making the energy in the inductor, being converted into switching spikes. Theoretically, the switching in the SPMC must be instantaneous and simultaneous; unfortunately, it is impossible for realization in practical systems due to turn-on/turn-off IGBT characteristics; to solve these difficulties, safe commutation strategy was developed in Ref. [18] to suppress the spikes induced by manipulation of the switch according to the switching pattern as in Fig. 2.

The controlled rectifier using SPMC for boost operation is shown in Fig. 8.44. A boost inductor L is connected at the ac side to reduce electromagnetic interference. The circuit in Fig. 8.44 operates in two modes; in the mode 1, S1a and S3a are switched "on" at $t=0$. And the input current flows through inductor L. At $t=1$, switches S1a and S4a are switched "on" at $t=1$, while S3a is switched "off." Current would reverse and now flow through the load. The inductor current falls until switch S3a is turned "on" again in the next cycle. The energy stored in inductor L is then transferred to the load. The switching waveform is shown in the Fig. 8.45.

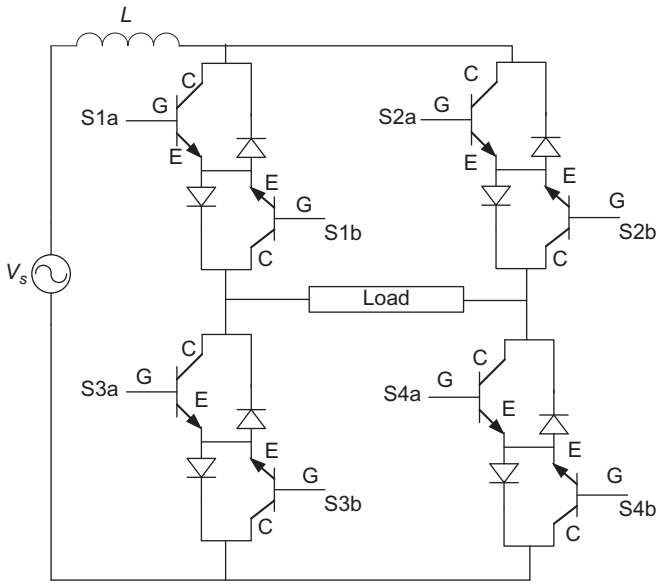


FIG. 8.44 Controlled rectifier using SPMC topology for boost rectifier operation [23].

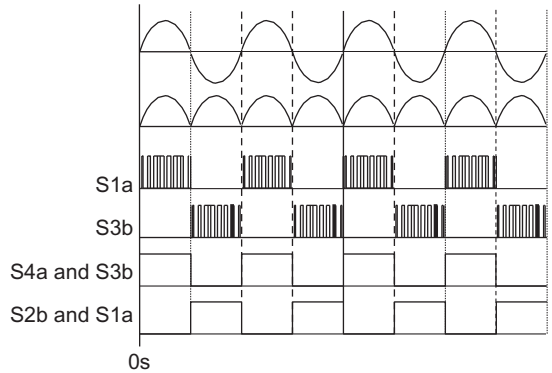


FIG. 8.45 Switching pattern for commutation strategy [23].

References

[1] M.H. Rashid, Power Electronics, Circuits, Devices and Applications, third ed., Academic, New York, 2001.

[2] N. Mohan, T. Undeland, W. Robbins, Power Electronics: Converters Applications and Design, third ed., Wiley, New York, 2002.

[3] J. Rodríguez, P. Lezana, S. Kouro, A. Weinstein, Single-Phase Controlled Rectifiers, in: M.H. Rashid (Ed.), Power Electronics Handbook, third ed., Butterworth-Heinemann, Boston, 2011, pp. 183–204 (Chapter 11).

[4] J. Perkinson, UPS systems: a review, in: Proc. of IEEE Applied Power Electronics Conference and Exposition, 1988, pp. 151–154.

[5] J.R. Rodriguez, J.W. Dixon, J.R. Espinoza, J. Pontt, P. Lezana, PWM regenerative rectifiers: state of the art, IEEE Trans. Ind. Electron. 52 (1) (2005) 5–22.

[6] R. Dwyer, D. Mueller, Selection of transformers for commercial buildings, in: Proc. of IEEE/IAS 1992 Annual Meeting, U.S.A., Oct 1992, 1992, pp. 1335–1342.

[7] IEC 61000-3-2:2014, Electromagnetic compatibility (EMC)—Part 3-2: Limits—Limits for harmonic current emissions (equipment input current $\leq$ 16 A per phase), IEC 61000-3-2:2004, International Standard, 2004.

[8] D.C. Martins, F.J.M. de Seixas, J.A. Brilhante, I. Barbi, A family of dc-to-dc PWM converters using a new ZVS commutation cell, in: Proc. IEEE PESC'93, 1993, pp. 524–530.

[9] J. Bassett, New, zero voltage switching, high frequency boost converter topology for power factor correction, in: Proc. INTELEC'95, 1995, pp. 813–820.

[10] R. Streit, D. Tollik, High efficiency telecom rectifier using a novel soft-switched boost-based input current shaper, in: Proc. INTELEC'91, 1991, pp. 720–726.

[11] Y. Jang, M.M. Jovanović, A new, soft-switched, high-power-factor boost converter with IGBTs, in: Presented at the INTELEC'99, 1999. Paper 8–3.

[12] M.M. Jovanović, A technique for reducing rectifier reverse-recovery-related losses in high-voltage, high-power boost converters, in: Proc. IEEE APEC'97, 1997, pp. 1000–1007.

[13] D.M. Mitchell, 1983. AC-DC converter having an improved power factor. U.S. Patent 4 412 277.

[14] A.F. de Souza, I. Barbi, A new ZVS-PWM unity power factor rectifier with reduced conduction losses, IEEE Trans. Power Electron. 10 (6) (1995) 746–752.

[15] A.F. de Souza, I. Barbi, A new ZVS semiresonant power factor rectifier with reduced conduction losses, IEEE Trans. Ind. Electron. 46 (1) (1999) 82–90.

[16] P. Todd, UC3854 controlled power factor correction circuit design. Application Note U-134, Unitrode Corp.

[17] J. Adams, T. Ribarich, J. Ribarich, A new control IC for dimmable high-frequency electronic ballast, in: IEEE Applied Power Electronics Conference APEC'99, USA, 1999, pp. 713–719.

[18] C. Jacobina, M. Beltrao, E. Cabral, A. Nogueira, Induction motor drive system for low-power applications, IEEE Trans. Ind. Appl. 35 (1) (1999) 52–60.

[19] K. Hirachi, H. Yamamoto, T. Matsui, S. Watanabe, M. Nakaoka, Cost-effective practical developments of high-performance 1kVA UPS with new system configurations and their specific control implementations, in: European Conference on Power Electronics EPE 95, Spain, 1995, pp. 2035–2040.

[20] K. Hückelheim, C. Mangold, Novel 4-quadrant converter control method, in: European Conference on Power Electronics EPE 89, Germany, 1989, pp. 573–576.

[21] T. Ohmae, K. Nakamura, Hitachi's role in the area of power electronics for transportation, in: Proc. of the IECON'93. Hawai, 1993, pp. 714–718.

[22] http://www.ti.com/lit/wp/snva595a/snva595a.pdf (Accessed 23 February 2017).

[23] R. Baharom, N.R. Hamzah, M.K. Hamzah, Advanced single-phase AC-DC converter using single-phase matrix converter topology, in: Proc. IEEE International Conference on Electrical, Control and Computer Engineering, 2011, pp. 33–38.

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9

Three-Phase Controlled Rectifiers

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Florida Polytechnic University, Lakeland, FL, United States

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9.1 Introduction

Three-phase controlled rectifiers have a wide range of applications, from small rectifiers to large high-voltage direct-current (HVDC) transmission systems. They are used for electrochemical processes, many kinds of motor drives, traction equipment, controlled power supplies, and many other applications. From the point of view of the commutation process, they can be classified into two important categories: *line-commutated controlled rectifiers (thyristor rectifiers) and force-commutated pulse-width modulated (PWM) rectifiers.*

9.2 Line-Commutated Controlled Rectifiers

9.2.1 Three-Phase Half-Wave Rectifier

Fig. 9.1 shows the three-phase half-wave rectifier topology. To control the load voltage, the half-wave rectifier uses three common cathode thyristor arrangements. In this figure, the power supply and the transformer are assumed ideal. The thyristor will conduct (*ON* state), when the anode-to-cathode voltage v_{AK} is positive and a firing current pulse i_G is applied to the gate terminal. Delaying the firing pulse by an angle α controls the load voltage. As shown in Fig. 9.2, the firing angle α is measured from the crossing point between the phase supply voltages. At that point, the anode-to-cathode thyristor voltage v_{AK} begins to be positive. Fig. 9.3 shows that the possible range for gating delay is between $\alpha = 0$ and 180 degrees, but because of commutation problems in actual situations, the maximum firing angle is limited to around 160 degrees. As shown in Fig. 9.4, when the load is resistive, current i_d has the same waveform of the load voltage. As the load becomes more and more inductive, the current flattens and finally becomes constant. The thyristor goes to the nonconducting condition (*OFF* state) when the following thyristor is switched *ON* or the current tries to reach a negative value.

With the help of Fig. 9.2, the load average voltage can be evaluated and is given by

$$\begin{aligned} V_D &= \frac{V_{MAX}}{\frac{2}{3}\pi} \int_{-\pi/3+\alpha}^{\pi/3+\alpha} \cos\omega t d(\omega t) \\ &= V_{MAX} \frac{\sin\frac{\pi}{3}}{\frac{\pi}{3}} \cos\alpha \asymp 1.17 V_{f-N}^{rms} \cos\alpha \end{aligned} \tag{9.1}$$

where V_{MAX} is the secondary phase-to-neutral peak voltage, V_{f-N}^{rms} is its root-mean-square (*rms)* value, and ω is the angular frequency of the main power supply. It can be seen from Eq. (9.1) that the load average voltage V_D is modified by changing

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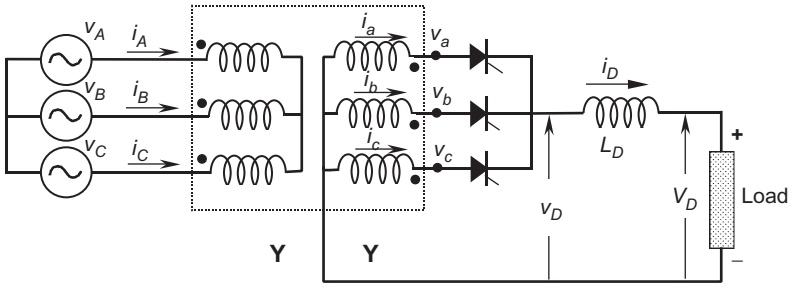


FIG. 9.1 Three-phase half-wave rectifier.

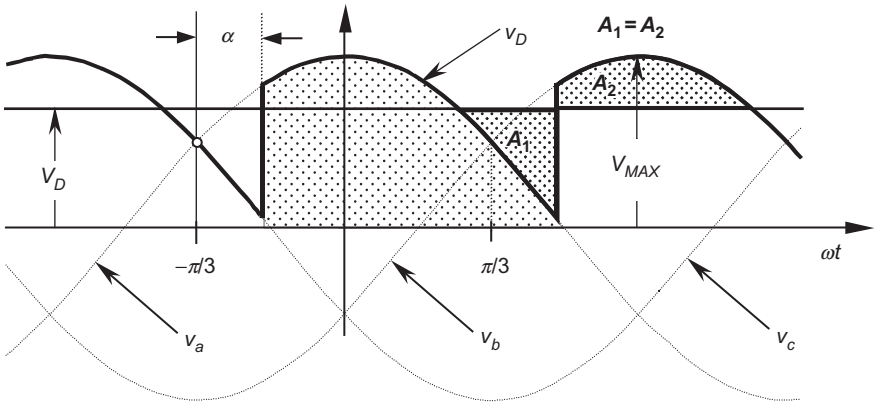


FIG. 9.2 Instantaneous *dc* voltage v_D, average *dc* voltage V_D, and firing angle α.

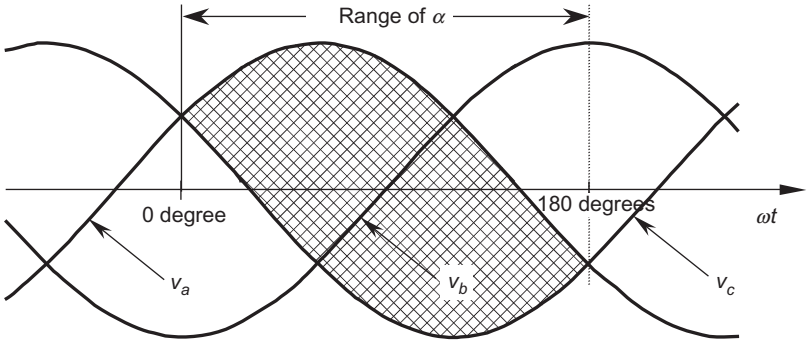


FIG. 9.3 Possible range for gating delay in angle α.

firing angle α. When $\alpha < 90$ degrees, V_D is positive, and when $\alpha > 90$ degrees, the average *dc* voltage becomes negative. In such a case, the rectifier begins to work as an inverter, and the load needs to be able to generate power reversal by reversing its *dc* voltage.

The *ac* currents of the half-wave rectifier are shown in Fig. 9.5. This drawing assumes that the *dc* current is constant (very large L_D). Disregarding commutation overlap, each valve conducts during 120 degrees per period. The secondary currents (and thyristor currents) present a *dc* component that is undesirable and makes this rectifier not useful for high-power applications. The primary currents show the same waveform but with the *dc* component removed. This very distorted waveform requires an input filter to reduce harmonic contamination.

The current waveforms shown in Fig. 9.5 are useful for designing the power transformer. Starting from

$$\begin{aligned} VA_{prim} &= 3V^{rms}_{(prim)f-N} I^{rms}_{prim} \\ VA_{sec} &= 3V^{rms}_{(sec)f-N} I^{rms}_{sec} \\ P_D &= V_D I_D \end{aligned} \tag{9.2}$$

where VA_{prim} and VA_{sec} are the ratings of the transformer for the primary and secondary side, respectively. Here, P_D is

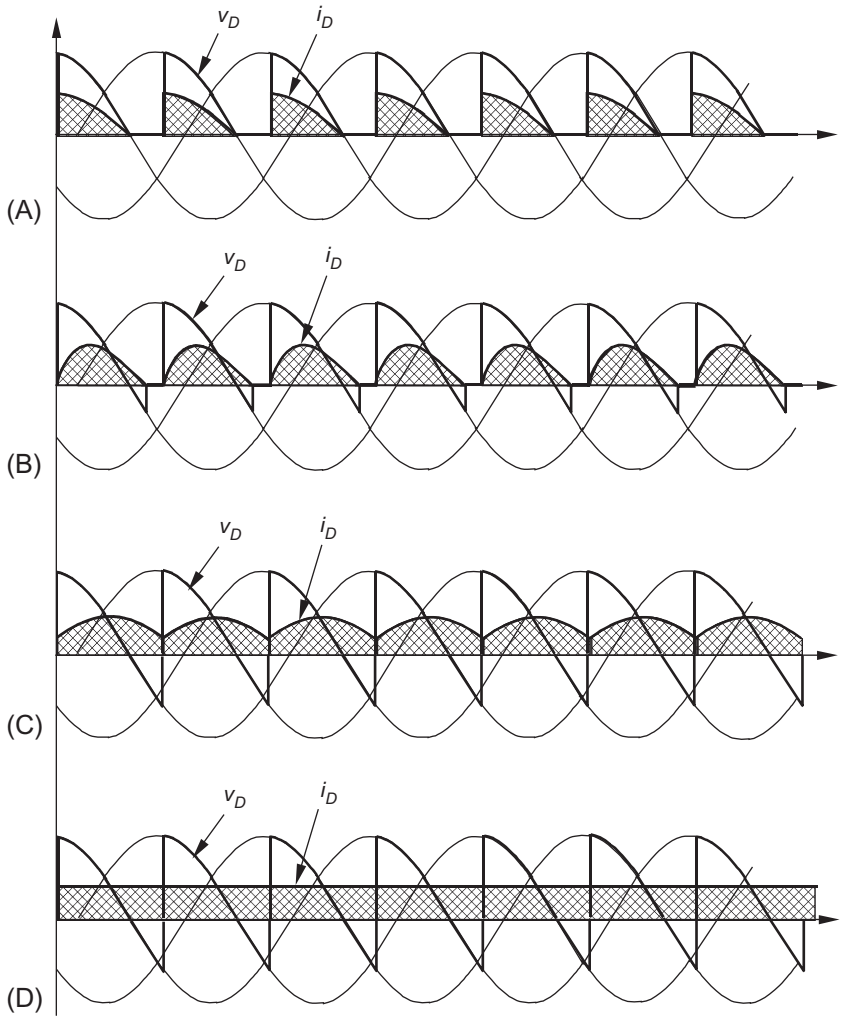


FIG. 9.4 *DC* current waveforms. (A) $R>0$, $L_D=0$, (B) $R>0$, $L_D>0$, (C) $R>0$, L_D large, and (D) R small, L_D very large.

the power transferred to the *dc* side. The maximum power transfer is with $\alpha=0$ degree (or $\alpha=180$ degrees). Then, to establish a relation between *ac* and *dc* voltages, Eq. (9.1) for $\alpha=0$ degree is required:

$$V_D = 1.17V^{rms}_{(sec)f-N} \tag{9.3}$$

and

$$V_D = 1.17aV^{rms}_{(prim)f-N} \tag{9.4}$$

where a is the secondary to primary turn relation of the transformer. On the other hand, a relation between the currents is also possible to obtain. With the help of Fig. 9.5,

$$I^{rms}_{sec} = \frac{I_D}{\sqrt{3}} \tag{9.5}$$

$$I^{rms}_{prim} = a\frac{I_D\sqrt{2}}{3} \tag{9.6}$$

Combining Eqs. (9.2)–(9.6), it yields

$$\begin{aligned} VA_{prim} &= 1.21P_D \\ VA_{sec} &= 1.48P_D \end{aligned} \tag{9.7}$$

Eq. (9.7) shows that the power transformer has to be oversized 21% at the primary side and 48% at the secondary side. Then, a special transformer has to be built for this rectifier. In terms of average *VA*, the transformer needs to be 35% larger than the rating of the *dc* load. The larger rating of the secondary with respect to primary is because the secondary carries a *dc* component inside the windings. Furthermore, the transformer is oversized because the circulation of current harmonics does not generate active power. Core saturation, due to the *dc* components inside the secondary windings, also needs to be taken in account for iron oversizing.

9.2.2 Six-Pulse or Double Star Rectifier

The thyristor side windings of the transformer shown in Fig. 9.6 form a six-phase system, resulting in a six-pulse starpoint (midpoint connection). Disregarding commutation overlap, each

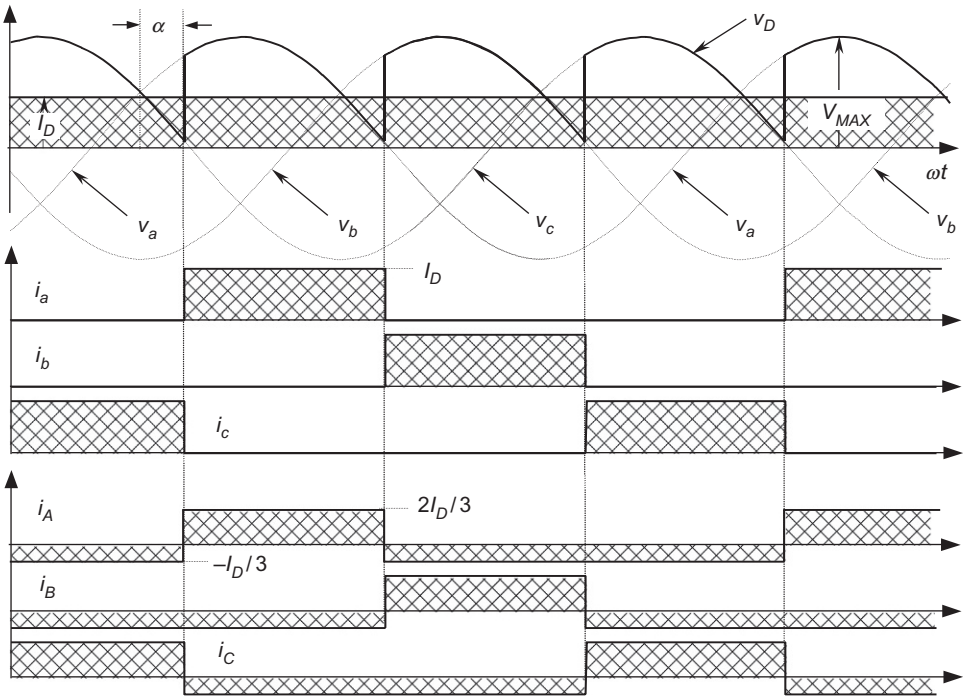


FIG. 9.5 *AC* current waveforms for the half-wave rectifier.

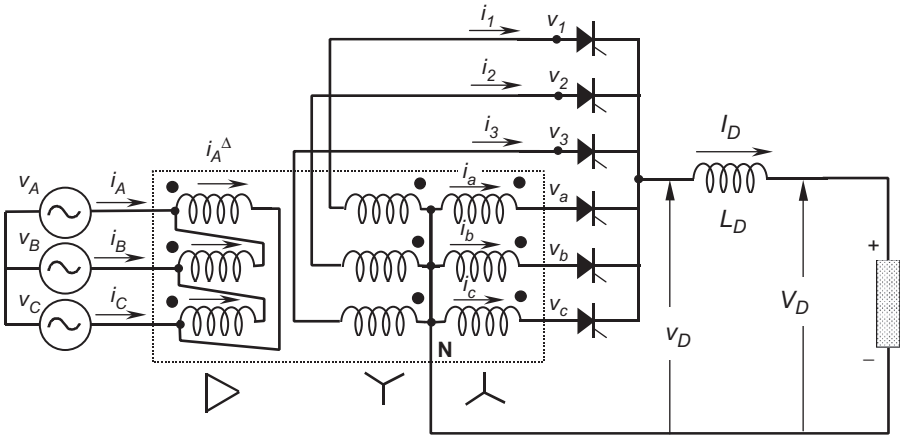


FIG. 9.6 Six-pulse rectifier.

valve conducts only during 60 degrees per period. The direct voltage is higher than that from the half-wave rectifier, and its average value is given by

$$V_D = \frac{V_{MAX}}{\frac{\pi}{3}} \int_{-\pi/6+\alpha}^{\pi/6+\alpha} \cos \omega t d(\omega t) = V_{MAX} \frac{\sin \frac{\pi}{6}}{\frac{\pi}{6}} \cos \alpha \approx 1.35 V_{f-N}^{rms} \cos \alpha \tag{9.8}$$

The *dc* voltage ripple is also smaller than the one generated by the half-wave rectifier, due to the absence of the third harmonic with its inherently high amplitude. The smoothing reactor L_D is also considerably smaller than the one needed for a three-pulse (half-wave) rectifier.

The *ac* currents of the six-pulse rectifier are shown in Fig. 9.7. The currents in the secondary windings present a *dc* component, but the magnetic flux is compensated by the double star. As can be observed, only one valve is fired at a time, and then this connection in no way corresponds to a parallel connection. The currents inside the delta show a symmetrical waveform with 60 degrees conduction. Finally, due to the particular transformer connection shown in Fig. 9.6, the source currents also show a symmetrical waveform but with 120 degrees conduction.

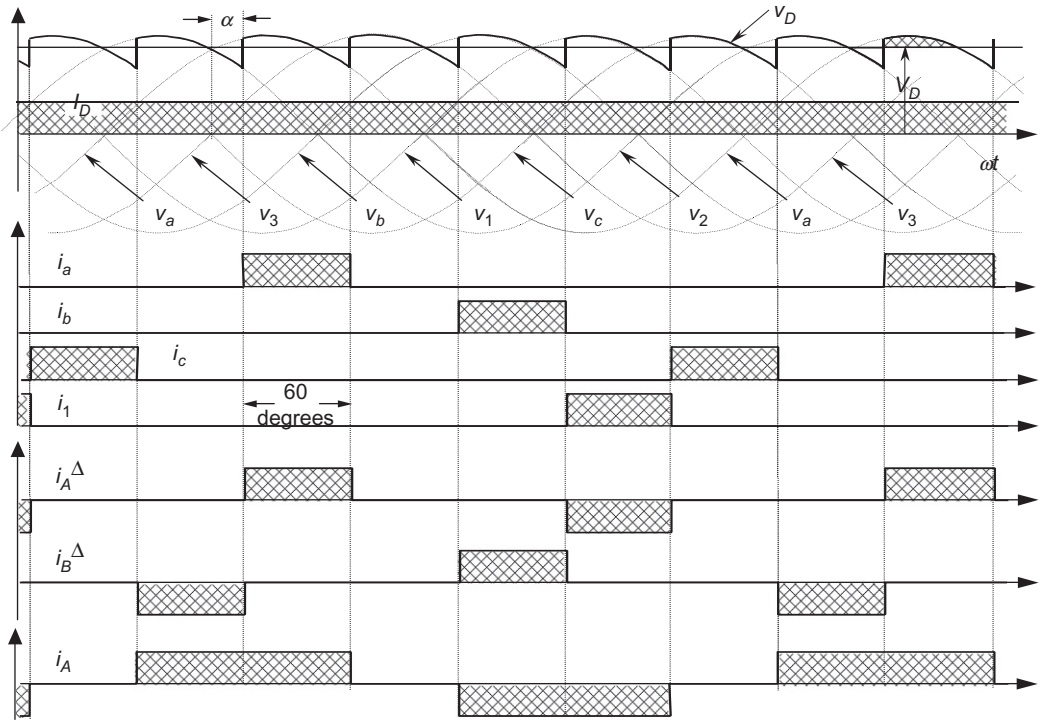


FIG. 9.7 *AC* current waveforms for the six-pulse rectifier.

Evaluation of the rating of the transformer is done in similar fashion to the way the half-wave rectifier is evaluated:

$$VA_{prim} = 1.28P_D$$
$$VA_{sec} = 1.81P_D \tag{9.9}$$

Thus, the transformer must be oversized 28% at the primary side and 81% at the secondary side. In terms of size, it has an average apparent power of 1.55 times the power P_D (55% oversized). Because of the short conducting period of the valves, the transformer is not particularly well utilized.

9.2.3 Double Star Rectifier With Interphase Connection

This topology works as two half-wave rectifiers in parallel and is very useful when high *dc* current is required. An optimal way to reach both good balance and elimination of harmonics is through the connection shown in Fig. 9.8. The two rectifiers are shifted by 180 degrees, and their secondary neutrals are connected through a middle-point autotransformer called "interphase transformer." The interphase transformer is connected between the two secondary neutrals and the middle

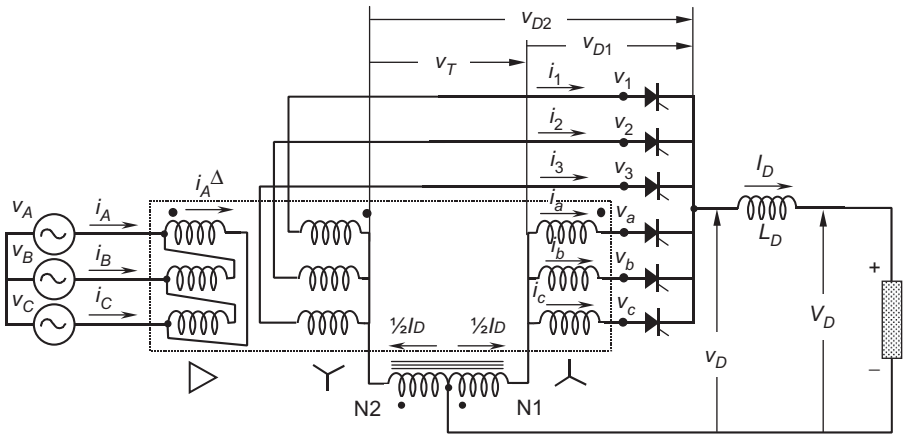


FIG. 9.8 Double-star rectifier with interphase transformer.

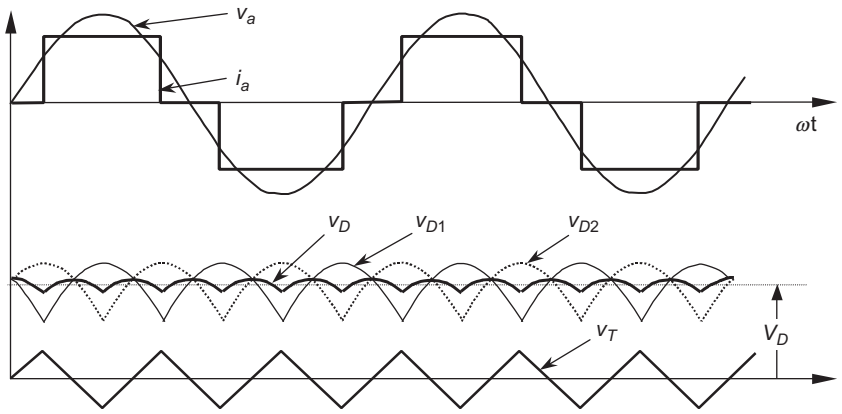


FIG. 9.9 Operation of the interphase connection for $\alpha = 0$ degree.

point at the load return. In this way, both groups operate in parallel. Half the direct current flows in each half of the interphase transformer, and then its iron core does not become saturated. The potential of each neutral can oscillate independently, generating an almost triangular voltage waveform (v_T) in the interphase transformer, as shown in Fig. 9.9. As this converter works like two half-wave rectifiers connected in parallel, the load average voltage is the same as in Eq. (9.1):

$$V_D \approx 1.17 V_{f-N}^{rms} \cos\alpha \tag{9.10}$$

where V_{f-N}^{rms} is the phase-to-neutral *rms* voltage at the valve side of the transformer (secondary).

Fig. 9.9 also shows the two half-wave rectifier voltages, related to their respective neutrals. Voltage v_{D1} represents the potential between the common cathode connection and the neutral N1. The voltage v_{D2} is between the common cathode connection and N2. It can be seen that the two instantaneous voltages are shifted, which gives as a result, a voltage v_D that is smoother than v_{D1} and v_{D2}.

Fig. 9.10 shows how v_D, v_{D1}, v_{D2}, and v_T change when the firing angle changes from $\alpha = 0$ to 180 degrees.The transformer rating in this case is

$$\begin{aligned} VA_{prim} &= 1.05 P_D \\ VA_{sec} &= 1.48 P_D \end{aligned} \tag{9.11}$$

And the average rating power will be $1.26 P_D$, which is better than the previous rectifiers (1.35 for the half-wave rectifier and 1.55 for the six-pulse rectifier). Thus, the transformer is well utilized. Fig. 9.11 shows *ac* current waveforms for a rectifier with interphase transformer.

9.2.4 Three-Phase Full-Wave Rectifier or Graetz Bridge

Parallel connection via interphase transformers permits the implementation of rectifiers for high current applications. Series connection for high voltage is also possible, as shown in the full-wave rectifier of Fig. 9.12. With this arrangement,

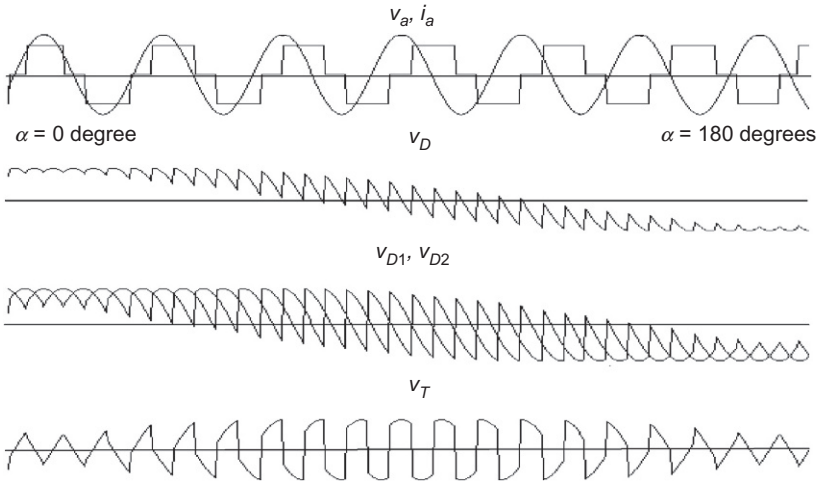


FIG. 9.10 Firing angle variation from $\alpha = 0$ to 180 degrees.

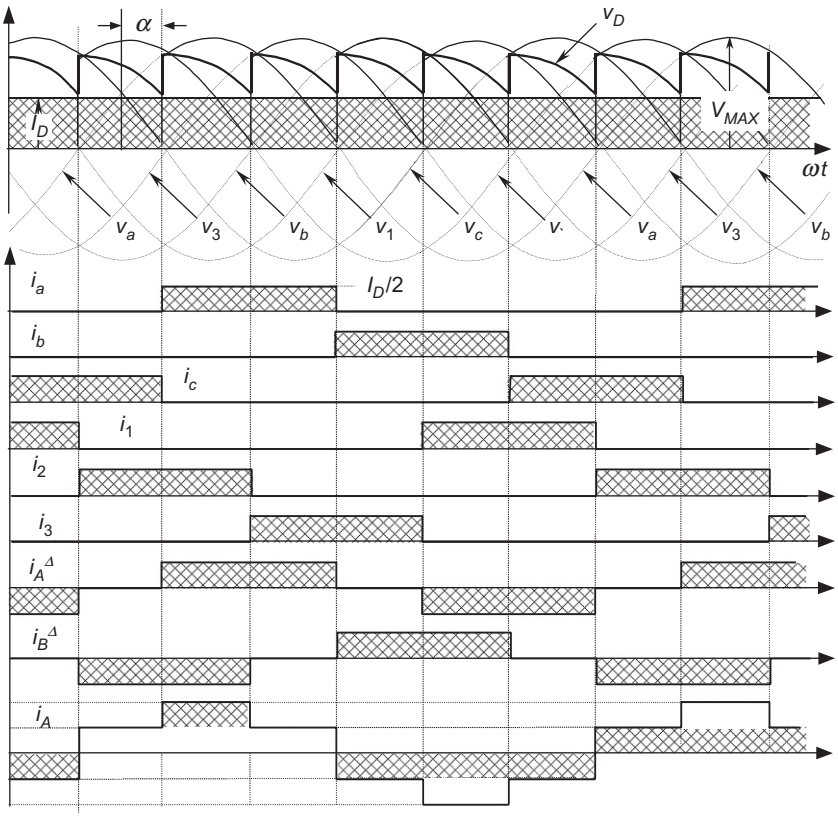


FIG. 9.11 *AC* current waveforms for the rectifier with interphase transformer.

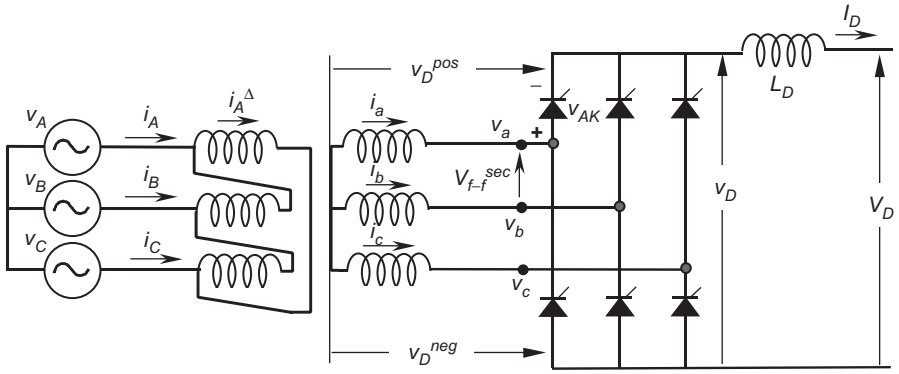


FIG. 9.12 Three-phase full-wave rectifier or Graetz bridge.

it can be seen that the three common cathode valves generate a positive voltage with respect to the neutral and the three common anode valves produce a negative voltage. The result is a *dc* voltage, twice the value of the half-wave rectifier. Each half of the bridge is a three-pulse converter group. This bridge connection is a two-way connection, and alternating currents flow in the valve-side transformer windings during both half periods, avoiding *dc* components into the windings and saturation in the transformer magnetic core. These characteristics make the so-called Graetz bridge the most widely used line-commutated thyristor rectifier. The configuration does not need any special transformer and works as a six-pulse rectifier. The series characteristic of this rectifier produces a *dc* voltage twice the value of the half-wave rectifier. The load average voltage is given by

$$V_D = \frac{2V_{MAX}}{\frac{2}{3}\pi} \int_{-\pi/3+\alpha}^{\pi/3+\alpha} \cos\omega t d(\omega t) = 2V_{MAX} \frac{\sin\frac{\pi}{3}}{\frac{\pi}{3}} \cos\alpha \approx 2.34 V_{f-N}^{rms} \cos\alpha \tag{9.12}$$

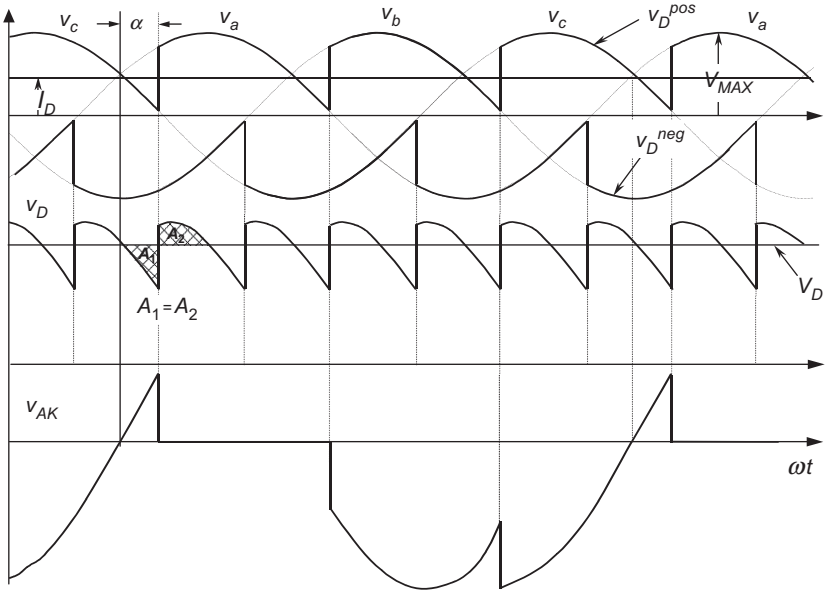


FIG. 9.13 Voltage waveforms for the Graetz bridge.

or

$$V_D = \frac{3\sqrt{2}V_{f-f}^{sec}}{\pi}\cos\alpha \approx 1.35V_{f-f}^{sec}\cos\alpha \qquad (9.13)$$

where V_{MAX} is the peak phase-to-neutral voltage at the secondary transformer terminals, V_{f-N}^{rms} its *rms* value, and V_{f-f}^{sec} the *rms* phase-to-phase secondary voltage at the valve terminals of the rectifier.

Fig. 9.13 shows the voltages of each half-wave bridge of this topology, v_D^{pos} and v_D^{neg}, the total instantaneous *dc* voltage v_D, and the anode-to-cathode voltage v_{AK} in one of the bridge thyristors. The maximum value of v_{AK} is $\sqrt{3}V_{MAX}$, which is the same as that of the half-wave converter and the interphase transformer rectifier. The double-star rectifier presents a maximum anode-to-cathode voltage of two times V_{MAX}. Fig. 9.14 shows the currents of the rectifier, which assumes that L_D is large enough to keep the *dc* current smooth. The example is for the same ΔY transformer connection shown in the topology of Fig. 9.9. It can be noted that the secondary currents do not carry any *dc* component, thereby avoiding overdesign of the windings and transformer saturation. These two figures have been drawn for a firing angle, α, of approximately 30 degrees. The perfect symmetry of the currents in all windings and lines is one of the reasons why this rectifier is the most popular of its type. The transformer rating in this case is

$$\begin{aligned} VA_{prim} &= 1.05P_D \\ VA_{sec} &= 1.05P_D \end{aligned} \qquad (9.14)$$

As can be noted, the transformer needs to be oversized only 5%, and both primary and secondary windings have the same rating. Again, this value can be compared with the previous rectifier transformers: $1.35P_D$ for the half-wave rectifier, $1.55P_D$ for the six-pulse rectifier, and $1.26P_D$ for the interphase transformer rectifier. The Graetz bridge makes excellent use of the power transformer.

9.2.5 Half Controlled Bridge Converter

The fully controlled three-phase bridge converter shown in Fig. 9.12 has six thyristors. As already explained here, this circuit operates as a rectifier when each thyristor has a firing angle $\alpha < 90$ degrees and functions as an inverter for $\alpha > 90$ degrees. If inverter operation is not required, the circuit may be simplified by replacing three controlled rectifiers with power diodes, as in Fig. 9.15A. This simplification is economically attractive because diodes are considerably less expensive than thyristors and they do not require firing angle control electronics.

The half-controlled bridge, or "semiconverter," is analyzed by considering it as a phase-controlled half-wave circuit in series with an uncontrolled half-wave rectifier. The average *dc* voltage is given by the following equation:

$$V_D = \frac{3\sqrt{2}V_{f-f}^{sec}}{2\pi}(1+\cos\alpha) \qquad (9.15)$$

Then, the average voltage V_D never reaches negative values. The output voltage waveforms of half-controlled bridge are similar to those of a fully controlled bridge with a freewheeling diode. The advantage of the freewheeling diode connection, shown in Fig. 9.15B, is that there is always a path for the *dc* current, independent of the status of the *ac* line and of the converter. This can be important if the load is inductive-resistive

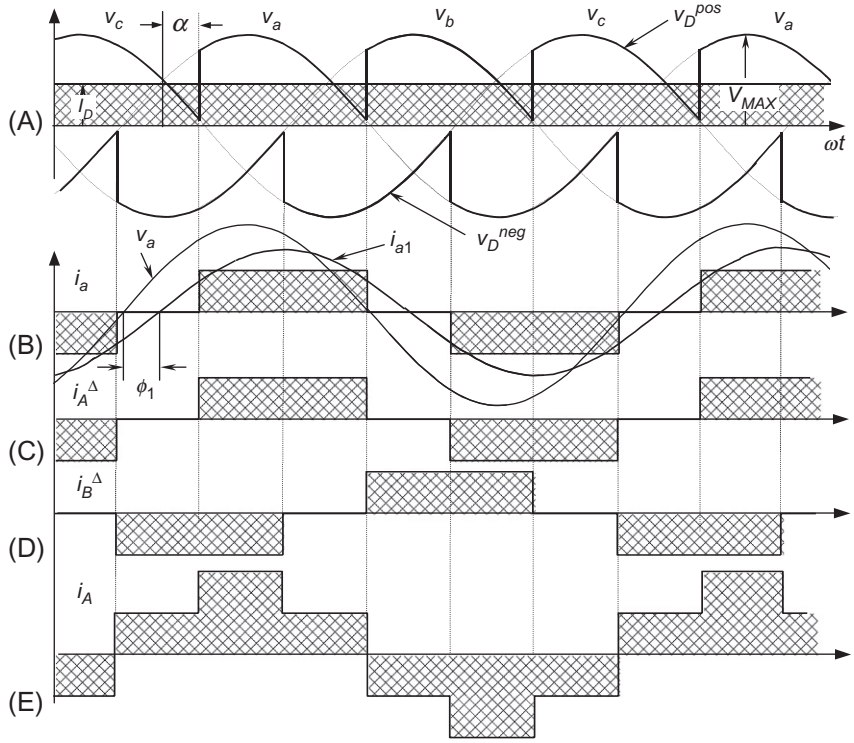


FIG. 9.14 Current waveforms for the Graetz bridge. (A) Output voltages for phases "*a*," "*b*," and "*c*"; (B) Phase "*a*" current, fundamental phase voltage, and current; (C) Phase "*b*" current; (D) Phase "*c*" current; (E) Line "*a*" current.

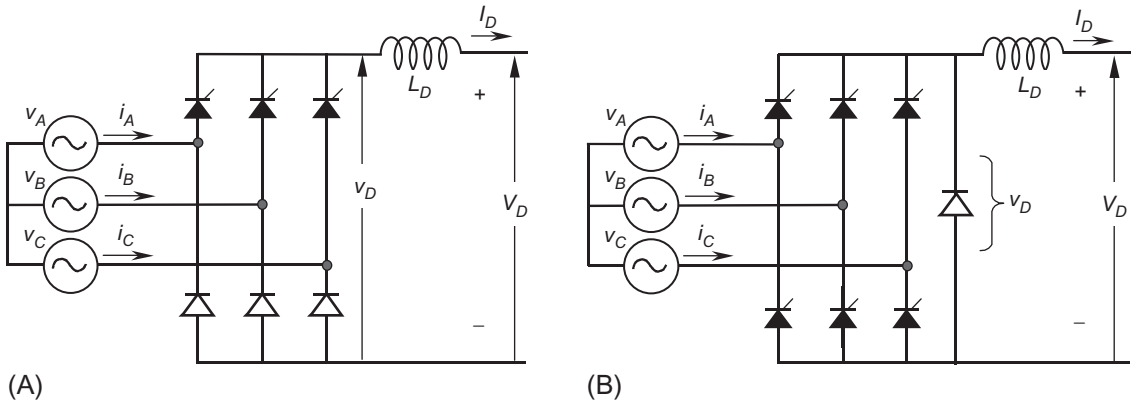


FIG. 9.15 One-quadrant bridge converter circuits: (A) half-controlled bridge and (B) freewheeling diode bridge.

with a large time constant and there is an interruption in one or more of the line phases. In such a case, the load current could commutate to the freewheeling diode.

9.2.6 Commutation

The description of the converters in the previous sections was based upon the assumption that the commutation was instantaneous. In practice, this is not possible, because the transfer of current between two consecutive valves in a commutation group takes a finite time. This time, called *overlap time*, depends on the phase-to-phase voltage between the valves participating in the commutation process and the line inductance L_S between the converter and power supply. During the overlap time, two valves conduct, and the phase-to-phase voltage drops entirely on the inductances L_S. Assuming the *dc* current I_D to be smooth and with the help of Fig. 9.16, the following relation is deduced:

$$2L_S\frac{di_{sc}}{dt} = \sqrt{2}V_{f-f}\sin\omega t = v_A - v_B \tag{9.16}$$

where i_{sc} is the current in the valve being fired during the commutation process (thyristor T2 in Fig. 9.16). This current can be evaluated, and it yields

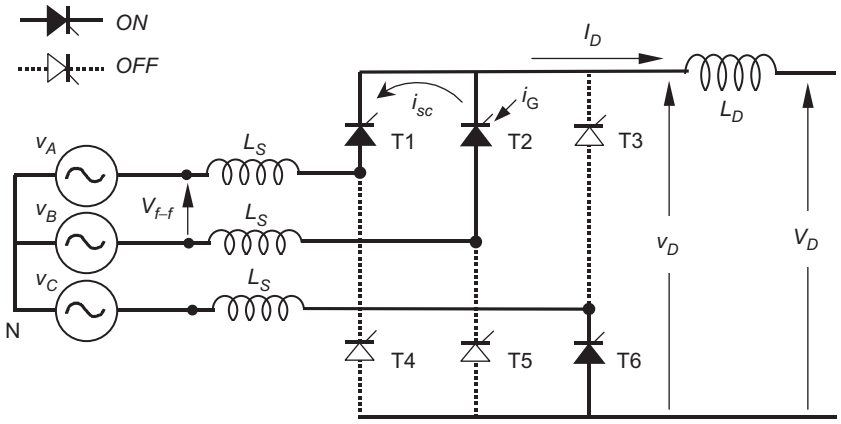


FIG. 9.16 Commutation process.

$$i_{sc} = -\frac{\sqrt{2}}{2L_S} V_{f-f} \frac{\cos \omega t}{\omega} + C \tag{9.17}$$

The constant "C" is evaluated through initial conditions at the instant when T2 is ignited. In terms of angle, when $\omega t = \alpha$,

$$\begin{aligned} &\text{when} \quad \omega t = \alpha, \quad i_{sc} = 0 \\ &\therefore C = \frac{V_{f-f}^{sec}}{\sqrt{2}\omega L_S} \cos \alpha \end{aligned} \tag{9.18}$$

Replacing Eq. (9.18) in (9.17),

$$i_{sc} = \frac{V_{f-f}}{\sqrt{2}\omega L_S} (\cos \alpha - \cos \omega t) \tag{9.19}$$

Before commutation, the current I_D was carried by thyristor T1 (see Fig. 9.16). During the commutation time, the load current I_D remains constant, i_{sc} returns through T1, and T1 is automatically switched off when the current i_{sc} reaches the value of I_D. This happens because thyristors cannot conduct in reverse direction. At this moment, the overlap time lasts, and the current I_D is then conducted by T2. In terms of angle, when $\omega t = \alpha + \mu$, $i_{sc} = I_D$, where μ is defined as the *overlap angle*. Replacing this final condition in Eq. (9.19) yields

$$I_D = \frac{V_{f-f}^{sec}}{\sqrt{2} \cdot \omega L_S} [\cos \alpha - \cos (\alpha + \mu)] \tag{9.20}$$

To avoid confusion in a real analysis, it has to be remembered that V_{f-f} corresponds to the secondary voltage in the case of transformer utilization. For this reason, the abbreviation "*sec*" has been added to the phase-to-phase voltage in Eq. (9.20).

During commutation, two valves conduct at a time, which means that there is an instantaneous short circuit between the two voltages participating in the process. As the inductances of each phase are the same, the current i_{sc} produces the same voltage drop in each L_S but with opposite sign because this current flows in reverse direction and with opposite slope in each inductance. The phase with the higher instantaneous voltage suffers a voltage drop $-\Delta v$, and the phase with the lower voltage suffers a voltage increase $+\Delta v$. This situation affects the *dc* voltage V_C, reducing its value an amount ΔV_{med}. Fig. 9.17 shows the meanings of Δv, ΔV_{med}, μ, and i_{sc}.

The area ΔV_{med} shown in Fig. 9.17 represents the loss of voltage that affects the average voltage V_C and can be evaluated through the integration of Δv during the overlap angle μ. The voltage drop Δv can be expressed as

$$\Delta v = \left(\frac{v_A - v_B}{2}\right) = \frac{\sqrt{2} V_{f-f}^{sec} \sin \omega t}{2} \tag{9.21}$$

Integrating Eq. (9.21) into the corresponding period (60 degrees) and interval (μ) and starting at the instant when the commutation begins (α),

$$\Delta V_{med} = \frac{3}{\pi} \frac{1}{2} \int_{\alpha}^{\alpha+\mu} \sqrt{2} V_{f-f}^{sec} \sin \omega t \, d\omega t \tag{9.22}$$

$$\Delta V_{med} = \frac{3}{\pi} \frac{V_{f-f}^{sec}}{\sqrt{2}} [\cos \alpha - \cos (\alpha + \mu)] \tag{9.23}$$

Subtracting ΔV_{med} in Eq. (9.13),

$$V_D = \frac{3\sqrt{2} V_{f-f}^{sec}}{\pi} \cos \alpha - \Delta V_{med} \tag{9.24}$$

$$V_D = \frac{3\sqrt{2} V_{f-f}^{sec}}{2\pi} [\cos \alpha + \cos (\alpha + \mu)] \tag{9.25}$$

or

$$V_D = \frac{3\sqrt{2} V_{f-f}^{sec}}{\pi} \left[\cos \left(\alpha + \frac{\mu}{2}\right) \cos \frac{\mu}{2}\right] \tag{9.26}$$

Eqs. (9.20), (9.25) can be written as a function of the primary winding of the transformer, if there is any transformer:

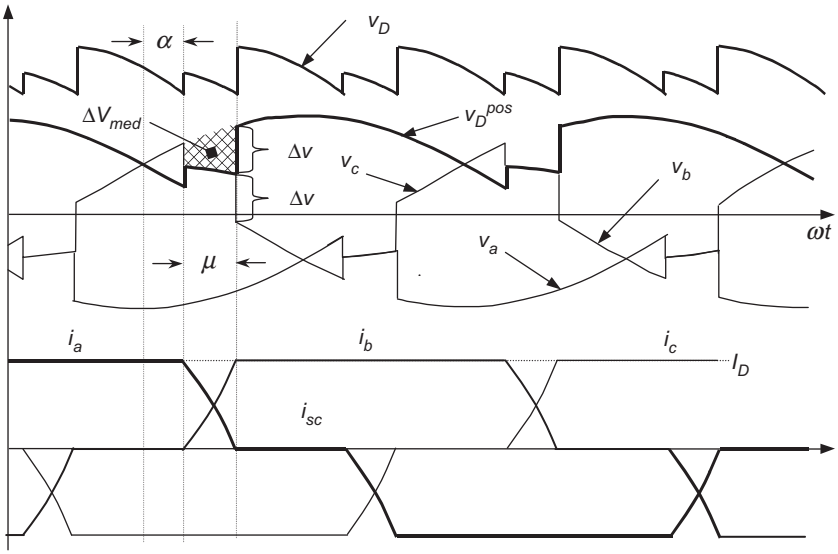


FIG. 9.17 Effect of the overlap angle on the voltages and currents.

$$I_D = \frac{aV_{f-f}^{prim}}{\sqrt{2}\omega L_S}[\cos\alpha - \cos(\alpha+\mu)] \tag{9.27}$$

$$V_D = \frac{3\sqrt{2}aV_{f-f}^{prim}}{2\pi}[\cos\alpha + \cos(\alpha+\mu)] \tag{9.28}$$

where $a = V_{f-f}^{sec}/V_{f-f}^{prim}$. With Eqs. (9.27), (9.28), one gets

$$V_D = \frac{3\sqrt{2}}{\pi}aV_{f-f}^{prim}\cos\alpha - \frac{3I_D\omega L_S}{\pi} \tag{9.29}$$

Eq. (9.29) allows a very simple equivalent circuit of the converter to be made, as shown in Fig. 9.18. It is important to note that the equivalent resistance of this circuit is not real, because it does not dissipate power.

From the equivalent circuit, regulation curves for the rectifier under different firing angles are shown in Fig. 9.19. It should be noted that these curves correspond only to an ideal situation but help in understanding the effect of voltage drop Δv on *dc* voltage. The commutation process and the overlap angle also affect the voltage v_a and anode-to-cathode thyristor voltage, as shown in Fig. 9.20.

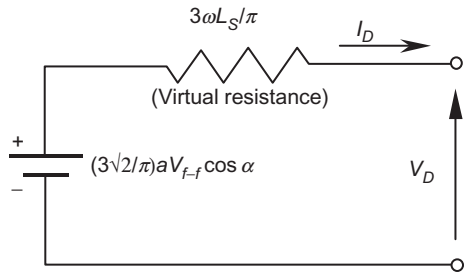


FIG. 9.18 Equivalent circuit for the converter.

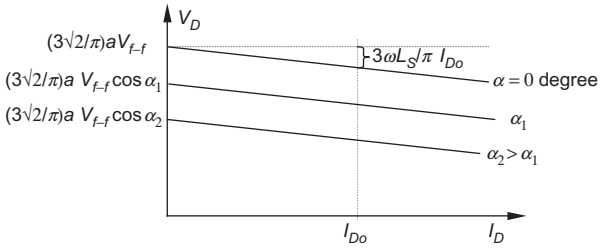


FIG. 9.19 *DC* voltage regulation curves for rectifier operation.

9.2.7 Power Factor

The displacement factor of the fundamental current, obtained from Fig. 9.14, is

$$\cos\phi_1 = \cos\alpha \tag{9.30}$$

In the case of nonsinusoidal current, the active power delivered per phase by the sinusoidal supply is

$$P = \frac{1}{T}\int_0^T v_a(t)i_a(t)dt = V_a^{rms}I_{a1}^{rms}\cos\phi_1 \tag{9.31}$$

where V_a^{rms} is the *rms* value of the voltage v_a and I_{a1}^{rms} the *rms* value of i_{a1} (fundamental component of i_a). Analog relations can be obtained for v_b and v_c.

The apparent power per phase is given by

$$S = V_a^{rms}I_a^{rms} \tag{9.32}$$

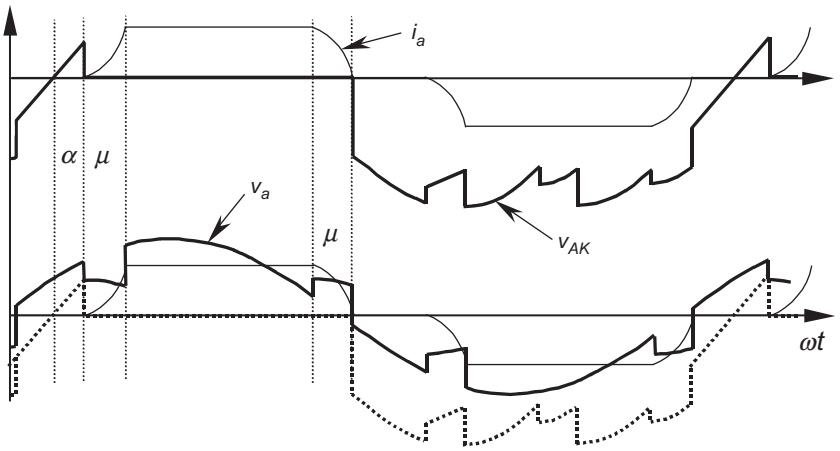


FIG. 9.20 Effect of the overlap angle on v_a and on thyristor voltage v_{AK}.

The power factor is defined by

$$PF = \frac{P}{S} \tag{9.33}$$

By substituting Eqs. (9.30)–(9.32) into Eq. (9.33), the power factor can be expressed as follows:

$$PF = \frac{I_{a1}^{rms}}{I_a^{rms}} \cos\alpha \tag{9.34}$$

This equation shows clearly that due to the nonsinusoidal waveform of the currents, the power factor of the rectifier is negatively affected by both the firing angle α and the distortion of the input current. In effect, an increase in the distortion of the current produces an increase in the value of I_a^{rms} in Eq. (9.34), which deteriorates the power factor.

9.2.8 Harmonic Distortion

The currents of the line-commutated rectifiers are far from being sinusoidal. For example, the currents generated from the Graetz rectifier (see Fig. 9.14B) have the following harmonic content:

$$i_A = \frac{2\sqrt{3}}{\pi} I_D \left(\cos\omega t - \frac{1}{5}\cos 5\omega t + \frac{1}{7}\cos 7\omega t - \frac{1}{11}\cos 11\omega t + \ldots \right) \tag{9.35}$$

Some of the characteristics of the currents, obtained from Eq. (9.35), include (i) the absence of triple harmonics, (ii) the presence of harmonics of order $6k \pm 1$ for integer values of k, (iii) those harmonics of orders $6k+1$ that are of positive sequence, (iv) those of orders $6k-1$ that are of negative sequence, (v) the *rms* magnitude of the fundamental frequency that is

$$I_1 = \frac{\sqrt{6}}{\pi} I_D \tag{9.36}$$

and (vi) the *rms* magnitude of the nth harmonic that is

$$I_n = \frac{I_1}{n} \tag{9.37}$$

If either the primary or the secondary three-phase windings of the rectifier transformer are connected in delta, the *ac* side current waveforms consist of the instantaneous differences between two rectangular secondary currents 120e apart as shown in Fig. 9.14E. The resulting Fourier series for the current in phase "a" on the primary side is

$$i_A = \frac{2\sqrt{3}}{\pi} I_D \left(\cos\omega t + \frac{1}{5}\cos 5\omega t - \frac{1}{7}\cos 7\omega t - \frac{1}{11}\cos 11\omega t + \ldots \right) \tag{9.38}$$

This series differs from that of a star-connected transformer only by the sequence of rotation of harmonic orders $6k \pm 1$ for odd values of k, that is, the 5th, 7th, 17th, and 19th.

9.2.9 Special Configurations for Harmonic Reduction

A common solution for harmonic reduction is through the connection of passive filters, which are tuned to trap a particular harmonic frequency. A typical configuration is shown in Fig. 9.21.

However, harmonics also can be eliminated using special configurations of converters. For example, 12-pulse configuration consists of 2 sets of converters connected as shown in Fig. 9.22. The resultant *ac* current is given by the sum of the two Fourier series of the star connection (Eq. 9.35) and delta connection transformers (Eq. 9.38):

$$i_A = 2\left(\frac{2\sqrt{3}}{\pi}\right) I_D\left(\cos\omega t - \frac{1}{11}\cos 11\omega t + \frac{1}{13}\cos 13\omega t - \frac{1}{23}\cos 23\omega t + \ldots\right) \tag{9.39}$$

The series only contains harmonics of order $12k \pm 1$. The harmonic currents of orders $6k \pm 1$ (with k odd), that is, 5th, 7th, 17th, and 19th, circulate between the two converter transformers but do not penetrate the *ac* network.

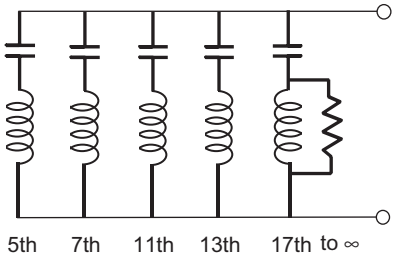


FIG. 9.21 Typical passive filter for one phase.

The resulting line current for the 12-pulse rectifier, shown in Fig. 9.23, is closer to a sinusoidal waveform than previous line currents. The instantaneous *dc* voltage is also smoother with this connection.

Higher-pulse configuration using the same principle is also possible. The 12-pulse rectifier was obtained with a 30 degrees phase shift between the two secondary transformers. The addition of further, appropriately shifted, transformers in parallel provides the basis for increasing pulse configurations. For instance, 24-pulse operation is achieved by means of 4 transformers with 15 degrees phase shift, and 48-pulse operation requires 8 transformers with 7.5 degrees phase shift (transformer connections in zigzag configuration).

Although theoretically possible, pulse numbers above 48 are rarely justified due to the practical levels of distortion found in the supply voltage waveforms. Further, the converter topology becomes more and more complicated.

An ingenious and very simple way to reach high-pulse operation is shown in Fig. 9.24. This configuration is called *dc* ripple reinjection. It consists of two parallel converters connected to the load through a multistep reactor. The reactor

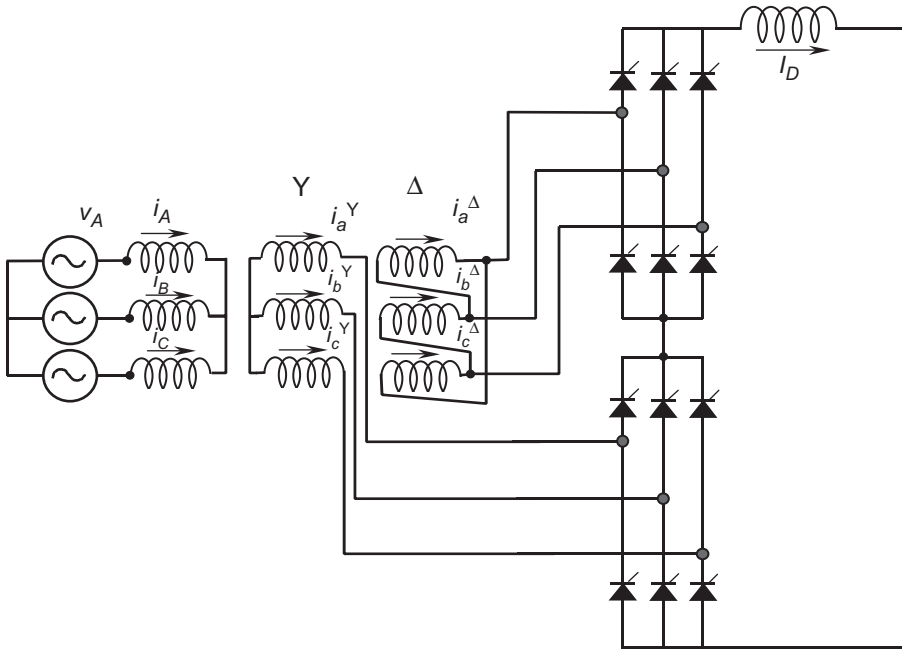


FIG. 9.22 Twelve-pulse rectifier configuration.

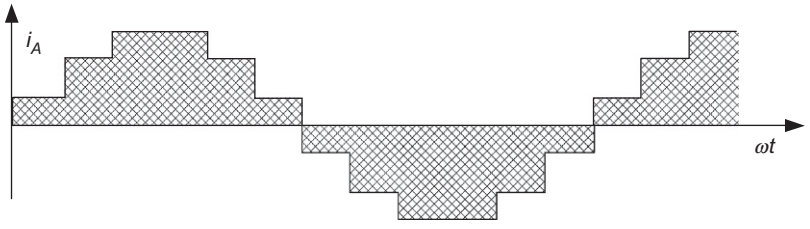


FIG. 9.23 Line current for the 12-pulse rectifier.

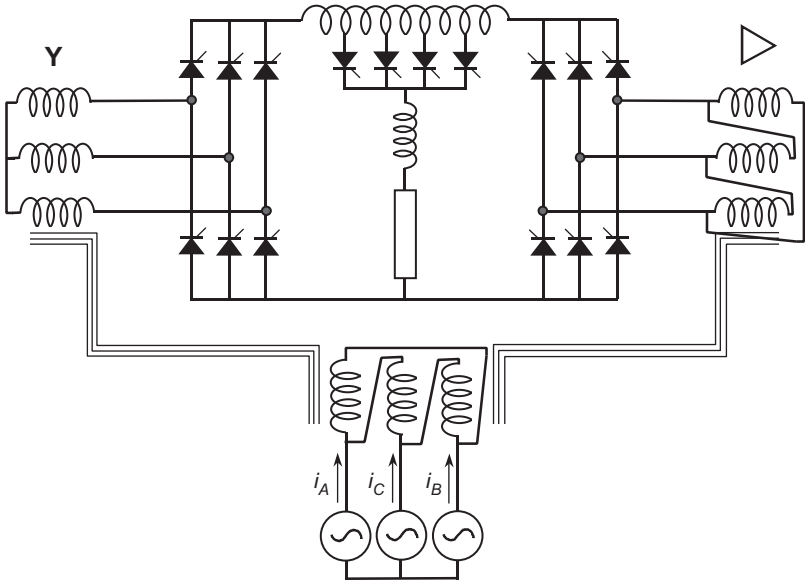


FIG. 9.24 *DC* ripple reinjection technique for 48-pulse operation.

uses a chain of thyristor-controlled taps, which are connected to symmetrical points of the reactor. By firing the thyristors located at the reactor at the right time, high-pulse operation is reached. The level of pulse operation depends on the number of thyristors connected to the reactor. They multiply the basic level of operation of the two converters. The example in Fig. 9.24 shows a 48-pulse configuration, obtained by the multiplication of basic 12-pulse operation by 4 reactor thyristors. This technique also can be applied to series-connected bridges.

Another solution for harmonic reduction is the utilization of active power filters. Active power filters are special pulse-width modulated (PWM) converters, able to generate the harmonics the converter requires. Fig. 9.25 shows a current-controlled shunt active power filter.

9.2.10 Applications of Line-Commutated Rectifiers in Machine Drives

Important applications for line-commutated three-phase controlled rectifiers are found in machine drives. Fig. 9.26 shows a *dc* machine control implemented with a six-pulse rectifier. Torque and speed are controlled through the armature current I_D and excitation current I_{exc}. Current I_D is adjusted with V_D, which is controlled by the firing angle α through Eq. (9.12). This *dc* drive can operate in two quadrants: positive and negative *dc* voltage. This two-quadrant operation allows regenerative braking when $\alpha > 90$ degrees and $I_{exc} < 0$.

The converter of Fig. 9.26 can also be used to control synchronous machines, as shown in Fig. 9.27. In this case, a second converter working in the inverting mode operates the machine as self-controlled synchronous motor. With this second converter, the synchronous motor behaves like a *dc* motor but has none of the disadvantages of mechanical commutation. This converter is not line commutated, but machine commutated.

The nominal synchronous speed of the motor on a 50 or 60 Hz *ac* supply is now meaningless, and the upper speed limit is determined by the mechanical limitations of the rotor construction. There is disadvantage that the rotational *emfs* required for load commutation of the machine side converter are not available at standstill and low speeds. In such a case, auxiliary force-commutated circuits must be used.

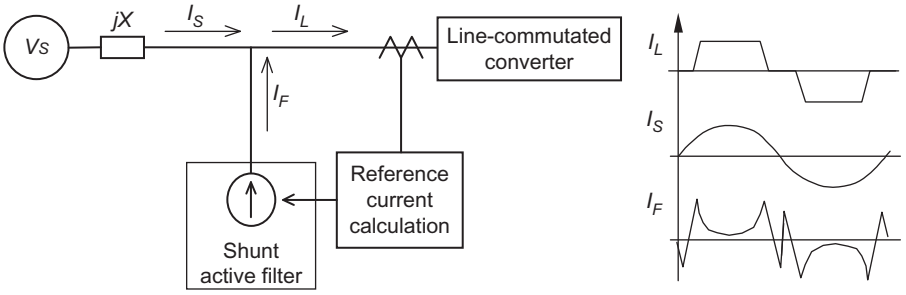


FIG. 9.25 Current-controlled shunt active power filter.

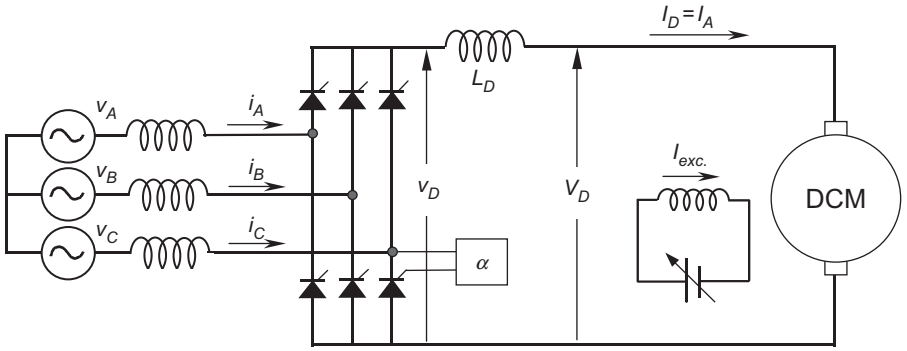


FIG. 9.26 *DC* machine drive with a six-pulse rectifier.

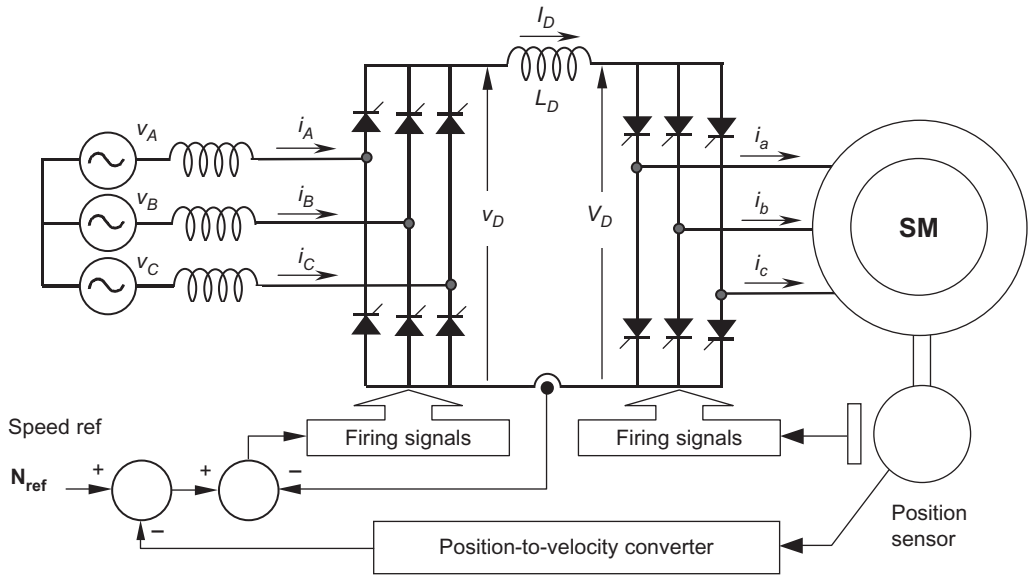


FIG. 9.27 Self-controlled synchronous motor drive.

The line-commutated rectifier controls the torque of the machine through firing angle a. This approach gives direct torque control of the commutatorless motor and is analogous to the use of armature current control shown in Fig. 9.26 for the converter-fed *dc* motor drive.

Line-commutated rectifiers are also used for speed control of wound rotor induction motors. Subsynchronous and supersynchronous static converter cascades using a naturally commutated *dc* link converter can be implemented. Fig. 9.28 shows a supersynchronous cascade for a wound rotor induction motor, using a naturally commutated *dc* link converter.

In the supersynchronous cascade shown in Fig. 9.28, the right-hand bridge operates at slip frequency as a rectifier or inverter, while the other operates at network frequency as an inverter or rectifier. Control is difficult near synchronism when slip frequency *emfs* are insufficient for natural commutation and special circuit configuration employing forced commutation or devices with a self-turn-off capability are necessary for the passage through synchronism. This kind of supersynchronous cascade works better with cycloconverters.

9.2.11 Applications in HVDC Power Transmission

High-voltage direct-current (HVDC) power transmission is the most powerful application for line-commutated converters that exist today. There are power converters with ratings in excess of 1000 MW. Series operation of hundreds of valves can be found in some HVDC systems. In high-power and long-distance applications, these systems become more economical than conventional *ac* systems. They also have some other advantages compared with *ac* systems:

1. They can link two *ac* systems operating unsynchronized or with different nominal frequencies, that is, $50 \leftrightarrow 60$ Hz.

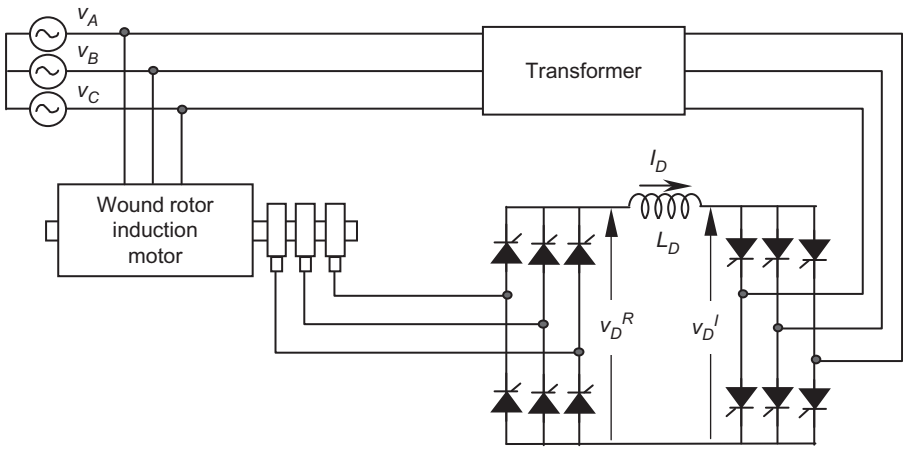


FIG. 9.28 Supersynchronous cascade for a wound rotor induction motor.

2. They can help in stability problems related with subsynchronous resonance in long *ac* lines.
3. They have very good dynamic behavior and can interrupt short-circuit problems very quickly.
4. If transmission is by submarine or underground cable, it is not practical to consider *ac* cable systems exceeding 50 km, but *dc* cable transmission systems are in service whose length is in hundreds of kilometers and even distances of 600 km or greater have been considered feasible.
5. Reversal of power can be controlled electronically by means of the delay firing angles a.
6. Some existing overhead *ac* transmission lines cannot be increased. If overbuilt with or upgraded to *dc* transmission, it can substantially increase the power transfer capability on the existing right-of-way.

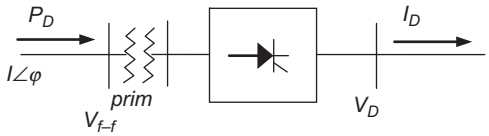
The use of HVDC systems for interconnections of asynchronous systems is an interesting application. Some continental electric power systems consist of asynchronous networks such as those for the East, West, Texas, and Quebec networks in North America, and island loads such as that for the island of Gotland in the Baltic Sea make good use of the HVDC interconnections.

Nearly all HVDC power converters with thyristor valves are assembled in a converter bridge of 12-pulse configuration, as shown in Fig. 9.29. Consequently, the *ac* voltages applied to each 6-pulse valve group that makes up the 12-pulse valve group have a phase difference of 30 degrees that is utilized to cancel the *ac* side, 5th and 7th harmonic currents, and *dc* side, 6th harmonic voltage, thus resulting in a significant saving in harmonic filters.

Some useful relations for HVDC systems include the following:

(a) Rectifier side

$$P_D = V_D I_D = \sqrt{3} V_{f-f}^{prim} I_{line}^{rms} \cos\varphi \tag{9.40}$$



$$I_P = I\cos\varphi$$

$$I_Q = I\sin\varphi \tag{9.41}$$

$$\therefore P_D = V_D I_D = \sqrt{3} V_{f-f}^{prim} I_P$$

$$I_P = \frac{V_D I_D}{\sqrt{3} V_{f-f}^{prim}} \tag{9.42}$$

$$I_P = \frac{a^2\sqrt{3} V_{f-f}^{prim}}{4\pi\omega L_S}[\cos 2\alpha - \cos 2(\alpha+\mu)] \tag{9.43}$$

$$I_Q = \frac{a^2\sqrt{3} V_{f-f}^{prim}}{4\pi\omega L_S}[\sin 2(\alpha+\mu) - \sin 2\alpha - 2\mu] \tag{9.44}$$

$$I_P = I_D \frac{a\sqrt{6}}{\pi}\left[\frac{\cos\alpha + \cos(\alpha+\mu)}{2}\right] \tag{9.45}$$

Fundamental secondary component of I

$$I = \frac{a\sqrt{6}}{\pi} I_D \tag{9.46}$$

Replacing Eq. (9.46) in (9.45),

$$I_P = I\left[\frac{\cos\alpha + \cos(\alpha+\mu)}{2}\right] \tag{9.47}$$

As $I_p = I\cos\varphi$, it yields Fig. 9.30A:

$$\cos\varphi = \left[\frac{\cos\alpha + \cos(\alpha+\mu)}{2}\right] \tag{9.48}$$

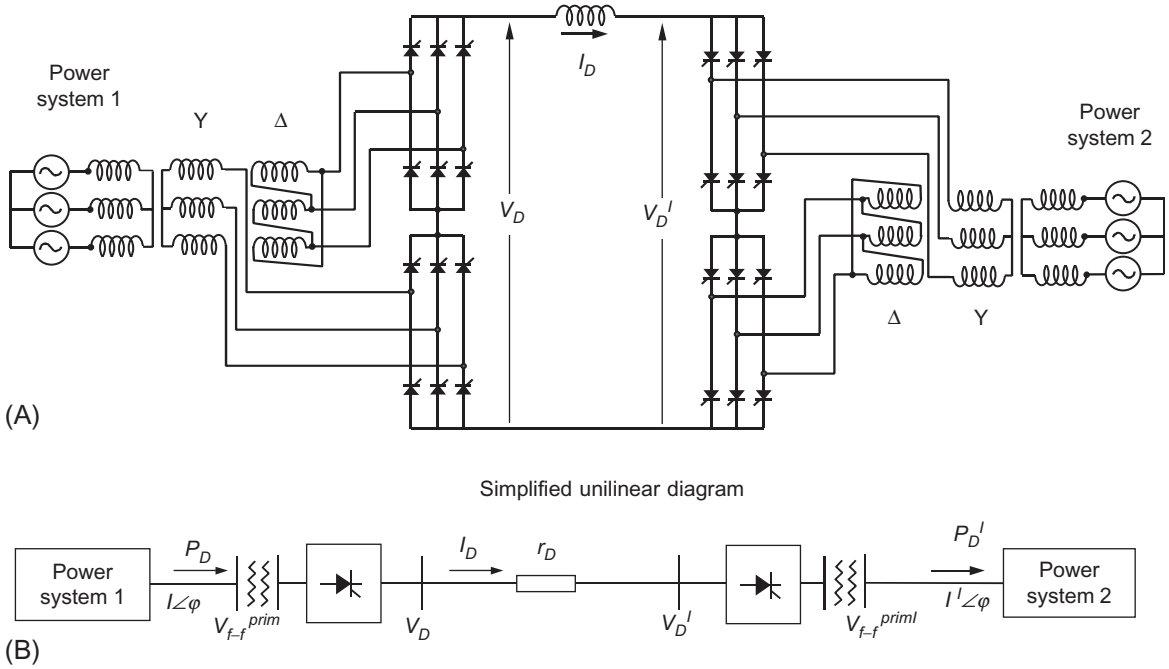


FIG. 9.29 Typical HVDC power system: (A) detailed circuit and (B) unilinear diagram.

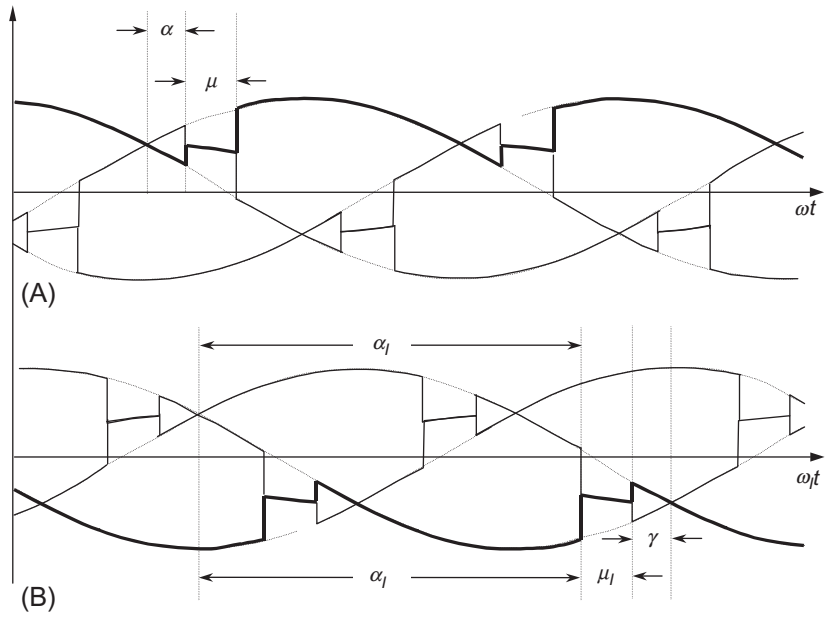


FIG. 9.30 Definition of angle γ for inverter side: (A) rectifier side and (B) inverter side.

(b) Inverter side

The same equations are applied for the inverter side, but the firing angle α is replaced by γ, where γ is

$$\gamma = 180 \text{ degrees} - (\alpha + \mu) \tag{9.49}$$

As reactive power always goes in the converter direction, Eq. (9.44) for inverter side becomes (Fig. 9.30B)

$$I_{QI} = -\frac{a_I^2\sqrt{3}V_{f-f_I}^{prim}}{4\pi\omega_I L_I}[\sin 2(\gamma + \mu_I) - \sin 2\gamma - 2\mu_I] \tag{9.50}$$

9.2.12 Dual Converters

In many variable-speed drives, four-quadrant operation is required, and three-phase dual converters are extensively used in applications up to 2 MW level. Fig. 9.31 shows a three-phase dual converter, where two converters are connected back-to-back.

In the dual converter, one rectifier provides the positive current to the load and the other the negative current. Due to the instantaneous voltage differences between the output voltages of the converters, a circulating current flows through the bridges. The circulating current is normally limited by circulating reactor, L_D, as shown in Fig. 9.31. The two converters are controlled in such a way that if α^+ is the delay angle of the positive current converter, the delay angle of the negative current converter is $\alpha^- = 180 \text{ degrees} - \alpha^+$.

Fig. 9.32 shows the instantaneous *dc* voltages of each converter, v_D^+ and v_D^-. Despite the average voltage V_D is the same in both the converters, their instantaneous voltage differences shown as voltage v_r are producing the circulating current i_r, which is superimposed with the load currents i_D^+ and i_D^-.

To avoid the circulating current i_r, it is possible to implement a "circulating current-free" converter if a dead time of a few milliseconds is acceptable. The converter section, not required to supply current, remains fully blocked. When a current reversal is required, a logic switchover system determines at first the instant at which the conducting converter's current becomes zero. This converter section is then blocked, and the further supply of gating pulses to it is prevented. After a short safety

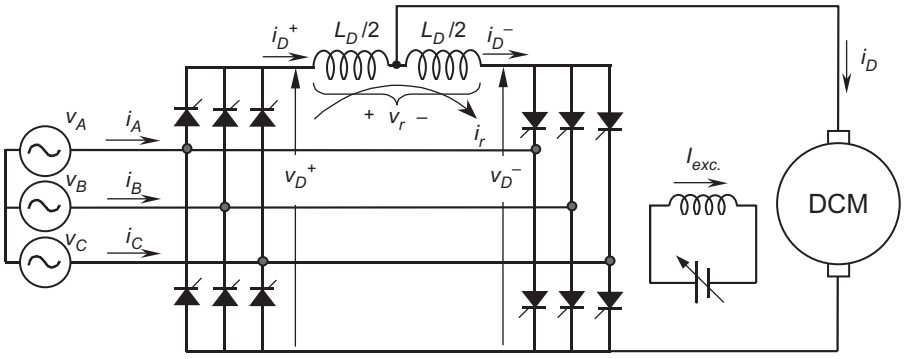


FIG. 9.31 Dual converter in a four-quadrant *dc* drive.

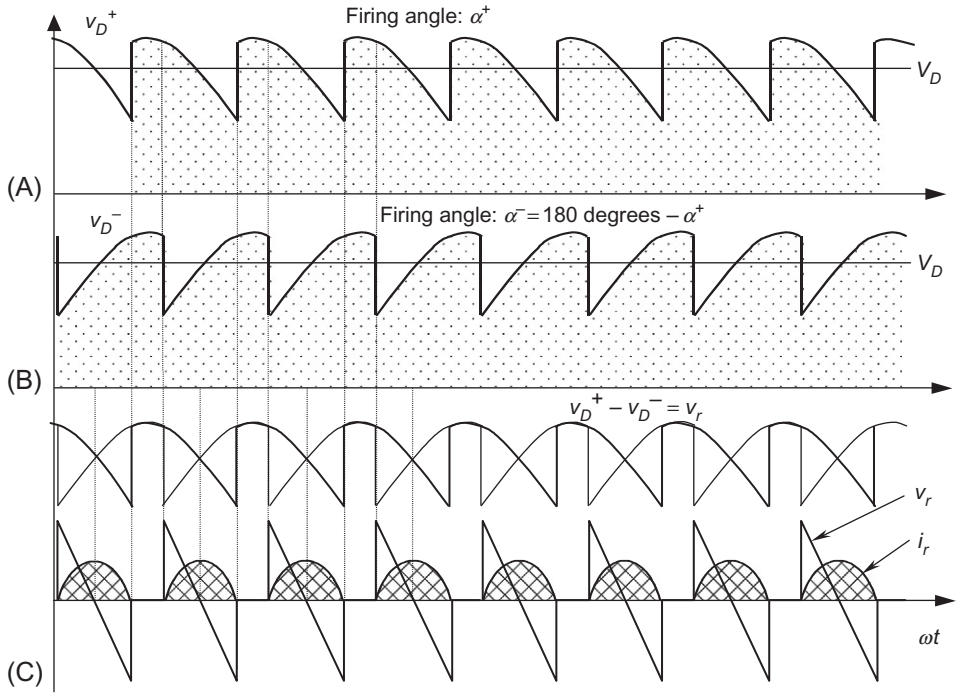


FIG. 9.32 Waveform of circulating current: (A) instantaneous *dc* voltage from positive converter; (C) instantaneous *dc* voltage from negative converter; and (C) voltage difference between v_D^+ and v_D^-, v_r, and circulating current i_r.

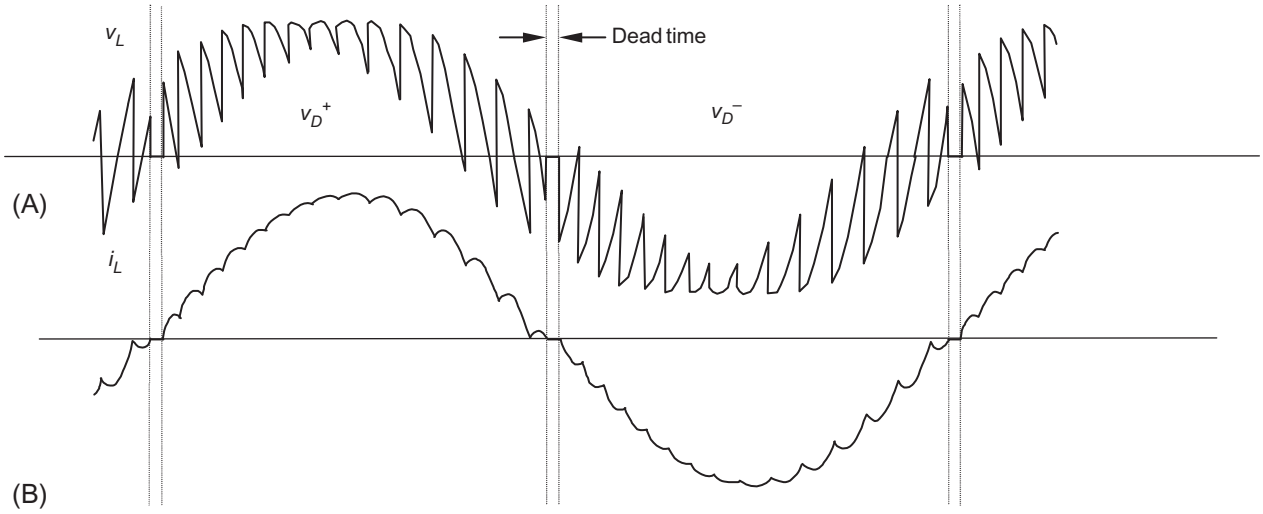


FIG. 9.33 Cycloconverter operation: (A) voltage waveform and (B) current waveform for inductive load.

interval (dead time), the gating pulses for the other converter section are released.

9.2.13 Cycloconverters

A different principle of frequency conversion is derived from the fact that a dual converter is able to supply an *ac* load with a lower frequency than the system frequency. If the control signal of the dual converter is a function of time, the output voltage will follow this signal. If this control signal value alters sinusoidally with the desired frequency, then the waveform depicted in Fig. 9.33A consists of a single-phase voltage with a large harmonic current. As shown in Fig. 9.33B, if the load is inductive, the current will present less distortion than voltage.

The cycloconverter operates in all four quadrants during a period. A pause (dead time) at least as small as the time required by the switchover logic occurs after the current reaches zero, that is, between the transfer to operation in the quadrant corresponding to the other direction of current flow.

Three single-phase cycloconverters may be combined to build a three-phase cycloconverter. The three-phase cycloconverters find an application in low-frequency, high-power requirements. Control speed of large synchronous motors in the low-speed range is one of the most common applications of three-phase cycloconverters. Fig. 9.34 is a diagram for this application. They are also used to control slip frequency in wound rotor induction machines, for supersynchronous cascade (Scherbius system).

9.2.14 Harmonic Standards and Recommended Practices

In view of the proliferation of the power converter equipment connected to the utility system, various national and international agencies have been considering limits on harmonic current injection to maintain good power quality. As a consequence, various standards and guidelines have been established that specify limits on the magnitudes of harmonic currents and harmonic voltages.

The Comité Européen de Normalisation Electrotechnique (CENELEC), International Electrotechnical Commission (IEC), and West German Standards (VDE) specify the limits on the voltages (as a percentage of the nominal voltage) at various harmonic frequencies of the utility frequency, when the equipment-generated harmonic currents are injected into a network whose impedances are specified.

According to the Institute of Electrical and Electronics Engineers-519 standards (IEEE), Table 9.1 lists the limits on the harmonic currents that a user of power electronics equipment and other nonlinear loads is allowed to inject into the utility system. Table 9.2 lists the quality of voltage that the utility can furnish the user.

In Table 9.1, the values are given at the point of connection of nonlinear loads. The *THD* is the total harmonic distortion given by Eq. (9.51), and h is the number of the harmonic:

$$THD = \frac{\sqrt{\sum_{h=2}^{\infty} I_h^2}}{I_1} \tag{9.51}$$

The total current harmonic distortion allowed in Table 9.1 increases with the value of short-circuit current.

The total harmonic distortion in the voltage can be calculated in a manner similar to that given by Eq. (9.51). Table 9.2 specifies the individual harmonics and the *THD* limits on the voltage that the utility supplies to the user at the connection point.

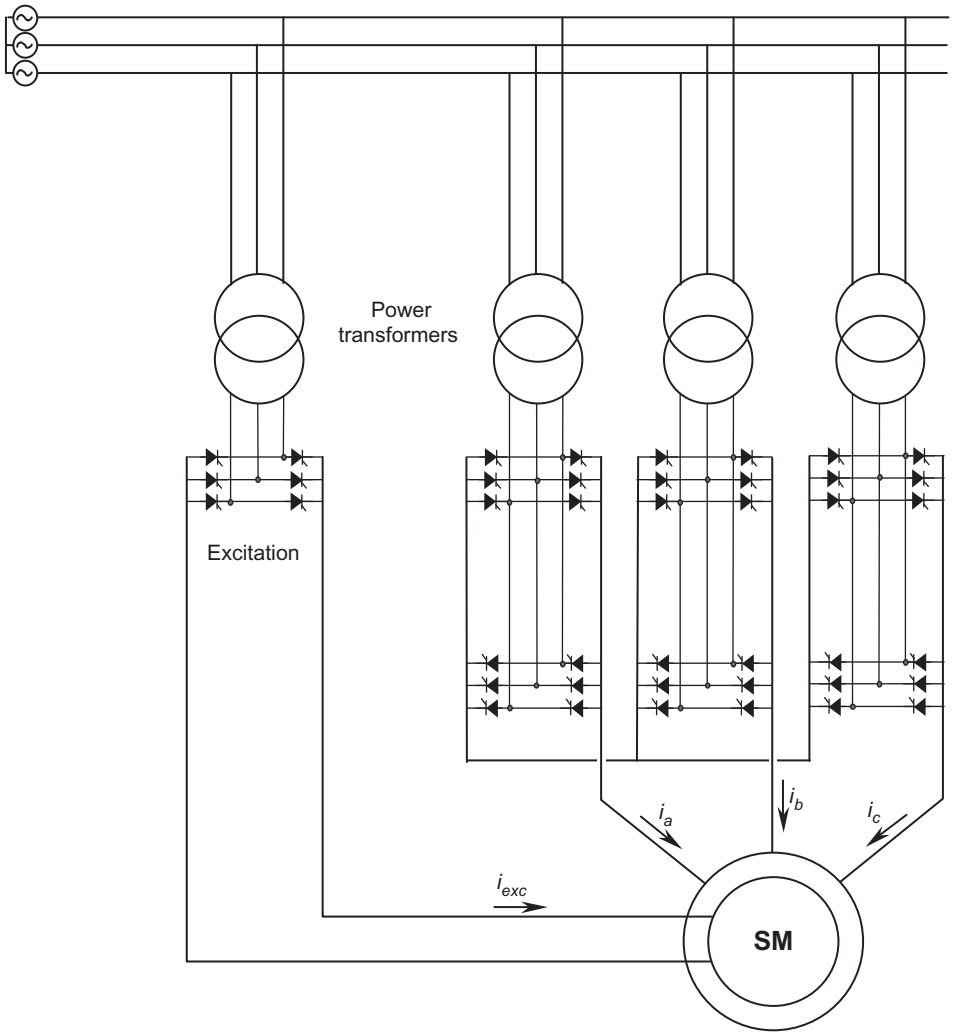


FIG. 9.34 Synchronous machine drive with a cycloconverter.

TABLE 9.1 Harmonic current limits in percent of fundamental

Short-circuit current (p.u.)	$h<11$	$11<h<17$	$17<h<23$	$23<h<35$	$35<h$	THD
<20	4.0	2.0	1.5	0.6	0.3	5.0
20–50	7.0	3.5	2.5	1.0	0.5	8.0
50–100	10.0	4.5	4.0	1.5	0.7	12.0
100–1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

TABLE 9.2 Harmonic voltage limits in percent of fundamental

Voltage level	2.3–69 kV	69–138 kV	>138 kV
Maximum for individual harmonic	3.0	1.5	1.0
Total harmonic distortion (*THD*)	5.0	2.5	1.5

9.3 Force-Commutated Three-Phase Controlled Rectifiers

9.3.1 Basic Topologies and Characteristics

Force-commutated rectifiers are built with semiconductors with gate-turn-off capability. The gate-turn-off capability allows full control of the converter, because valves can be

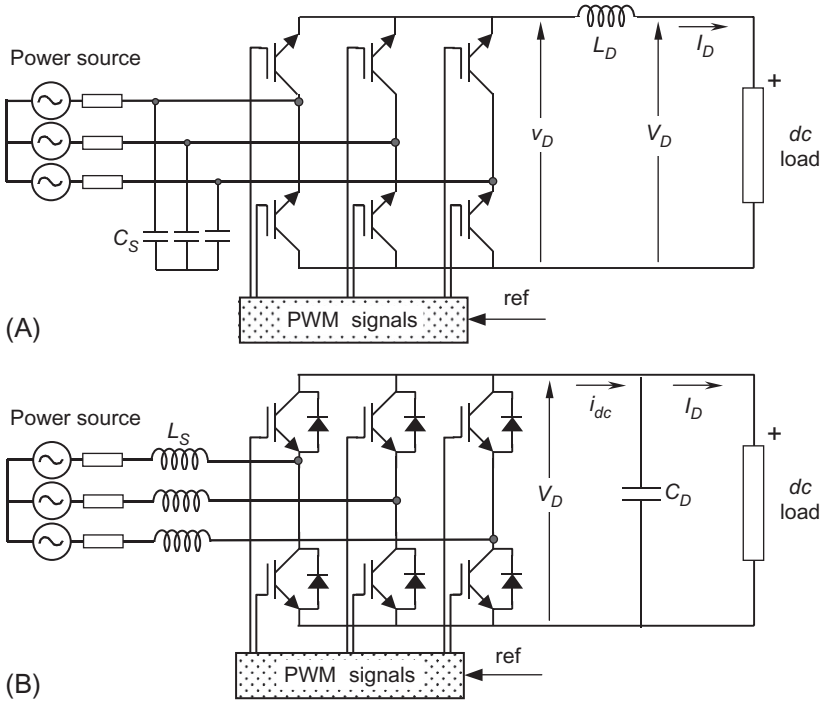


FIG. 9.35 Basic topologies for force-commutated PWM rectifiers: (A) current-source rectifier and (B) voltage-source rectifier.

switched *ON* and *OFF* whenever is required. This allows the commutation of the valves, hundreds of times in one period that is not possible with line-commutated rectifiers, where thyristors are switched *ON* and *OFF* only once a cycle. This feature has the following advantages: (a) The current or voltage can be modulated (PWM), generating less harmonic contamination; (b) power factor can be controlled and even it can be made leading; (c) they can be built as voltage-source or current-source rectifiers; and (d) the reversal of power in thyristor rectifiers is by reversal of voltage at the *dc* link. Instead, force-commutated rectifiers can be implemented for both, reversal of voltage or reversal of current.

There are two ways to implement force-commutated three-phase rectifiers: (A) as a current-source rectifier, where power reversal is by *dc* voltage reversal, and (B) as a voltage-source rectifier, where power reversal is by current reversal at the *dc* link. Fig. 9.35 shows the basic circuits for these two topologies.

9.3.2 Operation of the Voltage Source Rectifier

The voltage-source rectifier is by far the most widely used, and because of the duality of the two topologies shown in Fig. 9.35, only this type of force-commutated rectifier will be explained in detail.

The voltage-source rectifier operates by keeping the *dc* link voltage at a desired reference value, using a feedback control loop as shown in Fig. 9.36. To accomplish this task, the *dc* link voltage is measured and compared with a reference V_{REF}. The error signal generated from this comparison is used to switch the six valves of the rectifier *ON* and *OFF*. In this way, power can come or return to the *ac* source according to the *dc* link voltage requirements. The voltage V_D is measured at the capacitor C_D.

When the current I_D is positive (rectifier operation), the capacitor C_D is discharged, and the error signal asks the control block for more power from the *ac* supply. The control block takes the power from the supply by generating the appropriate PWM signals for the six valves. In this way, more current flows from the *ac* to the *dc* side, and the capacitor voltage is recovered. Inversely, when I_D becomes negative (inverter operation), the capacitor C_D is overcharged, and the error signal asks the control to discharge the capacitor and return power to the *ac* mains.

The PWM control can manage not only the active power but also the reactive power, allowing this type of rectifier to correct power factor. In addition, the *ac* current waveforms can be maintained as almost sinusoidal, which reduces harmonic contamination to the mains supply.

The PWM consists of switching the valves *ON* and *OFF*, following a preestablished template. This template could be a sinusoidal waveform of voltage or current. For example, the modulation of one phase could be as the one shown in Fig. 9.37. This PWM pattern is a periodical waveform whose fundamental is a voltage with the same frequency of the template. The amplitude of this fundamental, called V_{MOD} in Fig. 9.37, is also proportional to the amplitude of the template.

To make the rectifier work properly, the PWM pattern must generate a fundamental V_{MOD} with the same frequency as the

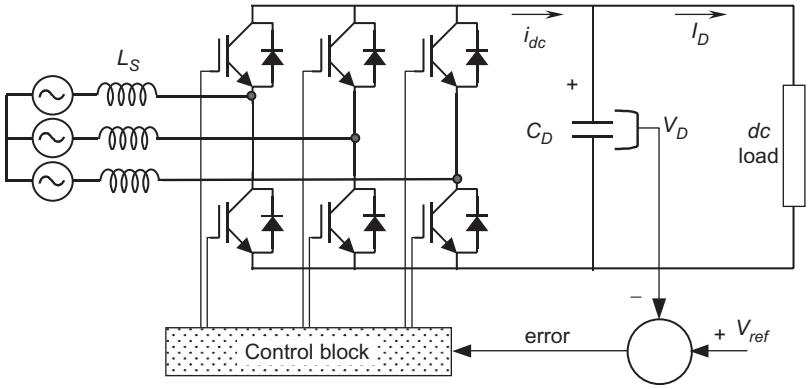


FIG. 9.36 Operation principle of the voltage-source rectifier.

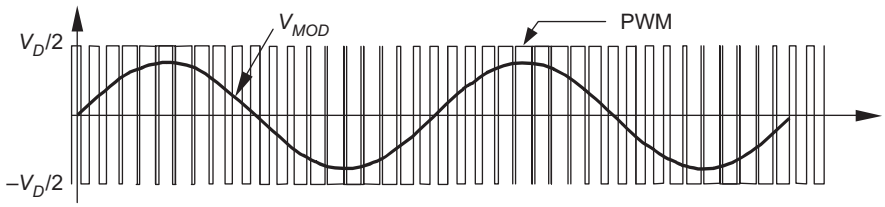


FIG. 9.37 A PWM pattern and its fundamental V_{MOD}.

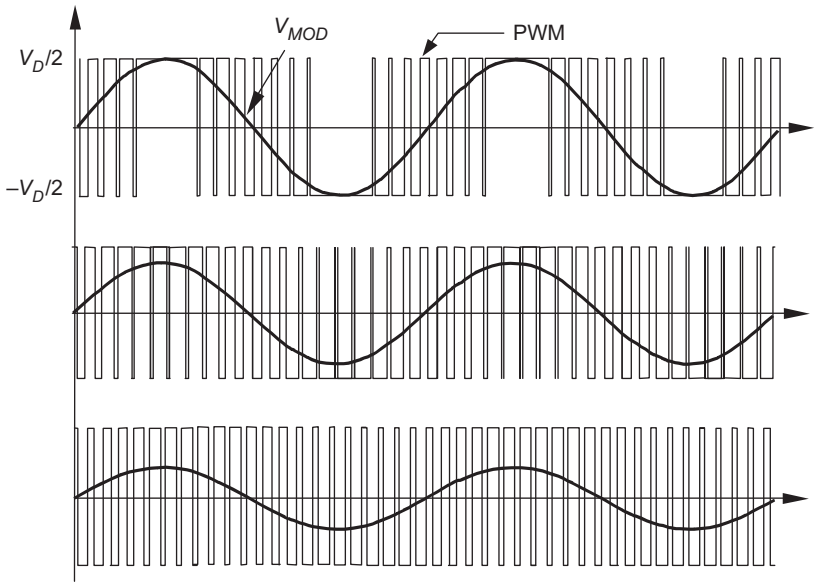


FIG. 9.38 Changing V_{MOD} through the PWM pattern.

power source. Changing the amplitude of this fundamental and its phase shift with respect to the mains, the rectifier can be controlled to operate in the four quadrants: leading power factor rectifier, lagging power factor rectifier, leading power factor inverter, and lagging power factor inverter. Changing the pattern of modulation, as shown in Fig. 9.38, modifies the magnitude of V_{MOD}. Displacing the PWM pattern changes the phase shift.

The interaction between V_{MOD} and V (source voltage) can be seen through a phasor diagram. This interaction permits understanding of the four-quadrant capability of this rectifier. In Fig. 9.39, the following operations are displayed: (A) rectifier at unity power factor, (B) inverter at unity power factor, (C) capacitor (zero power factor), and (D) inductor (zero power factor).

In Fig. 9.39, I_S is the *rms* value of the source current i_s. This current flows through the semiconductors in the way

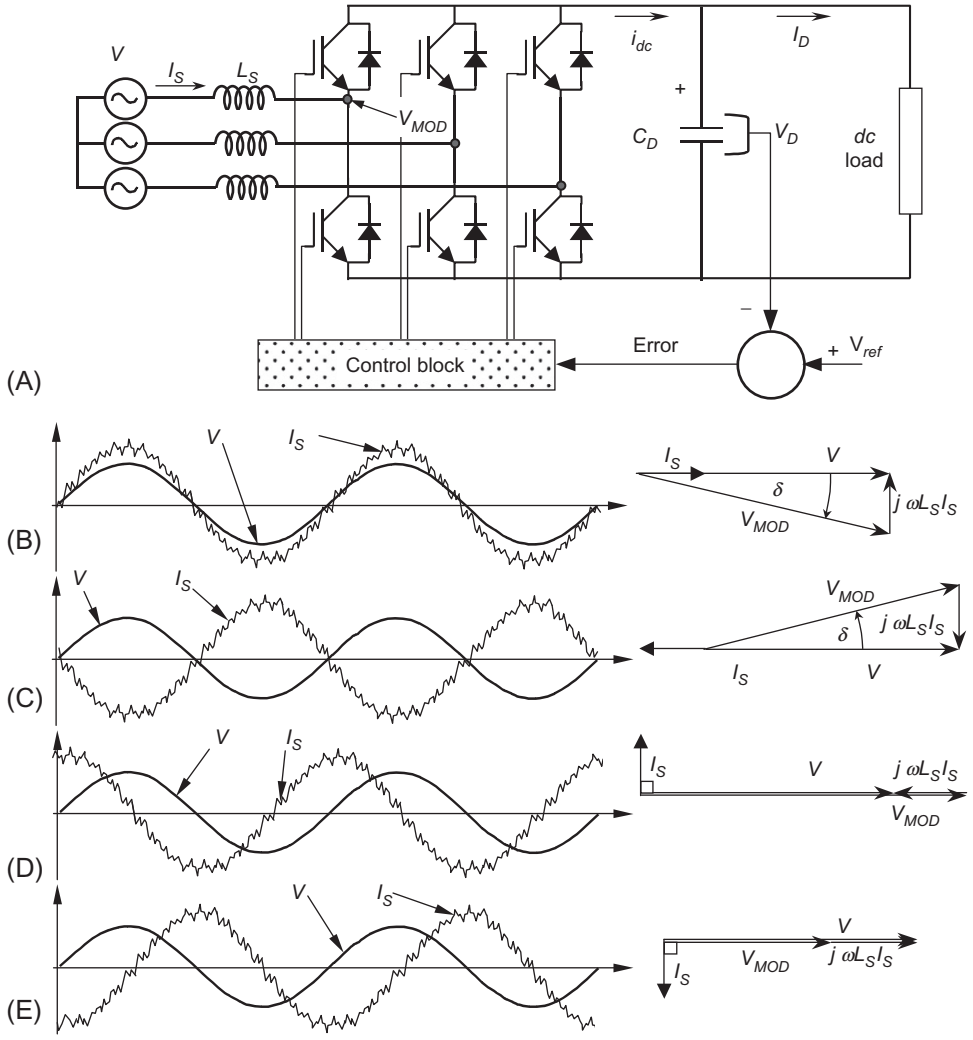


FIG. 9.39 Four-quadrant operation of the force-commutated rectifier: (A) the PWM force-commutated rectifier, (B) rectifier operation at unity power factor, (C) inverter operation at unity power factor, (D) capacitor operation at zero power factor, and (E) inductor operation at zero power factor.

shown in Fig. 9.40. During the positive half cycle, the transistor T_N, connected at the negative side of the *dc* link, is switched *ON*, and the current i_s begins to flow through T_N (i_{Tn}). The current returns to the mains and comes back to the valves, closing a loop with another phase and passing through a diode connected at the same negative terminal of the *dc* link. The current can also go to the *dc* load (inversion) and return through another transistor located at the positive terminal of the *dc* link. When the transistor T_N is switched *OFF,* the current path is interrupted, and the current begins to flow through the diode *Dp*, connected at the positive terminal of the *dc* link. This current, called i_{Dp} in Fig. 9.39, goes directly to the *dc* link, helping in the generation of the current i_{dc}. The current i_{dc} charges the capacitor C_D and permits the rectifier to produce *dc* power. The inductances L_S are very important in this process, because they generate an induced voltage that allows the conduction of the diode D_p. Similar operation occurs during the negative half cycle but with T_p and D_N (see Fig. 9.40).

Under inverter operation, the current paths are different because the currents flowing through the transistors come mainly from the *dc* capacitor, C_D. Under rectifier operation, the circuit works like a boost converter, and under inverter, it works as a buck converter.

To have full control of the operation of the rectifier, their six diodes must be polarized negatively at all values of instantaneous *ac* voltage supply. Otherwise, diodes will conduct, and the PWM rectifier will behave like a common diode rectifier bridge. The way to keep the diodes blocked is to ensure a *dc* link voltage higher than the peak *dc* voltage generated by the diodes alone, as shown in Fig. 9.41. In this way, the diodes remain polarized negatively, and they will conduct only when at least one transistor is switched *ON,* and favorable instantaneous *ac* voltage conditions are given. In Fig. 9.41, V_D represents the

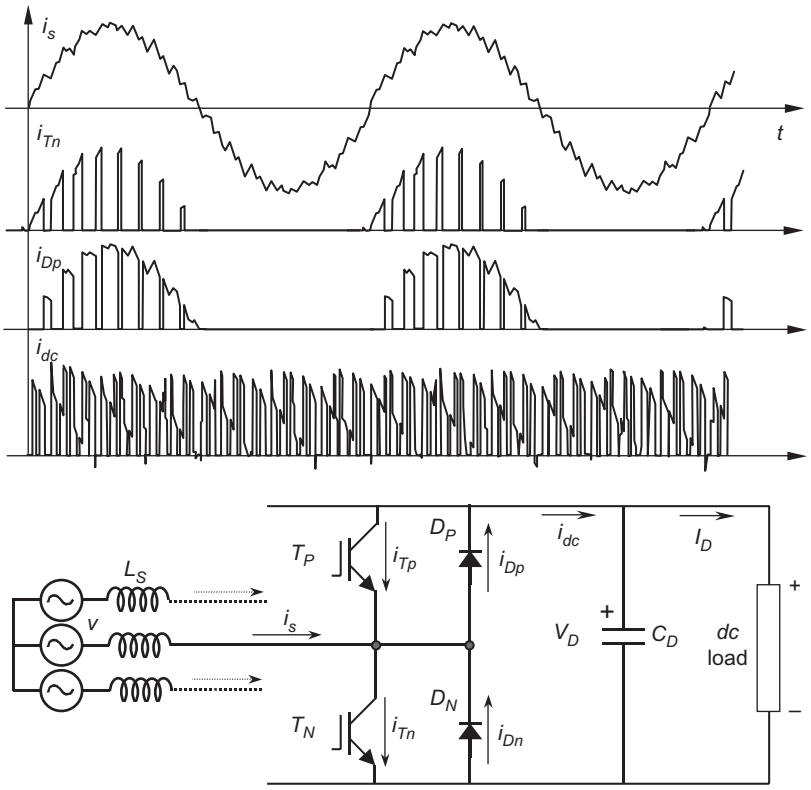


FIG. 9.40 Current waveforms through the mains, the valves, and the *dc* link.

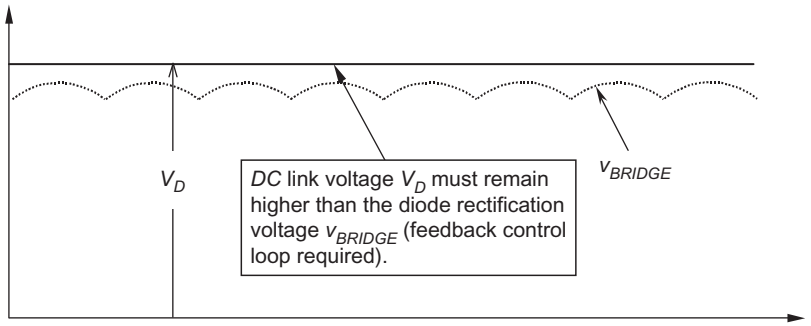


FIG. 9.41 The *DC* link voltage condition for the operation of the PWM rectifier.

capacitor *dc* voltage, which is kept higher than the normal diode-bridge rectification value v_{BRIDGE}. To maintain this condition, the rectifier must have a control loop like the one displayed in Fig. 9.36.

9.3.3 PWM Phase-to-Phase and Phase-to-Neutral Voltages

The PWM waveforms shown in the preceding figures are voltages measured between the middle point of the *dc* voltage and the corresponding phase. The phase-to-phase PWM voltages can be obtained with the help of Eq. (9.52), where the voltage V_{PWM}^{AB} is evaluated:

$$V_{PWM}^{AB} = V_{PWM}^{A} - V_{PWM}^{B} \tag{9.52}$$

where V_{PWM}^{A} and V_{PWM}^{B} are the voltages measured between the middle point of the *dc* voltage and the phases *a* and *b*, respectively. In a less straightforward fashion, the phase-to-neutral voltage can be evaluated with the help of Eq. (9.53):

$$V_{PWM}^{AN} = \frac{1}{3}\left(V_{PWM}^{AB} - V_{PWM}^{CA}\right) \tag{9.53}$$

where V_{PWM}^{AN} is the phase-to-neutral voltage for phase *a* and V_{PWM}^{jk} is the phase-to-phase voltage between phase *j* and phase *k*. Fig. 9.42 shows the PWM patterns for the phase-to-phase and phase-to-neutral voltages.

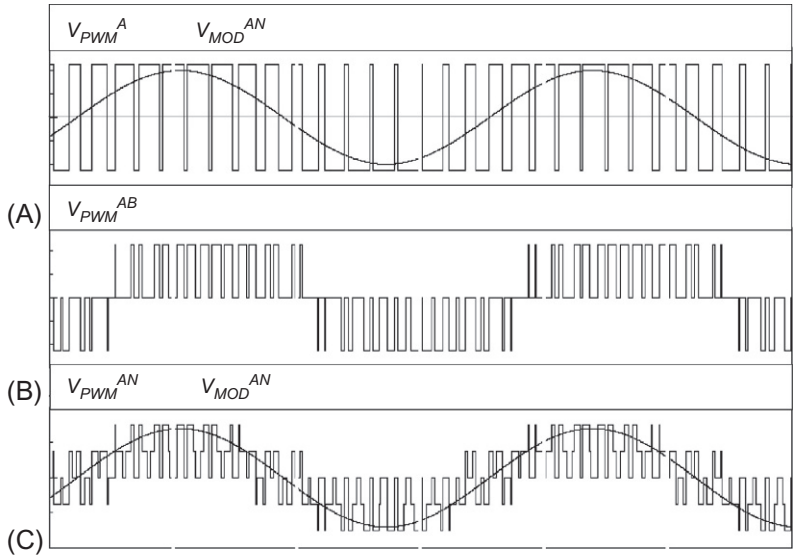


FIG. 9.42 PWM phase voltages: (A) PWM phase modulation, (B) PWM phase-to-phase voltage, and (C) PWM phase-to-neutral voltage.

9.3.4 Control of the *DC* Link Voltage

Control of the *dc* link voltage requires a feedback control loop. As already explained in Section 9.3.2, the *dc* voltage V_D is compared with a reference V_{REF}, and the error signal "e" obtained from this comparison is used to generate a template waveform. The template should be a sinusoidal waveform with the same frequency of the mains supply. This template is used to produce the PWM pattern and allows controlling the rectifier in two different ways: (1) as a voltage-source current-controlled PWM rectifier and (2) as a voltage-source voltage-controlled PWM rectifier. The first method controls the input current, and the second controls the magnitude and phase of the voltage V_{MOD}. The current-controlled method is simpler and more stable than the voltage-controlled method, and for these reasons, it will be explained first.

9.3.4.1 Voltage-Source Current-Controlled PWM Rectifier

This method of control is shown in the rectifier in Fig. 9.43. Control is achieved by measuring the instantaneous phase

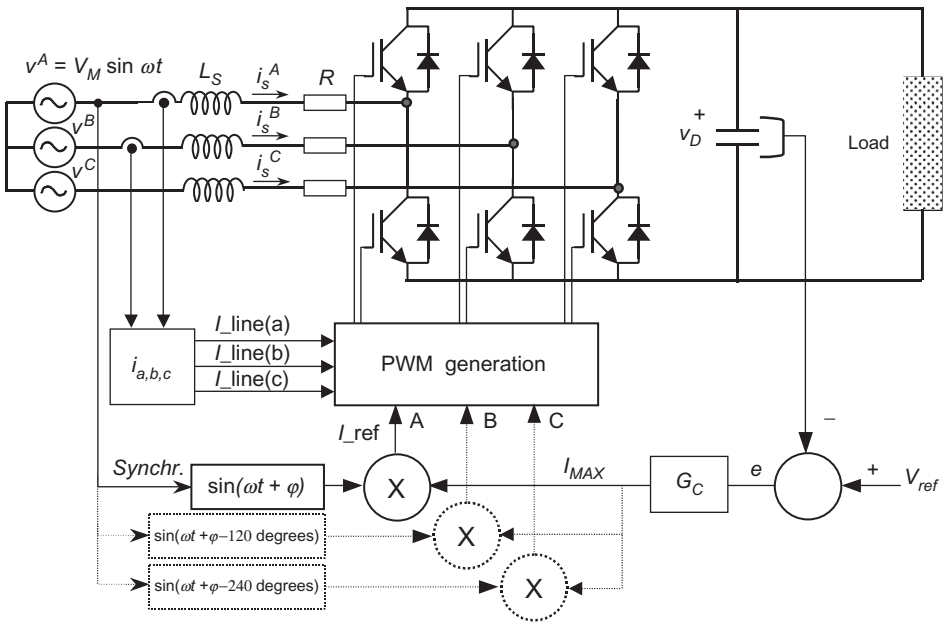


FIG. 9.43 Voltage-source current-controlled PWM rectifier.

currents and forcing them to follow a sinusoidal current reference template, *I*_ref. The amplitude of the current reference template, I_{MAX}, is evaluated using the following equation:

$$I_{MAX} = G_C e = G_C(V_{REF} - v_D) \tag{9.54}$$

where G_C is shown in Fig. 9.43 and represents a controller such as PI, P, Fuzzy, or other. The sinusoidal waveform of the template is obtained by multiplying I_{MAX} with a sine function, with the same frequency of the mains and with the desired phase-shift angle φ, as shown in Fig. 9.43. Further, the template must be synchronized with the power supply. After that, the template has been created and is ready to produce the PWM pattern.

However, one problem arises with the rectifier because the feedback control loop on the voltage V_C can produce instability. Then, it becomes necessary to analyze this problem during rectifier design. Upon introducing the voltage feedback and the G_C controller, the control of the rectifier can be represented in a block diagram in Laplace dominion, as shown in Fig. 9.44. This block diagram represents a linearization of the system around an operating point, given by the *rms* value of the input current, I_S.

The blocks $G_1(s)$ and $G_2(s)$ in Fig. 9.44 represent the transfer function of the rectifier (around the operating point) and the transfer function of the *dc* link capacitor C_D, respectively:

$$G_1(s) = \frac{\Delta P_1(s)}{\Delta I_S(s)} = 3(V\cos\varphi - 2RI_S - L_S I_S s) \tag{9.55}$$

$$G_2(s) = \frac{\Delta V_D(s)}{\Delta P_1(s) - \Delta P_2(s)} = \frac{1}{V_D C_D s} \tag{9.56}$$

where $\Delta P_1(s)$ and $\Delta P_2(s)$ represent the input and output power of the rectifier in Laplace dominion, V the *rms* value of the mains voltage supply (phase-to-neutral), I_S the input current being controlled by the template, L_S the input inductance, and R the resistance between the converter and power supply. According to stability criteria and assuming a *PI* controller, the following relations are obtained:

$$I_S \le \frac{C_D V_D}{3K_P L_S} \tag{9.57}$$

$$I_S \le \frac{K_P V\cos\varphi}{2RK_P + L_S K_I} \tag{9.58}$$

These two relations are useful for the design of the current-controlled rectifier. They relate the values of *dc* link capacitor, *dc* link voltage, *rms* voltage supply, input resistance and inductance, and input power factor with the *rms* value of the input current, I_S. With these relations, the proportional and integral gains K_P and K_I can be calculated to ensure the stability of the rectifier. These relations only establish limitations for rectifier operation, because negative currents always satisfy the inequalities.

With these two stability limits satisfied, the rectifier will keep the *dc* capacitor voltage at the value of V_{REF} (*PI* controller), for all load conditions, by moving power from the *ac* to the *dc* side. Under inverter operation, the power will move in the opposite direction.

Once the stability problems have been solved and the sinusoidal current template has been generated, a modulation method will be required to produce the PWM pattern for the power valves. The PWM pattern will switch the power valves to force the input currents *I*_line to follow the desired current template *I*_ref. There are many modulation methods in the literature, but three methods for voltage-source current-controlled rectifiers are the most widely used ones: *periodical sampling* (PS), *hysteresis band* (HB), and *triangular carrier* (TC).

The PS method switches the power transistors of the rectifier during the transitions of a square-wave clock of fixed frequency: the *periodical sampling* frequency. In each transition, a comparison between *I*_ref and *I*_line is made, and corrections take place. As shown in Fig. 9.45A, this type of control is very simple to implement: only a comparator and a D-type flip-flop are needed per phase. The main advantage of this method is that the minimum time between switching transitions is limited to the period of the sampling clock. This characteristic determines the maximum switching frequency of the converter. However, the average switching frequency is not clearly defined.

The HB method switches the transistors when the error between *I*_ref and *I*_line exceeds a fixed magnitude: the *hysteresis band*. As it can be seen in Fig. 9.45B, this type of control needs a single comparator with hysteresis per phase. In this case, the switching frequency is not determined, but its maximum value can be evaluated through the following equation:

$$f_S^{\max} = \frac{V_D}{4hL_S} \tag{9.59}$$

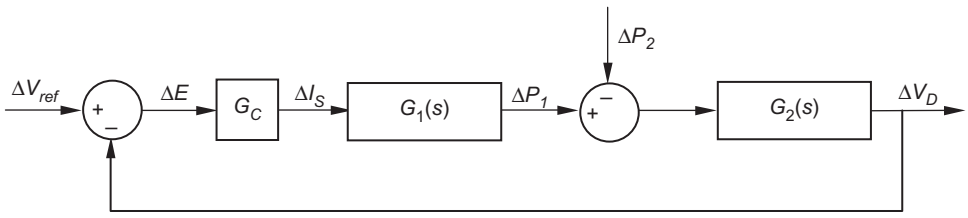


FIG. 9.44 Closed-loop rectifier transfer function.

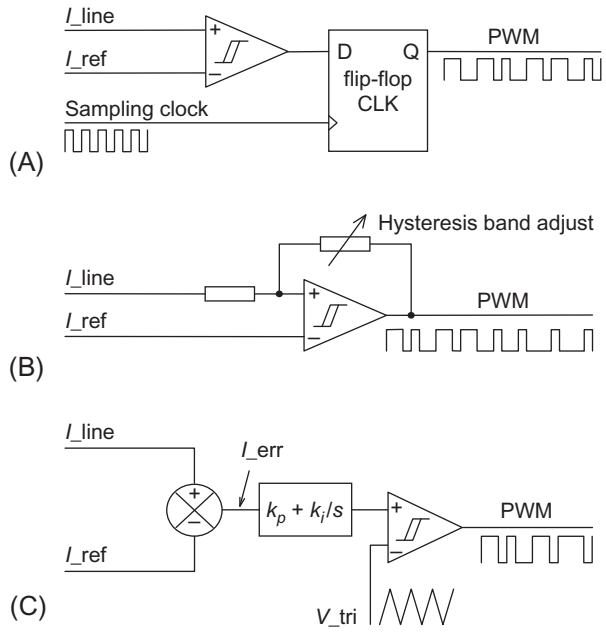


FIG. 9.45 Modulation control methods: (A) periodical sampling, (B) hysteresis band, and (C) triangular carrier.

where h is the magnitude of the hysteresis band.

The TC method, shown in Fig. 9.45C, compares the error between I_ref and I_line with a triangular wave. This triangular wave has fixed amplitude and frequency and is called the *triangular carrier*. The error is processed through a proportional-integral (PI) gain stage before comparison with the TC takes place. As can be seen, this control scheme is more complex than PS and HB. The values for k_p and k_i determine the transient response and steady-state error of the TC method. It has been found empirically that the values for k_p and k_i shown in Eqs. (9.60), (9.61) give a good dynamic performance under several operating conditions:

$$k_p = \frac{L_s \omega_c}{2V_D} \tag{9.60}$$

$$k_i = \omega_c K_P \tag{9.61}$$

where L_S is the total series inductance seen by the rectifier, ω_c is the TC frequency, and V_D is the *dc* link voltage of the rectifier.

In order to measure the level of distortion (or undesired harmonic generation) introduced by these three control methods, Eq. (9.62) is defined:

$$\%\text{Distortion} = \frac{100}{I_{rms}} \sqrt{\frac{1}{T}\int_T (I_\text{line} - I_\text{ref})^2 dt} \tag{9.62}$$

In Eq. (9.62), the term I_{rms} is the effective value of the desired current. The term inside the square root gives the *rms* value of the error current, which is undesired. This formula measures the percentage of error (or distortion) of the generated waveform. This definition considers the ripple, amplitude, and phase errors of the measured waveform, as opposed to the *THD*, which does not take into account offsets, scalings, and phase shifts.

Fig. 9.46 shows the current waveforms generated by the three aforementioned methods. The example uses an average switching frequency of 1.5 kHz. The PS is the worst, but its digital implementation is simpler. The HB method and TC with PI control are quite similar, and the TC with only proportional control gives a current with a small phase shift. However, Fig. 9.47 shows that the higher the switching frequency, the closer the results obtained with the different modulation methods. Over 6 kHz of switching frequency, the distortion is very small for all methods.

9.3.4.2 Voltage-Source Voltage-Controlled PWM Rectifier

Fig. 9.48 shows a one-phase diagram from which the control system for a voltage-source voltage-controlled rectifier is

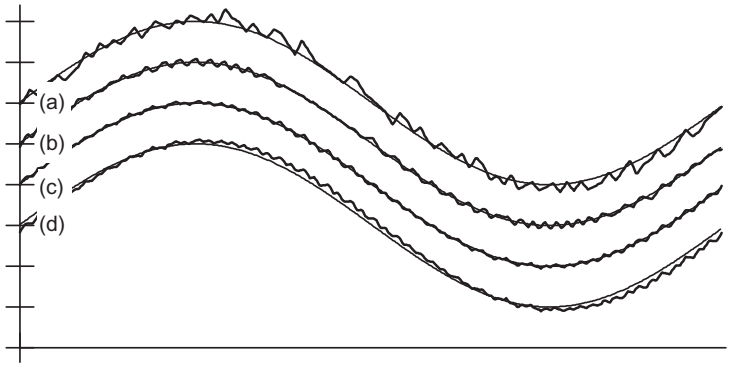


FIG. 9.46 Waveforms obtained using 1.5 kHz switching frequency and $L_S = 13$ mH: (a) PS method, (b) HB method, (c) TC method ($K_P + K_I$), and (d) TC method (K_P only).

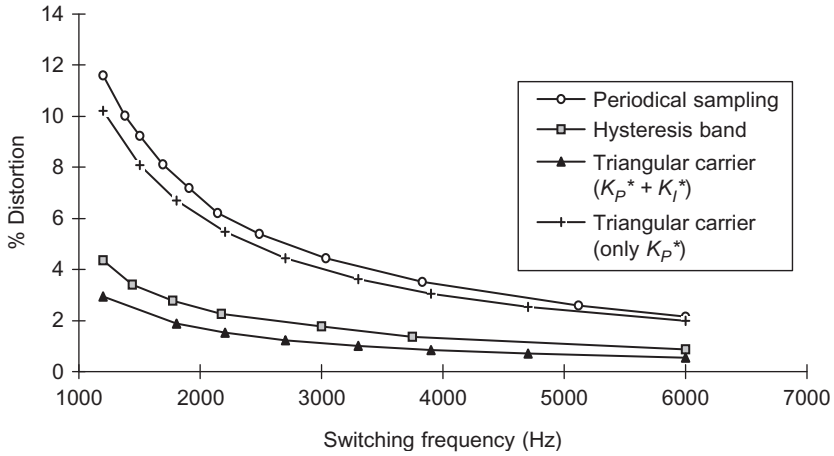


FIG. 9.47 Distortion comparison for a sinusoidal current reference.

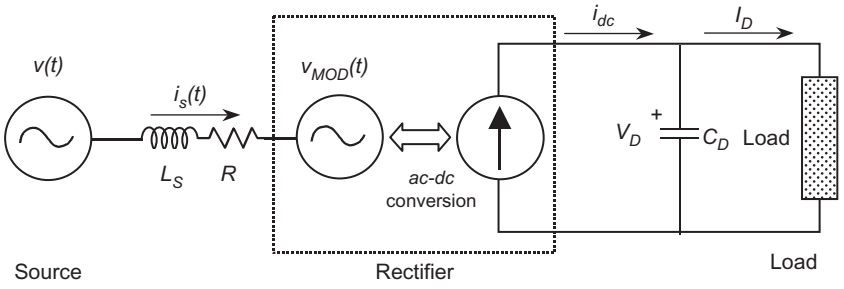


FIG. 9.48 One-phase fundamental diagram of the voltage-source rectifier.

derived. This diagram represents an equivalent circuit of the fundamentals, that is, pure sinusoidal at the mains side and pure *dc* at the *dc* link side. The control is achieved by creating a sinusoidal voltage template V_{MOD}, which is modified in amplitude and angle to interact with the mains voltage V. In this way, the input currents are controlled without measuring them. The template V_{MOD} is generated using the differential equations that govern the rectifier.

The following differential equation can be derived from Fig. 9.48:

$$v(t) = L_S \frac{di_s}{dt} + Ri_s + v_{MOD}(t) \tag{9.63}$$

Assuming that $v(t) = V\sqrt{2}\sin\omega t$, then the solution for $i_s(t)$, to acquire a template V_{MOD} able to make the rectifier work at constant power factor, should be of the form

$$i_s(t) = I_{max}(t)\sin(\omega t + \varphi) \tag{9.64}$$

Eqs. (9.63), (9.64), and $v(t)$ allow a function of time able to modify V_{MOD} in amplitude and phase that will make the rectifier work at a fixed power factor. Combining these equations with $v(t)$ yields

$$v_{MOD}(t) = \left[V\sqrt{2} + X_S I_{max}\sin\varphi - \left(RI_{max} + L_S\frac{dI_{max}}{dt}\right)\cos\varphi\right]\sin\omega t - \left[X_S I_{max}\cos\varphi - \left(RI_{max} + L_S\frac{dI_{max}}{dt}\right)\sin\varphi\right]\cos\omega t \tag{9.65}$$

Eq. (9.65) provides a template for V_{MOD}, which is controlled through variations of the input current amplitude I_{max}. Substituting the derivatives of I_{max} into Eq. (9.65) makes sense, because I_{max} changes every time the *dc* load is modified. The term X_S in Eq. (9.65) is ωL_S. This equation can also be written for unity power factor operation. In such a case, $\cos\varphi = 1$ and $\sin\varphi = 0$:

$$v_{MOD}(t) = \left(V\sqrt{2} - RI_{max} - L_S\frac{dI_{max}}{dt}\right)\sin\omega t - X_S I_{max}\cos\omega t \tag{9.66}$$

With this last equation, a unity power factor, voltage-source, voltage-controlled PWM rectifier can be implemented as shown in Fig. 9.49. It can be observed that Eqs. (9.65), (9.66) have an *in-phase* term with the mains supply ($\sin\omega t$) and an

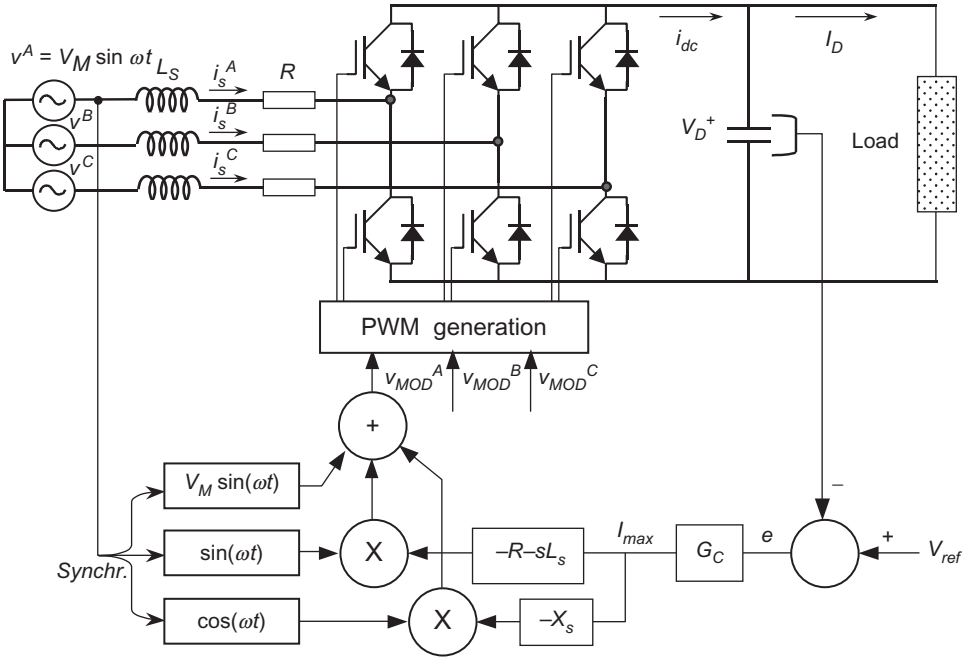


FIG. 9.49 Implementation of the voltage-controlled rectifier for unity power factor operation.

in-quadrature term (cos ωt). These two terms allow the template V_{MOD} to change in magnitude and phase so as to have full unity power factor control of the rectifier.

Compared with the control block of Fig. 9.43, in the voltage-source voltage-controlled rectifier of Fig. 9.49, there is no need to sense the input currents. However, to ensure stability limits as good as the limits of the current-controlled rectifier, the blocks "$-R-sL_S$" and "$-X_S$" in Fig. 9.49 have to emulate and reproduce exactly the real values of R, X_S, and L_S of the power circuit. However, these parameters do not remain constant, and this fact affects the stability of this system, making it less stable than the system shown in Fig. 9.43. In theory, if the impedance parameters are reproduced exactly, the stability limits of this rectifier are given by the same equations as used for the current-controlled rectifier seen in Fig. 9.43 (Eqs. 9.57, 9.58).

Under steady state, I_{max} is constant, and Eq. (9.66) can be written in terms of phasor diagram, resulting in Eq. (9.67). As shown in Fig. 9.50, different operating conditions for the unity power factor rectifier can be displayed with this equation:

$$\vec{V}_{MOD} = \vec{V} - R\vec{I}_S - jX_S\vec{I}_S \tag{9.67}$$

With the sinusoidal template V_{MOD} already created, a modulation method to commutate the transistors will be required. As in the case of current-controlled rectifier, there are many methods to modulate the template, with the most well-known the so-called sinusoidal pulse-width modulation (SPWM), which uses a TC to generate the PWM as shown in Fig. 9.51. Only this method will be described in this chapter.

In this method, there are two important parameters to define: the amplitude modulation ratio or modulation index m and the frequency modulation ratio p. Definitions are given by

$$m = \frac{V_{MOD}^{max}}{V_{TRIANG}^{max}} \tag{9.68}$$

$$p = \frac{f_T}{f_S} \tag{9.69}$$

where V_{MOD}^{max} and V_{TRIANG}^{max} are the amplitudes of V_{MOD} and V_{TRIANG}, respectively. On the other hand, f_S is the frequency of the mains supply and f_T the frequency of the TC. In Fig. 9.51, $m = 0.8$ and $p = 21$. When $m > 1$, overmodulation is defined.

The modulation method described in Fig. 9.51 has a harmonic content that changes with p and m. When $p < 21$, it is recommended that synchronous PWM be used, which means that the TC and the template should be synchronized. Furthermore, to avoid subharmonics, it is also desired that p be an integer. If p is an odd number, even harmonics will be eliminated. If p is a multiple of 3, then the PWM modulation of the three phases will be identical. When m increases, the amplitude of the fundamental voltage increases proportionally, but some harmonics decrease. Under overmodulation ($m > 1$), the fundamental voltage does not increase linearly, and more harmonics appear. Fig. 9.52 shows the harmonic spectrum of the three-phase PWM voltage waveforms for different values of m, and $p = 3k$ where k is an odd number.

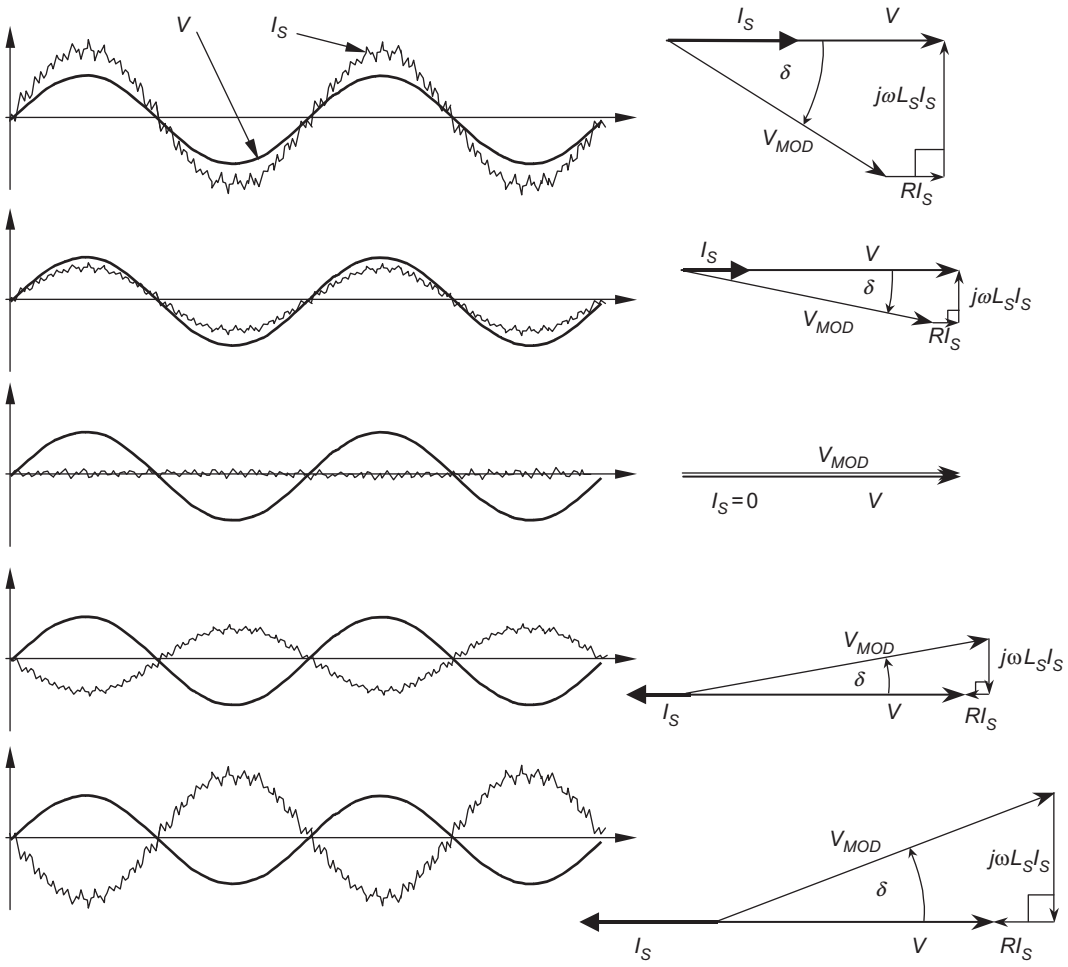


FIG. 9.50 Steady-state operation of the unity power factor rectifier under different load conditions.

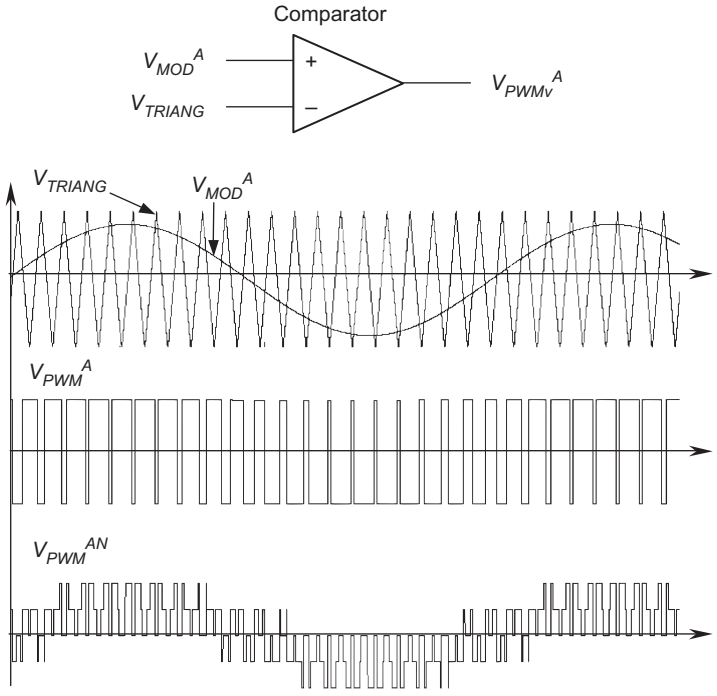


FIG. 9.51 Sinusoidal modulation method based on TC.

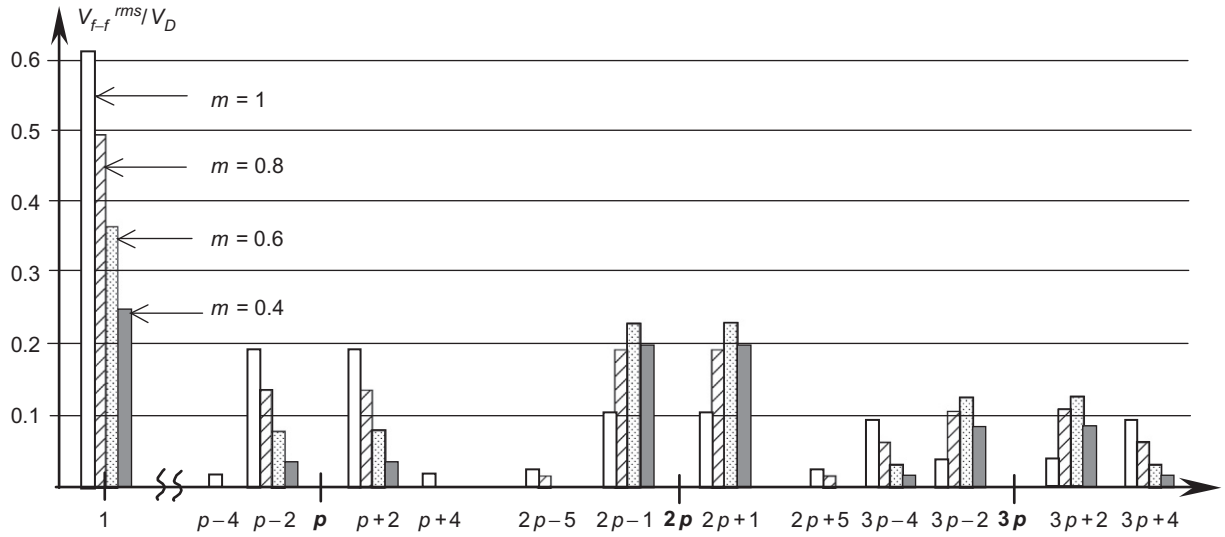


FIG. 9.52 Harmonic spectrum for SPWM modulation.

Due to the presence of the input inductance L_S, the harmonic currents that result are proportionally attenuated with the harmonic number. This characteristic is shown in the current waveforms of Fig. 9.53, where larger p numbers generate cleaner currents. The rectifier that originated the currents of Fig. 9.53 has the following characteristics: $V_D = 450 V_{dc}$, $V_{f-f}^{rms} = 220 V_{ac}$, $L_S = 2$ mH, and input current $I_S = 80$ A_{rms}. It can be observed that with $p > 21$, the current distortion is quite small. The value of $p = 81$ in Fig. 9.53 produces an almost pure sinusoidal waveform, and it means 4860 Hz of switching frequency at 60 Hz or only 4.050 Hz in a rectifier operating in a 50 Hz supply. This switching frequency can be managed by MOSFETs, IGBTs, and even Power Darlingtons. Then, a number $p = 81$ is feasible for today's low- and medium-power rectifiers.

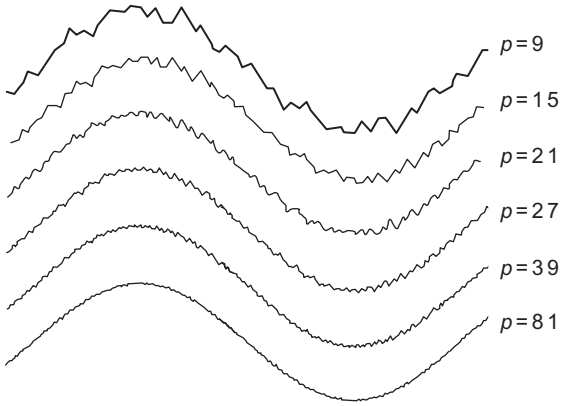


FIG. 9.53 Current waveforms for different values of p.

9.3.4.3 Voltage-Source Load-Controlled PWM Rectifier

A simple method of control for small PWM rectifiers (up to 10–20 kW) is based on direct control of the *dc* current. Fig. 9.54 shows the schematic of this control system. The fundamental voltage V_{MOD} modulated by the rectifier is produced by a fixed and unique PWM pattern, which can be carefully selected to eliminate most undesirable harmonics. As the PWM does not change, it can be stored in a permanent digital memory (ROM).

The control is based on changing the power angle δ between the mains voltage V and fundamental PWM voltage V_{MOD}. When δ changes, the amount of power flow transferred from the *ac* to the *dc* side also changes. When the power angle is negative (V_{MOD} lags V), the power flow goes from the *ac* to the *dc* side. When the power angle is positive, the power flows in the opposite direction. Then, the power angle can be controlled through the current I_D. The voltage V_D does not need to be sensed, because this control establishes a stable *dc* voltage operation for each *dc* current and power angle. With these characteristics, it is possible to find a relation between I_D and δ so as to obtain constant *dc* voltage for all load conditions. This relation is given by

$$I_D = f(\delta) = \frac{V\left(\cos\delta - \dfrac{\omega L_S}{R}\sin\delta - 1\right)}{R\left[1 + \left(\dfrac{\omega L_S}{R}\right)^2\right]} \tag{9.70}$$

From Eq. (9.70), a plot and a reciprocal function $\delta = f(I_D)$ is obtained to control the rectifier. The relation between I_D and δ allows for leading power factor operation and null regulation. The leading power factor operation is shown in the phasor diagram of Fig. 9.54.

The control scheme of the voltage-source load-controlled rectifier is characterized by the following: (i) There is neither

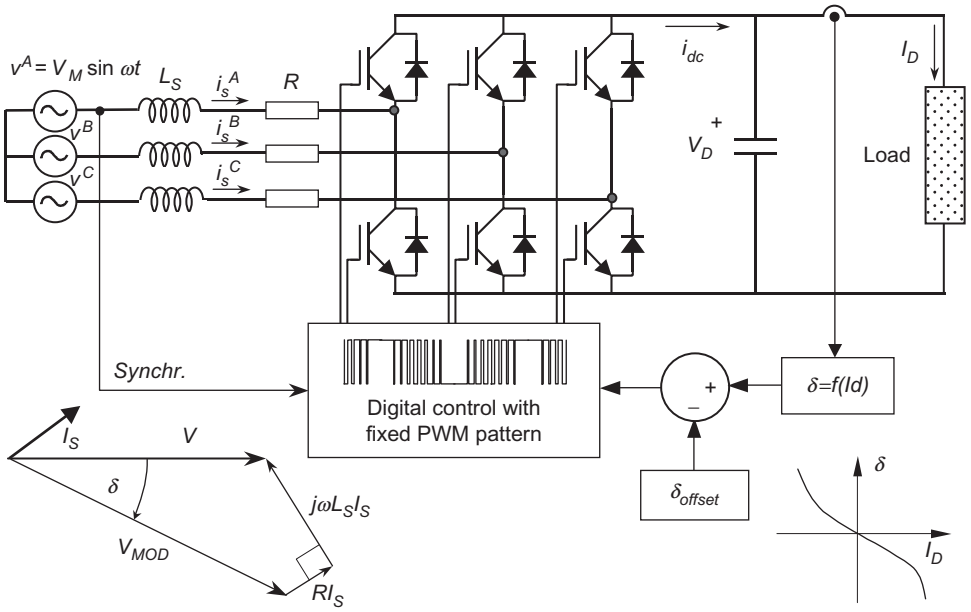


FIG. 9.54 Voltage-source load-controlled PWM rectifier.

input current sensors nor *dc* voltage sensor, (ii) it works with a fixed and predefined PWM pattern, (iii) it presents very good stability, (iv) its stability does not depend on the size of the *dc* capacitor, (v) it can work at leading power factor for all load conditions, and (vi) it can be adjusted with Eq. (9.70) to work at zero regulation. The drawback appears when R in Eq. (9.70) becomes negligible, because in such a case, the control system is unable to find an equilibrium point for the *dc* link voltage. That is why this control method is not applicable to large systems.

9.3.5 New Technologies and Applications of Force-Commutated Rectifiers

The additional advantages of force-commutated rectifiers with respect to line-commutated rectifiers make them better candidates for industrial requirements. They permit new applications such as rectifiers with harmonic elimination capability (active filters), power factor compensators, machine drives with four-quadrant operation, frequency links to connect 50 Hz with 60 Hz systems, and regenerative converters for traction power supplies. Modulation with very fast valves such as IGBTs permits almost sinusoidal currents to be obtained. The dynamics of these rectifiers is so fast that they can reverse power almost instantaneously. In machine drives, current-source PWM rectifiers, like the one shown in Fig. 9.35A, can be used to drive *dc* machines from the three-phase supply. Four-quadrant applications using voltage-source PWM rectifiers are extended for induction machines, synchronous machines with starting control, and special machines such as brushless dc motors. Back-to-back systems are being used in Japan to link power systems with different frequencies.

9.3.5.1 Active Power Filter

Force-commutated PWM rectifiers can work as active power filters. The voltage-source current-controlled rectifier has the capability to eliminate harmonics produced by other polluting loads. It only needs to be connected as shown in Fig. 9.55.

The current sensors are located at the input terminals of the power source, and these currents (instead of the rectifier currents) are forced to be sinusoidal. As there are polluting loads in the system, the rectifier is forced to deliver the harmonics that loads need, because the current sensors do not allow the harmonics going to the mains. As a result, the rectifier currents become distorted, but an adequate *dc* capacitor C_D can keep the *dc* link voltage in good shape. In this way, the rectifier can do its duty and also eliminate harmonics to the source. In addition, it also can compensate power factor and unbalanced load problems.

9.3.5.2 Frequency Link Systems

Frequency link systems permit power to be transferred form one frequency to another one. They are also useful for linking unsynchronized networks. Line-commutated converters are widely used for this application, but they have some drawbacks that force-commutated converters can eliminate. For example, the harmonic filter requirement, the poor power factor, and the necessity to count with a synchronous compensator when generating machines at the load side are absent. Fig. 9.56 shows a typical line-commutated system in which a 60 Hz load is fed by a 50 Hz supply. As the 60 Hz side needs excitation to commutate the valves, a synchronous compensator has been required.

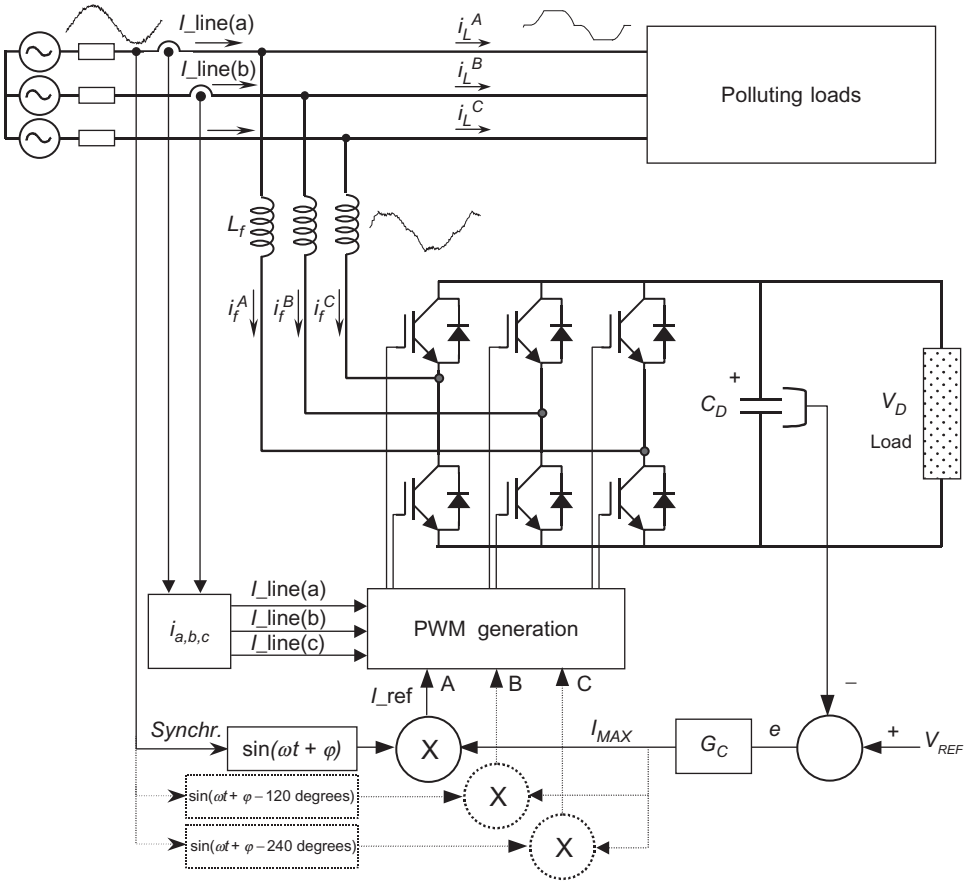


FIG. 9.55 Voltage-source rectifier with harmonic elimination capability.

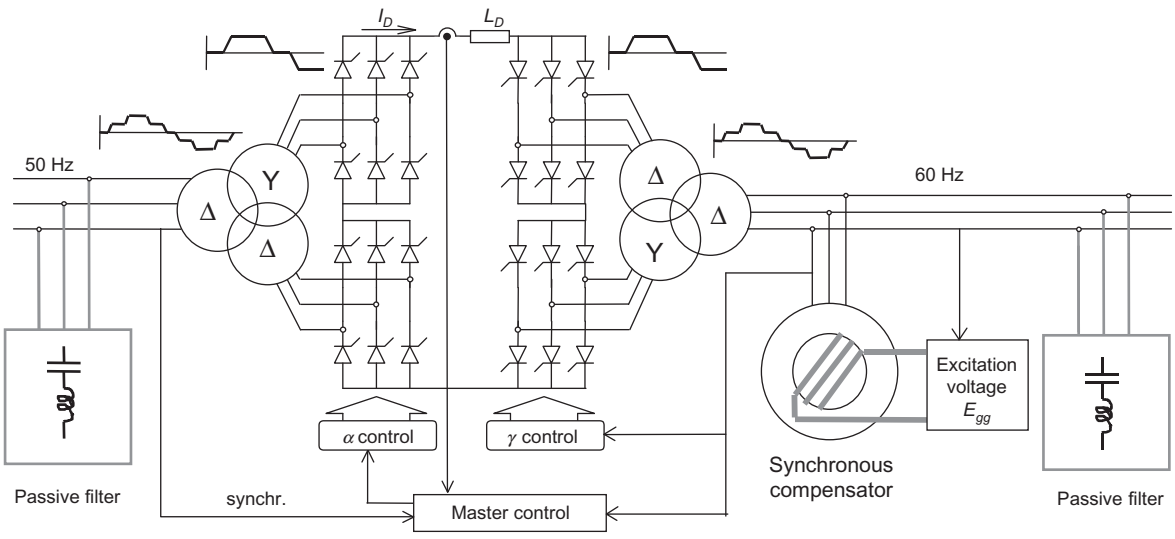


FIG. 9.56 Frequency link systems with line-commutated converters.

In contrast, an equivalent system with force-commutated converters is simpler, cleaner, and more reliable. It is implemented with a *dc* voltage-controlled rectifier and another identical converter working in the inversion mode. The power factor can be adjusted independently at the two *ac* terminals, and filters or synchronous compensators are not required. Fig. 9.57 shows a frequency-link system with force-commutated converters.

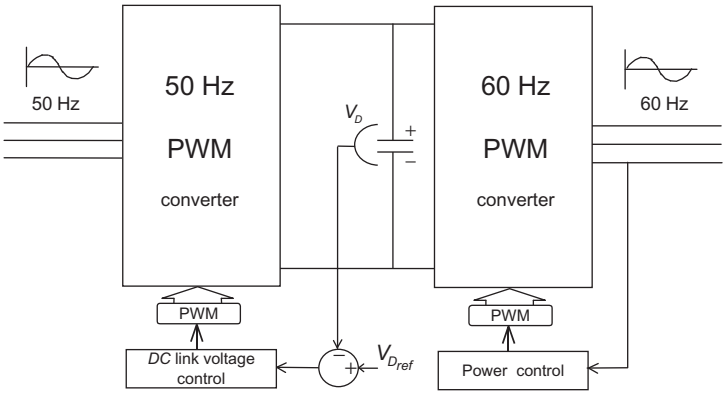


FIG. 9.57 Frequency link systems with force-commutated converters.

9.3.5.3 Special Topologies for High Power Applications

High-power applications require series- and/or parallel-connected rectifiers. Series and parallel operations with force-commutated rectifiers allow improving the power quality because harmonic cancelation can be applied to these topologies. Fig. 9.58 shows a series connection of force-commutated rectifiers, where the modulating carriers of the valves in each bridge are shifted to cancel harmonics. The example uses sinusoidal PWM that are with TC shifted.

The waveforms of the input currents for the series connection system are shown in Fig. 9.59. The frequency modulation ratio shown in this figure is for $p=9$. The carriers are shifted by 90 degrees each, to obtain harmonic cancelation. Shifting of the carriers δ_T depends on the number of converters in series (or in parallel) and is given by

$$\delta_T = \frac{2\pi}{n} \tag{9.71}$$

where n is the number of converters in series or in parallel. It can be observed that despite the low value of p, the total current becomes quite clean and clear, better than the current of one of the converters in the chain.

The harmonic cancelation with series- or parallel-connected rectifiers, using the same modulation but the carriers shifted, is quite effective. The resultant current is better with n converters and frequency modulation $p=p_1$ than with one converter and $p=np_1$. This attribute is verified in Fig. 9.60, where the total current of four converters in series with $p=9$ and carriers shifted is compared with the current of only one converter and $p=36$. This technique also allows for the use of valves with slow commutation times, such as high-power GTOs. Generally, high-power valves have low commutation times, and hence, the parallel and/or series options remain very attractive.

Another special topology for high power was implemented for Asea Brown Boveri (ABB) in Bremen. A 100 MW power converter supplies energy to the railways at $16^{2/3}$ Hz. It uses basic "H" bridges like the one shown in Fig. 9.61, connected to the load through power transformers. These transformers are connected in parallel at the converter side and in series at the load side.

The system uses SPWM with TCs shifted, and depending on the number of converters connected in the chain of bridges, the voltage waveform becomes more and more sinusoidal. Fig. 9.62 shows a back-to-back system using a chain of 12 "H" converters connected as shown in Fig. 9.61B.

The *ac* voltage waveform obtained with the topology of Fig. 9.62 is displayed in Fig. 9.63. It can be observed that the voltage is formed by small steps that depend on the number of converters in the chain (12 in this case). The current is almost perfectly sinusoidal.

Fig. 9.64 shows the voltage waveforms for different number of converters connected in the bridge. It is clear that the larger the number of converters, the better the voltage.

Another interesting result with this converter is that the *ac* voltages become modulated by both PWM and amplitude modulation (AM). This is because when the pulse modulation changes, the steps of the amplitude change. The maximum number of steps of the resultant voltage is equal to the number of converters. When the voltage decreases, some steps disappear, and then, the AM becomes a discrete function. Fig. 9.65 shows the AM of the voltage.

9.3.5.4 Machine Drives Applications

One of the most important applications of force-commutated rectifiers is in machine drives. Line-commutated thyristor converters have limited applications because they need excitation to extinguish the valves. This limitation does not allow the use of line-commutated converters in induction machine drives. On the other hand, with force-commutated converters, four-quadrant operation is achievable. Fig. 9.66 shows a typical frequency converter with a force-commutated rectifier-inverter link. The rectifier side controls the *dc* link, and the inverter side controls the machine. The machine can be a synchronous, brushless *dc*, or induction machine. The reversal of both speed and power is possible with this topology. At the rectifier side,

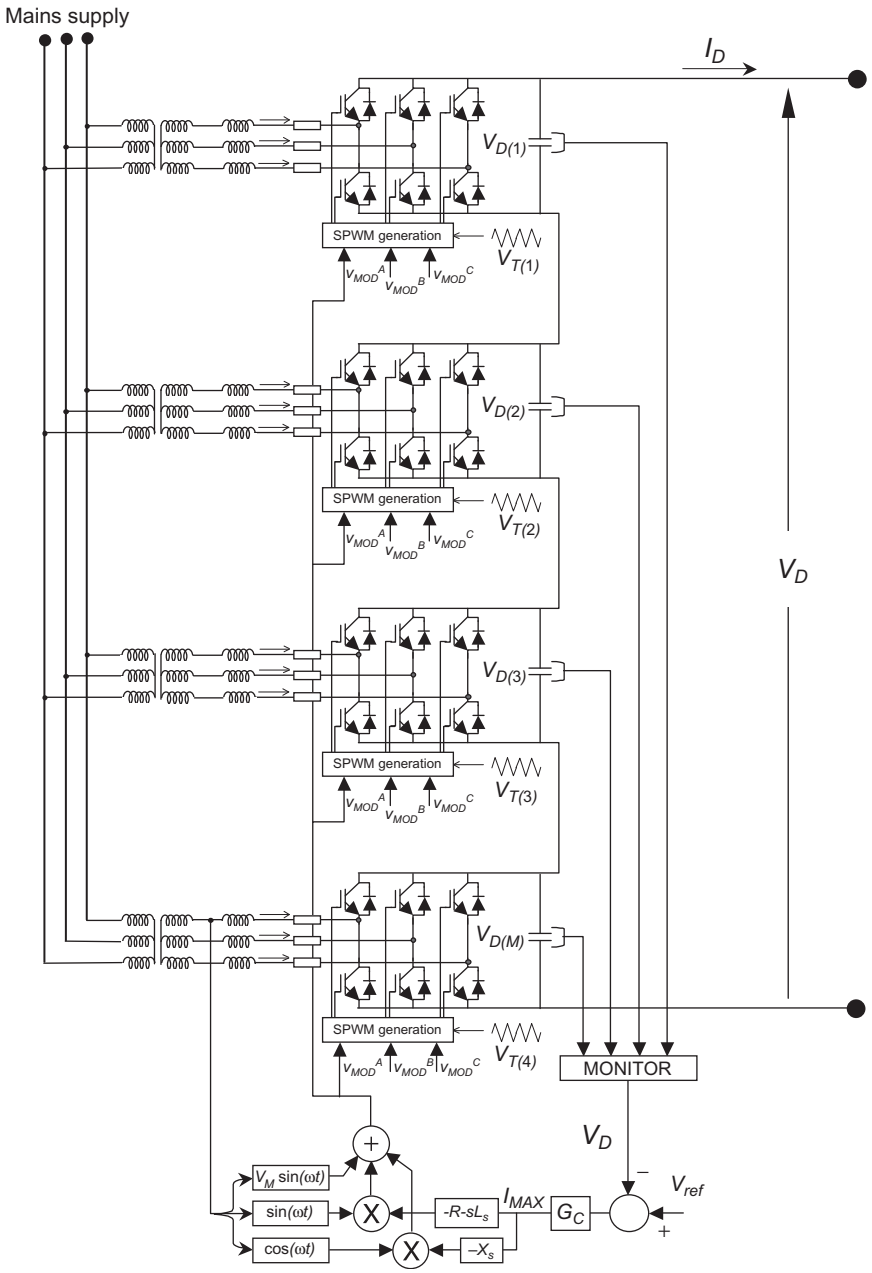


FIG. 9.58 Series connection system with force-commutated rectifiers.

the power factor can be controlled, and even with an inductive load such as an induction machine, the source can "see" the load as capacitive or resistive. Changing the frequency of the inverter controls the machine speed, and the torque is controlled through the stator currents and torque angle. The inverter will become a rectifier during regenerative braking, which is possible by making slip negative in an induction machine or by making the torque angle negative in synchronous and brushless *dc* machines.

A variation of the drive of Fig. 9.66 is found in electric traction applications. Battery-powered vehicles use the inverter as a rectifier during regenerative braking, and sometimes, the inverter is also used as a battery charger. In this case, the rectifier can be fed by a single-phase or three-phase system. Fig. 9.67 shows a battery-powered electric bus system. This system uses the power inverter of the traction motor as rectifier for two purposes: regenerative braking and as a battery charger fed by a three-phase power source.

9.3.5.5 Variable Speed Power Generation

Power generation at 50 or 60 Hz requires constant speed machines. In addition, induction machines are not currently

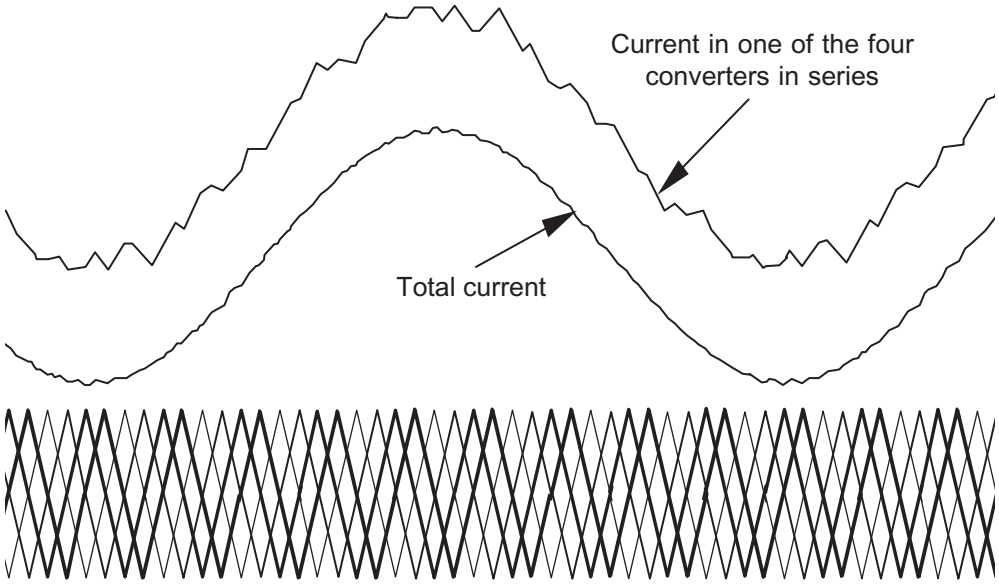


FIG. 9.59 Input currents and carriers of the series connection system of Fig. 9.58.

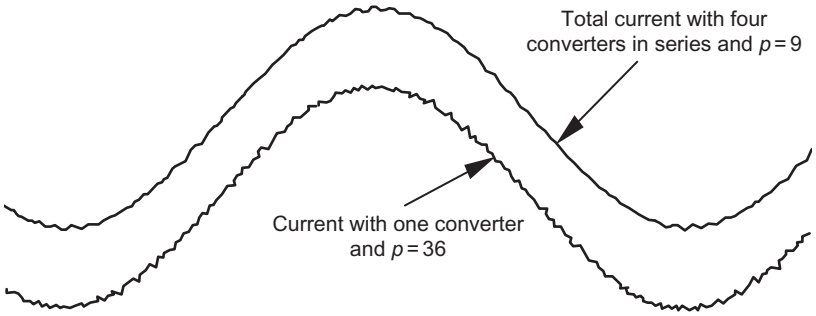


FIG. 9.60 Four converters in series and $p=9$ compared with one converter and $p=36$.

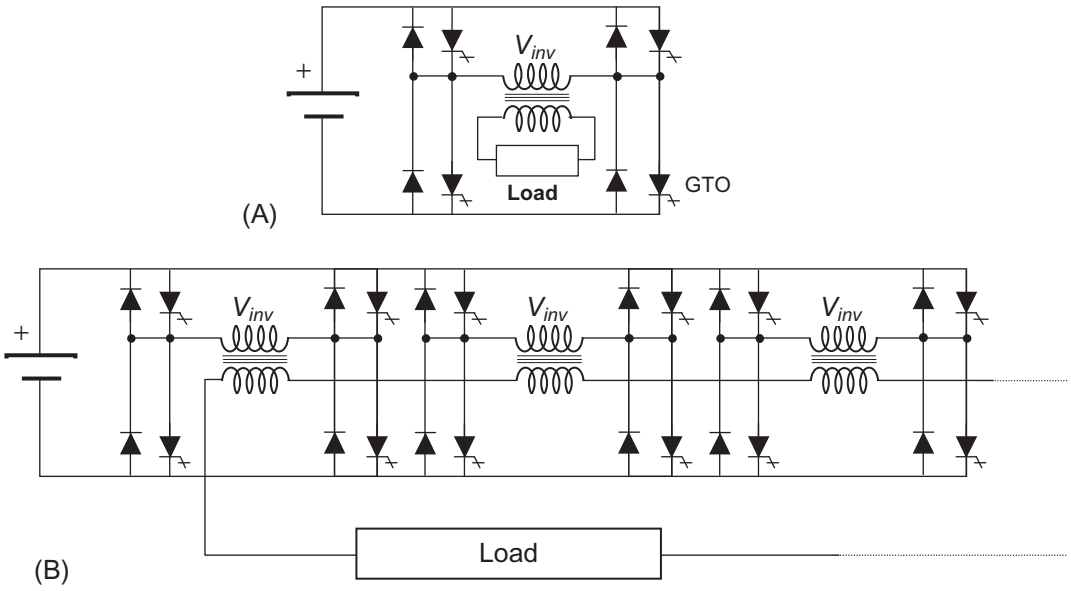


FIG. 9.61 The "H" modulator: (A) one bridge and (B) bridges connected in series at load side through isolation transformers.

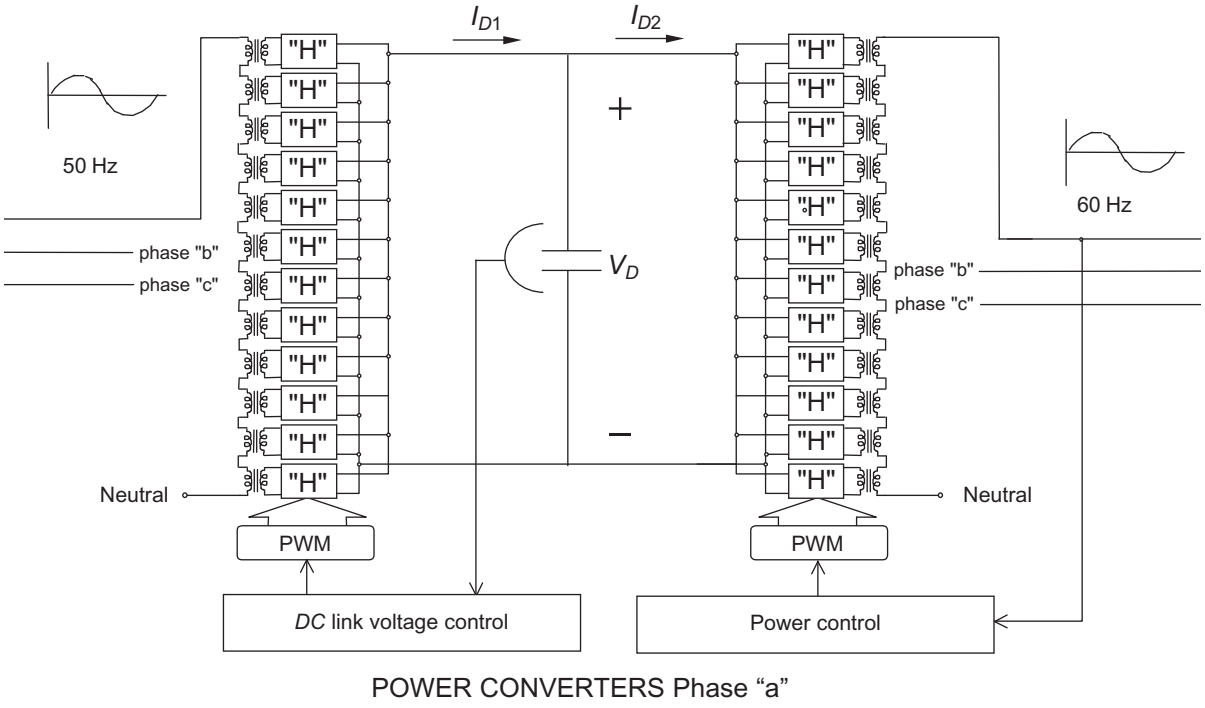


FIG. 9.62 Frequency link with force-commutated converters and sinusoidal voltage modulation.

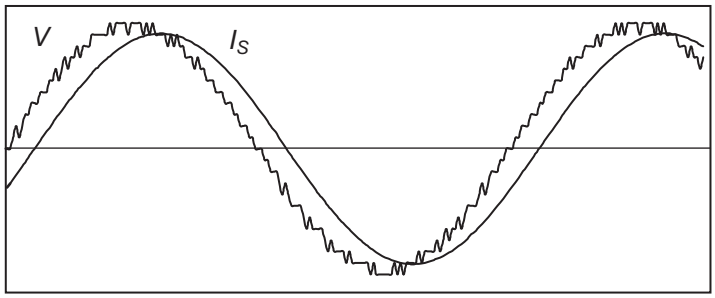


FIG. 9.63 Voltage and current waveforms with 12 converters.

used in power plants because of magnetization problems. With the use of frequency-link force-commutated converters, variable-speed constant-frequency generation becomes possible even with induction generators. The power plant in Fig. 9.68 shows a wind generator implemented with an induction machine and a rectifier-inverter frequency link connected to the utility. The *dc* link voltage is kept constant with the converter located at the mains side. The converter connected at the machine side controls the slip of the generator and adjusts it according to the speed of wind or power requirements. The utility is not affected by the power factor of the generator, because the two converters keep the cos φ of the machine independent of the mains supply. The converter at the mains side can even be adjusted to operate at leading power factor.

Variable-speed constant-frequency generation also can be used in either hydraulic or thermal plants. This allows for optimal adjustment of the efficiency-speed characteristics of the machines. In many places, wound rotor induction generators working as variable-speed synchronous machines are being used as constant-frequency generators. They operate in hydraulic plants that are able to store water during low-demand periods. A power converter is connected at the slip rings of the generator. The rotor is then fed with variable-frequency excitation. This allows the generator to generate at different speeds around the synchronous rotating flux.

9.3.5.6 Power Rectifiers Using Multilevel Topologies

Almost all voltage-source rectifiers already described are two-level configurations. Today, multilevel topologies are becoming very popular, mainly three-level converters. The most popular three-level configuration is called diode-clamped converter, which is shown in Fig. 9.69. This topology is today the standard

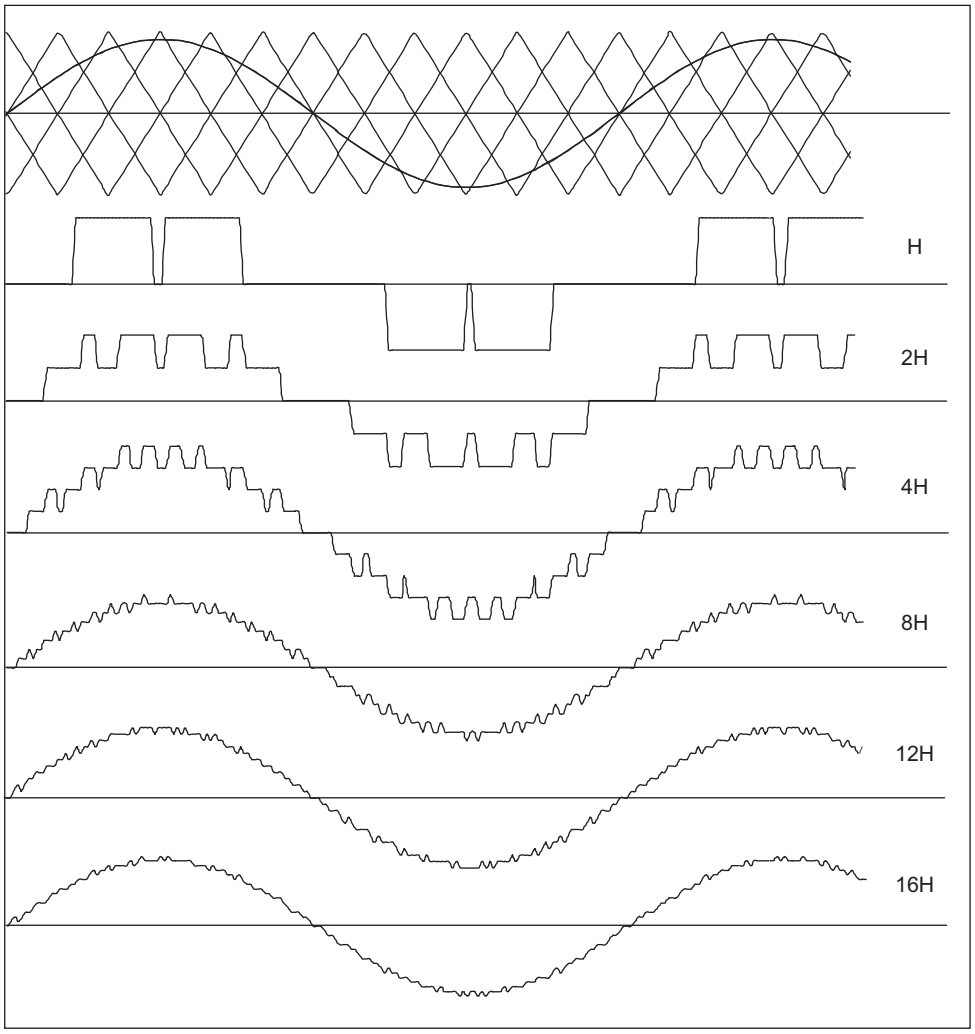


FIG. 9.64 Voltage waveforms with different numbers of "H" bridges in series.

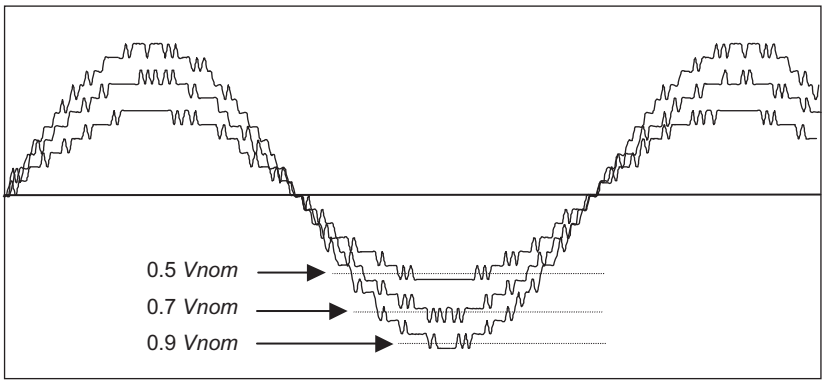


FIG. 9.65 Amplitude modulation of the "H" bridges of Fig. 9.62.

solution for high-power steel rolling mills, which uses back-to-back three-phase rectifier-inverter link configuration. In addition, this solution has been recently introduced in high-power downhill conveyor belts that operate almost permanently in the regeneration mode or rectifier operation. The more important advantage of three-level rectifiers is that voltage and current harmonics are reduced due to the increased number of levels.

Higher number of levels can be obtained using the same diode-clamped strategy, as shown in Fig. 9.70, where only

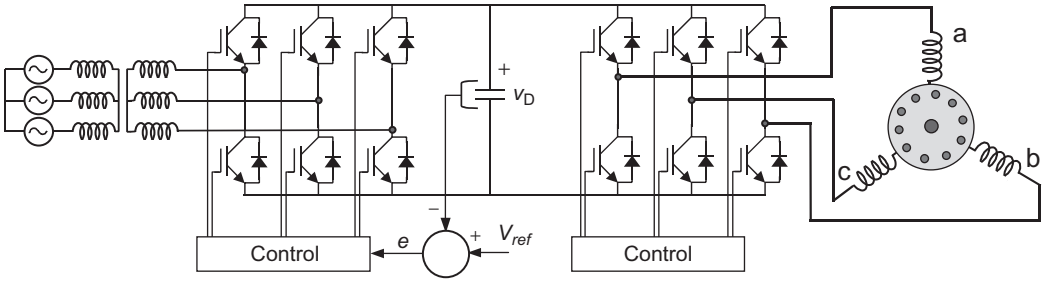


FIG. 9.66 Frequency converter with force-commutated converters.

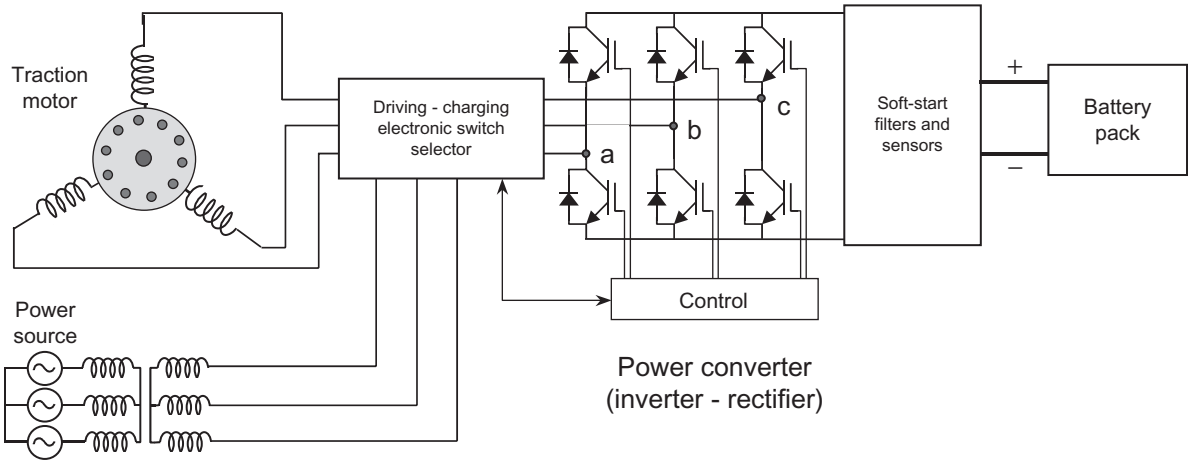


FIG. 9.67 Electric bus system with regenerative braking and battery charger.

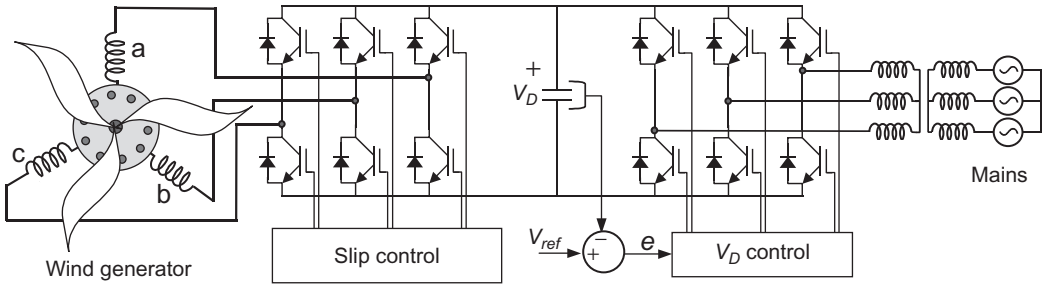


FIG. 9.68 Variable-speed constant-frequency wind generator.

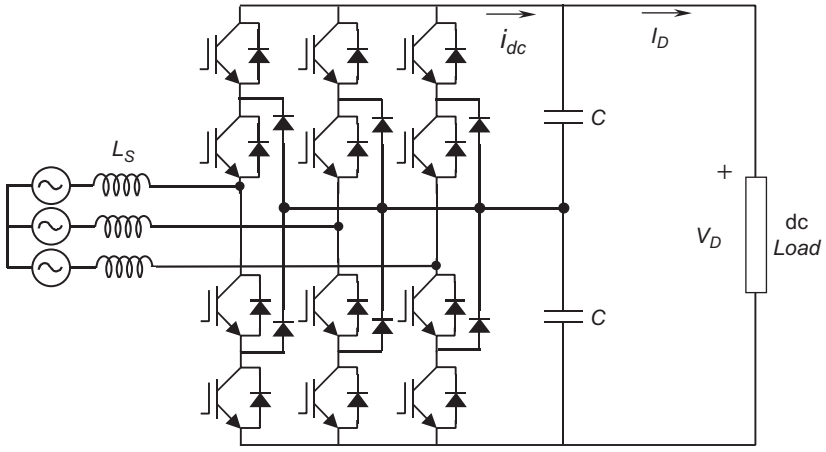


FIG. 9.69 Voltage-source rectifier using three-level converter.

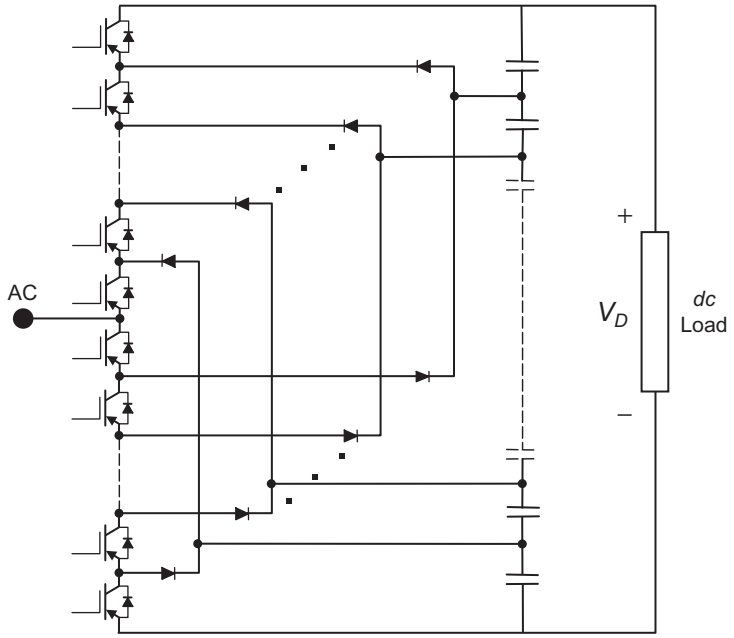


FIG. 9.70 Multilevel rectifier using diode-clamped topology.

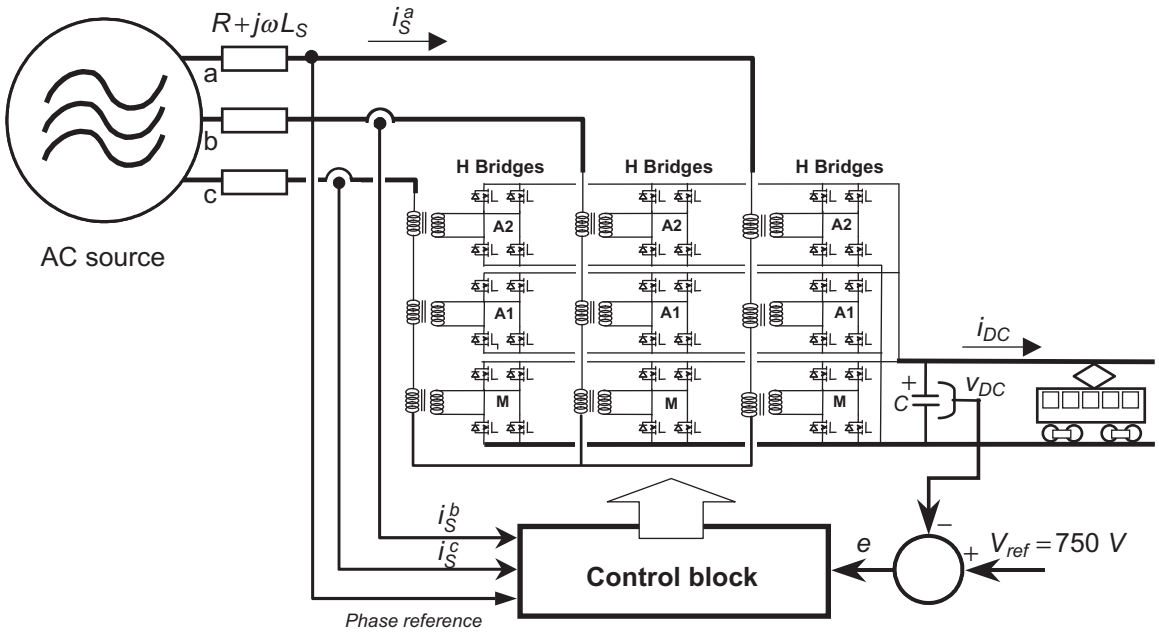


FIG. 9.71 Twenty-seven-level rectifier for railways, using H-bridges scaled in power of three.

one phase of a general approach is displayed. However, this topology becomes more and more complex with the increase of the number of levels. For this reason, new topologies are being studied to get a large number of levels with less power transistors. One example of such of these topologies is the multistage, 27-level converter shown in Fig. 9.71. This special 27-level, 4-quadrant rectifier uses only 3 H-bridges per phase with independent input transformers for each H-bridge. The transformers allow galvanic isolation and power escalation to get high-quality voltage waveforms, with *THD* of less than 1%. The power scalation consists on increasing the voltage rates of each transformer making use of the "three-level" characteristics of H-bridges. Then, the number of levels is optimized when transformers are scaled in power of three. Some advantages of this 27-level topology are the following: (a) Only one of the three H-bridges, called "main converter," manages more

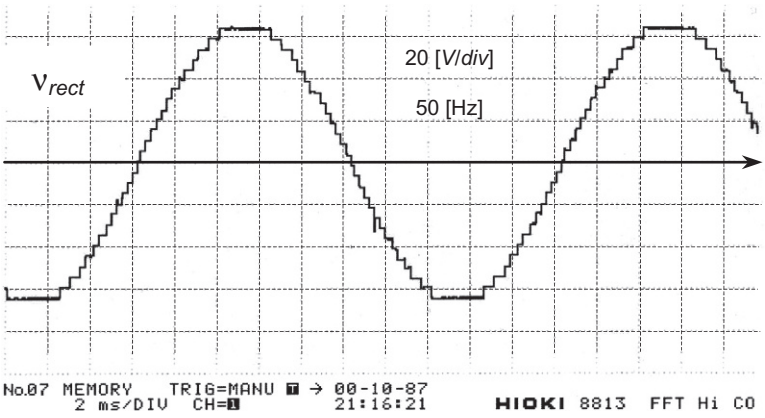


FIG. 9.72 *AC* voltage waveform generated by the 27-level rectifier.

than 80% of the total active power in each phase, and (b) this main converter switches at fundamental frequency reducing the switching losses at a minimum value. The rectifier of Fig. 9.71 is a current-controlled voltage-source type, with a conventional feedback control loop, which is being used as a rectifier in a subway substation. It includes fast reversal of power and the ability to produce clean *ac* and *dc* waveforms with negligible ripple. This rectifier can also compensate power factor and eliminate harmonics produced by other loads in the *ac* line. Fig. 9.72 shows the *ac* voltage waveform obtained with this rectifier from an experimental prototype. If one more H-bridge is added, 81 levels are obtained, because the number of levels increases according with $N=3^k$, where N is the number of levels or voltage steps and k the number of H-bridges used per phase.

Many other high-level topologies are under study, but this matter is beyond the main topic of this chapter.

Further Reading

[1] G. Möltgen, Line Commutated Thyristor Converters, Siemens Aktiengesellschaft, Berlin-Munich, Pitman Publishing, London, 1972.
[2] G. Möltgen, Converter Engineering, and Introduction to Operation and Theory, John Wiley and Sons, New York, NY, 1984.
[3] K. Thorborg, Power Electronics, Prentice-Hall International (UK) Ltd., London, 1988.
[4] M.H. Rashid, Power Electronics, Circuits Devices and Applications, Prentice-Hall International Editions, London, 1992.
[5] N. Mohan, T.M. Undeland, W.P. Robbins, Power Electronics: Converters, Applications, and Design, John Wiley and Sons, New York, NY, 1989.
[6] J. Arrillaga, D.A. Bradley, P.S. Bodger, Power System Harmonics, John Wiley and Sons, New York, NY, 1989.
[7] J.M.D. Murphy, F.G. Turnbull, Power Electronic Control of AC Motors, Pergamon Press, Oxford, England, 1988.
[8] M.E. Villablanca, J. Arrillaga, Pulse multiplication in parallel convertors by multitap control of interphase reactor, IEE Proc. B 139 (1) (1992) 13–20.
[9] D.A. Woodford, HVDC transmission, Professional report from Manitoba HVDC Research Center, Winnipeg, Manitoba, March 1998.
[10] D.R. Veas, J.W. Dixon, B.T. Ooi, A novel load current control method for a leading power factor voltage source PEM rectifier, IEEE Trans. Power Electron. 9 (2) (1994) 153–159.
[11] L. Morán, E. Mora, R. Wallace, J. Dixon, Performance analysis of a power factor compensator which simultaneously eliminates line current harmonics, in: IEEE Power Electronics Specialists Conference, PESC'92, Toledo, España, June 29 to July 3, 1992.
[12] P.D. Ziogas, L. Morán, G. Joos, D. Vincenti, A refined PWM scheme for voltage and current source converters, in: IEEE-IAS Annual Meeting, 1990, pp. 977–983.
[13] W. McMurray, Modulation of the chopping frequency in DC choppers and PWM inverters having current hysteresis controllers, IEEE Trans. Ind. Appl. IA-20 (1984) 763–768.
[14] J.W. Dixon, B.T. Ooi, Indirect current control of a unity power factor sinusoidal current boost type three-phase rectifier, IEEE Trans. Ind. Electron. 35 (4) (1988) 508–515.
[15] L. Morán, J. Dixon, R. Wallace, A three-phase active power filter operating with fixed switching frequency for reactive power and current harmonic compensation, IEEE Trans. Ind. Electron. 42 (4) (1995) 402–408.
[16] M.A. Boost, P. Ziogas, State-of-the-art PWM techniques, a critical evaluation, IEEE Trans. Ind. Appl. 24 (2) (1988) 271–280.
[17] J.W. Dixon, B.T. Ooi, Series and parallel operation of hysteresis current-controlled PWM rectifiers, IEEE Trans. Ind. Appl. 25 (4) (1989) 644–651.
[18] B.T. Ooi, J.W. Dixon, A.B. Kulkarni, M. Nishimoto, An integrated AC drive system using a controlled-current PWM rectifier/inverter link, IEEE Trans. Power Electron. 3 (1) (1988) 64–71.
[19] M. Koyama, Y. Shimomura, H. Yamaguchi, M. Mukunoki, H. Okayama, S. Mizoguchi, Large capacity high efficiency three-level GCT inverter system for steel rolling mill drivers, in: Proceedings of the 9th European Conference on Power Electronics, EPE, Austria, CDROM, 2001.
[20] J. Rodríguez, J. Dixon, J. Espinoza, P. Lezana, PWM regenerative rectifiers: state of the art, IEEE Trans. Ind. Electron. 52 (4) (2005) 5–22.
[21] J. Dixon, L. Morán, A clean four-quadrant sinusoidal power rectifier, using multistage converters for subway applications, IEEE Trans. Ind. Electron. 52 (5) (2005) 653–661.

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10

DC-DC Converters

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10.1 Introduction

Modern electronic systems require high-quality, small, lightweight, reliable, and efficient power supplies. Linear power regulators, whose principle of operation is based on a voltage or current divider, are inefficient. They are limited to output voltages smaller than the input voltage. Also, their power density is low because they require low-frequency (50 or 60 Hz) line transformers and filters. Linear regulators can, however, provide a very high-quality output voltage. Their main area of application is at low power levels as low-dropout voltage (LDO) regulators. Electronic devices in linear regulators operate in their active (linear) modes. At higher power levels, switching regulators are used. Switching regulators use power electronic semiconductor switches in *on* and *off* states. Since there is a small power loss in those states (low voltage across a switch in the *on* state, zero current through a switch in the *off* state), switching regulators can achieve high energy conversion efficiencies. Modern power electronic switches can operate at high frequencies. The higher the operating frequency, the smaller and lighter the transformers, filter inductors, and capacitors. In addition, dynamic characteristics of converters improve with increasing operating frequencies. The bandwidth of a control loop is usually determined by the corner frequency of the output filter. Therefore, high operating frequencies allow for achieving a faster dynamic response to rapid changes in the load current and/or the input voltage.

High-frequency electronic power processors are used in dc-dc power conversion. The functions of dc-dc converters are

- to convert a dc input voltage V_S into a dc output voltage V_O,
- to regulate the dc output voltage against load and line variations,
- to reduce the ac voltage ripple on the dc output voltage below the required level,
- to provide isolation between the input source and the load (isolation is not always required),
- to protect the supplied system and the input source from electromagnetic interference (EMI),
- to satisfy various international and national safety standards.

The dc-dc converters can be divided into two main types: hard-switching pulse-width-modulated (PWM) converters and resonant and soft-switching converters. This chapter deals with the former type of dc-dc converters. The PWM converters have been very popular for the last three decades. They are widely used at all power levels. Topologies and properties of PWM converters are well understood and described in literature. Advantages of PWM converters include low component count, high efficiency, constant frequency operation, relatively

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simple control and commercial availability of integrated circuit controllers, and ability to achieve high conversion ratios for both step-down and step-up application. A disadvantage of PWM dc-dc converters is that PWM rectangular voltage and current waveforms cause turn-on and turn-off losses in semiconductor devices that limit practical operating frequencies to a megahertz range. Rectangular waveforms also inherently generate EMI.

This chapter starts from a section on dc choppers that are used primarily in dc drives. The output voltage of dc choppers is controlled by adjusting the *on* time of a switch, which in turn adjusts the width of a voltage pulse at the output. This is the so-called pulse-width-modulation (PWM) control. The dc choppers with additional filtering components form PWM dc-dc converters. Four basic dc-dc converter topologies are presented in Sections 10.3–10.6: buck, boost, buck-boost, and Ćuk converters. Popular isolated versions of these converters are also discussed. Operation of converters is explained under ideal component and semiconductor device assumptions. Section 10.7 discusses effects of nonidealities in PWM converters. Section 10.8 presents topologies for increased efficiency at low output voltage and for bidirectional power flow. Section 10.9 reviews control principles of PWM dc-dc converters. Two main control schemes, voltage-mode control and current-mode control, are described. Summary of application areas of PWM dc-dc converters is given in Section 10.10. Finally, a list of modern textbooks on power electronics is provided. These books are excellent resources for deeper exploration of the area of dc-dc power conversion.

10.2 DC Choppers

A step-down dc chopper with a resistive load is shown in Fig. 10.1A. It is a series connection of a dc input voltage source V_S, controllable switch S, and load resistance R. In most cases, switch S has a unidirectional voltage blocking capabilities and unidirectional current conduction capabilities. Power electronic switches are usually implemented with power MOSFETs, IGBTs, MCTs, power BJTs, or GTOs. If an antiparallel diode is used or embedded in a switch, a switch exhibits a bidirectional current conduction property. Fig. 10.1B depicts waveforms in a step-down chopper. The switch is being operated with a duty ratio D defined as a ratio of the switch *on* time to the sum of the *on* and the *off* times. For a constant frequency operation,

$$D \equiv \frac{t_{on}}{t_{on} + t_{off}} = \frac{t_{on}}{T} \tag{10.1}$$

where $T = 1/f$ is the period of the switching frequency f. The average value of the output voltage is

$$V_O = DV_S \tag{10.2}$$

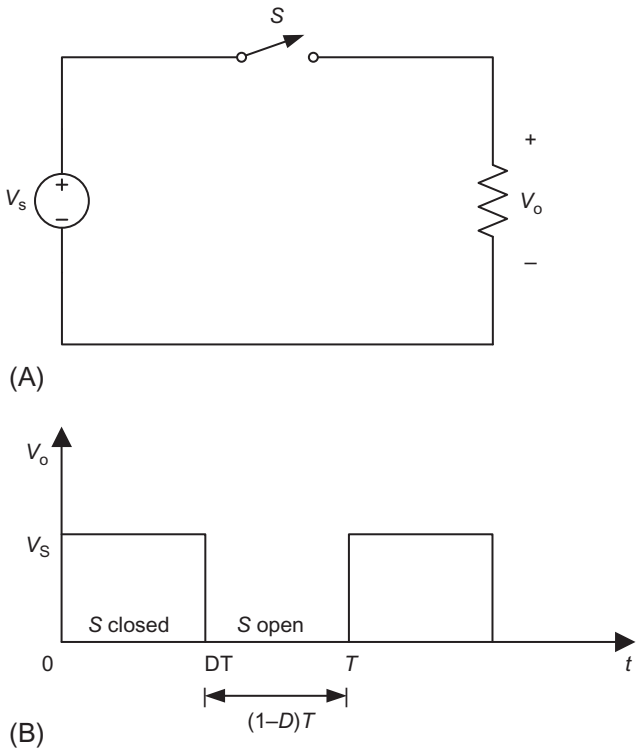


FIG. 10.1 DC chopper with resistive load, (A) circuit diagram and (B) output voltage waveform.

and can be regulated by adjusting duty ratio D. The average output voltage is always smaller than the input voltage, hence, the name of the converter.

The dc step-down choppers are commonly used in dc drives. In such a case, the load is presented as a series combination of inductance L, resistance R, and back emf E as shown in Fig. 10.2A. To provide a path for a continuous inductor current flow when the switch is in the *off* state, an antiparallel diode D must be connected across the load. Since the chopper of Fig. 10.2A provides a positive voltage and a positive current to the load, it is called a first-quadrant chopper. The load voltage and current are graphed in Fig. 10.2B under assumptions that the load current never reaches zero and the load time constant $\tau = L/R$ is much greater than the period T. Average values of the output voltage and current can be adjusted by changing the duty ratio D.

The dc choppers can also provide peak output voltages higher than the input voltage. Such a step-up configuration is presented in Fig. 10.3. It consists of dc input source V_S, inductor L connected in series with the source, switch S connecting the inductor to ground, and a series combination of diode D and load. If the switch operates with a duty ratio D, the output voltage is a series of pulses of duration $(1-D)T$ and amplitude $V_S/(1-D)$. Neglecting losses, the average value of the output voltage is V_S. To obtain an average value of the output voltage greater than V_S, a capacitor must be connected in parallel with

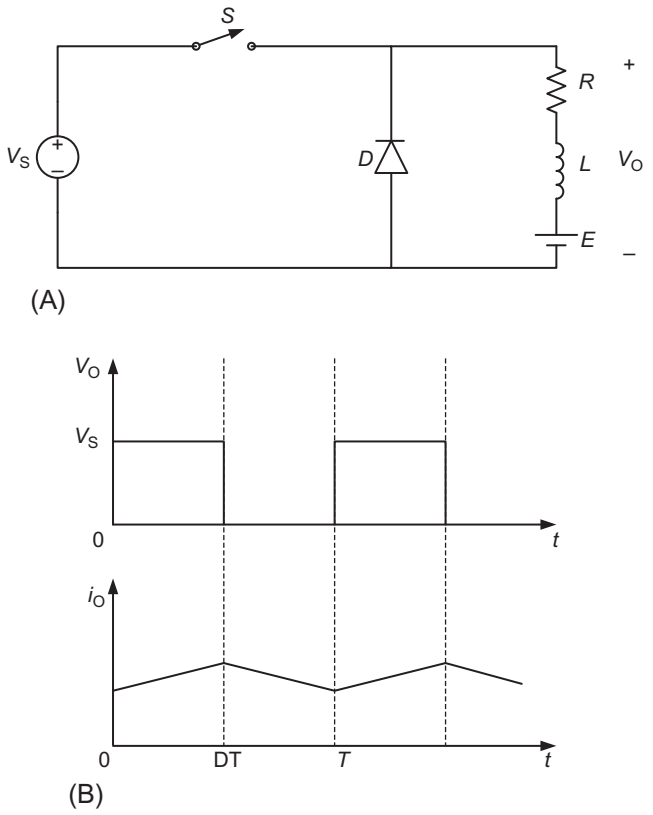


FIG. 10.2 DC chopper with RLE load, (A) circuit diagram and (B) waveforms.

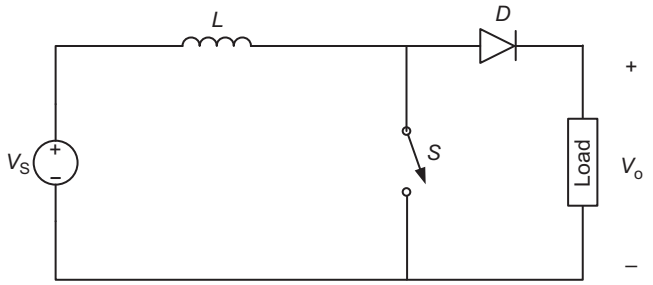


FIG. 10.3 The dc step-up chopper.

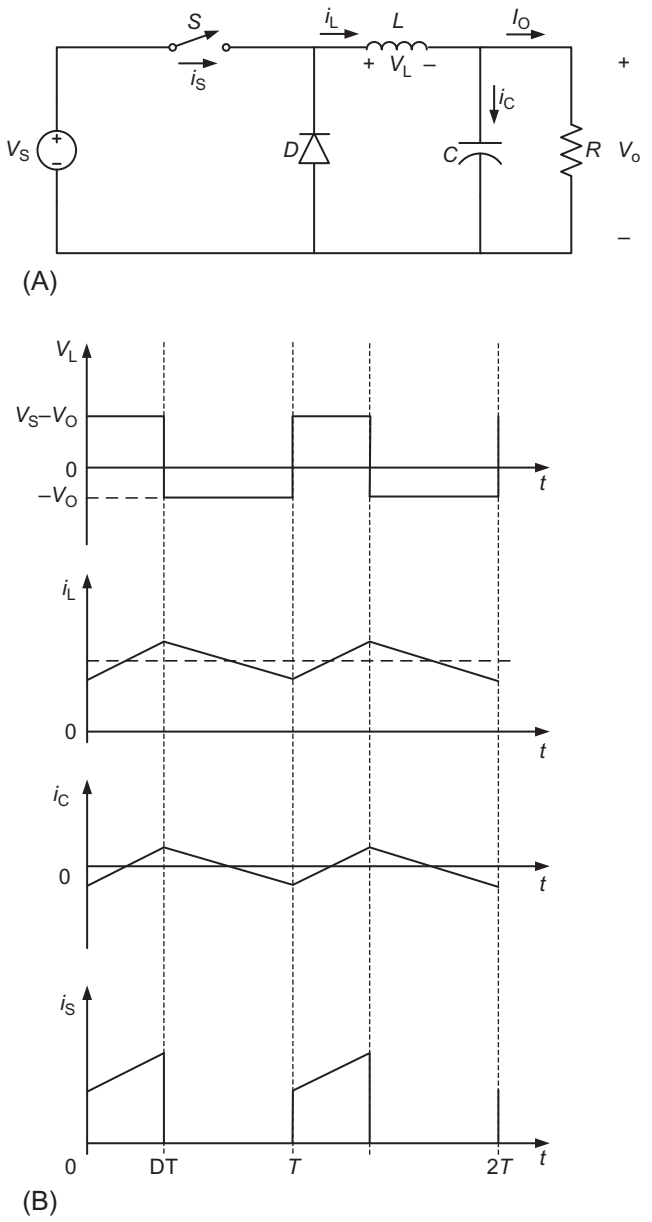


FIG. 10.4 Buck converter: (A) circuit diagram and (B) waveforms.

the load. This results in a topology of a boost dc-dc converter that is described in Section 10.4.

10.3 Step-Down (Buck) Converter

10.3.1 Basic Converter

The step-down dc-dc converter, commonly known as a buck converter, is shown in Fig. 10.4A. It consists of dc input voltage source V_S, controlled switch *S*, diode *D*, filter inductor *L*, filter capacitor *C*, and load resistance *R*. Typical waveforms in the converter are shown in Fig. 10.4B under assumption that the inductor current is always positive. The state of the converter in which the inductor current is never zero for any period of time is called the continuous conduction mode (CCM). It can be seen from the circuit that when the switch *S* is commanded to the *on* state, the diode *D* is reverse biased. When the switch *S* is off, the diode conducts to support an uninterrupted current in the inductor.

The relationship among the input voltage, output voltage, and the switch duty ratio *D* can be derived, for instance, from the inductor voltage v_L waveform (see Fig. 10.4B). According to Faraday's law, the inductor volt-second product over a period of steady-state operation is zero. For the buck converter,

$$(V_S - V_O)DT = -V_O(1-D)T \tag{10.3}$$

Hence, the dc voltage transfer function, defined as the ratio of the output voltage to the input voltage, is

$$M_V \equiv \frac{V_O}{V_S} = D \tag{10.4}$$

It can be seen from Eq. (10.4) that the output voltage is always smaller than the input voltage.

The dc-dc converters can operate in two distinct modes with respect to the inductor current i_L. Fig. 10.4B depicts the CCM in which the inductor current is always greater than zero. When the average value of the input current is low (high R) and/or the switching frequency f is low, the converter may enter the discontinuous conduction mode (DCM). In the DCM, the inductor current is zero during a portion of the switching period. The CCM is preferred for high efficiency and good utilization of semiconductor switches and passive components. The DCM may be used in applications with special control requirements, since the dynamic order of the converter is reduced (the energy stored in the inductor is zero at the beginning and at the end of each switching period). It is uncommon to mix these two operating modes because of different control algorithms. For the buck converter, the value of the filter inductance that determines the boundary between CCM and DCM is given by

$$L_b = \frac{(1-D)R}{2f} \tag{10.5}$$

For typical values of $D = 0.5$, $R = 10\,\Omega$, and $f = 100\,\text{kHz}$, the boundary is $L_b = 25\,\mu\text{H}$. For $L > L_b$, the converter operates in the CCM.

The filter inductor current i_L in the CCM consists of a dc component I_O with a superimposed triangular ac component. Almost all of this ac component flows through the filter capacitor as a current i_c. Current i_c causes a small voltage ripple across the dc output voltage V_O. To limit the peak-to-peak value of the ripple voltage below certain value V_r, the filter capacitance C must be greater than

$$C_{min} = \frac{(1-D)V_O}{8V_r L f^2} \tag{10.6}$$

At $D = 0.5$, $V_r/V_O = 1\%$, $L = 25\,\mu\text{H}$, and $f = 100\,\text{kHz}$, the minimum capacitance is $C_{min} = 25\,\mu\text{F}$.

Eqs. (10.5) and (10.6) are the key design equations for the buck converter. The input and output dc voltages (hence the duty ratio D) and the range of load resistance R are usually determined by preliminary specifications. The designer needs to determine values of passive components L and C and of the switching frequency f. The value of the filter inductor L is calculated from the CCM/DCM condition using Eq. (10.5). The value of the filter capacitor C is obtained from the voltage ripple condition Eq. (10.6). For the compactness and low conduction losses of a converter, it is desirable to use small passive components. Eqs. (10.5) and (10.6) show that it can be accomplished by using a high switching frequency f. The switching frequency is limited, however, by the type of semiconductor switches used and by switching losses. It should be also noted that values of L and C may be altered by effects of parasitic components in the converter, especially by the equivalent series resistance of the capacitor. The issue of parasitic components in dc-dc converters is discussed in Section 10.7.

10.3.2 Transformer Versions of Buck Converter

In many dc power supplies, a galvanic isolation between the dc or ac input and the dc output is required for safety and reliability. An economical mean of achieving such an isolation is to employ a transformer version of a dc-dc converter. High-frequency transformers are of a small size and weight and provide high efficiency. Their turns ratio can be used to additionally adjust the output voltage level. Among buck-derived dc-dc converters, the most popular are forward converter, push-pull converter, half-bridge converter, and full-bridge converter.

10.3.2.1 Forward Converter

The circuit diagram of a forward converter is depicted in Fig. 10.5. When the switch S is *on*, diode D_1 conducts, and diode D_2 is *off*. The energy is transferred from the input, through the transformer, to the output filter. When the switch is *off*, the state of diodes D_1 and D_2 is reversed. The dc voltage transfer function of the forward converter is

$$M_V = \frac{D}{n} \tag{10.7}$$

where $n = N_1/N_2$.

In the forward converter, the energy-transfer current flows through the transformer in one direction. Hence, an additional winding with diode D_3 is needed to bring the magnetizing current of the transformer to zero. This prevents transformer saturation. The turns ratio N_1/N_3 should be selected in such a way that the magnetizing current decreases to zero during a fraction of the time interval when the switch is *off*.

Eqs. (10.5) and (10.6) can be used to design the filter components. The forward converter is very popular for low-power applications. For medium power levels, converters with

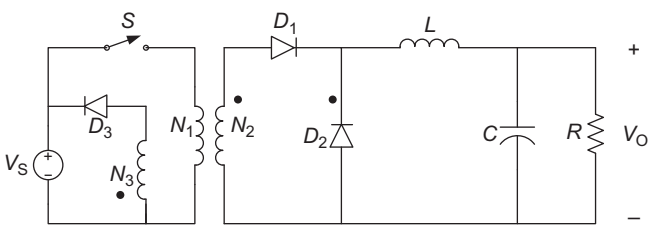


FIG. 10.5 Forward converter.

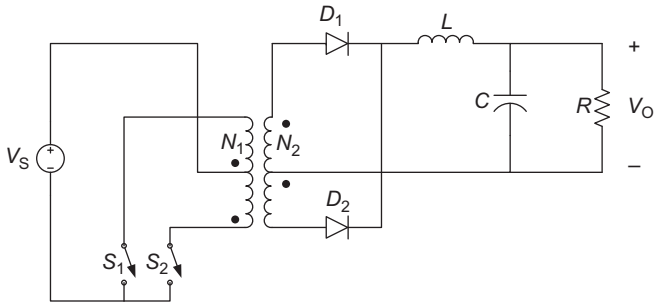


FIG. 10.6 Push-pull converter.

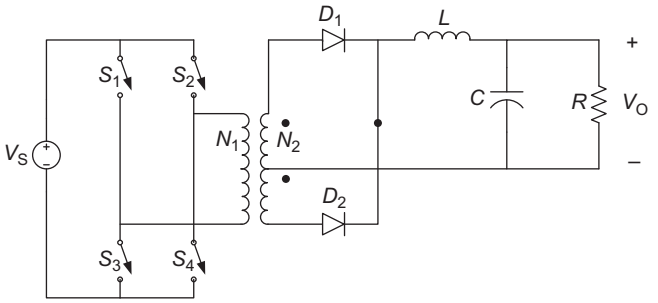


FIG. 10.8 Full-bridge converter.

bidirectional transformer excitation (push-pull, half bridge, and full bridge) are preferred due to better utilization of magnetic components.

10.3.2.2 Push-Pull Converter

The PWM dc-dc push-pull converter is shown in Fig. 10.6. The switches S_1 and S_2 operate shifted in phase by $T/2$ with the same duty ratio D. The duty ratio must be smaller than 0.5. When switch S_1 is *on*, diode D_1 conducts, and diode D_2 is *off*. Diode states are reversed when switch S_2 is *on*. When both controllable switches are *off*, the diodes are *on* and share equally the filter inductor current. The dc voltage transfer function of the push-pull converter is

$$M_V = \frac{2D}{n} \tag{10.8}$$

where $n = N_1/N_2$. The boundary value of the filter inductor is

$$L_b = \frac{(1-2D)R}{4f} \tag{10.9}$$

The filter capacitor can be obtained from

$$C_{min} = \frac{(1-2D)V_O}{32V_r L f^2} \tag{10.10}$$

10.3.2.3 Half-Bridge Converter

Fig. 10.7 shows the dc-dc half-bridge converter. The operation of the PWM half-bridge converter is similar to that of the push-pull converter. In comparison with the push-pull converter, the primary of the transformer is simplified at the expense of two voltage-sharing input capacitors. The half-bridge converter dc voltage transfer function is

$$M_V \equiv \frac{V_D}{V_S} = \frac{D}{n} \tag{10.11}$$

where $D \leq 0.5$. Eqs. (10.9) and (10.10) apply to the filter components of this converter.

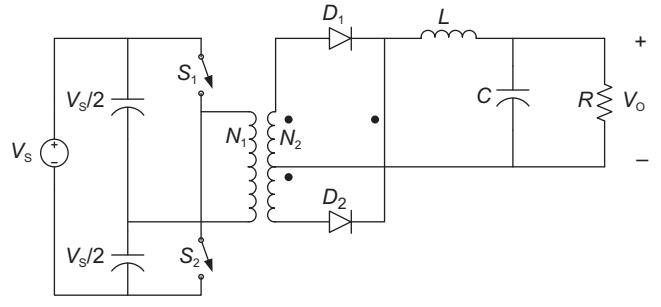


FIG. 10.7 Half-bridge converter.

10.3.2.4 Full-Bridge Converter

Comparing the PWM dc-dc full-bridge converter of Fig. 10.8 with the half-bridge converter, it can be seen that the input capacitors have been replaced by two controllable switches. The controllable switches are operated in pairs. When S_1 and S_4 are *on*, voltage V_S is applied to the primary of the transformer, and diode D_1 conducts. With S_2 and S_3 *on*, there is voltage $-V_S$ across the primary transformer, and diode D_2 is *on*. With all controllable switches *off*, both diodes conduct, similarly as in the push-pull and half-bridge converters. The dc voltage transfer function of the full-bridge converter is

$$M_V \equiv \frac{V_O}{V_S} = \frac{2D}{n} \tag{10.12}$$

where $D \leq 0.5$. Values of filter components can be obtained from Eqs. (10.9) and (10.10).

It should be stressed that the full-bridge topology is a very versatile one. With different control algorithms, it is very popular in dc-ac conversion (square-wave and PWM single-phase inverters). It is also used in four-quadrant dc drives.

10.4 Step-Up (Boost) Converter

Fig. 10.9A depicts a step-up or a PWM boost converter. It is composed of dc input voltage source V_S, boost inductor L, controlled switch S, diode D, filter capacitor C, and load resistance R. The converter waveforms in the CCM are presented in Fig. 10.9B. When the switch S is in the *on* state, the current in the boost inductor increases linearly. The diode D is *off* at

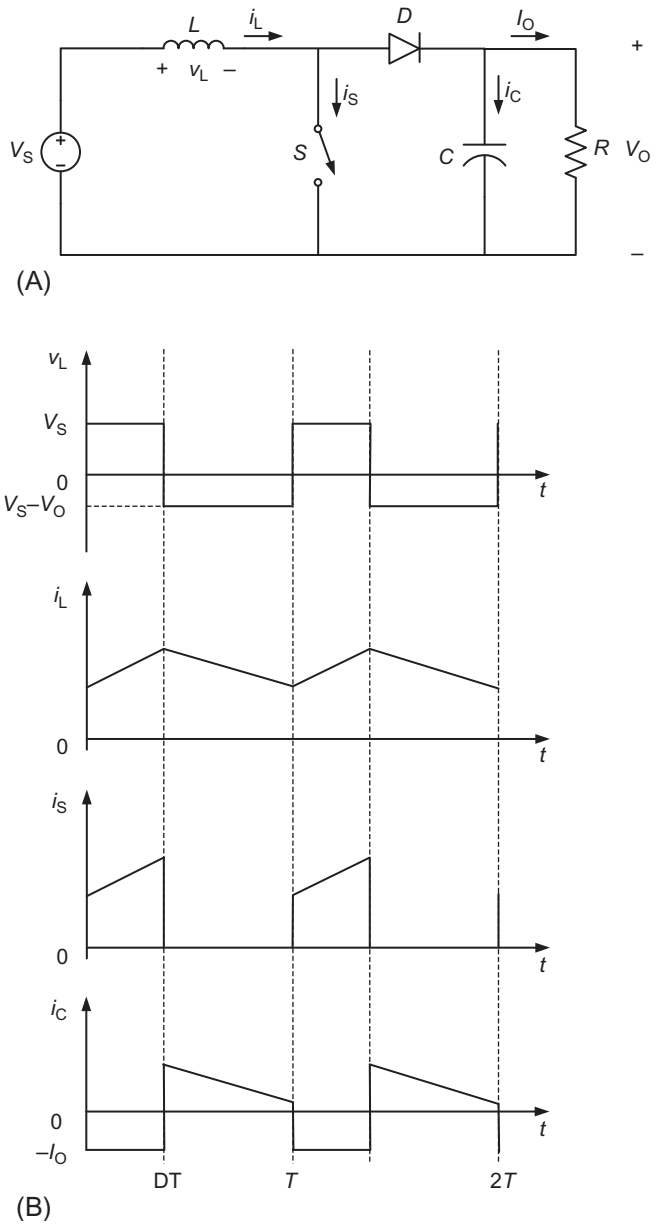


FIG. 10.9 Boost converter: (A) circuit diagram and (B) waveforms.

the time. When the switch S is turned *off*, the energy stored in the inductor is released through the diode to the input RC circuit.

Using the Faraday's law for the boost inductor,

$$V_S DT = (V_O - V_S)(1-D)T \tag{10.13}$$

from which the dc voltage transfer function turns out to be

$$M_V \equiv \frac{V_O}{V_S} = \frac{1}{1-D} \tag{10.14}$$

As the name of the converter suggests, the output voltage is always greater than the input voltage.

The boost converter operates in the CCM for $L > L_b$ where

$$L_b = \frac{(1-D)^2 DR}{2f} \tag{10.15}$$

For $D = 0.5$, $R = 10\,\Omega$, and $f = 100\,\text{kHz}$, the boundary value of the inductance is $L_b = 6.25\,\mu\text{H}$.

As shown in Fig. 10.9B, the current supplied to the output RC circuit is discontinuous. Thus, a larger filter capacitor is required in comparison with that in the buck-derived converters to limit the output voltage ripple. The filter capacitor must provide the output dc current to the load when the diode D is *off*. The minimum value of the filter capacitance that results in the voltage ripple V_r is given by

$$C_{min} = \frac{DV_O}{V_r Rf} \tag{10.16}$$

At $D = 0.5$, $V_r/V_O = 1\%$, $R = 10\,\Omega$, and $f = 100\,\text{kHz}$, the minimum capacitance for the boost converter is $C_{min} = 50\,\mu\text{F}$.

The boost converter does not have a popular transformer (isolated) version.

10.5 Buck-Boost Converter

10.5.1 Basic Converter

A nonisolated (transformerless) topology of the buck-boost converter is shown in Fig. 10.10A. The converter consists of dc input voltage source V_S, controlled switch S, inductor L, diode D, filter capacitor C, and load resistance R. With the switch *on*, the inductor current increases, while the diode is maintained *off*. When the switch is turned *off*, the diode provides a path for the inductor current. Note the polarity of the diode that results in its current being *drawn from* the output.

The buck-boost converter waveforms are depicted in Fig. 10.10B. The condition of a zero volt-second product for the inductor in steady state yields

$$V_S DT = -V_O(1-D)T \tag{10.17}$$

Hence, the dc voltage transfer function of the buck-boost converter is

$$M_V \equiv \frac{V_O}{V_S} = -\frac{D}{1-D} \tag{10.18}$$

The output voltage V_O is negative with respect to the ground. Its magnitude can be either greater or smaller (equal at $D = 0.5$) than the input voltage as the converter's name implies.

The value of the inductor that determines the boundary between the CCM and DCM is

$$L_b = \frac{(1-D)^2 R}{2f} \tag{10.19}$$

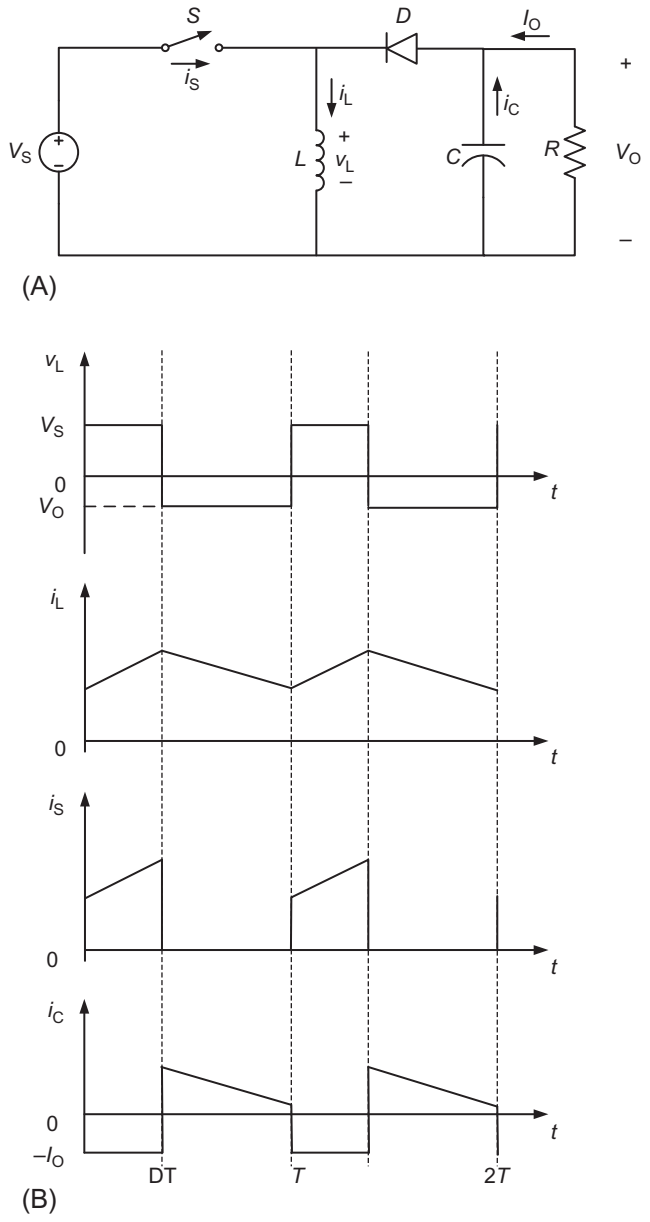


FIG. 10.10 Buck-boost converter: (A) circuit diagram and (B) waveforms.

The structure of the output part of the converter is similar to that of the boost converter (reversed polarities being the only difference). Thus, the value of the filter capacitor can be obtained from Eq. (10.16).

10.5.2 Flyback Converter

A PWM flyback converter is a very practical isolated version of the buck-boost converter. The circuit of the flyback converter is presented in Fig. 10.11A. The inductor of the buck-boost converter has been replaced by a flyback transformer. The input dc source V_S and switch S are connected in series with the primary

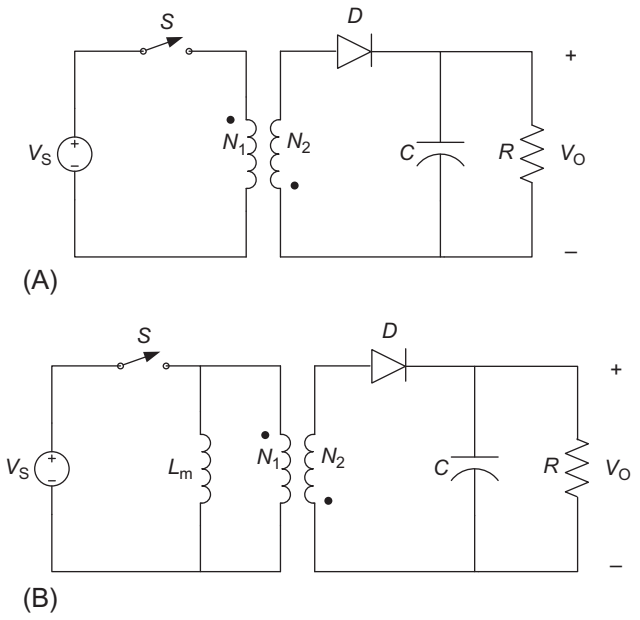


FIG. 10.11 Flyback converter: (A) circuit diagram and (B) circuit with a transformer model showing the magnetizing inductance L_m.

transformer. The diode D and the RC output circuit are connected in series with the secondary of the flyback transformer. Fig. 10.11B shows the converter with a simple flyback transformer model. The model includes a magnetizing inductance L_m and an ideal transformer with a turns ratio $n = N_1/N_2$. The flyback transformer leakage inductances and losses are neglected in the model. It should be noted that leakage inductances, although not important from the principle of operation point of view, affect adversely switch and diode transitions. Snubbers are usually required in flyback converters.

Refer to Fig. 10.11B for the converter operation. When the switch S is *on*, the current in the magnetizing inductance increases linearly. The diode D is *off*, and there is no current in the ideal transformer windings. When the switch is turned *off*, the magnetizing inductance current is diverted into the ideal transformer, the diode turns *on*, and the transformed magnetizing inductance current is supplied to the RC load. The dc voltage transfer function of the flyback converter is

$$M_V \equiv \frac{V_O}{V_S} = \frac{D}{n(1-D)} \tag{10.20}$$

It differs from the buck-boost converter voltage transfer function by the turns ratio factor n. A positive sign has been obtained by an appropriate coupling of the transformer windings.

Unlike in transformer buck-derived converters, the magnetizing inductance L_m of the flyback transformer is an important design parameter. The value of the magnetizing inductance that determines the boundary between the CCM and DCM is given by

$$L_{mb} = \frac{n^2(1-D)^2 R}{2f} \tag{10.21}$$

The value of the filter capacitance can be calculated using Eq. (10.16).

10.6 Ćuk Converter

The circuit of the Ćuk converter is shown in Fig. 10.12A. It consists of dc input voltage source V_S, input inductor L_1, controllable switch S, energy-transfer capacitor C_1, diode D, filter inductor L_2, filter capacitor C, and load resistance R. An important advantage of this topology is a continuous current at both the input and the output of the converter. Disadvantages of the Ćuk converter include a high number of reactive components and high current stresses on the switch, the diode, and the capacitor C_1. Main waveforms in the converter are presented in Fig. 10.12B. When the switch is *on*, the diode is *off*, and the capacitor C_1 is discharged by the inductor L_2 current. With the switch in the *off* state, the diode conducts currents of the inductors L_1 and L_2, whereas capacitor C_1 is charged by the inductor L_1 current.

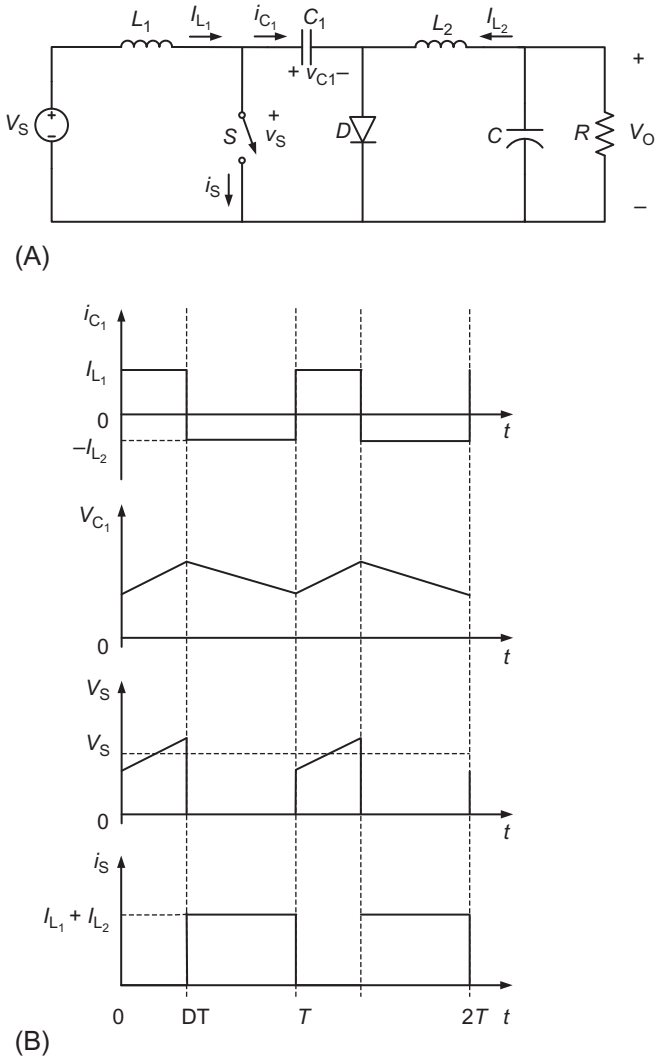


FIG. 10.12 Ćuk converter: (A) circuit diagram and (B) waveforms.

To obtain the dc voltage transfer function of the converter, we shall use the principle that the average current through a capacitor is zero for steady-state operation. Let us assume that inductors L_1 and L_2 are large enough that their ripple current can be neglected. Capacitor C_1 is in a steady state if

$$I_{L_2} DT = I_{L_1}(1-D)T \tag{10.22}$$

For a lossless converter,

$$P_S = V_S I_{L_1} = -V_O I_{L_2} = P_O \tag{10.23}$$

Combining these two equations, the dc voltage transfer function of the Ćuk converter is

$$M_V \equiv \frac{V_O}{V_S} = -\frac{D}{1-D} \tag{10.24}$$

This voltage transfer function is the same as that for the buck-boost converter.

The boundaries between the CCM and DCM are determined by

$$L_{b1} = \frac{(1-D)R}{2Df} \tag{10.25}$$

for L_1 and

$$L_{b2} = \frac{(1-D)R}{2f} \tag{10.26}$$

for L_2.

The output part of the Ćuk converter is similar to that of the buck converter. Hence, the expression for the filter capacitor C is

$$C_{min} = \frac{(1-D)V_O}{8V_r L_2 f^2} \tag{10.27}$$

The peak-to-peak ripple voltage in the capacitor C_1 can be estimated as

$$V_{r1} = \frac{DV_O}{C_1 Rf} \tag{10.28}$$

A transformer (isolated) version of the Ćuk converter can be obtained by splitting capacitor C_1 and inserting a high-frequency transformer between the split capacitors.

10.7 Effects of Parasitic Components

The analysis of converters in Sections 10.2–10.6 has been performed under ideal switch, diode, and passive component

assumptions. Nonidealities or parasitics of practical devices and components may, however, greatly affect some performance parameters of dc-dc converters. In this section, effects of parasitics on output voltage ripple, efficiency, and voltage transfer function of converters will be illustrated.

A more realistic model of a capacitor than just a capacitance C consists of a series connection of capacitance C and resistance r_C. The resistance r_C is called an equivalent series resistance (ESR) of the capacitor and is due to losses in the dielectric and physical resistance of leads and connections. Recall Eq. (10.6) that provided a value of the filter capacitance in a buck converter that limits the peak-to-peak output voltage ripple to V_r. The equation was derived under an assumption that the entire triangular ac component of the inductor current flows through a capacitance C. It is, however, closer to reality to maintain that this triangular component flows through a series connection of capacitance C and resistance r_C.

The peak-to-peak ripple voltage is independent of the voltage across the filter capacitor and is determined only by the ripple voltage of the ESR if the following condition is satisfied:

$$C \geq C_{\min} = \max\left\{\frac{1-D_{\min}}{2r_C f}, \frac{D_{\max}}{2r_C f}\right\} \tag{10.29}$$

If condition (10.29) is satisfied, the peak-to-peak ripple voltage of the buck and forward converters is

$$V_r = r_C \Delta i_{L\max} = \frac{r_C V_O (1-D_{\min})}{fL} \tag{10.30}$$

For push-pull, half-bridge, and full-bridge converters,

$$C \geq C_{\min} = \max\left\{\frac{0.5-D_{\min}}{2r_C f}, \frac{D_{\max}}{2r_C f}\right\} \tag{10.31}$$

where $D_{\max} \leq 0.5$. If condition (10.31) is met, the peak-to-peak ripple voltage V_r of these converters is given by

$$V_r = r_C \Delta i_{L\max} = \frac{r_C V_O (0.5-D_{\min})}{fL} \tag{10.32}$$

Waveforms of voltage across the ESR V_{rC}, voltage across the capacitance V_C, and total ripple voltage V_r are depicted in Fig. 10.13 for three values of the filter capacitances. For the case of the top graph in Fig. 10.13, the peak-to-peak value of V_r is higher than the peak-to-peak value of V_{rC} because $C < C_{\min}$. Middle and bottom graphs in Fig. 10.13 show the waveforms for $C = C_{\min}$ and $C > C_{\min}$, respectively. For both these cases, the peak-to-peak voltages of V_r and V_{rC} equal to each other.

Note that when the resistance r_C sets the ripple voltage V_r, the minimum value of inductance L is determined either by the boundary between the CCM and DCM according to Eq. (10.5) (buck and forward converters) or Eq. (10.9) (push-pull, half-bridge, and full-bridge converters) or by the voltage ripple condition (10.30) or (10.32).

In buck-boost and boost converters, the peak-to-peak capacitor current I_{Cpp} is equal to the peak-to-peak diode current and is given by

$$I_{Cpp} = \frac{I_O}{1-D} \tag{10.33}$$

under condition that the inductor current ripple is much lower than the average value of the inductor current. The peak-to-peak voltage across the ESR is

$$V_{rC} = r_C I_{Cpp} = \frac{r_C I_O}{1-D} \tag{10.34}$$

$L = 40\,\mu\text{H}$, $r_C = 0.05\,\Omega$, and various values of C: $C = 33\,\mu\text{F}$ (top graph), $C = C_{\min} = 65\,\mu\text{F}$ (middle graph), and $C = 100\,\mu\text{F}$ (bottom graph).

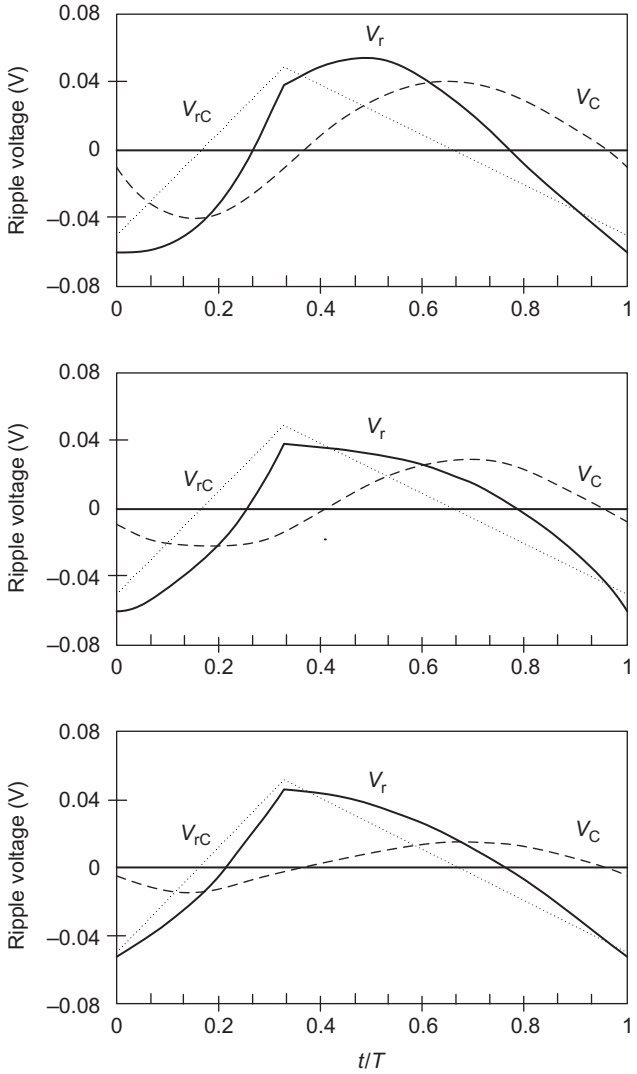


FIG. 10.13 Voltage ripple waveforms V_{rC}, V_C, and V_r for a buck converter at $V_O = 12\,\text{V}$, $f = 100\,\text{kHz}$.

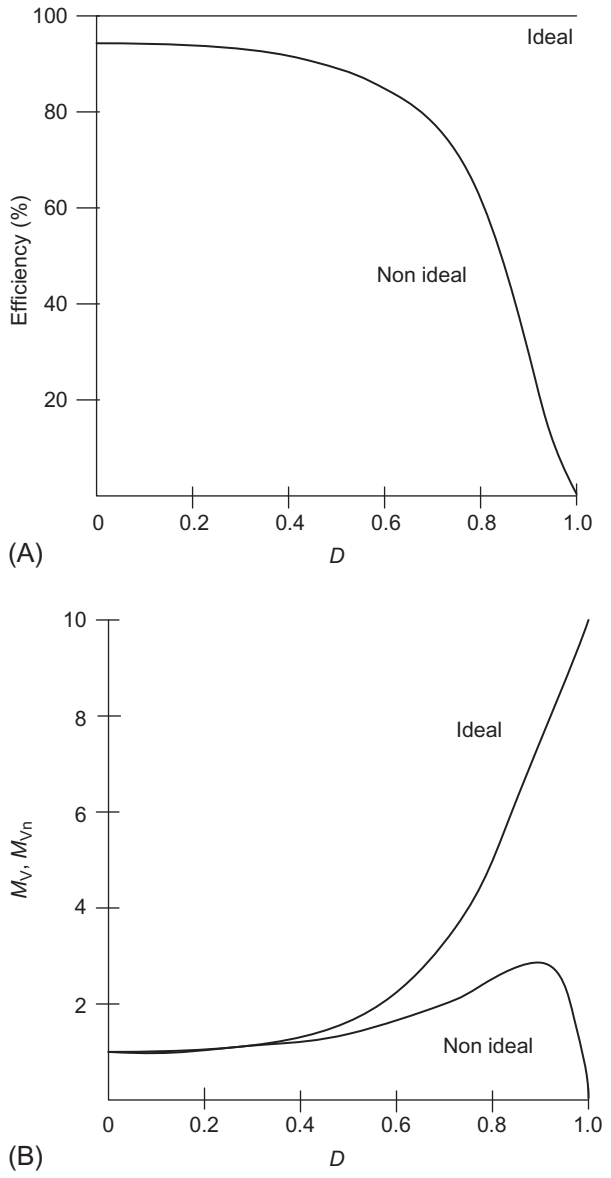


FIG. 10.14 Effects of parasitics on characteristics of a boost converter, (A) efficiency and (B) dc voltage transfer function.

Assuming that the total ripple voltage V_r is approximately equal to the sum of the ripple voltages across the ESR and the capacitance, the maximum value of the peak-to-peak ripple voltage across the capacitance is

$$V_{Cmax} \approx V_r - V_{rC} \tag{10.35}$$

Finally, by analogy to Eq. (10.16), when the ESR of the filter capacitor is taken into account in the boost-type output filter, the filter capacitance should be greater than

$$C_{min} = \frac{DV_O}{V_{Cmax} Rf} \tag{10.36}$$

Parasitic resistances, capacitances, and voltage sources affect also an energy conversion efficiency of dc-dc converters. The efficiency η is defined as a ratio of output power to the input power:

$$\eta \equiv \frac{P_O}{P_S} = \frac{V_O I_O}{V_S I_S} \tag{10.37}$$

Efficiencies are usually specified in percent. Let us consider the boot converter as an example. Under low ripple assumption, the boost converter efficiency can be estimated as

$$\eta = \frac{R(1-D)^2}{R(1-D)^2(1+(V_D/V_O)+fC_oR)+r_L+Dr_S+(1-D)r_D+D(1-D)r_C} \tag{10.38}$$

where V_D is the forward conduction voltage drop of the diode, C_o is the output capacitance of the switch, r_L is the ESR of the inductor, and r_D is the forward *on* resistance of the diode. The term fC_oR in Eq. (10.38) represents switching losses in the converter. Other terms account for conduction losses. Losses in a dc-dc converter also contribute to a decrease in the dc voltage transfer function. The nonideal dc voltage transfer function M_{Vn} is a product of the ideal one and the efficiency:

$$M_{Vn} = \eta M_V \tag{10.39}$$

Sample graphs for the boost converter that correspond to Eqs. (10.38) and (10.39) are presented in Fig. 10.14.

10.8 Synchronous and Bidirectional Converters

It can be observed in Eq. (10.38) that the forward voltage of a diode V_D contributes to a decrease in efficiency. This contribution is especially significant in low-output-voltage power supplies, for example, 3.3 V power supplies for microprocessors or power supplies for portable telecommunication equipment. Even with a Schottky diode, which has V_D in the range of 0.4 V, the power loss in the diode can easily exceed 10% of the total power delivered to the load. To reduce conduction losses in the diode, a low on-resistance switch can be added in parallel as shown in Fig. 10.15 for a buck converter. The input switch and the switch parallel to the diode must be turned on and off alternately. The arrangement of Fig. 10.15 is called a synchronous converter or a synchronous rectifier. Modern low-voltage MOSFETs have *on* resistances of only several milliohms. Hence, a synchronous converter may exhibit higher efficiency than a conventional one at output currents as large as tens of amperes. The efficiency is increased at an expense of more complicated driving circuitry for the switches. In particular, a special can must be exercised to avoid having both switches *on* at the same time as this would short the input voltage source. Since power semiconductor devices usually have

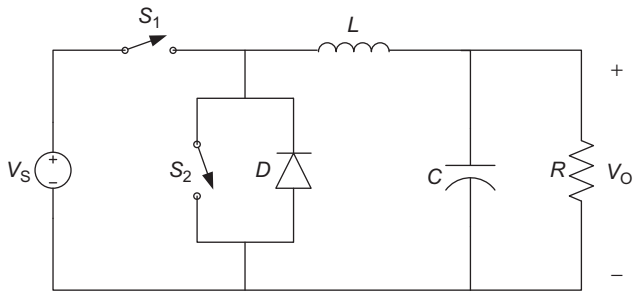


FIG. 10.15 Synchronous buck converter.

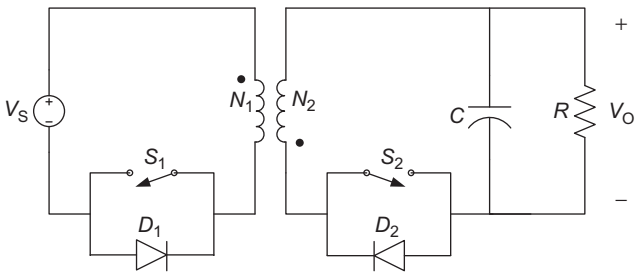


FIG. 10.16 Bidirectional flyback converter.

longer turn-off times than turn-on times, a dead time (sometimes called a blanking time) must be introduced in PWM driving signals.

The parallel combination of a controllable switch and a diode is also used in converters that allow for a current flow in both directions: from the input source to the load and from the load back to the input source. Such converters are called bidirectional power flow or simply bidirectional converters. As an example, a flyback bidirectional converter is shown in Fig. 10.16. It contains unipolar voltage and bidirectional current switch-diode combinations at both primary and secondary of the flyback transformer. When the primary switch and secondary diode operate, the current flows from the input source to the load. The converter current can also flow from the output to the input through the secondary switch and primary diode. Bidirectional arrangements can be made for buck and boost converters. A bidirectional buck converter operates as a boost converter when the current flow is from the output to the input. A bidirectional boost converter operates as a buck converter with a reversed current flow. If for any reason (for instance, to avoid the DCM) the controllable switches are driven at the same time, they must be driven alternately with a sufficient dead time to avoid a shot-through current.

10.9 Control Principles

A dc-dc converter must provide a regulated dc output voltage under varying load and input voltage conditions. The converter component values are also changing with time, temperature, pressure, etc. Hence, the control of the output voltage should be performed in a closed-loop manner using principles of negative feedback. Two most common closed-loop control methods for PWM dc-dc converters, namely, the voltage-mode control and the current-mode control, are presented schematically in Fig. 10.17.

In the voltage-mode control scheme shown in Fig. 10.17A, the converter output voltage is sensed and subtracted from an external reference voltage in an error amplifier. The error amplifier produces a control voltage that is compared to a constant-amplitude sawtooth waveform. The comparator produces a PWM signal that is fed to drivers of controllable switches in the dc-dc converter. The duty ratio of the PWM signal depends on the value of the control voltage. The frequency of the PWM signal is the same as the frequency of the sawtooth waveform. An important advantage of the voltage-mode control is its simple hardware implementation and flexibility.

The error amplifier in Fig. 10.17A reacts fast to changes in the converter output voltage. Thus, the voltage-mode control provides good load regulation, that is, regulation against variations in the load. Line regulation (regulation against variations in the input voltage) is, however, delayed because changes in the input voltage must first manifest themselves in the converter output before they can be corrected. To alleviate this problem, the voltage-mode control scheme is sometimes augmented by the so-called voltage feedforward path. The feedforward path affects directly the PWM duty ratio according to variations in the input voltage. As will be explained below, the input voltage feedforward is an inherent feature of current-mode control schemes.

The current-mode control scheme is presented in Fig. 10.17B. An additional inner control loop feeds back an inductor current signal. This current signal, converted into its voltage analog, is compared with the control voltage. This modification of replacing the sawtooth waveform of the voltage-mode control scheme by a converter current signal significantly alters the dynamic behavior of the converter. The converter takes on some characteristics of a current source. The output current in PWM dc-dc converters is either equal to the *average* value of the output inductor current (buck-derived and Ćuk converters) or a product of an *average* inductor current and a function of the duty ratio. In practical implementations of the current-mode control, it is feasible to sense the peak inductor current instead of the average value. Since the peak inductor current is equal to the peak switch current, the latter can be used in the inner loop, which often simplifies the current sensor. Note that the peak inductor (switch) current is proportional to the input voltage. Hence, the inner loop of the current-mode control naturally accomplishes the input voltage feedforward technique. Among several current-mode control versions, the most popular is the constant frequency one that requires a clock signal. Advantages of the current-mode control include input voltage feedforward, limit on the peak switch current, equal current sharing in modular converters, and reduction in the converter dynamic order.

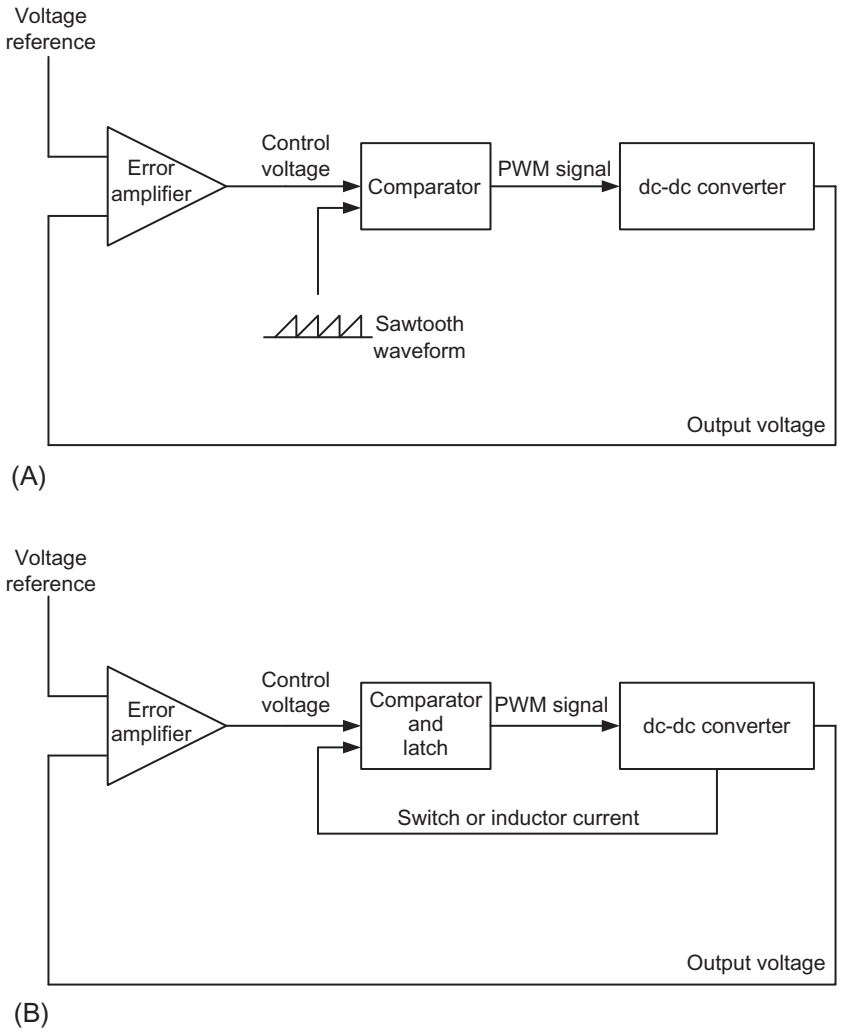


FIG. 10.17 Main control schemes for dc-dc converters, (A) voltage-mode control and (B) current-mode control.

The main disadvantage of the current-mode control is its complicated hardware that includes a need to compensate the control voltage by ramp signals (to avoid converter instability).

Among other control methods of dc-dc converters, a hysteretic (or bang-bang) control is very simple for hardware implementation. The hysteretic control results, however, in variable frequency operation of semiconductor switches. Generally, a constant switching frequency is preferred in power electronic circuits for easier elimination of electromagnetic interference and better utilization of magnetic components.

Application-specific integrated circuits (ASICs) are commercially available that contain main elements of voltage- or current-mode control schemes. On a single 14- or 16-pin chip, there is error amplifier, comparator, sawtooth generator, or sensed current input, latch, and PWM drivers. The switching frequency is usually set by an external *RC* network and can be varied from tens of kilohertz to a few megahertz. The controller has an oscillator output for synchronization with other converters in modular power supply systems. A constant voltage reference is generated on the chip as well. Additionally, the ASIC controller may be equipped in various diagnostic and protection features: current limiting, overvoltage and undervoltage protection, soft start, dead time in case of multiple PWM outputs, and duty ratio limiting. In several dc-dc converter topologies, for example, buck and buck-boost, neither control terminal of semiconductor switches is grounded (so-called high-side switches). The ASIC controllers are usually designed for a particular topology, and their PWM drivers may be able to drive high-side switches in low-voltage applications. In high-voltage applications, external PWM drivers must be used. External PWM drivers are also used for switches with high input capacitances. To take a full advantage of the input-output isolation in transformer versions of dc-dc converters, such an isolation must be also provided in the control loop. Signal transformers or optocouplers are used for isolating feedback signals.

Dynamic characteristic of closed-loop dc-dc converters must fulfill certain requirements. To simple analysis, these

requirements are usually translated into desired properties of the open loop. The open loop should provide a sufficient (typically, at least 45 degrees) phase margin for stability, high bandwidth (about one-tenth of the switching frequency) for good transient response, and high gain (several tens of decibels) at low frequencies for small steady-state error.

The open-loop dynamic characteristics are shaped by compensating networks of passive components around the error amplifier. Second- or third-order *RC* networks are commonly used. Since the converter itself is a part of the control loop, the design of compensating networks requires a knowledge of small-signal characteristics of the converter. There are several methods of small-signal characterization of PWM dc-dc converters. The most popular methods provide average models of converters under high-switching-frequency assumption. The averaged models are then linearized at an operating point to obtain small-signal transfer functions. Among analytic averaging methods, state-space averaging has been popular since the late 1970s. Circuit-based averaging is usually performed using PWM switch or direct replacement of semiconductor switches by controlled current and voltage sources. All these methods can take into account converter parasitics.

The most important small-signal characteristic is the *control-to-output* transfer function T_p. Other converter characteristics that are investigated include the *input-to-output* (or *line-to-output*) voltage transfer function, also called the *open-loop dynamic line regulation* or the *audio susceptibility*, which describes the input-output disturbance transmission; the *open-loop input impedance*; and the *open-loop dynamic load regulation*. Buck-derived, boost, and buck-boost converters are second-order dynamic systems; the Ćuk converter is a fourth-order system. Characteristics of buck and buck-derived converters are similar to each other. Another group of converters with similar small-signal characteristics is formed by boost, buck-boost, and flyback converters. Among parasitic components, the ESR of the filter capacitor r_C introduces additional dynamic terms into transfer functions. Other parasitic resistances usually modify slightly the effective value of the load resistance. Sample characteristics below are given for nonzero r_C, neglecting other parasitics.

The control-to-output transfer function of the forward converter is

$$T_p(s) \equiv \frac{v_o(s)}{d(s)}\Big|_{v_s(s)=0} = \frac{V_I R r_C}{nL(R+r_C)} \times \frac{s+(1/Cr_C)}{s^2+s(CRr_C+L/LC(R+r_C))+R/(LC(R+r_C))} \tag{10.40}$$

It can be seen that this transfer function has two poles and one zero. The zero is due to the filter capacitor ESR. Buck-derived converters can be easily compensated for stability with second-order controllers.

The control-to-output transfer function of the boost converter is given by

$$T_p(s) = -\frac{V_O r_C}{(1-D)(R+r_C)} \times \frac{[s+(1/Cr_C)]\left[s-\left((1-D)^2R\right)/L\right]}{s^2+s\left[\left((1-D)^2CRr_C+L\right)/(LC(R+r_C))\right]+\left[\left((1-D)^2R\right)/(LC(R+r_C))\right]} \tag{10.41}$$

The zero $-(1-D)^2R/L$ is located in the right half of the s-plane. Therefore, the boost converter (and buck-boost and flyback converters) is a nonminimum phase system. Nonminimum phase dc-dc converters are typically compensated with third-order controllers. Step-by-step procedures for a design of compensating networks are usually given by manufacturers of ASIC controllers in application notes.

The final word of this section is on the behavior of dc-dc converters in distributed power supply systems. An important feature of closed-loop regulated dc-dc converters is that they exhibit a negative input resistance. As the load voltage is kept constant by the controller, the output power changes with the load. With slow load changes, an increase (decrease) in the input voltage results in a decrease (increase) in the input power. This negative resistance property must be carefully examined during the system design to avoid resonances.

10.10 Applications of DC-DC Converters

Step-down choppers find most of their applications in high-performance dc drive systems, for example, electric traction, electric vehicles, and machine tools. The dc motors with their winding inductances and mechanical inertia act as filters resulting in high-quality armature currents. The average output voltage of step-down choppers is a linear function of the switch duty ratio. Step-up choppers are used primarily in radar and ignition systems. The dc choppers can be modified for two-quadrant and four-quadrant operation. Two-quadrant choppers may be a part of autonomous power supply system that contain battery packs and such renewable dc sources as photovoltaic arrays, fuel cells, or wind turbines. Four-quadrant choppers are applied in drives in which regenerative breaking of dc motors is desired, for example, transportation systems with frequent stops. The dc choppers with inductive outputs serve as inputs to current-driven inverters.

An addition of filtering reactive components to dc choppers results in PWM dc-dc converters. The dc-dc converters can be viewed as dc transformers that deliver to the load as dc voltage or current at a different level than the input source. This dc transformation is performed by electronic switching means, not by electromagnetic means like in conventional transformers. Output voltages of dc-dc converters range from a volt for special VLSI circuits to tens of kilovolts in x-ray lamps. The most common output voltages are 3.3 V for modern

microprocessors, 5 and 12 V for logic circuits, 48 V for telecommunication equipment, and 270 V for main dc bus on airplanes. Typical input voltages include 48, 170 (the peak value of a 120 V rms line), and 270 V.

Selection of a topology of dc-dc converters is determined not only by input/output voltages, which can be additionally adjusted with the turns ratio in isolated converters, but also by power levels, voltage and current stresses of semiconductor switches, and utilization of magnetic components. The low part-count flyback converter is popular in low-power applications (up to 200 W). Its main deficiencies are the large size of the flyback transformer core and high voltage stress on the semiconductor switch. The forward converter is also a single-switch converter. Since its core size requirements are smaller, it is popular in low-/medium (up to several hundreds of watts)-power applications. Disadvantages of the forward converter are in a need for demagnetizing winding and in a high voltage stress on the semiconductor switch. The push-pull converter is also used at medium power levels. Due to bidirectional excitation, the transformer size is small. An advantage of the push-pull converter is also a possibility to refer driving terminals of both switches to the ground, which greatly simplifies the control circuitry. A disadvantage of the push-pull converter is a potential core saturation in a case of asymmetry. The half-bridge converter has similar range of applications as the push-pull converter. There is no danger of transformer saturation in the half-bridge converter. It requires, however, two additional input capacitors to split in half the input dc source. The full-bridge converter is used at high (several kilowatts) power and voltage levels. The voltage stress on power switches is limited to the input voltage source value. A disadvantage of the full-bridge converter is a high number of semiconductor devices.

The dc-dc converters are building blocks of distributed power supply systems in which a common dc bus voltage is converted to various other voltages according to the requirements of particular loads. Such distributed dc systems are common in space stations, ships, and airplanes, as well as in computer and telecommunication equipment. It is expected that modern portable wireless communication and signal processing systems will use variable supply voltages to minimize power consumption and extend battery life. Low-output-voltage converters in these applications utilize the synchronous rectification arrangement.

Another big area of dc-dc converter applications is related to the utility ac grid. For critical loads, if the utility grid fails, there must be a backup source of energy, for example, a battery pack. This need for continuous power delivery gave rise to various types of uninterruptible power supplies (UPSs). The dc-dc converters are used in UPSs to adjust the level of a rectified grid voltage to that of the backup source. Since during normal operation the energy flows from the grid to the backup source and during emergency conditions the backup source must supply the load, bidirectional dc-dc converters are often used. The dc-dc converters are also used in dedicated battery chargers.

Power electronic loads, especially those with front-end rectifiers, pollute the ac grid with odd harmonics. The dc-dc converters are used as intermediate stages, just after a rectifier and before the load-supplying dc-dc converter, for shaping the input ac current to improve power factor and decrease the harmonic content. The boost converter is especially popular in such power-factor-correction (PFC) applications. Another utility grid-related application of dc-dc converters is in interfaces between ac networks and dc renewable energy sources such as fuel cells and photovoltaic arrays.

In isolated dc-dc converters, multiple outputs are possible with additional secondary windings of transformers. Only one output is regulated with a feedback loop. Other outputs depend on the duty ratio of the regulated one and on their loads. A multiple-output dc-dc converter is a convenient solution in application where there is a need for one closely regulated output voltage and for one or more noncritical other output voltage levels.

Further Reading

[1] R.P. Severns, G. Bloom, Modern DC-to-DC Switchmode Power Converter Circuits, Van Nostrand Reinhold Company, New York, NY, 1985.
[2] A.I. Pressman, Switching Power Supply Design, second ed., McGraw-Hill, New York, NY, 1998.
[3] R. Erickson, D. Maksimovic, Fundamentals of Power Electronics, second ed., Kluwer Academic, Norwell, MA, 2001.
[4] N. Mohan, T.M. Undeland, W.P. Robbins, Power Electronics: Converters, Applications and Design, third ed., John Wiley & Sons, New York, NY, 2003.
[5] D.W. Hart, Power Electronics, McGraw-Hill, New York, NY, 2010.
[6] A. Ioinovici, Power Electronics and Energy Conversion Systems, Fundamentals and Hard-Switching Converters, Wiley, New York, NY, 2013.
[7] M.H. Rashid, Power Electronics Circuits, Devices, and Applications, fourth ed., Pearson Prentice Hall, Upper Saddle River, NJ, 2013.
[8] P.T. Krein, Elements of Power Electronics, second ed., Oxford University Press, New York, NY, 2014.
[9] M.K. Kazimierczuk, Pulse-Width Modulated DC-DC Power Converters, second ed., Wiley, New York, NY, 2015.
[10] A.M. Trzynadlowski, Introduction to Modern Power Electronics, third ed., Wiley, New York, NY, 2015.

11

Inverters

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11.1 Introduction

To produce an ac output waveform from a dc power supply is the main objective of inverters. These types of converters are required in many applications, like adjustable speed drives (ASDs), uninterruptible power supplies, static var compensators, active power filters, flexible ac transmission systems, and grid-connected photovoltaic systems, which are only a few applications. For sinusoidal ac outputs, the magnitude, frequency, and phase of the waveform should be controllable. In the literature, different topologies have been reported; one of the most known converters is the voltage-source inverters (VSIs), but current-source inverters (CSIs) and impedance-source inverters (ISIs) can also be found; in Fig. 11.1, a classification of inverters is illustrated that considers the input source. The VSIs are the most widely used because they naturally behave as voltage sources as required by many industrial applications, such as ASDs, which are the most popular application of inverters. Similarly, the other topologies are widely used in medium-voltage industrial or low-power commercial applications.

The inverters are constructed from power switches and diodes. This leads to the generation of waveforms that feature fast transitions rather than smooth ones. These waveforms are made up of a fundamental component that behaves as a pure sinusoidal and an infinite number of harmonics. This behavior should be ensured by a modulating technique that controls the amount of time and the sequence used to switch the power semiconductors on and off. The modulating techniques mostly used are the carrier-based technique (e.g., sinusoidal pulse width modulation, SPWM), the space-vector (SV) technique, and the selective harmonic elimination (SHE) technique.

As an alternative not only to produce an inverter output with low harmonic content but also to avoid the negative side effects of high dv/dt (such as bearing and isolation problems), the multilevel topologies should be used. The basic principle is

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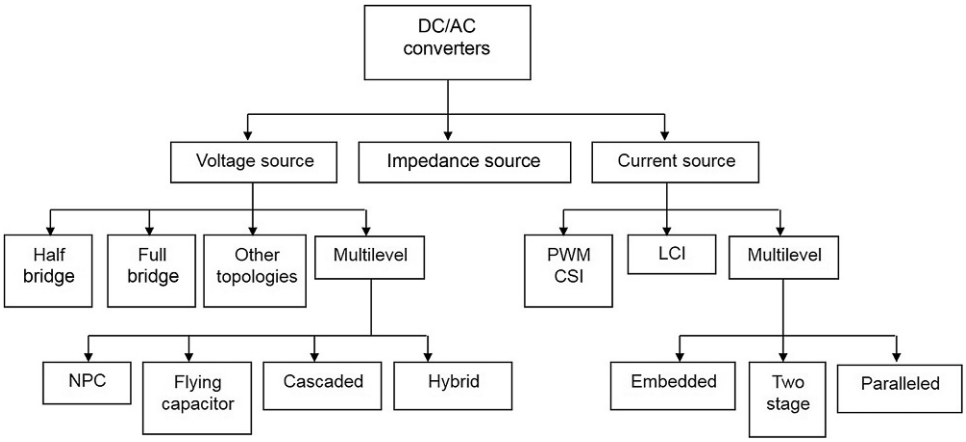


FIG. 11.1 Classification of the inverters.

to construct the required ac output waveform from various levels, which achieves waveforms at reduced dv/dt. Although these topologies are well developed in ASDs, they are also suitable for static var compensators, active power filters, and so on. Specialized modulating techniques have been developed to switch the higher number of power semiconductors involved in these topologies. Among others, the carrier-based (SPWM) and SV-based techniques have been naturally extended to these applications.

In many applications, it is required to take energy from the ac side of the inverter and send it back into the dc side. For instance, whenever ASDs need to either brake or slow down the motor speed, the kinetic energy is sent into the voltage dc link. This is known as the regenerative operating mode, and in contrast to the motoring mode, the dc link current direction is reversed due to the fact that the dc link voltage is fixed. If a capacitor is used to maintain the dc link voltage (as in standard ASDs), the energy must be either dissipated or fed back into the distribution system; otherwise, the dc link voltage gradually increases. The first approach requires the dc link capacitor be connected in parallel with a resistor, which must be properly switched only when the energy flows from the motor to the dc link. A better alternative is to feed back such energy into the distribution system. However, this alternative requires a reversible-current topology connected between the distribution system and the dc link capacitor. A modern approach to such a requirement is to use the active front-end rectifier technologies, where the regeneration mode is a natural operating mode of the system.

In this chapter, not only single-phase inverters in their voltage-, current-, and impedance-source alternatives but also the three-phase inverters in their voltage- and current-source configurations will be reviewed. Specifically, the topologies, the modulating techniques, and the control aspects oriented to standard applications are analyzed. In order to simplify the analysis, the inverters are considered lossless topologies, and the dc link will be assumed to be a perfect dc. Nevertheless, some practical nonideal conditions are also considered.

11.2 Single-Phase Inverters

Single-phase inverters can be classified by its input source; they are VSIs, CSIs, and ISIs. The operating principles are different in each converter. The main features of the different approaches are reviewed and presented in the following subsections. Although these converters cover the low-power range, they are widely used in power supplies or single-phase UPSs.

11.2.1 Voltage Source Inverter

The traditional topologies for single-phase VSIs are half bridge and full bridge (Fig. 11.2). The converter is composed of capacitors, switches, and diodes, where an array of two switches is called "inverter leg." For instance, the inverter leg of the half bridge is composed of S_+ and S_-. The capacitors required to provide a neutral point N are large, such that each capacitor maintains a constant voltage.

In order to operate properly the voltage-source inverter, the following rules are compulsory:

1. Switches of the same leg cannot be on simultaneously, because a short circuit across the dc link voltage source v_i would be produced.
2. Diode in antiparallel to each switch must be placed, in order to provide a current path for inductive loads. If the commercial switch includes this diode, then the circuit is already complete.
3. In practical implementation, a dead time, also known as blanking time, must be considered in the control signals of the leg switches, to avoid breaking rule 1.

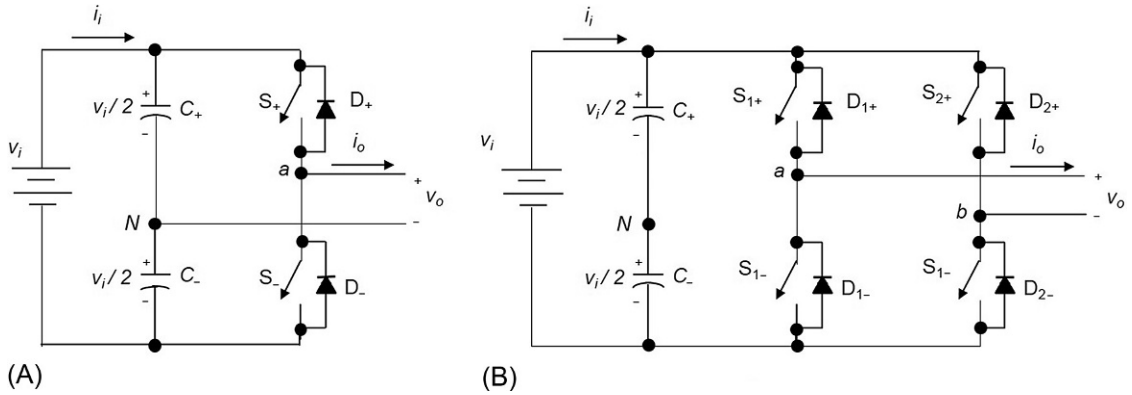


FIG. 11.2 Single-phase VSI: (A) half bridge and (B) full bridge.

TABLE 11.1 Switch states for a half-bridge single-phase VSI

State	State no.	v_o	Components conducting	
S_+ is on, and S_- is off	1	$v_i/2$	S_+	If $i_o > 0$
			D_+	If $i_o < 0$
S_- is on, and S_+ is off	2	$-v_i/2$	D_-	If $i_o > 0$
			S_-	If $i_o < 0$
S_+ and S_- are all off	3	$-v_i/2$	D_-	If $i_o > 0$
		$v_i/2$	D_+	If $i_o < 0$

For the half-bridge VSI (Fig. 11.2A), there are two defined (states 1 and 2) and one undefined (state 3) switching state as shown in Table 11.1. In order to avoid an undefined ac output voltage condition, state 3 should be used just for the dead time. Then, the modulating technique should always ensure that at any instant either the top or the bottom switch of the inverter leg is on.

Fig. 11.3 shows the ideal waveforms associated with the half-bridge inverter shown in Fig. 11.2A. The states for the switches S_+ and S_- are defined by the modulating technique, which in this case is a carrier-based PWM.

For the full-bridge VSI (Fig. 11.2B), there are four defined (states 1–4) and one undefined (state 5) switching state as shown in Table 11.2. Again, in order to avoid an undefined ac output voltage condition, state 5 should be used just for the dead time. Then, the modulating technique should always ensure that at any instant either the top or the bottom switch of an inverter leg is on.

Fig. 11.4 shows the ideal waveforms associated with the full-bridge inverter shown in Fig. 11.2B. The states for the switches are defined by the modulating technique, which in this case is a carrier-based PWM, but unipolar output is considered.

For the VSIs, different output filters may be employed, in order to provide the fundamental component of the output. Depending on the application, it would be desirable to provide a voltage or a current output. In Fig. 11.5, some output filters for this converter are shown; in all cases, an inductor is required immediately for the output of the converter. The first and the last one are used to provide a current output, such as in VSIs connected to the grid, where a current-like performance is required. The second-order filter is used for voltage output, such as stand-alone applications or ASDs.

11.2.2 Current Source Inverter

The topology for the single-phase CSIs is the shown in Fig. 11.6. The converter is composed of inductors, switches, and diodes. The inductors required are large, such that the inductors maintain a constant current i_i. Current-source topologies feature a low switching dv/dt and reliable overcurrent/short-circuit protection.

In order to operate properly the current-source inverter, the following rules are compulsory:

1. Top or bottom switches of the different legs cannot be off simultaneously, because no current path is provided to the input inductors.
2. Diode in series to each switch must be placed, because a short circuit across the output voltage v_o would be produced. If the commercial switch does not include anti-parallel diodes, then the circuit is already complete.
3. In practical implementation, an overlapping time must be considered in the control signals of the top or bottom switches of the different legs.

According to the previous rules, it should be noticed that both switches of the inverter leg can be turned on at the same time, and this is not possible in VSI.

For the CSI (Fig. 11.6), there are four defined (states 1–4) and one not permitted switching state (state 5) as shown in Table 11.3. The modulating technique should always ensure that at any instant, at least one of the top and bottom switch of the inverter legs is on; otherwise, the inverter will be damaged.

Fig. 11.7 shows the ideal waveforms associated with the CSI shown in Fig. 11.6. Notice that only the control signals of one inverter leg are graphed, since the other control signals are the

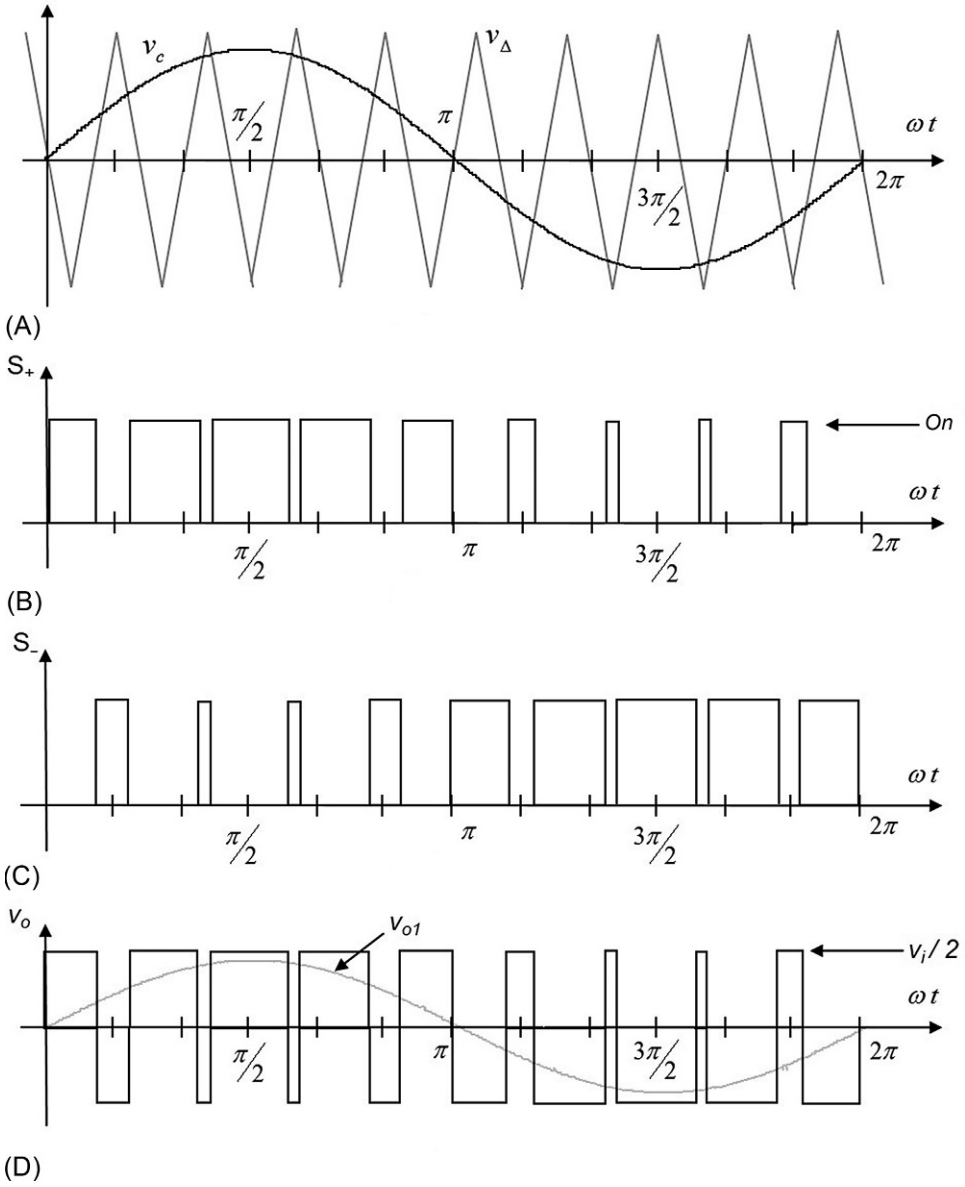


FIG. 11.3 The half-bridge VSI. Ideal waveforms for the SPWM: (A) carrier and modulating signals, (B) switch S_+ state, (C) switch S_- state, and (D) ac output voltage.

TABLE 11.2 Switch states for a full-bridge single-phase VSI

State	State no.	v_{aN}	v_{bN}	v_o	Components conducting	
S_{1+} and S_{2-} are on, and S_{1-} and S_{2+} are off	1	$v_i/2$	$-v_i/2$	v_i	S_{1+} and S_{2-}	If $i_o > 0$
					D_{1+} and D_{2-}	If $i_o < 0$
S_{1-} and S_{2+} are on, and S_{1+} and S_{2-} are off	2	$-v_i/2$	$v_i/2$	$-v_i$	D_{1-} and D_{2+}	If $i_o > 0$
					S_{1-} and S_{2+}	If $i_o < 0$
S_{1+} and S_{2+} are on, and S_{1-} and S_{2-} are off	3	$v_i/2$	$v_i/2$	0	S_{1+} and D_{2+}	If $i_o > 0$
					D_{1+} and S_{2+}	If $i_o < 0$
S_{1-} and S_{2-} are on, and S_{1+} and S_{2+} are off	4	$-v_i/2$	$-v_i/2$	0	D_{1-} and S_{2-}	If $i_o > 0$
					S_{1-} and D_{2-}	If $i_o < 0$
S_{1-} and S_{1+} are off	5	$-v_i/2$		Depends on S_{2-} and S_{2+}	D_{1-}	If $i_o > 0$
		$v_i/2$			D_{1+}	If $i_o < 0$
S_{2-} and S_{2+} are off			$v_i/2$	Depends on S_{1-} and S_{1+}	D_{2+}	If $i_o > 0$
			$-v_i/2$		D_{2-}	If $i_o < 0$

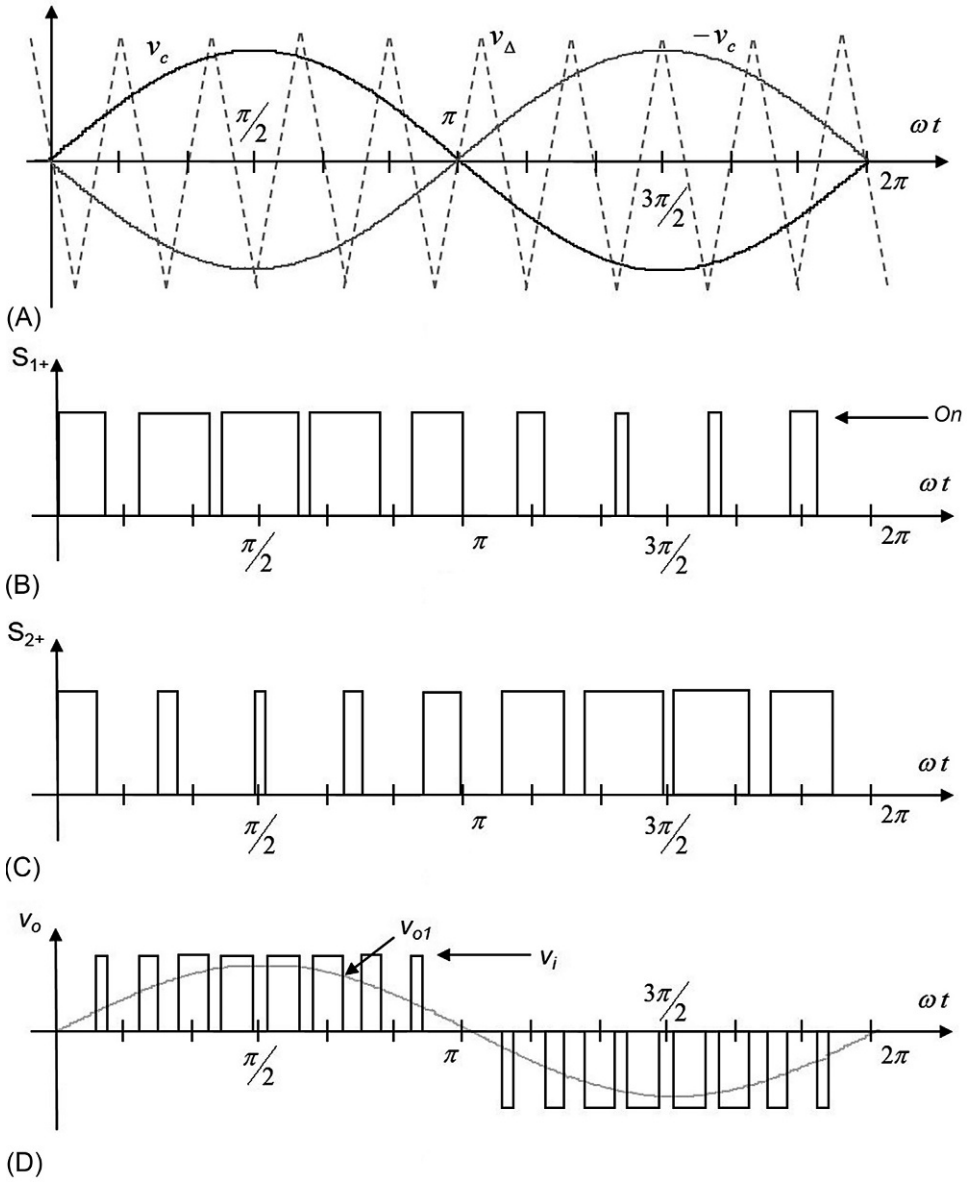


FIG. 11.4 The full-bridge VSI. Ideal waveforms for the unipolar SPWM: (A) carrier and modulating signals, (B) switch S_{1+} state, (C) switch S_{2+} state, and (D) ac output voltage.

opposite due to the rules (S_{1+} = not S_{2+} and S_{1-} = not S_{2-}), but the overlapping time should be considered for implementation. The states for the switches are defined by the modulating technique, which in this case is a carrier-based PWM, but unipolar output is considered.

For the CSIs, different output filters may be employed, in order to provide the fundamental component of the output waveform. Depending on the application, it would be desirable to provide a voltage or current output. In Fig. 11.8, some output filters for this converter are shown; in all cases, a capacitor is required immediately for the output of the converter.

11.2.3 Impedance Source Inverter

There are different topologies for single-phase ISIs, namely, "Z,"- "qZ,"- and "TZ"-source inverters; in Fig. 11.9, the Z-source inverter (ZSI) is shown. The converter is composed of capacitors and inductors, switches, and diodes. The capacitors and the inductors are arranged to form an input impedance for the inverter.

In order to operate properly the impedance-source inverter of Fig. 11.9, the following rules are compulsory:

1. No restrictions to the switches of the inverter leg apply.

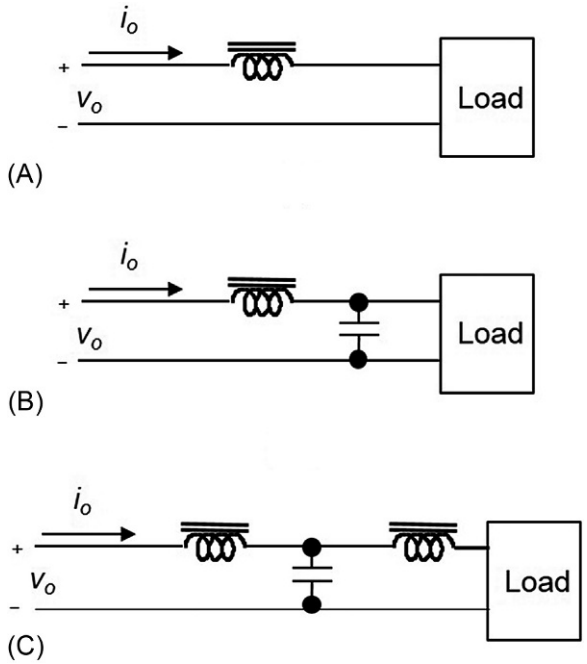


FIG. 11.5 Output filter for a VSI: (A) inductor, (B) second-order filter, and (C) LCL filter.

2. Diodes in antiparallel to each switch must be placed, in order to provide a current path for inductive loads. If the commercial switch includes these diodes, then the circuit is already complete.
3. In practical implementation, no dead or overlapping time must be considered in the control signals of the leg switches.

TABLE 11.3 Switch states for a single-phase CSI

State	State no.	i_o	Components conducting
S_{1+} and S_{2-} are on, and S_{1-} and S_{2+} are off	1	i_i	S_{1+}, S_{2-}, D_{1+}, and D_{2-}
S_{1-} and S_{2+} are on, and S_{1+} and S_{2-} are off	2	$-i_i$	S_{1-}, S_{2+}, D_{1-}, and D_{2+}
S_{1+} and S_{1-} are on, and S_{2+} and S_{2-} are off	3	0	S_{1+}, S_{1-}, D_{1+}, and D_{1-}
S_{2+} and S_{2-} are on, and S_{1+} and S_{1-} are off	4	0	S_{2+}, S_{2-}, D_{1-}, and D_{2-}
S_{1+} and S_{1-} are off, and S_{2+} and S_{2-} are off	5		This state must be avoided

According to the previous rules, it should be noticed that the switches of the inverter leg can be turned on and off at any time, and then, this converter has more switching states than the others, and this is used to boost the input voltage.

For the ISI shown in Fig. 11.9, there are five defined (states 1–5) and one undefined switching state as shown in Table 11.4. The modulating technique may permit to use the additional switching state (no. 5, known as shoot-through state), and then, another modulating signal should be employed for this purpose, but usually, it has a constant waveform.

Fig. 11.10 shows the ideal waveforms associated with the ZSI shown in Fig. 11.9. The states for the switches are defined by the modulating technique, which in this case is a carrier-based PWM, but unipolar output is considered; the shoot-through state is modulated by v_r.

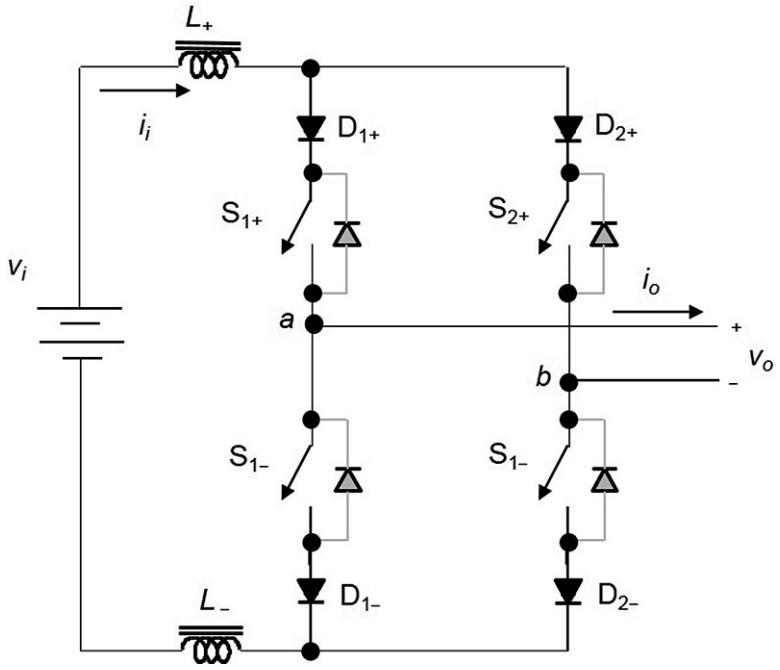


FIG. 11.6 Single-phase CSI.

For the converter ZSI, the output filter may be the same as for the VSI, and then, the filters are like the ones shown in Fig. 11.5.

11.2.4 Other Inverter Schemes

In the literature, other inverter topologies, with different operation from the previous discussed converters, have been proposed. However, the compulsory rules are valid, according to the input source. The entitled boost inverter is based on two bidirectional dc/dc boost converters and is able to produce an output voltage higher than the input voltage. This idea can be easily extrapolated to other dc/dc converter topologies. For more details, the appropriate references can be consulted.

11.2.5 Pulse Width Modulation

In order to produce a sinusoidal output, the pulse width modulation is employed. The modulating techniques mostly used are the carrier-based technique (e.g., sinusoidal pulse width modulation, SPWM), the space-vector (SV) technique, and the selective harmonic elimination (SHE) technique.

11.2.5.1 The Carrier-Based Pulse Width Modulation (PWM) Technique

As mentioned earlier, it is desired that the ac output voltage, v_o, follows a given waveform (e.g., sinusoidal) on a continuous basis by properly switching the semiconductors. The carrier-based PWM technique fulfills such a requirement as it defines

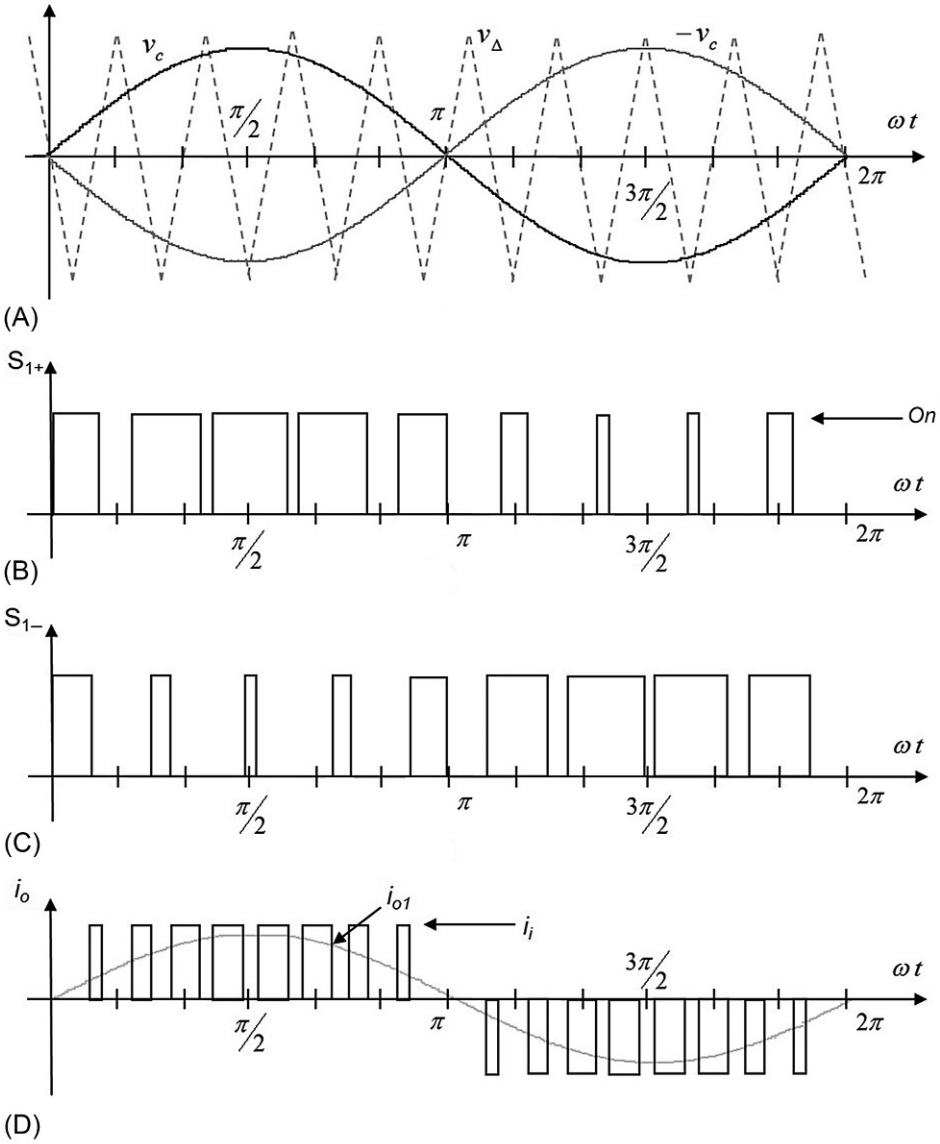


FIG. 11.7 The CSI, ideal waveforms for the unipolar SPWM: (A) carrier and modulating signals, (B) switch S_{1+} state, (C) switch S_{1-} state, and (D) ac output current.

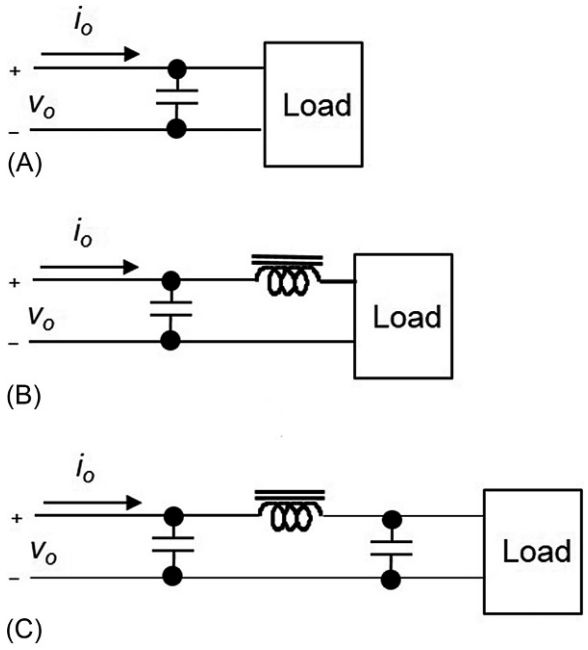


FIG. 11.8 Output filter for a CSI: (a) just capacitor, (b) second-order filter, and (c) CLC filter.

the on and off states of the switches of the inverter legs by comparing a modulating signal v_c (desired ac output voltage) and a triangular waveform v_Δ (carrier signal).

A special case is when the modulating signal v_c is a sinusoidal at frequency f_c and amplitude $\hat{v}_c$, and the triangular signal v_Δ is at frequency f_Δ and amplitude $\hat{v}_\Delta$. This is the sinusoidal PWM (SPWM) scheme. In this case, the modulation index m_a (also known as the amplitude modulation ratio) is defined as

$$m_a = \frac{\hat{v}_c}{\hat{v}_\Delta} \tag{11.1}$$

and the normalized carrier frequency m_f (also known as the frequency modulation ratio) is

$$m_f = \frac{f_\Delta}{f_c} \tag{11.2}$$

There are two known output waveforms entitled bipolar and unipolar output. Figs. 11.3D (bipolar) and 11.4d (unipolar) clearly show that the ac output voltage v_o is basically a sinusoidal waveform plus harmonics.

Bipolar PWM technique

To generate a bipolar output, a carrier-based technique can be used as shown in Fig. 11.3. In this technique, only one modulating signal v_c is used and also only one triangular signal v_Δ. The important features for the bipolar output are the following:

(a) The amplitude of the fundamental component of the ac output voltage $\hat{v}_{o1}$ satisfies the following expression:

$$\hat{v}_{o1} = \hat{v}_{aN1} = \frac{v_i}{2} m_a \tag{11.3}$$

for half-bridge VSI, Fig. 11.2A,

$$\hat{v}_{o1} = \hat{v}_{ab1} = v_i m_a \tag{11.4}$$

for the full-bridge VSI, Fig. 11.2B; these equations are valid for $m_a \leq 1$, which is called the linear region of the modulating technique (higher values of m_a lead to overmodulation that will be discussed later).

(b) For odd values of the normalized carrier frequency m_f, the harmonics in the ac output voltage appear at normalized frequencies f_h centered around m_f and its multiples, specifically,

$$h = l m_f \pm k \quad l = 1,2,3,\ldots \tag{11.5}$$

where $k = 2,4,6,\ldots$ for $l = 1,3,5,\ldots$ and $k = 1,3,5,\ldots$ for $l = 2,4,6,\ldots$.

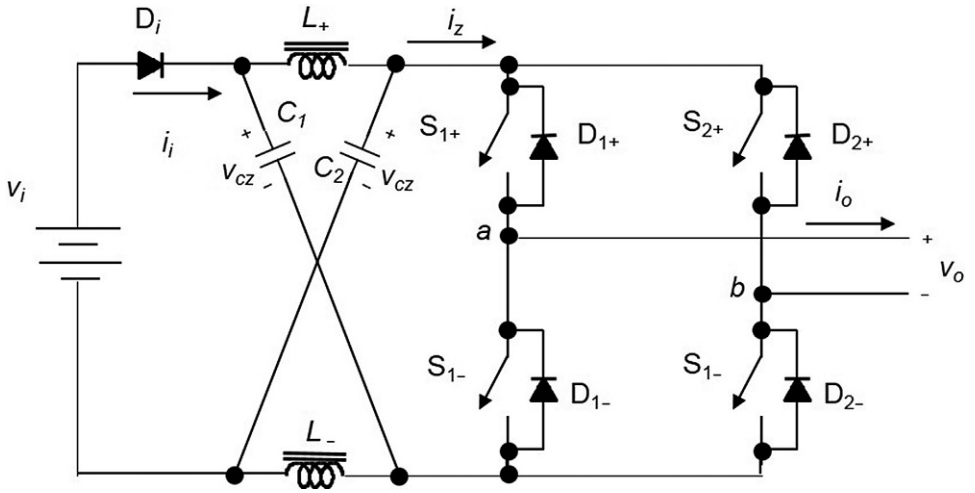


FIG. 11.9 Single-phase ZSI.

TABLE 11.4 Switch states for a single-phase ZSI

State	State no.	v_o
S_{1+} and S_{2-} are on, and S_{1-} and S_{2+} are off	1	$2v_{cz}-v_i$
S_{1-} and S_{2+} are on, and S_{1+} and S_{2-} are off	2	$-(2v_{cz}-v_i)$
S_{1+} and S_{2+} are on, and S_{1-} and S_{2-} are off	3	0
S_{1-} and S_{2-} are on, and S_{1+} and S_{2+} are off	4	0
S_{1+} and S_{2+} are on, and S_{1-} or S_{2-} is on S_{1-} and S_{2-} are on, and S_{1+} or S_{2+} is on	5	0
S_{1-} and S_{1+} are off	6	Depends on S_{2-} and S_{2+}
S_{2-} and S_{2+} are off		Depends on S_{1-} and S_{1+}

(c) The amplitude of the ac output voltage harmonics is a function of the modulation index m_a and is independent of the normalized carrier frequency m_f for $m_f > 9$.

(d) The harmonics in the dc link current (due to the modulation) appear at normalized frequencies f_p centered around the normalized carrier frequency m_f and its multiples, specifically,

$$p = lm_f \pm k \pm 1 \quad l = 1,2,\ldots \tag{11.6}$$

where $k = 2,4,6,\ldots$ for $l = 1,3,5,\ldots$ and $k = 1,3,5,\ldots$ for $l = 2,4,6,\ldots$.

Additional important issues are the following: (a) For small values of m_f ($m_f < 21$), the carrier signal v_Δ and the signal v_c should be synchronized to each other (m_f integer), which is required to hold the previous features; if this is not the case, subharmonics will be present in the ac output voltage; (b) for large values of m_f ($m_f > 21$), the subharmonics are negligible if an asynchronous PWM technique is used; however, due to potential very low-order subharmonics, its use should be avoided; finally, (c) in the overmodulation region ($m_a > 1$), some intersections between the carrier and the modulating signal are missed, which leads to the generation of low-order harmonics, but a higher fundamental ac output voltage is obtained; unfortunately, the linearity between m_a and $\hat{v}_{o1}$ achieved in the linear region does not hold in the overmodulation region; moreover, a saturation effect can be observed (Fig. 11.11).

As mentioned before, the PWM technique allows an ac output voltage to be generated that tracks a given modulating signal. In the SPWM technique, the modulating signal is a sinusoidal that provides, in the linear region, an ac output voltage that varies linearly as a function of the modulation index, and the harmonics are at well-defined frequencies and amplitudes. These features simplify the design of filtering components. Unfortunately, the maximum amplitude of the fundamental ac voltage is bounded in this operating mode. Higher voltages are obtained by using the overmodulation region ($m_a > 1$); however, low-order harmonics appear in the ac output voltage. Very large values of the modulation index ($m_a > 3.24$) lead to a totally square ac output voltage.

Unipolar PWM technique

To generate a unipolar output, also a carrier-based technique can be used as shown in Fig. 11.4, where two sinusoidal modulating signals (v_c and $-v_c$) are used. The signal v_c is used to generate S_{1+}, and $-v_c$ is used to generate S_{2+}. Notice that this output cannot be produced by a half-bridge inverter. Important features for the unipolar output are the following:

(a) The amplitude of the fundamental component of the ac output voltage $\hat{v}_{o1}$ satisfies the following expression:

$$\hat{v}_{o1} = 2 \cdot \hat{v}_{aN1} = m_a \cdot v_i \tag{11.7}$$

(b) Since the phase voltages (v_{aN} and v_{bN}) are identical but 180° out of phase, the output voltage ($v_o = v_{ab} = v_{aN} - v_{bN}$) will not contain even harmonics. Thus, if m_f is taken even, the harmonics in the ac output voltage appear at normalized odd frequencies f_h centered around twice the normalized carrier frequency m_f and its multiples. Specifically,

$$h = lm_f \pm k \quad l = 2,4,\ldots \tag{11.8}$$

where $k = 1,3,5,\ldots$; this feature is considered to be an advantage because it allows the use of smaller filtering components to obtain high-quality voltage and current waveforms while using the same switching frequency as in VSIs modulated by the bipolar approach.

(c) The amplitude of the ac output voltage harmonics is also a function of the modulation index m_a.

(d) The harmonics in the dc link current appear at normalized frequencies f_p centered around twice the normalized carrier frequency m_f and its multiples. Specifically,

$$p = lm_f \pm k \pm 1 \quad l = 2,4,\ldots \tag{11.9}$$

where $k = 1,3,5,\ldots$

11.2.5.2 Selective Harmonic Elimination

The main objective is to obtain a sinusoidal ac output voltage waveform where the fundamental component can be adjusted arbitrarily within a range and the intrinsic harmonics selectively eliminated. This is achieved by mathematically generating the exact instant of the turn-on and turnoff of the power semiconductors. The ac output voltage features odd half- and quarter-wave symmetry; therefore, even harmonics are not present ($v_{oh} = 0$, $h = 2,4,6,\ldots$). Moreover, the phase voltage waveform (v_o) should be chopped N times per half cycle in order to adjust the fundamental and eliminate $N-1$ harmonics in the ac output voltage waveform.

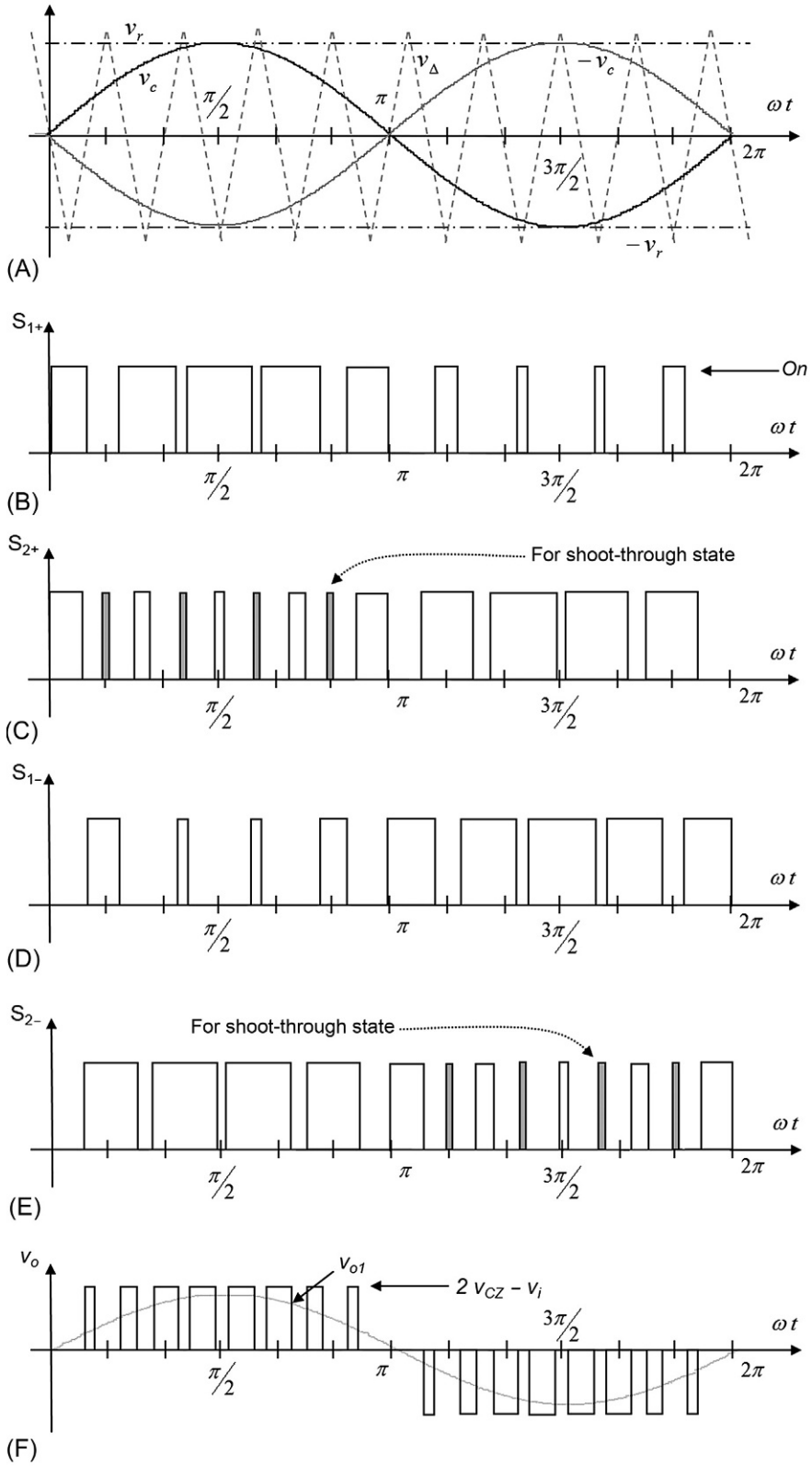


FIG. 11.10 The ZSI, ideal waveforms for the unipolar SPWM: (A) carrier and modulating signals, (B) switch S_{1+} state, (C) switch S_{2+} state, (D) switch S_{1-} state, (E) switch S_{2-} state, and (F) ac output voltage.

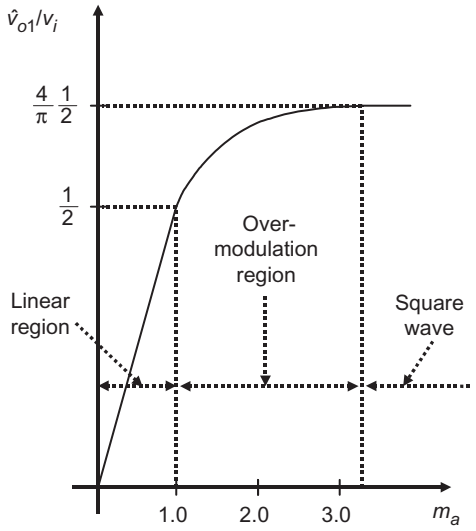


FIG. 11.11 Normalized fundamental ac component of the output voltage in a half-bridge VSI SPWM modulated.

For this modulation, also the output may be bipolar or unipolar.

Bipolar SHE technique

The general expressions to eliminate an even $N-1$ $(N-1=2,4,6,\ldots)$ number of harmonics are

$$\begin{aligned} -\sum_{k=1}^{N}(-1)^k\cos(\alpha_k) &= \frac{(2+\pi\hat{v}_{o1})/v_i}{4} \\ -\sum_{k=1}^{N}(-1)^k\cos(n\alpha_k) &= \frac{1}{2} \quad \text{for } n=3,5,\ldots,2N-1 \end{aligned} \tag{11.10}$$

where $\alpha_1, \alpha_2, \ldots, \alpha_N$ should satisfy $\alpha_1<\alpha_2<\cdots<\alpha_N<\pi/2$.

For instance, to eliminate the third and fifth harmonics and to perform fundamental magnitude control $(N=3)$, the equations to be solved are the following:

$$\begin{aligned} \cos(1\alpha_1)-\cos(1\alpha_2)+\cos(1\alpha_3) &= (2+\pi\hat{v}_{o1}/v_i)/4 \\ \cos(3\alpha_1)-\cos(3\alpha_2)+\cos(3\alpha_3) &= 1/2 \\ \cos(5\alpha_1)-\cos(5\alpha_2)+\cos(5\alpha_3) &= 1/2 \end{aligned} \tag{11.11}$$

where the angles α_1, α_2, and α_3 are defined as shown in Fig. 11.12A and the spectrum in Fig. 11.12B. The angles are found by means of iterative algorithms as no analytic solutions can be derived. The angles α_1, α_2, and α_3 are plotted for different values of $\hat{v}_{o1}/v_i$ in Fig. 11.13A.

Similarly, the general expressions to eliminate an odd $N-1$ $(N-1=3,5,7,\ldots)$ number of harmonics are given by

$$\begin{aligned} -\sum_{k=1}^{N}(-1)^k\cos(n\alpha_k) &= \frac{(2-\pi\hat{v}_{o1})/v_i}{4} \\ -\sum_{k=1}^{N}(-1)^k\cos(n\alpha_k) &= \frac{1}{2} \quad \text{for } n=3,5,\ldots,2N-1 \end{aligned} \tag{11.12}$$

where $\alpha_1, \alpha_2, \ldots, \alpha_N$ should satisfy $\alpha_1<\alpha_2<\cdots<\alpha_N<\pi/2$.

For instance, to eliminate the third, fifth, and seventh harmonics and to perform the fundamental magnitude control $(N-1=3)$, the equations to be solved are

$$\begin{aligned} &\cos(1\alpha_1)-\cos(1\alpha_2)+\cos(1\alpha_3)-\cos(1\alpha_4)=(2-\pi\hat{v}_{o1}/v_i)/4 \\ &\cos(3\alpha_1)-\cos(3\alpha_2)+\cos(3\alpha_3)-\cos(3\alpha_4)=1/2 \\ &\cos(5\alpha_1)-\cos(5\alpha_2)+\cos(5\alpha_3)-\cos(5\alpha_4)=1/2 \\ &\cos(7\alpha_1)-\cos(7\alpha_2)+\cos(7\alpha_3)-\cos(7\alpha_4)=1/2 \end{aligned} \tag{11.13}$$

where the angles α_1, α_2, α_3, and α_4 are defined as shown in Fig. 11.12C, and the spectrum in Fig. 11.12D. The angles α_1, α_2, and α_3 are plotted for different values of $\hat{v}_{o1}/v_i$ in Fig. 11.13B.

Unipolar SHE technique

The general expressions to eliminate an arbitrary $N-1$ $(N-1=3,5,7,\ldots)$ number of harmonics are given by

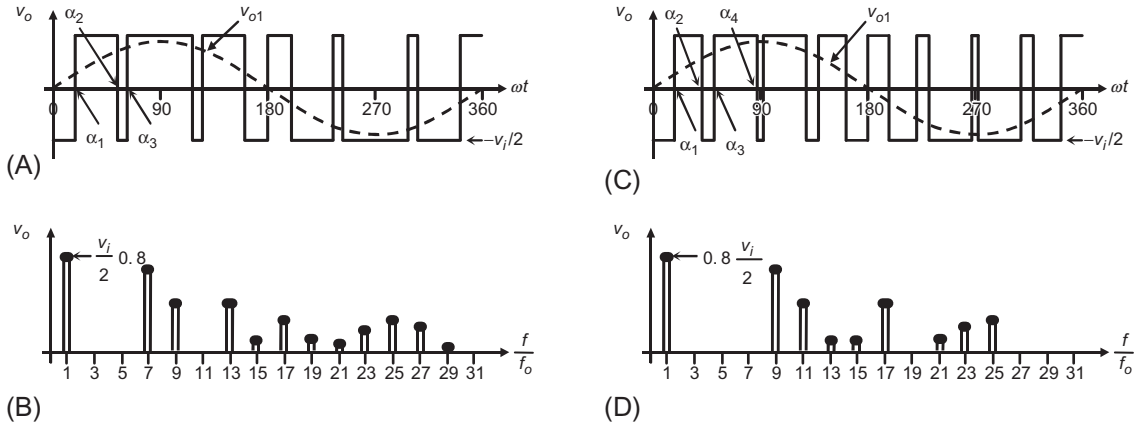


FIG. 11.12 The half-bridge VSI. Ideal waveforms for the SHE technique: (A) ac output voltage for third- and fifth-harmonic elimination, (B) spectrum of (A), (C) ac output voltage for third-, fifth-, and seventh-harmonic elimination, and (D) spectrum of (C).

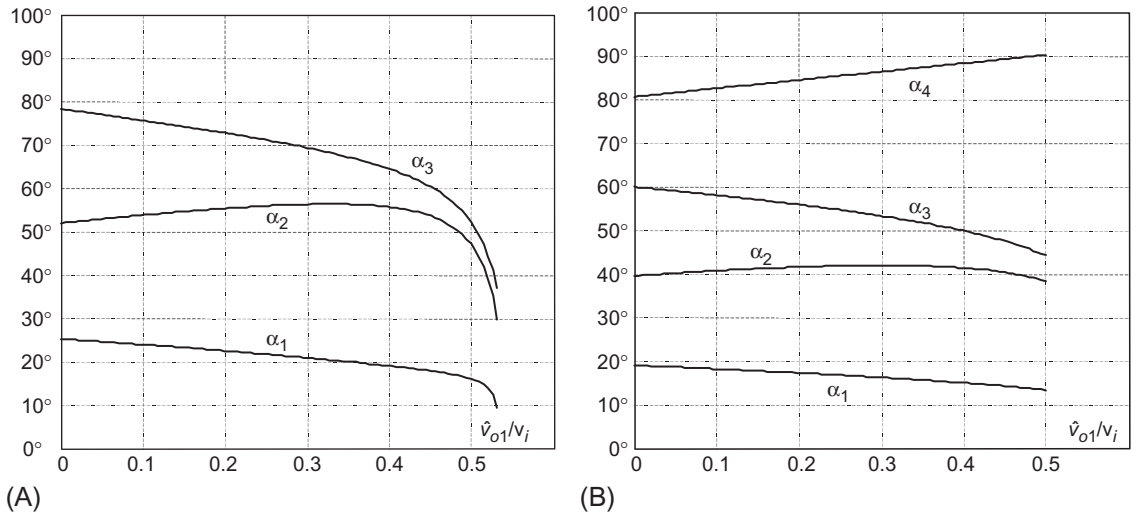


FIG. 11.13 Chopping angles for SHE and fundamental voltage control in half-bridge VSIs: (A) third- and fifth-harmonic elimination and (B) third-, fifth-, and seventh-harmonic elimination.

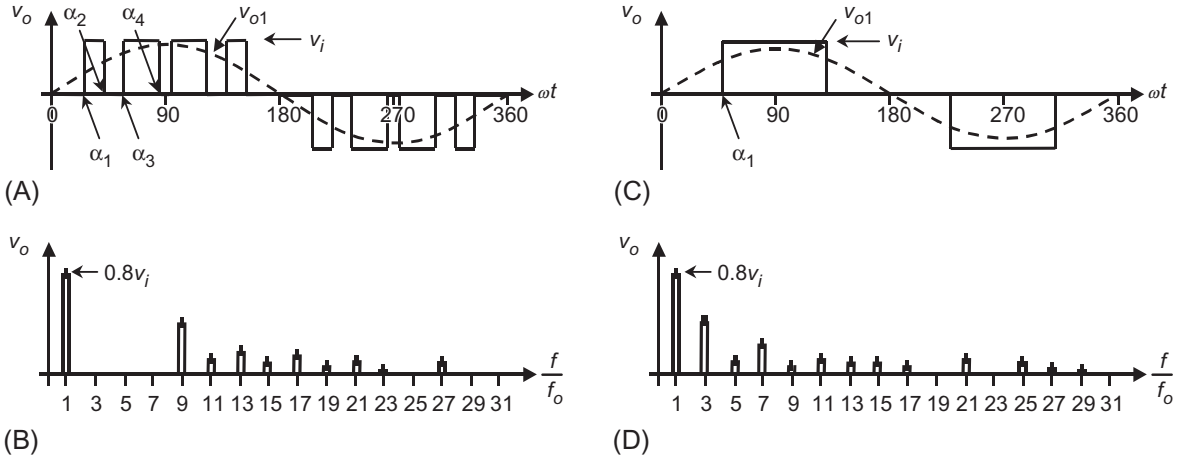


FIG. 11.14 The half-bridge VSI. Ideal waveforms for the SHE technique: (A) ac output voltage for third-, fifth-, and seventh-harmonic elimination; (B) spectrum of (A); (C) ac output voltage for fundamental control; and (D) spectrum of (C).

$$\begin{aligned} -\sum_{k=1}^{N}(-1)^k\cos(n\alpha_k) &= \frac{\pi}{4}\left(\frac{\hat{v}_{o1}}{v_i}\right) \\ -\sum_{k=1}^{N}(-1)^k\cos(n\alpha_k) &= 0 \quad \text{for } n=3,5,\ldots,2N-1 \end{aligned} \tag{11.14}$$

where $\alpha_1,\alpha_2,\ldots,\alpha_N$ should satisfy $\alpha_1<\alpha_2<\cdots<\alpha_N<\pi/2$.

For instance, to eliminate the third, the fifth, and the seventh harmonics and to perform fundamental component magnitude control ($N=4$), the equations to be solved are

$$\begin{aligned} &\cos(1\alpha_1)-\cos(1\alpha_2)+\cos(1\alpha_3)-\cos(1\alpha_4) = \pi\hat{v}_{o1}/(v_i4) \\ &\cos(3\alpha_1)-\cos(3\alpha_2)+\cos(3\alpha_3)-\cos(3\alpha_4) = 0 \\ &\cos(5\alpha_1)-\cos(5\alpha_2)+\cos(5\alpha_3)-\cos(5\alpha_4) = 0 \\ &\cos(7\alpha_1)-\cos(7\alpha_2)+\cos(7\alpha_3)-\cos(7\alpha_4) = 0 \end{aligned} \tag{11.15}$$

where the angles α_1, α_2, α_3, and α_4 are defined as shown in Fig. 11.14A and the spectrum in Fig. 11.14B. The angles α_1, α_2, α_3, and α_4 are plotted for different values of $\hat{v}_{o1}/v_i$ in Fig. 11.15A.

Fig. 11.14C shows a special case where only the fundamental ac output voltage is controlled. This is known as output control by voltage cancellation, which derives from the fact that its implementation is easily attainable by using two phase-shifted square-wave switching signals as shown in Fig. 11.16. The phase-shift angle becomes two · α_1 (Fig. 11.16B). Thus, the amplitude of the fundamental component and harmonics in the ac output voltage are given by

$$\hat{v}_{oh} = \frac{4}{\pi}v_i\frac{(-1)^{(h-1)/2}}{h}\cos(h\alpha_1) \quad h=1,3,5,\ldots \tag{11.16}$$

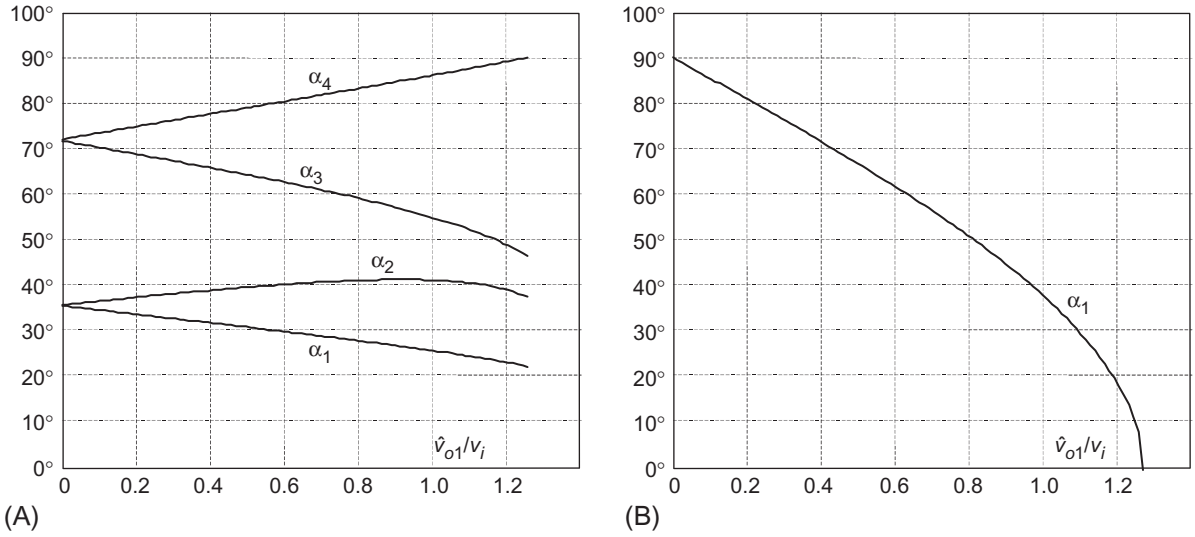


FIG. 11.15 Chopping angles for SHE and fundamental voltage control in half-bridge VSIs: (A) fundamental control and third-, fifth-, and seventh-harmonic elimination and (B) fundamental control.

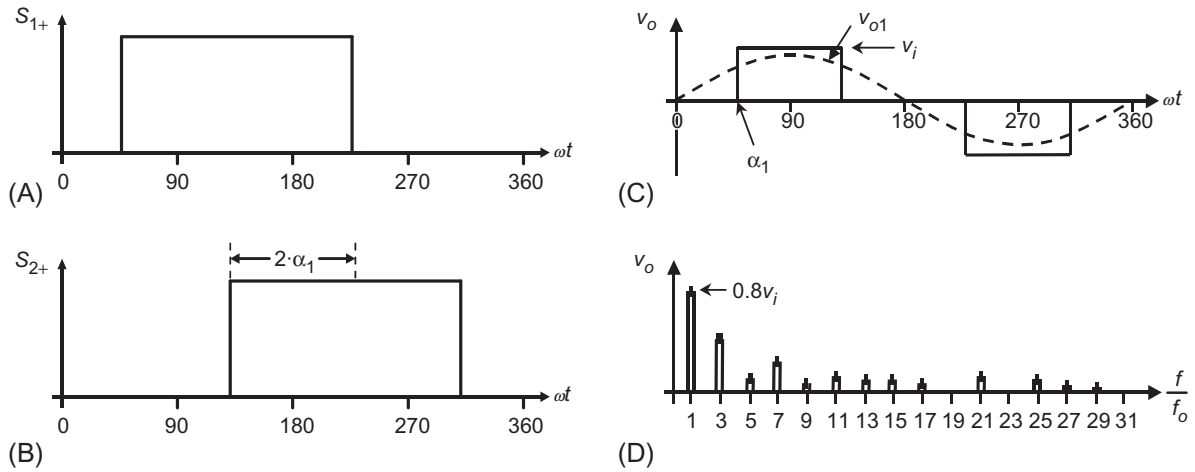


FIG. 11.16 The full-bridge VSI. Ideal waveforms for the output control by voltage cancellation: (A) switch S_{1+} state, (B) switch S_{2+} state, (C) ac output voltage, and (D) ac output voltage spectrum.

It can also be observed in Fig. 11.16C that for $\alpha_1 = 0$ square-wave operation is achieved. In this case, the fundamental ac output voltage is given by

$$\hat{v}_{o1} = \frac{4}{\pi} v_i \tag{11.17}$$

where the fundamental load voltage can be controlled by the manipulation of the dc link voltage v_i. Additional means to modify this voltage should be provided. Depending on the dc link source of power, this could be a controlled rectifier, for ac sources, or a dc/dc converter, for dc sources.

To implement the SHE modulating technique, the modulator should generate the gating pattern according to the angles as shown in Figs. 11.13 and 11.15. This task is usually performed by digital systems that normally store the angles in look-up tables.

11.2.5.3 DC Link Current

Due to the fact that the inverter is assumed lossless and constructed without storage energy components, the instantaneous power balance indicates that

$$v_i(t) \cdot i_i(t) = v_o(t) \cdot i_o(t) \tag{11.18}$$

For inductive load and relatively high switching frequencies, the load current *Io* is nearly sinusoidal. As a first approximation, the ac output voltage can also be considered sinusoidal. On the other hand, if the dc link voltage remains constant $v_i(t) = V_i$, Eq. (11.18) can be simplified to

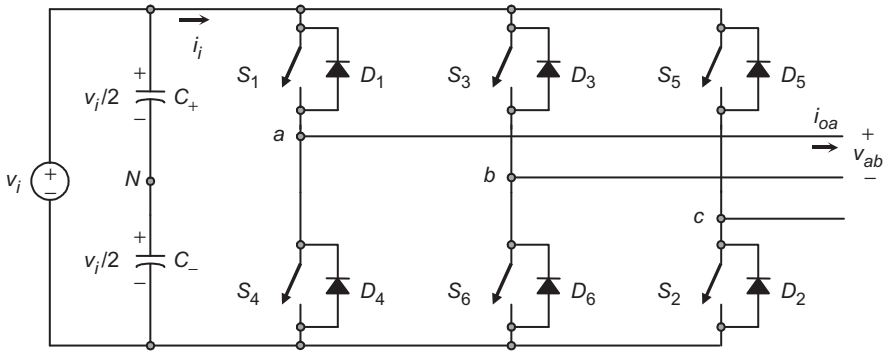


FIG. 11.17 Three-phase VSI topology.

$$i_i(t) = 1/\ V_i\sqrt{2}\ V_{o1}\sin(\omega t)\cdot\sqrt{2}\ I_o\sin(\omega t-\varphi) \qquad (11.19)$$

where V_{o1} is the fundamental rms ac output voltage, Io is the rms load current, and φ is an arbitrary inductive load power factor. Thus, the dc link current can be further simplified to

$$i_i(t) = V_{o1}/V_iI_o\cos(\varphi) - V_{o1}/Vi\ I_o\cos(2\omega t-\varphi) \qquad (11.20)$$

The preceding expression reveals an important issue, that is, the presence of a large second-order harmonic in the dc link current (its amplitude is similar to the dc link current). This second harmonic is injected back into the dc voltage source; thus, its design should be considered in order to guarantee a nearly constant dc link voltage. In practical terms, the dc voltage source is required to feature large amounts of capacitance, which is costly and demands space, both undesired features, especially in medium- to high-power supplies.

TABLE 11.5 Valid switch states for a three-phase VSI

State	State no.	v_{ab}	v_{bc}	v_{ca}	Space vector
S_1, S_2, and S_6 are on, and S_4, S_5, and S_3 are off	1	v_i	0	$-v_i$	$\vec{\mathbf{v}}_1 = 1 + j0.577$
S_2, S_3, and S_1 are on, and S_5, S_6, and S_4 are off	2	0	v_i	$-v_i$	$\vec{\mathbf{v}}_2 = j1.155$
S_3, S_4, and S_2 are on, and S_6, S_1, and S_5 are off	3	$-v_i$	v_i	0	$\vec{\mathbf{v}}_3 = -1 + j0.577$
S_4, S_5, and S_3 are on, and S_1, S_2, and S_6 are off	4	$-v_i$	0	v_i	$\vec{\mathbf{v}}_4 = -1 - j0.577$
S_5, S_6, and S_4 are on, and S_2, S_3, and S_1 are off	5	0	$-v_i$	v_i	$\vec{\mathbf{v}}_5 = -j1.155$
S_6, S_1, and S_5 are on, and S_3, S_4, and S_2 are off	6	v_i	$-v_i$	0	$\vec{\mathbf{v}}_6 = 1 - j0.577$
S_1, S_3, and S_5 are on, and S_4, S_6, and S_2 are off	7	0	0	0	$\vec{\mathbf{v}}_7 = 0$
S_4, S_6, and S_2 are on, and S_1, S_3, and S_5 are off	8	0	0	0	$\vec{\mathbf{v}}_8 = 0$

11.3 Three-Phase Voltage Source Inverters

Single-phase VSIs cover low-range power applications, and three-phase VSIs cover medium- to high-power applications. The main purpose of these topologies is to provide a three-phase voltage source, where the amplitude, phase, and frequency of the voltages should always be controllable. Although most of the applications require sinusoidal voltage waveforms (e.g., ASDs, UPSs, FACTS, and var compensators), arbitrary voltages are also required in some other applications (e.g., active power filters and voltage compensators).

The standard three-phase VSI topology is shown in Fig. 11.17, and the eight valid switch states are given in Table 11.5. As in single-phase VSIs, the compulsory rules previously described in Section 11.2.1 also apply.

Of the eight valid states, two of them (7 and 8 in Table 11.5) produce zero ac line voltages. The remaining states (1–6 in Table 11.5) produce nonzero ac output voltages. In order to generate a given voltage waveform, the inverter moves from one state to another. Thus, the resulting ac output line voltages consist of discrete values of voltages that are v_i, 0, and $-v_i$ for the topology shown in Fig. 11.17. The selection of the states in order to generate the given waveform is done by the modulating technique that should ensure the use of only the valid states.

11.3.1 Sinusoidal PWM

This is an extension of the one introduced for single-phase VSIs. In this case and in order to produce 120° out-of-phase load voltages, three modulating signals that are 120° out of phase are used. Fig. 11.18 shows the ideal waveforms of three-phase VSI SPWM. In order to use a single-carrier signal and preserve the features of the PWM technique, the normalized carrier frequency m_f should be an odd multiple of 3. Thus, all phase voltages (v_{aN}, v_{bN}, and v_{cN}) are identical, but 120° out of phase without even harmonics; moreover, harmonics at frequencies, a multiple of 3, are identical in amplitude and phase in all phases. For instance, if the ninth harmonic in phase aN is

$$v_{aN9}(t) = \hat{v}_9\sin(9\omega t) \qquad (11.21)$$

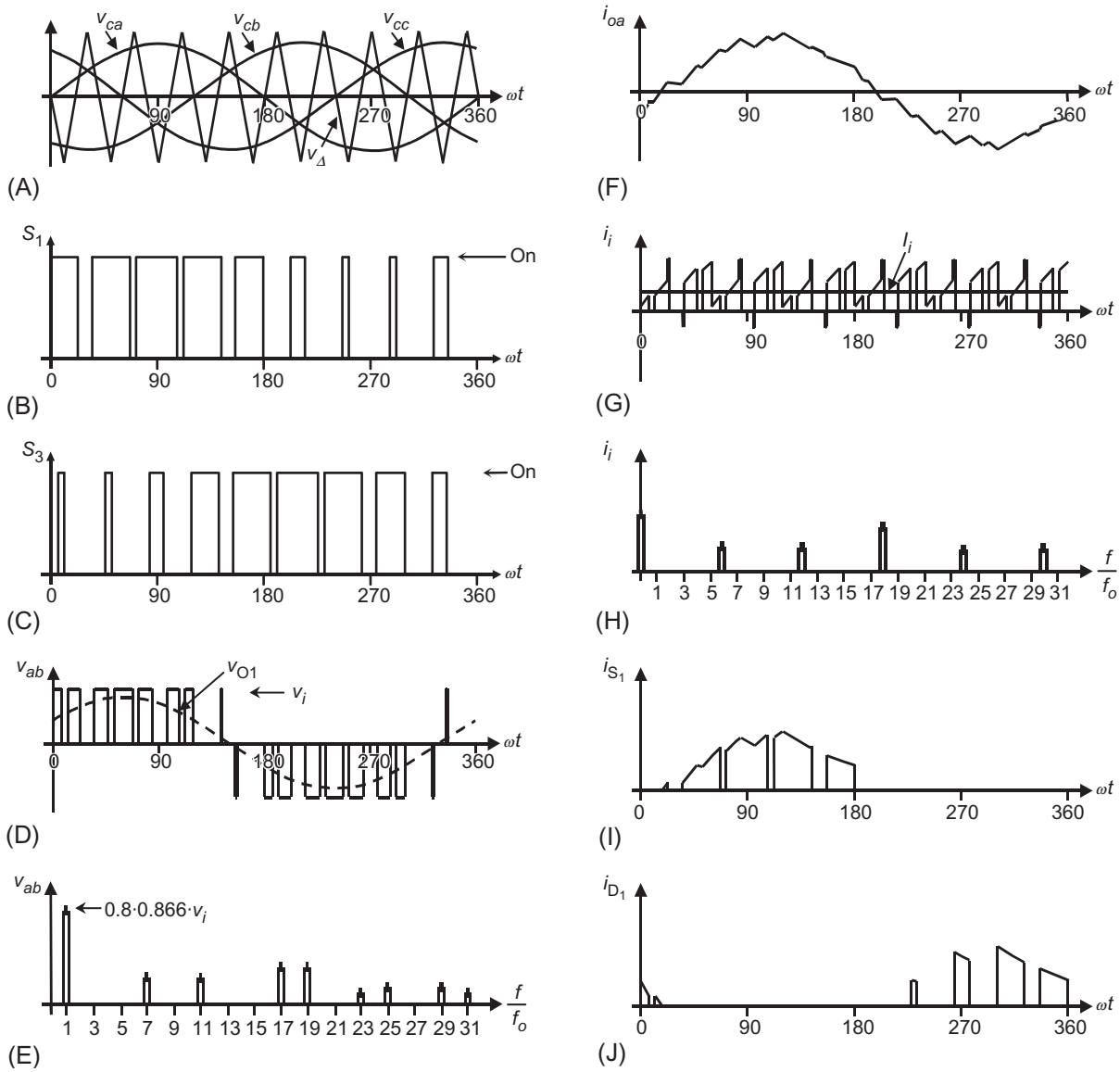


FIG. 11.18 The three-phase VSI. Ideal waveforms for the SPWM ($m_a = 0.8$, $m_f = 9$): (A) carrier and modulating signals, (B) switch S_1 state, (C) switch S_3 state, (D) ac output voltage, (E) ac output voltage spectrum, (F) ac output current, (G) dc current, (H) dc current spectrum, (I) switch S_1 current, and (J) diode D_1 current.

the ninth harmonic in phase bN will be

$$\begin{aligned} v_{bN9}(t) &= \hat{v}_9 \sin[9(\omega t - 120°)] \\ &= \hat{v}_9 \sin(9\omega t - 1080°) = \hat{v}_9 \sin(9\omega t) \end{aligned} \tag{11.22}$$

Thus, the ac output line voltage $v_{ab} = v_{aN} - v_{bN}$ will not contain the ninth harmonic. Therefore, for odd multiple of 3 values of the normalized carrier frequency m_f, the harmonics in the ac output voltage appear at normalized frequencies f_h centered around m_f and its multiples, specifically, at

$$h = lm_f \pm k \quad l = 1,2,\ldots \tag{11.23}$$

where $l = 1,3,5,\ldots$ for $k = 2,4,6,\ldots$ and $l = 2,4,\ldots$ for $k = 1,5,7,\ldots$ such that h is not a multiple of 3. Therefore, the harmonics will be at $m_f \pm 2$, $m_f \pm 4,\ldots$, $2m_f \pm 1$, $2m_f \pm 5,\ldots, 3m_f \pm 2$, $3m_f \pm 4,\ldots, 4m_f \pm 1$, $4m_f \pm 5,\ldots$. For nearly sinusoidal ac load current, the harmonics in the dc link current are at frequencies given by

$$h = lm_f \pm k \pm 1 \quad l = 1,2,\ldots \tag{11.24}$$

where $l = 0,2,4,\ldots$ for $k = 1,5,7,\ldots$ and $l = 1,3,5,\ldots$ for $k = 2,4,6,\ldots$ such that $h = l \cdot m_f \pm k$ is positive and not a multiple of 3.

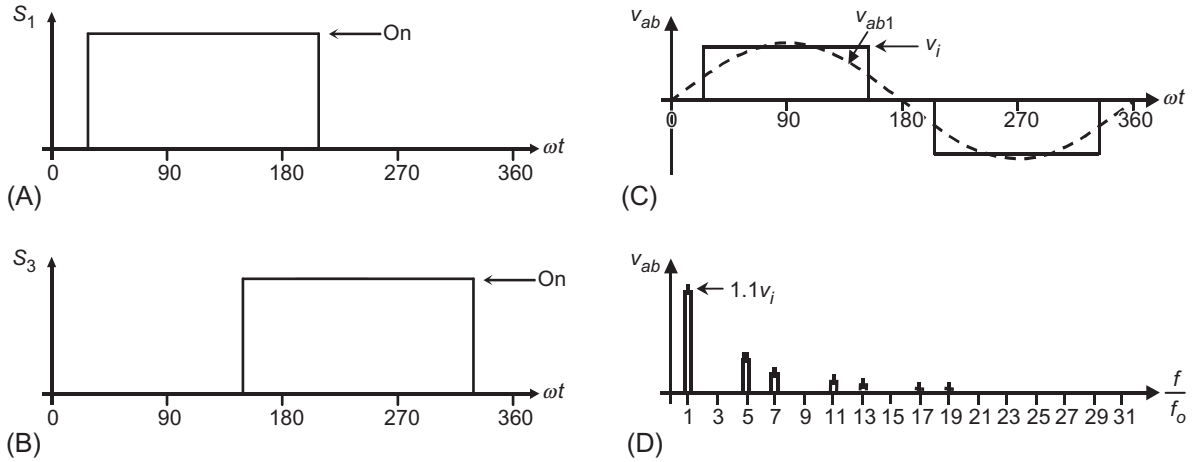


FIG. 11.19 The three-phase VSI. Square-wave operation: (A) switch S_1 state, (B) switch S_3 state, (C) ac output voltage, and (D) ac output voltage spectrum.

The identical conclusions can be drawn for the operation at small and large values of m_f as for the single-phase configurations. However, because the maximum amplitude of the fundamental phase voltage in the linear region ($m_a \leq 1$) is $v_i/2$, the maximum amplitude of the fundamental ac output line voltage is $\sqrt{3}v_i/2$. Therefore, one can write

$$\hat{v}_{ab1} = m_a \sqrt{3}\frac{v_i}{2} \quad 0 < m_a \leq 1 \tag{11.25}$$

To further increase the amplitude of the load voltage, the amplitude of the modulating signal $\hat{v}_c$ can be made higher than the amplitude of the carrier signal $\hat{v}_\Delta$, which leads to overmodulation. The relationship between the amplitude of the fundamental ac output line voltage and the dc link voltage becomes nonlinear as in single-phase VSIs. Thus, in the overmodulation region, the line voltages range is

$$\sqrt{3}\frac{v_i}{2} < \hat{v}_{ab1} = \hat{v}_{bc1} = \hat{v}_{ca1} < \frac{4}{\pi}\sqrt{3}\frac{v_i}{2} \tag{11.26}$$

11.3.2 Square-Wave Operation of Three-phase VSIs

Large values of m_a in the SPWM technique lead to full overmodulation. This is known as square-wave operation as illustrated in Fig. 11.19, where the power semiconductors are on for 180°. In this operation mode, the VSI cannot control the load voltage except by means of the dc link voltage v_i. This is based on the fundamental ac line-voltage expression

$$\hat{v}_{ab1} = \frac{4}{\pi}\sqrt{3}\frac{v_i}{2} \tag{11.27}$$

The ac line output voltage contains the harmonics f_h, where $h = 6 \cdot k \pm 1$ ($k = 1,2,3,\ldots$), and they feature amplitudes that are inversely proportional to their harmonic order (Fig. 11.18D). Their amplitudes are

$$\hat{v}_{abh} = \frac{1}{h}\frac{4}{\pi}\sqrt{3}\frac{v_i}{2} \tag{11.28}$$

11.3.3 Sinusoidal PWM with Zero Sequence Signal Injection

The restriction for m_a ($m_a \leq 1$) can be relaxed if a zero-sequence signal is added to the modulating signals before they are compared with the carrier signal. Fig. 11.20 shows the block diagram of the technique. Clearly, the addition of the zero sequence reduces the peak amplitude of the resulting modulating signals (u_{ca}, u_{cb}, u_{cc}), while the fundamental components remain unchanged. This approach expands the range of the linear region as it allows the use of modulation indexes m_a up to $2/\sqrt{3}$ without getting into the overmodulating region.

The maximum amplitude of the fundamental phase voltage in the linear region $\left(m_a \leq 2/\sqrt{3}\right)$ is $v_i/2$; thus, the maximum amplitude of the fundamental ac output line voltage is v_i. Therefore, one can write

$$\hat{v}_{ab1} = m_a \sqrt{3}\frac{v_i}{2} \quad \left(0 < m_a \leq 2/\sqrt{3}\right) \tag{11.29}$$

Fig. 11.21 shows the ideal waveforms of a three-phase VSI SPWM with zero injection for $m_a = 0.8$.

11.3.4 Selective Harmonic Elimination in Three-phase VSIs

As in single-phase VSIs, the SHE technique can be applied to three-phase VSIs. In this case, the power semiconductors of each leg of the inverter are switched so as to eliminate a given

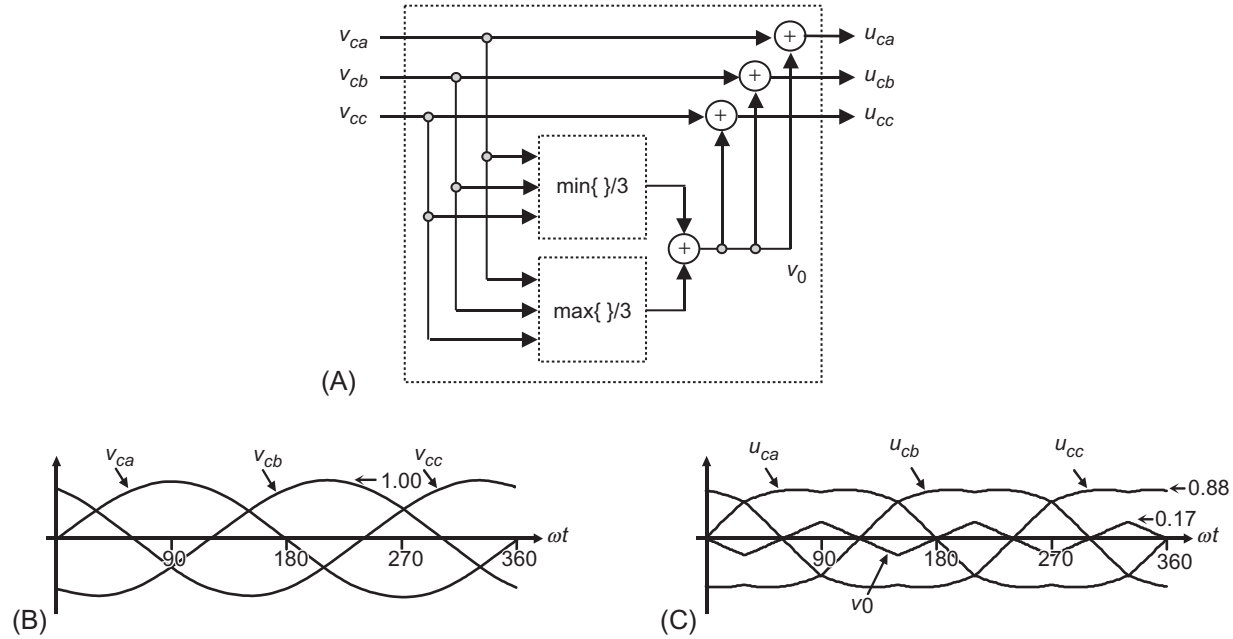


FIG. 11.20 Zero-sequence signal generator ($m_a = 1.0$, $m_f = 9$): (A) block diagram, (B) modulating signals, and (C) zero sequence and modulating signals with zero-sequence injection.

number of harmonics and to control the fundamental phase voltage amplitude. Considering that in many applications the required line output voltages should be balanced and 120° out of phase, the harmonic multiples of 3 ($h = 3,9,15,\ldots$), which could be present in the phase voltages (v_{aN}, v_{bN}, and v_{cN}), will not be present in the load voltages (v_{ab}, v_{bc}, and v_{ca}). Therefore, these harmonics are not required to be eliminated; thus, the chopping angles are used to eliminate only the harmonics at frequencies $h = 5,7,11,13,\ldots$ as required.

The expressions to eliminate a given number of harmonics are the same as those used in single-phase inverters. For instance, to eliminate the fifth and seventh harmonics and perform fundamental magnitude control ($N = 3$), the equations to be solved are

$$\begin{aligned} &\cos(1\alpha_1) - \cos(1\alpha_2) + \cos(1\alpha_3) = (2 + \pi\hat{v}_{aN1}/v_i)/4 \\ &\cos(5\alpha_1) - \cos(5\alpha_2) + \cos(5\alpha_3) = 1/2 \\ &\cos(7\alpha_1) - \cos(7\alpha_2) + \cos(7\alpha_3) = 1/2 \end{aligned} \tag{11.30}$$

where the angles α_1, α_2, and α_3 are defined as shown in Fig. 11.22A and plotted in Fig. 11.23. Fig. 11.22B shows that the third, ninth, fifteenth, … harmonics are all present in the phase voltages; however, they are not in the line voltages (Fig. 11.22D). If necessary, higher-order harmonics not eliminated with this technique can be filtered using small filters.

11.3.5 Space-Vector (SV)-Based Modulating Techniques

At present, the control strategies are implemented in digital systems, and therefore, digital modulating techniques are also available. The SV-based modulating technique is a digital technique in which the objective is to generate PWM load line voltages that are on average equal to given load line voltages. This is done in each sampling period by properly selecting the switch states from the valid ones of the VSI (Table 11.5) and by proper calculation of the period of times they are used. The selection and calculation times are based upon the SV transformation.

11.3.5.1 Space-Vector Transformation

Any three-phase set of variables that add up to zero in the stationary *abc* frame can be represented in a complex plane by a complex vector that contains a real (α) and an imaginary (β) component. For instance, the vector of three-phase line-modulating signals $\mathbf{v}_c^{abc} = [v_{ca} v_{cb} v_{cc}]^T$ can be represented by the complex vector $\vec{\mathbf{v}}_c = \mathbf{v}_c^{\alpha\beta} = [v_{c\alpha} v_{c\beta}]^T$ by means of the following transformation:

$$v_{c\alpha} = \frac{2}{3}[v_{ca} - 0.5(v_{cb} + v_{cc})] \tag{11.31}$$

$$v_{c\beta} = \frac{\sqrt{3}}{3}(v_{cb} - v_{cc}) \tag{11.32}$$

If the line-modulating signals $\mathbf{v}_c^{abc}$ are three balanced sinusoidal waveforms that feature an amplitude $\hat{v}_c$ and an angular frequency ω, the resulting modulating signals in the $\alpha\beta$ stationary frame become a vector $\vec{\mathbf{v}}_c = \mathbf{v}_c^{\alpha\beta}$ of fixed module $\hat{v}_c$, which rotates at frequency ω (Fig. 11.24). Similarly, the SV transformation is applied to the line voltages of the eight states of the VSI normalized with respect to v_i (Table 11.5), which generates

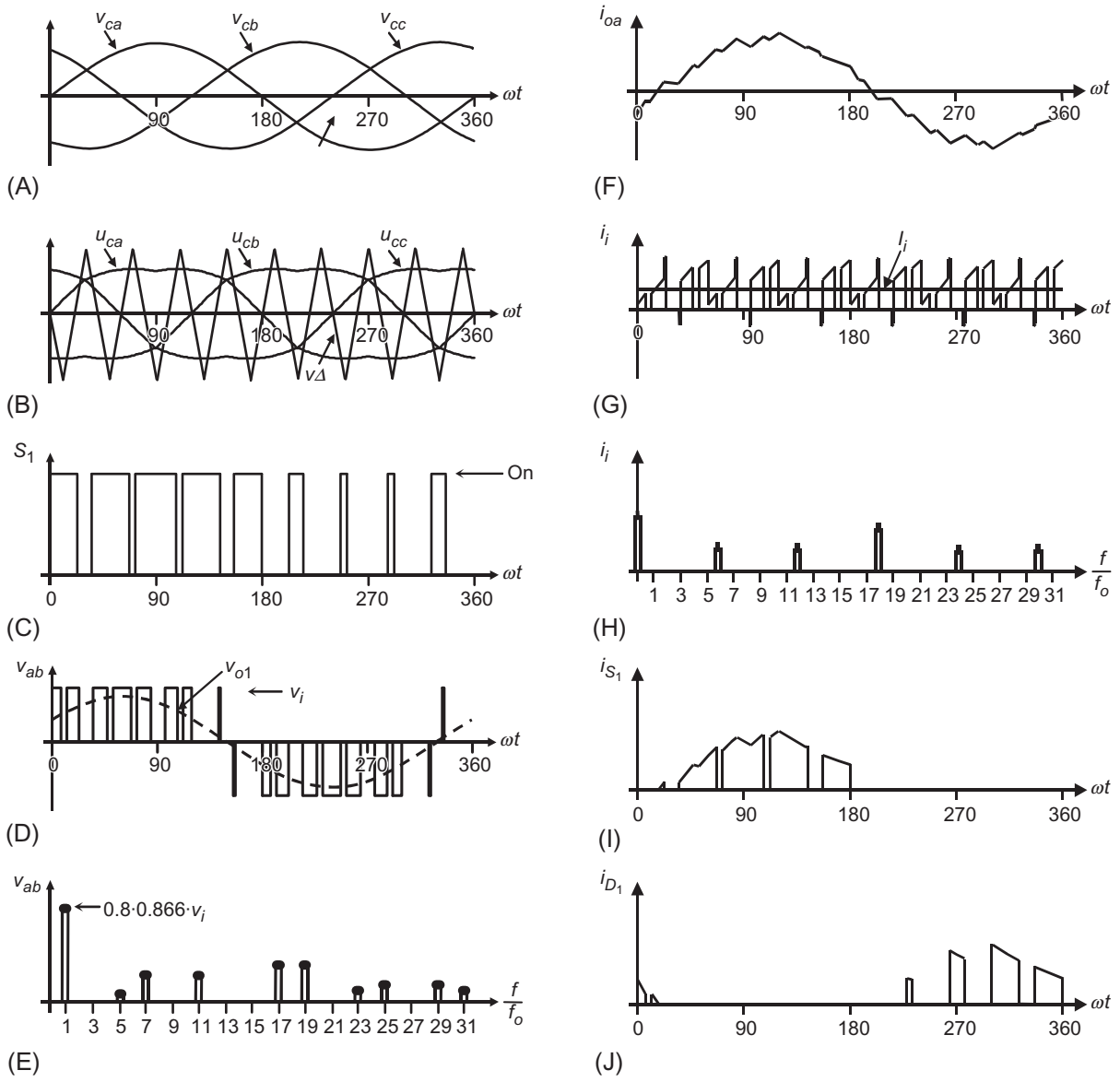


FIG. 11.21 The three-phase VSI. Ideal waveforms for the SPWM ($m_a = 0.8$, $m_f = 9$) with zero-sequence signal injection: (A) modulating signals, (B) carrier and modulating signals with zero-sequence signal injection, (C) switch S_1 state, (D) ac output voltage, (E) ac output voltage spectrum, (F) ac output current, (G) dc current, (H) dc current spectrum, (I) switch S_1 current, and (J) diode D_1 current.

the eight space vectors ($\vec{\mathbf{v}}_i$, $i = 1,2,\ldots,8$) in Fig. 11.24. As expected, $\vec{\mathbf{v}}_1$ to $\vec{\mathbf{v}}_6$ are nonnull line-voltage vectors, and $\vec{\mathbf{v}}_7$ and $\vec{\mathbf{v}}_8$ are null line-voltage vectors.

The objective of the SV technique is to approximate the line-modulating signal space vector $\vec{\mathbf{v}}_\mathbf{c}$ with the eight space vectors ($\vec{\mathbf{v}}_i$, $i = 1,2,\ldots,8$) available in VSIs. However, if the modulating signal $\vec{\mathbf{v}}_\mathbf{c}$ is laying between the arbitrary vectors $\vec{\mathbf{v}}_i$ and $\vec{\mathbf{v}}_{i+1}$, only the nearest two nonzero vectors ($\vec{\mathbf{v}}_i$ and $\vec{\mathbf{v}}_{i+1}$) and the zero SV ($\vec{\mathbf{v}}_z = \vec{\mathbf{v}}_7$ or $\vec{\mathbf{v}}_8$) should be used. Thus, the maximum load line voltage is maximized, and the switching frequency is minimized. To ensure that the generated voltage in one sampling period T_s (made up of the voltages provided by the vectors $\vec{\mathbf{v}}_i$, $\vec{\mathbf{v}}_{i+1}$, and $\vec{\mathbf{v}}_z$ used during times T_i, T_{i+1}, and T_z) is on average equal to the vector $\vec{\mathbf{v}}_\mathbf{c}$, the following expression should hold:

$$\vec{\mathbf{v}}_\mathbf{c} \cdot T_s = \vec{\mathbf{v}}_i \cdot T_s + \vec{\mathbf{v}}_{i+1} \cdot T_{i+1} + \vec{\mathbf{v}}_z \cdot T_z \tag{11.33}$$

The solution of the real and imaginary parts of Eq. (11.32) for a line-load voltage that features an amplitude restricted to $0 \le \hat{v}_c \le 1$ gives

$$T_i = T_s \cdot \hat{v}_c \cdot \sin(\pi/3 - \theta) \tag{11.34}$$

$$T_{i+1} = T_s \cdot \hat{v}_c \cdot \sin(\theta) \tag{11.35}$$

$$T_z = T_s - T_i - T_{i+1} \tag{11.36}$$

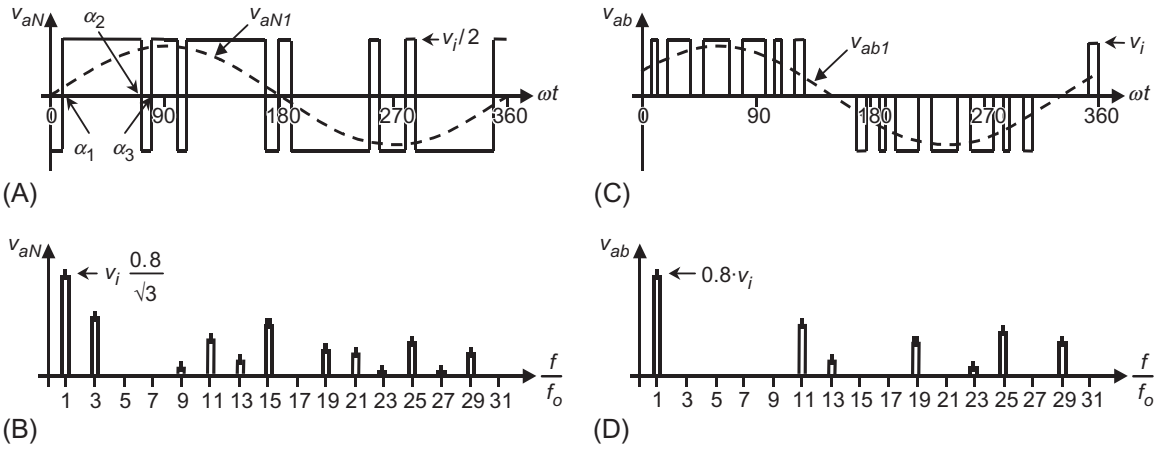


FIG. 11.22 The three-phase VSI. Ideal waveforms for the SHE technique: (A) phase voltage v_{aN} for fifth- and seventh-harmonic elimination, (B) spectrum of (A), (C) line voltage v_{ab} for fifth- and seventh-harmonic elimination, and (D) spectrum of (C).

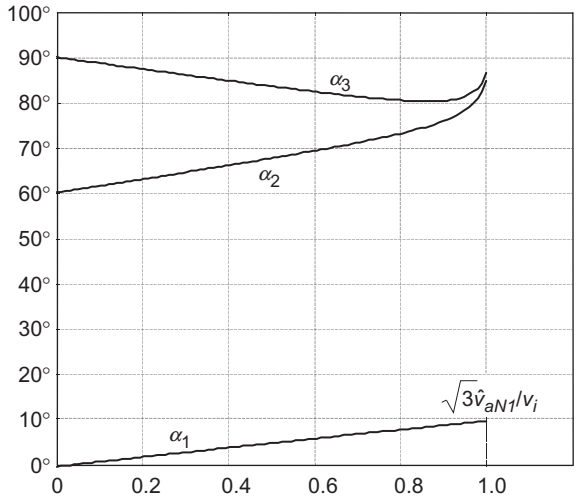


FIG. 11.23 Chopping angles for SHE and fundamental voltage control in three-phase VSIs: fifth- and seventh-harmonic elimination.

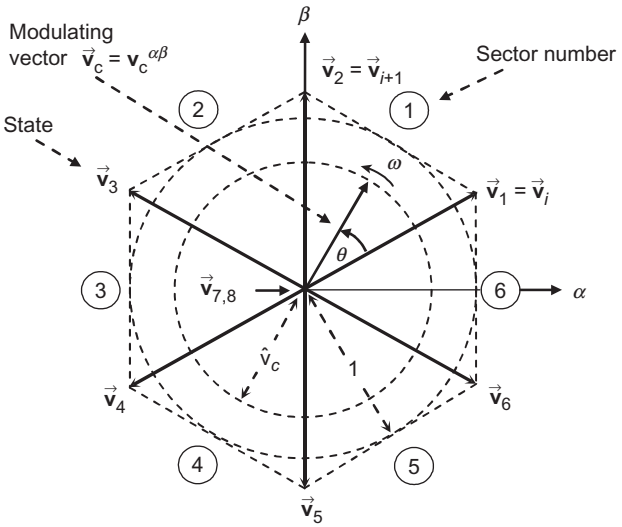


FIG. 11.24 The space-vector representation.

The preceding expressions indicate that the maximum fundamental line-voltage amplitude is unity as $0 \leq \theta \leq \pi/3$. This is an advantage over the SPWM technique that achieves a $\sqrt{3}/2$ maximum fundamental line-voltage amplitude in the linear operating region. Although the space-vector-modulation (SVM) technique selects the vectors to be used and their respective on-times, the sequence in which they are used, the selection of the zero space vector, and the normalized sampled frequency remain undetermined.

For instance, if the modulating line-voltage vector is in sector 1 (Fig. 11.24), the vectors $\vec{v}_1$, $\vec{v}_2$, and $\vec{v}_z$ should be used within a sampling period by intervals given by T_1, T_2, and T_z, respectively. However, the sequence should be different, for example, (i) $\vec{v}_1 - \vec{v}_2 - \vec{v}_z$, (ii) $\vec{v}_z - \vec{v}_1 - \vec{v}_2 - \vec{v}_z$, and (iii) $\vec{v}_z - \vec{v}_1 - \vec{v}_2 - \vec{v}_1 - \vec{v}_z$. Finally, the technique does not indicate whether $\vec{v}_z$ should be $\vec{v}_7$, $\vec{v}_8$, or a combination of both.

11.3.5.2 Space-Vector Sequences and Zero Space-Vector Selection

The sequence to be used should ensure load line voltages that feature quarter-wave symmetry in order to reduce unwanted harmonics in their spectra (even harmonics). Additionally, the zero SV selection should be done in order to reduce the switching frequency. Although there is not a systematic approach to generate a SV sequence, a graphic representation shows that the sequence $\vec{v}_i$, $\vec{v}_{i+1}$, $\vec{v}_z$ (where v_z is alternately chosen among $\vec{v}_7$ and $\vec{v}_8$) provides high performance in terms of minimizing unwanted harmonics and reducing the switching frequency.

11.3.5.3 The Normalized Sampling Frequency

The normalized carrier frequency m_f in three-phase carrier-based PWM techniques is chosen to be an odd integer number

multiple of 3 ($m_f = 3 \cdot n$, $n = 1,3,5,\ldots$). Thus, it is possible to minimize parasitic or nonintrinsic harmonics in the PWM waveforms. A similar approach can be used in the SVM technique to minimize uncharacteristic harmonics. Hence, it is found that the normalized sampling frequency f_{sn} should be an integer multiple of 6. This is due to the fact that in order to produce symmetrical line voltages, all the sectors (a total of six) should be used equally in one period. As an example, Fig. 11.25 shows the relevant waveforms of a VSI SVM for $f_{sn} = 18$ and $\hat{v}_c = 0.8$. Fig. 11.25 confirms that the first set of relevant harmonics in the load line voltage are at f_{sn}, which is also the switching frequency.

11.3.6 DC Link Current in Three-Phase VSIs

Due to the fact that the inverter is assumed to be lossless and constructed without storage energy components, the instantaneous power balance indicates that

$$v_i(t) \cdot i_i(t) = v_{ab}(t) \cdot i_a(t) + v_{bc}(t) \cdot i_b(t) + v_{ca}(t) \cdot i_c(t) \quad (11.37)$$

where $i_a(t)$, $i_b(t)$, and $i_c(t)$ are the phase-load currents as shown in Fig. 11.26. If the load is balanced and inductive and a relatively high switching frequency is used, the load currents become nearly sinusoidal balanced waveforms. On the other hand, if the ac output voltages are considered sinusoidal and

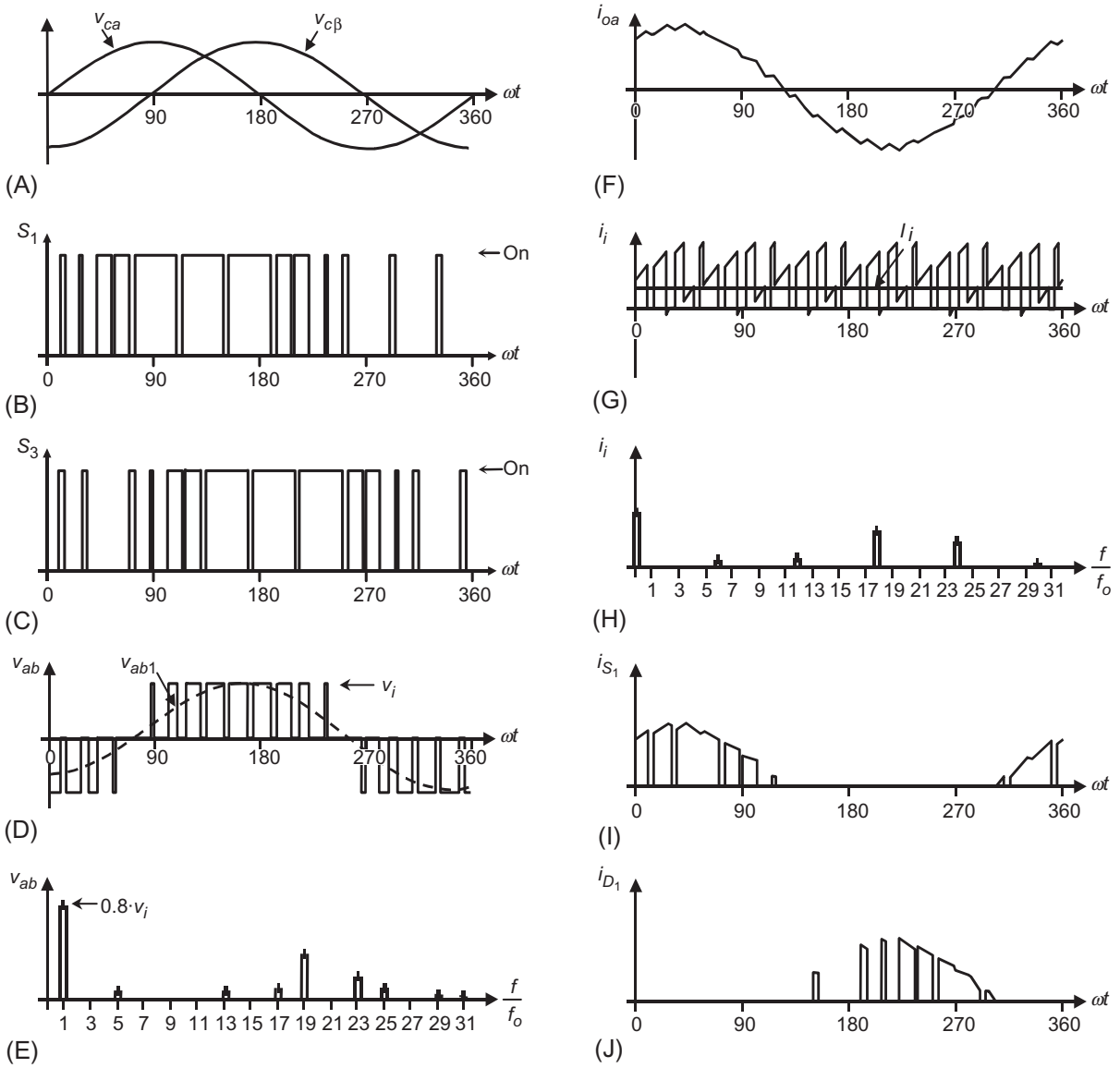


FIG. 11.25 The three-phase VSI. Ideal waveforms for space-vector modulation ($\hat{v}_c = 0.8$, $f_{sn} = 18$): (A) modulating signals, (B) switch S_1 state, (C) switch S_3 state, (D) ac output voltage, (E) ac output voltage spectrum, (F) ac output current, (G) dc current, (H) dc current spectrum, (I) switch S_1 current, and (J) diode D_1 current.

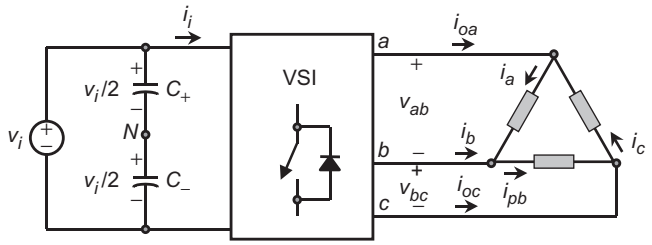


FIG. 11.26 Phase-load currents definition in a delta-connected load.

the dc link voltage is assumed constant $v_i(t) = V_i$, Eq. (11.37) can be simplified to

$$i_i(t) = \frac{1}{V_i}\left\{\begin{array}{l}\sqrt{2}V_{o1}\sin(\omega t)\cdot\sqrt{2}I_o\sin(\omega t-\phi)\\ +\sqrt{2}V_{o1}\sin(\omega t-120^\circ)\cdot\sqrt{2}I_o\sin(\omega t-120^\circ-\phi)\\ +\sqrt{2}V_{o1}\sin(\omega t-240^\circ)\cdot\sqrt{2}I_o\sin(\omega t-240^\circ-\phi)\end{array}\right\} \tag{11.38}$$

where V_{o1} is the fundamental rms ac output line voltage, I_o is the rms phase-load current, and ϕ is an arbitrary inductive load power factor. Hence, the dc link current expression can be further simplified to

$$i_i(t) = 3\frac{V_{o1}}{V_i}I_o\cos(\phi) = \sqrt{3}\frac{V_{o1}}{V_i}I_l\cos(\phi) \tag{11.39}$$

where $I_l = \sqrt{3}I_o$ is the rms load line current. The resulting dc link current expression indicates that under harmonic-free load voltages, only a clean dc current should be expected in the dc bus and, compared with single-phase VSIs, there is no presence of second harmonic. However, as the ac load line voltages contain harmonics around the normalized sampling frequency f_{sn}, the dc link current will contain harmonics but around f_{sn} as shown in Fig. 11.25H.

11.3.7 Phase-Load Voltage in Three-Phase VSIs

The load is sometimes wye-connected, and the phase-load voltages v_{an}, v_{bn}, and v_{cn} may be required (Fig. 11.27). To obtain them, it should be considered that the line-voltage vector is

$$\begin{bmatrix}v_{ab}\\ v_{bc}\\ v_{ca}\end{bmatrix} = \begin{bmatrix}v_{an}-v_{bn}\\ v_{bn}-v_{cn}\\ v_{cn}-v_{an}\end{bmatrix} \tag{11.40}$$

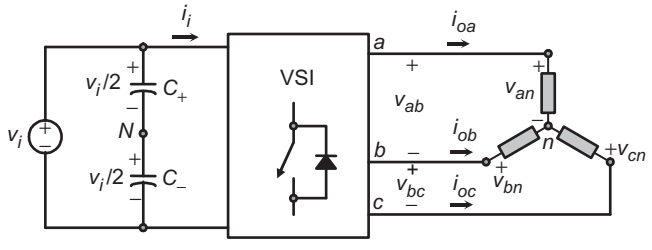


FIG. 11.27 Phase-load voltages definition in a wye-connected load.

which can be written as a function of the phase voltage vector $[v_{an}v_{bn}v_{cn}]^T$ as

$$\begin{bmatrix}v_{ab}\\ v_{bc}\\ v_{ca}\end{bmatrix} = \begin{bmatrix}1 & -1 & 0\\ 0 & 1 & -1\\ -1 & 0 & 1\end{bmatrix}\begin{bmatrix}v_{an}\\ v_{bn}\\ v_{cn}\end{bmatrix} \tag{11.41}$$

Expression (11.41) represents a linear system where the unknown quantity is the vector $[v_{an}v_{bn}v_{cn}]^T$. Unfortunately, the system is singular as the rows add up to zero (line voltages add up to zero); therefore, the phase-load voltages cannot be obtained by matrix inversion. However, if the phase-load voltages add up to zero, Eq. (11.41) can be rewritten as

$$\begin{bmatrix}v_{ab}\\ v_{bc}\\ 0\end{bmatrix} = \begin{bmatrix}1 & -1 & 0\\ 0 & 1 & -1\\ 1 & 1 & 1\end{bmatrix}\begin{bmatrix}v_{an}\\ v_{bn}\\ v_{cn}\end{bmatrix} \tag{11.42}$$

which is not singular, and hence,

$$\begin{bmatrix}v_{an}\\ v_{bn}\\ v_{cn}\end{bmatrix} = \begin{bmatrix}1 & -1 & 0\\ 0 & 1 & -1\\ 1 & 1 & 1\end{bmatrix}^{-1}\begin{bmatrix}v_{ab}\\ v_{bc}\\ 0\end{bmatrix} = \frac{1}{3}\begin{bmatrix}2 & 1 & 1\\ -1 & 1 & 1\\ -1 & -2 & 1\end{bmatrix}\begin{bmatrix}v_{ab}\\ v_{bc}\\ 0\end{bmatrix} \tag{11.43}$$

that can be further simplified to

$$\begin{bmatrix}v_{an}\\ v_{bn}\\ v_{cn}\end{bmatrix} = \frac{1}{3}\begin{bmatrix}2 & 1\\ -1 & 1\\ -1 & -2\end{bmatrix}\begin{bmatrix}v_{ab}\\ v_{bc}\end{bmatrix} \tag{11.44}$$

The final expression for the phase-load voltages is only a function of v_{ab} and v_{bc}, which is due to the fact that the last row in Eq. (11.42) is chosen to be only ones. Fig. 11.28 shows the line and phase voltages obtained using Eq. (11.44).

In the particular case of a square-wave three-phase VSI, this is known as a six-step inverter because of the six voltage changes per output voltage cycle.

11.4 Three-Phase Current Source Inverters

The main objective of these static power converters is to produce an ac output current waveforms from a dc current power supply. For sinusoidal ac outputs, its magnitude, frequency, and phase should be controllable. Due to the fact that the ac line currents i_{oa}, i_{ob}, and i_{oc} (Fig. 11.29) feature high di/dt, a capacitive filter should be connected at the ac output. These topologies are mainly used in medium-voltage industrial applications, where high-quality voltage waveforms are required.

In order to properly gate the power switches of a three-phase CSI, the compulsory rules of Section 11.2.2 are valid. The main constraints are that one top switch (1, 3, or 5 (Fig. 11.29)) and

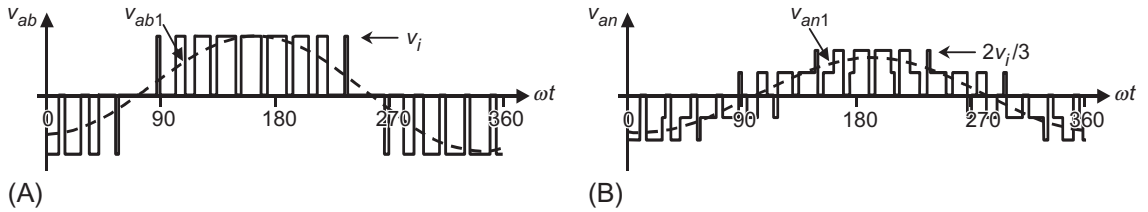


FIG. 11.28 The three-phase VSI and line- and phase-load voltages: (A) line-load voltage v_{ab} and (B) phase-load voltage v_{an}.

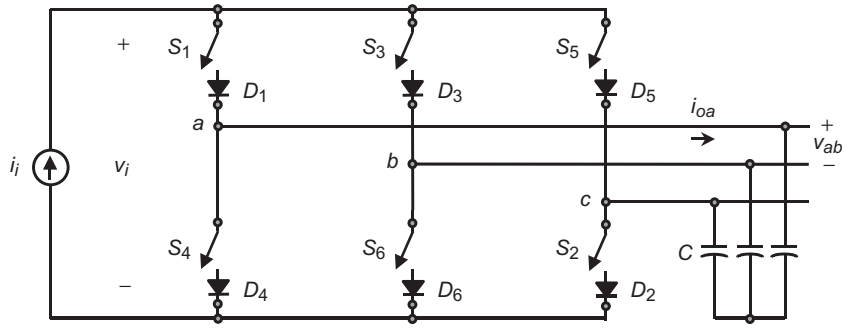


FIG. 11.29 Three-phase CSI topology.

TABLE 11.6 Valid switch states for a three-phase CSI

State	State no.	i_{oa}	i_{ob}	i_{oc}	Space vector
S_1 and S_2 are on, and S_3, S_4, S_5, and S_6 are off	1	i_i	0	$-i_i$	$\vec{\mathbf{i}}_1 = 1 + j0.577$
S_2 and S_3 are on, and S_4, S_5, S_6, and S_1 are off	2	0	i_i	$-i_i$	$\vec{\mathbf{i}}_2 = j1.155$
S_3 and S_4 are on, and S_5, S_6, S_1, and S_2 are off	3	$-i_i$	i_i	0	$\vec{\mathbf{i}}_3 = -1 + j0.577$
S_4 and S_5 are on, and S_6, S_1, S_2, and S_3 are off	4	$-i_i$	0	i_i	$\vec{\mathbf{i}}_4 = -1 - j0.577$
S_5 and S_6 are on, and S_1, S_2, S_3, and S_4 are off	5	0	$-i_i$	i_i	$\vec{\mathbf{i}}_5 = -j1.155$
S_6 and S_1 are on, and S_2, S_3, S_4, and S_5 are off	6	i_i	$-i_i$	0	$\vec{\mathbf{i}}_6 = 1 - j0.577$
S_1 and S_4 are on, and S_2, S_3, S_5, and S_6 are off	7	0	0	0	$\vec{\mathbf{i}}_7 = 0$
S_3 and S_6 are on, and S_1, S_2, S_4, and S_5 are off	8	0	0	0	$\vec{\mathbf{i}}_8 = 0$
S_5 and S_2 are on, and S_6, S_1, S_3, and S_4 are off	9	0	0	0	$\vec{\mathbf{i}}_9 = 0$

one bottom switch (4, 6, or 2 (Fig. 11.29)) should be closed at any time.

There are nine valid states in three-phase CSIs. The states 7, 8, and 9 (Table 11.6) produce zero ac line currents. The remaining states (1–6 in Table 11.6) produce nonzero ac output line currents. In order to generate a given set of ac line current waveforms, the inverter must move from one state to another. Thus, the resulting line currents consist of discrete values of current, which are i_i, 0, and $-i_i$. The selection of the states in order to generate the given waveforms is done by the modulating technique that should ensure the use of only the valid states.

There are several modulating techniques that deal with the special requirements of CSIs and can be implemented. These techniques are classified into three categories: (a) the carrier-based, (b) the SHE-based, and (c) the SV-based techniques. Although they are different, they generate gating signals that satisfy the special requirements of CSIs. To simplify the analysis, a constant dc link current source is considered ($i_i = I_i$).

11.4.1 Carrier-Based PWM Techniques in CSIs

It has been mentioned that the carrier-based PWM techniques that were initially developed for three-phase VSIs can be extended to three-phase CSIs. The circuit shown in Fig. 11.30 obtains the gating pattern for a CSI from the gating pattern developed for a VSI. As a result, the line current appears to be identical to the line voltage in a VSI for similar carrier and modulating signals.

It is composed of a switching pulse generator, a shorting pulse generator, a shorting pulse distributor, and a switching and shorting pulse combinator. The circuit basically produces the gating signals ($\mathbf{s} = [s_1 \ldots s_6]^T$) according to a carrier i_Δ and three modulating signals $\mathbf{i}_\mathbf{c}^{abc} = [i_{ca} i_{cb} i_{ca}]^T$.

The first component of this stage (Fig. 11.30) is the switching pulse generator, where the signals $\mathbf{s}_\mathbf{a}^{123}$ are generated according to

$$\mathbf{s}_\mathbf{a}^{123} = \begin{cases} \text{HIGH} = 1 \; if & \mathbf{i}_\mathbf{c}^{abc} > v_c \\ \text{LOW} = 0 & otherwise \end{cases} \tag{11.45}$$

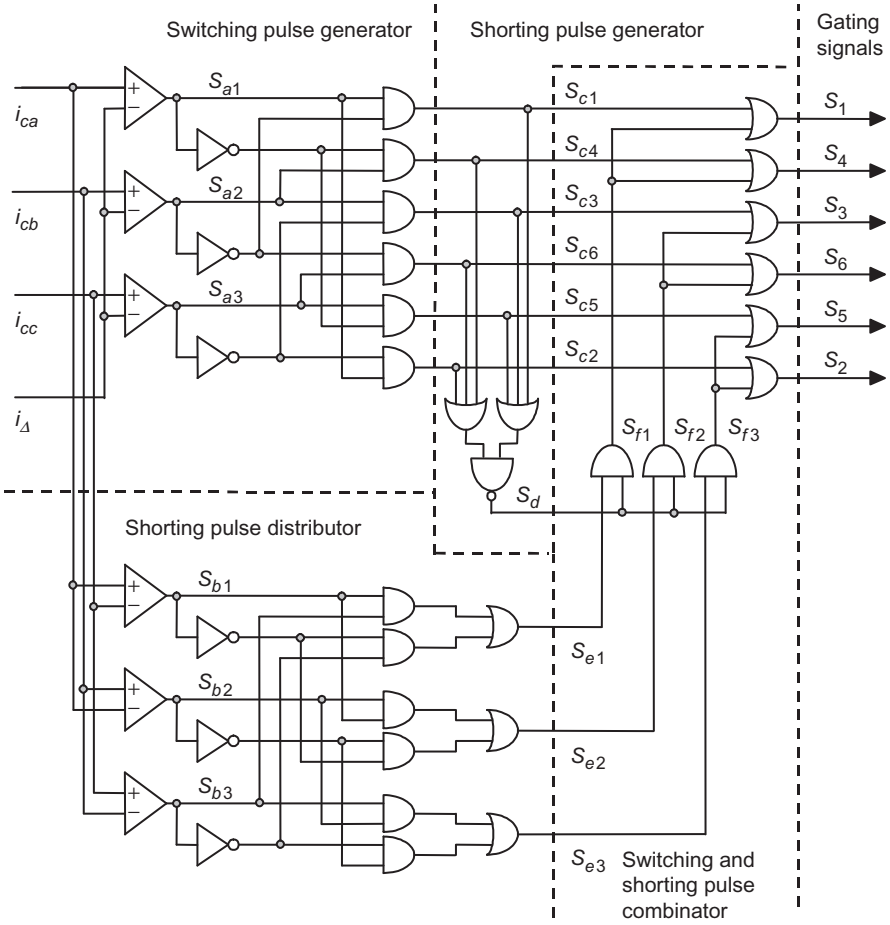


FIG. 11.30 The three-phase CSI. Gating pattern generator for analog online carrier-based PWM.

The outputs of the *switching pulse generator* are the signals $\mathbf{s_c}$, which are basically the gating signals of the CSI without the shorting pulses. These are necessary to inject the dc link current i_i when no zero ac output currents are required.

In order to satisfy the first compulsory rule for CSI, the shorting pulse ($s_d = 1$) is generated by the *shorting pulse generator* (Fig. 11.30); this are used to produce zero ac output currents. Then, this pulse is added (using OR gates) to only one leg of the CSI (either to the switches 1 and 4, 3 and 6, or 5 and 2) by means of the *switching and shorting pulse combinator* (Fig. 11.30). The signals generated by the *shorting pulse generator* $\mathbf{s_e}^{123}$ not only ensure that only one leg of the CSI is shorted at any time but also give an even distribution of the shorting pulse, as $\mathbf{s_e}^{123}$ is high for 120° in each period. This ensures that the rms currents are equal in all legs.

Fig. 11.31 shows the relevant waveforms if a triangular carrier i_{Δ} and sinusoidal modulating signals $\mathbf{i_c}^{abc}$ are used in combination with the gating pattern generator circuit (Fig. 11.30); this is SPWM in CSIs. It can be observed that some of the waveforms (Fig. 11.31) are identical to those obtained in three-phase VSIs, where an SPWM technique is used (Fig. 11.18). Specifically, (i) the load line voltage (Fig. 11.18D) in the VSI is identical to the load line current (Fig. 11.31D) in the CSI and (ii) the dc link current (Fig. 11.18G) in the VSI is identical to the dc link voltage (Fig. 11.31G) in the CSI.

This brings up the duality issue between both the topologies when similar modulation approaches are used. Therefore, for odd multiples of 3 values of the normalized carrier frequency m_f, the harmonics in the ac output current appear at normalized frequencies f_h centered around m_f and its multiples, specifically, at

$$h = l m_f \pm k \quad l = 1, 2, \ldots \tag{11.46}$$

where $l = 1, 3, 5, \ldots$ for $k = 2, 4, 6, \ldots$ and $l = 2, 4, \ldots$ for $k = 1, 5, 7, \ldots$ such that h is not a multiple of 3. Therefore, the harmonics will be at $m_f \pm 2$, $m_f \pm 4, \ldots$, $2m_f \pm 1$, $2m_f \pm 5, \ldots$, $3m_f \pm 2$, $3m_f \pm 4, \ldots$, $4m_f \pm 1$, $4m_f \pm 5, \ldots$. For nearly sinusoidal ac load voltages, the harmonics in the dc link voltage are at frequencies given by

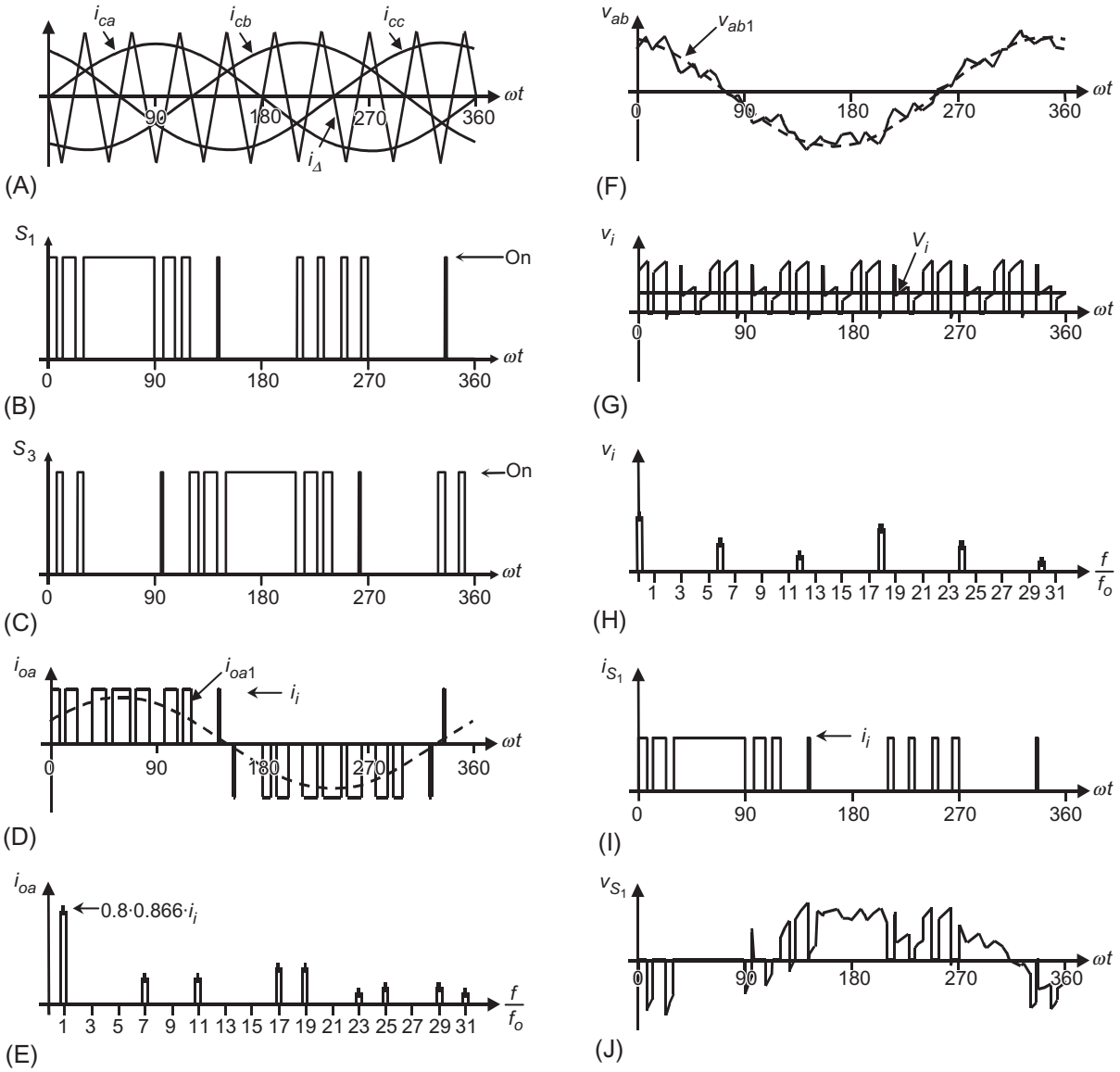


FIG. 11.31 The three-phase CSI. Ideal waveforms for the SPWM ($m_a = 0.8$, $m_f = 9$): (A) carrier and modulating signals, (B) switch S_1 state, (C) switch S_3 state, (D) ac output current, (E) ac output current spectrum, (F) ac output voltage, (G) dc voltage, (H) dc voltage spectrum, (I) switch S_1 current, and (J) switch S_1 voltage.

$$h = lm_f \pm k \pm 1 \quad l = 1,2,\ldots \tag{11.47}$$

where $l = 0,2,4,\ldots$ for $k = 1,5,7,\ldots$ and $l = 1,3,5,\ldots$ for $k = 2,4,6,\ldots$ such that $h = l \cdot m_f \pm k$ is positive and not a multiple of 3. For instance, Fig. 11.31H shows the sixth harmonic ($h = 6$), which is due to $h = 1 \cdot 9 - 2 - 1 = 6$. Identical conclusions can be drawn for the small and large values of m_f in the same way as for three-phase VSI configurations. Thus, the maximum amplitude of the fundamental ac output line current is $\hat{i}_{oa1} = \sqrt{3}i_i/2$, and therefore, one can write

$$\hat{i}_{oa1} = m_a \frac{\sqrt{3}}{2} i_i \quad 0 < m_a \leq 1 \tag{11.48}$$

To further increase the amplitude of the load current, the overmodulation approach can be used. In this region, the fundamental line currents range in

$$\frac{\sqrt{3}}{2} i_i < \hat{i}_{oa1} = \hat{i}_{ob1} = \hat{i}_{oc1} < \frac{4}{\pi}\frac{\sqrt{3}}{2} i_i \tag{11.49}$$

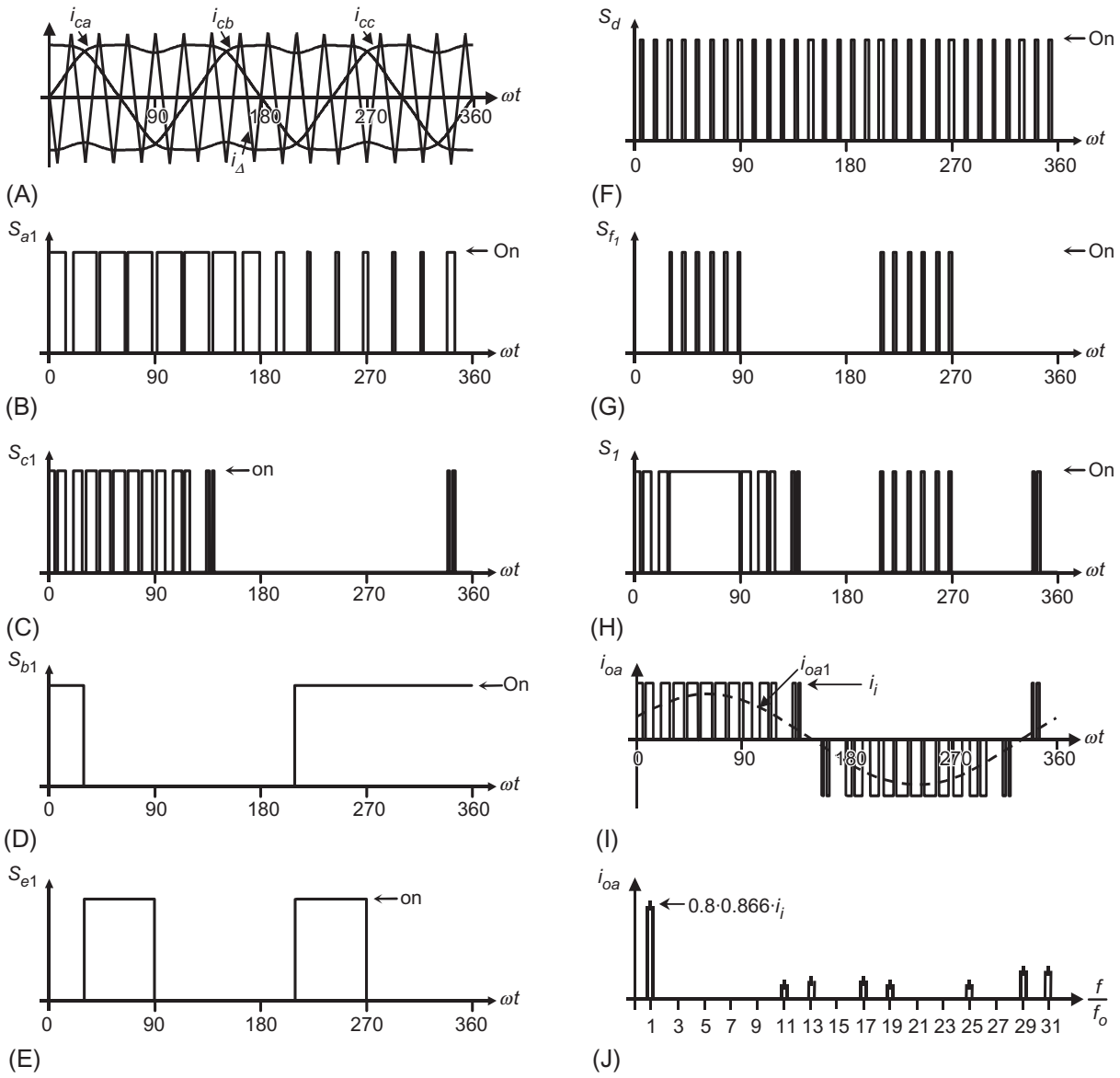


FIG. 11.32 Gating pattern generator. Waveforms for third- and ninth-harmonic injection PWM ($m_a = 0.8$, $m_f = 15$): signals as described in Fig. 11.30.

To further test the gating signal generator circuit (Fig. 11.30), a sinusoidal set with third- and ninth-harmonic injection modulating signals are used. Fig. 11.32 shows the relevant waveforms.

11.4.2 Square-Wave Operation of Three-phase CSIs

As in VSIs, large values of m_a in the SPWM technique lead to full overmodulation. This is known as square-wave operation. Fig. 11.33 depicts this operating mode in a three-phase CSI, where the power semiconductors are on for 120°. As presumed, the CSI cannot control the load current except by means of the dc link current i_i. This is due to the fact that the fundamental ac line current expression is

$$\hat{i}_{oa1} = \frac{4}{\pi}\frac{\sqrt{3}}{2} i_i \tag{11.50}$$

The ac line current contains the harmonics f_h, where $h = 6 \cdot k \pm 1$ ($k = 1, 2, 3, \ldots$), and they feature amplitudes that are inversely proportional to their harmonic order (Fig. 11.33D). Thus,

$$\hat{i}_{oah} = \frac{1}{h}\frac{4}{\pi}\frac{\sqrt{3}}{2} i_i \tag{11.51}$$

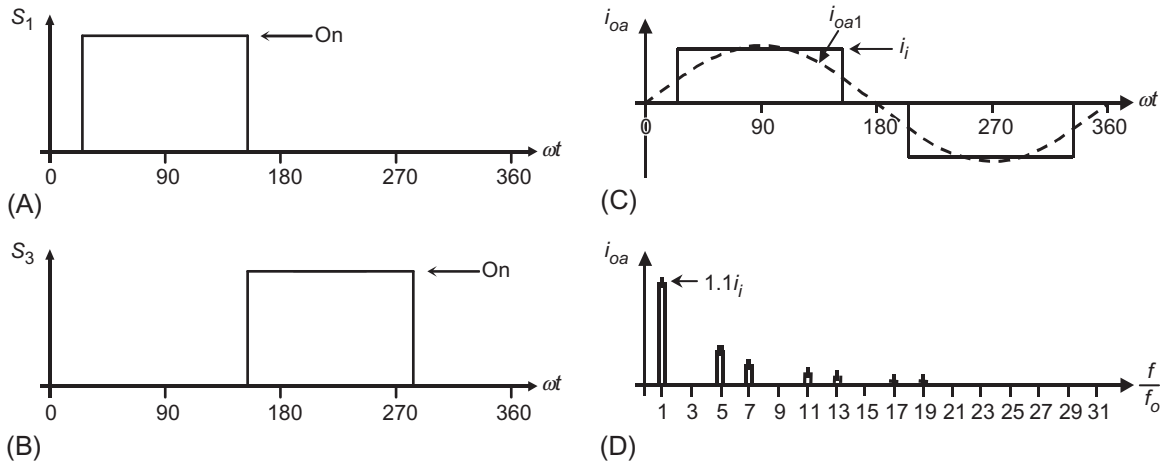


FIG. 11.33 The three-phase CSI. Square-wave operation: (A) switch S_1 state, (B) switch S_3 state, (C) ac output current, and (D) ac output current spectrum.

The duality issue among both the three-phase VSI and CSI should be noted especially in terms of the line-load waveforms. The line-load voltage produced by a VSI is identical to the load line current produced by the CSI when both are modulated using identical techniques. The next section will show that this also holds for SHE-based techniques.

11.4.3 Selective Harmonic Elimination in Three-phase CSIs

The SHE-based modulating techniques in VSIs define the gating signals such that a given number of harmonics are eliminated and the fundamental phase voltage amplitude is controlled. If the required line output voltages are balanced and 120° out of phase, the chopping angles are used to eliminate only the harmonics at frequencies $h = 5,7,11,13,\ldots$ as required.

The circuit shown in Fig. 11.34 uses the gating signals $\mathbf{s}_\mathbf{a}^{123}$ developed for a VSI and a set of synchronizing signals $\mathbf{i}_\mathbf{c}^{abc}$ to obtain the gating signals $\mathbf{s}$ for a CSI. The synchronizing signals $\mathbf{i}_\mathbf{c}^{abc}$ are sinusoidal balanced waveforms that are synchronized with the signals $\mathbf{s}_\mathbf{a}^{123}$ in order to symmetrically distribute the shorting pulse and thus generate symmetrical gating patterns. The circuit ensures line current waveforms as the line-voltage ones in a VSI. Therefore, any arbitrary number of harmonics can be eliminated, and the fundamental line current can be controlled in CSIs. Moreover, the same chopping angles obtained for VSIs can be used in CSIs.

For instance, to eliminate the fifth and seventh harmonics, the chopping angles are shown in Fig. 11.35, which are identical to that obtained for a VSI using Eq. (11.10). Fig. 11.36 shows that the line current does not contain the fifth and the seventh harmonics as expected. Hence, any number of harmonics can be eliminated in three-phase CSIs by means of the circuit (Fig. 11.34) without the hassle of how to satisfy the gating signal constrains.

11.4.4 Space-Vector-Based Modulating Techniques in CSIs

The objective of the SV-based modulating technique is to generate PWM load line currents that are on average equal to given load line currents. This is done digitally in each sampling period by properly selecting the switch states from the valid ones of the CSI (Table 11.6) and the proper calculation of the period of times they are used. As in VSIs, the selection and time calculations are based upon the space-vector transformation.

11.4.4.1 Space-Vector Transformation in CSIs

Similarly to VSIs, the vector of three-phase line-modulating signals $\mathbf{i}_\mathbf{c}^{abc} = [i_{ca}\, i_{cb}\, i_{cc}]^T$ can be represented by the complex vector $\vec{\mathbf{i}}_\mathbf{c} = \mathbf{i}_\mathbf{c}^{\alpha\beta} = [i_{c\alpha}\, i_{c\beta}]^T$ by means of Eqs. (11.31) and (11.32). For three-phase balanced sinusoidal modulating waveforms, which feature an amplitude $\hat{\imath}_c$ and an angular frequency ω, the resulting modulating signal complex vector $\vec{\mathbf{i}}_\mathbf{c} = \mathbf{i}_\mathbf{c}^{\alpha\beta}$ becomes a vector of fixed module $\hat{\imath}_c$, which rotates at frequency ω (Fig. 11.37). Similarly, the SV transformation is applied to the line currents of the nine states of the CSI normalized with respect to i_i, which generates nine space vectors ($\vec{\mathbf{i}}_i$, $i = 1,2,\ldots,9$ in Fig. 11.37). As expected, $\vec{\mathbf{i}}_1$ to $\vec{\mathbf{i}}_6$ are nonnull line current vectors, and $\vec{\mathbf{i}}_7$, $\vec{\mathbf{i}}_8$, and $\vec{\mathbf{i}}_9$ are null line current vectors.

The SV technique approximates the line-modulating signal space vector $\vec{\mathbf{i}}_\mathbf{c}$ by using the nine space vectors ($\vec{\mathbf{i}}_i$, $i = 1,2,\ldots,9$) available in CSIs. If the modulating signal vector $\vec{\mathbf{i}}_\mathbf{c}$ is between the arbitrary vectors $\vec{\mathbf{i}}_i$ and $\vec{\mathbf{i}}_{i+1}$, then $\vec{\mathbf{i}}_i$ and $\vec{\mathbf{i}}_{i+1}$ combined with one zero SV ($\vec{\mathbf{i}}_z = \vec{\mathbf{i}}_7$ or $\vec{\mathbf{i}}_8$ or $\vec{\mathbf{i}}_9$) should be used to generate $\vec{\mathbf{i}}_\mathbf{c}$. To ensure that the generated current in one sampling period T_s (made up of the currents provided by the vectors $\vec{\mathbf{i}}_i$, $\vec{\mathbf{i}}_{i+1}$, and $\vec{\mathbf{i}}_z$ used during times T_i, T_{i+1}, and T_z) is on average equal to the vector $\vec{\mathbf{i}}_\mathbf{c}$, the following expressions should hold:

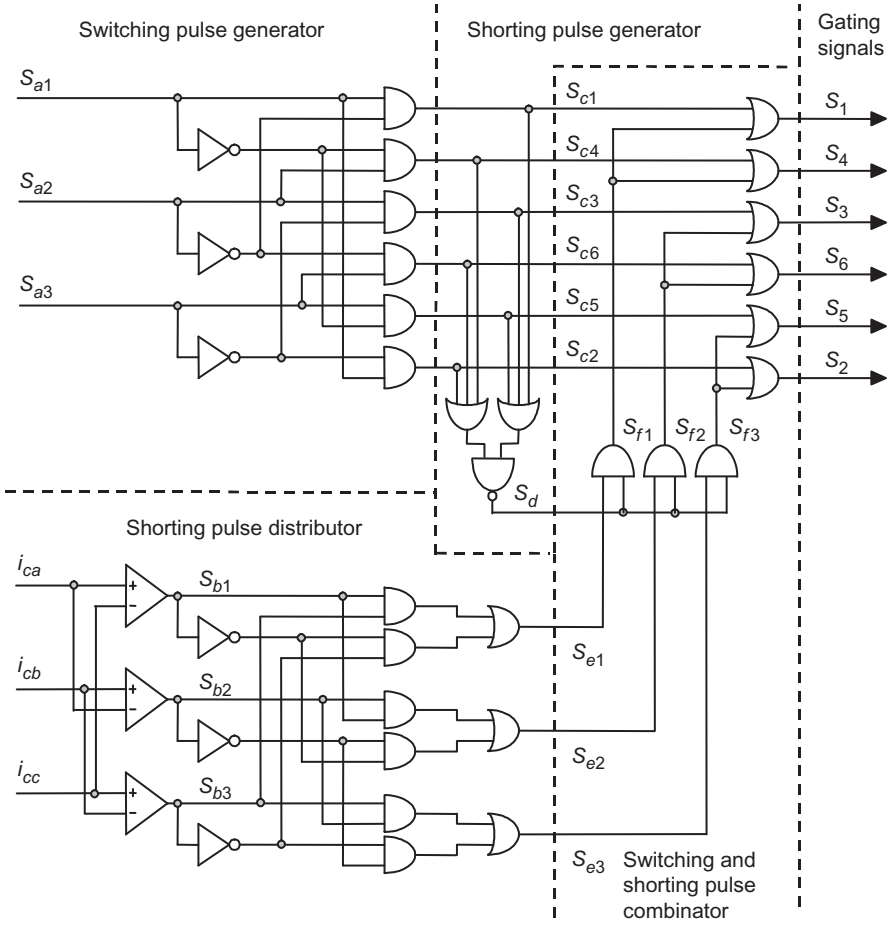


FIG. 11.34 The three-phase CSI. Gating pattern generator for SHE PWM techniques.

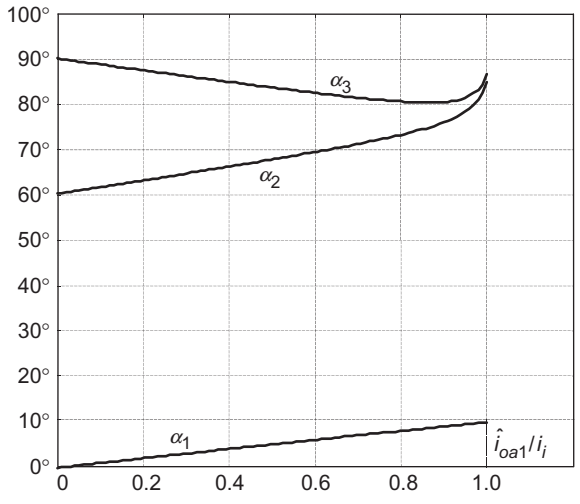


FIG. 11.35 Chopping angles for SHE and fundamental current control in three-phase CSIs, fifth- and seventh-harmonic elimination.

$$T_i = T_s \cdot \hat{i}_c \cdot \sin(\pi/3 - \theta) \tag{11.52}$$

$$T_{i+1} = T_s \cdot \hat{i}_c \cdot \sin(\theta) \tag{11.53}$$

$$T_z = T_s - T_i - T_{i+1} \tag{11.54}$$

where $0 \leq \hat{i}_c \leq 1$. Although the SVM technique selects the vectors to be used and their respective on-times, the sequence in which they are used, the selection of the zero space vector, and the normalized sampled frequency remain undetermined.

11.4.4.2 Space-Vector Sequences and Zero Space-Vector Selection

Although there is no systematic approach to generate a SV sequence, a graphic representation shows that the sequence $\vec{\mathbf{i}}_i$, $\vec{\mathbf{i}}_z$, $\vec{\mathbf{i}}_{i+1}$ (where the chosen $\vec{\mathbf{i}}_z$ depends upon the sector) provides high performance in terms of minimizing unwanted harmonics and reducing the switching frequency. To obtain

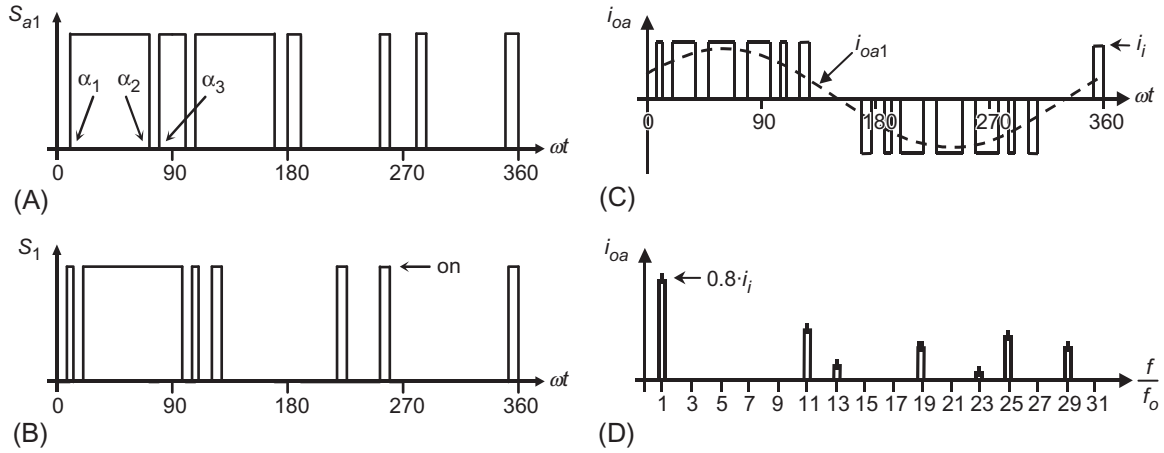


FIG. 11.36 The three-phase CSI. Ideal waveforms for the SHE technique: (A) VSI gating pattern for fifth- and seventh-harmonic elimination, (B) CSI gating pattern for fifth- and seventh-harmonic elimination, (C) line current i_{oa} for fifth- and seventh-harmonic elimination, and (D) spectrum of (C).

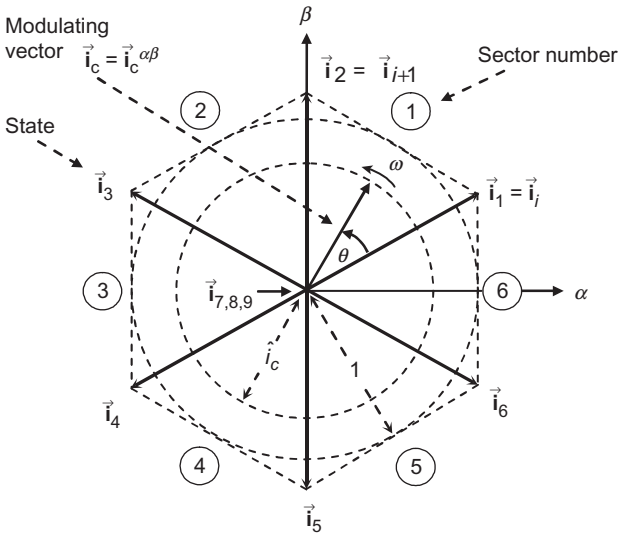


FIG. 11.37 The space-vector representation in CSIs.

the zero SV that minimizes the switching frequency, it is assumed that $\mathbf{I_c}$ is in sector ②. Then, Fig. 11.38 shows all the possible transitions that could be found in sector ②. It can be seen that the zero vector $\vec{\mathbf{i}}_9$ should be chosen to minimize the switching frequency in all cases. Table 11.7 gives a summary of the zero space vector to be used in each sector in order to minimize the switching frequency. However, it should be noted that Table 11.7 is valid only for the sequence $\vec{\mathbf{i}}_i$, $\vec{\mathbf{i}}_{i+1}$, $\vec{\mathbf{i}}_z$. Another sequence will require reformulating the zero space-vector selection algorithm.

11.4.4.3 The Normalized Sampling Frequency

As in VSIs modulated by an SV approach, the normalized sampling frequency f_{sn} should be an integer multiple of 6 to minimize uncharacteristic harmonics. As an example, Fig. 11.39 shows the relevant waveforms of a CSI SVM for $f_{sn} = 18$ and $\hat{i}_c = 0.8$. Fig. 11.39 also shows that the first set of relevant harmonics load line current are at f_{sn}.

11.4.5 DC Link Voltage in Three-phase CSIs

An instantaneous power balance indicates that

$$v_i(t) \cdot i_i(t) = v_{an}(t) \cdot i_{oa}(t) + v_{bn}(t) \cdot i_{ob}(t) + v_{cn}(t) \cdot i_{oc}(t) \tag{11.55}$$

where $v_{an}(t)$, $v_{bn}(t)$, and $v_{cn}(t)$ are the phase filter voltages as shown in Fig. 11.40. If the filter is large enough and a relatively high switching frequency is used, the phase voltages become nearly sinusoidal balanced waveforms. On the other hand, if the ac output currents are considered sinusoidal and the dc link current is assumed constant $i_i(t) = I_i$, Eq. (11.55) can be simplified to

$$v_i(t) = \frac{1}{I_i}\left\{\begin{array}{l}\sqrt{2}V_{on}\sin(\omega t)\cdot\sqrt{2}I_{o1}\sin(\omega t - \phi) \\ +\sqrt{2}V_{on}\sin(\omega t - 120^\circ)\cdot\sqrt{2}I_{o1}\sin(\omega t - 120^\circ - \phi) \\ +\sqrt{2}V_{on}\sin(\omega t - 240^\circ)\cdot\sqrt{2}I_{o1}\sin(\omega t - 240^\circ - \phi)\end{array}\right\} \tag{11.56}$$

where V_{on} is the rms ac output phase voltage, I_{o1} is the rms fundamental line current, and ϕ is an arbitrary filter-load angle. Hence, the dc link voltage expression can be further simplified to the following:

$$v_i(t) = 3\frac{I_{o1}}{I_i}V_{on}\cos(\phi) = \sqrt{3}\frac{I_{o1}}{I_i}V_o\cos(\phi) \tag{11.57}$$

where $V_o = \sqrt{3}V_{on}$ is the rms load line voltage. The resulting dc link voltage expression indicates that the first line current harmonic I_{o1} generates a clean dc current. However, as the load line currents contain harmonics around the normalized

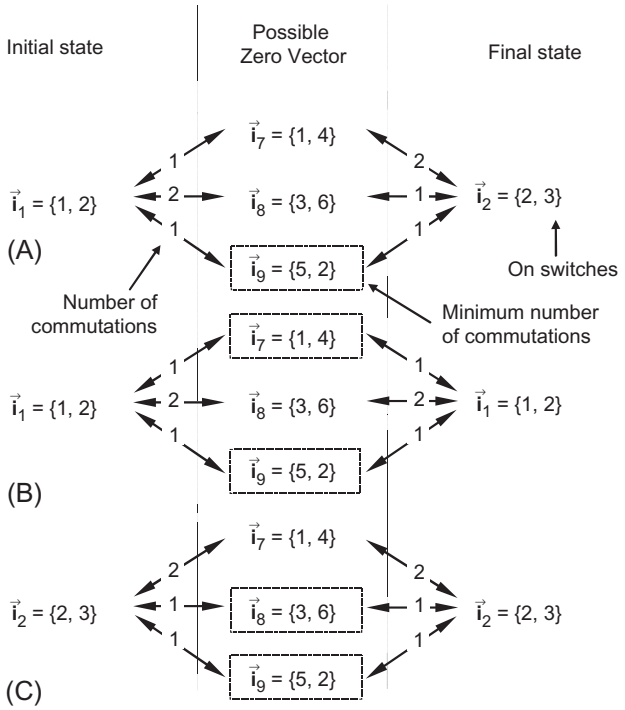


FIG. 11.38 Possible state transitions in sector ② involving a zero SV: (A) transition, $\vec{i}_1 \Leftrightarrow \vec{i}_z \Leftrightarrow \vec{i}_2$ or $\vec{i}_2 \Leftrightarrow \vec{i}_z \Leftrightarrow \vec{i}_1$; (B) transition, $\vec{i}_1 \Leftrightarrow \vec{i}_z \Leftrightarrow \vec{i}_1$; and (C) transition, $\vec{i}_2 \Leftrightarrow \vec{i}_z \Leftrightarrow \vec{i}_2$.

TABLE 11.7 Zero SV for minimum switching frequency in CSI and sequence $\vec{i}_i$, $\vec{i}_{i+1}$, $\vec{i}_z$

Sector	$\vec{i}_i$	$\vec{i}_{i+1}$	$\vec{i}_z$
①	$\vec{i}_6$	$\vec{i}_1$	$\vec{i}_7$
②	$\vec{i}_1$	$\vec{i}_2$	$\vec{i}_9$
③	$\vec{i}_2$	$\vec{i}_3$	$\vec{i}_8$
④	$\vec{i}_3$	$\vec{i}_4$	$\vec{i}_7$
⑤	$\vec{i}_4$	$\vec{i}_5$	$\vec{i}_9$
⑥	$\vec{i}_5$	$\vec{i}_6$	$\vec{i}_8$

sampling frequency f_{sn}, the dc link current will contain harmonics but around f_{sn} as shown in Fig. 11.39H. Similarly, in carrier-based PWM techniques, the dc link current will contain harmonics around the carrier frequency m_f (Fig. 11.31).

In practical implementations, a CSI requires a dc current source that should behave as a constant (as required by PWM CSIs) or variable (as square-wave CSIs) current source. Such current sources should be implemented as separate units.

11.5 Multilevel Inverters

The traditional inverters can generate an output in two or three different levels. For instance, a single-phase full-bridge inverter can produce v_i, $-v_i$, and zero; this type of output is unacceptable in the medium- to high-voltage ranges due to the high dv/dt present in the PWM ac line voltages. In order to solve this, the multilevel inverters were initially proposed. However, now, their use has been more extended not only due to the low harmonic content obtained at low switching frequencies but also for the good efficiency obtained.

Different multilevel topologies have been proposed. The goal is to produce an output defined by different levels that can be voltage or current levels. The basic principle is to connect the output to multiple points, one at a time. Fig. 11.41A shows the idea for a voltage-source configuration. Usually, the number M of possible level defines the name of the inverter; for instance, if five points are available as in Fig. 11.41A ($M = 5$), the inverter is usually named a five-level inverter.

For a five-level inverter, the output voltage shown in Fig. 11.41B would be produced. By simple inspection, this output voltage looks more similar to a sinusoidal waveform; then, the harmonic content is expected to be lower than traditional inverters, and the power semiconductors are operating at low switching frequency.

11.5.1 Voltage Source-Based Multilevel Topologies

The three-phase VSI can be called also two-level VSI due to the fact that the inverter phase voltages v_{aN}, v_{bN}, and v_{cN}

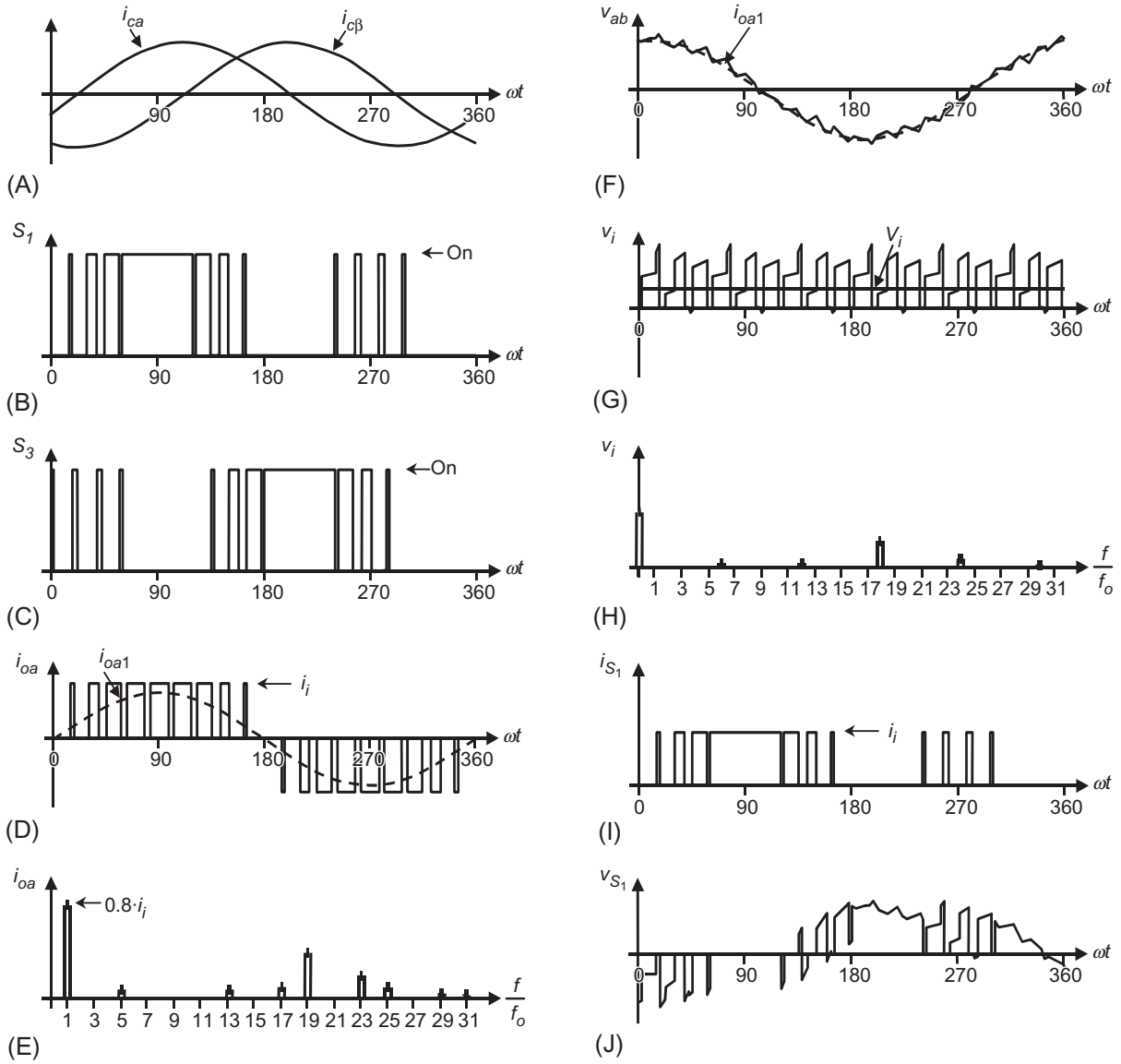


FIG. 11.39 The three-phase CSI. Ideal waveforms for space-vector modulation ($\hat{i}_c = 0.8$, $f_{sn} = 18$): (A) modulating signals, (B) switch S_1 state, (C) switch S_3 state, (D) ac output current, (E) ac output current spectrum, (F) ac output voltage, (G) dc voltage, (H) dc voltage spectrum, (I) switch S_1 current, and (J) switch S_1 voltage.

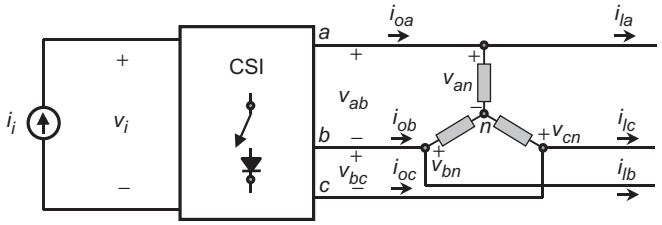


FIG. 11.40 Phase voltage definition in a wye-connected filter.

(Fig. 11.17) are instantaneously either $v_i/2$ or $-v_i/2$. In other words, the phase voltages can take one of the two voltage levels. However, regarding to multilevel inverters, the topologies usually have more than two levels.

The typical multilevel voltage-source topologies are the neutral-point-clamped (also called diode-clamped) inverters, the flying capacitors, and the cascaded configuration. Since they are voltage-source converters, the compulsory rules described in Section 11.2.1 also apply, but certainly, some remarks are made for each converter.

11.5.1.1 Neutral Point Clamped Inverter

In Fig. 11.42, the neutral-point-clamped inverter is shown (three levels). For this topology, not only an M-level inverter requires $(M-1)$ capacitors and $2(M-1)$ switching semiconductors per leg, but also $2(M-2)$ additional diodes must be

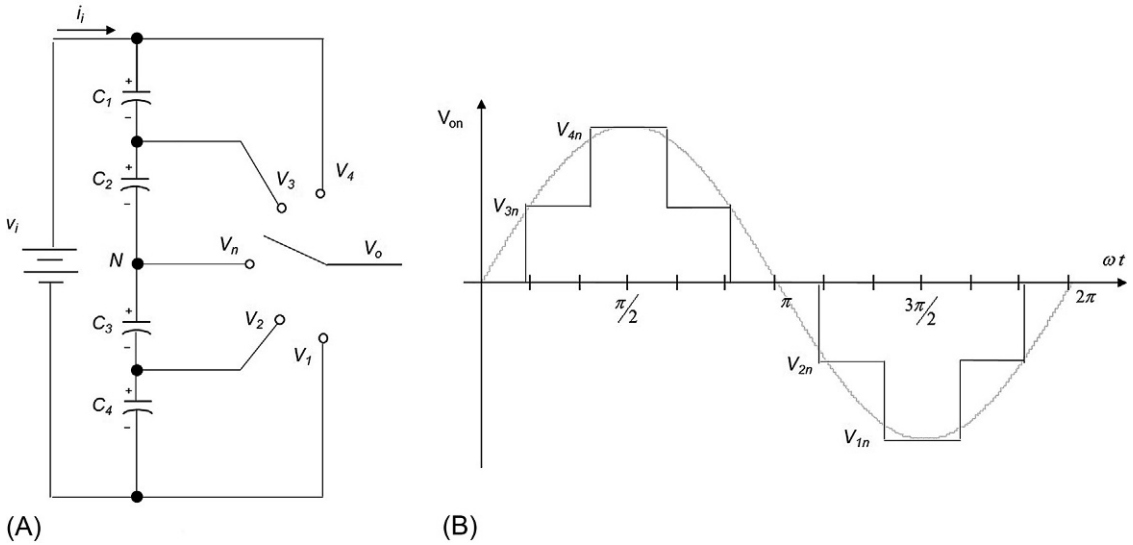


FIG. 11.41 Basic principle of multilevel output: (A) voltage source and (B) typical output.

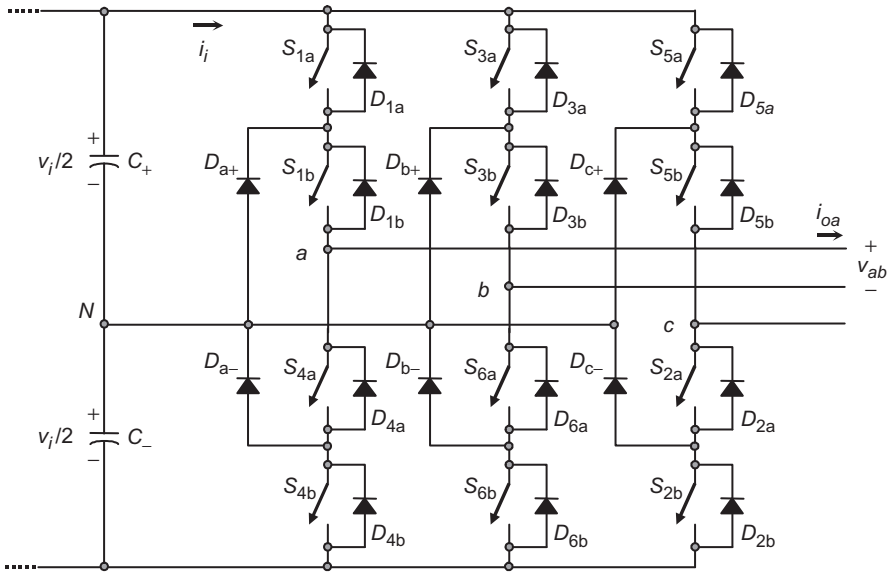


FIG. 11.42 Three-phase three-level VSI topology, neutral-point-clamped inverter.

included per leg; for instance, D_{a+} and D_{a-} are added for the left leg. $M-1$ devices per leg must be on to select the desired level.

Table 11.8 gives the switch states of the three-level inverter, just left leg. As it can be observed, not only always two switches are on, but also the signal S_{1a} is the opposite of S_{4a}, and S_{1b} is the opposite of S_{4b}. These conditions must be always satisfied. The switch states for phases *b* and c are identical to those of phase *a*.

TABLE 11.8 Valid switch states for the three-level neutral-point-clamped inverter, the left leg

s_{1a}	s_{1b}	s_{4a}	s_{4b}	v_{an}	Components conducting	
1	1	0	0	$v_i/2$	S_{1a}, S_{1b}	If $i_{oa}>0$
					D_{1a}, D_{1b}	If $i_{oa}<0$
0	1	1	0	0	S_{1b}, D_{a+}	If $i_{oa}>0$
					S_{4a}, D_{a-}	If $i_{oa}<0$
0	0	1	1	$-v_i/2$	D_{4a}, D_{4b}	If $i_{oa}>0$
					S_{4a}, S_{4b}	If $i_{oa}<0$

11.5.1.2 Flying Capacitors Inverter

In Fig. 11.43, the flying capacitor inverter is shown (three levels). For this topology, an *M*-level inverter requires

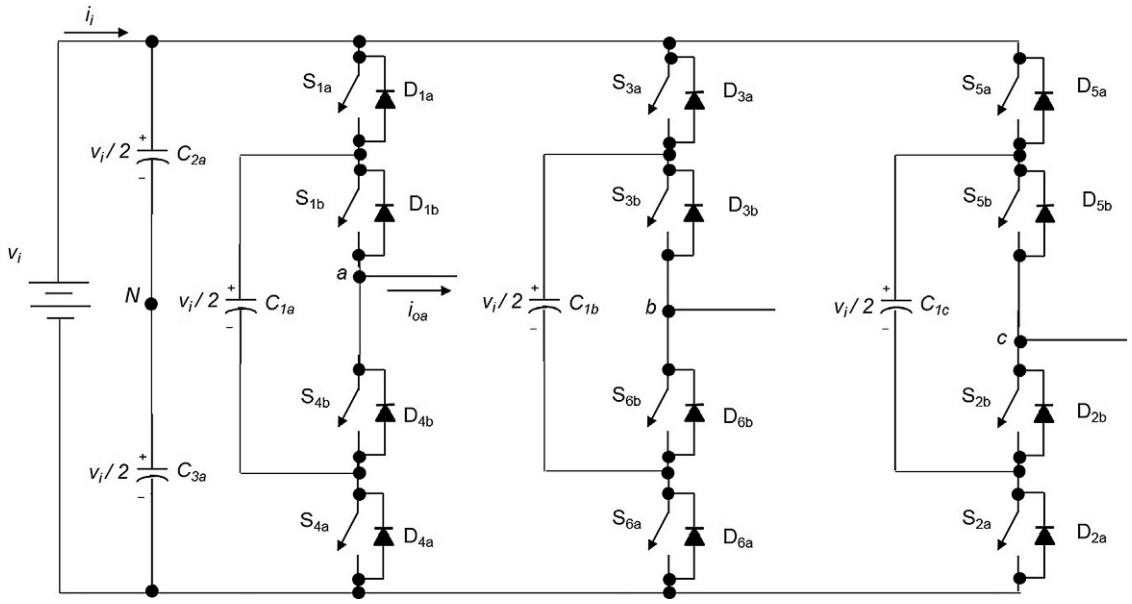


FIG. 11.43 Three-phase three-level VSI topology, flying capacitors.

$\sum_{j=1}^{M-1}(M-j)$ capacitors per leg (considering that the capacitors have the same voltage rating) and $2(M-1)$ switching semiconductors per leg, but no additional diodes are required. Also $M-1$ switches per leg must be on to select the desired level.

Table 11.9 is the switch state of the three-level inverter, just left leg. As it can be observed, not only always two switches are on, but also the signal S_{1a} is the opposite of S_{4a}, and S_{1b} is the opposite of S_{4b}. These conditions must be always satisfied. Table 11.9 shows that there is more than one switching state to produce the zero output level; this redundancy should be employed to distribute the losses or to regulate the capacitor voltages. Moreover, as the number of levels increase, more redundancy exists at different levels.

11.5.1.3 Casacade Inverter

In Fig. 11.44, the cascade inverter is shown (five levels). This topology is based on several full-bridge single-phase voltage-source inverters with their output connected in series. An M-level inverter requires $(M-1)/2$ single-phase full-bridge VSI per leg and $2(M-1)$ switching semiconductors per leg, but no additional diodes are required. Also $M-1$ switches per leg must be on to select the desired level.

Table 11.10 gives the switch states of the five-level inverter. Notice that only the top switch control signals of each single-phase full-bridge VSI are shown. Their respective bottom switch control signals are complementary, in order to accomplish with the first compulsory rule for VSIs. As it can be observed, always four devices are on; notice that since a single-phase full-bridge inverter is used, the same rules apply for the control signals of the semiconductors. As it can be observed in Table 11.10, there are more than one switching state to produce some output levels; this redundancy should be employed to distribute the losses. Moreover, as the number of levels increases, more redundancy exists at different levels.

TABLE 11.9 Valid switch states for the three-level flying capacitors inverter, left leg

s_{1a}	s_{1b}	s_{4a}	s_{4b}	v_{aN}	Components conducting	
1	1	0	0	$v_i/2$	S_{1a}, S_{1b}	If $i_{oa}>0$
					D_{1a}, D_{1b}	If $i_{oa}<0$
1	0	0	1	0	S_{1a}, D_{4b}	If $i_{oa}>0$
					D_{1a}, S_{4b}	If $i_{oa}<0$
0	1	1	0	0	S_{1b}, D_{4a}	If $i_{oa}>0$
					D_{1b}, S_{4a}	If $i_{oa}<0$
0	0	1	1	$-v_i/2$	D_{4a}, D_{4b}	If $i_{oa}>0$
					S_{4a}, S_{4b}	If $i_{oa}<0$

11.5.2 Current Source-Based Multilevel Topologies

Duality is found in many aspects related to voltage- and current-source inverters. Perhaps, the most evident is the duality in terms of modulating techniques. Thus, current-source-based multilevel topologies are available as well. There are different topologies reported: paralleled, two-stage, and embedded configurations.

Fig. 11.45 shows a three-level $M=3$ current-source topology, which is formed by paralleling two three-phase CSI topologies, the named paralleled CSI (Table 11.11). The main goal is to share evenly the ac current $\mathbf{i}_{\mathbf{o}}^{\mathbf{abc}}$ among the two topologies ($\mathbf{i}_{\mathbf{o}}^{\mathbf{abc}}/2=\mathbf{i}_{\mathbf{o1}}^{\mathbf{abc}}=\mathbf{i}_{02}^{\mathbf{abc}}$). This should be ensured by having equal

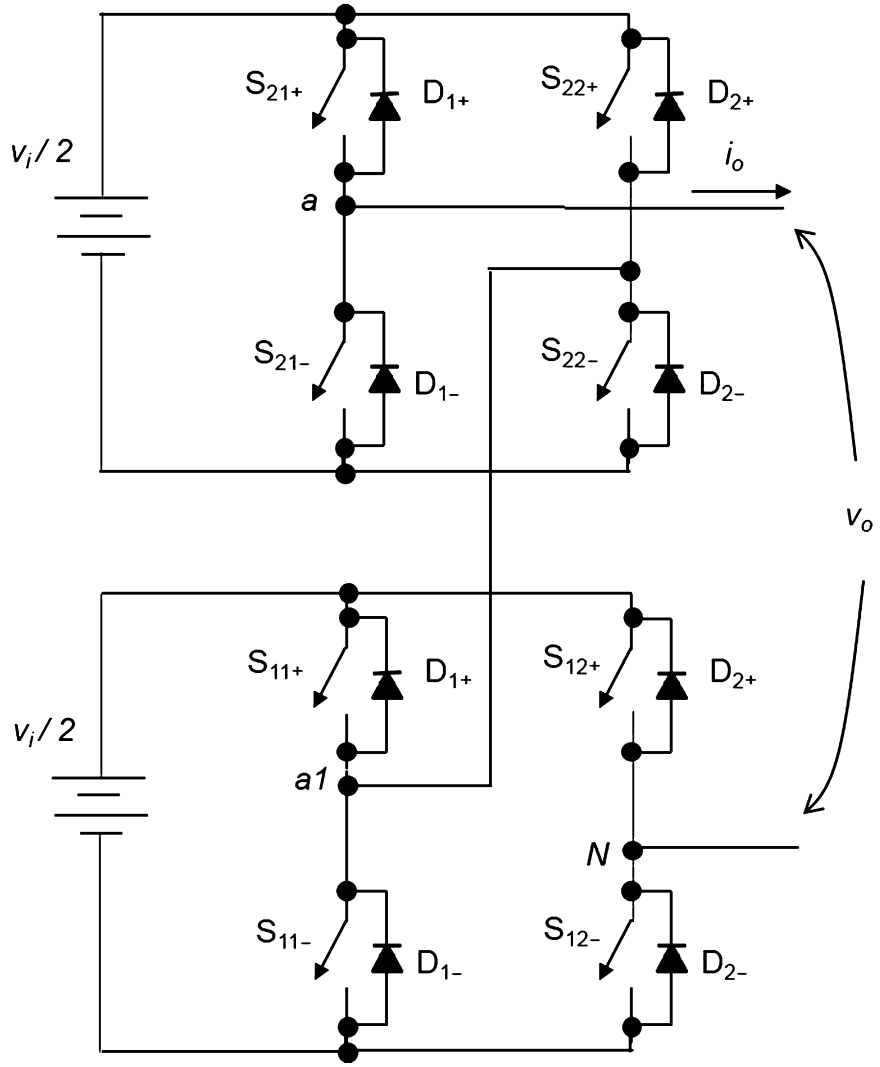


FIG. 11.44 Single-phase five-level VSI topology, cascade.

TABLE 11.10 Valid switch states for the five-level cascade inverter, left leg

s_{21+}	s_{22+}	s_{11+}	s_{12+}	v_{an}
1	0	1	0	v_i
1	0	0	0	$v_i/2$
1	0	1	1	$v_i/2$
0	0	1	0	$v_i/2$
1	1	1	0	$v_i/2$
0	0	0	0	0
0	0	1	1	0
1	0	0	1	0
0	1	1	0	0
1	1	0	0	0
1	1	1	1	0
0	1	0	0	$-v_i/2$
0	1	1	1	$-v_i/2$
0	0	0	1	$-v_i/2$
1	1	0	1	$-v_i/2$
0	1	0	1	$-v_i$

dc link currents ($i_{i1} = i_{i2}$). Similarly to voltage-source-based multilevel topologies, this could be achieved either by using two independent dc link currents or by properly gating the power semiconductors.

11.5.3 Modulation Techniques in Multilevel Inverters

As in traditional inverters, the sinusoidal pulse width and space-vector modulation can be employed in multilevel inverters, for both CSI and VSI.

11.5.3.1 The SPWM Technique

The main objective is to generate the appropriate gating signals so as to obtain fundamental inverter phase voltages or currents equal to a given set of modulating signals. Specifically, the SPWM in three-level VSIs uses a sinusoidal set of modulating signals (v_{ca}, v_{cb}, and v_{cc} for phases a, b, and c, respectively) and

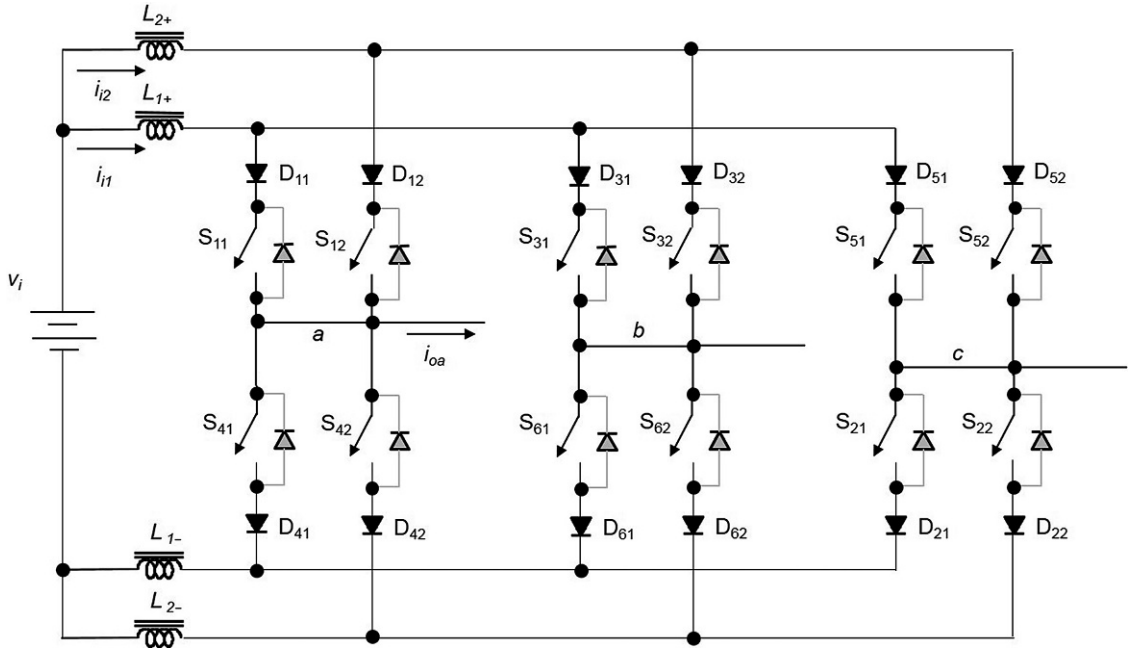


FIG. 11.45 Three-phase three-level paralleled CSI topology.

TABLE 11.11 Valid switch states for the three-level paralleled inverter, left legs

s_{11}	s_{12}	s_{41}	s_{42}	i_{oa}
1	1	0	0	$i_{i2}+i_{i1}$
1	1	0	1	i_{i1}
1	1	1	0	i_{i2}
1	1	1	1	0
1	0	1	1	$-i_{i2}$
0	1	1	1	$-i_{i1}$
0	0	1	1	$-(i_{i2}+i_{i1})$

$M-1=2$ triangular type of carrier signals ($v_{\Delta 1}$ and $v_{\Delta 2}$) as illustrated in Fig. 11.46A. The best results are obtained if the carrier signals are in-phase (synchronized with the modulating signal) and feature an odd normalized frequency (e.g., $m_f=15$). According to Fig. 11.46A and considering a neutral-point-clamped inverter (Fig. 11.42), the switch S_{1a} is turned either on if $v_{ca}>v_{\Delta 1}$ or off if $v_{ca}<v_{\Delta 1}$, and switch S_{1b} is turned either on if $v_{ca}>v_{\Delta 2}$ or off if $v_{ca}<v_{\Delta 2}$. Additionally, the switch S_{4a} status is obtained as the opposite to switch S_{1a}, and the switch S_{4b} status is obtained as the opposite to switch S_{1b}. In order to use the same set of carrier signals to generate the gating signals for phases b and c, the normalized frequency of the carrier signal m_f should be a multiple of 3. Thus, the possible values are $m_f=3,9,15,21,\ldots$.

Fig. 11.46 shows the relevant waveforms for a three-level neutral-point-clamped inverter modulated by means of an SPWM technique ($m_f=15$, $m_a=0.8$). Specifically, Fig. 11.46D shows the inverter phase voltage, which is clearly a three-level type of voltage, and Fig. 11.46F shows the load line voltage, which shows that the step voltages are at most $v_i/2$. More importantly, the inverter phase voltage (Fig. 11.46E) contains harmonics at $l\cdot m_f\pm k$ with $l=1,3,\ldots$ and $k=0,2,4,\ldots$ and at $l\cdot m_f\pm k$ with $l=2,4,\ldots$ and $k=1,3,\ldots$. For instance, the first set of harmonics ($l=1$, $m_f=15$) are at 15, 15 ± 2, $15\pm 4,\ldots$. The inverter line voltage (Fig. 11.46G) contains harmonics at $l\cdot m_f\pm k$ with $l=1,3,\ldots$ and $k=2,4,\ldots$ and at $l\cdot m_f\pm k$ with $l=2,4,\ldots$ and $k=1,3,\ldots$. For instance, the first set of harmonics in the line voltages ($l=1$, $m_f=15$) are at 15 ± 2, $15\pm 4,\ldots$.

All the other features of carrier-based PWM techniques also apply in multilevel inverters. Firstly, the fundamental component of the inverter phase voltages satisfies

$$\hat{v}_{aN1}=\hat{v}_{bN1}=\hat{v}_{cN1}=m_a\frac{v_i}{2}\quad 0<m_a\leq 1 \tag{11.58}$$

and thus, the line voltages satisfy

$$\hat{v}_{ab1}=\hat{v}_{bc1}=\hat{v}_{ca1}=m_a\sqrt{3}\frac{v_i}{2}\quad 0<m_a\leq 1 \tag{11.59}$$

where $0<m_a\leq 1$ is the linear operating region. To further increase the amplitude of the load voltages, the overmodulation operating region can be used by further increasing the modulating signal amplitudes ($m_a>1$), where the line voltages range in

$$\sqrt{3}\frac{v_i}{2}<\hat{v}_{ab1}=\hat{v}_{bc1}=\hat{v}_{ca1}<\frac{4}{\pi}\sqrt{3}\frac{v_i}{2} \tag{11.60}$$

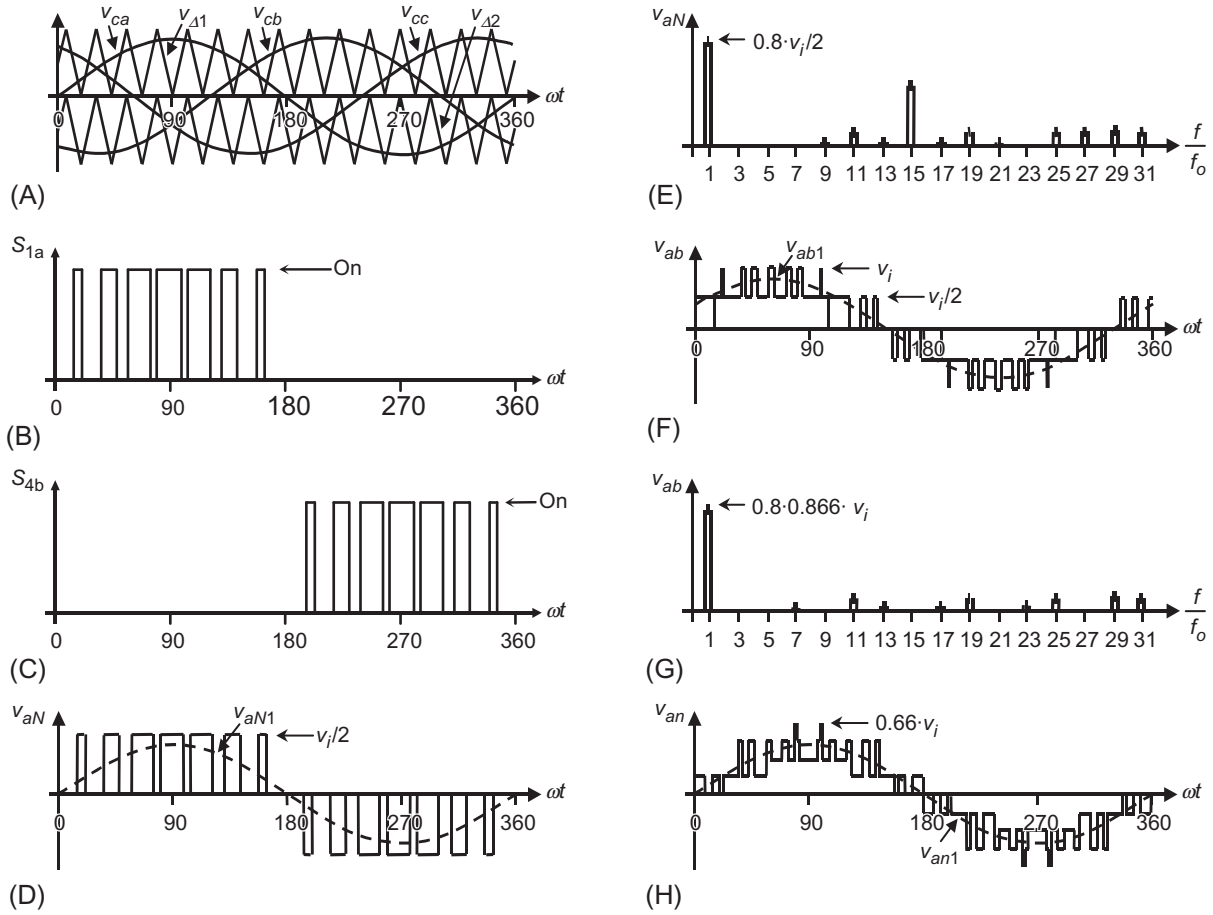


FIG. 11.46 Three-level VSI topology. Relevant waveforms using an SPWM ($m_f = 15$, $m_a = 0.8$): (A) modulating and carrier signals, (B) switch S_{1a} status, (C) switch S_{4b} status, (D) inverter phase *a* voltage, (E) inverter phase *a* voltage spectrum, (F) load line voltage, (G) load line voltage spectrum, and (H) phase-load *a* voltage.

Second, the modulating signals could be improved by adding a third harmonic (zero sequence), which will increase the linear region up to $m_a = 1.15$. This results in a maximum fundamental line-voltage component equal to v_i; as a third point, a nonsinusoidal set of modulating signals could also be used by the modulating technique. This is the case where nonsinusoidal line voltages are required as in active filter applications, and finally, because of the two quadrants operation of VSIs, the multilevel inverter could equally be used in applications where the active power flow goes from the dc to the ac side or from the ac to the dc side.

In general, for an *M*-level inverter modulated by means of a carrier-based technique, three modulating signals 120° out of phase and $M-1$ carrier signals are required. Key waveforms are shown in Fig. 11.47.

One of the drawbacks of the multilevel inverter is that the dc link capacitor voltages or inductor currents, depending on the type of inverter, should be regulated. Unfortunately, this is not a natural operating condition mainly due to the fact that the storage elements are operated in a not symmetrical manner, and therefore, they will not equally share energy.

11.5.3.2 The SPWM Technique in Three-level CSIs

As in three-level VSIs, the main objective is to generate the appropriate 12 gating signals so as to obtain fundamental inverter line currents equal to a given set of modulating signals. Specifically, the SPWM in three-level inverters uses a sinusoidal set of modulating signals (i_{ca}, i_{cb}, and i_{cc} for phases *a*, *b*, and *c*, respectively) and $N-1=2$ triangular type of carrier signals ($i_{\Delta 1}$ and $i_{\Delta 2}$) as illustrated in Fig. 11.48A and E. The best results are obtained if the carrier signals are 180° out of phase and feature an odd normalized frequency (e.g., $m_f = 15$). In order to use the same set of carrier signals to generate the gating signals for phases *b* and *c*, the normalized frequency of the carrier signal m_f should be a multiple of 3. Thus, the possible values are $m_f = 3, 9, 15, 21, \ldots$.

Fig. 11.48 shows the relevant waveforms for a three-level inverter modulated by means of an SPWM technique

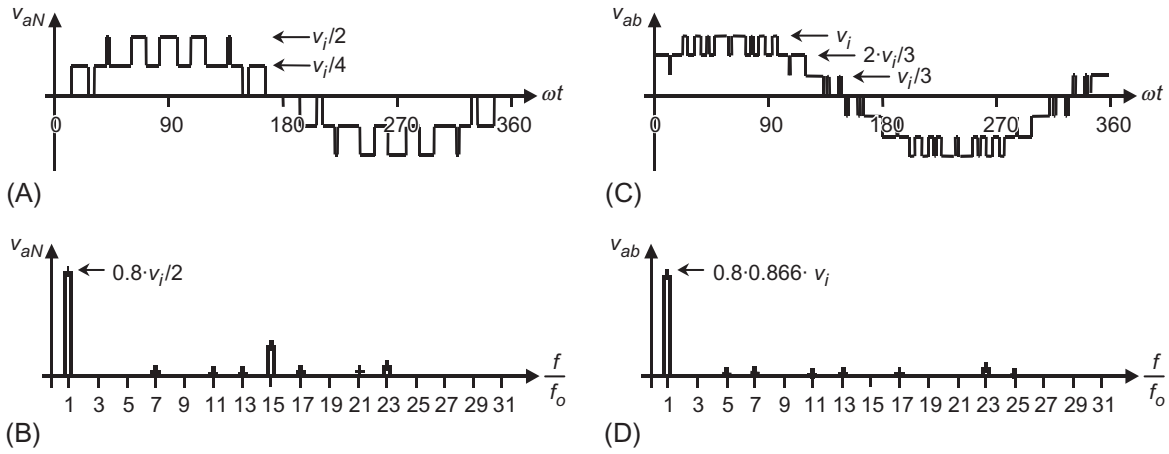


FIG. 11.47 Five-level VSI topology. Relevant waveforms using a SPWM ($m_f = 15$, $m_a = 0.8$): (A) inverter phase *a* voltage, (B) inverter phase *a* voltage spectrum, (C) load line voltage, and (D) load line voltage spectrum.

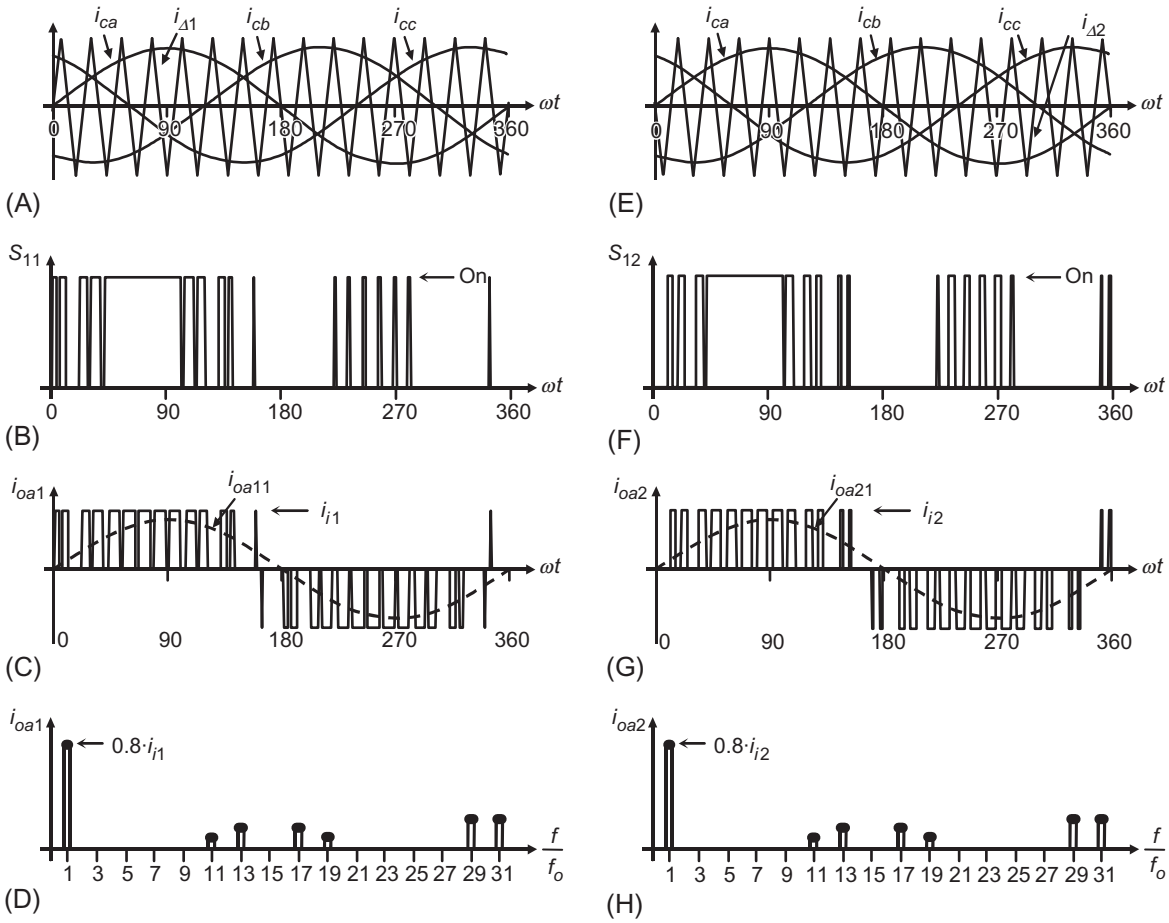


FIG. 11.48 Three-level CSI topology. Relevant waveforms using an SPWM ($m_f = 15$, $m_a = 0.8$): (A) modulating signals and carrier signal 1, (B) switch S_{11} status, (C) inverter 1 linear current, (D) inverter 1 linear current spectrum, (E) modulating signals and carrier signal 2, (F) switch S_{12} status, (G) inverter 2 linear current, and (H) inverter 2 linear current spectrum.

($m_f = 15$, $m_a = 0.8$). Specifically, Fig. 11.48B and F show the gating signals obtained as described earlier in this chapter. The inverter line currents shown in Fig. 11.48C and G feature spectra shown in Fig. 11.48D and H, respectively. As expected, the inverter line currents contain harmonics at $l \cdot m_f \pm k$ with $l = 1,3,\ldots$ and $k = 2,4,\ldots$ and at $l \cdot m_f \pm k$ with $l = 2,4,\ldots$ and $k = 1,3,\ldots$. For instance, the first set of harmonics in the line currents ($l = 1$, $m_f = 15$) are at 15 ± 2, $15 \pm 4, \ldots$.

The total inverter line current is shown in Fig. 11.49A and features the first set of unwanted harmonics around $2m_f$(Fig. 11.49B). This becomes the first advantage of using a multilevel topology as the filtering component requirements become more relaxed. All the other features of carrier-based PWM techniques also apply in current-source multilevel inverters. For instance, (I) the fundamental component of the line currents satisfies

$$\hat{i}_{oa1} = \hat{i}_{ob1} = \hat{i}_{oc1} = m_a \frac{\sqrt{3}}{2}(i_{i1} + i_{i2}) \quad 0 < m_a \leq 1 \qquad (11.61)$$

where $0 < m_a \leq 1$ is the linear operating region. Also, (II) to further increase the amplitude of the load currents, a zero-sequence signal could be injected to the modulating signals, in this case,

$$\hat{i}_{oa1} = \hat{i}_{ob1} = \hat{i}_{oc1} = m_a \frac{\sqrt{3}}{2}(i_{i1} + i_{i2}) \quad 0 < m_a \leq 2/\sqrt{3} \qquad (11.62)$$

the overmodulation operating region can be used by further increasing the modulating signal amplitudes ($m_a > 2/\sqrt{3}$), where the line currents range in

$$(i_{i1} + i_{i2}) < \hat{i}_{oa1} = \hat{i}_{ob1} = \hat{i}_{oc1} < \frac{4}{\pi}(i_{i1} + i_{i2}) \qquad (11.63)$$

Also, (III) a nonsinusoidal set of modulating signals could also be used by the modulating technique. This is the case where nonsinusoidal line currents are required as in active filter applications, and (IV) because of the two quadrants operation of CSIs, the multilevel inverter could equally be used in applications where the active power flow goes from the dc to the ac side or from the ac to the dc side. In general, for an N-level inverter modulated by means of a carrier-based technique, three modulating signals 120° out of phase and $N-1$ carrier signals are required, and the line currents in the inverters have a peak value of $i_i/(N-1)$.

One of the drawbacks of the multilevel inverter is that the dc link capacitors cannot be supplied by a single dc voltage source. This is due to the fact that the currents required by the inverter in the dc bus are not symmetrical, and therefore, the capacitors will not equally share the dc supply voltage v_i. To overcome this problem, two alternatives are developed later on.

11.5.3.3 The Space-Vector Modulation

The SV modulating technique can be applied using the same principles used in two-level inverters. However, the higher number of voltage levels increases the complexity of the practical implementation of the technique. For instance, in $M = 3$-level inverters, each leg allows $M = 3$ different switch combinations as indicated in the previous sections. Therefore, in a three-phase system, there are $M^3 = 27$ total valid switch combinations, which generate $M^3 = 27$ load line voltages that are represented by $M^3 = 27$ space vectors ($\vec{\mathbf{v}}_1, \vec{\mathbf{v}}_2, \ldots, \vec{\mathbf{v}}_{27}$) in Fig. 11.50. For instance, $\vec{\mathbf{v}}_2 = 0.5 + j0.866$ is due to the line voltages $v_{ab} = 0.5$, $v_{bc} = 0.5$, $v_{ca} = -1.0$ in per unit. Thus, although the principle of operation is the same, the SV digital algorithm will have to deal with a higher number of states M^3. Moreover, because some space vectors (e.g., $\vec{\mathbf{v}}_{13}$ and $\vec{\mathbf{v}}_{14}$ in Fig. 11.50) produce the same load voltage terminals, the algorithm will have to decide between the two based on additional criteria and that of

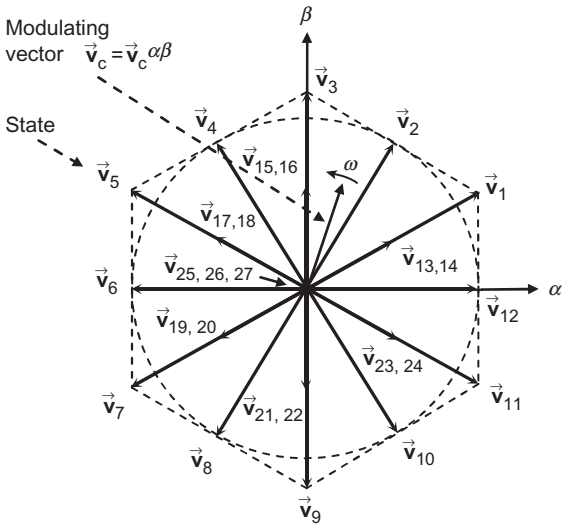


FIG. 11.50 The space-vector representation in a three-level VSI.

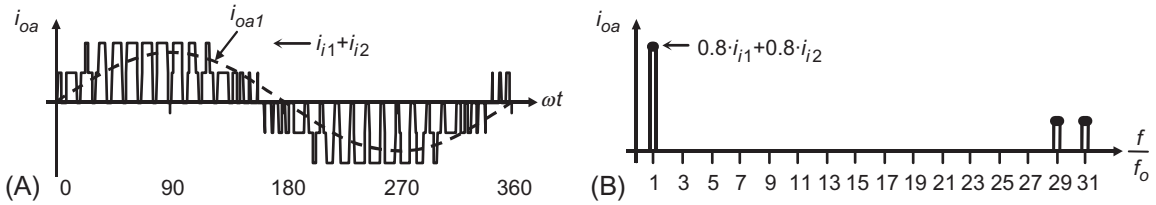


FIG. 11.49 Three-level CSI topology. Relevant waveforms using an SPWM ($m_f = 15$, $m_a = 0.8$): (A) total inverter line current and (B) total inverter line current spectrum.

the basic SV approach. Clearly, as the number of level increases, the algorithm becomes more and more elaborate. However, the benefits are not evident as the number of level increases. The maximum number of levels used in practical applications is five. This is based on a compromise between the complexity of the implementation and the benefits of the resulting waveforms.

11.5.3.4 Balancing Issues

The operation for the multilevel converter was made considering an even distribution of the voltage across the dc link capacitors or current of the inductors, depending of the type of inverter. This even distribution is not naturally achieved and could be overcome by supplying the storage elements from independent supplies or properly gating the power semiconductors of the inverter in order to minimize the unbalance.

Fig. 11.51 shows an ASD based on a three-level VSI, where the dc link capacitors are feed from two different sources. This approach is being commercially used as it ensures a robust balanced dc link voltage distribution and operates with a high-performance type of ac main current. Indeed, for an M-level inverter, $M-1$-independent dc voltage supplies are required that could be provided by $M-1$ six-pulse rectifiers feed from an $M-1$ pulse transformer. Therefore, the ac main currents are an $M-1$-level type of waveform.

This approach cannot be used when the inverter does not feature dc link voltage supplies. This is the case of static power reactive power compensators and static power active filters. In this case, the proper gating of the power semiconductors becomes the only choice to keep and balance the dc link voltages. Fig. 11.52A shows this case where the current added by the inverter i_o^{abc} provides the reactive power and current harmonics such that the ac main current i_s^{abc} features a given power factor.

The SPWM modulating technique could be used as in Fig. 11.46; however, the zero level of the carrier δ is left as a manipulable variable in Fig. 11.52B. In fact, it is used to control the difference of the upper and lower capacitor voltages $\Delta v_i = v_{i1} - v_{i2}$. A closed-loop alternative is depicted in Fig. 11.52C to manipulate δ. The modulating signals $\mathbf{v_c^{abc}}$ are left to control the reactive power and current harmonics injected into the ac mains by regulating the currents $\mathbf{i_o^{abc}}$ and

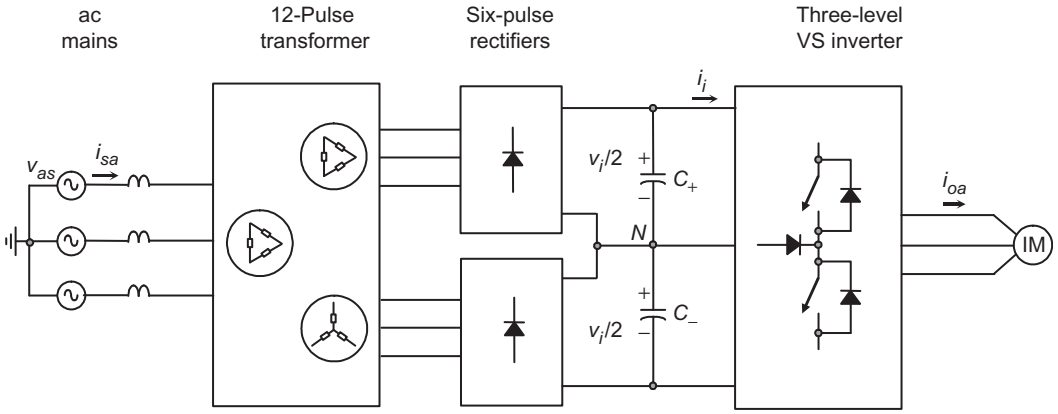


FIG. 11.51 ASD based on a three-phase three-level VSI topology.

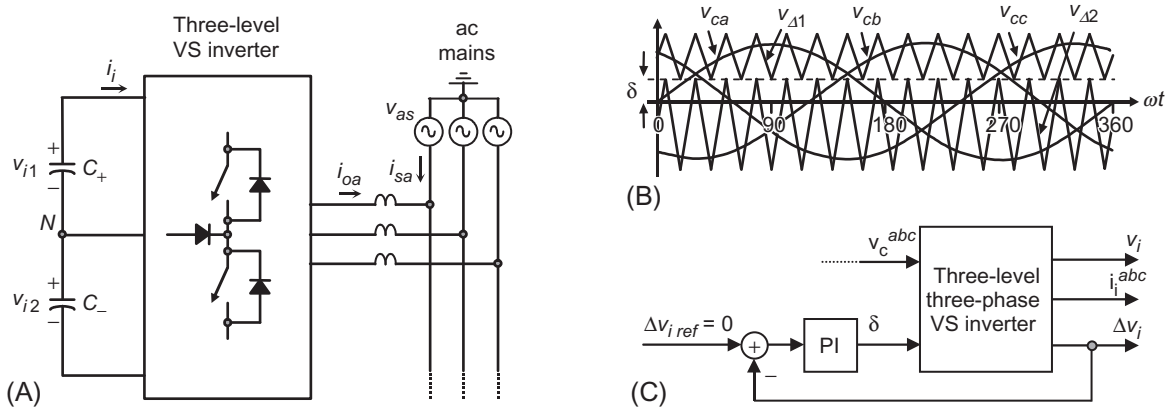


FIG. 11.52 Reactive power and current harmonics compensator based on a three-phase three-level VSI topology: (A) power topology, (B) carrier and modulating signals, and (C) δ closed-loop scheme.

keep the total dc link voltage $v_i = v_{i1} + v_{i2}$ equal to a reference. Both loops are not included in Fig. 11.52C.

11.6 Closed-Loop Operation of Inverters

In the inverter, as a classic power converter, the output depends on different conditions. For instance, in ASDs, the load usually changes, so the ac waveforms should be adjusted to these new conditions. Also, as the dc power supplies are not ideal and the dc quantities are not fixed, the inverter should compensate for such variations. Such adjustments can be done automatically by means of a closed-loop approach. Inverters also provide an alternative to changing the load operating conditions.

There are two alternatives for closed-loop operation, the feedback and the feedforward approaches. It is known that the feedback approach can compensate for both the perturbations (dc power variations) and the load variations (load torque changes). However, the feedforward strategy is more effective in mitigating perturbations as it prevents its negative effects at the load side. These cause-effect issues are analyzed in three-phase inverters in the following, although similar results are obtained for single-phase VSIs.

11.6.1 Feedforward Techniques in Voltage Source Inverters

The dc link bus voltage in VSIs is usually considered a constant-voltage source v_i. Unfortunately and due to the fact that most practical applications generate the dc bus voltage by means of a diode rectifier (Fig. 11.53), the dc bus voltage contains low-order harmonics such as the sixth, twelfth, … (due to six-pulse diode rectifiers) and the second harmonic if the ac voltage supply features an unbalance, which is usually the case. Additionally, if the three-phase load is unbalanced, as in UPS applications, the dc input current in the inverter i_i also contains the second harmonic, which in turn contributes to the generation of a second voltage harmonic in the dc bus.

The basic principle of feedforward approaches is to sense the perturbation and then modify the input in order to compensate for its effect. In this case, the dc link voltage should be sensed, and the modulating technique should accordingly be modified. The fundamental *ab* line voltage in a VSI SPWM can be written as

$$v_{ab1}(t) = \left\{ \frac{v_{ca1}(t)}{\hat{v}_\Delta} - \frac{v_{cb1}(t)}{\hat{v}_\Delta} \right\} \frac{\sqrt{3}}{2} v_i(t) \quad \hat{v}_\Delta > \hat{v}_{ca1}, \hat{v}_{cb1} \tag{11.64}$$

where $\hat{v}_\Delta$ is the carrier signal peak, $\hat{v}_{ca1}$ and $\hat{v}_{cb1}$ are the modulating signal peaks, and $v_{ca}(t)$ and $v_{cb}(t)$ are the modulating signals. If the dc bus voltage v_i varies around a nominal V_i value, then the fundamental line voltage varies proportionally; however, if the carrier signal peak $\hat{v}_\Delta$ is redefined as

$$\hat{v}_\Delta = \hat{v}_{\Delta m} \frac{v_i(t)}{V_i} \tag{11.65}$$

where $\hat{v}_{\Delta m}$ is the carrier signal peak (Fig. 11.54), then the resulting fundamental *ab* line voltage in a VSI SPWM is

$$v_{ab1}(t) = \left\{ \frac{v_{ca1}(t)}{\hat{v}_{\Delta m}} - \frac{v_{cb1}(t)}{\hat{v}_{\Delta m}} \right\} \frac{\sqrt{3}}{2} V_i \tag{11.66}$$

where, clearly, the result does not depend upon the variations of the dc bus voltage.

Fig. 11.55 shows the waveforms generated by the SPWM under a severe dc bus voltage variation (a second harmonic has been added manually to a constant V_i). As a consequence, the ac line voltage generated by the VSI is distorted as it contains low-order harmonics (Fig. 11.55E). These operating conditions may not be acceptable in standard applications such as

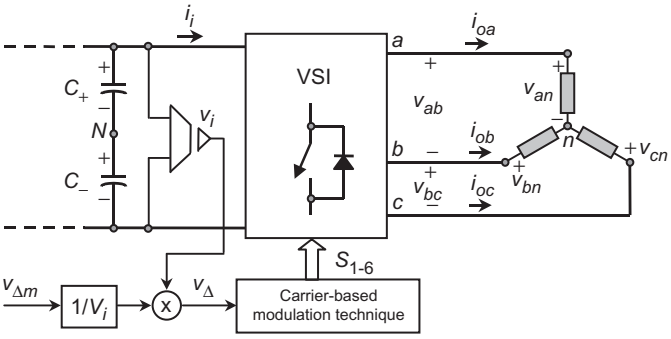


FIG. 11.54 The three-phase VSI. Feedforward control technique to reject dc bus voltage variations.

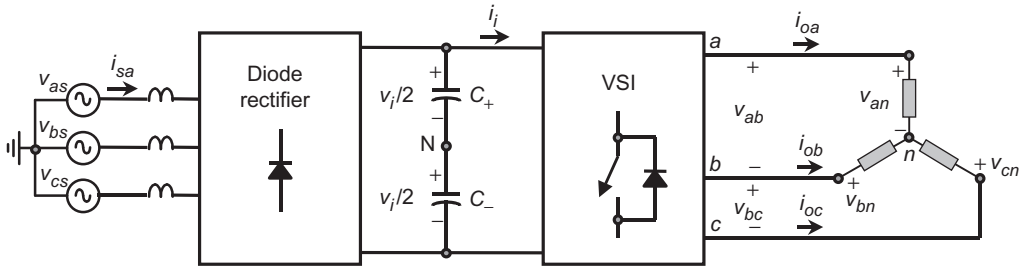


FIG. 11.53 Three-phase VSI topology with a diode-based front-end rectifier.

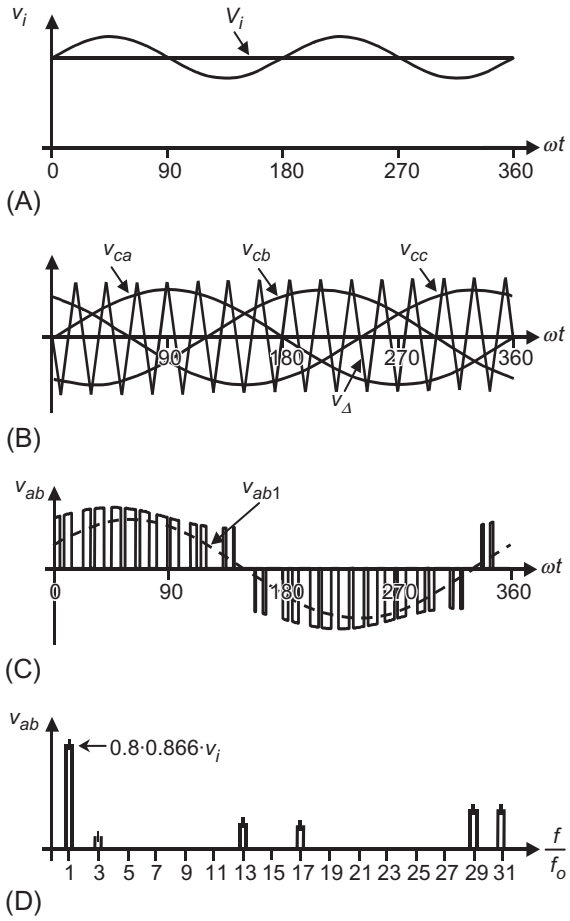


FIG. 11.55 The three-phase VSI. Waveforms for regular SPWM ($m_a = 0.8$, $m_f = 9$): (A) dc bus voltage, (B) carrier and modulating signals, (C) ac output voltage, and (D) ac output voltage spectrum.

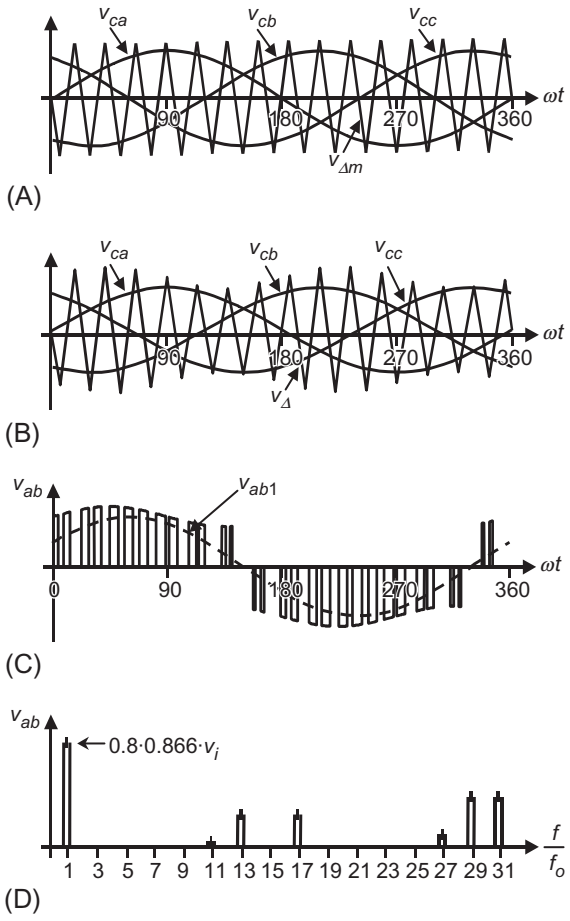


FIG. 11.56 The three-phase VSI. Waveforms for SPWM including a feedforward loop ($m_a = 0.8$, $m_f = 9$): (A) carrier and modulating signals, (B) modified carrier and modulating signals, (C) ac output voltage, and (D) ac output voltage spectrum.

ASDs because the load will draw distorted three-phase currents as well. The feedforward loop performance is illustrated in Fig. 11.56. As expected, the carrier signal is modified so as to compensate for the dc bus voltage variation (Fig. 11.56B). This is probed by the spectrum of the ac line voltage that does not contain low-order harmonics (Fig. 11.56E). It should be noted that $\hat{v}_\Delta > \hat{v}_{ca1}, \hat{v}_{cb1}$; therefore, the compensation capabilities are limited by the required ac line voltage.

The performance of the feedforward approach depends upon the frequency of the harmonics present in the dc bus voltage and the carrier signal frequency. Fortunately, the relevant unwanted harmonics to be found in the dc bus voltage are the second, due to unbalanced supply voltages, and/or the sixth as the dc bus voltage is generated by means of a six-pulse diode rectifier. Therefore, a carrier signal featuring a 15-pu frequency is found to be sufficient to properly compensate for dc bus voltage variations.

Unbalanced loads generate a dc input current i_i that contains a second harmonic, which contributes to the dc bus voltage variation. The previous feedforward approach can compensate for such perturbation and maintain balanced ac load voltages.

Digital techniques can also be modified in order to compensate for dc bus voltage variations by means of a feedforward approach.

The duality principle between the voltage- and the current-source inverters indicates that, as described previously, the feedforward approach can be also used for CSIs and for VSIs. Therefore, low-order harmonics present in the dc bus current can be compensated for before they appear at the load side. This can be done for both analog-based (e.g., carrier-based) and digital-based (e.g., space-vector) modulating techniques.

11.6.2 Feedback Techniques in Voltage Source Inverters

Unlike the feedforward advantages, the feedback techniques are more effective to regulate than the system output by gating signals of the inverters properly. Another important difference is

that feedback techniques need to sense the controlled variables. In general, the controlled variables (output to the system) are chosen according to the control objectives. For instance, in ASDs, it is usually necessary to keep the motor line currents equal to a given set of sinusoidal references. Therefore, the controlled variables become the ac line currents. There are several alternatives to implement feedback techniques in VSIs, and three of them are discussed next.

11.6.2.1 Hysteresis Current Control

The main purpose here is to force the ac line current to follow a given reference. The status of the power semiconductors are changed whenever the actual i_{oa} current goes beyond a given reference $i_{oa,ref} \pm \Delta i/2$. Fig. 11.57 shows the hysteresis current controller for one phase. Identical controllers are used in the other phases. The implementation of this controller is simple as it requires a simple comparator operating in the hysteresis mode; thus, the controller and modulator are combined in one unit.

Unfortunately, there are several drawbacks associated with the technique itself. First, the switching frequency cannot be predicted as in carrier-based modulators, and therefore, the harmonic content of the ac line voltages and currents becomes random (Fig. 11.58D). This could be a disadvantage when designing the filtering components. Second, as three-phase loads do not have the neutral connected as in ASDs, the load currents add up to zero. This means that only two ac line currents can be controlled independently at any given instant. Therefore, one of the hysteresis controllers is redundant at a given time. This explains why the load current goes beyond the limits and introduces limit cycles (Fig. 11.58A). Finally, although the ac load currents add up to zero, the controllers cannot ensure that all load line currents feature a zero dc component in one load cycle.

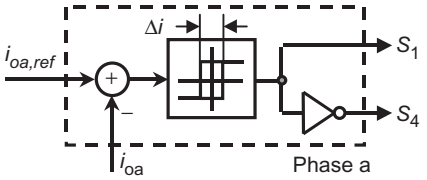


FIG. 11.57 Hysteresis current control, one phase.

11.6.2.2 Linear Control of VSIs

Proportional and proportional-integrative controllers can also be used in VSIs by employing a transformation. The main purpose is to generate the modulating signals v_{ca}, v_{cb}, and v_{cc} in a closed-loop fashion as depicted in Fig. 11.59. The modulating signals can be used by a carrier-based technique such as the

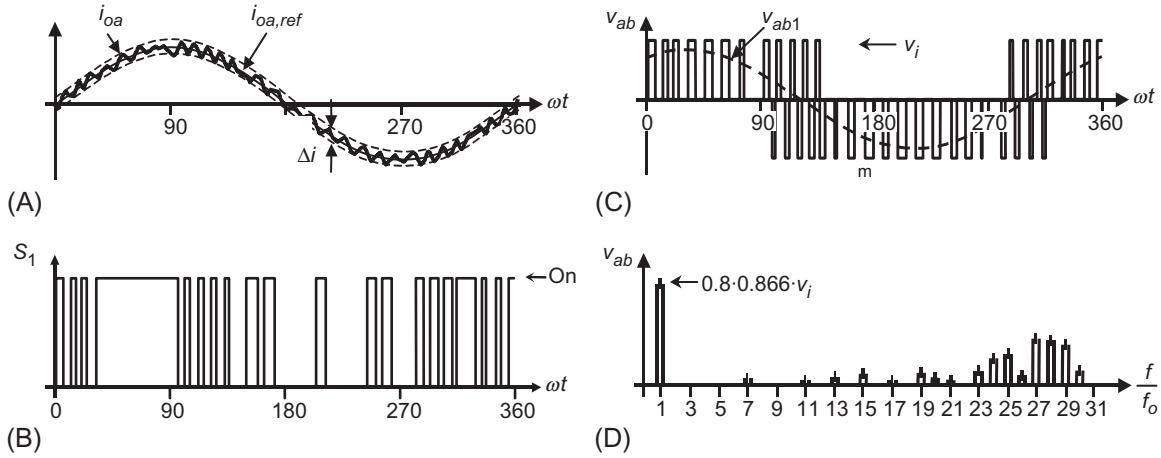


FIG. 11.58 The three-phase VSI. Ideal waveforms for hysteresis current control: (A) actual ac load current and reference, (B) switch S_1 state, (C) ac output voltage, and (D) ac output voltage spectrum.

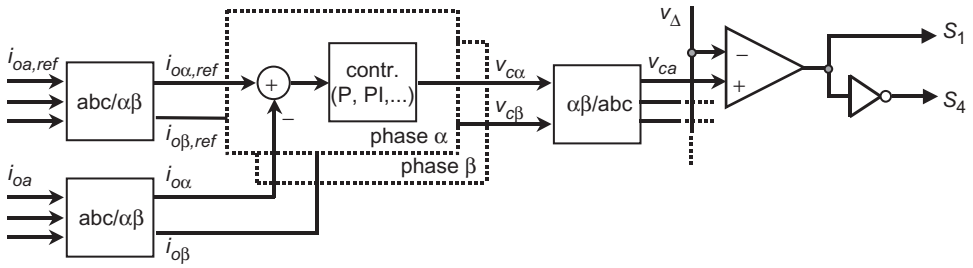


FIG. 11.59 The three-phase VSI. Feedback control based on linear controllers.

SPWM (as depicted in Fig. 11.59) or by space-vector modulation. Because the load line currents add up to zero, the load line current references must add up to zero. Thus, the abc/ αβγ transformation can be used to reduce to two controllers the overall implementation scheme as the γ component is always zero. This avoids limit cycles in the ac load currents.

The transformation of a set of variables in the stationary abc frame $\mathbf{x}^{abc}$ into a set of variables in the stationary αβ frame $\mathbf{x}^{\alpha\beta}$ is given by

$$\mathbf{x}^{\alpha\beta} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\mathbf{x}^{abc} \tag{11.67}$$

The selection of the controller (P, PI, …) is done according to the control procedures such as steady-state error, settling time, and overshoot. Fig. 11.60 shows the relevant waveforms of a VSI SPWM controlled by means of a PI controller as shown in Fig. 11.59.

Although it is difficult to prove that no limit cycles are generated, the ac line current appears very much sinusoidal. Moreover, the ac line voltage generated by the VSI preserves the characteristics of such waveforms generated by SPWM modulators.

However, an error between the actual i_{oa} and the ac line current reference $i_{oa,ref}$ can be observed (Fig. 11.60A). This error is inherent to linear controllers and cannot be totally eliminated, but it can be minimized by increasing the gain of the controller. However, the noise in the circuit is also increased, which could deteriorate the overall performance of the control scheme. The inherent presence of the error in this type of controllers is due to the fact that the controller needs a sinusoidal error to generate sinusoidal modulating signals v_{ca}, v_{cb}, and v_{cc}, as required by the modulator. Therefore, an error must exist between the actual and the ac line current references.

Nevertheless, as current-controlled VSIs are actually the inner loops in many control strategies, their inherent errors are compensated by the outer loop. This is the case of ASDs, where the outer speed loop compensates the inner current loops. In general, if the outer loop is implemented with dc quantities (such as speed), it can compensate the ac inner loops (such as ac line currents). If it is mandatory that a zero steady-state error be achieved with the ac quantities, then a stationary (abc frame) to rotating (dq frame) transformation is a valid alternative to use.

11.6.2.3 Linear Control of VSIs in a Rotating Frame

The rotating dq transformation allows ac three-phase circuits to be operated as if they were dc circuits. This is based upon a mathematical operation, that is, the transformation of a set of variables in the stationary abc frame $\mathbf{x}^{abc}$ into a set of variables in the rotating dq0 frame $\mathbf{x}^{dq0}$. The transformation is given by

$$\mathbf{x}^{dq} = \frac{2}{3}\begin{bmatrix} \sin(\omega t) & \sin(\omega t - 2\pi/3) & \sin(\omega t - 4\pi/3) \\ \cos(\omega t) & \cos(\omega t - 2\pi/3) & \cos(\omega t - 4\pi/3) \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix}\mathbf{x}^{abc} \tag{11.68}$$

where ω is the angular frequency of the ac quantities. For instance, the current vector given by

$$\mathbf{i}^{abc} = \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} I\sin(\omega t - \varphi) \\ I\sin(\omega t - 2\pi/3 - \varphi) \\ I\sin(\omega t - 4\pi/3 - \varphi) \end{bmatrix} \tag{11.69}$$

becomes the vector

$$\mathbf{i}^{dq0} = \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \begin{bmatrix} I\cos(\varphi) \\ -I\sin(\varphi) \\ 0 \end{bmatrix} \tag{11.70}$$

where I and φ are the amplitude and phase of the line currents, respectively. It can be observed that (a) the zero-component i_0 is always zero as the three-phase quantities add up to zero and

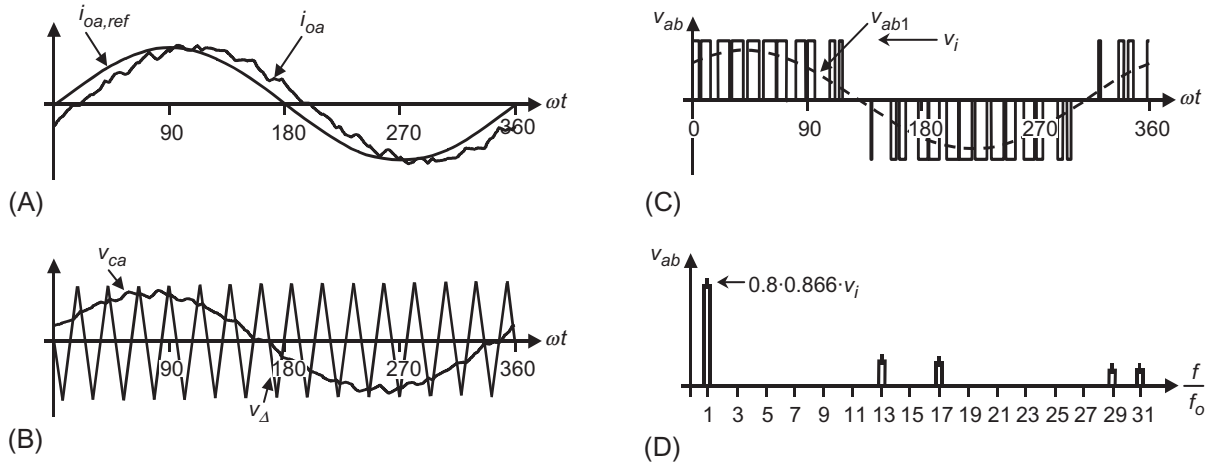


FIG. 11.60 The three-phase VSI. Ideal waveforms for a PI controller in a feedback loop ($m_a = 0.8$, $m_f = 15$): (A) actual ac load current and reference, (B) carrier and modulating signals, (C) ac output voltage, and (D) ac output voltage spectrum.

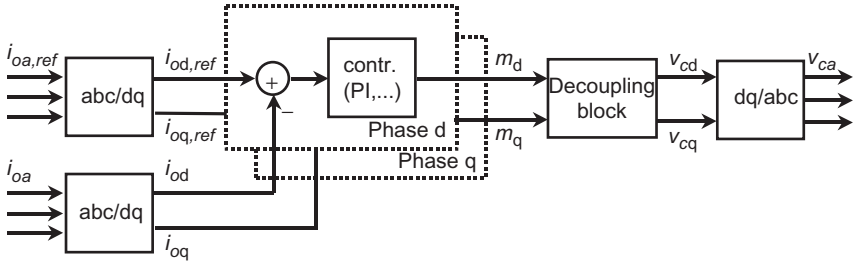


FIG. 11.61 The three-phase VSI. Feedback control based on dq0 transformation.

(b) the d and q components i_d, i_q are dc quantities. Thus, linear controllers should help to achieve zero steady-state error. The control strategy shown in Fig. 11.61 is an alternative where the zero-component controller has been eliminated due to the fact that the line currents at the load side add up to zero.

The controllers in Fig. 11.61 include an integrator that generates the appropriate dc outputs m_d and m_q even if the actual and the line current references are identical. This ensures that the zero steady-state error is achieved. The decoupling block in Fig. 11.61 is used to eliminate the cross coupling effect generated by the dq0 transformation and to allow an easier design of the parameters of the controllers.

The dq0 transformation requires the intensive use of multiplications and trigonometric functions. These operations can readily be done by means of digital microprocessors. Also, analog implementations would indeed be involved.

11.6.3 Feedback Techniques in Current Source Inverters

Duality indicates that CSIs should be controlled as equally as VSIs except that the voltages become currents and the currents become voltages. Thus, hysteresis, linear, and dq linear-based control strategies are also applicable to CSIs; however, the controlled variables are the load voltages instead of the load line currents.

For instance, the linear control of a CSI based on a dq transformation is depicted in Fig. 11.62. In this case, a passive balanced load is considered. In order to show that zero steady-state error is achieved, the per phase equations of the converter are written as

$$C\frac{d}{dt}\mathbf{v}_\mathbf{p}^{\mathbf{abc}} = \mathbf{i}_\mathbf{o}^{\mathbf{abc}} - \mathbf{i}_\mathbf{l}^{\mathbf{abc}} \tag{11.71}$$

$$L\frac{d}{dt}\mathbf{i}_\mathbf{l}^{\mathbf{abc}} = \mathbf{v}_\mathbf{p}^{\mathbf{abc}} - R\mathbf{i}_\mathbf{l}^{\mathbf{abc}} \tag{11.72}$$

The ac line currents are in fact imposed by the modulator, and they satisfy

$$\mathbf{i}_\mathbf{o}^{\mathbf{abc}} = i_i\mathbf{i}_\mathbf{c}^{\mathbf{abc}} \tag{11.73}$$

Replacing Eq. (11.73) into the model of the converter Eqs. (11.71) and (11.72), using the dq0 transformation and assuming null zero component, the model of the converter becomes

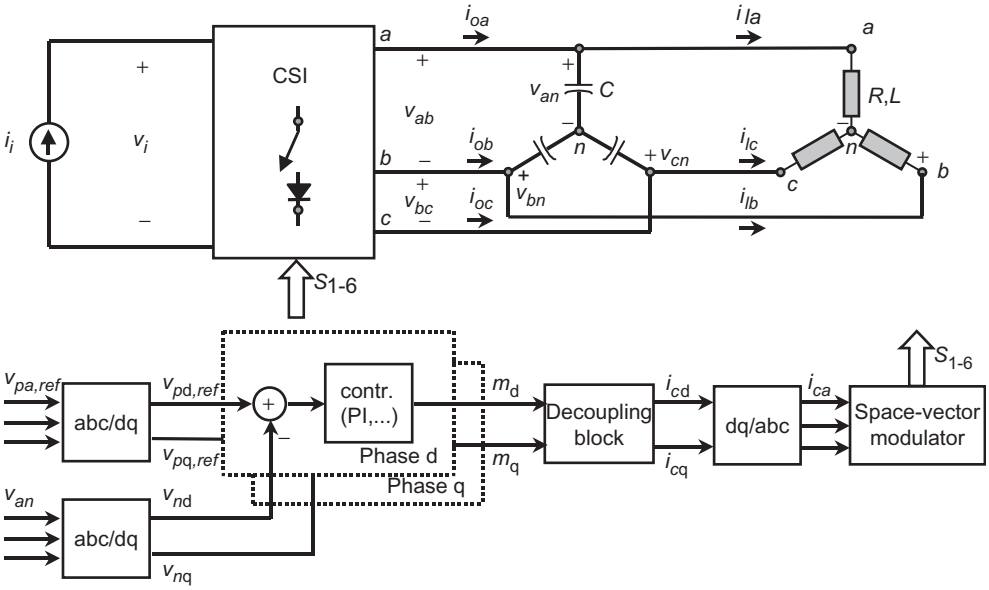


FIG. 11.62 The three-phase CSI. Feedback control based on dq0 transformation.

$$\frac{d}{dt}\mathbf{v}_{\mathbf{p}}^{\mathrm{dq}} = -\mathbf{W}\mathbf{v}_{\mathbf{p}}^{\mathrm{dq}} + \frac{i_i}{C}\mathbf{i}_{\mathbf{c}}^{\mathrm{dq}} - \frac{1}{C}\mathbf{i}_{\mathrm{l}}^{\mathrm{dq}} \tag{11.74}$$

$$\frac{d}{dt}\mathbf{i}_{\mathrm{l}}^{\mathrm{dq}} = -\mathbf{W}\mathbf{i}_{\mathrm{l}}^{\mathrm{dq}} + \frac{1}{L}\mathbf{v}_{\mathbf{p}}^{\mathrm{dq}} - \frac{R}{L}\mathbf{i}_{\mathrm{l}}^{\mathrm{dq}} \tag{11.75}$$

where $\mathbf{W}$ is given by

$$\mathbf{W} = \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix} \tag{11.76}$$

A first approximation is to assume that the decoupling block is not there; in other words, $\mathbf{i}_{\mathbf{c}}^{\mathrm{dq}} = \mathbf{m}^{\mathrm{dq}}$. On the other hand, the model of the controllers can be written as

$$\mathbf{m}^{\mathrm{dq}} = k\left\{\mathbf{v}_{\mathbf{p,ref}}^{\mathrm{dq}} - \mathbf{v}_{\mathbf{p}}^{\mathrm{dq}}\right\} + \frac{1}{T}\int_{-\infty}^{t}\left(\mathbf{v}_{\mathbf{p,ref}}^{\mathrm{dq}} - \mathbf{v}_{\mathbf{p}}^{\mathrm{dq}}\right)dt \tag{11.77}$$

where k and T are the proportional and integrative gains of the PI controller that are chosen to achieve a desired dynamic response. Combining the model of the controllers and the model of the converter in dq coordinates and using the Laplace transform, the following relationship between the reference and actual phase-load voltages is found:

$$\begin{aligned}\mathbf{v}_{\mathbf{p}}^{\mathrm{dq}} = {} & \frac{i_i}{C}\left\{sk + \frac{1}{T}\right\}\left\{s\mathbf{I} + \mathbf{W} + \frac{R}{L}\mathbf{I}\right\}\times \\ & \left[\left\{s\mathbf{I} + \mathbf{W} + \frac{R}{L}\mathbf{I}\right\}\left\{s^2\mathbf{I} + s\left(\mathbf{W} + \frac{i_i}{C}k\mathbf{I}\right) + \frac{i_i}{CT}\mathbf{I}\right\}\right. \\ & \left. + \frac{s}{LC}\mathbf{I}\right]^{-1}\mathbf{v}_{\mathbf{p,ref}}^{\mathrm{dq}}\end{aligned} \tag{11.78}$$

Finally, in order to prove that the zero steady-state error is achieved for step inputs in either the d or q component of the phase-load voltage reference, the previous expression is evaluated in $s = 0$. This results in the following:

$$\begin{aligned}\mathbf{v}_{\mathbf{p}}^{\mathrm{dq}} = {} & \frac{i_i}{C}\left\{\frac{1}{T}\right\}\left\{\mathbf{W} + \frac{R}{L}\mathbf{I}\right\}\left[\left\{W + \frac{R}{L}\mathbf{I}\right\}\left\{\frac{i_i}{CT}\mathbf{I}\right\}\right]^{-1}\mathbf{v}_{\mathbf{p,ref}}^{\mathrm{dq}} \\ = {} & \mathbf{v}_{\mathbf{p,ref}}^{\mathrm{dq}}\end{aligned} \tag{11.79}$$

As expected, the actual and reference values are identical. Finally, the relationship in Eq. (11.78) is a matrix that is not diagonal. This means that both the actual and the reference phase-load voltages are coupled. In order to obtain a decoupled control, the decoupling block in Fig. 11.62 should be properly chosen.

11.7 Regeneration in Inverters

Industrial applications are usually characterized by a power flow that goes from the ac distribution system to the load. This is, for example, the case of an ASD operating in the motoring mode. In this instance, the active power flows from the dc side to the ac side of the inverter. However, there are an important number of applications in which the load may supply power to the system. Moreover, this could be an occasional condition and a normal operating condition. This is known as the regenerative operating mode. For example, when an ASD reduces the speed of an electric machine, this can be considered a transient condition. Downhill belt conveyors in mining applications can be considered as a normal operating condition. In order to simplify the notation, it could be said that an inverter operates in the motoring mode when the power flows from the dc to the ac side and in the regenerative mode when the power flows from the ac to the dc side.

11.7.1 Motoring Operating Mode in Three-phase VSIs

This is the case where the power flows from the dc side to the ac side of the inverter. Fig. 11.63 shows a simplified scheme of an ASD where the motor has been modeled by three *RLe* branches, where the sources $\mathbf{e}^{\mathrm{abc}}$ are the back emf. Because the ac line voltages applied by the inverter are imposed by the pulse width modulation technique being used, they can be adjusted according to specific requirements. In particular, Fig. 11.64 shows the relevant waveforms in a steady state for the motoring operating mode of the ASD. To simplify the analysis, a constant dc bus voltage $v_i = V_i$ has been considered.

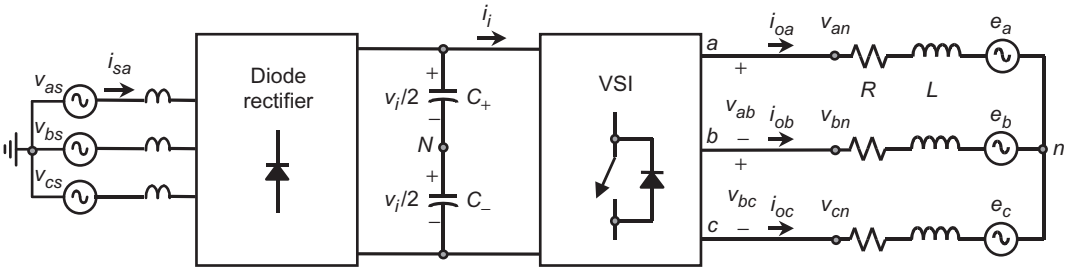


FIG. 11.63 Three-phase VSI topology with a diode-based front-end rectifier.

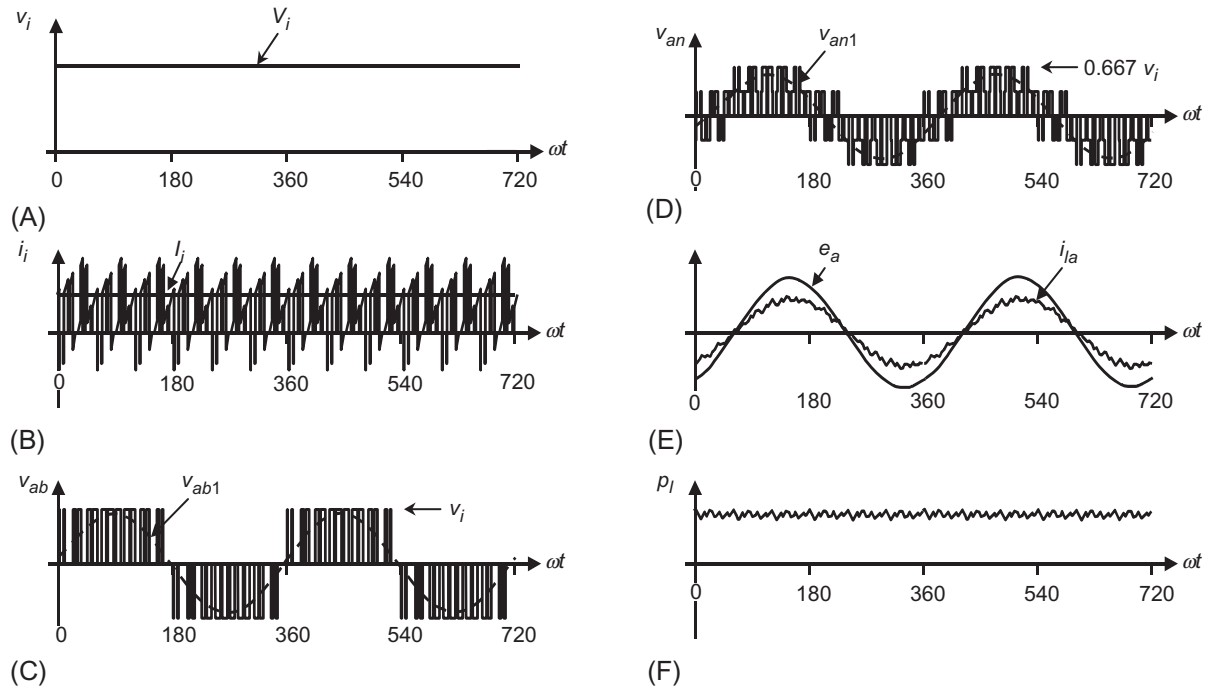


FIG. 11.64 The ASD based on a VSI. Motoring mode: (A) dc bus voltage, (B) dc bus current, (C) ac line-load voltage, (D) ac phase-load voltage, (E) motor line current and back emf, and (F) shaft power.

It can be observed that (i) the dc bus current i_i features a dc value I_i that is positive and (ii) the motor line current is in phase with the back emf. Both features confirm that the active power flows from the dc source to the motor. This is also confirmed by the shaft power plot (Fig. 11.64F), which is obtained as

$$p_l(t) = e_a(t)i_{la}(t) + e_b(t)i_{lb}(t) + e_c(t)i_{lc}(t) \tag{11.80}$$

11.7.2 Regenerative Operating Mode in Three-phase VSIs

The back emf sources $\mathbf{e}^{abc}$ are functions of the machine speed, and as such, they ideally change just as the speed changes. The regeneration operating mode can be achieved by properly modifying the ac line voltages applied to the machine. This is done by the speed outer loop that could be based on a scalar (e.g., V/f) or vectorial (e.g., field-oriented) control strategy. As indicated earlier, there are two cases of regenerative operating modes.

11.7.2.1 Occasional Regenerative Operating Mode

This mode is required during transient conditions such as in occasional braking of electric machines (ASDs). Specifically, the speed needs to be reduced, and the kinetic energy is taken into the dc bus. Because the motor line voltage is imposed by the VSI, the speed reduction should be done in such a way that the motor line currents do not exceed the maximum values. This boundary condition will limit the ramp-down speed to a minimum, but shorter braking times will require a mechanical braking system.

Fig. 11.65 shows a transition from the motoring to regenerative operating mode for an ASD as shown in Fig. 11.63. Here, a stiff dc bus voltage has been used. Zone I in Fig. 11.65 is the motoring mode, zone II is a transition condition, and zone III is the regeneration mode. The line voltage is adjusted dynamically to obtain nominal motor line currents during regeneration (Fig. 11.65D). Zone III clearly shows that the shaft power gets reversed.

Occasional regeneration means that the drive rarely goes into this operating mode. Therefore, such energy can be (a) left uncontrolled or (b) burned in resistors that are paralleled to the dc bus. The first option is used in low- to medium-power applications that use diode-based front-end rectifiers. Therefore, the dc bus current flows into the dc bus capacitor, and the dc bus voltage rises accordingly to

$$\Delta v_i = \frac{1}{C} I_i \Delta t \tag{11.81}$$

where Δv_i is the dc bus voltage variation, C is the dc bus voltage capacitor, I_i is the average dc bus current during regeneration, and Δt is the duration of the regeneration operating mode. Usually, the drives have the capacitor C designed to allow a 10% overvoltage in the dc bus.

The second option uses burning resistors R_R that are paralleled in the dc bus as shown in Fig. 11.66 by means of the switch

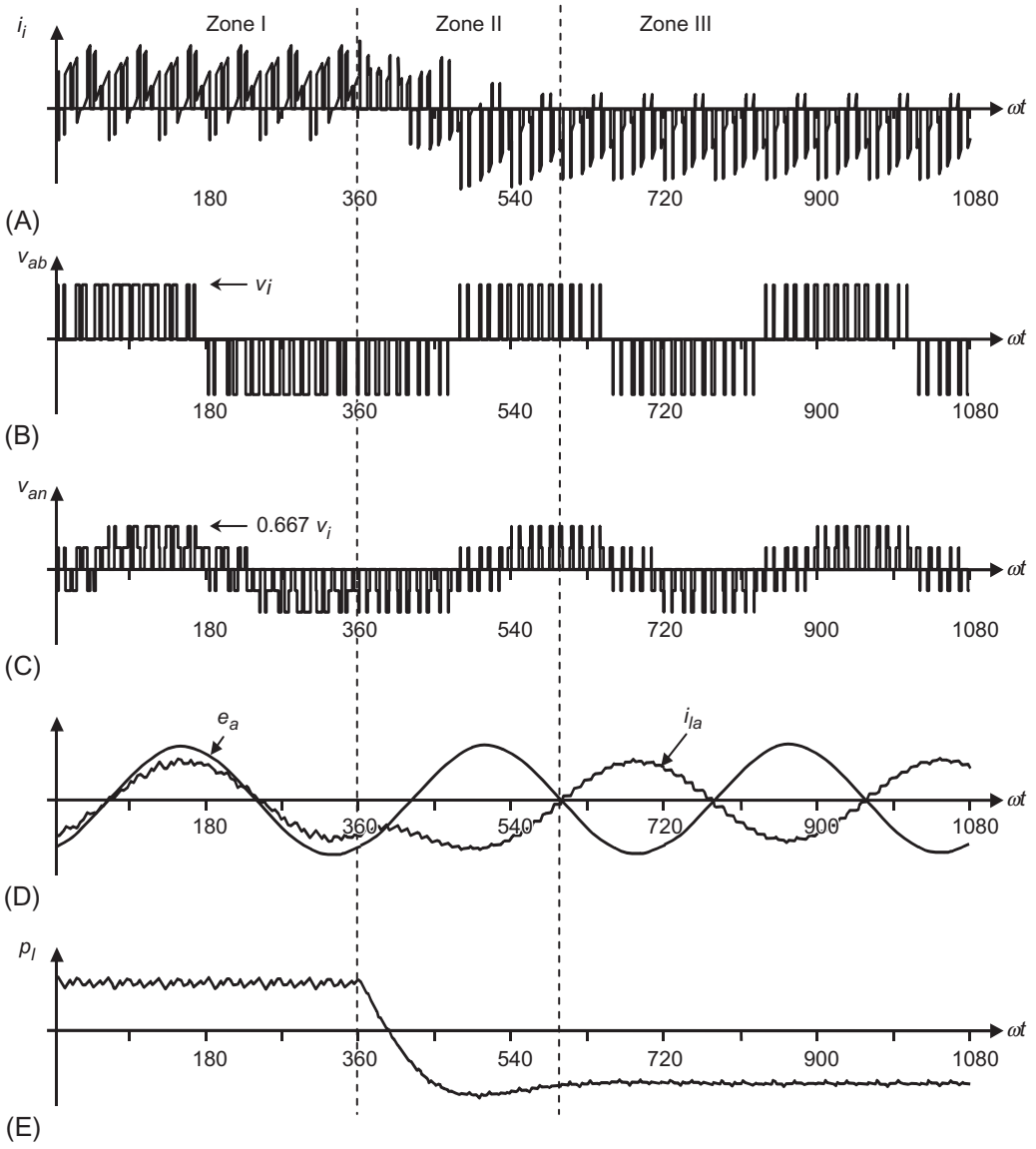


FIG. 11.65 The ASD based on a VSI. Motoring to regenerative operating mode transition: (A) dc bus current, (B) ac line motor voltage, (C) ac phase motor voltage, (D) motor line current and back emf, and (E) shaft power.

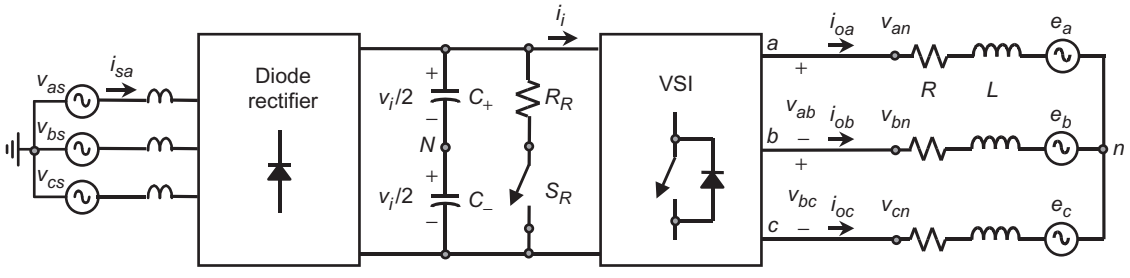


FIG. 11.66 The ASD based on a VSI. Burning resistor strategy.

S_R. A closed-loop strategy based on the actual dc bus voltage modifies the duty cycle of the turn-on/turnoff of the switch S_R in order to keep such voltage under a given reference. This alternative is used when the energy recovered by the VSI would result in an acceptable dc bus voltage variation if an uncontrolled alternative is used.

There are some special cases where the regeneration operating mode is frequently used. For instance, electric shovels in mining companies have repetitive working cycles, and $\asymp 15\%$ of the energy is sent back into the dc bus. In this case, a valid alternative is to send back the energy into the ac distribution system.

The schematic shown in Fig. 11.67 is capable of taking the kinetic energy and sending it into the ac grid. As reviewed earlier, the regeneration operating mode reverses the polarity of the dc current i_i, and because the diode-based front-end converter cannot take negative currents, a thyristor-based front-end converter is added. Similarly to the burning resistor approach, a closed-loop strategy based on the actual dc bus voltage v_i modifies the commutation angle α of the thyristor rectifier in order to keep such voltage under a given reference.

11.7.2.2 Regenerative Operating Mode as Normal operating Mode

Fewer industrial applications are capable of returning energy into the ac distribution system on a continuous basis. For instance, mining companies usually transport their product downhill for a few kilometers before processing it. In such cases, the drive maintains the transportation belt conveyor at constant speed and takes the kinetic energy. Due to the large amount of energy and the continuous operating mode, the drive should be capable of taking the kinetic energy, transforming it into electric energy, and sending it into the ac distribution system. This would make the drive a generator that would compensate for the active power required by other loads connected to the electric grid.

The schematic shown in Fig. 11.68 is a modern alternative for adding regeneration capabilities to the VSI-based drive on a continuous basis. In contrast to the previous alternatives, this scheme uses a VSI topology as an active front-end converter, which is generally called voltage-source rectifier (VSR). The VSR operates in two quadrants, that is, positive dc voltages and positive/negative dc currents as reviewed earlier. This feature makes it a perfect match for ASDs based on a

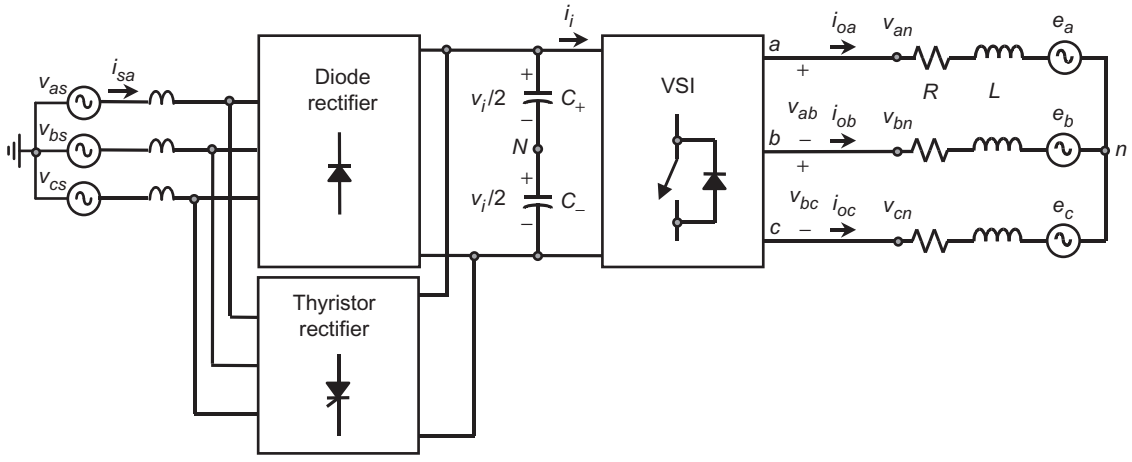


FIG. 11.67 The ASD based on a VSI. Diode-thyristor-based front-end rectifier with regeneration capabilities.

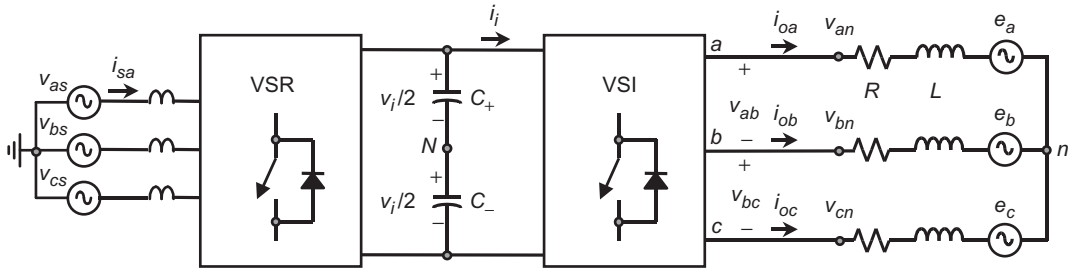


FIG. 11.68 The ASD based on a VSI. Active front-end rectifier with regeneration capabilities.

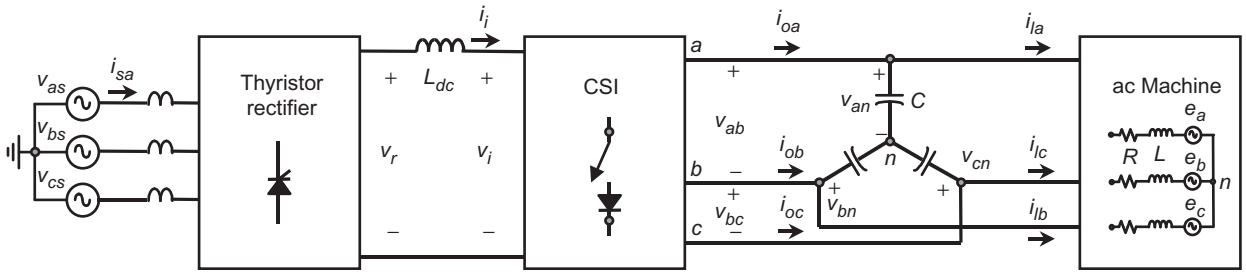


FIG. 11.69 The ASD based on a CSI. Thyristor-based rectifier.

VSI. Some of the advantages of using a VSR topology are the following: (i) The ac supply current can be as sinusoidal as required (by increasing the switching frequency of the VSR or the ac line inductance), (ii) the operation can be done at a unity displacement power factor in both motoring and regenerative operating modes, and (iii) the control of the VSR is done in both motoring and regenerative operating modes by a single dc bus voltage loop.

11.7.3 Regenerative Operating Mode in Three-phase CSIs

There are drives where the motor side converter is a CSI. This is usually the case where near sinusoidal motor voltages are needed instead of the PWM type of waveform generated by VSIs. This is normally the case for medium-voltage applications. Such inverters require a dc current source that is constructed by means of a controlled rectifier.

Fig. 11.69 shows a CSI-based ASD where the dc current source is generated by means of a thyristor-based rectifier in combination with a dc link inductor L_{dc}. In order to maintain a constant dc link current $i_i = I_i$, the thyristor-based rectifier adjusts the commutation angle α by means of a closed-loop control strategy. Assuming a constant dc link current, the regenerating operating mode is achieved when the dc link voltage v_i reverses its polarity. This can be done by modifying the PWM pattern applied to the CSI as in the VSI-based drive. To maintain the dc link current constant, the thyristor-based rectifier also reverses its dc link voltage v_r. Fortunately, the thyristor rectifier operates in two quadrants, that is, positive dc link currents and positive/negative dc link voltages. Thus, no additional equipment is required to include regeneration capabilities in CSI-based drives.

Similarly, an active front-end rectifier could be used to improve the overall performance of the thyristor-based rectifier. A PWM current-source rectifier (CSR) could replace the thyristor-based rectifier with the following added advantages: (i) The ac supply current can be as sinusoidal as required (e.g., by increasing the switching frequency of the CSR), (ii) the operation can be done at a unity displacement power factor in both motoring and regenerative operating modes, and (iii) the control of the CSR is done in both motoring and regenerative operating modes by a single dc bus current loop.

Further Reading

Inverters Applications

[1] Chih-Yi Huang, Chao-Peng Wei, Jung-Tai Yu, Yeu-Jent Hu, Torque and current control of induction motor drives for inverter switching frequency reduction, IEEE Trans. Ind. Electron. 52 (5) (2005) 1364–1371.
[2] Chih-Yi Huang, Chao-Peng Wei, Jung-Tai Yu, Yeu-Jent Hu, Torque and current control of induction motor drives for inverter switching frequency reduction, IEEE Trans. Ind. Electron. 52 (5) (2005) 1364–1371.
[3] J. Espinoza, L. Morán, J. Guzmán, Multi-level three-phase current source inverter based AC drive for high performance applications, Conf. Rec. PESC'05, Recife, Brazil, June 2005.
[4] G. Joós, J. Espinoza, Three phase series var compensation based on a voltage controlled current source inverter with supplemental modulation index control, IEEE Trans. Power Electron. 15 (3) (1999) 587–598.
[5] P. Jain, J. Espinoza, H. Jin, Performance of a single-stage UPS system for single-phase trapezoidal-shaped ac voltage supplies, IEEE Trans. Power Electron. 13 (5) (1998) 912–923.
[6] H. Akagi, The state-of-the-art of power electronics in Japan, IEEE Trans. Power Electron. 13 (2) (1998) 345–356.
[7] T. Wu, T. Yu, Off-line applications with single-stage converters, IEEE Trans. Ind. Appl. 44 (5) (1997) 638–647.
[8] T. Wu, T. Yu, Off-line applications with single-stage converters, IEEE Trans. Ind. Appl. 44 (5) (1997) 638–647.
[9] J. Espinoza, G. Joós, A current source inverter induction motor drive system with reduced losses, IEEE Trans. Ind. Appl. 34 (4) (1998) 796–805.
[10] M. Ryan, W. Brumsickle, R. Lorenz, Control topology options for single-phase UPS inverters, IEEE Trans. Ind. Appl. 33 (2) (1997) 493–501.
[11] A. Jungreis, A. Kelly, Adjustable speed drive for residential applications, IEEE Trans. Ind. Appl. 31 (6) (1995) 1315–1322.
[12] K. Rajashekara, History of electrical vehicles in General Motors, IEEE Trans. Ind. Appl. 30 (4) (1994) 897–904.
[13] B. Bose, Power electronics and motion control – Technology status and recent trends, IEEE Trans. Ind. Appl. 29 (5) (1993) 902–909.
[14] S. Bhowmik, R. Spée, A guide to the application-oriented selection of ac/ac converter topologies, IEEE Trans. Power Electron. 8 (2) (1993) 156–163.

Current Source Inverters

[15] J. Espinoza, L. Morán, N. Zargari, Multi-level three-phase current source inverter based series voltage compensator, Conf. Rec. PESC'05, Recife, Brazil, June 2005.

[16] M. Pande, H. Jin, G. Joós, Modulated integral control technique for compensating switch delays and nonideal dc buses in voltage-source inverters, IEEE Trans. Ind. Electron. 44 (2) (1997) 182–190.
[17] J. Espinoza, G. Joós, Current-source converter on-line pattern generator switching frequency minimization, IEEE Trans. Ind. Appl. 44 (2) (1997) 198–206.
[18] G. Joós, G. Moschopoulos, P. Ziogas, A high performance current source inverter, IEEE Trans. Power Electron. 8 (4) (1993) 571–579.
[19] Poh Chiang Loh, D.G. Holmes, Analysis of multiloop control strategies for LC/CL/LCL-filtered voltage-source and current-source inverters, IEEE Trans. Ind. Appl. 41 (2) (2005) 644–654.
[20] M. Salo, H. Tuusa, Vector-controlled PWM current-source-inverter-fed induction motor drive with a new stator current control method, IEEE Trans. Ind. Electron. 52 (2) (2005) 523–531.
[21] Shen Dong, P.W. Lehn, Modeling, analysis, and control of a current source inverter-based STATCOM, IEEE Trans. Power Delivery 17 (1) (2002) 248–253.
[22] A. Bendre, I. Wallace, J. Nord, G. Venkataramanan, A current source PWM inverter with actively commutated SCRs, IEEE Trans. Power Electron. 17 (4) (2002) 461–468.
[23] B.M. Han, S.I. Moon, Static reactive-power compensator using soft-switching current-source inverter, IEEE Trans. Ind. Electron. 48 (6) (2001) 1158–1165.
[24] D.N. Zmood, D.G. Holmes, Improved voltage regulation for current-source inverters, IEEE Trans. Ind. Appl. 37 (4) (2001) 1028–1036.

Impedance Source Inverters

[25] Fang Zheng Peng, Z-Source Inverter, IEEE Trans. Ind. Appl. 39 (2) (2003) 504–510.
[26] F.Z. Peng, X. Yuan, X. Fang, Z. Qian, Z-source inverter for adjustable speed drives, IEEE Power Electron. Lett. 1 (2) (2003) 33–35.
[27] N. Vázquez, E. Baeza, A. Perea, C. Hernández, E. Vázquez, H. López, 'Z' and 'qZ' Source Inverters as Electronic Ballast, IEEE Trans. Power Electron. 31 (11) (2016) 7651–7660.
[28] Y.P. Siwakoti, P.C. Loh, F. Blaabjerg, G.E. Town, Y-Source Impedance Network, IEEE Trans. Power Electron. 29 (7) (2014) 3250–3254.
[29] C. Xia, X. Li, Z-source inverter-based approach to the zero-crossing point detection of back EMF for sensorless brushless DC motor, IEEE Trans. Power Electron. 30 (3) (2015) 1488–1498.
[30] V. Fernao Pires, A. Cordeiro, D. Foito, J.F. Martins, Quasi-Z-source inverter with a T-type converter in normal and failure moden, IEEE Trans. Power Electron. 31 (11) (2016) 7462–7470.
[31] K. Beer, B. Piepenbreier, Properties and Advantages of the Quasi-Z-Source Inverter for DC-AC Conversion for Electric Vehicle Applications, in: Anti-Counterfeiting, Security and Identification (ASID), 2012 International Conference on, 2010, pp. 1–6.
[32] L. Yuan, Z. Peng, AC Small Signal Modeling, Analysis and Control of Quasi-Z-Source Converter, in: Power Electronics and Motion Control Conference (IPEMC), 2012 7th International, 2012, pp. 1848–1854.

Modulating Techniques and Control Strategies

[33] J. Espinoza, G. Joós, DSP implementation of output voltage reconstruction in CSI based converters, IEEE Trans. Ind. Electron. 45 (6) (1998) 895–904.
[34] M. Kazmierkowski, L. Malesani, Current control techniques for three-phase voltage-source PWM converters: A survey, IEEE Trans. Ind. Electron. 45 (5) (1998) 691–703.
[35] A. Tilli, A. Tonielli, Sequential design of hysteresis current controller for three-phase inverter, IEEE Trans. Ind. Electron. 45 (5) (1998) 771–781.
[36] D. Chung, J. Kim, S. Sul, Unified voltage modulation technique for real-time three-phase power conversion, IEEE Trans. Ind. Appl. 34 (2) (1998) 374–380.
[37] L. Malesani, P. Mattavelli, P. Tomasin, Improved constant-frequency hysteresis current control of VSI inverters with simple feed-forward bandwidth prediction, IEEE Trans. Ind. Appl. 33 (5) (1997) 1194–1202.
[38] M. Rahman, T. Radwin, A. Osheiba, A. Lashine, Analysis of current controllers for voltage-source inverter, IEEE Trans. Ind. Electron. 44 (4) (1997) 477–485.
[39] A. Trzynadlowski, R. Kirlin, S. Legowski, Space vector PWM technique with minimum switching losses and a variable pulse rate, IEEE Trans. Ind. Electron. 44 (2) (1997) 173–181.
[40] S. Tadakuma, S. Tanaka, H. Naitoh, K. Shimane, Improvement of robustness of vector-controlled induction motors using feedforward and feedback control, IEEE Trans. Power Electron. 12 (2) (1997) 221–227.
[41] J. Holtz, B. Beyer, Fast current trajectory tracking control based on synchronous optimal pulse width modulation, IEEE Trans. Ind. Appl. 31 (5) (1995) 1110–1120.
[42] J. Espinoza, G. Joós, P. Ziogas, Voltage controlled current source inverters, in: Conf. Rec. IECON'92, San Diego CA, USA, 1992, pp. 512–517. November.
[43] Fei Wang, Sine-triangle versus space-vector modulation for three-level PWM voltage-source inverters, IEEE Trans. Ind. Appl. 38 (2) (2002) 500–506.
[44] K.K. Tse, Henry Shu-Hung Chung, S.Y. Ron Hui, H.C. So, A comparative study of carrier-frequency modulation techniques for conducted EMI suppression in PWM converters, IEEE Trans. Ind. Electron. 49 (3) (2002) 618–627.
[45] K.L. Shi, H. Li, Optimized PWM strategy based on genetic algorithms, IEEE Trans. Ind. Electron. 52 (5) (2005) 1558–1561.

Overmodulation

[46] A. Hava, S. Sul, R. Kerkman, T. Lipo, Dynamic overmodulation characteristics of triangle intersection PWM methods, IEEE Trans. Ind. Appl. 35 (4) (1999) 896–907.
[47] A. Hava, R. Kerkman, T. Lipo, Carrier-based PWM-VSI overmodulation strategies: Analysis, comparison, and design, IEEE Trans. Power Electron. 13 (4) (1998) 674–689.
[48] Bon-Ho Bae, Seung-Ki Sul, A novel dynamic overmodulation strategy for fast torque control of high-saliency-ratio AC motor, IEEE Trans. Ind. Appl. 41 (4) (2005) 1013–1019.
[49] Hee-Jhung Park, Myung-Joong Youn, A new time-domain discontinuous space-vector PWM technique in overmodulation region, IEEE Trans. Ind. Electron. 50 (2) (2003) 349–355.
[50] S.K. Mondal, B.K. Bose, V. Oleschuk, J.O.P. Pinto, Space vector pulse width modulation of three-level inverter extending operation into overmodulation region, IEEE Trans. Power Electron. 18 (2) (2003) 604–611.
[51] A.M. Khambadkone, J. Holtz, Compensated synchronous PI current controller in overmodulation range and six-step operation of space-

vector-modulation-based vector-controlled drives, IEEE Trans. Ind. Electron. 49 (3) (2002) 574–580.
[52] G. Narayanan, V.T. Ranganathan, Extension of operation of space vector PWM strategies with low switching frequencies using different overmodulation algorithms, IEEE Trans. Power Electron. 17 (5) (2002) 788–798.
[53] A.R. Bakhshai, G. Joos, P.K. Jain, Hua Jin, Incorporating the overmodulation range in space vector pattern generators using a classification algorithm, IEEE Trans. Power Electron. 15 (1) (2000) 83–91.

Selective Harmonic Elimination

[54] S. Bowe, S. Grewal, Novel space-vector-based harmonic elimination inverter control, IEEE Trans. Ind. Appl. 36 (2) (2000) 549–557.
[55] L. Li, D. Czarkowski, Y. Liu, P. Pillay, Multilevel selective harmonic elimination PWM technique in series-connected voltage inverters, IEEE Trans. Ind. Appl. 36 (1) (2000) 160–170.
[56] H. Karshenas, H. Kojori, S. Dewan, Generalized techniques of selective harmonic elimination and current control in current source inverters/converters, IEEE Trans. Power Electron. 10 (5) (1995) 566–573.
[57] H. Patel, R. Hoft, Generalized techniques of harmonic elimination and voltage control in thyristor inverters, Part I-Harmonic elimination, IEEE Trans. Ind. Appl. 9 (3) (1973) 310–317.
[58] J.R. Wells, B.M. Nee, P.L. Chapman, P.T. Krein, Selective harmonic control: a general problem formulation and selected solutions, IEEE Trans. Power Electron. 20 (6) (2005) 1337–1345.
[59] M.J. Newman, D.G. Holmes, J.G. Nielsen, F. Blaabjerg, A dynamic voltage restorer (DVR) with selective harmonic compensation at medium voltage level, IEEE Trans. Ind. Appl. 41 (6) (2005) 1744–1753.
[60] J.R. Espinoza, G. Joos, J.I. Guzman, L.A. Moran, R.P. Burgos, Selective harmonic elimination and current/voltage control in current/voltage-source topologies: a unified approach, IEEE Trans. Ind. Electron. 48 (1) (2001) 71–81.

Effects of PWM-Type of Voltage Waveforms

[61] N. Aoki, K. Satoh, A. Nabae, Damping circuit to suppress motor terminal overvoltage and ringing in PWM inverter-fed ac motor drive systems with long motor leads, IEEE Trans. Ind. Appl. 35 (5) (1999) 1015–1020.
[62] D. Rendusara, P. Enjeti, An improved inverter output filter configuration reduces common and differential modes at the motor terminals in PWM drive systems, IEEE Trans. Power Electron. 13 (6) (1998) 1135–1153.
[63] S. Chen, T. Lipo, Bearing currents and shaft voltages of an induction motor under hard- and soft-switching inverter excitation, IEEE Trans. Ind. Appl. 34 (5) (1998) 1042–1048.
[64] A. von Jouanne, H. Zhang, A. Wallace, An evaluation of mitigation techniques for bearing currents, EMI and overvoltages in ASD applications, IEEE Trans. Ind. Appl. 34 (5) (1998) 1113–1122.
[65] H. Akagi, T. Doumoto, A passive EMI filter for preventing high-frequency leakage current from flowing through the grounded inverter heat sink of an adjustable-speed motor drive system, IEEE Trans. Ind. Appl. 41 (5) (2005) 1215–1223.

Multilevel Inverters

[66] L. Tolbert, T. Habetler, Novel multilevel inverter carrier-based PWM method, IEEE Trans. Ind. Appl. 35 (5) (1999) 1098–1107.
[67] G. Walker, G. Ledwich, Bandwidth considerations for multilevel converters, IEEE Trans. Power Electron. 15 (1) (1999) 74–81.
[68] Y. Liang, C. Nwankpa, A new type of STATCOM based on cascading voltage-source inverters with phase-shifted unipolar SPWM, IEEE Trans. Ind. Appl. 35 (5) (1999) 1118–1123.
[69] N. Schibli, T. Nguyen, A. Rufer, A three-phase multilevel converter for high-power induction motors, IEEE Trans. Power Electron. 13 (5) (1998) 978–986.
[70] J. Lai, F. Peng, Multilevel converters – A new breed of power converters, IEEE Trans. Ind. Appl. 32 (3) (1997) 509–517.
[71] R.M. Tallam, R. Naik, T.A. Nondahl, A carrier-based PWM scheme for neutral-point voltage balancing in three-level inverters, IEEE Trans. Ind. Appl. 41 (6) (2005) 1734–1743.
[72] M.A. Perez, J.R. Espinoza, J.R. Rodriguez, P. Lezana, Regenerative medium-voltage AC drive based on a multicell arrangement with reduced energy storage requirements, IEEE Trans. Ind. Electron. 52 (1) (2005) 171–180.
[73] F.L.M. Antunes, H.A.C. Braga, I. Barbi, Application of a Generalized Current Multilevel Cell to Current-Source Inverters, IEEE Trans. Ind. Electron. 46 (1) (1999) 31–38.
[74] P.G. Barbosa, H.A. Carvalho, M. do C. Barbosa, E. Coelho, Boost current multilevel inverter and its application on single-phase grid-connected photovoltaic systems, IEEE Trans. Power Electron. 21 (4) (2006) 1116–1124.
[75] N. Vázquez, H. López, C. Hernández, E. Vázquez, R. Osorio, J. Arau, A Different Multilevel Current Source Inverter, IEEE Trans. Ind. Electron. 57 (8) (2010) 2623–2632.

Regeneration

[76] P. Verdelho, G. Marques, DC voltage control and stability analysis of PWM-voltage-type reversible rectifiers, IEEE Trans. Ind. Electron. 45 (2) (1998) 263–273.
[77] J. Espinoza, G. Joós, A. Bakhshai, Non-linear control and stabilization of PWM current source rectifiers in the regeneration mode, in: Conf. Rec. APEC'97, Atlanta GA, USA, 1997, pp. 902–908 February.
[78] M. Hinkkanen, J. Luomi, Stabilization of regenerating-mode operation in sensorless induction motor drives by full-order flux observer design, IEEE Trans. Ind. Electron. 51 (6) (2004) 1318–1328.
[79] T. Tanaka, S. Fujikawa, S. Funabiki, A new method of damping harmonic resonance at the DC link in large-capacity rectifier-inverter systems using a novel regenerating scheme, IEEE Trans. Ind. Appl. 38 (4) (2002) 1131–1138.
[80] J. Rodriguez, J. Pontt, E. Silva, J. Espinoza, M. Perez, Topologies for regenerative cascaded multilevel inverters" in: Conf. Rec. PESC'03, Acapulco, Mexico, 2003, pp. 519–524.

12

Resonant and Soft-Switching Converters

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12.1 Introduction

Advances in power electronics in the last few decades have led to not only improvements in power devices but also new concepts in converter topologies and control. In the 1970s, conventional pulse-width modulation (PWM) power converters were operated in a switched-mode operation. Power switches have to cut off the load current within the turn-on and turn-off times under the hard-switching conditions. Hard switching refers to the stressful switching behavior of the power electronic devices. The switching trajectory of a hard-switched power device is shown in Fig. 12.1. During the turn-on and turn-off processes, the power device has to withstand high voltage and current simultaneously, resulting in high switching losses and stress.

Dissipative passive snubbers are usually added to the power circuits so that the *dv/dt* and *di/dt* of the power devices could be reduced and the switching loss and stress be diverted to the

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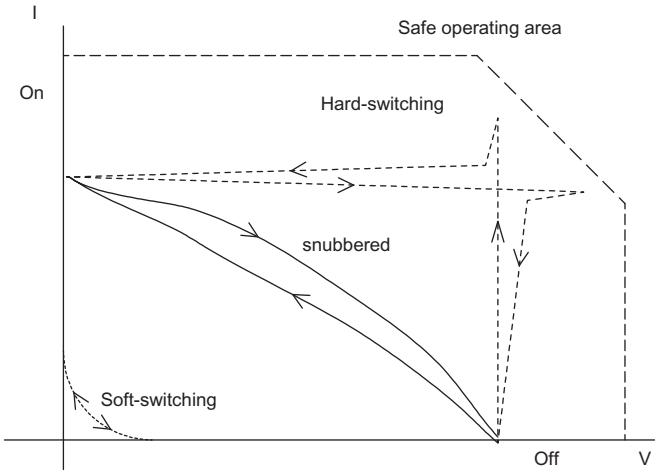


FIG. 12.1 Typical switching trajectories of power switches.

passive snubber circuits. However, the switching loss is proportional to the switching frequency, thus limiting the maximum switching frequency of the power converters. Typical converter switching frequency was limited to a few tens of kilohertz (typically 20–50 kHz) in the early 1980s. The stray inductive and capacitive components in the power circuits and power devices still cause considerable transient effects, which in turn give rise to electromagnetic interference (EMI) problems. Fig. 12.2 shows ideal switching waveforms and typical practical waveforms of the switch voltage. The transient ringing effects are major causes of EMI.

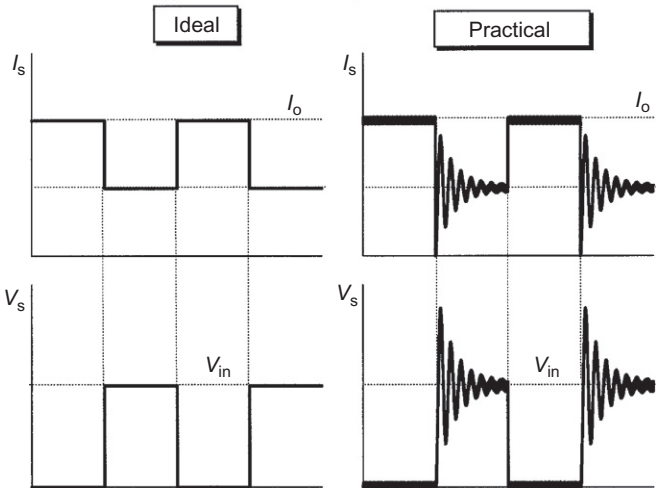
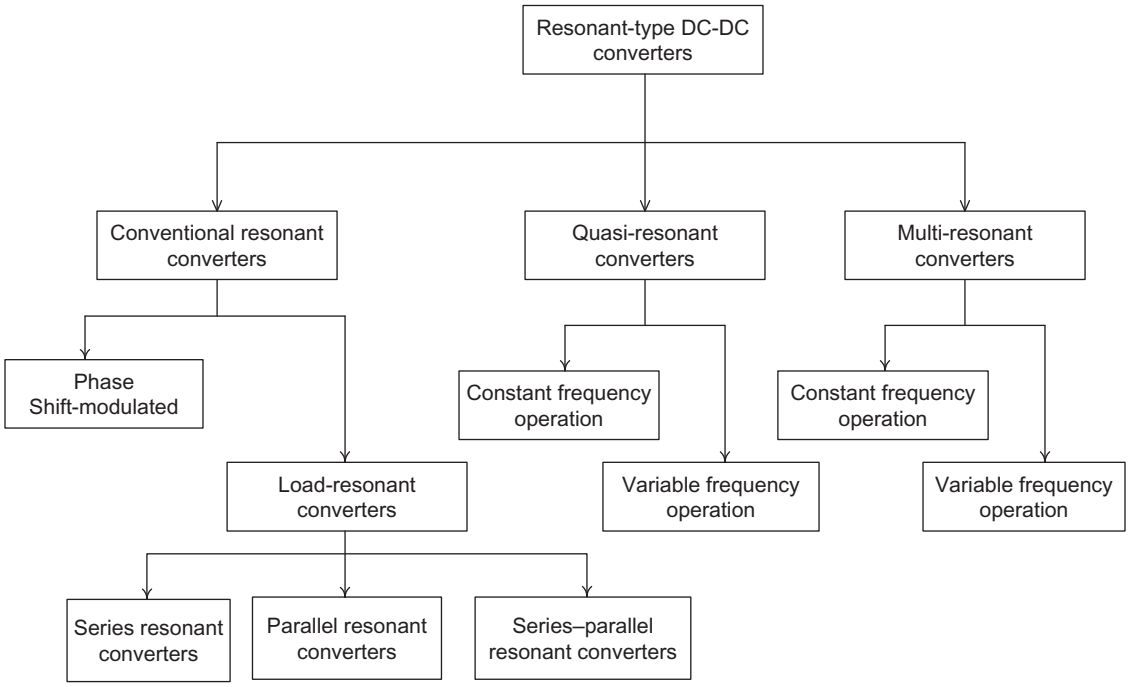


FIG. 12.2 Typical: (A) ideal and (B) practical switching waveforms.

In the 1980s, lots of research efforts were diverted toward the use of resonant converters. The concept was to incorporate resonant tanks in the converters to create oscillatory (usually sinusoidal) voltage and/or current waveforms so that zero-voltage switching (ZVS) or zero-current switching (ZCS) conditions can be created for the power switches. The reduction of switching loss and the continual improvement of power switches allow the switching frequency of the resonant converters to reach hundreds of kilohertz (typically 100–500 kHz). Consequently, the size of magnetic components can be reduced, and the power density of the converters increased. Various forms of resonant converters have been proposed and developed. However, most of the resonant converters suffer several problems. When compared with the conventional PWM converters, the resonant current and the voltage of resonant converters have high peak values, leading to higher conduction loss and higher V and I rating requirements for the power devices. Also, many resonant converters require frequency modulation (FM) for output regulation. Variable switching frequency operation makes the filter design and control more complicated.

In the late 1980s and throughout the 1990s, further improvements have been made in converter technology. New generations of soft-switched converters that combine the advantages of conventional PWM converters and resonant converters have been developed. These soft-switched converters have switching waveforms similar to those of conventional PWM converters except that the rising and falling edges of the waveforms are "smoothed" with no transient spikes. Unlike the resonant converters, new soft-switched converters usually utilize the resonance in a controlled manner. Resonance is allowed to occur just before and during the turn-on and turn-off processes so as to create ZVS and ZCS conditions. Other than that, they behave just like conventional PWM converters. With simple modifications, many customized control integrated circuits (ICs) designed for conventional converters can be employed for soft-switched converters. Because the switching loss and stress have been reduced, soft-switched converter can be operated at the very high frequency (typically 500 kHz to a few megahertz). Soft-switching converters also provide an effective solution to suppress EMI and have been applied to DC-DC, AC-DC, and DC-AC converters. This chapter covers the basic technology of resonant and soft-switching converters. Various forms of soft-switching techniques such as ZVS, ZCS, voltage clamping, and zero-voltage transition methods are addressed. The emphasis is placed on the basic operating principle and practicality of the converters without using much mathematical analysis.

12.2 Classification



12.3 Resonant Switch

Prior to the availability of fully controllable power switches, thyristors were the major power devices used in power electronic circuits. Each thyristor requires a commutation circuit, which usually consists of an *LC* resonant circuit, for forcing the current to zero in the turn-off process [1]. This mechanism is in fact a type of zero-current turn-off process. With the recent advancement in semiconductor technology, the voltage and current handling capability and the switching speed of fully controllable switches have significantly been improved. In many high-power applications, controllable switches such as gate turn-offs (GTOs) and insulated-gate bipolar transistors (IGBTs) have replaced thyristors [2,3]. However, the use of resonant circuit for achieving ZCS and/or ZVS [4–8] has also emerged as a new technology for power converters. The concept of resonant switch that replaces conventional power switch is introduced in this section.

A resonant switch is a subcircuit comprising a semiconductor switch S and resonant elements, L_r and C_r [9–11]. The switch S can be implemented by a unidirectional or bidirectional switch, which determines the operation mode of the resonant switch. Two types of resonant switches [12], including zero-current (ZC) resonant switch and zero-voltage (ZV) resonant switches, are shown in Figs. 12.3 and 12.4, respectively.

12.3.1 ZC Resonant Switch

In a ZC resonant switch, an inductor L_r is connected in series with a power switch S in order to achieve zero-current switching (ZCS). If the switch S is a unidirectional switch, the switch current is allowed to resonate in the positive half cycle only. The resonant switch is said to operate in *half-wave* mode. If a diode is connected in antiparallel with the unidirectional switch, the switch current can flow in both directions. In this case, the resonant switch can operate in *full-wave* mode. At turn-on, the switch current will rise slowly from zero. It will then oscillate, because of the resonance between L_r and C_r. Finally, the switch can be commutated at the next zero-current duration. The objective of this type of switch is to shape the switch current waveform during conduction time in order to create a zero-current condition for the switch to turn off [13].

12.3.2 ZV Resonant Switch

In a ZV resonant switch, a capacitor C_r is connected in parallel with the switch S for achieving zero-voltage switching (ZVS). If

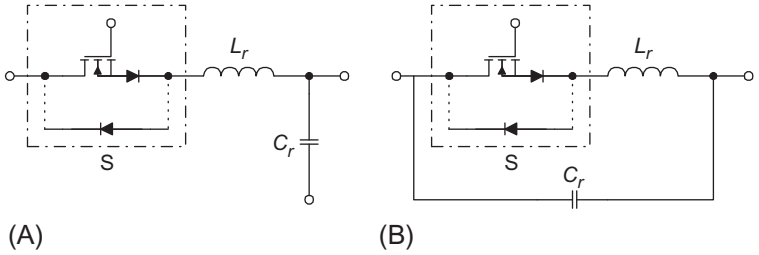


FIG. 12.3 Zero-current (ZC) resonant switch. (A) Option 1. (B) Option 2.

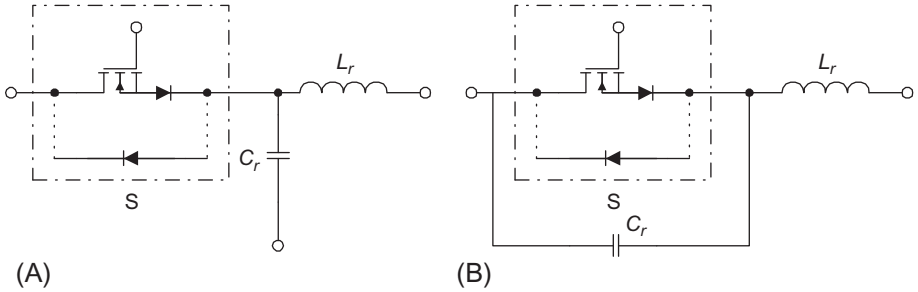


FIG. 12.4 Zero-voltage (ZV) resonant switch. (A) Option 1. (B) Option 2.

the switch S is a unidirectional switch, the voltage across the capacitor C_r can oscillate freely in both positive and negative half cycle. Thus, the resonant switch can operate in *full-wave* mode. If a diode is connected in antiparallel with the unidirectional switch, the resonant capacitor voltage is clamped by the diode to zero during the negative half cycle. The resonant switch will then operate in *half-wave* mode. The objective of a ZV switch is to use the resonant circuit to shape the switch voltage waveform during the off time in order to create a zero-voltage condition for the switch to turn on [13].

12.4 Quasi-Resonant Converters

Quasi-resonant converters (QRCs) can be considered as a hybrid of resonant and PWM converters. The underlying principle is to replace the power switch in PWM converters with the resonant switch. A large family of conventional converter circuits can be transformed into their resonant converter counterparts. The switch current and/or voltage waveforms are forced to oscillate in a quasi-sinusoidal manner, so that ZCS and/or ZVS can be achieved. Both ZCS-QRCs and ZVS-QRCs have *half-wave* and *full-wave* mode of operations [8–10,12].

12.4.1 ZCS-QRCs

A ZCS-QRC designed for *half-wave* operation is illustrated with a buck-type DC-DC converter. The schematic is shown in Fig. 12.5A. It is formed by replacing the power switch in conventional PWM buck converter with the ZC resonant switch in Fig. 12.3A. The circuit waveforms in steady state are shown in Fig. 12.5B. The output filter inductor L_f is sufficiently large so that its current is approximately constant. Prior to turning the switch on, the output current I_o freewheels through the output diode D_f. The resonant capacitor voltage V_{Cr} equals zero. At t_0, the switch is turned on with ZCS. A quasi-sinusoidal current I_S flows through L_r and C_r, the output filter, and the load. S is then softly commutated at t_1 with ZCS again. During and after the gate pulse, the resonant capacitor voltage V_{Cr} rises and then decays at a rate depending on the output current. Output voltage regulation is achieved by controlling the switching frequency. Operation and characteristics of the converter depend mainly on the design of the resonant circuit L_r C_r. The following parameters are defined: voltage conversion ratio M, characteristic impedance Z_r, resonant frequency f_r, normalized load resistance r, and normalized switching frequency γ:

$$M = \frac{V_o}{V_i} \tag{12.1A}$$

$$Z_r = \sqrt{\frac{L_r}{C_r}} \tag{12.1B}$$

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{12.1C}$$

$$r = \frac{R_L}{z_r} \tag{12.1D}$$

$$\gamma = \frac{f_s}{f_r} \tag{12.1E}$$

It can be seen from the waveforms that if $I_o > V_i/Z_r$, I_S will not come back to zero naturally and the switch will have to be forced off, thus resulting in turn-off losses.

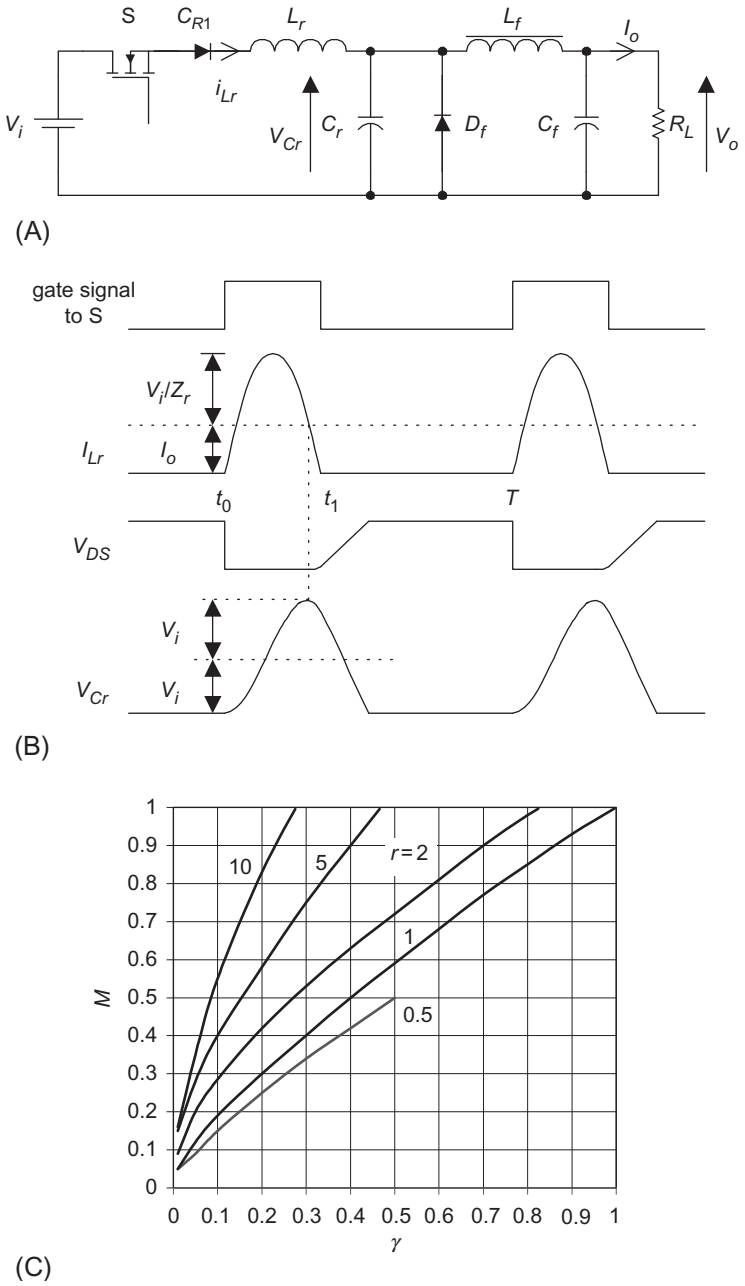


FIG. 12.5 Half-wave, quasi-resonant buck converter with ZCS: (A) schematic diagram, (B) circuit waveforms, and (C) relationship between M and γ.

The relationships between M and γ at different r are shown in Fig. 12.5C. It can be seen that M is sensitive to the load variation. At light-load conditions, the unused energy is stored in C_r, leading to an increase in the output voltage. Thus, the switching frequency has to be controlled, in order to regulate the output voltage.

If an antiparallel diode is connected across the switch, the converter will be operating in *full-wave* mode. The circuit schematic is shown in Fig. 12.6A. The circuit waveforms in steady state are shown in Fig. 12.6B. The operation is similar to the one in *half-wave* mode. However, the inductor current is allowed to reverse through the antiparallel diode, and the duration for the resonant stage is lengthened. This permits excess energy in the resonant circuit at light loads to be transferred back to the voltage source V_i. This significantly reduces the dependence of V_o on the output load. The relationships between M and γ at different r are shown in Fig. 12.6C. It can be seen that M is insensitive to load variation.

By replacing the switch in the conventional converters, a family of QRC [9] with ZCS is shown in Fig. 12.7.

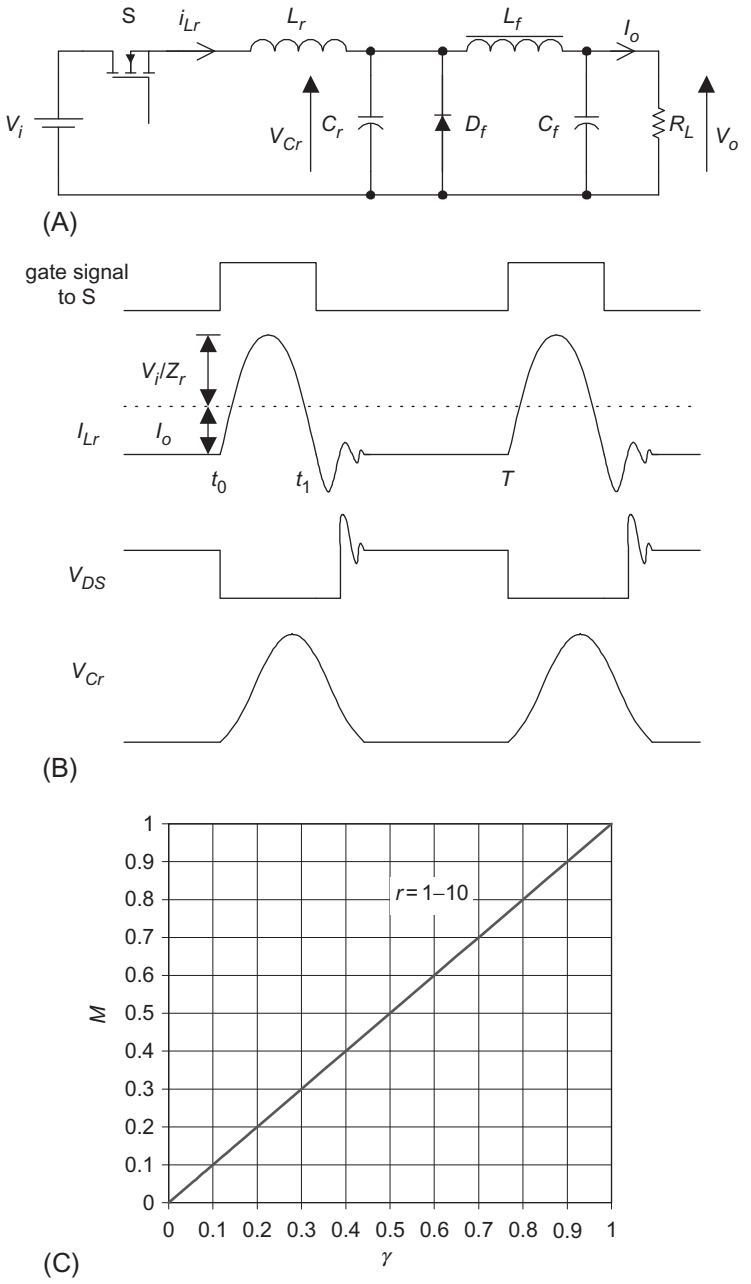


FIG. 12.6 Full-wave, quasi-resonant buck converter with ZCS: (A) schematic diagram, (B) circuit waveforms, and (C) relationship between M and γ.

12.4.2 ZVS-QRC

In these converters, the resonant capacitor provides a zero-voltage condition for the switch to turn on and off. A quasi-resonant buck converter designed for *half-wave* operation is shown in Fig. 12.8A—using a ZV resonant switch in Fig. 12.4B. The steady-state circuit waveforms are shown in Fig. 12.8B. Basic relations of ZVS-QRCs are given in Eqs. (12.1A)–(12.1E). When the switch S is turned on, it carries the output current I_o. The supply voltage V_i reverse biases the diode D_f. When the switch is zero-voltage (ZV) turned off, the output current starts to flow through the resonant capacitor C_r. When the resonant capacitor voltage V_{Cr} is equal to V_i, D_f turns on. This starts the resonant stage. When V_{Cr} equals zero, the antiparallel diode turns on. The resonant capacitor is shorted, and the source voltage is applied to the resonant inductor L_r. The resonant inductor current I_{Lr} increases linearly until it reaches I_o. Then, D_f turns off. In order to achieve ZVS, S should be triggered during the time when the antiparallel diode conducts. It can be seen from the waveforms that the

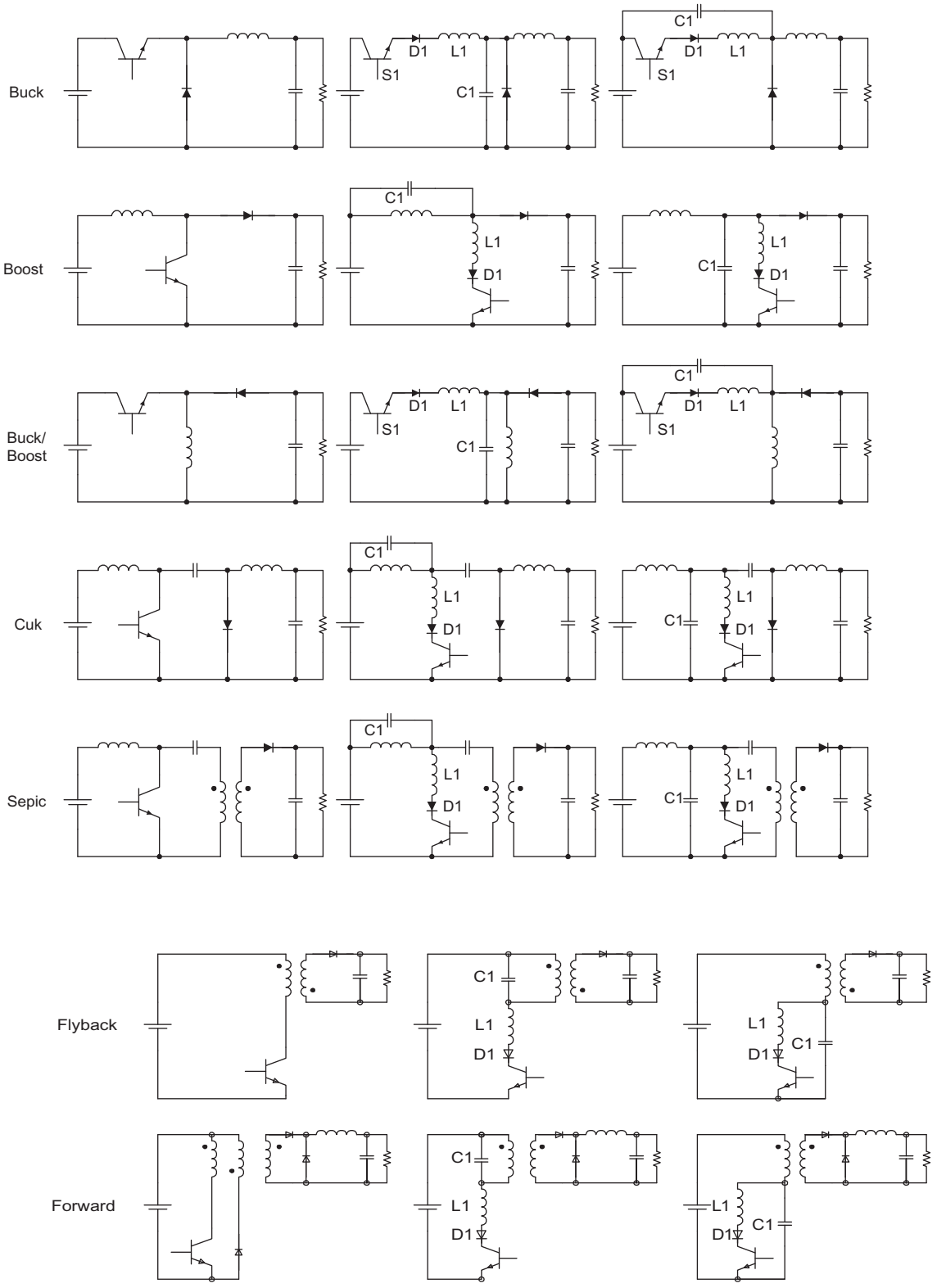


FIG. 12.7 A family of quasi-resonant converter with ZCS.

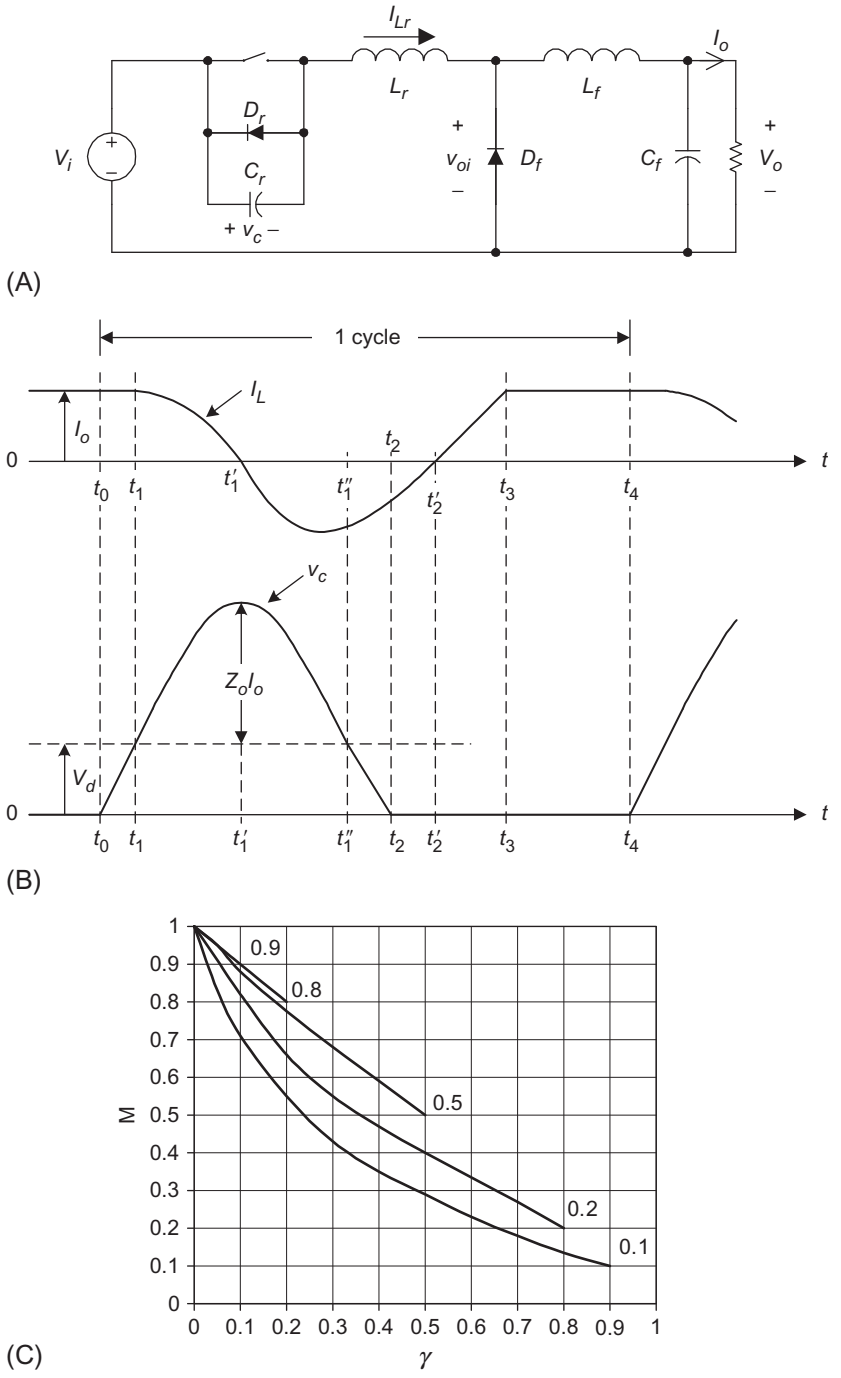


FIG. 12.8 Half-wave, quasi-resonant buck converter with ZVS: (A) schematic diagram, (B) circuit waveforms, and (C) relationship between M and γ.

peak amplitude of the resonant capacitor voltage should be greater or equal to the input voltage (i.e., $I_o Z_r > V_{in}$). From Fig. 12.8C, it can be seen that the voltage conversion ratio is load-sensitive. In order to regulate the output voltage for different loads r, the switching frequency should also be changed accordingly.

ZVS converters can be operated in *full-wave* mode. The circuit schematic is shown in Fig. 12.9A. The circuit waveforms in steady state are shown in Fig. 12.9B. The operation is similar to *half-wave* mode of operation, except that V_{Cr} can swing between positive and negative voltages. The relationships between M and γ at different r are shown in Fig. 12.9C.

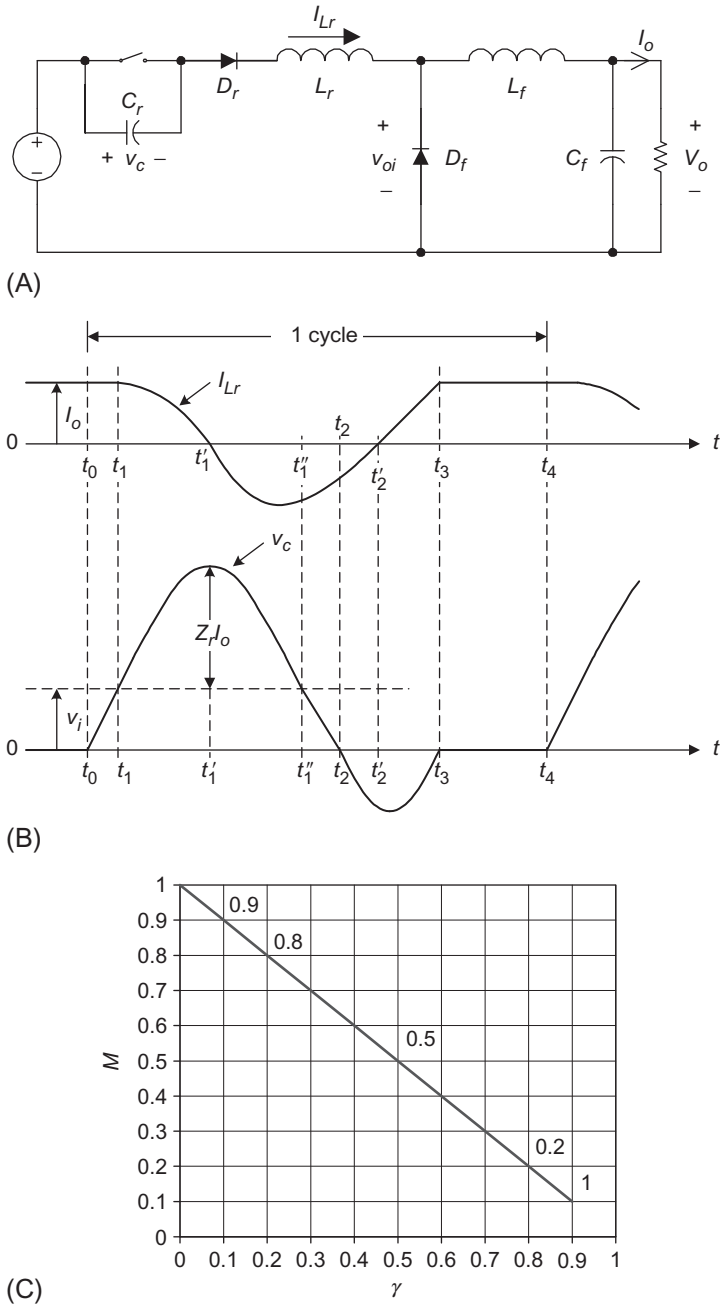


FIG. 12.9 Full-wave, quasi-resonant buck converter with ZVS: (A) schematic diagram, (B) circuit waveforms, and (C) relationship between M and γ.

Comparing Fig. 12.8C with Fig. 12.9C, it can be seen that M is load-insensitive in *full-wave* mode. This is a desirable feature. However, as the series diode limits the direction of the switch current, energy will be stored in the output capacitance of the switch and will dissipate in the switch during turn-on. Hence, the *full-wave* mode has the problem of capacitive turn-on loss and is less practical in high-frequency operation. In practice, ZVS-QRCs are usually operated in *half-wave* mode rather than *full-wave* mode.

By replacing the ZV resonant switch in the conventional converters, various ZVS-QRCs can be derived. They are shown in Fig. 12.10.

12.4.3 Comparisons Between ZCS and ZVS

ZCS can eliminate the switching losses at turnoff and reduce the switching losses at turn-on. As a relatively large capacitor is connected across the output diode during resonance,

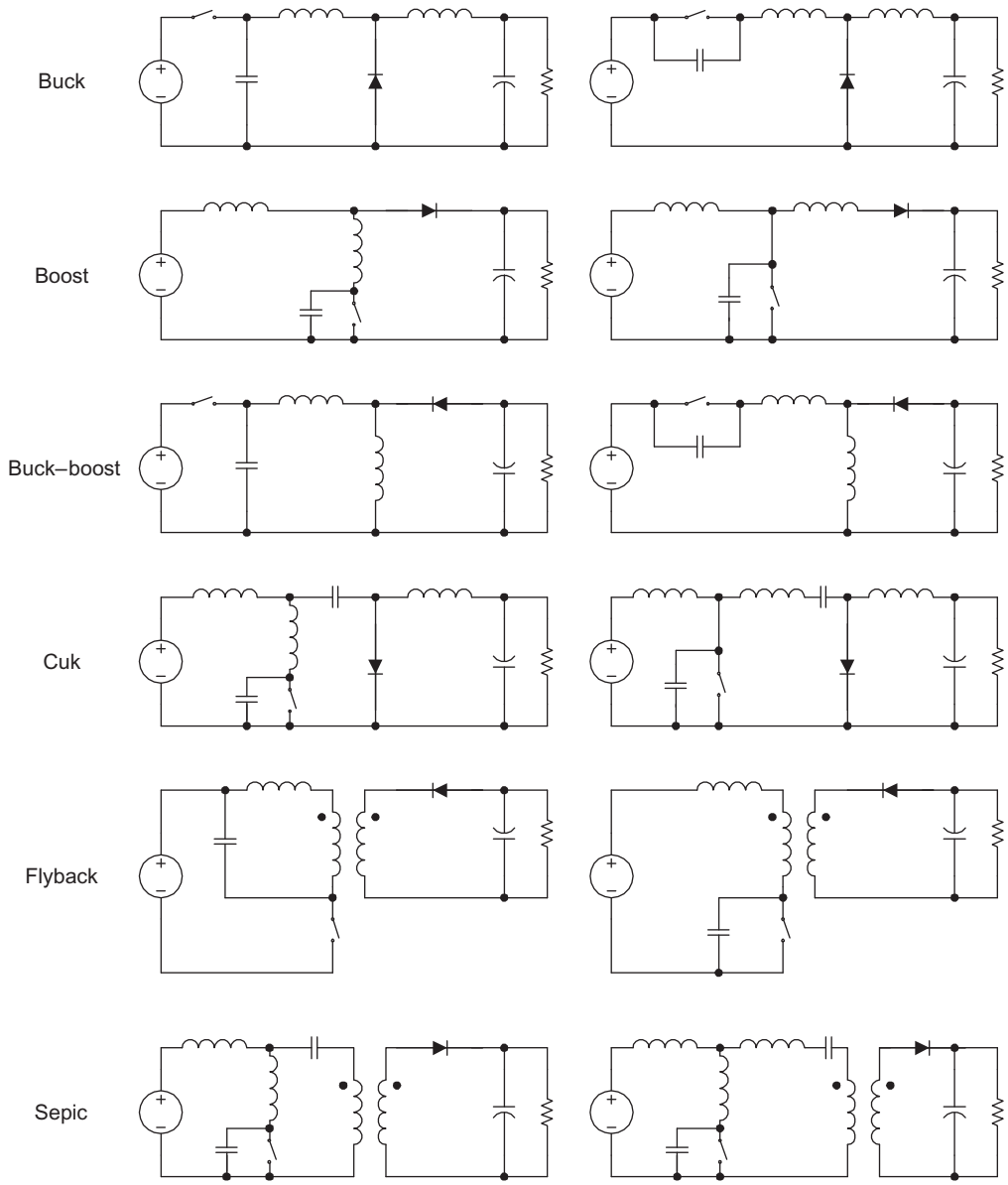


FIG. 12.10 A family of quasi-resonant converter with ZVS.

the converter operation becomes insensitive to the diode's junction capacitance. When power MOSFETs are zero-current switched on, the energy stored in the device's capacitance will be dissipated. This capacitive turn-on loss is proportional to the switching frequency. During turn-on, considerable rate of change of voltage can be coupled to the gate drive circuit through the Miller capacitor, thus increasing switching loss and noise. Another limitation is that the switches are under high current stress, resulting in higher conduction loss. However, it should be noted that ZCS is particularly effective in reducing switching loss for power devices (such as IGBT) with large tail current in the turn-off process.

ZVS eliminates the capacitive turn-on loss. It is suitable for high-frequency operation. For single-ended configuration, the switches could suffer from excessive voltage stress, which is proportional to the load. It will be shown in Section 12.5 that the maximum voltage across switches in half-bridge and full-bridge configurations is clamped to the input voltage.

For both ZCS and ZVS, the output regulation of the resonant converters can be achieved by variable frequency control. ZCS operates with constant on-time control, while ZVS operates with constant off-time control. With a wide input and load range, both techniques have to operate with a wide switching frequency range, making it not easy to design resonant converters optimally.

12.5 ZVS in High Frequency Applications

By the nature of the resonant tank and ZCS, the peak switch current in resonant converters is much higher than that in the square-wave counterparts. In addition, a high voltage will be established across the switch in the off state after the resonant stage. When the switch is switched on again, the energy stored in the output capacitor will be discharged through the switch, causing a significant power loss at high frequencies and high voltages. This switching loss can be reduced by using ZVS.

ZVS can be viewed as square-wave power utilizing a constant off-time control. Output regulation is achieved by controlling the on-time or switching frequency. During the off time, the resonant tank circuit traverses the voltage across the switch from zero to its peak value and then back to zero again. At that ZV instant, the switch can be reactivated. Apart from the conventional single-ended converters, some other examples of converters with ZVS are illustrated in the following section.

12.5.1 ZVS With Clamped Voltage

The high voltage stress problem in the single-switch configuration with ZVS can be avoided in half-bridge (HB) and full-bridge (FB) configurations [14–17]. The peak switch voltage can be clamped to the DC supply rail, thus reducing the switch voltage stress. In addition, the series transformer leakage and circuit inductance can form parts of the resonant path. Therefore, these parasitic components, which are undesirable in hard-switched converter, become useful components in ZVS ones. Figs. 12.11 and 12.12 show the ZVS HB and FB circuits, respectively, together with the circuit waveforms. The resonant capacitor is equivalent to the parallel connection of the two capacitors ($C_r/2$) across the switches. The off-state voltage of the switches will not exceed the input voltage during resonance because they will be clamped to the supply rail by the antiparallel diode of the switches.

12.5.2 Phase-shifted Converter With Zero Voltage Transition

In a conventional FB converter, the two diagonal switch pairs are driven alternatively. The output transformer is fed with an AC rectangular voltage. By applying a phase-shifting approach, a deliberate delay can be introduced between the gate signals and the switches [18]. The circuit waveforms are shown in Fig. 12.13. Two upper or lower switches can be conducting (either through the switch or the antiparallel diode), yet the applied voltage to the transformer is zero. This zero-voltage condition appears in the interval $[t_1, t_2]$ of V_{pri} in Fig. 12.13. This operating stage corresponds to the required off time for that particular switching cycle. When the desired switch is turned off, the primary transformer current flows into the switch output capacitance causing the switch voltage to resonate to the opposite input rail. Effects of the parasitic circuit components are used advantageously to facilitate the resonant transitions. This enables a ZVS condition for turning on the opposite switch. Thus, varying the phase shift controls the effective duty cycle and hence the output power. The resonant circuit is necessary to meet the requirement of providing sufficient inductive energy to drive the capacitors to the opposite bus rail. The resonant transition must be achieved within the designed transition time.

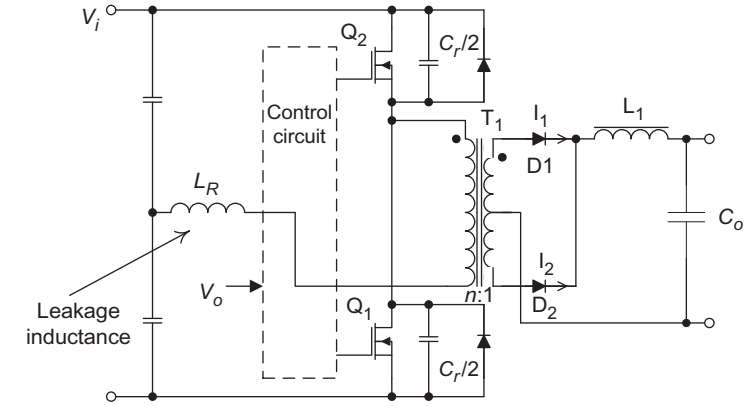
12.6 Multi-resonant Converters

The ZCS-QRCs and ZVS-QRCs optimize the switching condition for either the active switch or the output diode only, but not for both of them simultaneously. Multiresonant switch concept, which is an extension of the concept of the resonant switch, has been developed to overcome such limitation. The zero-current multiresonant (ZC-MR) and zero-voltage multiresonant (ZV-MR) switches [12,17] are shown in Fig. 12.14.

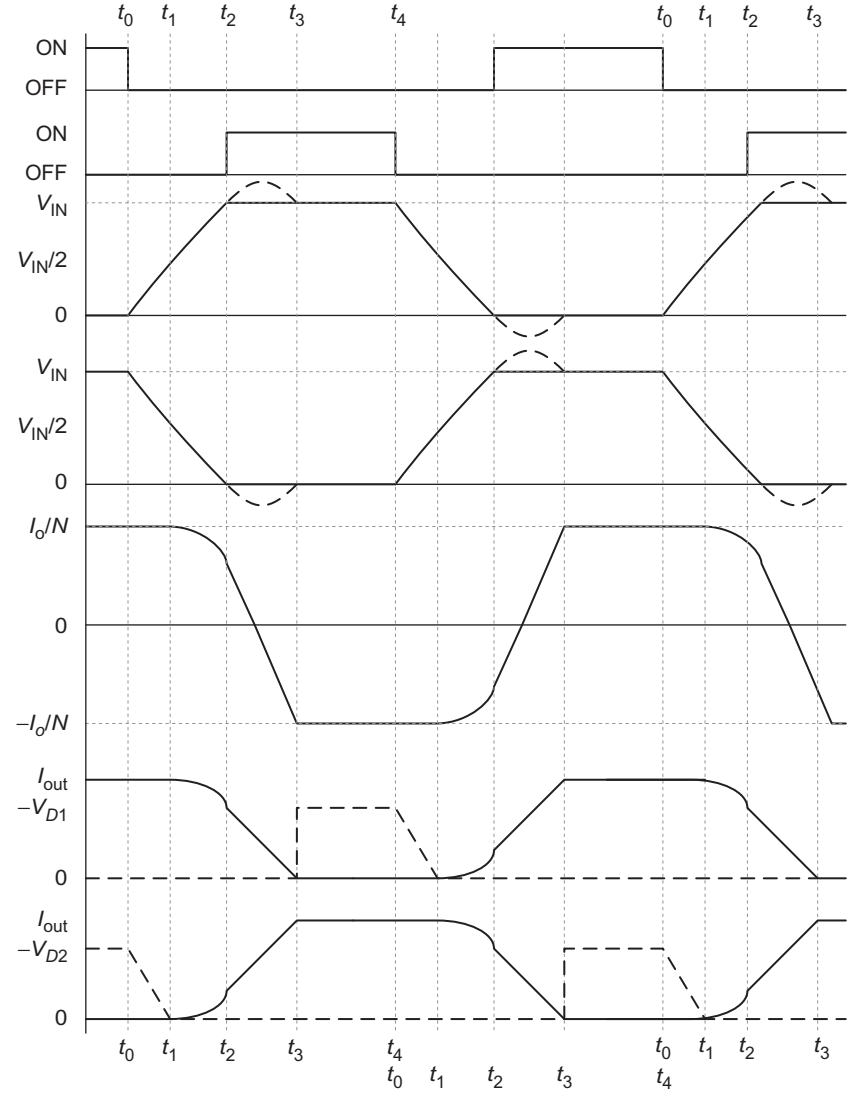
The multiresonant circuits incorporate all major parasitic components, including switch output capacitance, diode junction capacitance, and transformer leakage inductance into the resonant circuit. In general, ZVS (*half-wave* mode) is more favorable than ZCS in DC-DC converters for high-frequency operation because the parasitic capacitance of the active switch and the diode will form a part of the resonant circuit.

An example of a buck ZVS-MRC is shown in Fig. 12.15. Depending on the ratio of the resonant capacitance C_D/C_S, two possible topological modes, namely, mode I and mode II, can be operated [19]. The ratio affects the time at which the voltages across the switch S and the output diode D_f become zero. Their waveforms are shown in Fig. 12.16A and B, respectively. If diode voltage V_D falls to zero earlier than the switch voltage V_S, the converter will follow mode I. Otherwise, the converter will follow mode II.

Instead of having one resonant stage, there are three in this converter. The mode I operation in Fig. 12.16A is described first. Before the switch S is turned on, the output diode D_f is conducting, and the resonant inductor current I_{Lr} is negative (flowing through the antiparallel diode of S). S is then turned on with ZVS. The resonant inductor current I_{Lr} increases linearly and D_f is still conducting. When I_{Lr} reaches the output current I_o, the first resonant stage starts. The resonant circuit is formed by the resonant inductor L_r and the capacitor C_D across the output diode. This stage ends when S is turned off with ZVS. Then, a second resonant stage starts. The resonant circuit consists of L_r, C_D, and the capacitor across the switch C_s. This stage ends when the output diode becomes forward-biased. A third resonant stage will then start. L_r and C_s form the resonant circuit. This stage ends and completes one operation cycle when the diode C_s becomes forward-biased.

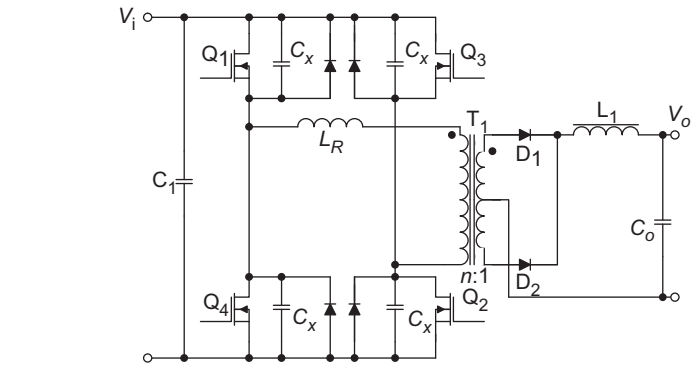


(A)

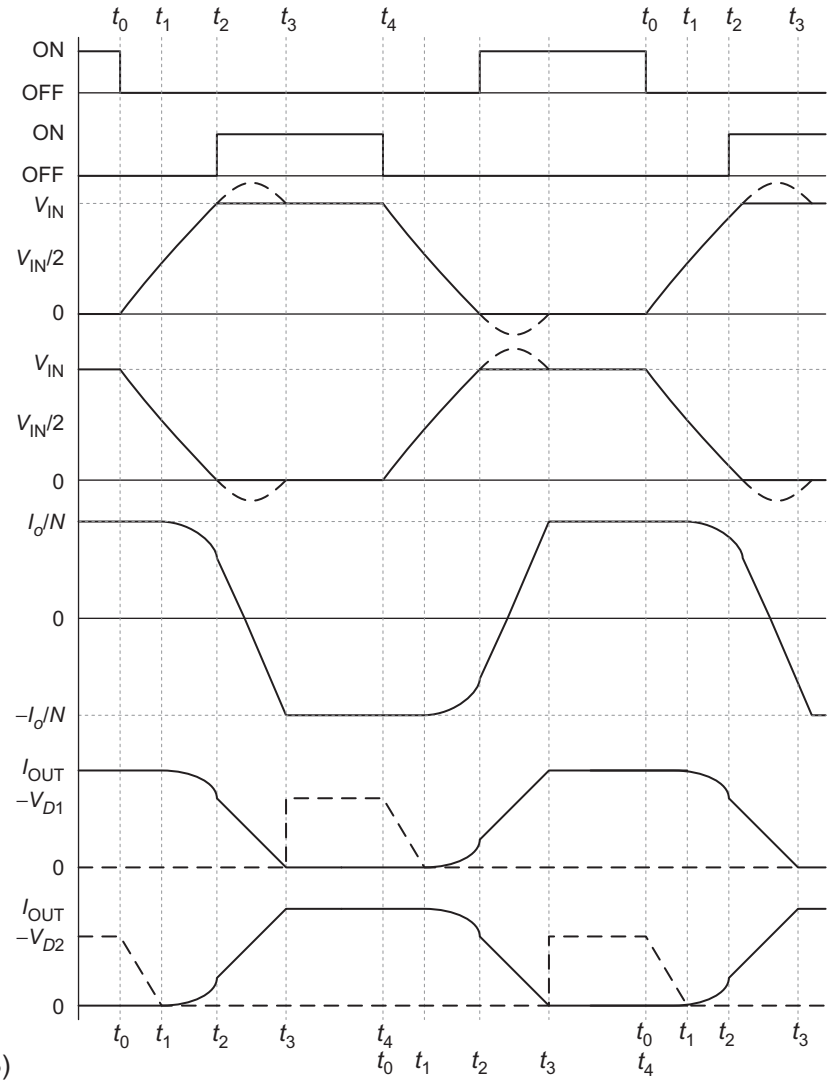


(B)

FIG. 12.11 Half-bridge converter with ZVS: (A) circuit diagram and (B) circuit waveforms.



(A)



(B)

FIG. 12.12 Full-bridge converter with ZVS: (A) circuit schematics and (B) circuit waveforms.

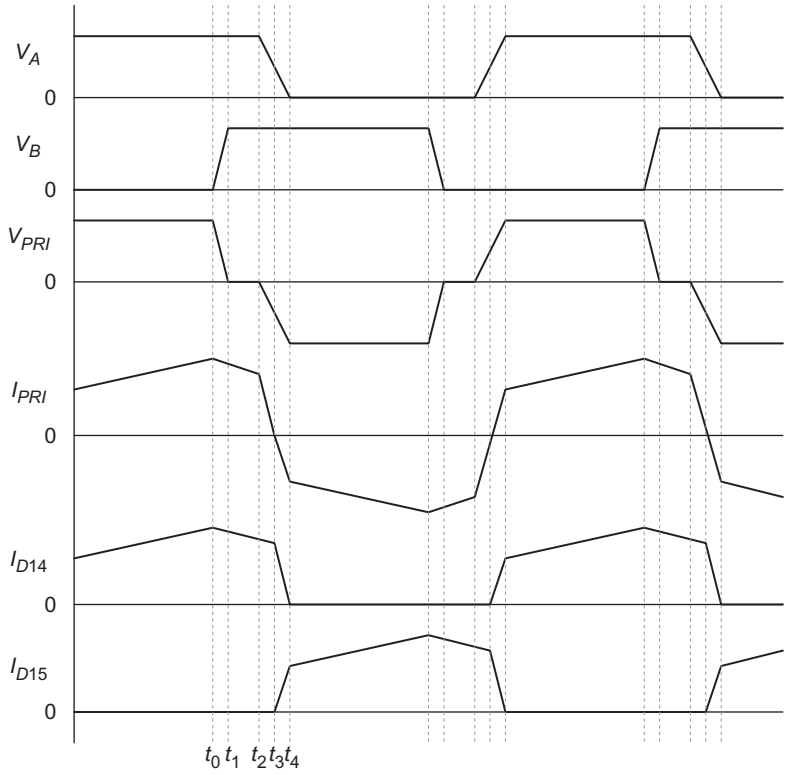


FIG. 12.13 Circuit waveforms of the phase-shifted, ZVT FB converter.

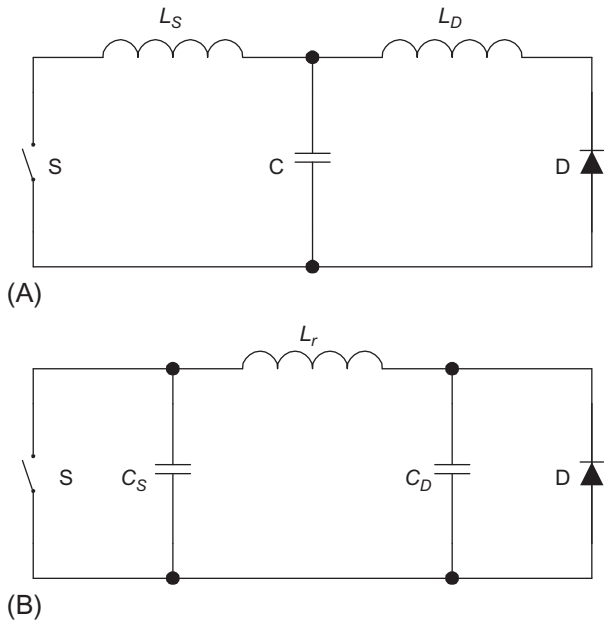


FIG. 12.14 Multiresonant switches: (A) ZC-MR switch and (B) ZV-MR switch.

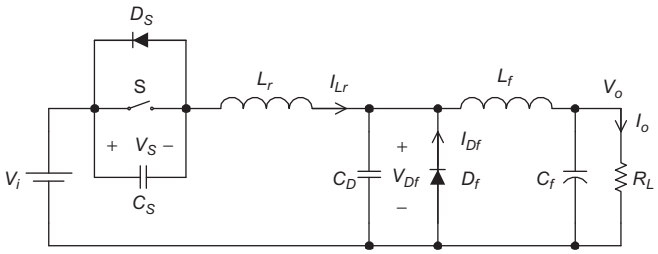


FIG. 12.15 Buck ZVS-MRC.

The only difference between mode I and mode II in Fig. 12.16B is in the third resonant stage, in which the resonant circuit is formed by L_r and C_D. This stage ends when D_f becomes forward-biased. The concept of the multiresonant switch can be applied to conventional converters [19–21]. A family of multi-resonant converters (MRCs) are shown in Fig. 12.17.

Although the variation of the switching frequency for regulation in MRCs is smaller than that of QRCs, a wideband frequency modulation is still required. Hence, the optimal design of magnetic components and the EMI filters in MRCs is not easy.

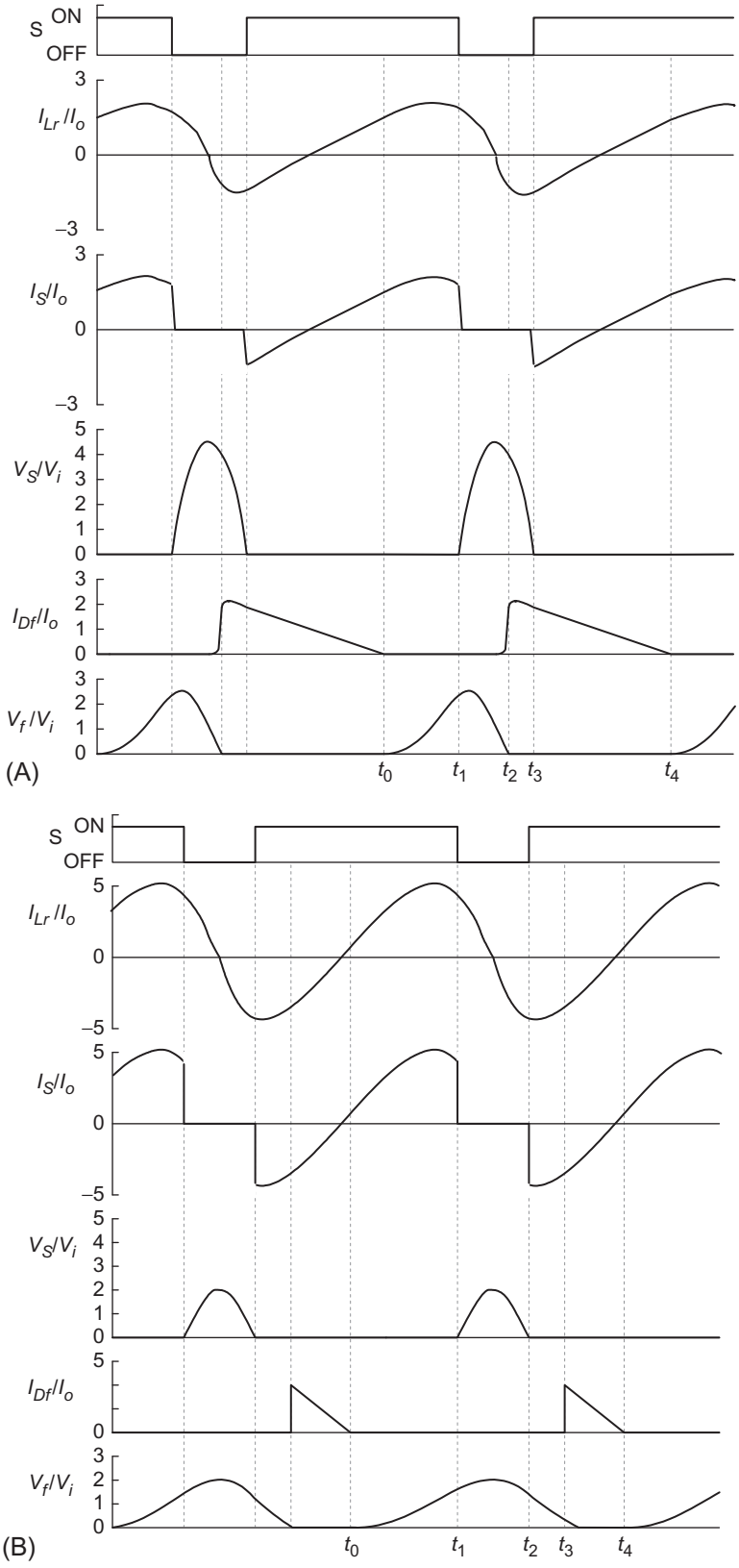


FIG. 12.16 Possible modes of the buck ZVS-MRC: (A) mode I and (B) mode II.

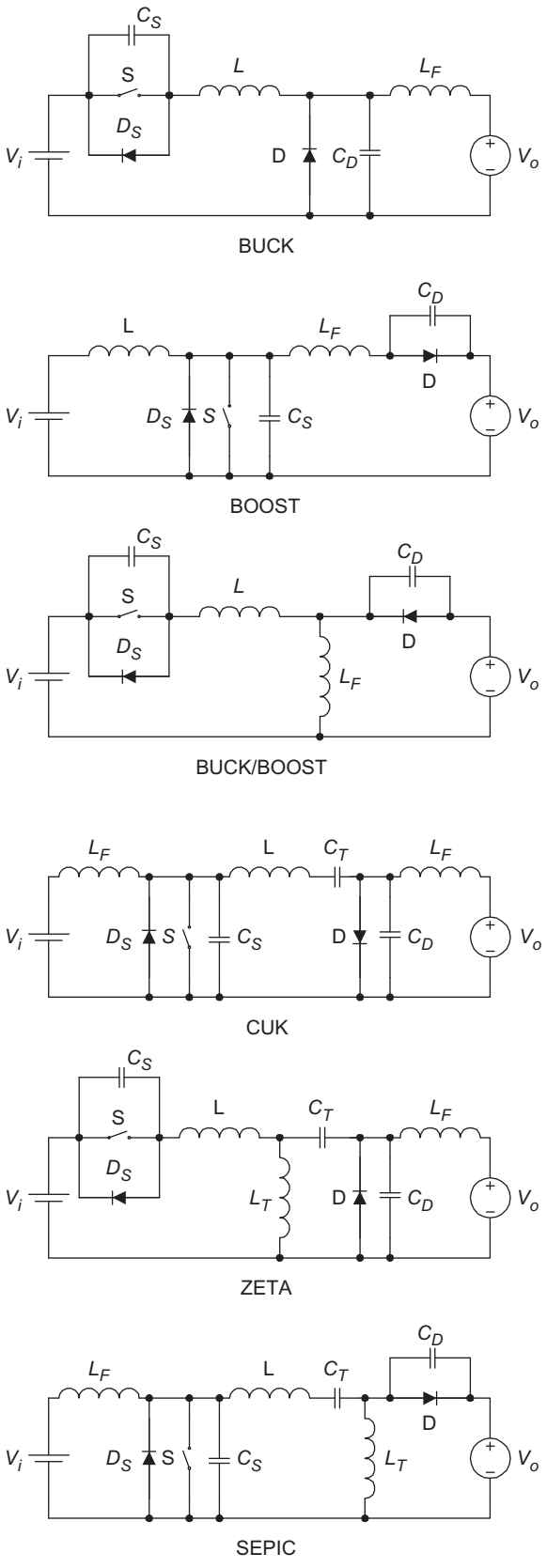


FIG. 12.17 Use of the multiresonant switch in conventional PWM converters.

It would be desirable to have a constant switching frequency operation. In order to operate the MRCs with constant switching frequency, the diode in Fig. 12.14 can be replaced with an active switch S_2 [22]. A constant-frequency multiresonant (CF-MR) switch is shown in Fig. 12.18. The output voltage is regulated by controlling the on-time of the two switches. This concept can be illustrated with the buck converter as shown in Fig. 12.19, together with the gate drive waveforms and operating

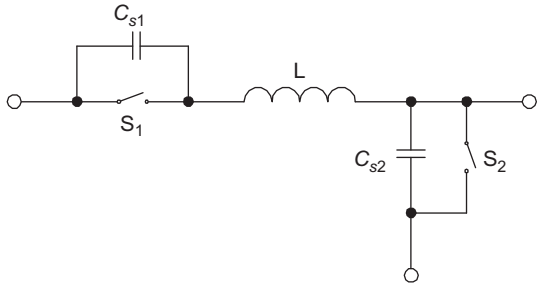


FIG. 12.18 Constant frequency multiresonant switch.

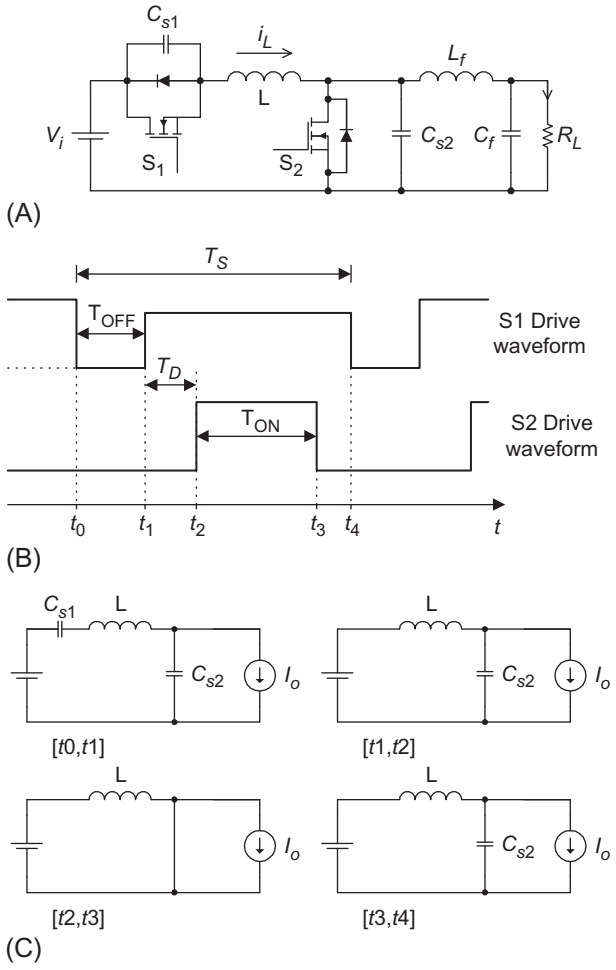


FIG. 12.19 Constant frequency buck MRC: (A) circuit schematics, (B) gate drive waveforms, and (C) operating stages.

stages. S_1 and S_2 are turned on during the time when currents flow through the anti-parallel diodes of S_1 and S_2. This stage ends when S_2 is turned off with ZVS. The first resonant stage is then started. L_r and C_{S2} form the resonant circuit. A second resonant stage begins. L_r resonates with C_{S1} and C_{S2}. The voltage across S_1 oscillates to zero. When I_{Lr} becomes negative, S_1 will be turned on with ZVS. Then, L_r resonates with C_{S2}. S_2 will be turned on when current flows through D_{S2}. As the output voltage is the average voltage across S_2, output voltage regulation is achieved by controlling the conduction time of S_2.

All switches in MRCs operate with ZVS, which reduces the switching losses and switching noise and eliminates the oscillation due to the parasitic effects of the components (such as the junction capacitance of the diodes). However, all switches are under high current and voltage stresses, resulting in an increase in the conduction loss.

12.7 Zero-voltage-transition Converters

By introducing a resonant circuit in parallel with the switches, the converter can achieve ZVS for both power switch and diode without significantly increasing their voltage and current stresses [23]. Fig. 12.20A shows a buck-type ZVT-PWM converter, and Fig. 12.20B shows the associated waveforms. The converter consists of a main switch S and an auxiliary switch S_1. It can be seen that the voltage and current waveforms of the switches are square-wave-like except during turn-on and turn-off switching intervals, where zero-voltage-transition (ZVT) takes place. The main switch and the output diode are under ZVS and are subjected to low voltage and current stresses. The auxiliary switch is under ZCS, resulting in low switching loss.

The concept of ZVT can be extended to other PWM circuits by adding the resonant circuit. Some basic ZVT-PWM converters are shown in Fig. 12.21.

12.8 Non-dissipative Active Clamp Network

The active-clamp circuit can utilize the transformer leakage inductance energy and can minimize the turn-off voltage stress in the isolated converters. The active-clamp circuit provides a means of achieving ZVS for the power switch and reducing the rate of change of the diode's reverse-recovery current. An example of a flyback converter with active clamp is shown in Fig. 12.22A, and the circuit waveforms are shown in Fig. 12.22B. Clamping action is obtained by using a series combination of an active switch (i.e., S_2) and a large capacitor so that the voltage across the main switch (i.e., S_1) is clamped to a minimum value. S_2 is turned on with ZVS. However, S_2 is turned off with finite voltage and current and has turn-off switching loss. The clamp-mode ZVS-MRCs is discussed in [24–26].

12.9 Load Resonant Converters

Load resonant converters (LRCs) have many distinct features over conventional power converters. Due to the soft commutation of the switches, no turn-off loss or stress is present. LRCs are especially suitable for high-power applications because they allow high-frequency operation for equipment size/weight reduction, without sacrificing the conversion efficiency and imposing extra stress on the switches. Basically, LRCs can be divided into three different configurations, namely, series resonant converters, parallel resonant converters, and series-parallel resonant converters.

12.9.1 Series Resonant Converters

Series resonant converters (SRCs) have their load connected in series with the resonant tank circuit, which is formed by L_r and C_r [15,27–29]. The half-bridge configuration is shown in Fig. 12.23. When the resonant inductor current i_{Lr} is positive, it flows through T_1 if T_1 is on; otherwise, it flows through the diode D_2. When i_{Lr} is negative, it flows through T_2 if T_2 is on; otherwise, it flows through the diode D_1. In the steady-state symmetrical operation, both the active switches are operated in a complementary manner. Depending on the ratio between the switching frequency ω_S and the converter resonant frequency ω_r, the converter has several possible operating modes.

12.9.1.1 Discontinuous Conduction Mode With $\omega_S < 0.5\omega_r$

Fig. 12.24A shows the waveforms of i_{Lr} and the resonant capacitor voltage v_{Cr} in this mode of operation. From 0 to t_1, T_1 conducts. From t_1 to t_2, the current in T_1 reverses its direction. The current flows through D_1 and back to the supply source. From t_2 to t_3, all switches are in the off state. From t_3 to t_4, T_2 conducts. From t_4 to t_5, the current in T_2 reverses its direction. The current flows through D_2 and back to the supply source. T_1 and T_2 are switched on under ZCS condition, and they are switched off under zero-current and zero-voltage conditions. However, the switches are under high current stress in this mode of operation and thus have higher conduction loss.

12.9.1.2 Continuous Conduction Mode With $0.5\omega_r < \omega_S < \omega_r$

Fig. 12.24B shows the circuit waveforms. From 0 to t_1, i_{Lr} transfers from D_2 to T_1. T_1 is switched on with finite switch current and voltage, resulting in turn-on switching loss. Moreover, the diodes must have good reverse-recovery characteristics in order to reduce the reverse-recovery current. From t_1 to t_2, D_1 conducts and T_1 is turned off softly with zero voltage and zero current. From t_2 to t_3, T_2 is switched on with finite switch current and voltage. At t_3, T_2 is turned off softly and D_2 conducts until t_4.

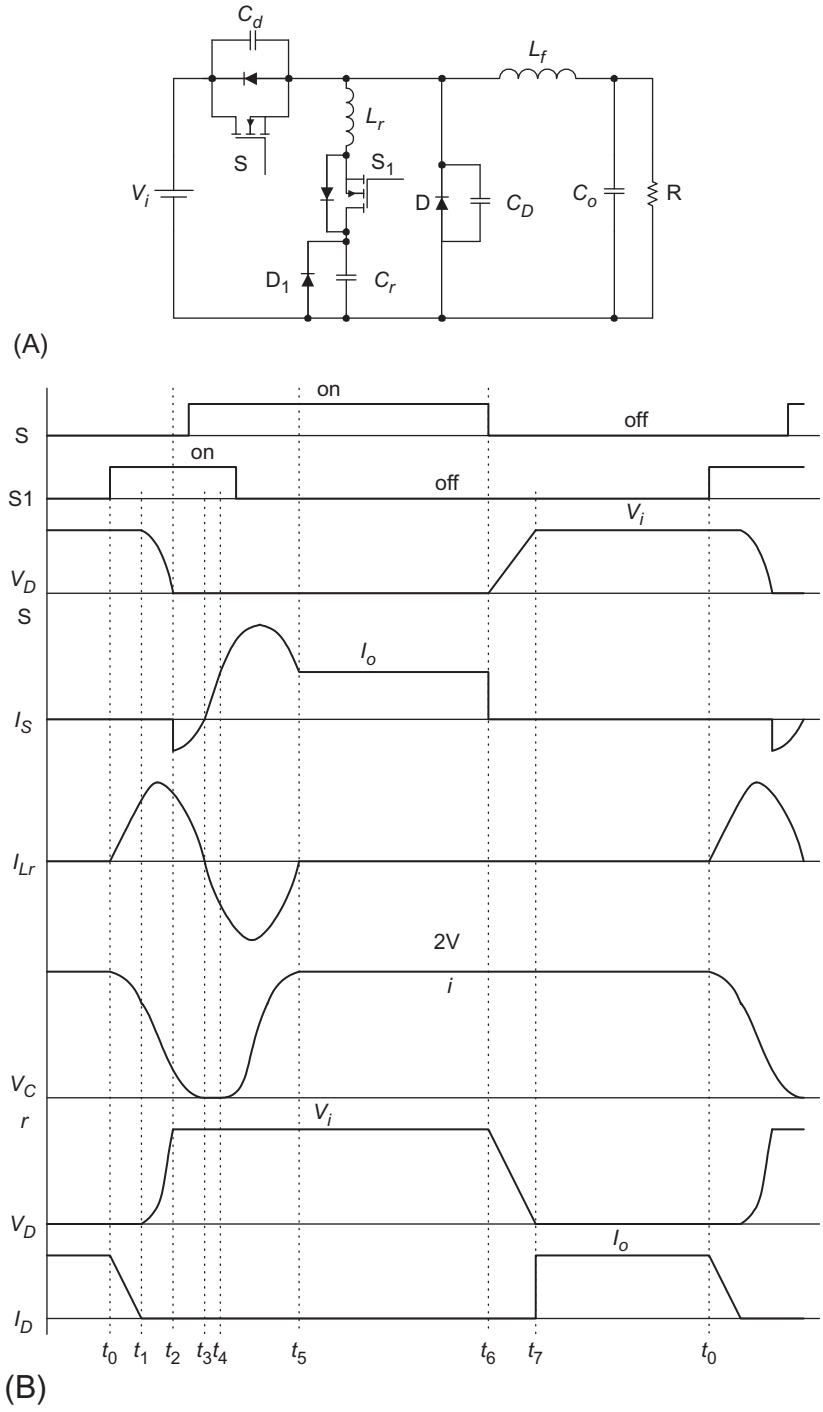


FIG. 12.20 Buck ZVT-PWM converter: (A) circuit schematics and (B) waveforms.

12.9.1.3 Continuous Conduction Mode With $\omega_r < \omega_S$

Fig. 12.24C shows the circuit waveforms. From 0 to t_1, i_{Lr} transfers from D_1 to T_1. Thus, T_1 is switched on with zero current and zero voltage. At t_1, T_1 is switched off with finite voltage and current, resulting in turn-off switching loss. From t_1 to t_2, D_2 conducts. From t_2 to t_3, T_2 is switched on with zero current and zero voltage. At t_3, T_2 is switched off. i_{Lr} transfers from T_2 to D_1. As the switches are turned on with ZVS, lossless snubber capacitors can be added across the switches.

The following parameters are defined: voltage conversion ratio M, characteristic impedance Z_r, resonant frequency f_r, normalized load resistance r, normalized switching frequency γ.

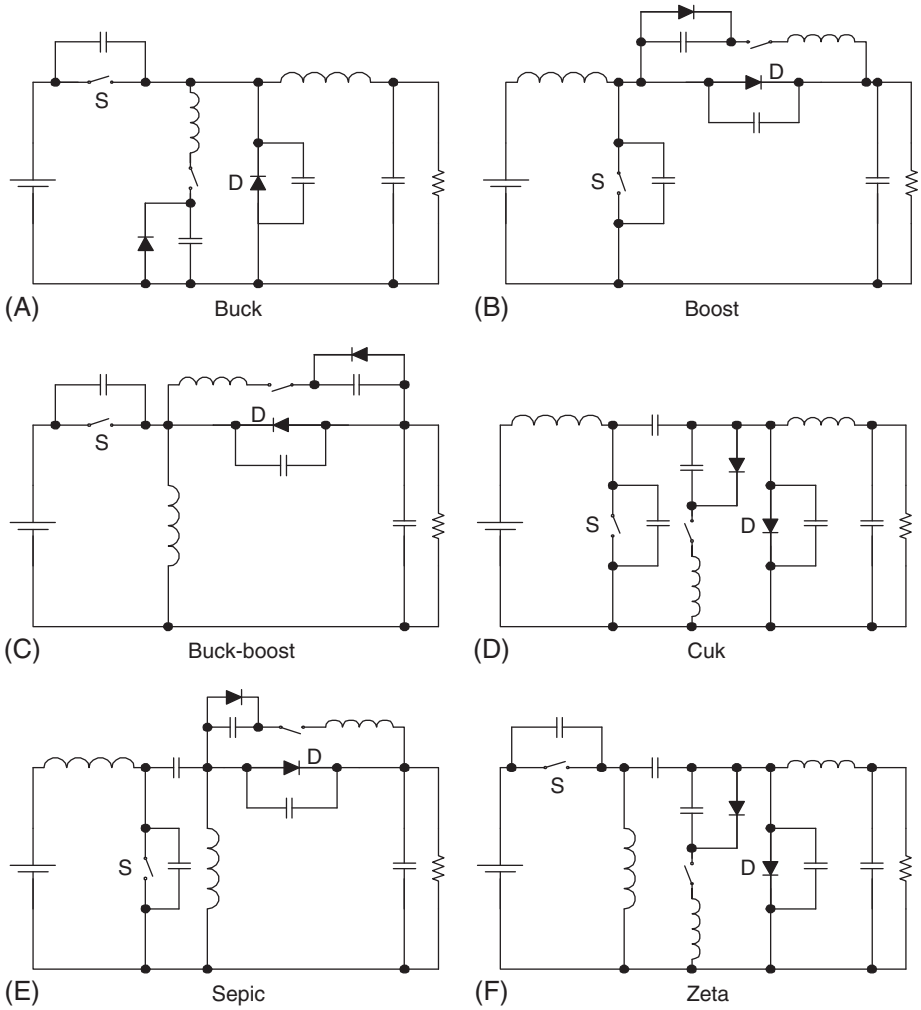


FIG. 12.21 Conventional ZVT-PWM converters. (A) Buck converter. (B) Boost converter. (C) Buck-boost converter. (D) Cuk converter. (E) SEPIC. (F) ZETA converter.

$$M = nV_o/V_{in} \tag{12.2A}$$

$$Z_r = \sqrt{L_r/C_r} \tag{12.2B}$$

$$f_r = 1/\left(2\pi\sqrt{L_rC_r}\right) \tag{12.2C}$$

$$r = n^2R_L/Z_r \tag{12.2D}$$

$$\gamma = f_s/f_r \tag{12.2E}$$

$$M = 1/\sqrt{(\gamma - 1/\gamma)^2/\left(r^2+1\right)} \tag{12.2F}$$

The relationships between M and γ for different value of r are shown in Fig. 12.25. The boundary between continuous conduction mode (CCM) and discontinuous conduction mode (DCM) is at $r = 1.27\gamma$. When the converter is operating in DCM and $0.2 < \gamma < 0.5$, $M = 1.27r\gamma$.

The SRC has the following advantages. Transformer saturation can be avoided since the series capacitor can block the DC component. The light-load efficiency is high because the device current and conduction loss are low. However, the major disadvantages are that there is difficulty in regulating the output voltage under light-load and no-load conditions. Moreover, the output DC filter capacitor has to carry high ripple current, which could be a major problem in low-output-voltage and high-output-current applications [29].

12.9.2 Parallel Resonant Converters

Parallel resonant converters (PRCs) have their load connected in parallel with the resonant tank capacitor C_r [27–30]. The half-bridge configuration is shown in Fig. 12.26. SRC behaves as a current source, whereas the PRC acts as a voltage source. For voltage regulation, PRC requires a smaller operating frequency range than the SRC to compensate for load variation.

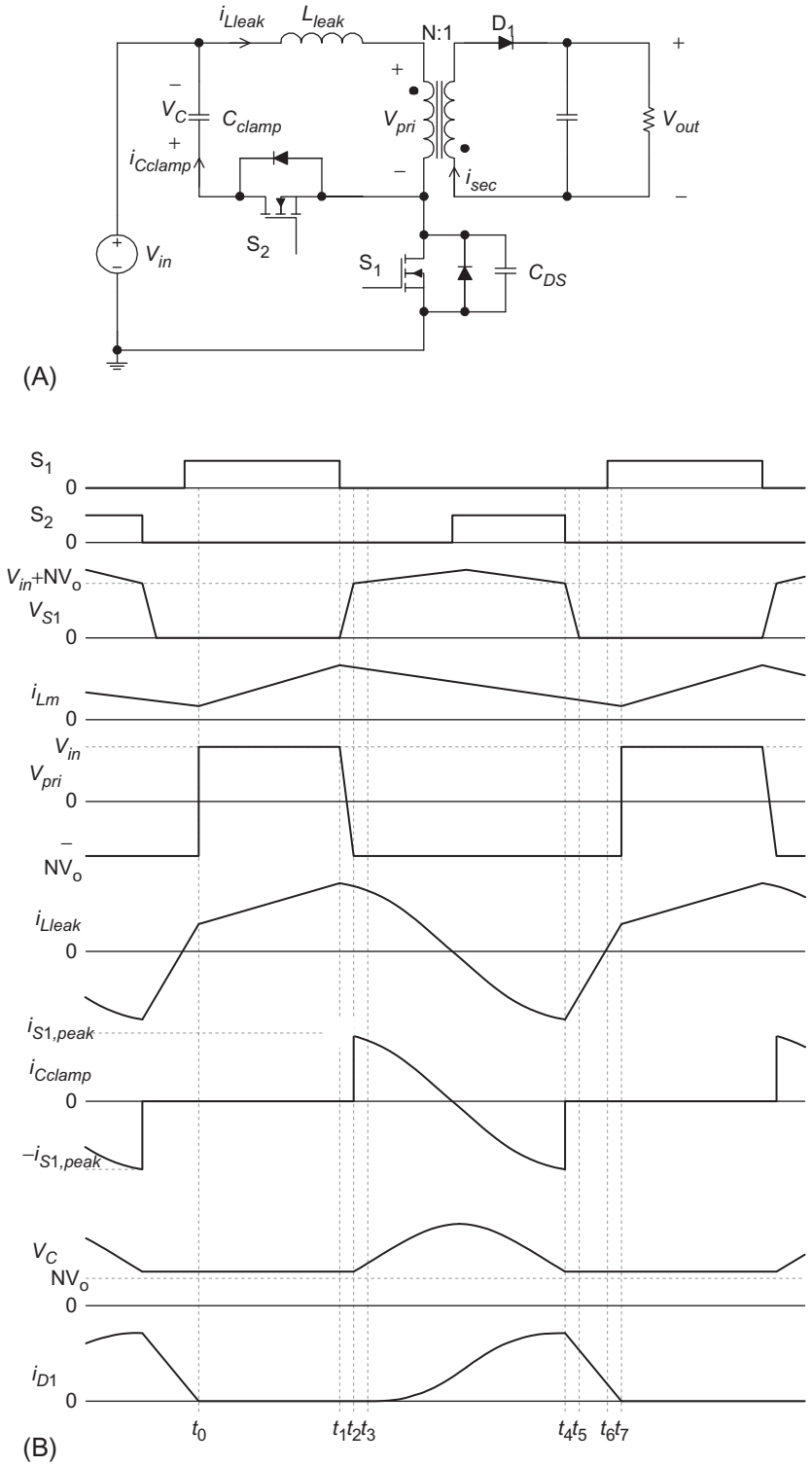


FIG. 12.22 Active-clamp flyback converter: (A) circuit schematics and (B) circuit waveforms.

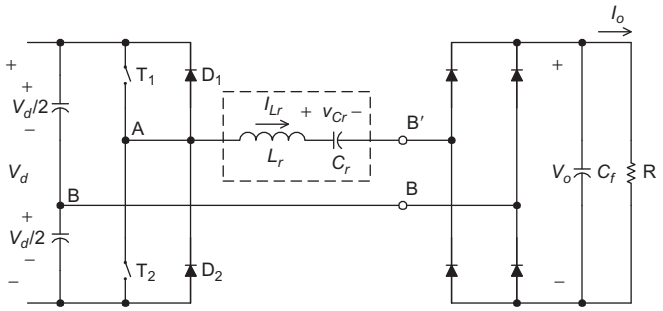


FIG. 12.23 SRC half-bridge configuration.

12.9.2.1 Discontinuous Conduction Mode

The steady-state waveforms of the resonant inductor current i_{Lr} and the resonant capacitor voltage v_{Cr} are shown in Fig. 12.27A. Initially, both i_{Lr} and v_{Cr} are zero. From 0 to t_2, T_1 conducts and is turned on with zero current. When i_{Lr} is less than the output current I_o, i_{Lr} increases linearly from 0 to t_1 and the output current circulates through the diode bridge. From t_1 to t_3, L_r resonates with C_r. Starting from t_2, i_{Lr} reverses its direction and flows through D_1. T_1 is then turned off with zero current and zero voltage. From t_3 to t_4, v_{Cr} decreases linearly due to the relatively constant value of I_o. At t_4, when v_{Cr} equals zero, the output current circulates through the diode bridge again. Both i_{Lr} and v_{Cr} will stay at zero for an interval. From t_5 to t_9, the above operations will be repeated for T_2 and D_2. The output voltage is controlled by adjusting the time interval of $[t_4, t_5]$.

12.9.2.2 Continuous Conduction Mode $\omega_S < \omega_r$

This mode is similar to the operation in the DCM but with a higher switching frequency. Both i_{Lr} and v_{Cr} become continuous. The waveforms are shown in Fig. 12.27B. The switches T_1 and T_2 are hard turned on with finite voltage and current and are soft turned off with ZVS.

12.9.2.3 Continuous Conduction Mode $\omega_S > \omega_r$

If the switching frequency is higher than ω_r (Fig. 12.27C), the antiparallel diode of the switch will be turned on before the switch is triggered. Thus, the switches are turned on with ZVS. However, the switches are hard turned off with finite current and voltage.

The parameters defined in Eq. (12.2) are applicable. The relationships between M and γ for various values of r are shown in Fig. 12.28. During the DCM (i.e., $\gamma < 0.5$), M is in linear relationship with γ. Output voltage regulation can be achieved easily. The output voltage is independent on the output current. The converter shows good voltage-source characteristics. It is also possible to step up and step down the input voltage.

The PRC has the advantages that the load can be short-circuited and the circuit is suitable for low-output-voltage, high-output-current applications. However, the major disadvantage of the PRC is the high device current. Moreover, since the device current does not decrease with the load, the efficiency drops with a decrease in the load [29].

12.9.3 Series-Parallel Resonant Converter

Series-parallel resonant converter (SPRC) combines the advantages of the SRC and PRC. The SPRC has an additional capacitor or inductor connected in the resonant tank circuit [29–31]. Fig. 12.29A shows an LCC-type SPRC, in which an additional capacitor is placed in series with the resonant inductor. Fig. 12.29B shows an LLC-type SPRC, in which an additional inductor is connected in parallel with the resonant capacitor in the SRC. However, there are many possible combinations of the resonant tank circuit. Detailed analysis can be found in [31].

12.10 Control Circuits for Resonant Converters

Since the 1985s, various control integrated circuits (ICs) for resonant converters have been developed. Some common ICs for different converters are described in this section.

12.10.1 QRCs and MRCs

Output regulations in many resonant-type converters, such as QRCs and MRCs, are achieved by controlling the switching frequency. ZCS applications require controlled switch-on times, while ZVS applications require controlled switch-off times. The fundamental control blocks in the IC include an error amplifier, voltage-controlled oscillator (VCO), one-shot generator with a zero wave-crossing detection comparator, and an output stage to drive the active switch. Typical ICs include UC1861-UC1864 for ZVS applications and UC 1865-UC 1868 for ZCS applications [32]. Fig. 12.30 shows the controller block diagram of UC 1864.

The maximum and minimum switching frequencies (i.e., f_{max} and f_{min}) are controlled by the resistors R_{ange} and R_{min} and the capacitor C_{vco}. f_{max} and f_{min} can be expressed as

$$f_{\max} = \frac{3.6}{(R_{ange} // R_{\min}) C_{VCO}} \quad \text{and} \quad f_{\min} = \frac{3.6}{R_{\min} C_{VCO}} \tag{12.3}$$

The frequency range Δf is then equal to

$$\Delta f = f_{\max} - f_{\min} = \frac{3.6}{R_{ange} C_{VCO}} \tag{12.4}$$

The frequency range of the ICs is from 10 kHz to 1 MHz. The output frequency of the oscillator is controlled by the error amplifier (E/A) output. An example of a ZVS-MR forward converter is shown in Fig. 12.31.

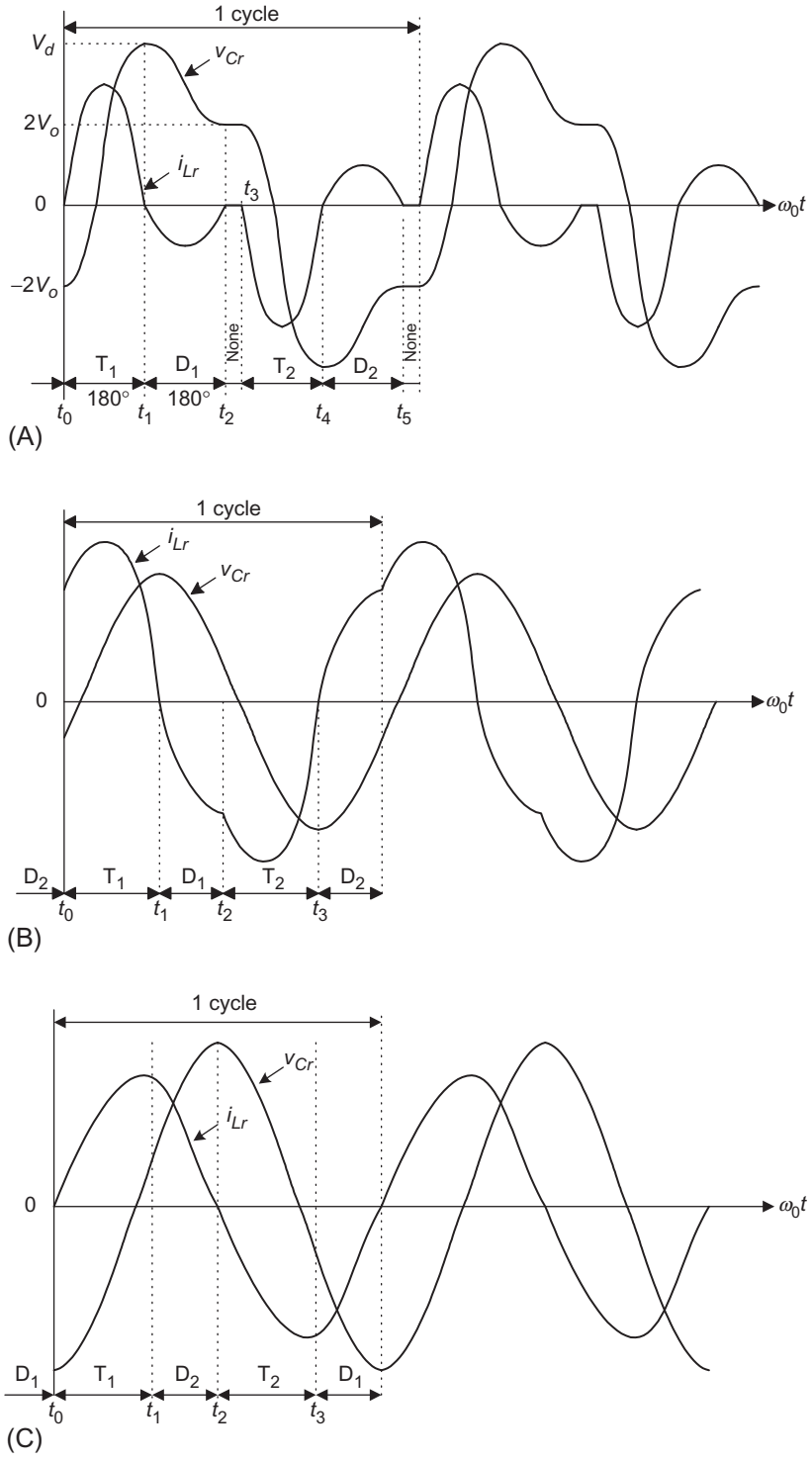


FIG. 12.24 Circuit waveforms under different operating conditions: (A) $\omega_S < 0.5\omega_r$, (B) $0.5\ \omega_r < \omega_S < \omega$, and (C) $\omega_r < \omega_S$.

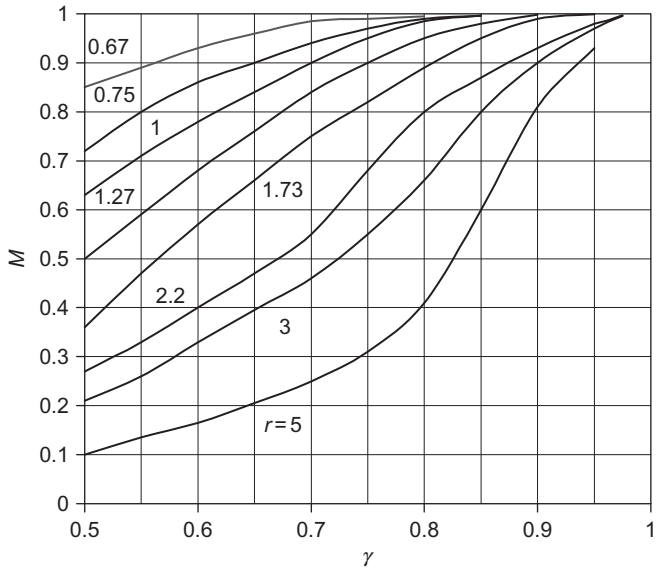


FIG. 12.25 M vs γ in SRC.

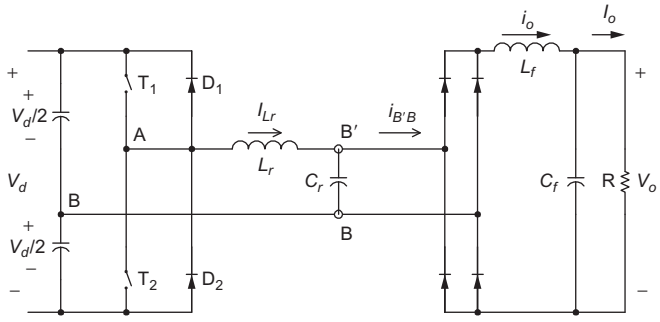


FIG. 12.26 PRC half-bridge configuration.

12.10.2 Phase-shifted, ZVT FB Circuit

The UCC3895 is a phase-shift PWM controller that can generate a phase-shifting pattern of one half-bridge with respect to the other. The application diagram is shown in Fig. 12.32.

The four outputs "OUTA," "OUTB," "OUTC," and "OUTD" are used to drive the MOSFETs in the full-bridge. The dead time between "OUTA" and "OUTB" is controlled by "DELAB," and the dead time between "OUTC" and "OUTD" is controlled by "DELCD." Separate delays are provided for the two half-bridges to accommodate differences in resonant capacitor charging currents. The delay in each set is approximated by

$$t_{DELAY} = \frac{25 \times 10^{-12} R_{DEL}}{0.75(V_{CS} - V_{ADS}) + 0.5} + 25\,ns \qquad (12.5)$$

where R_{DEL} is the resistor value connected between "DELAB" and "DELCD" to ground.

The oscillator period is determined by R_T and C_T. It is defined as

$$t_{OSC} = \frac{5R_TC_T}{48} + 120\,ns \qquad (12.6)$$

The maximum operating frequency is 1 MHz. The phase shift between the two sets of signals is controlled by the ramp voltage and the error amplifier output having a 7-MHz bandwidth.

12.11 Extended-Period Quasi-Resonant Converters

Generally, resonant and quasi-resonant converters operate with frequency control. The extended-period quasi-resonant (EP-QR) converters proposed by Barbi [33] offer a simple solution to modify existing hard-switched converters into soft-switched ones with constant frequency operation. This makes both output filter design and control simple. Fig. 12.33 shows a standard hard-switched boost-type PFC converter. In this hard-switched circuit, the main switch SW1 could be subject to significant switching stress because the reverse-recovery current of the diode D_F could be excessive when SW1 is turned on. In practice, a small saturable inductor may be added in series with the power diode D_F in order to reduce the di/dt of the reverse-recovery current. In addition, an optional R-C snubber may be added across SW1 to reduce the dv/dt of SW1. These extra reactance components can in fact be used in the EP-QR circuit to achieve soft switching, as shown in Fig. 12.34. The resonant components L_r and C_r are of small values and can come from the snubber circuits of a standard hard-switched converter. Thus, the only additional component is the auxiliary switch Q2. The small resonant inductor is put in series with the main switch SW1 so that SW1 can be switched on under ZC condition and the di/dt problem of the reverse-recovery current be eliminated. The resonant capacitor C_r is used to store energy for creating condition for soft switching. Q2 is used to control the resonance during the main switch transition. It should be noted that all power devices including SW1, Q1, and main power diode D_F are turned on and off under ZV and/or ZC conditions. Therefore, the large di/dt problem due to the reverse recovery of the power diode can be eliminated. The soft-switching method is an effective technique for EMI suppression.

Together with power factor correction technique, soft-switching converters offer a complete solution to meet EMI regulations for both conducted and radiated EMI. The operation of the EP-QR boost PFC circuit [34,35] can be described in six modes as shown in Fig. 12.35. The corresponding idealized waveforms are included in Fig. 12.36.

12.11.0.1 Circuit Operation

Interval I: ($t_0 - t_1$). Due to the resonant inductor L_r limits the di/dt of the switch current, switch SW1 is turned on at zero-current condition with a positive gating signal V_{GS1} to start a switching cycle at $t = t_0$. Current in D_F is diverted to

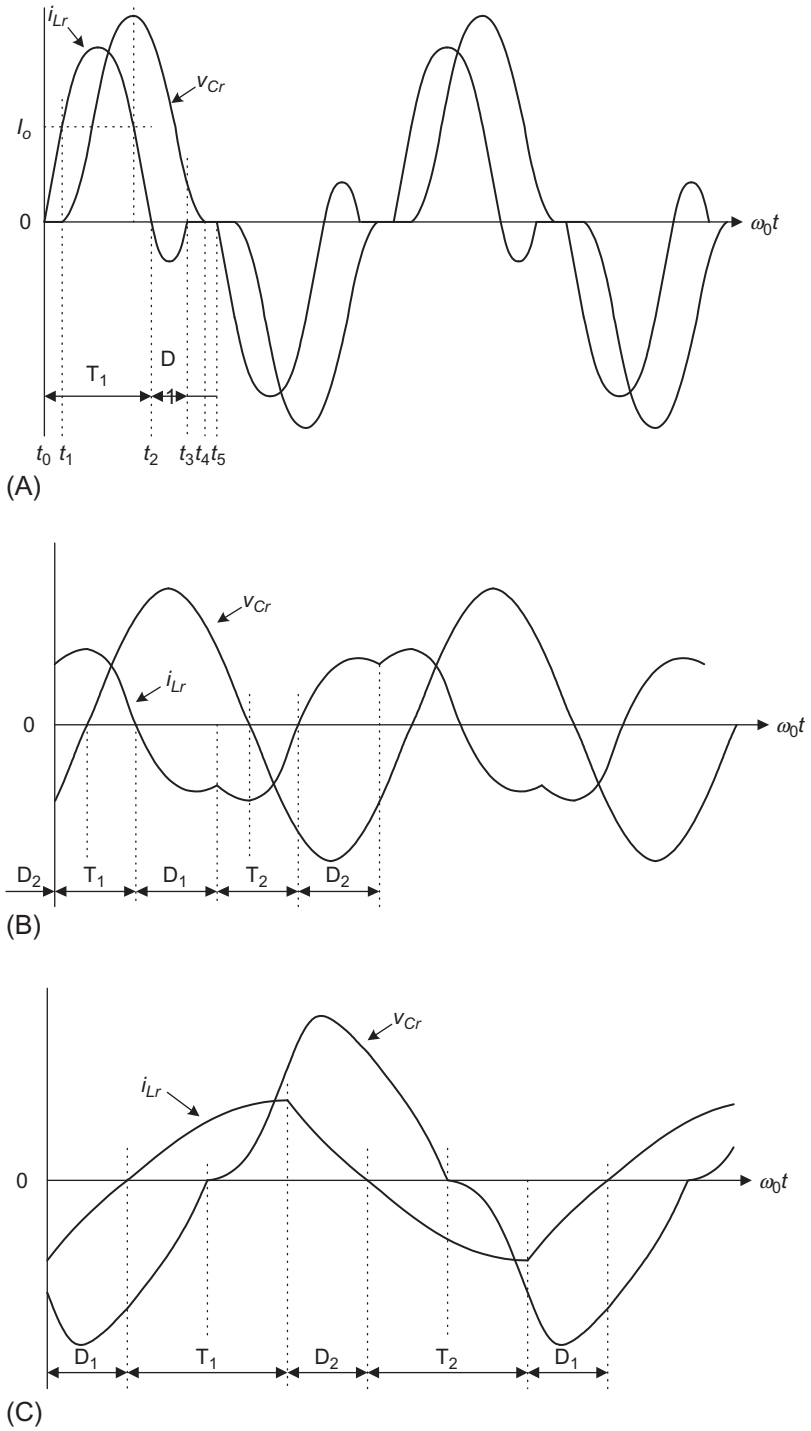


FIG. 12.27 Circuit waveforms under different operating conditions: (A) discontinuous conduction mode, (B) continuous conduction mode $\omega_S < \omega_r$, and (C) continuous conduction mode $\omega_S > \omega_r$.

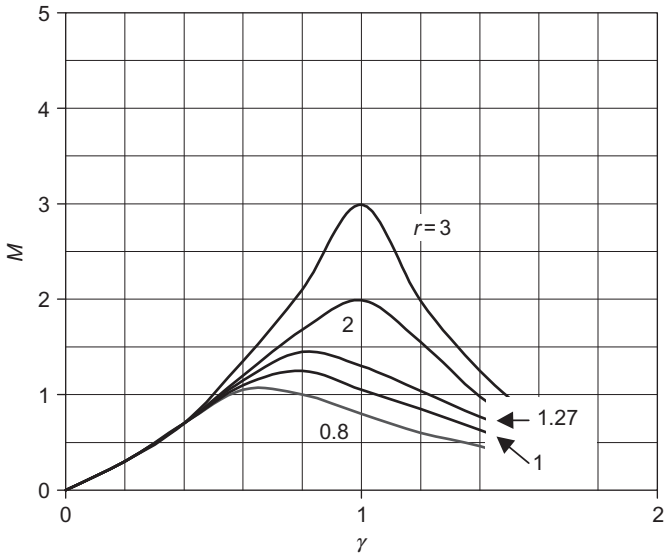


FIG. 12.28 M versus γ in PRC.

inductor L_r. Because D_F is still conducting during this short period, D_{S2} is still reverse-biased and is thus not conducting. The equivalent circuit topology for the conducting paths is shown in Fig. 12.35A. Resonant switch Q_2 remains off in this interval.

Interval II: $(t_1 - t_a)$. When D_F regains its blocking state, D_{S2} becomes forward-biased. The first half of the resonance cycle occurs and resonant capacitor C_r starts to discharge, and current flows in the loop C_r-Q_2-L_r-SW_1. The resonance half cycle stops at time $t = t_a$ because D_{S2} prevents the loop current i_{Cr} from flowing in the opposition direction. The voltage across C_r is reversed at the end of this interval. The equivalent circuit is shown in Fig. 12.35B.

Interval III: $(t_a - t_b)$. Between t_a and t_b, current in L_F and L_r continues to build up. This interval is the extended period for the resonance during which energy is pumped into L_r. The corresponding equivalent circuit is shown in Fig. 12.35C.

Interval IV: $(t_b - t_2)$. Fig. 12.35D shows the equivalent circuit for this operating mode. Before SW_1 is turned off, the second half of the resonant cycle needs to take place in order that a zero-voltage condition can be created for the turn-off process of SW_1. The second half of the resonant cycle starts

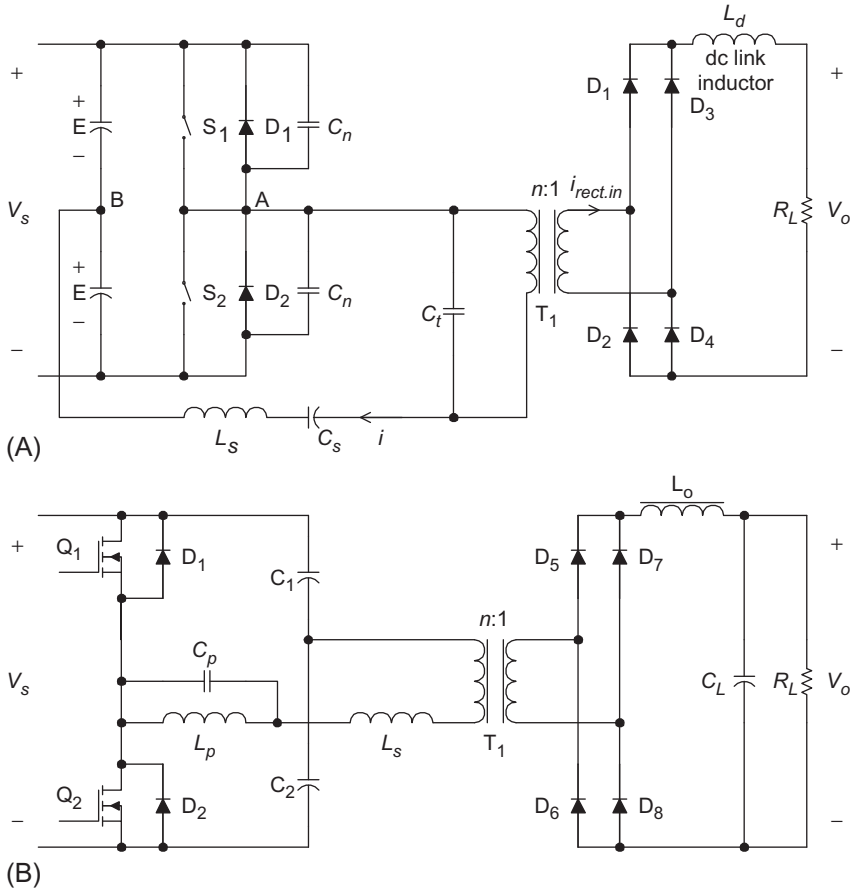


FIG. 12.29 Different types of SPRC: (A) LCC-type and (B) LLC-type.

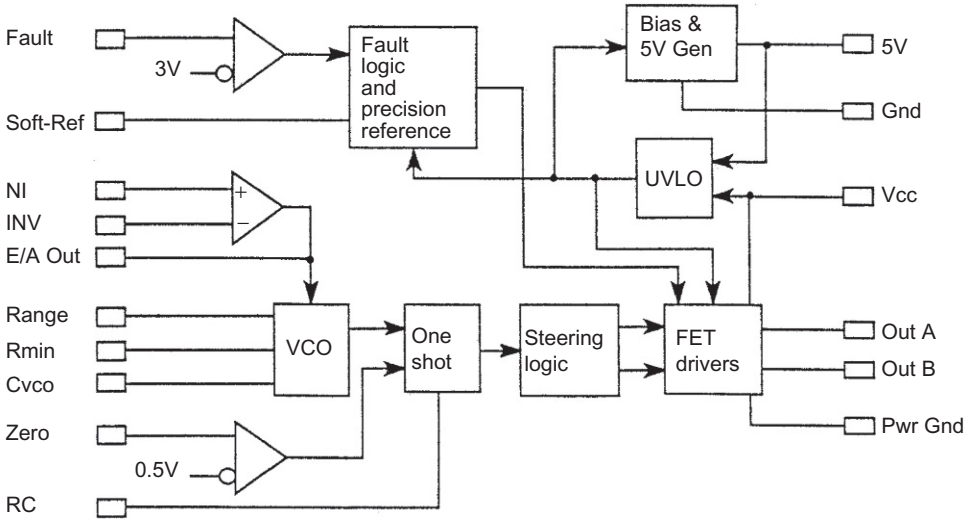


FIG. 12.30 Controller block diagram of UC1864. Courtesy of Unitrode Corp. and Texas Instruments.

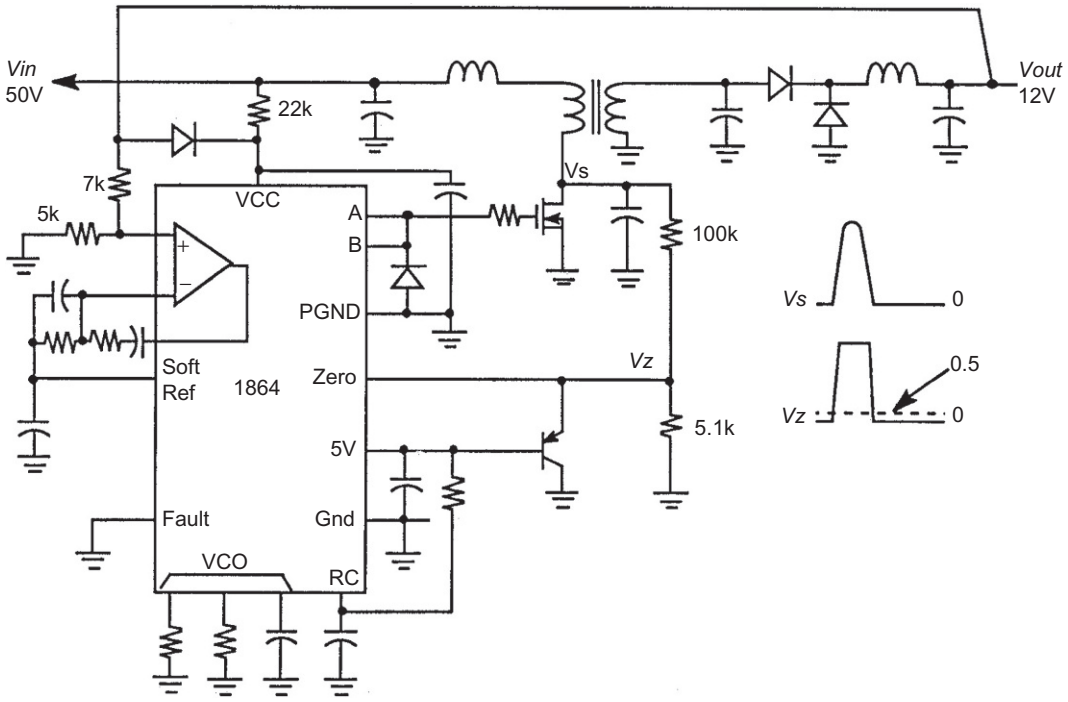


FIG. 12.31 ZV-MR forward converter. Courtesy of Unitrode Corp. and Texas Instruments.

when auxiliary switch Q_2 is turned on at $t = t_b$. Resonant current then flows through the loop L_r-Q_2-C_r-antiparallel diode of SW_1. This current is limited by L_r, and thus, Q_2 is turned on under zero-current condition. Since the antiparallel diode of SW_1 is conducting, the voltage across SW_1 is clamped to the on-state voltage of the antiparallel diode. SW_1 can therefore be turned off at (near) zero-voltage condition before $t = t_2$ at which the second half of the resonant cycle ends.

Interval V: ($t_2 - t_3$). During this interval, the voltage across C_r is less than the output voltage V_o. Therefore, D_F is still reverse-biased. Inductor current I_s flows into C_r until V_{Cr} reaches V_o at $t = t_3$. The equivalent circuit is represented in Fig. 12.35E.

Interval VI: ($t_3 - t_4$). During this period, the resonant circuit is not in action, and the inductor current I_s charges the output capacitor C_F via D_F, as in the case of a classical boost-type PFC circuit. C_r is charged to V_o; therefore, Q_2 can be turned

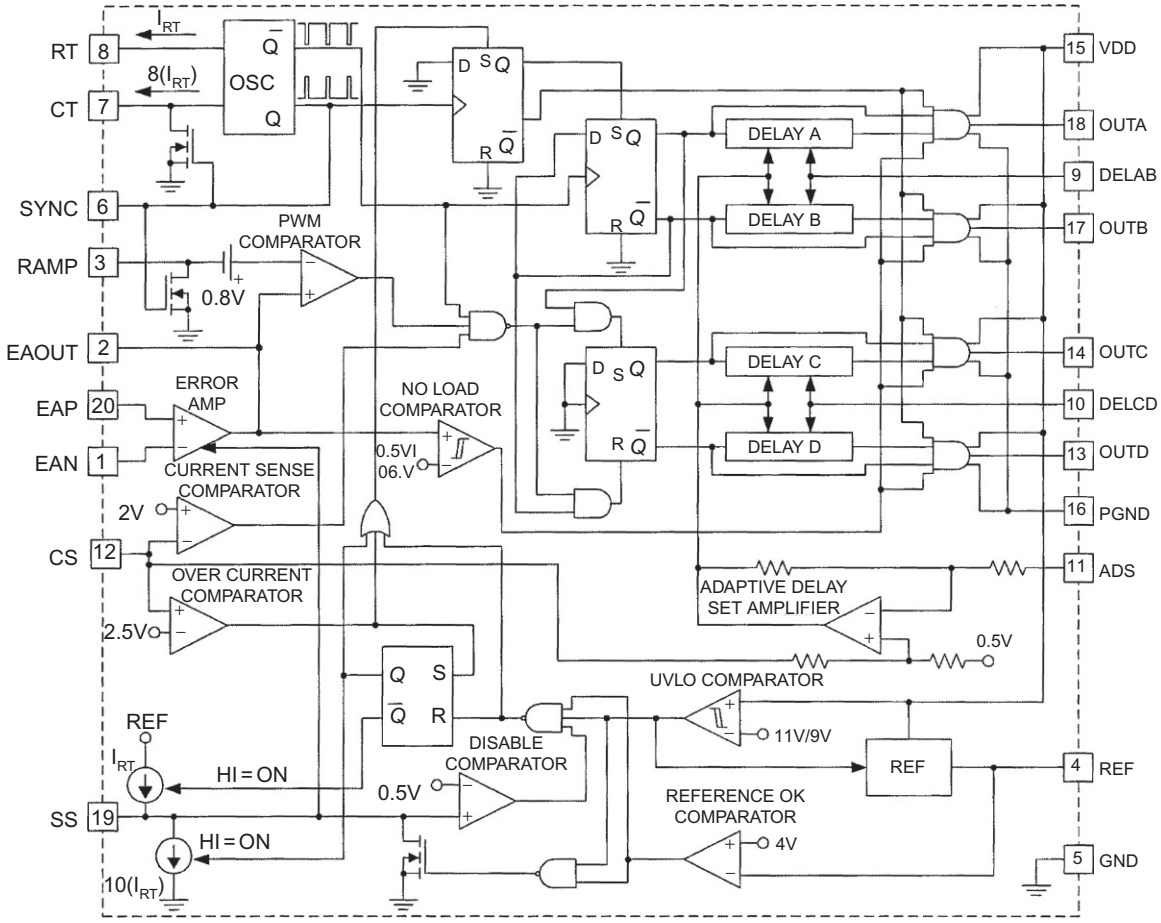


FIG. 12.32 Application diagram of UCC3895. Courtesy of Unitrode Corp. and Texas Instruments.

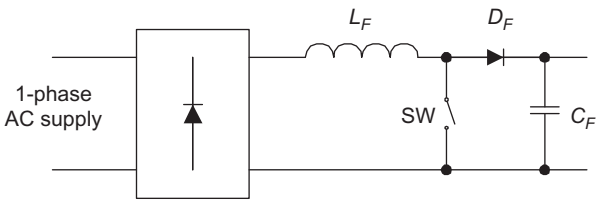


FIG. 12.33 Boost-type AC-DC power factor correction circuit.

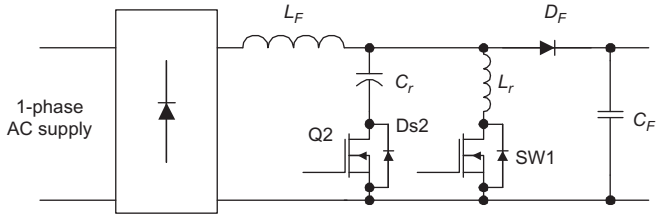


FIG. 12.34 EP-QR boost-type AC-DC power factor correction circuit.

off at zero-voltage and zero-current conditions. Fig. 12.35F shows the equivalent topology of this operating mode.

In summary, SW1, Q2, and D_F are fully soft-switched. Since the two resonance half cycles take place within a closed loop outside the main inductor, the high resonant pulse will not occur in the inductor current, thus making a well-established averaged current mode control technique applicable for such QR circuit. For full soft switching in the turn-off process, the resonant components need to be designed so that the peak resonant current exceeds the maximum value of the inductor current. Typical measured switching waveforms and trajectories of SW1, Q2, and D_F are shown in Figs. 12.37, 12.38, and 12.39, respectively.

12.11.0.2 Design Procedure

Given: Input AC voltage = V_s (V)
Peak AC voltage = $V_s(max)$ (V)
Nominal output DC voltage = V_o (V)
Switching frequency = f_{sw} (Hz)
Output power = P_o (W)

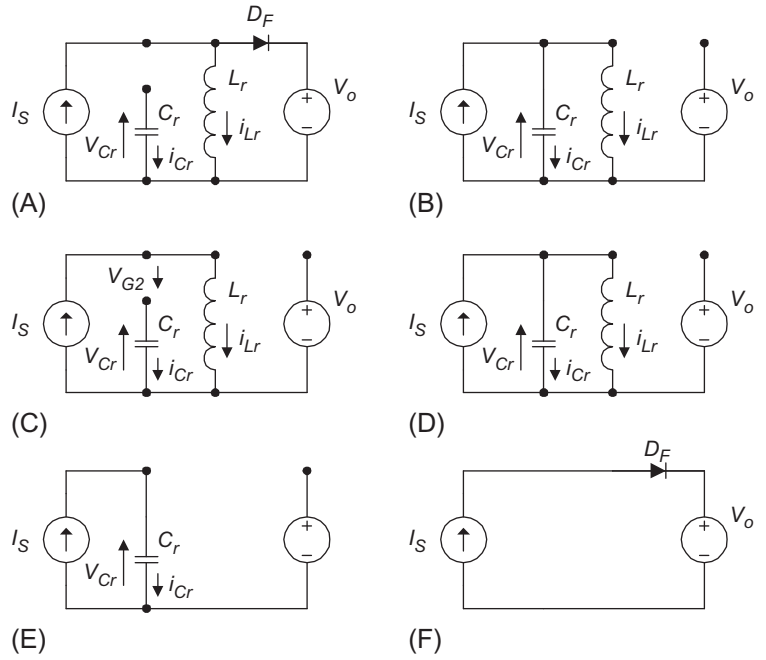


FIG. 12.35 Operating modes of EP-QR boost-type AC-DC power factor correction circuit. (A) Mode I. (B) Mode II. (C) Mode III. (D) Mode IV. (E) Mode V. (F) Mode VI.

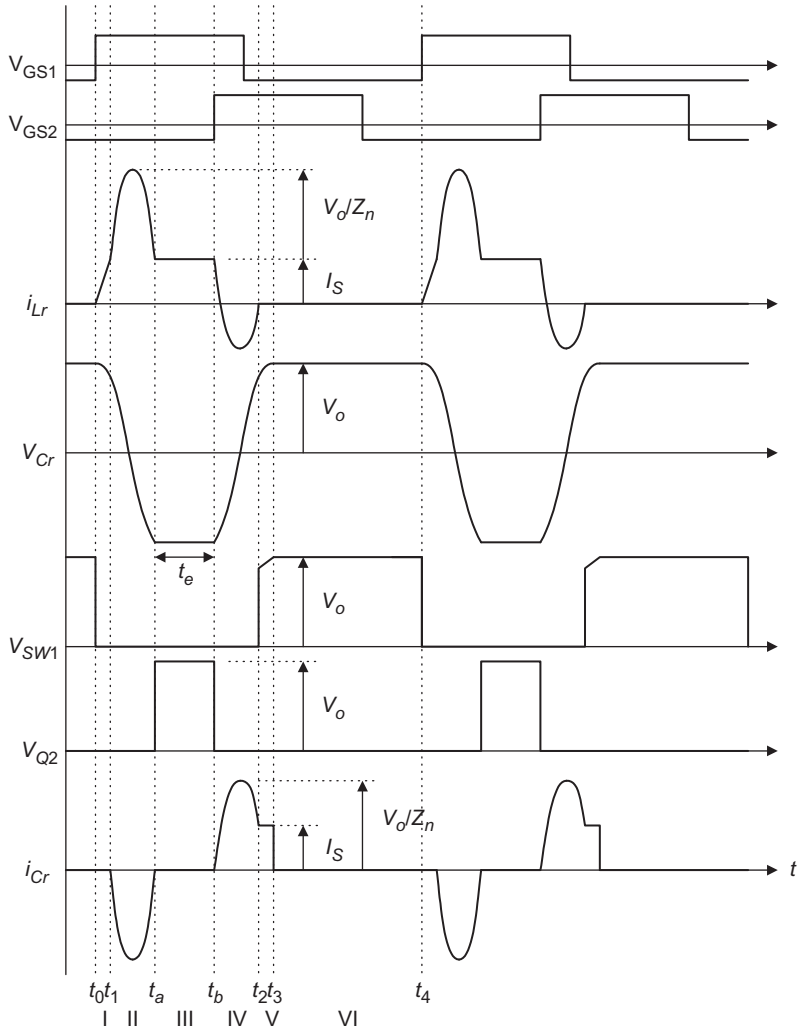


FIG. 12.36 Idealized waveforms of EP-QR boost-type AC-DC power factor correction circuit.

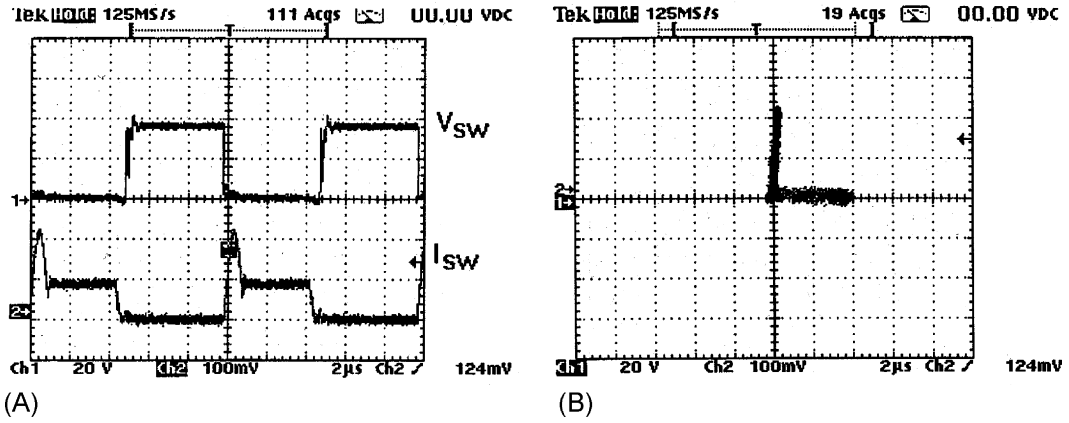


FIG. 12.37 (A) Drain-source voltage and current of SW1 and (B) switching locus of SW1.

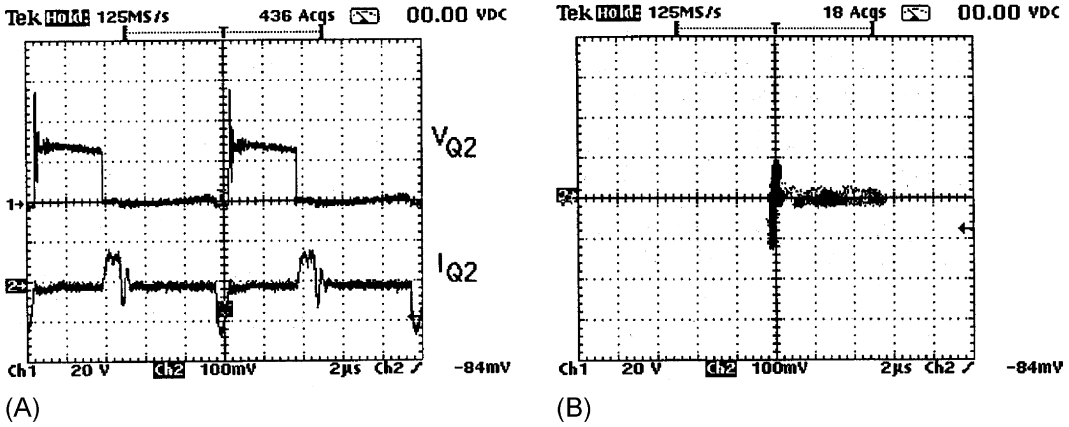


FIG. 12.38 (A) Drain-source voltage and current of Q2 and (B) switching locus of Q2.

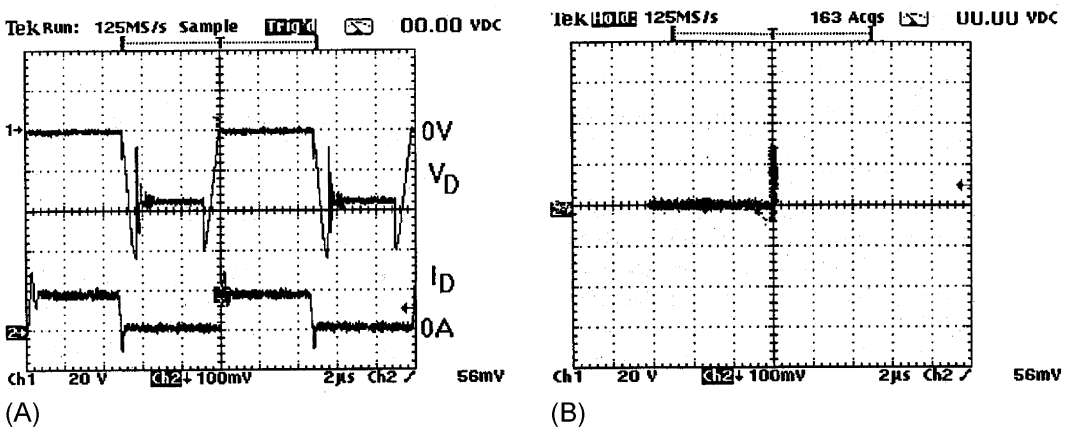


FIG. 12.39 (A) Diode voltage and current and (B) switching locus of diode.

Input current ripple = ΔI (A)
Output voltage ripple = ΔV (V)

(I) Resonant tank design:

Step 1. Because the peak resonant current must be greater than the peak inductor current (same as peak input line current) in order to achieve soft turnoff, it is necessary to determine the peak input current $I_s(max)$. Assuming lossless AC-DC power conversion, $I_s(max)$ can be estimated from the following equation:

$$I_{s(\max)} \approx \frac{2V_oI_o}{V_{s(\max)}} \tag{12.7}$$

where $I_o = P_o/V_o$ is the maximum output current.

Step 2. Soft-switching criterion is

$$Z_r \le \frac{V_o}{I_{s(\max)}} \tag{12.8}$$

where $Z_r = \sqrt{\frac{L_r}{C_r}}$ is the impedance of the resonant tank.

For a chosen resonant, frequency f_r, L_r, and C_r can be obtained from

$$2\pi f_r = \frac{1}{\sqrt{L_rC_r}} \tag{12.9}$$

(II) Filter component design:

The minimum conversion ratio is

$$M_{(\max)} = \frac{V_o}{V_{s(\max)}} = \frac{1}{1-\left(\frac{f_{sw}}{f_r}+\frac{t_e}{T_{sw}}\right)} \tag{12.10}$$

where $T_{sw} = 1/f_{sw}$ and t_e is the extended period. From Eq. (12.10), minimum t_e can be estimated.

The turn-on period of the SW1 is

$$T_{on}(sw1) = t_e + 1/f_r \tag{12.11}$$

Inductor value L is obtained from

$$L \ge \left(\frac{T_{on(sw1)}}{\Delta I}\right)V_{s(\max)} \tag{12.12}$$

The filter capacitor value C can be determined from

$$C\left(\frac{\Delta V}{\frac{T_s}{\pi}\sin^{-1}\left(\frac{I_o}{I_{s(\max)}}\right)}\right) = I_o \tag{12.13}$$

where $T_s = 1/f_s$ is the period of the AC voltage supply frequency.

12.11.1 Soft-Switched DC-DC Flyback Converter

A simple approach that can turn an existing hard-switched converter design into a soft-switched one is shown in Fig. 12.40. The key advantage of the proposal is that many well proved and reliable hard-switched converter designs can be kept. The modification required is the addition of a simple circuit (consisting an auxiliary winding, a switch, and a small capacitor) to an existing isolated converter [36]. This principle, which is the modified version of the EPQR technique for isolated converter, is demonstrated in an isolated soft-switched flyback converter with multiple outputs. Other advantageous features of the proposal are as follows:

- All switches and diodes of the converter are "fully" soft-switched, that is, soft-switched at both turn-on and turn-off transitions under zero-voltage and/or zero-current conditions.
- The leakage inductance of each winding in the flyback transformer forms part of the resonant circuit for achieving ZVS and ZCS of all switches and diodes.
- The control technique is simply PWM-based as in standard hard-switched converters.
- The soft-switched technique is a proved method for EMI reduction [37].

12.11.2 A ZCS Bidirectional Flyback DC-DC Converter

A bidirectional flyback DC-DC converter that uses one auxiliary circuit for both power flow directions is proposed in Fig. 12.41 [38]. The methodology is based on extending the unidirectional soft-switched flyback converter in Ref. [36] and replacing the output diode with a controlled switch, which acts as either a rectifier [39] or a power control switch in the corresponding power flow direction. An auxiliary circuit that consists of a winding in the coupled inductor, a switch, and a capacitor converts the hard-switched design into a soft-switched one. The operation is the same as [36] in the forward mode. An extended-period resonant stage [34] is introduced when the power control switch is on. Conversely, in the reverse mode, a complete resonant stage is initiated before the main switch is off. In both the power flow operations, the leakage inductance of the coupled inductor is used to create zero-current switching conditions for all switches.

12.12 Soft-Switching and EMI Suppression

A family of EP-QR converters are displayed in Fig. 12.42. Their radiated EMI emissions have been compared with that from their hard-switched counterparts [37]. Fig. 12.43A and B shows the conducted EMI emission from a hard-switched flyback

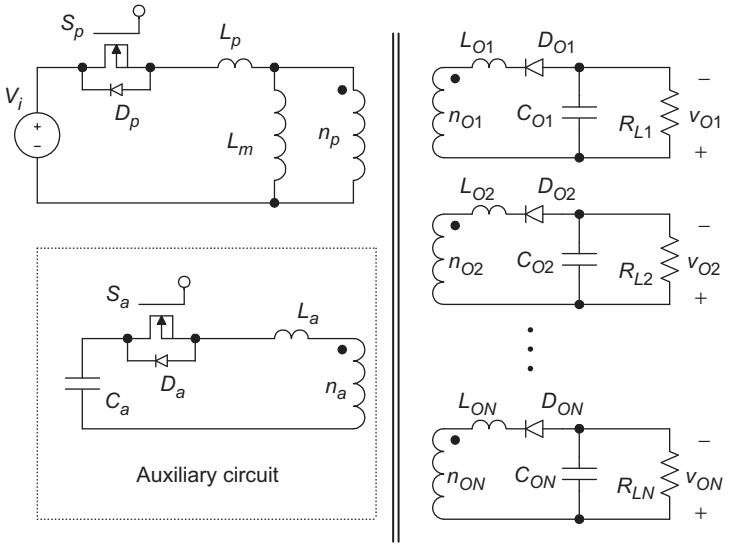


FIG. 12.40 Fully soft-switched isolated flyback converter.

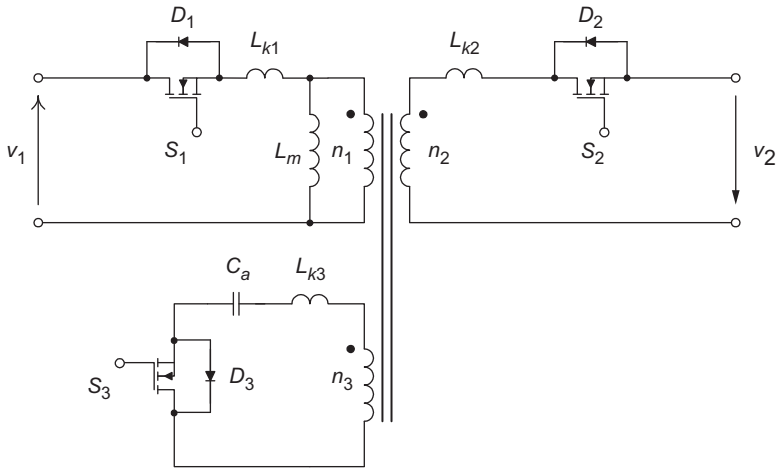


FIG. 12.41 Bidirectional soft-switched isolated flyback converter.

converter and a soft-switched one, respectively. Their radiated EMI emissions are included in Fig. 12.44. Both converters are tested at an output power of 50 W. No special filtering or shielding measures have been taken during the measurement. It is clear from the measurements that soft switching is an effective means to EMI suppression.

12.13 Snubbers and Soft-Switching for High Power Devices

Today, most of the medium power (up to 200 kVA) and medium voltage (up to 800 V) inverter are hard-switched. Compared with low-power switched-mode power supplies, the high voltage involved in the power inverters makes the *dv/dt*, *di/dt*, and the switching stress problems more serious. In addition, the reverse recovery of power diodes in the inverter leg may cause very sharp current spike, leading to severe EMI problem. It should be noted that some high-power devices such as GTO thyristors do not have a square safe operating area (SOA). It is therefore essential that the switching stress they undergone must be within their limits. Commonly used protective measures are to use snubber circuits for protecting high-power devices.

Among various snubbers, two snubber circuits are most well-known for applications in power inverters. They are the Undeland snubber [40] (Fig. 12.45) and McMurray snubber circuits [41] (Fig. 12.46). The Undeland snubber is an asymmetrical snubber circuit with one turn-on inductor and one

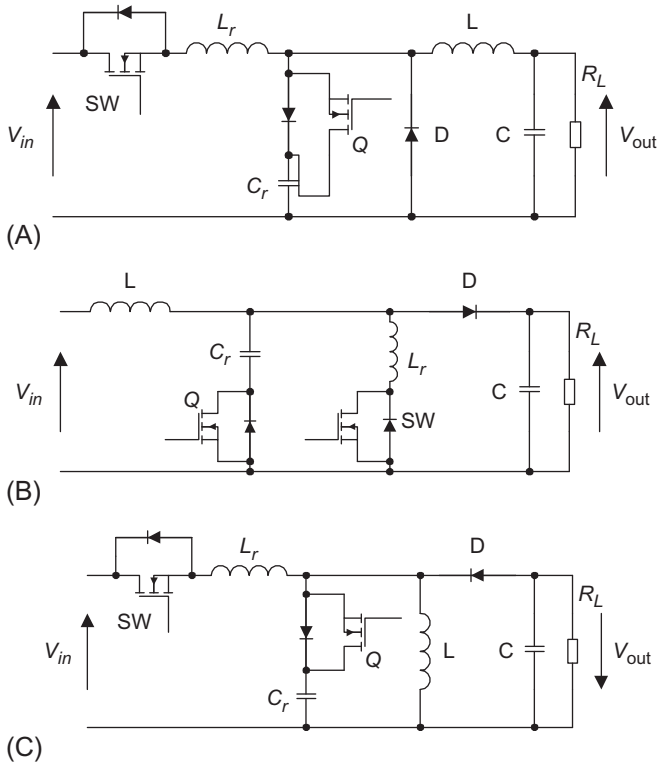


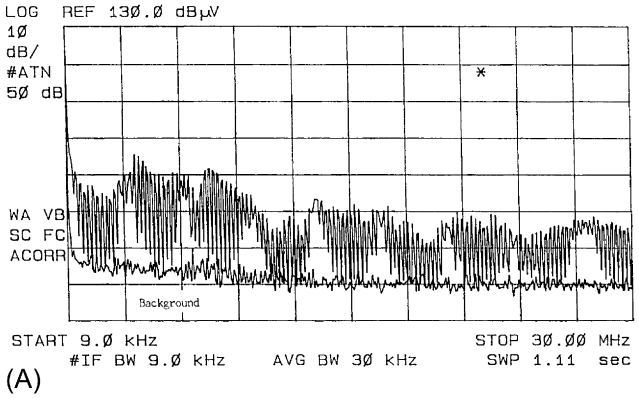
FIG. 12.42 A family of EP-QR converters: (A) buck converter, (B) boost converter, and (C) flyback converter.

turn-off capacitor. The turn-off snubber capacitor C_s is clamped by another capacitor C_c. At the end of each switching cycle, the snubber energy is dumped into C_c and then discharged into the DC bus via a discharge resistor. In order to reduce the snubber loss, the discharge resistor can be replaced by a switched-mode circuit. In this way, the Undeland snubber can become a snubber with energy recovery. The McMurray snubber is symmetrical. Both the turn-off snubber capacitors share current in parallel during turnoff. The voltage transient is limited by the capacitor closest to the turn-off device because the stray inductance to the other capacitor will prevent instantaneous current sharing. The turn-on inductors require midpoint connection. Snubber energy is dissipated into the snubber resistor. Like the Undeland snubber, the McMurray snubber can be modified into an energy recovery snubber. By using an energy recovery transformer as shown in Fig. 12.47, this snubber becomes a regenerative one. Although other regenerative circuits have been proposed, their complexity makes them unattractive in industrial applications. Also, they do not necessarily solve the power diode reverse-recovery problems.

Although the use of snubber circuits can reduce the switching stress in the power devices, the switching loss is actually damped into the snubber resistors unless regenerative snubbers are used. The switching loss is still a limiting factor to the high-frequency operation of power inverters. However, the advent of soft-switching techniques opens a new way to high-frequency inverter operation. Because the switching trajectory of a soft-switched switch is close to the voltage and current axis, faster power electronic devices with smaller SOAs can in principle be used. In general, both ZVS and ZCS can reduce switching loss in high-power power switches. However, for power switches with tail currents, such as IGBT, ZCS is more effective than ZVS.

12.14 Soft-Switching DC-AC Power Inverters

Soft-switching technique not only offers a reduction in switching loss and thermal requirement but also allows the possibility



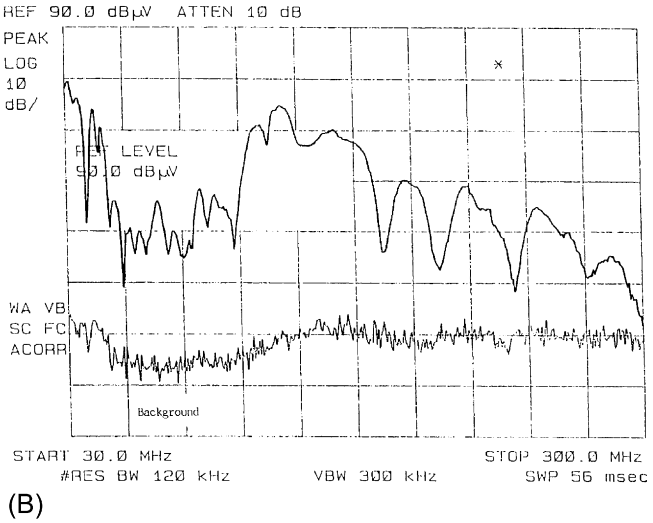


FIG. 12.43 (A) Conducted EMI from hard-switched flyback converter and (B) radiated EMI from hard-switched flyback converter.

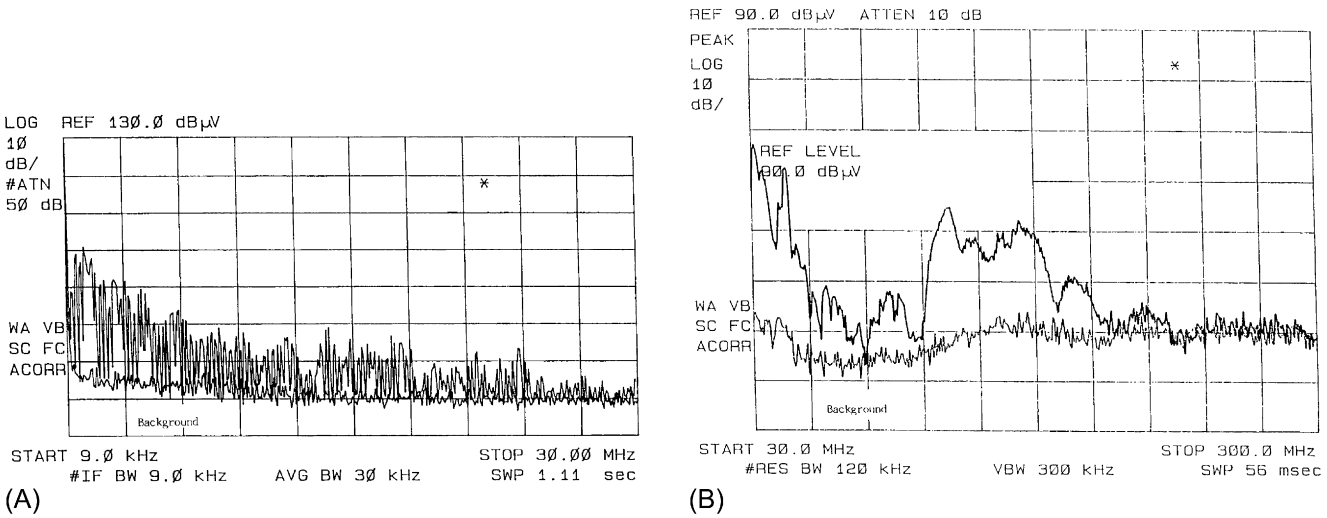


FIG. 12.44 (A) Conducted EMI from soft-switched flyback converter and (B) radiated EMI from soft-switched flyback converter.

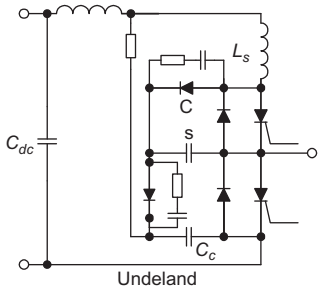


FIG. 12.45 Undeland snubber.

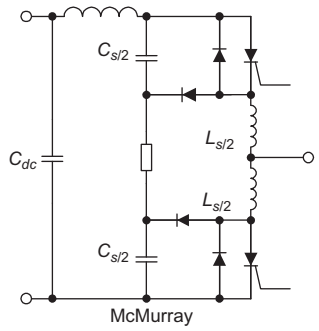


FIG. 12.46 McMurray snubber.

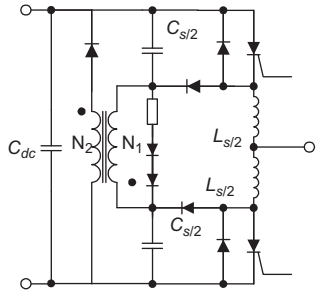


FIG. 12.47 McMurray snubber with energy recovery.

of high-frequency and snubberless operation. Improved circuit performance and efficiency and reduction of EMI emission can be achieved. For zero-voltage switching (ZVS) inverter applications, two major approaches that enable inverters to be soft-switched have been proposed. The first approach pulls the DC link voltage to zero momentarily so that the inverter's switches can be turned on and off with ZVS. Resonant DC link and quasi-resonant inverters belong to this category. The second approach uses the resonant pole idea. By incorporating the filter components into the inverter operation, resonance condition and thus zero-voltage/current conditions can be created for the inverter switches.

In this section, the following soft-switched inverters are described:

Approach 1: Resonant DC link inverters are as follows:

1. Resonant (pulsating) DC link inverters
2. Actively clamped resonant DC link inverters
3. Resonant inverters with minimum voltage stress
4. Quasi-resonant soft-switched inverter
5. Parallel resonant DC link inverter

Approach 2: Resonant pole inverters (RPIs) are as follows:

1. Resonant pole inverters
2. Auxiliary RPIs
3. Auxiliary resonant commutated pole inverters (ARCPIs)

Type 1 is the resonant DC link inverter [42–44] that sets the DC link voltage into oscillation so that the zero-voltage instants are created periodically for ZVS. Despite the potential advantages that this soft-switching approach can offer, a recent review on existing resonant-link topologies for inverters [45] concludes that the resonant DC link system results in an increase in circuit complexity and the frequency spectrum is restricted by the need of using integral pulse-density modulation (IPDM) when compared with a standard hard-switched

inverter. In addition, the peak pulsating link voltage of resonant-link inverters is twice the DC link voltage in a standard hard-switched inverter. Although clamp circuits (type 2) can be used to limit the peak voltage to 1.3–1.5 per unit [44], power devices with higher than normal voltage ratings have to be used.

Circuits of types 3–5 employ a switched-mode front-stage circuit that pulls the DC link voltage to zero momentarily whenever inverter switching is required. This soft-switching approach does not cause extra voltage stress to the inverter, and hence, the voltage rating of the power devices is only 1 per unit. As ZVS conditions can be created at any time, there is virtually no restriction in the PWM strategies. Therefore, well-established PWM schemes developed in the last 2 decades can be employed. In some ways, this approach is similar to some DC-side commutation techniques proposed in the past for thyristor inverters [46,47], although these DC-side commutation techniques were used for turning off thyristors in the inverter bridge and were not primarily developed for soft switching.

Circuits of type 6–8 retain the use of a constant DC link voltage. They incorporate the use of the resonant components and/or filter components into the inverter circuit operation. This approach is particularly useful for inverter applications in which output filters are required. Examples include uninterruptible power supplies (UPS) and inverters with output filters for motor drives. The LC filter components can form the auxiliary resonant circuits that create the soft-switching conditions. However, these tend to have high-power device count and require complex control strategy.

12.14.1 Resonant (Pulsating) DC Link Inverter

Resonant DC link converter for DC-AC power conversion was proposed in 1986 [42]. Instead of using a nominally constant DC link voltage, a resonant circuit is added to cause the DC link voltage to be pulsating at a high frequency. This resonant circuit theoretically creates periodic zero-voltage duration at which the inverter switches can be turned on or off. Fig. 12.48 shows the schematics of the pulsating link inverter. Typical DC link voltage, inverter's phase voltage, and the line voltages are shown in Fig. 12.49. Because the inverter switching can only occur at zero-voltage duration, integral pulse-density modulation (IPDM) has to be adopted in the switching strategy.

Analysis of the resonant DC link converter can be simplified by considering that the inverter system is highly inductive. The equivalent circuit is shown in Fig. 12.50.

The link current I_x may vary with the changing load condition but can be considered constant during the short resonant cycle. If switch S is turned on when the inductor current is I_{Lo}, the resonant DC link voltage can be expressed as

$$V_c(t) = V_s + e^{-\alpha t}[-V_s cos(\omega t) + \omega L I_M sin(\omega t)] \qquad (12.14)$$

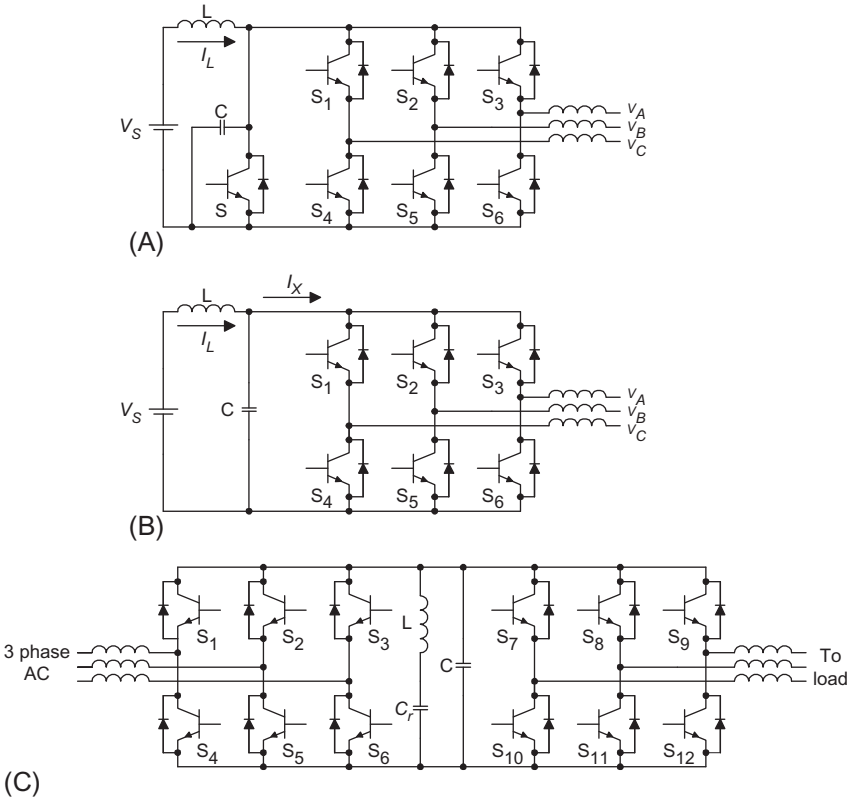


FIG. 12.48 Resonant-link inverters. (A) With resonant switch in the DC link. (B) With resonant tank in the DC link. (C) With resonant tank in the tank for AC-DC-AC system.

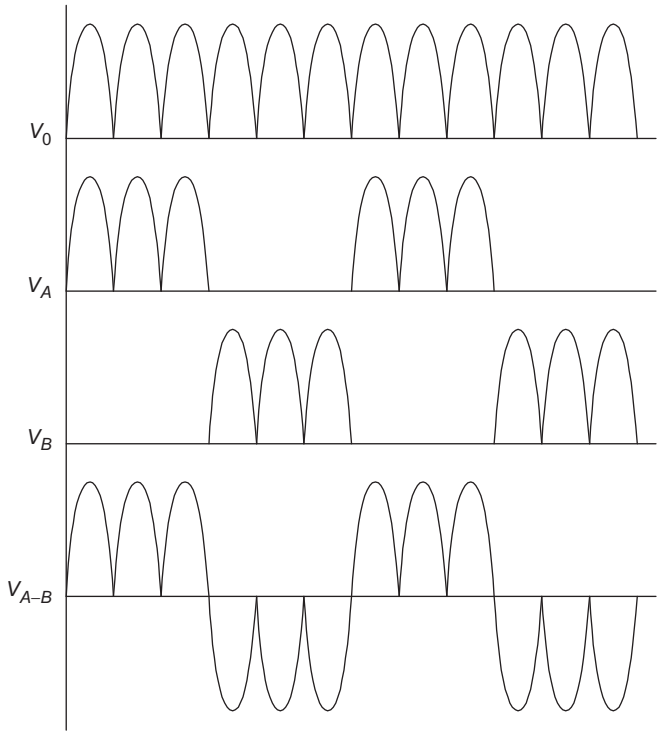


FIG. 12.49 Typical DC link voltage (V_0), phase voltages (V_A,V_B), and line voltage (V_{AB}) of resonant-link inverters.

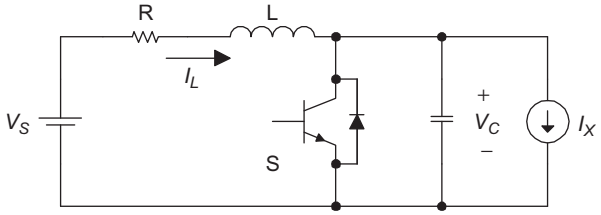


FIG. 12.50 Equivalent circuit of resonant-link inverter.

and inductor current i_L is

$$i_L(t) \approx I_x + e^{-\alpha t}\left[I_M \cos(\omega t) + \frac{V_s}{\omega L}\sin(\omega t)\right] \tag{12.15}$$

where

$$\alpha = \frac{R}{2L} \tag{12.16}$$

$$\omega_o = (LC)^{-0.5} \tag{12.17}$$

$$\omega = \left(\omega_0{}^2 - \alpha^2\right)^{0.5} \tag{12.18}$$

and

$$I_M = I_{Lo} - I_x \tag{12.19}$$

The resistance in the inductor could affect the resonant behavior because it dissipates some energy. In practice, $(i_L - I_x)$ has to be monitored when S is conducting. S can be turned on when $(i_L - I_x)$ is equal to a desired value. The objective is to ensure that the DC link voltage can be resonated to zero-voltage level in the next cycle.

The pulsating DC link inverter has the following advantages:

- Reduction of switching loss.
- Snubberless operation.
- High switching frequency (> 18 kHz) operation becomes possible, leading to the reduction of acoustic noise in inverter equipment.
- Reduction of heat sink requirements and thus improvement of power density.

This approach has the following limitations:

- The peak DC pulsating link voltage (2.0 per unit) is higher than the nominal DC voltage value of a conventional inverter. This implies that power devices and circuit components of higher voltage ratings must be used. This could be a serious drawback because power components of higher voltage ratings not only are more expensive but also usually have inferior switching performance than their low-voltage counterparts.
- Although voltage clamp can be used to reduce the peak DC link voltage, the peak voltage value is still higher than normal, and the additional clamping circuit makes the control more complicated.
- Integral pulse-density modulation has to be used. Many well-established PWM techniques cannot be employed.

Despite these advantages, this resonant converter concept has paved the way for other soft-switched converters to develop.

12.14.2 Active-Clamp Resonant DC Link Inverter

In order to solve the high voltage requirement in the basic pulsating DC link inverters, active-clamping techniques (Fig. 12.51)

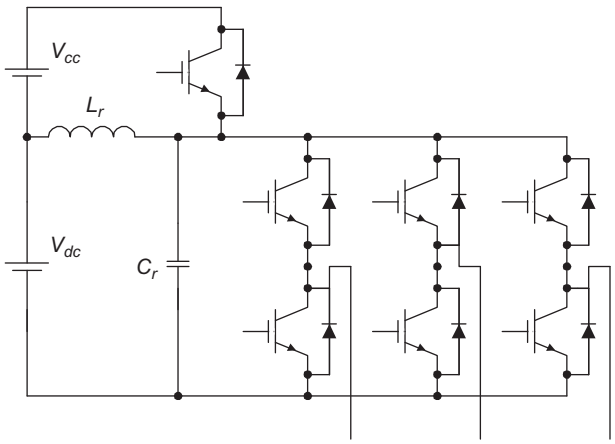


FIG. 12.51 Active-clamp resonant-link inverter.

have been proposed. The active clamp can reduce the per unit peak voltage from 2.0 to about 1.3–1.5 [44]. It has been reported that operating frequency in the range of 60–100 kHz has been achieved [48] with an energy efficiency of 97% for a 50 kVA drive system.

The design equations for active-clamp resonant-link inverter are

$$T_L = \frac{1}{f_L} = 2\sqrt{L_r C_r}\left(\cos^{-1}(1-k) + \frac{\sqrt{k(2-k)}}{k-1}\right) \tag{12.20}$$

where T_L is the minimum link period, f_L is the maximum link frequency, and k is the clamping ratio. For the active-clamp resonant inverter, k is typically 1.3–1.4 per unit.

The rate of rise of the current in the clamping device is

$$\frac{di}{dt} = \frac{(k-1)V_s}{L_r} \tag{12.21}$$

The peak clamping current required to ensure that the DC bus return to 0 V is

$$I_{sp} = V_s\sqrt{\frac{k(2-k)C_r}{L_r}} \tag{12.22}$$

In summary, resonant (pulsating) DC link inverters offer significant advantages such as the following:

- High switching frequency operation
- Low dv/dt for power devices
- ZVS with reduced switching loss
- Suitable for 1–250 kW
- Rugged operation with few failure mode

12.14.3 Resonant DC Link Inverter With Low Voltage Stress [49]

A resonant DC link inverter with low voltage stress is shown in Fig. 12.52. It consists of a front-end resonant converter that can pull the DC link voltage down just before any inverter switching. This resonant DC circuit serves as an interface between the DC power supply and the inverter. It essentially retains all the advantages of the resonant (pulsating) DC link inverters. But it offers extra advantages such as the following:

- No increase in the DC link voltage when compared with conventional hard-switched inverter. That is, the DC link voltage is 1.0 per unit.
- The zero-voltage condition can be created at any time. The ZVS is not restricted to the periodic zero-voltage instants as in resonant DC link inverter.
- Well-established PWM techniques can be employed.
- Power devices of standard voltage ratings can be used.

The timing program and the six operating modes of this resonant circuit are as shown in Figs. 12.53 and 12.54, respectively.

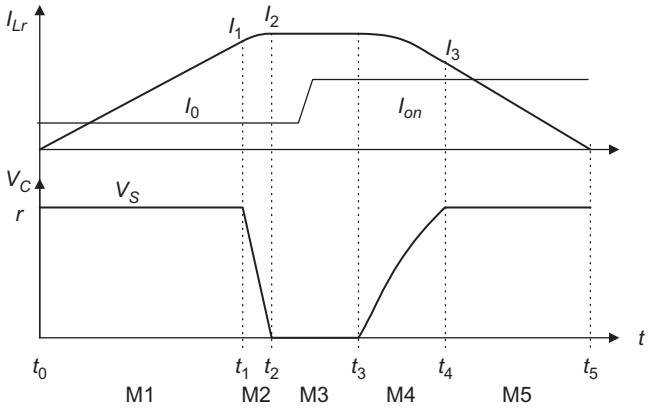


FIG. 12.53 Timing diagram of resonant-link inverter with minimum voltage stress.

(1) *Normal mode*

This is the standard PWM inverter mode. The resonant inductor current $i_{Lr}(t)$ and the resonant voltage $V_{cr}(t)$ are given by

$$i_{Lr}(t) = 0$$

$$v_{Cr}(t) = V_s$$

where V_s is the nominal DC link voltage.

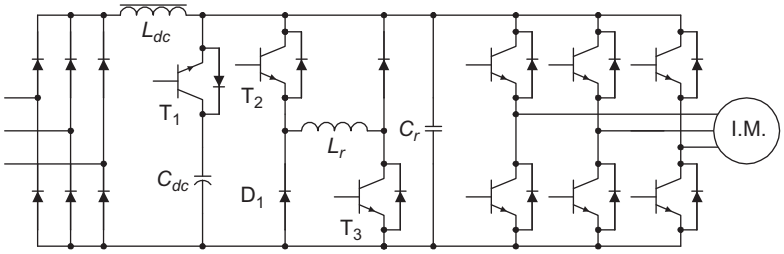


FIG. 12.52 Resonant DC link inverter with low voltage stress.

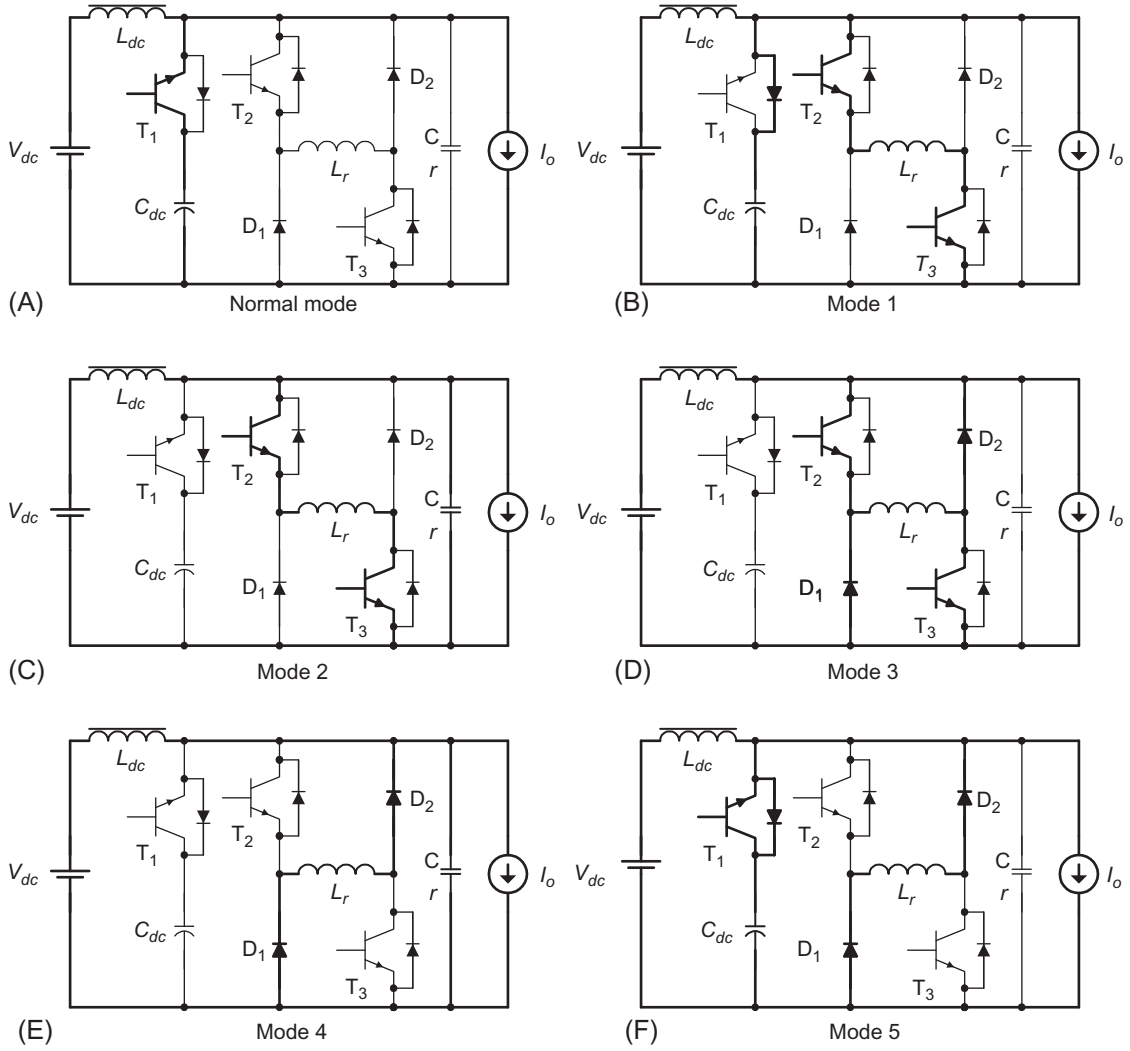


FIG. 12.54 Operating modes of resonant-link inverter with minimum voltage stress. (A) Normal mode. (B) Mode 1. (C) Mode 2. (D) Mode 3. (E) Mode 4. (F) Mode 5.

(2) *Mode 1 (Initiating mode): $(t_0 - t_1)$*

At t_0, mode 1 begins by switching on T_2 and T_3 on with zero current. $i_{Lr}(t)$ increases linearly with a di/dt of V_s/L_r. If $i_{Lr}(t)$ is equal to the initialized current I_i, T_1 is zero-voltage turned off. If $(I_s - I_o) < I_i$, then the initialization is ended when i_{Lr} (t) is equal to I_i, where I_s is the current flowing into the DC inductor L_{dc}. If $(I_s - I_o) > I_i$, then this mode continues until i_{Lr} (t) is equal to $(I_s - I_o)$. The equations in this interval are

$$i_{Lr}(t) = \frac{V_s}{L_r} t$$

$$v_{Cr}(t) = V_s$$

$$i_{Lr\,(t_1)} = \frac{V_s}{L_r} t_1 = I_i$$

(3) *Mode 2 (Resonant mode): $(t_1 - t_2)$*

After T_1 is turned off under ZVS condition, resonance between L_r and C_r occurs. V_{cr} (t) decreases from V_s to 0. At t_2, i_{Lr} (t) reaches the peak value in this interval. The equations are

$$i_{Lr}(t) = \frac{V_s}{Z_r} \sin(\omega_r t) + [I_1 + (I_o - I_s)] \cos(\omega_r t) - (I_o - I_s)$$

$$V_{Cr}(t) = -V_s \cos(\omega_r t) - [I_1 + (I_o - I_s)] Z_r \sin(\omega_r t)$$

$$i_{Lr}(t_2) = I_2 = I_{Lr,peak}$$

$$V_{Cr}(t_2) = 0$$

where

$$Z_r = \sqrt{\frac{L_r}{C_r}} \quad \text{and} \quad \omega_r = \frac{1}{\sqrt{L_r C_r}}$$

(4) *Mode 3 (Freewheeling mode): ($t_2 - t_3$)*

The resonant inductor current flows through two freewheeling paths (T_2-L_r-D_2 and T_3-D_1-L_r). This duration is the zero-voltage period created for ZVS of the inverter and should be longer than the minimum on and off times of the inverter's power switches:

$$i_{Lr}(t) = I_2$$

$$v_{Cr}(t) = 0$$

(5) *Mode 4 (Resonant mode): ($t_3 - t_4$)*

This mode begins when T_2 and T_3 are switched off under ZVS. The second half of the resonance between L_r and C_r starts again. The capacitor voltage V_{cr} (t) increases back from 0 to V_s and is clamped to V_s. The relevant equations in this mode are

$$i_{Lr}(t) = [I_2 - (I_{on} - I_s)]\cos(\omega_r t) - (I_{on} - I_s)$$
$$V_{Cr}(t) = [I_2 - (I_{on} - I_s)]Z_r \sin(\omega_r t)$$
$$i_{Lr}(t_4) = I_3$$
$$V_{Cr}(t_4) = V_s$$

where I_{on} is the load current after the switching state.

(6) *Mode 5 (Discharging mode): ($t_4 - t_5$)*

In this period, T_1 is switched on under ZV condition because V_{cr} (t) = V_s. The inductor current decreases linearly. This mode finishes when i_{Lr} (t) becomes zero:

$$i_{Lr}(t) = -\frac{V_s}{L_r}t + I_3$$
$$v_{Cr}(t) = V_s$$
$$i_{Lr}(t_5) = 0$$

12.14.4 Quasi-Resonant Soft-Switched Inverter [50]

12.14.4.1 Circuit Operation

Consider an inverter fed by a DC voltage source versus a front-stage interface circuit shown in Fig. 12.55 can be added between the DC voltage source and the inverter. The front-stage circuit consists of a quasi-resonant circuit in which the first half of the resonance cycle is set to occur to create the zero-voltage condition whenever inverter switching is needed. After inverter switching has been completed, the second half of the resonance cycle takes place so that the DC link voltage is set back to its normal level. To avoid excessive losses in the resonant circuit, a small capacitor C_{r1} is normally used to provide the DC link voltage, while the large smoothing DC link capacitor C_1 is isolated from the resonant circuit just before the zero-voltage duration. This method avoids the requirement for pulling the DC voltage of the bulk capacitor to zero.

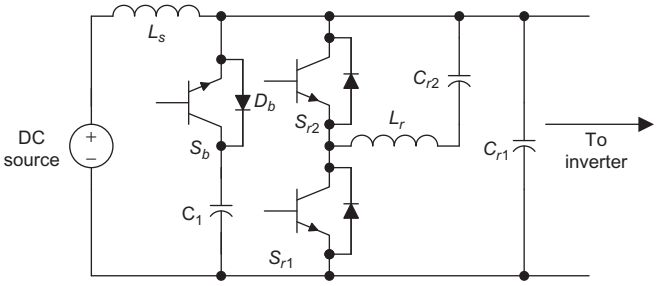


FIG. 12.55 Quasi-resonant circuit for soft-switched inverter.

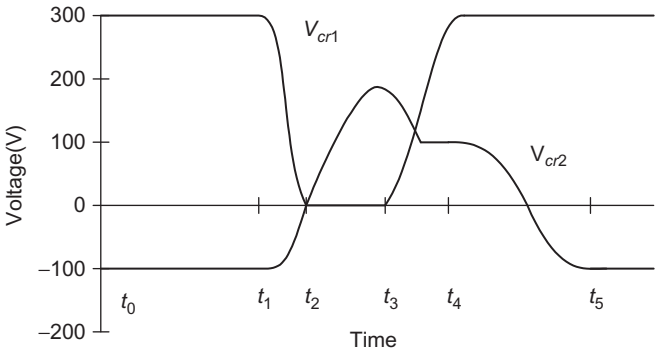


FIG. 12.56 Typical waveforms for V_{cr1} and V_{cr2}.

The period for this mode is from t_0 to t_1 in Fig. 12.56. In this mode, switch S_b is turned on, and switches S_{r1} and S_{r2} are turned off. The inverter in Fig. 12.55 works like a conventional DC link inverter. In this mode, $V_{cr1} = V_{c1}$. The voltage across switch S_b is zero. Before an inverter switching takes place, switch S_{r1} is triggered at t_1 to discharge C_{r1}. This operating mode ends at t_2 when V_{cr1} approaches zero. The equivalent circuit in this mode is shown in Fig. 12.57A. The switch S_b must be turned off at zero voltage when switch S_{r1} is triggered. After S_{r1} is triggered, C_{r1} will be discharged via the loop C_{r1}, C_{r2}, L_r, and S_{r1}. Under conditions of $V_{cr2} \leq 0$ and $C_{r1} \leq C_{r2}$, the energy stored in C_{r1} will be transferred to C_{r2}, and V_{cr1} falls to zero in the first half of the resonant cycle in the equivalent circuit of Fig. 12.57A. V_{cr1} will be clamped to zero by the freewheel diodes in the inverter bridge and will not become negative. Thus, V_{cr1} can be pulled down to zero for zero-voltage switching. When the current in inductor L_r becomes zero, switch S_{r1} can be turned off at zero current.

Inverter switching can take place in the period from t_2 to t_3 in which V_{cr1} remains zero. This period must be longer than the turn-on and turn-off times of the switches. When inverter switching has been completed, it is necessary to reset the voltage of capacitor C_{r1}. The equivalent circuit in this mode is shown in Fig. 12.57B. The current in inductor L_r reaches zero at t_3. Due to the voltage in V_{cr2} and the

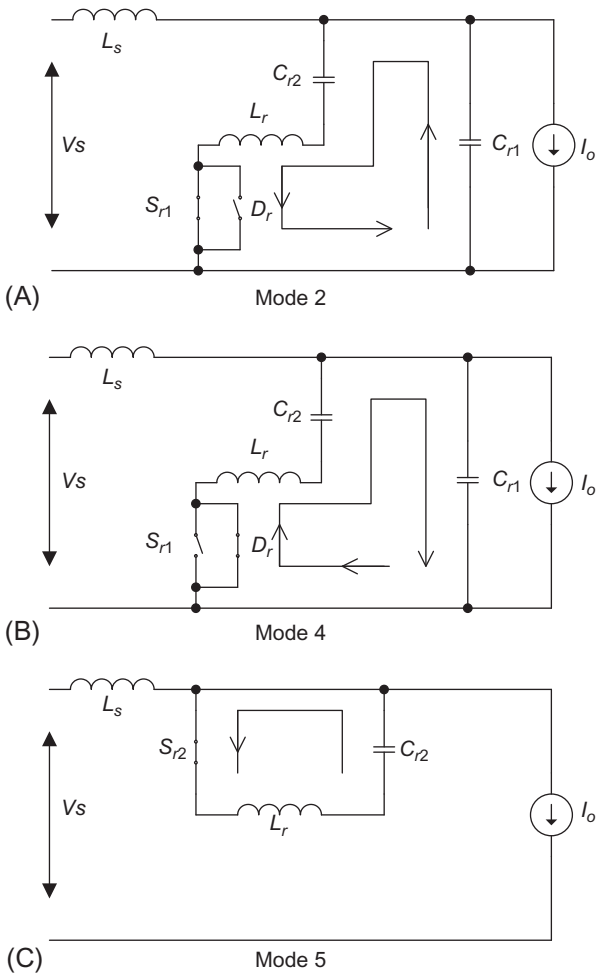


FIG. 12.57 Equivalent circuits of the quasi-resonant circuit for different modes. (A) Mode 2. (B) Mode 4. (C) Mode 5.

presence of diode D_r, this current then flows in the opposite direction. C_{r1} will be recharged via L_r, C_{r2}, C_{r1}, and D_r. The diode D_r turns off when the current in L_r becomes zero. V_{cr1} will not go beyond 1 per unit because C_{r1} is clamped to supply voltage by diode D_b. The switch S_b can be turned on again at zero-voltage condition when V_{cr1} returns to normal DC supply voltage. After D_r turns off, V_{cr2} may not be zero. Some positive residual capacitor voltage remains in C_2 at t_4, as shown in Fig. 12.56. In case V_{cr2} is positive, V_{cr1} cannot be pulled down to zero again in the next switching cycle. Therefore, S_{r2} should be triggered after t_4 to reverse the residual voltage in C_{r2}. At time t_5, Sr_2 turns off at zero-current condition, and V_{cr2} is now reversed to negative. The equivalent circuit in this mode is shown in Fig. 12.57C. When $V_{cr2} \leq 0$ and $C_{r1} \leq C_{r2}$, V_{cr1} can be pulled down to zero again before the next inverter switching. The operation can then be repeated in next switching cycle.

12.14.4.2 Design Considerations

(1) C_{r1} and C_{r2}

The criterion for getting zero capacitor voltages V_{cr1} is

$$(C_{r1} - C_{r2})V_s + 2C_{r2}V_{o2} - \Delta I\pi\sqrt{L_r C_e} \leq 0 \tag{12.23}$$

where

- V_{o1} is the initial voltage of C_{r1},
- V_{o2} is the initial voltage of C_{r2},
- i_{L0} is the initial current of inductor L_r,
- $\Delta I = I_o - I_s$ is the difference between load current and supply current. It is assumed to be a constant within a resonant cycle,
- R_r is the equivalent resistance in the resonant circuit,
- $C_e = \dfrac{C_{r1}C_{r2}}{C_{r1} + C_{r2}}$

When $\Delta I \geq 0$, the above criterion is always true under conditions of

$$C_{r1} \leq C_{r2}, V_{o2} \leq 0$$

The criterion for recharging voltage V_{cr1} to 1 per unit DC link voltage is

$$\frac{2C_{r2}}{C_{r1} + C_{r2}}V_{02} - \frac{\Delta I}{C_{r1} + C_{r2}}\pi\sqrt{L_r C_e} \geq V_s \tag{12.24}$$

(2) Inductor L_r

The inductor L_r should be small so that the DC link voltage can be decreased to zero quickly. However, a small L_r could result in large peak resonant current and therefore requirement of power devices with large current pulse ratings. An increase in the inductance of L_r can limit the peak current in the quasi-resonant circuit. Because the resonant frequency depends on both the inductor and the capacitor, therefore, the selection of L_r can be considered together with the capacitors C_{r1} and C_{r2} and with other factors such as the current ratings of power devices, the zero-voltage duration, and the switching frequency required in the soft-switching circuit.

(3) Triggering instants of the switches

The correct triggering instants for the switches are essential for the successful operation of this soft-switched inverter. For the inverter switches, the triggering instants are determined from a PWM modulation. Let T_s be the time at which the inverter switches change states. To get the zero-voltage inverter switching, switch S_{r1} should be turned on half resonant cycle before the inverter switching instant. The turn-on instant of S_{r1}, which is t_1 in Fig. 12.56, can be written as

$$t_1 = T_s - \frac{\pi}{\omega} \tag{12.25}$$

where $\omega = \sqrt{\omega_0^2 - \alpha^2}, \alpha = \frac{R_r}{2L_r}, \omega_0 = \sqrt{\frac{1}{L_r C_e}}$. The switch S_b is turned off at t_1.

S_{r1} may be turned off during its zero-current period when diode D_r is conducting. For easy implementation, its turn-off time can be selected as $T_s + \pi/\omega$. Because the DC link voltage can be pulled down to zero in less than half resonant cycle, T_s should occur between t_2 and t_3.

At time t_3 (the exact instant depends on the ΔI), the diode D_r turns on in the second half of the resonant cycle to recharge C_{r1}. At t_4, V_{cr1} reaches 1 per unit and diode D_b clamps V_{cr1} to 1 per unit. The switch S_b can be turned on again at t_4, which is half resonant cycle after the start of t_3:

$$t_4 \approx t_3 + \frac{\pi}{\omega} \tag{12.26}$$

As t_3 cannot be determined accurately, a voltage sensor in principle can be used to provide information for t_4 so that S_b can be turned on to reconnect C_1 to the inverter. In practice, however, S_b can be turned on a few microseconds (longer than $T_s + \pi/\omega$) after t_2 without using a voltage sensor (because it is not critical for S_b to be on exactly at the moment V_{cr} reaches the nominal voltage). As for switch S_{r2}, it can be turned on a few microseconds after t_4. It will be turned off half of resonant cycle $\left(\pi\sqrt{L_r C_{r2}}\right)$ in the $L_r - C_{r2}$ circuit later. In practice, the timing of S_{r1}, S_{r2}, and S_b can be adjusted in a simple tuning procedure for a given set of parameters. Fig. 12.58 shows the measured gating signals of S_{r1}, S_{r2}, and S_b with the DC link voltage V_{cr1} in a 20-kHz switching inverter. Figs. 12.59 and 12.60 show the measured waveforms of I_s, I_o, and V_{cr1} under no-load condition and loaded condition, respectively.

12.14.4.3 Control of Quasi-Resonant Soft-Switched Inverter Using Digital Time Control [51]

Based on the zero-average-current error (ZACE) control concept, a digital time control (DTC) method has been developed for a current-controlled quasi-resonant soft-switched inverter. The basic ZACE concept is shown in Fig. 12.61. The current error is obtained from the difference of a reference current

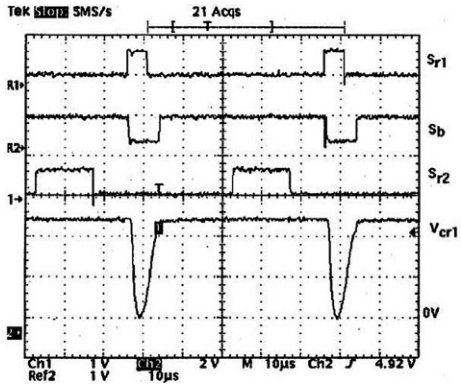


FIG. 12.58 Gating signals for S_{r1}, S_{r2}, and S_b with V_{cr1}.

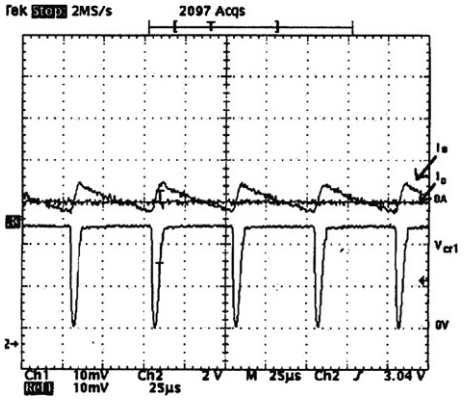


FIG. 12.59 Typical I_s, I_o, and V_{cr1} under no-load condition.

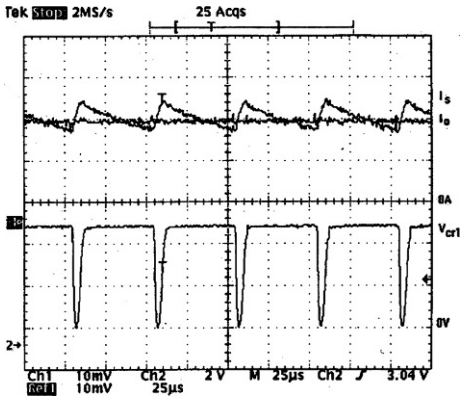


FIG. 12.60 Typical I_s, I_o, and V_{cr1} under loaded condition.

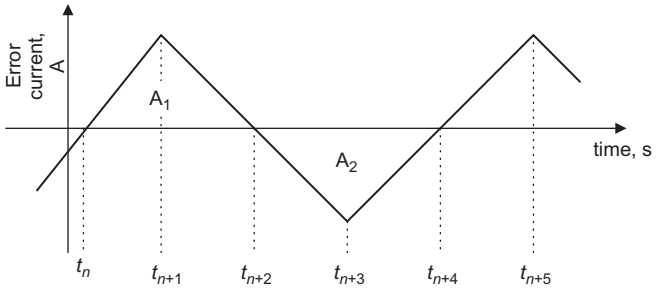


FIG. 12.61 Zero-average-current error (ZACE) control concept.

and the sensed current. The idea is to make the areas of each transition (A1 and A2) equal. If the switching frequency is significantly greater than the fundamental frequency of the reference signal, the rising and falling current segments can be assumed to be linear. The following simplified equation can be established:

$$\Delta t_{n+1} = t_{n+1} - t_n \tag{12.27}$$

The control algorithm for the inverter is

$$\Delta t_{n+3} = \Delta t_{n+2} + D\left[\frac{T_{sw}}{2} - (t_{n+2} - t_n)\right] \tag{12.28}$$

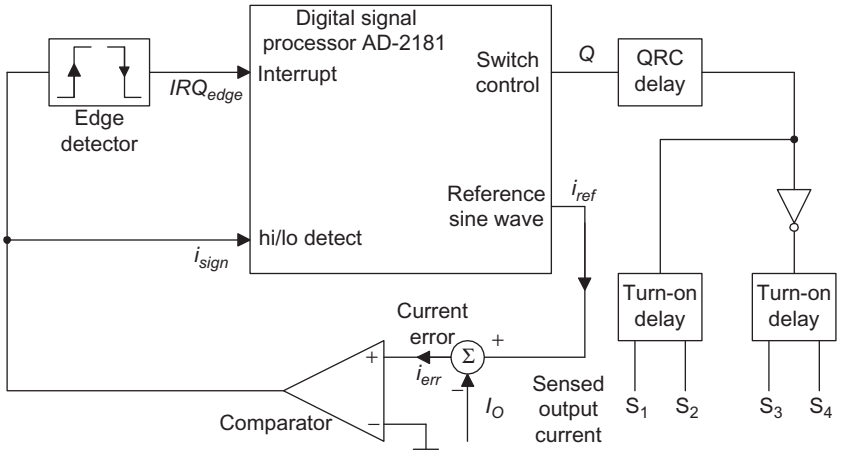


FIG. 12.62 Implementation of DTC.

where $D = \dfrac{\Delta t_{n+2}}{t_{n+2} - t_n}$ and $T_{sw} = t_{n+4} - t_n$.

The schematic of a digital signal processor (DSP)-based controller for the DTC method is shown in Fig. 12.62. The duty cycle can be approximated from the reference sine wave by level shifting and scaling it between 0 and 1. The time $t_{n+2} - t_n$ is the sum of Δt_{n+1} and Δt_{n+2}. These data provide information for the calculation of the next switching time Δt_{n+1}.

The switches are triggered by the changing edge of the switch control Q. Approximate delays are added to the individual switching signals for both the inverter switches and the quasi-resonant switches. Typical gating waveforms are shown in Fig. 12.63. The use of the quasi-resonant soft-switched inverter is a very effective way in suppressing switching transient and EMI emission. Fig. 12.64A and B shows the inverter switch voltage waveforms of a standard hard-switched inverter and a quasi-resonant soft-switched inverter, respectively. It is clear that the soft-switched waveform has much less transient than the hard-switched waveform.

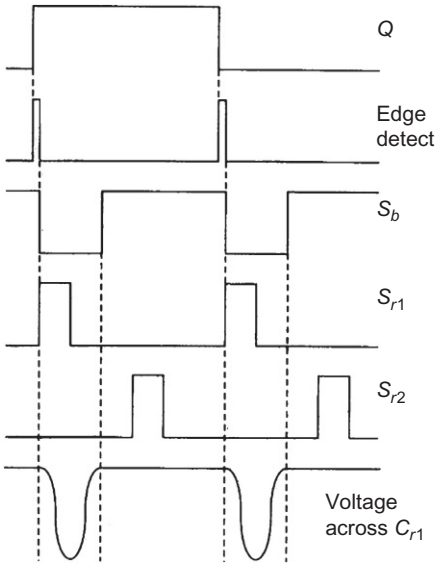


FIG. 12.63 Timing diagrams for the gating signals.

12.14.5 RPI and ARCPI

The RPI integrates the resonant components with the output filter components L_f and C_f. The load is connected to the

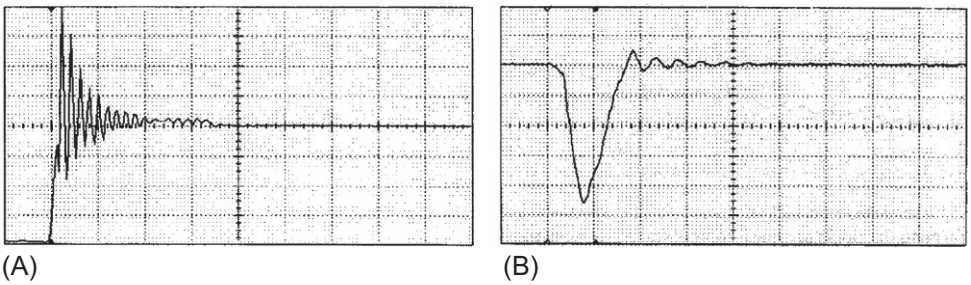


FIG. 12.64 (A) Typical switch voltage under hard turnoff and (B) typical switch voltage under soft turnoff.

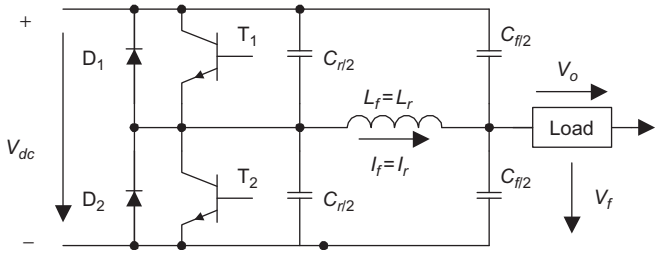


FIG. 12.65 One leg of a resonant pole inverter.

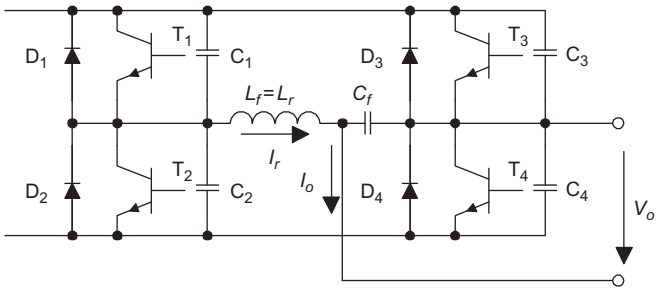


FIG. 12.66 Single-phase resonant pole inverter.

midpoint of the DC bus capacitors as shown in Fig. 12.65. It should however be noted that the RPI can be described as a resonant inverter. Fig. 12.66 shows a single-phase RPI. Its operation can be described with the timing diagram in Fig. 12.67. The operating modes are included in Fig. 12.68. The RPI provides soft switching for all power switches. But it has two disadvantages. First, the power devices have to be switched continuously at the resonant frequency determined by the resonant components. Second, the power devices in the RPI circuit require a 2.2–2.5 p.u. current turn-off capability.

An improved version of the RPI is the ARCPI. The ARCPI for one inverter leg is shown in Fig. 12.69. Unlike the basic RPI, the ARCPI allows the switching frequency to be controlled. Each of the primary switches is closely paralleled with a snubber capacitor to ensure ZV turnoff. Auxiliary switches are connected in series with an inductor, ensuring that they operate under ZC conditions. For each leg, an auxiliary circuit comprising two extra switches A1 and A2, two freewheeling diodes, and a resonant inductor L_r is required. This doubles the number of power switches when compared with hard-switched inverters. Fig. 12.70 shows the three-phase ARCPI system. Depending on the load conditions, three commutation modes are generally needed. The commutation methods at low and high current are different. This makes the control of the ARCPI very complex. The increase in control and circuit complexity represents a considerable cost penalty [52,53].

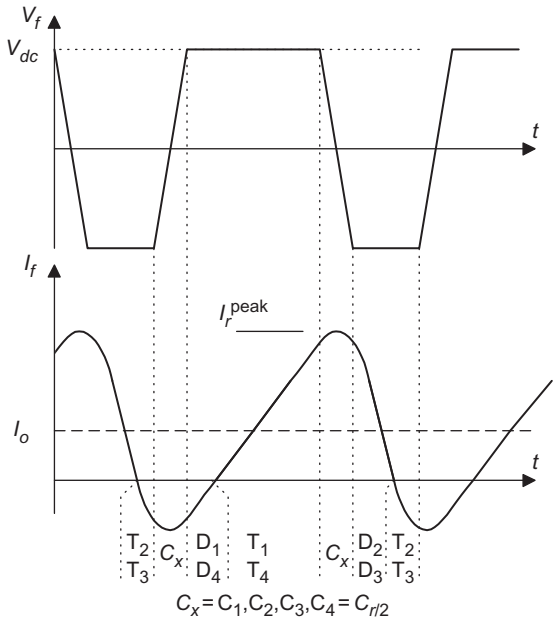


FIG. 12.67 Timing diagram for a single-phase resonant pole inverter.

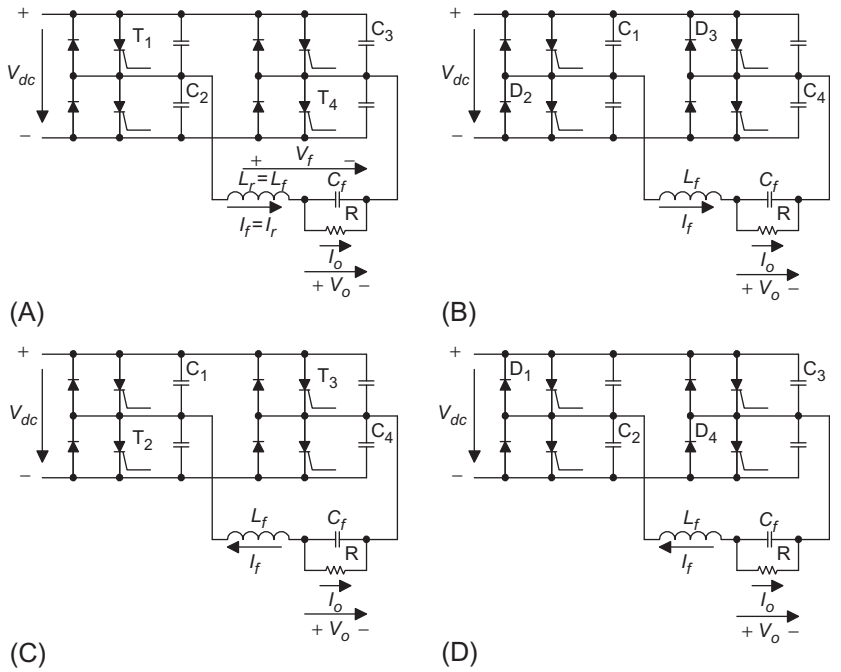


FIG. 12.68 Operating modes of a single-phase resonant pole inverter. (A) Mode 1. (B) Mode 2. (C) Mode 3. (D) Mode 4.

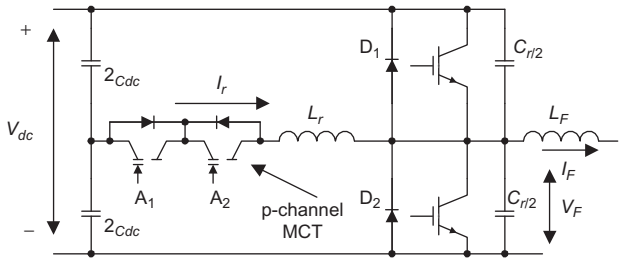


FIG. 12.69 Improved resonant pole inverter leg.

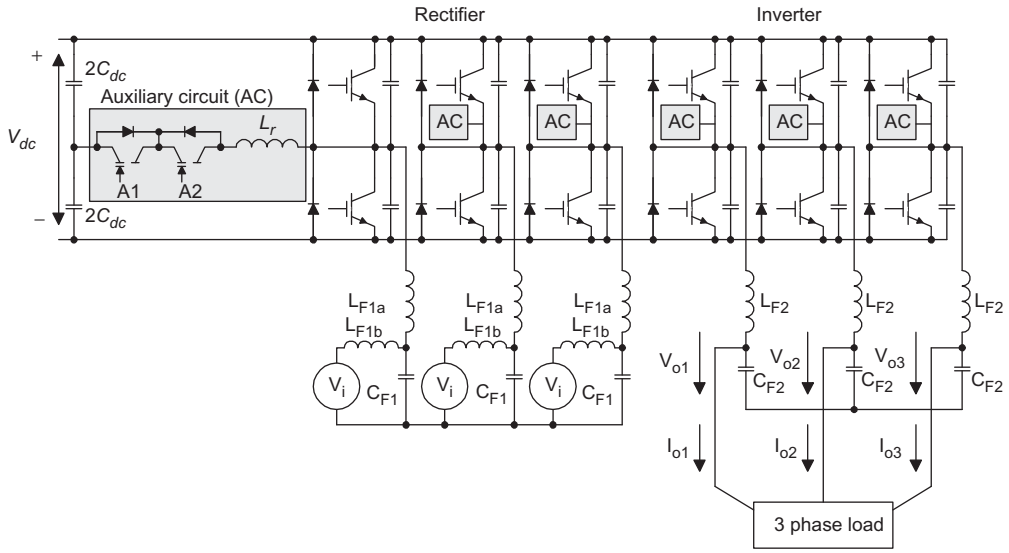


FIG. 12.70 Three-phase auxiliary resonant commutated pole inverter (ARCPI).

References

[1] R.M. Davis, in: Power Diode and Thyristor Circuits, IEE Monograph Series, vol. 7, Peregrinus, Herts, 1971.

[2] N. Mohan, T. Undeland, W. Robbins, Power Electronics, Converters, Applications, and Design, John Wiley and Sons, Hoboken, NJ, 1995.

[3] M.H. Rashid, Power Electronics, Circuits, Devices, and Applications, Pearson/Prentice Hall, Upper Saddle River, NJ, 2004.

[4] P. Vinciarelli, Forward Converter Switching at Zero Current. U.S. Patent 4,416,959, November 1983.

[5] F.C. Lee, High-Frequency Resonant, Quasi-Resonant and Multi-Resonant Converters, Virginia Power Electronics Center, Blacksburg, VA, 1991.

[6] F.C. Lee, High-Frequency Resonant and Soft-Switching Converters, Virginia Power Electronics Center, 1991.

[7] K. Kit Sum, Recent Developments in Resonant Converters, Intertec Communication Press, Ventura, CA, 1988.

[8] R.E. Tarter, Solid-State Power Conversion Handbook, Wiley-Interscience publication, New York, 1993.

[9] K.H. Liu, F.C. Lee, Resonant switches—a unified approach to improve performances of switching converters, in: Proceedings of the International Telecommunications Energy Conference, 1984, pp. 344–351.

[10] K.H. Liu, R. Oruganti, F.C. Lee, Resonant switches—topologies and characteristics, in: Proceedings of the IEEE Power Electronics Specialists Conference, 1985, pp. 62–67.

[11] K.D.T. Ngo, Generalized of resonant switches and quasi-resonant DC-DC converters, in: Proceedings of the IEEE Power Electronics Specialists Conference, 1986, pp. 58–70.

[12] F.C. Lee, High-frequency quasi-resonant and multi-resonant converter technologies, in: Proceedings of the IEEE International Conference on Industrial Electronics, 1988, pp. 509–521.

[13] K.H. Liu, F.C. Lee, Zero-voltage switching techniques in DC/DC converter circuits, in: Proceedings of the IEEE Power Electronics Specialists Conference, 1986, pp. 58–70.

[14] M. Jovanovic, W. Tabisz, F.C. Lee, Zero-voltage switching technique in high frequency off-line converters, in: Proceedings of the Applied Power Electronics Conference and Exposition, 1988, pp. 23–32.

[15] R. Steigerwald, A comparison of half-bridge resonant converter topologies, IEEE Trans. Power Electron. 3 (2) (1988) 174–182.

[16] O.D. Patterson, D.M. Divan, Pseudo-resonant full-bridge DC/DC converter, in: Proceedings of the IEEE Power Electronics Specialists Conference, 1987, pp. 424–430.

[17] C.P. Henze, H.C. Martin, D.W. Parsley, Zero-voltage switching in high frequency power converters using pulse width modulation, in: Proceedings of the IEEE Applied Power Electronics Conference and Exposition, 1988, pp. 33–40.

[18] General Electric Company, Full-bridge lossless switching converters, U.S. Patent 4,864,479, 1989.

[19] W.A. Tabisz, F.C. Lee, DC analysis and design of zero-voltage switched multi-resonant converters, in: Proceedings of the IEEE Power Electronics Specialists Conference, 1989, pp. 243–251.

[20] W.A. Tabisz, F.C. Lee, Zero-voltage-switching multi-resonant technique—a novel approach to improve performance of high frequency quasi-resonant converters, IEEE Trans. Power Electron. 4 (4) (1989) 450–458.

[21] M. Jovanovic, F.C. Lee, DC analysis of half-bridge zero-voltage-switched multi-resonant converter, IEEE Trans. Power Electron. 5 (2) (1990) 160–171.

[22] R. Farrington, M.M. Jovanovic, F.C. Lee, Constant-frequency zero-voltage-switched multi-resonant converters: analysis, design, and experimental results, in: Proceedings of the IEEE Power Electronics Specialists Conference, 1990, pp. 197–205.

[23] G. Hua, C.S. Leu, F.C. Lee, Novel zero-voltage-transition PWM converters, in: Proceedings of the IEEE Power Electronics Specialists Conference, 1992, pp. 55–61.

[24] R. Watson, G. Hua, F.C. Lee, Characterization of an active clamp flyback topology for power factor correction applications, IEEE Trans. Power Electron. 11 (1) (1996) 191–198.

[25] R. Watson, F.C. Lee, G. Hua, Utilization of an active-clamp circuit to achieve soft switching in flyback converters, IEEE Trans. Power Electron. 11 (1) (1996) 162–169.

[26] B. Carsten, Design techniques for transformer active reset circuits at high frequency and power levels, in: Proceedings of the High Frequency Power Conversion Conference, 1990, pp. 235–245.

[27] S.D. Johnson, A.F. Witulski, E.W. Erickson, A comparison of resonant technologies in high voltage DC applications, in: Proceedings of the IEEE Applied Power Electronics Conference, 1987, pp. 145–166.

[28] A.K.S. Bhat, S.B. Dewan, A generalized approach for the steady state analysis of resonant inverters, IEEE Trans. Ind. Appl. 25 (2) (1989) 326–338.

[29] A.K.S. Bhat, A resonant converter suitable for 650V DC bus operation, IEEE Trans. Power Electron. 6 (4) (1991) 739–748.

[30] A.K.S. Bhat, M.M. Swamy, Loss calculations in transistorized parallel converters operating above resonance, IEEE Trans. Power Electron. 4 (4) (1989) 449–458.

[31] A.K.S. Bhat, A unified approach for the steady-state analysis of resonant converter, IEEE Trans. Ind. Electron. 38 (4) (1991) 251–259.

[32] Unitrode Corporation, Applications Handbook, Unitrode Corporation, 1999.

[33] I. Barbi, J.C. Bolacell, D.C. Martins, F.B. Libano, Buck quasi-resonant converter operating at constant frequency: analysis, design and experimentation, in: PESC'89, 1989, pp. 873–880.

[34] K.W.E. Cheng, P.D. Evans, A family of extended-period circuits for power supply applications using high conversion frequencies, in: EPE'91, 1991, pp. 4.225–4.230.

[35] S.Y.R. Hui, K.W.E. Cheng, S.R.N. Prakash, A fully soft-switched extended-period quasi-resonant power correction circuit, IEEE Trans. Power Electron. 12 (5) (1997) 922–930.

[36] H.S.H. Chung, S.Y.R. Hui, W.H. Wang, A zero-current-switching PWM flyback converter with a simple auxiliary switch, IEEE Trans. Power Electron. 14 (2) (1999) 329–342.

[37] H.S.H. Chung, S.Y.R. Hui, Reduction of EMI in power converters using fully soft-switching technique, IEEE Trans. Electromag. 40 (3) (1998) 282–287.

[38] H.S.H. Chung, W.L. Cheung, K.S. Tang, A ZCS bidirectional flyback converter, IEEE Trans. Power Electron. 19 (6) (2004) 1426–1434.

[39] M.T. Zhang, M.M. Jovanovic, F.C. Lee, Design considerations and performance evaluation of synchronous rectification in flyback converter, IEEE Trans. Power Electron. 13 (3) (1998) 538–546.

[40] T. Undeland, Snubbers for pulse width modulated bridge converters with power transistors or GTOs, in: IPEC Conference proceedings Tokyo, vol. 1, 1983, pp. 313–323.

[41] McMurray, Efficient snubbers for voltage source GTO inverters, IEEE Trans. Power Electron. 2 (3) (1987) 264–272.

[42] D.M. Divan, The resonant dc link converter-A new concept in static power conversion, IEEE Trans. Ind. Appl. 25 (2) (1989) 317–325.
[43] Jin-Sheng Lai, B.K. Bose, An induction motor drive using an improved high frequency resonant DC link inverter, IEEE Trans. Power Electron. 6 (3) (1991) 504–513.
[44] D.M. Divan, G. Skibinski, Zero-switching-loss inverters for high-power applications, IEEE Trans. Ind. Appl. 25 (4) (1989) 634–643.
[45] S.J. Finney, T.C. Green, B.W. Williams, Review of resonant link topologies for inverters, IEE Proc. B 140 (2) (1993) 103–114.
[46] S.B. Dewan, D.L. Duff, Optimum design of an input commutated inverter for AC motor control, IEEE Trans. Indus. Gen. Appl. IGA-5 (6) (1969) 699–705.
[47] V.R. Stefanov, P. Bhagwat, A novel DC side commutated inverter, in: IEEE PESC Record, 1980.
[48] A. Kurnia, H. Cherradi, D. Divan, Impact of IGBT behavior on design optimization of soft switching inverter topologies, in: IEEE IAS Conference Record, 1993, pp. 140–146.
[49] Y.C. Jung, J.G. Cho, G.H. Cho, A new zero voltage switching resonant DC-link inverter with low voltage stress, in: Proceedings of IEEE Industrial Electronics Conference, 1991, pp. 308–313.
[50] S.Y.R. Hui, E.S. Gogani, J. Zhang, Analysis of a quasi-resonant circuit for soft-switched inverters, IEEE Trans. Power Electron. 11 (1) (1999) 106–114.51.
[51] D.M. Baker, V.G. Agelidis, C.W. Meng, C.V. Nayar, Integrating the digital time control algorithm with DC-Bus “Notching” circuit based soft-switching inverter, IEE Proc. Electric Power Appl. 146 (5) (1999) 524–529.
[52] F.C. Lee, D. Borojevic, Soft-switching PWM converters and inverters, tutorial notes, in: PESC’94, 1994.
[53] D.M. Divan, R.W. De Doncker, Hard and soft-switching voltage source inverters, tutorial notes, in: PESC’94, 1994.

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13

Multilevel Power Converters

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13.1 Introduction

Numerous industrial applications require higher power apparatus in recent years. Some medium-voltage motor drives and utility applications require medium-voltage and megawatt power level converters. For a medium-voltage grid, it is troublesome to connect only one power semiconductor switch directly. Hence, a multilevel power converter structure has been introduced as an alternative in high-power and medium-voltage situations. A multilevel converter not only achieves high-power ratings but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaics or wind turbines can be easily interfaced to a multilevel converter system for a high-power utility application [1–3].

The concept of multilevel converters has been introduced since 1975 [4]. The term *multilevel* began with the three-level converter [5]. Subsequently, several multilevel converter topologies have been developed [6–13]. However, the basic concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only on the rating of the dc voltage sources to which they are connected.

A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency pulse-width modulation (PWM). The attractive features of a multilevel converter are summarized as follows:

- *Staircase waveform quality*: Multilevel converters not only can generate the output voltages with very low distortion but also can reduce the dv/dt stresses; therefore, electromagnetic compatibility (EMC) problems can be reduced.
- *Common-mode (CM) voltage*: Multilevel converters produce smaller CM voltage; therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. Furthermore, CM voltage can be eliminated by using advanced modulation strategies such as that proposed in [14].
- *Input current*: Multilevel converters can draw input current with low distortion.
- *Switching frequency*: Multilevel converters can operate at both fundamental switching frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency.

Unfortunately, multilevel converters do have some disadvantages. One particular disadvantage is the requirement of greater number of power semiconductor switches. Although lower voltage rated switches can be utilized in a multilevel converter, each switch requires a related gate-drive circuit. This may cause the overall system to be more expensive and complex.

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Many multilevel converter topologies have been proposed during the last two decades. Contemporary research has engaged novel converter topologies and unique modulation schemes. Moreover, four different major multilevel converter structures have been reported in the literature: cascaded H-bridge converter with separate dc sources, diode clamp (neutral-clamped), flying capacitors (capacitor-clamped), and modular multilevel converter. Moreover, abundant modulation techniques and control paradigms have been developed for multilevel converters, such as sinusoidal pulse-width modulation (SPWM), selective harmonic elimination (SHE PWM), and space vector modulation (SVM). In addition, many multilevel converter applications focus on industrial medium-voltage motor drives [11,15], utility interface for renewable energy systems [16], flexible ac transmission system (FACTS) [17], and traction drive systems [18].

This chapter reviews the state of the art of multilevel power converter technology. Fundamental multilevel converter structures and modulation paradigms are discussed including the pros and cons of each. The main focus is on modern and more practical industrial applications of multilevel converters. Finally, the possible future developments of multilevel converter technology are noted.

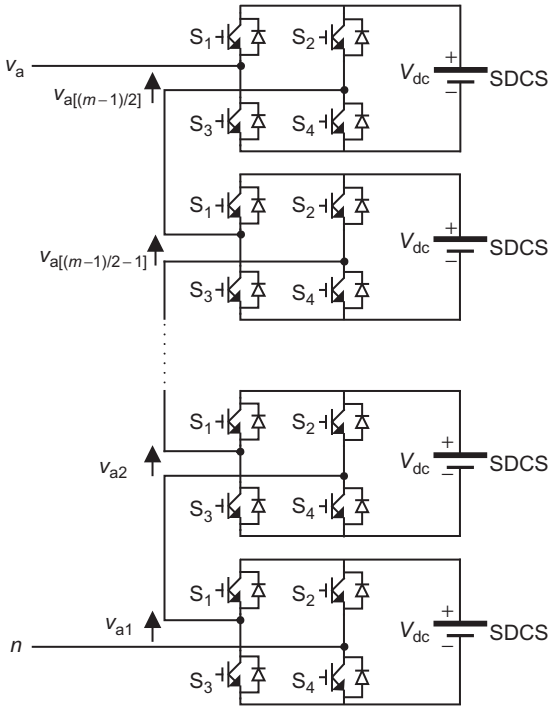


FIG. 13.1 Single-phase structure of a multilevel cascaded H-bridge inverter.

13.2 Multilevel Power Converter Structures

As mentioned earlier, four different major multilevel converter structures have been used in industrial applications: cascaded H-bridge converter with separate dc sources, diode clamped, flying capacitors, and modular multilevel converter. It should be noted that the term *multilevel converter* refers to a power electronic circuit that could operate in an inverter or rectifier mode. The multilevel inverter structures are the focus of this chapter; however, the illustrated structures can be implemented for rectifying operation as well.

13.2.1 Cascaded H-Bridges

A single-phase structure of an m-level cascaded inverter is illustrated in Fig. 13.1. Each separate dc source (SDCS) is connected to a single-phase full-bridge or H-bridge inverter.

Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$, by connecting the dc source to the ac output by different combinations of the four switches: S_1, S_2, S_3, and S_4. To obtain $+V_{dc}$, switches S_1 and S_4 are turned on, whereas to obtain $-V_{dc}$, switches S_2 and S_3 are turned on. By turning on either S_1 and S_2 or S_3 and S_4, the output voltage will be zero. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels, m, in a cascade inverter is defined by $m = 2s + 1$, where s is the number of separate dc sources. An example of phase voltage waveform for an 11-level cascaded H-bridge inverter with five SDCSs and five full bridges is shown in Fig. 13.2. The phase voltage $v_{an} = v_{a1} + v_{a2} + v_{a3} + v_{a4} + v_{a5}$.

For a stepped waveform such as the one depicted in Fig. 13.2 with s steps, the Fourier transform for this waveform follows [14,18]:

$$V(\omega t) = \frac{4V_{dc}}{\pi}\sum_n [\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_s)] \times \frac{\sin(n\omega t)}{n}, \quad \text{where } n = 1,3,5,7,\ldots \tag{13.1}$$

From Eq. (13.1), the magnitudes of the Fourier coefficients when normalized with respect to V_{dc} are as follows:

$$H(n) = \frac{4}{\pi n}[\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_s)], \quad \text{where } n = 1,3,5,7,\ldots \tag{13.2}$$

The conducting angles, $\theta_1, \theta_2, \ldots, \theta_s$, can be chosen such that the voltage total harmonic distortion is minimum. Generally, these angles are chosen so that predominant lower frequency harmonics, 5, 7, 11, and 13 are eliminated [19]. More details on harmonic elimination techniques will be discussed in the following section.

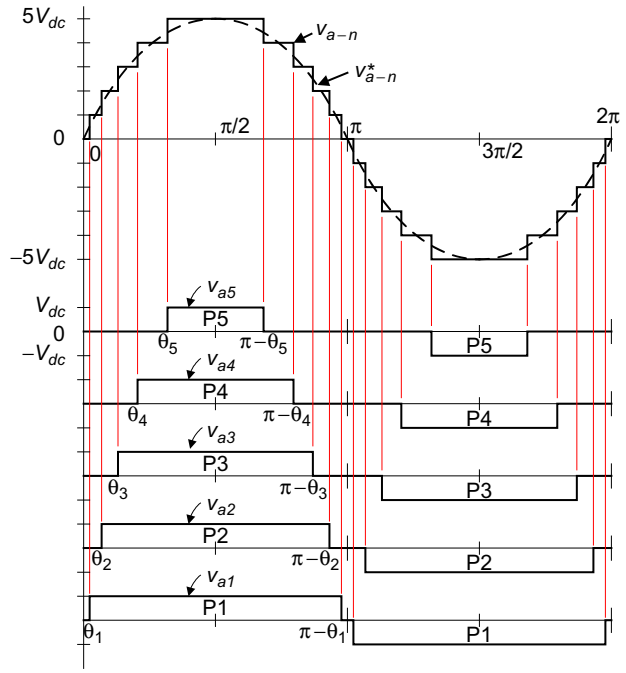


FIG. 13.2 Output phase voltage waveform of an 11-level cascade inverter with five separate dc sources.

Multilevel cascaded inverters have been proposed for such applications as static var generation, an interface with renewable energy sources, and for battery-based applications.

Three-phase cascaded inverters can be connected in wye, as shown in Fig. 13.3, or in delta. Peng et al. have demonstrated a prototype multilevel cascaded static var generator connected in parallel with an electric system that could supply or draw reactive current from an electric system [20–23]. The inverter could be controlled to regulate either the power factor of the current drawn from the source or the bus voltage of the electric system where the inverter was connected. Peng et al. [20] and Joos et al. [24] have also shown that a cascade inverter can be directly connected in series with the electric system for static var compensation. Cascaded inverters are ideal for connecting renewable energy sources with an ac grid because of the need for separate dc sources in applications such as photovoltaics or fuel cells.

Cascaded inverters have also been proposed for use as the main traction drive in electric vehicles where several batteries or ultracapacitors are well suited to serve as SDCSs [18,25]. The cascaded inverter could also serve as a rectifier or charger for the batteries of an electric vehicle while the vehicle was connected to an ac supply as shown in Fig. 13.3. In addition, the cascade inverter can act as a rectifier in a vehicle that uses regenerative braking.

Manjrekar and Lipo have proposed a cascade topology that uses multiple dc levels, which instead of being identical in value are multiples of each other [26,27]. They also used a combination of fundamental frequency switching for some of the levels and PWM switching for part of the levels to achieve the output voltage waveform. This approach enables a wider diversity of output voltage magnitudes; however, it also results in unequal voltage and current ratings for each of the levels and loses the advantage of being able to use identical modular units for each level.

The main advantages and disadvantages of multilevel cascaded H-bridge converters are as follows [28,29]:

13.2.1.1 Advantages

- The number of possible output voltage levels is more than twice the number of dc sources ($m = 2s + 1$).
- The series of H-bridges makes for modularized layout and packaging. This will enable the manufacturing process to be done more quickly and cheaply.

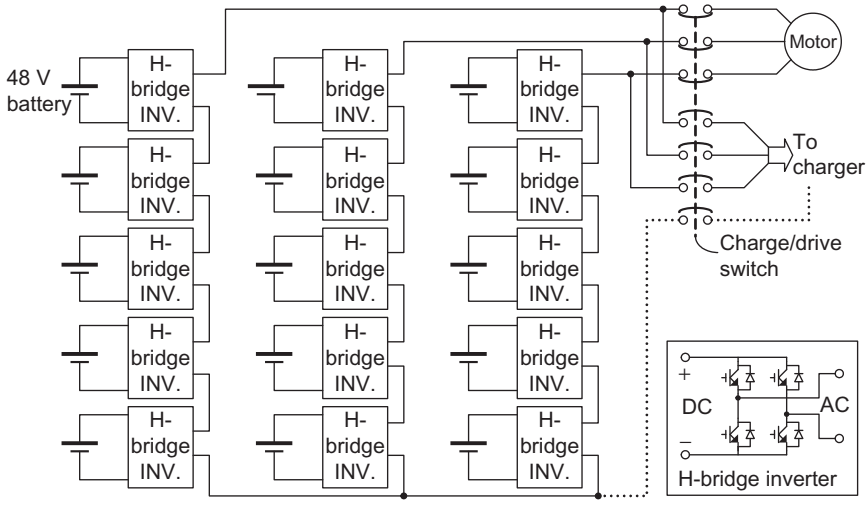


FIG. 13.3 Three-phase wye-connection structure for electric vehicle motor drive and battery charging.

13.2.1.2 Disadvantages

- Separate dc sources are required for each of the H-bridges. This will limit its application to products that already have multiple SDCSs readily available.

Another kind of cascaded multilevel converter with transformers using standard three-phase bilevel converters has been proposed [14]. The circuit is shown in Fig. 13.4. The converter uses output transformers to add different voltages. In order to add up the converter output voltages, the outputs of the three converters need to be synchronized with a separation of 120° between each phase. For example, for obtaining a three-level voltage between outputs *a* and *b*, the output voltage can be synthesized by $V_{ab} = V_{a1-b1} + V_{b1-a2} + V_{a2-b2}$. An isolated transformer is used to provide voltage boost. With three converters synchronized, the voltages, $V_{a1-b1}, V_{b1-a2}, V_{a2-b2}$, are all in phase, and thus, the output level can be tripled [1].

The advantage of the cascaded multilevel converters with transformers using standard three-phase bilevel converters is that the three converters are identical, and thus, control is more simple. However, the three converters need separate dc sources, and a transformer is needed to add up the output voltages.

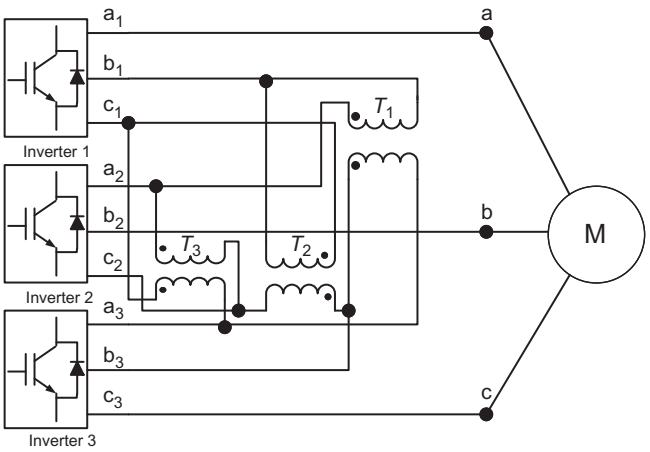


FIG. 13.4 Cascaded multilevel converter with transformers using standard three-phase bilevel converters.

13.2.2 Diode-Clamped Multilevel Inverter

The neutral point converter proposed by Nabae, Takahashi, and Akagi in 1981 was essentially a three-level diode-clamped inverter [5]. Several researchers published articles that have reported experimental results for four-, five-, and six-level diode-clamped converters for uses such as static var compensation, variable speed motor drives, and high-voltage system interconnections [17–30]. A three-phase six-level diode-clamped inverter is shown in Fig. 13.5. Each of the three phases of the inverter shares a common dc bus, which has been subdivided by five capacitors into six levels. The voltage across each capacitor is V_{dc}, and the voltage stress across each switching device is limited to V_{dc} through the clamping diodes. Table 13.1 lists the output voltage levels possible for one phase of the inverter with the negative dc rail voltage V_0 as a reference. State condition 1 means the switch is on, and 0 means the switch is off. Each phase has five complementary switch pairs such that turning on one of the switches of the pair requires the

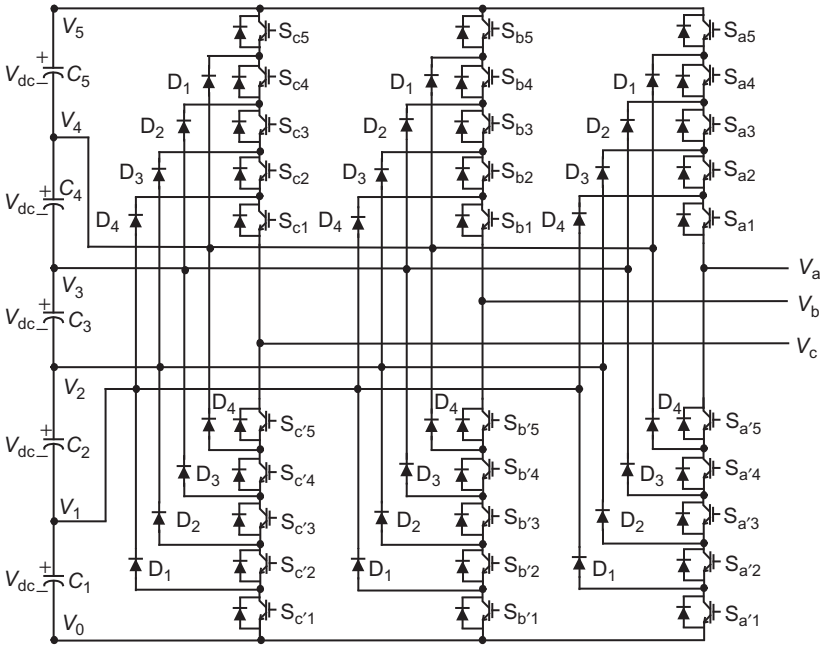


FIG. 13.5 Three-phase six-level structure of a diode-clamped inverter.

TABLE 13.1 Diode-clamped six-level inverter voltage levels and corresponding switch states

	Switch state									
Voltage V_{a0}	S_{a5}	S_{a4}	S_{a3}	S_{a2}	S_{a1}	$S_{a'5}$	$S_{a'4}$	$S_{a'3}$	$S_{a'2}$	$S_{a'1}$
$V_5 = 5V_{dc}$	1	1	1	1	1	0	0	0	0	0
$V_4 = 4V_{dc}$	0	1	1	1	1	1	0	0	0	0
$V_3 = 3V_{dc}$	0	0	1	1	1	1	1	0	0	0
$V_2 = 2V_{dc}$	0	0	0	1	1	1	1	1	0	0
$V_1 = 1V_{dc}$	0	0	0	0	1	1	1	1	1	0
$V_0 = 0$	0	0	0	0	0	1	1	1	1	1

other complementary switch to be turned off. The complementary switch pairs for phase-leg a are $(S_{a1}, S_{a'1})$, $(S_{a2}, S_{a'2})$, $(S_{a3}, S_{a'3})$, $(S_{a4}, S_{a'4})$, and $(S_{a5}, S_{a'5})$. Table 13.1 also shows that in a diode-clamped inverter, the switches that are on for a particular phase leg are always adjacent and in series. For a six-level inverter, a set of five switches should be on at any given time.

Fig. 13.6 shows one of the three line-line voltage waveforms for a six-level inverter. The line voltage V_{ab} consists of a phase-leg "a" voltage and a phase-leg "b" voltage. The resulting line voltage is an 11-level staircase waveform. This means that an m-level diode-clamped inverter has an m-level output phase voltage and a $(2m-1)$-level output line voltage.

Although each active switching device is required to block only a voltage level of V_{dc}, the clamping diodes require different ratings for reverse voltage blocking. Using phase a of Fig. 13.5 as an example, when all the lower switches $S_{a'1}$ through $S_{a'5}$ are turned on, D_4 must block four voltage levels or $4V_{dc}$. Similarly, D_3 must block $3V_{dc}$, D_2 must block $2V_{dc}$, and D_1 must block V_{dc}. If the inverter is designed such that each blocking diode has the same voltage rating as the active switches, D_n will require n diodes in series; consequently, the number of diodes required for each phase would be $(m-1)\times(m-2)$. Thus, the number of blocking diodes is quadratically related to the number of levels in a diode-clamped converter [28].

One application of the multilevel diode-clamped inverter is an interface between a high-voltage dc transmission line and an ac transmission line [29]. Another application would be a variable speed drive for high-power medium-voltage (2.4–13.8 kV) motors as proposed in [3,6,19,28–30]. Several authors have proposed for the diode-clamped converter that static var compensation is an additional function. The main advantages and disadvantages of multilevel diode-clamped converters are as follows [1–3].

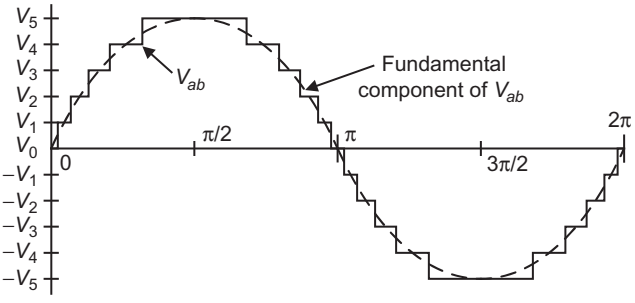


FIG. 13.6 Line voltage waveform for a six-level diode-clamped inverter.

13.2.2.1 Advantages

- All the phases share a common dc bus, which minimizes the capacitance requirements of the converter. For this reason, a back-to-back topology is not only possible but also practical for uses such as a high-voltage back-to-back interconnection or an adjustable speed drive.
- The capacitors can be precharged as a group.
- Efficiency is high for fundamental frequency switching.

13.2.2.2 Disadvantages

- Real power flow is difficult for a single inverter because the intermediate dc levels will tend to overcharge or discharge without precise monitoring and control.
- The number of clamping diodes required is quadratically related to the number of levels, which can be cumbersome for units with a high number of levels.

13.2.3 Flying-Capacitor Multilevel Inverter

Meynard and Foch introduced a flying-capacitor-based inverter in 1992 [31]. The structure of this inverter is similar to that of the diode-clamped inverter except that instead of using clamping diodes, the inverter uses capacitors. The circuit topology of the flying-capacitor multilevel inverter is shown in Fig. 13.7. This topology has a ladder structure of dc side capacitors, where the voltage on each capacitor differs from that of the next capacitor. The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform.

One advantage of the flying-capacitor-based inverter is that it has redundancies for inner voltage levels, that is, two or more valid switch combinations can synthesize an output voltage. Table 13.2 shows a list of all the combinations of phase voltage levels that are possible for the six-level circuit shown in Fig. 13.7. Unlike the diode-clamped inverter, the flying-capacitor inverter does not require all of the switches that are "on" (conducting) be in a consecutive series. Moreover, the flying-capacitor inverter has "phase" redundancies, whereas the diode-clamped inverter has only "line-line" redundancies [2,3,32]. These redundancies allow a choice of charging or discharging specific capacitors and can be incorporated in the control system for balancing the voltages across the various levels.

In addition to the $(m-1)$ dc link capacitors, the m-level flying-capacitor multilevel inverter will require $(m-1)\times(m-2)/2$ auxiliary capacitors per phase if the voltage rating of the capacitors is identical to that of the main switches. One application proposed

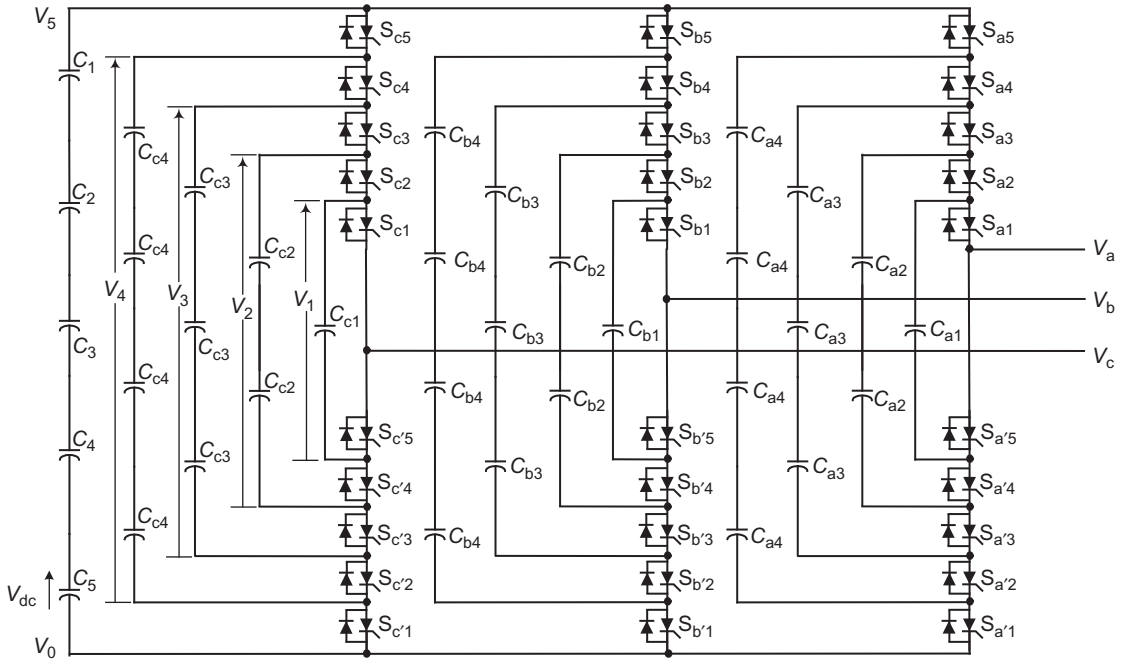


FIG. 13.7 Three-phase six-level structure of a flying-capacitor inverter.

TABLE 13.2 Flying-capacitor six-level inverter redundant voltage levels and corresponding switch states

	Switch state									
Voltage V_{a0}	S_{a5}	S_{a4}	S_{a3}	S_{a2}	S_{a1}	$S_{a'5}$	$S_{a'4}$	$S_{a'3}$	$S_{a'2}$	$S_{a'1}$
$V_{a0} = 5V_{dc}$ (noredundancies)										
$5V_{dc}$	1	1	1	1	1	0	0	0	0	0
$V_{a0} = 4V_{dc}$ (4 redundancies)										
$5V_{dc} - V_{dc}$	1	1	1	1	0	0	0	0	0	1
$4V_{dc}$	0	1	1	1	1	1	0	0	0	0
$5V_{dc} - 4V_{dc} + 3V_{dc}$	1	0	1	1	1	0	1	0	0	0
$5V_{dc} - 3V_{dc} + 2V_{dc}$	1	1	0	1	1	0	0	1	0	0
$5V_{dc} - 2V_{dc} + V_{dc}$	1	1	1	0	1	0	0	0	1	0
$V_{a0} = 3V_{dc}$ (5 redundancies)										
$5V_{dc} - 2V_{dc}$	1	1	1	0	0	0	0	0	1	1
$4V_{dc} - V_{dc}$	0	1	1	1	0	1	0	0	0	1
$3V_{dc}$	0	0	1	1	1	1	1	0	0	0
$5V_{dc} - 4V_{dc} + 3V_{dc} - V_{dc}$	1	0	1	1	0	0	1	0	0	1
$5V_{dc} - 3V_{dc} + V_{dc}$	1	1	0	0	1	0	0	1	1	0
$4V_{dc} - 2V_{dc} + V_{dc}$	0	1	1	0	1	1	0	0	1	0
$V_{a0} = 2V_{dc}$ (6 redundancies)										
$5V_{dc} - 3V_{dc}$	1	1	0	0	0	0	0	1	1	1
$5V_{dc} - 4V_{dc} + V_{dc}$	1	0	0	0	1	0	1	1	1	0
$4V_{dc} - 2V_{dc}$	0	1	1	0	0	1	0	0	1	1
$4V_{dc} - 3V_{dc} + V_{dc}$	0	1	0	0	1	1	0	1	1	0
$3V_{dc} - V_{dc}$	0	0	1	1	0	1	1	0	0	1
$3V_{dc} - 2V_{dc} + V_{dc}$	0	0	1	0	1	1	1	0	1	0
$2V_{dc}$	0	0	0	1	1	1	1	1	0	0
$V_{a0} = V_{dc}$ (4 redundancies)										
$5V_{dc} - 4V_{dc}$	1	0	0	0	0	0	1	1	1	1
$4V_{dc} - 3V_{dc}$	0	1	0	0	0	1	0	1	1	1
$3V_{dc} - 2V_{dc}$	0	0	1	0	0	1	1	0	1	1
$2V_{dc} - V_{dc}$	0	0	0	1	0	1	1	1	0	1
V_{dc}	0	0	0	0	1	1	1	1	1	0
$V_{a0} = 0$ (n redundancies)										
0	0	0	0	0	0	1	1	1	1	1

in the literature for the multilevel flying capacitor is static var generation [2,3]. The main advantages and disadvantages of multilevel flying-capacitor converters are as follows [2,3]:

13.2.3.1 Advantages

- Phase redundancies are available for balancing the voltage levels of the capacitors.
- Real and reactive power flow can be controlled.
- The large number of capacitors enables the inverter to ride through short duration outages and deep voltage sags.

13.2.3.2 Disadvantages

- Control is complicated to track the voltage levels for all of the capacitors. Also, precharging all of the capacitors to the same voltage level and start-up is complex.
- Switching utilization and efficiency is poor for real power transmission.
- The large number of capacitors is both more expensive and bulky than clamping diodes in multilevel diode-clamped converters. Packaging is also more difficult in inverters with a high number of levels.

13.2.4 Modular Mutilevel Inverter Structures

The modular multilevel converter (MMC) was first introduced by Marquardt in 2001 [33]. The configuration of a MMC is shown in Fig. 13.8A. Each phase leg of the MMC consists of one upper and one lower arm connected in series between the dc terminals. N series-connected SMs and one arm inductor L_{arm} form an arm. Each SM can be realized by a half-bridge [34] [35], H-bridge [36] [37], or clamp-double [38] circuit, as illustrated in Fig. 13.8B–D.

Among these, the MMC with half-bridge SM does not have any intrinsic fault current-limiting or current-blocking capability. Under a dc short-circuit fault, the fault current can flow from the ac side to the faulted dc side through the antiparalleled diodes of the controllable power switches, even though these switches are turned off. Therefore, fast-acting dc breakers are necessary to protect the system from damage. On the other hand, the H-bridge SM is capable of generating negative capacitor voltage, which can be used to block the fault current. However, compared with the half-bridge SM, the H-bridge one has twice the number of semiconductor devices, leading to higher cost and operating losses. For the "clamp-double" SM in Fig. 13.8D, power device T_5 always conducts under normal operation conditions, making the clamp-double SM equivalent to two series-connected half-bridge SMs. Under a dc side fault, T_5 is turned off, and dc voltage is inserted by both capacitors to minimize the dc fault current. Compared with the H-bridge SM, the output voltage of clamp-double SM can be doubled, with additional conduction loss of T_5.

Due to the lower cost and higher efficiency, the MMC with half-bridge SMs is used for most of the commercial HVDC projects [39]. Therefore, the basic operation principle of an MMC with half bridge will be introduced in this section. As illustrated in Fig. 13.9B, each half-bridge SM contains two IGBTs as switching elements and a DC storage capacitor C_{sub}. A SM is considered to be bypassed if the lower switch is closed and the upper switch is open, while if the lower switch is open

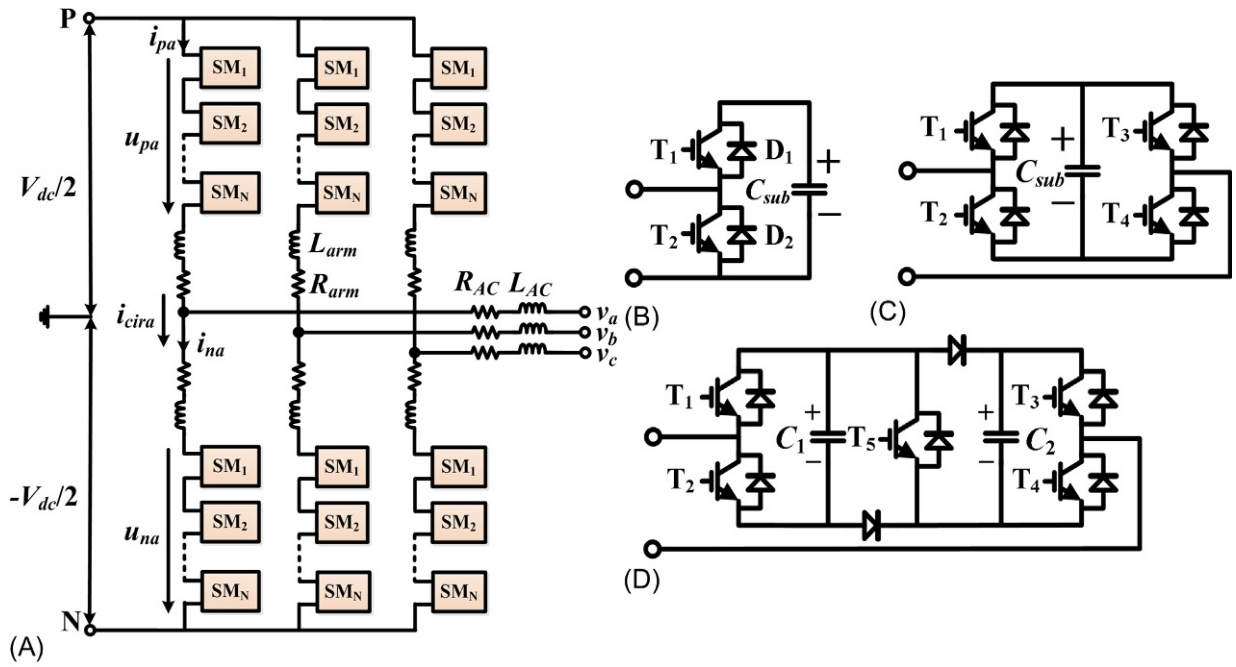


FIG. 13.8 (A) Circuit configuration of a MMC with (B) half-bridge cell, (C) full-bridge cell, and (D) clamp-double cell.

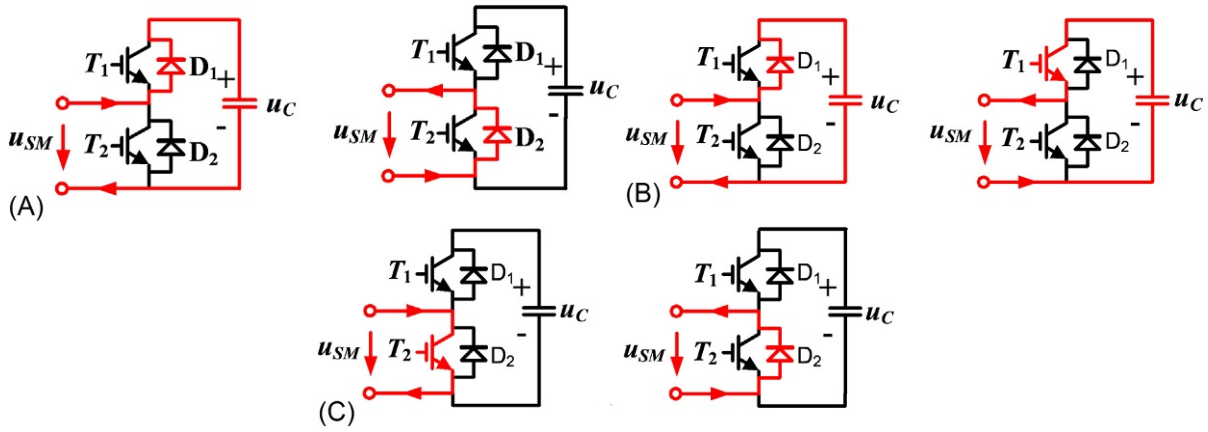


FIG. 13.9 States and current paths of an SM in the MMC converter, (A) both IGBTs are switched off, (B) IGBT1 is switched on, IGBT2 is switched off, (C) IGBT1 is switched off, and IGBT2 is switched on.

and the upper switch is closed, the SM is inserted. Three different states are relevant for the proper operation of an SM, as illustrated in Fig. 13.9:

1. Both IGBTs are switched off.
   This case does not occur during normal operation with power transfer. Upon charging, that is, after closing the AC power switch, all SMs of the converter are under this condition. In the event of a serious failure, all SMs of the converter should return to this state. If the current flows from the AC terminal to the dc side during this state, the flow passes through diode D_1 and charges the capacitor. When it flows in the opposite direction, the freewheeling diode D_2 conducts and bypasses the capacitor.
2. IGBT1 (T_1) is switched on, and IGBT2 (T_2) is switched off.
   Irrespective of the current flow direction, the voltage of the storage capacitor is applied to the terminals of the SM. Depending on the current direction, the current either flows through D_1 and charges the SM capacitor or flows through T_1 and discharges the SM capacitor.
3. IGBT1 is switched off, and IGBT2 is switched on.
   In this case, the current flows through either T_2 or D_2 depending on its direction, which ensures that zero voltage is applied to the terminals of the SM. The voltage in the capacitor remains unchanged.

It is thereby possible to separately and selectively control each of the individual SMs in a converter leg. In principle, the two converter arms of each phase represent a controllable voltage source. In this arrangement, the total voltage generated by the upper and lower arm SMs in one phase unit should equal to the dc link voltage. By adjusting the output voltage of SMs in both arms, that is, inserting and bypassing of SM capacitors according to a switching pattern created by a modulator, the desired sinusoidal voltage at the AC terminal can easily be achieved.

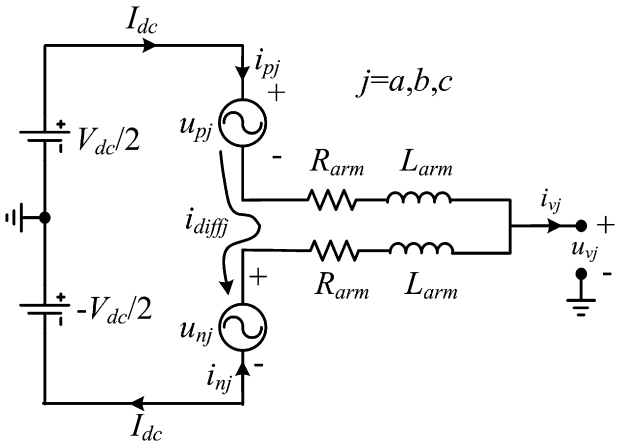


FIG. 13.10 Single-phase equivalent circuit of the MMC.

Fig. 13.10 illustrates the equivalent circuit of the MMC. L_{arm} and R_{arm} are the arm inductance and equivalent arm resistance, respectively. V_{dc} and I_{dc} are the total dc bus voltage and dc current individually. u_{vj} is the converter output voltage of j phase at point v, whereas i_{vj} is the corresponding line current. The arm voltages generated by the cascaded SMs are expressed as u_{pj} and u_{nj}, where the subscripts p and n denote the upper (positive) and lower (negative) arms, respectively. i_{pj} and i_{nj} are the corresponding arm currents, which can be expressed as

$$\begin{aligned} i_{pj} &= \frac{i_{vj}}{2} + i_{diffj} \\ i_{nj} &= \frac{i_{vj}}{2} - i_{diffj} \end{aligned} \tag{13.3}$$

where i_{diffj} denotes the inner circulating current of phase j, which flows through both the upper and lower arms and is given as

$$i_{diffj} = \frac{i_{pj} - i_{nj}}{2}. \tag{13.4}$$

According to [40], the MMC can be characterized by the following equations:

$$u_{vj} = e_j - \frac{R_{arm}}{2} \cdot i_{vj} - \frac{L_{arm}}{2} \cdot \frac{di_{vj}}{dt} \quad (j = a,b,c) \tag{13.5}$$

$$R_{arm} \cdot i_{diffj} + L_{arm} \cdot \frac{di_{diffj}}{dt} = \frac{V_{dc}}{2} - \frac{u_{nj} + u_{pj}}{2} \quad (j = a,b,c) \tag{13.6}$$

where e_j in (13.5) is the inner emf generated in a phase and

$$e_j = \frac{u_{nj} - u_{pj}}{2} \tag{13.7}$$

According to (13.5), when u_{vj} is regarded as the ac network voltage, the current i_{vj} can be controlled directly by regulating the control variable e_j. The inner dynamic performance of the MMC is characterized by (13.6) and can be redefined as

$$u_{diffj} = R_{arm} \cdot i_{diffj} + L_{arm} \cdot \frac{di_{diffj}}{dt} = \frac{V_{dc}}{2} - \frac{u_{nj} + u_{pj}}{2} \quad (j = a,b,c) \tag{13.8}$$

where u_{diffj} is the inner unbalance voltage of phase j.

According to (13.8), the circulating current i_{diffj} can be controlled by regulating the unbalance voltage u_{diffj}. Combining (13.7) and (13.8), the arm voltage references are

$$\begin{aligned} u_{pj_ref} &= \frac{V_{dc}}{2} - e_j - u_{diffj} \\ u_{nj_ref} &= \frac{V_{dc}}{2} + e_j - u_{diffj} \end{aligned} \tag{13.9}$$

Because the same voltage u_{diffj} is subtracted from u_{pj_ref} and u_{nj_ref}, according to (13.5) and (13.7), the resulting e_j will not change, and thus, the ac side dynamics are not affected. As previously described, the reference of e_j is generated from the traditional system control loops, whereas the inner unbalance voltage u_{diffj} is used to control the MMC inner dynamic performance including the three-phase inner circulating currents.

Due to its unique structure, MMC has two typical issues, which will be discussed in the following sections.

(1) *SM capacitor voltage balancing*

According to the operating principle described above, the arm current in an MMC will only flow through the SM capacitor when the upper switch turns on and the SM is inserted. However, determined by various modulation schemes, the switching state for SMs is different from each other, leading to different charging/discharging times of the SM capacitors and thus voltage deviations. These unbalanced SM capacitor voltages generate the output voltage distortion and bring high-voltage stress to SM capacitors, as illustrated in

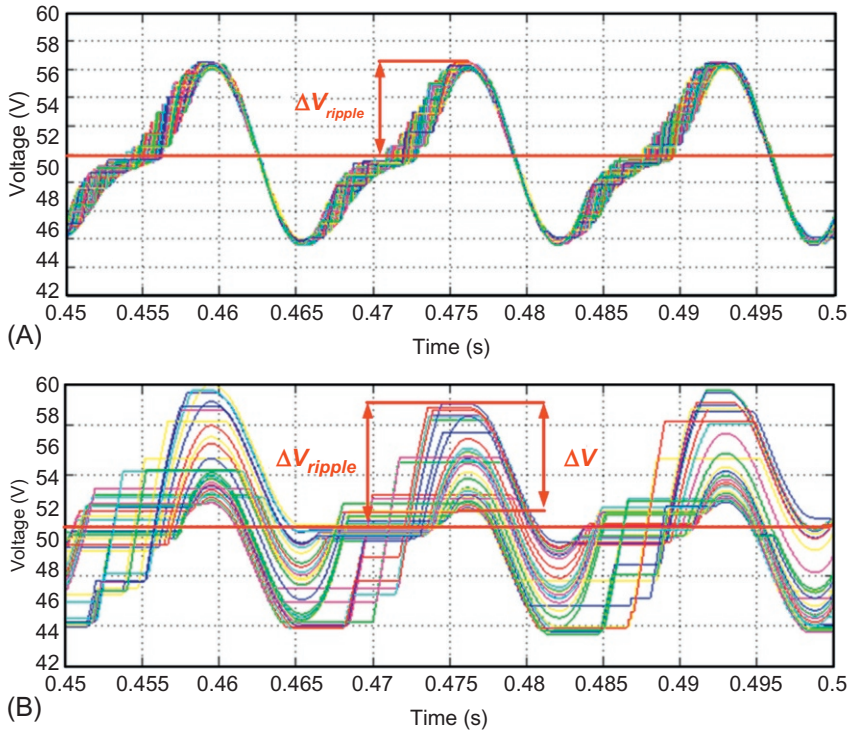


FIG. 13.11 SM capacitor voltages in well-balanced and poorly balanced conditions, (A) well-balanced capacitor voltage and (B) unbalanced capacitor voltage.

Fig. 13.11. To address this issue, several voltage-balancing control schemes have been proposed over the last decade.

In [41], a voltage-balancing control consisting of an averaging control, individual-balancing control, and arm-balancing control was proposed for phase-shifted modulation schemes. The most widely accepted voltage-balancing control is based on a sorting method [42] [43]. The selection criteria are based on (1) SM capacitor voltages and (2) the direction of the arm currents. If the arm current is charging the capacitors, the SMs with the lowest capacitor voltages will be inserted. On the other hand, if the arm current is discharging the capacitors, the SMs with the highest capacitor voltages will be inserted. With this algorithm, the SM capacitor voltages can be well balanced. Here, the total SMs that need to be inserted can be calculated based on different modulation schemes introduced earlier.

The main disadvantage of the above algorithms is the unnecessary switching actions of the SMs. Even if the capacitor voltage deviation is quite low and/or the number of required on-state SMs keep the same within two consecutive control periods, the SM insertion and bypassing may still occur, leading to increased switching frequency and loss. A modified sorting method has been proposed in [44] to avoid the high switching frequency, as shown in Fig. 13.12. In this method, a voltage deviation threshold is set, and the SM switching states only vary under the following two cases:

Case 1: The voltage deviation is larger than the predefined threshold (V_{th}).

Case 2: Different number of SMs need to be inserted.

In Case 1, two SM operation status will be changed based on the arm current direction. If the arm current is charging the capacitors, the SM with the highest capacitor voltage will be bypassed, and the SM with the lowest capacitor voltage will be inserted. If the current is discharging the capacitors in that arm, the SM with the lowest capacitor voltage is bypassed, and the SM with the highest capacitor voltage is inserted. For Case 2, an additional SM will be inserted or bypassed, and the same SM selection scheme in Case 1 is utilized. Due to its easy implementation and reduced switching losses, this modified sorting method with a capacitor voltage deviation threshold is widely used for MMC control.

(2) *Circulating current control*

According to (13.6), if the SM capacitor voltage in Fig. 13.8 equals to V_{dc}/N (V_{dc} is dc link voltage, and N is SM number per arm) all the time, no circulating current will be generated. However, in a real MMC converter, low-frequency voltage ripples exist due to alternating arm current. For modulation schemes assuming constant SM capacitor voltages, for example, the direct modulation in [43], the inserted SM voltages in different half bridges could be different, inducing circulating current among the three phases. The circulating current will not affect the ac output voltage and currents. However, if it is not effectively suppressed, it increases the peak and RMS values of the arm currents, leading to high power losses and large SM capacitor voltage ripples. Under normal operation conditions, the dominant circulating current is negative sequence with second-order harmonic frequency [45,46]. Although the circulating current can be effectively mitigated by increasing the arm inductance, active suppression control schemes are preferred for lower converter volume and cost. A comparative experimental result with and without circulating current suppression control is given in Fig. 13.13 as an example.

Several circulating current suppressing control schemes have been proposed to reduce the circulating current in an MMC [47,48]. The basic idea of these control schemes is injecting a common mode arm

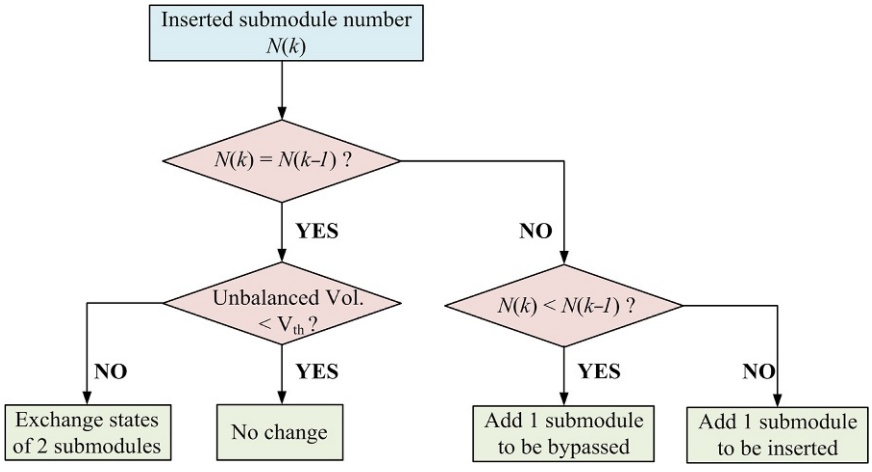
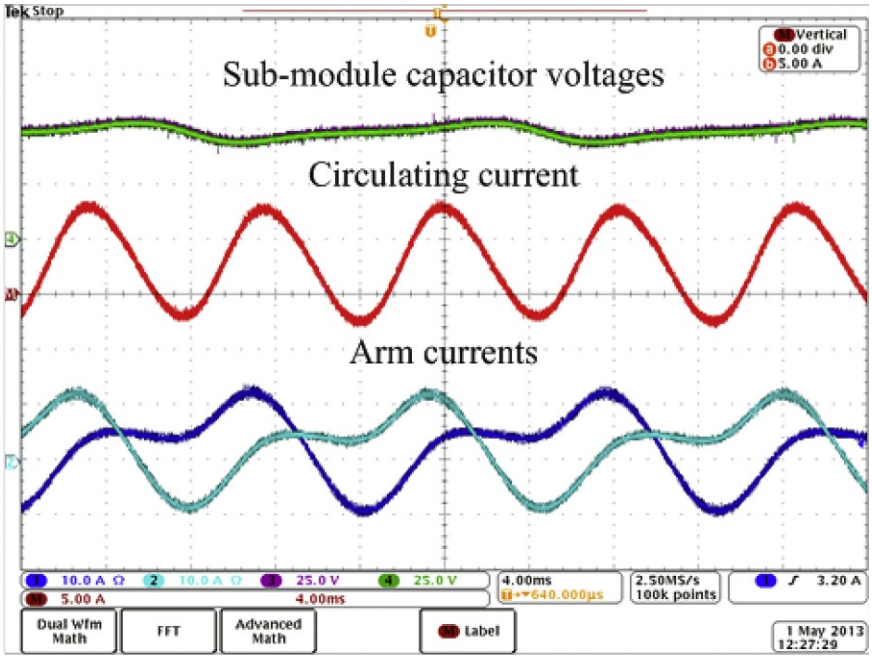
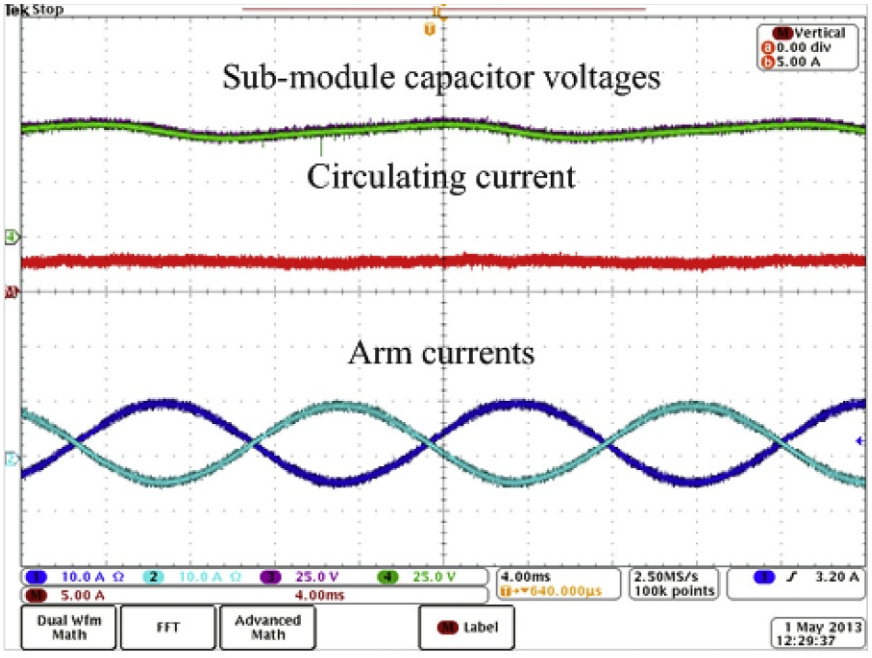


FIG. 13.12 Modified sorting algorithm in Ref. [44].



(A)



(B)

FIG. 13.13 Experimental results with $L_{arm} = 1$ mH and (A) circulating current suppressing control disabled and (B) circulating current suppressing control enabled.

voltage to counteract the submodule capacitor voltage variation. In the indirect modulation schemes proposed in [49,50], the sum of instantaneous capacitor voltages instead of the constant dc link voltage is used for insertion index calculation. In addition, the calculated or estimated total capacitor energy and the unbalanced arm energy are regulated, which inherently limit the circulating current. The second-order circulating current was transformed to d-q coordinates and controlled by a pair of PI controllers in [47]. During normal conditions, the dominant negative sequence second-order circulating current becomes dc components under d-q coordinates

and can be eliminated without steady-state error. However, under ac grid unbalanced conditions, positive and/or zero-sequence circulating current will also be generated, which are ac components under the previous d-q coordinates and cannot be completely removed [51]. As a solution, proportional-resonant (PR)-based controllers were developed in [52,53], targeting elimination of all second-order components in circulating current under abc or αβ coordinates.

13.2.4.1 Advantages

- The number of SMs in each arm depends on the HVDC voltage level and individual IGBT device voltage. For example, with N series-connected SMs per arm, voltage rating of devices is reduced to V_{dc}/N (V_{dc} is dc link voltage), which eliminates the direct series connection of devices in two- and three-level converters. Given that the IGBT ratings are in kV level and HVDC rating is typically in hundreds of kV, often several hundred SMs are used for one MMC [54].
- Higher quality output voltage. With higher number of SMs in each arm (N), the output phase voltage of MMC becomes much more sinusoidal, which enables smaller ac filters, lower cost and compact converter footprint, as illustrated in Fig. 13.14.
- Lower switching frequency and higher efficiency. The series connection of N SMs per arm can achieve an equivalent switching frequency of Nf_c (f_c represents carrier frequency of each device) in the output voltage. In practical applications, the device average switching frequency is generally below 200 Hz. Consequently, state-of-the-art MMC-HVDC has loss level about 1%, close to that of LCC.
- Lower high-frequency noise due to reduced dv/dt and di/dt.
- Modular design and inherent redundancy. The modular design of MMC contributes to lower cost, shorter manufacturing as well as maintenance period, and high extensibility for higher voltage and power applications. Furthermore, the system becomes more reliable since failed SMs can be easily replaced by redundant ones [55].

The comparison of site footprint, building area, and building volumes for LCC-HVDC (Grita project, 500 MW and 400 kV), two-level VSC-HVDC, and half-bridge MMC-HVDC (EWIC project, 500 MW and ±200 kV) is presented in Table 13.3, using the Grita project as the 100% reference [56]. Different from LCC-HVDC, the converter reactors and dc yard equipment in VSC-HVDC are mounted in converter buildings, which provide more convenient maintenance, improved personal safety, lower high-frequency emissions and acoustic noise, and protection for equipment from adverse weather.

Without the requirement for reactive power compensation, the overall site area for two-level VSC-HVDC is 77% of that for LCC-HVDC, in spite of its higher converter building footprint, height, and volume. By adopting MMC, the site area is further reduced to only 58% of the reference value, and lower building height is achieved because of a decreased internal suspension height of converter valves. The overall site area reduction of MMC-HVDC supplies a significant benefit, especially for locations with restricted available area and/or high land price.

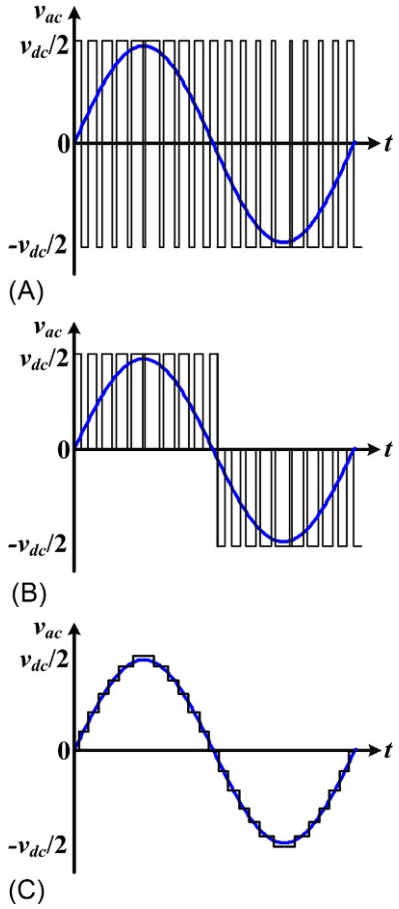


FIG. 13.14 Output ac voltage of a (A) two-level converter, (B) three-level converter, and (C) MMC.

13.2.4.2 Disadvantages

- To meet the requirement for capacitor voltage ripple, C_{sub}/N should be constant, which makes the power stage dimensioning quite difficult, especially for a MMC with numerous SMs per arm. Each SM requires a gate drive, protection, capacitor voltage monitoring, and associated communication resources, which greatly increase the cost of the system.
- The control scheme becomes much more complicated than that in a two-level converter. In addition to the generic upper level control to meet the overall system behavior requirements (V_{dc}-Q, P-Q, etc.), the capacitor voltage-balancing control and circulating current suppression control are indispensable in a MMC for desirable

TABLE 13.3 Comparison of site areas among LCC and two-level VSC- and MMC-based HVDC systems [56]

	Site footprint	Site area (%)	Max building height (%)	Converter building footprint	Converter building area (%)	Converter building volume (%)
LCC-HVDC (reference)	225 m × 120 m	27,000 m^2 (100%)	20 m (100%)	35 m × 20 m	700 m^2 (100%)	14,000 m^2 (100%)
Two-level VSC	180 m × 115 m	20,700 m^2 (77%)	24 m (120%)	38 m × 35 m	1330 m^2 (190%)	25,000 m^2 (179%)
Half-bridge MMC-HVDC	165 m × 95 m	15,675 m^2 (58%)	15 m (75%)	70 m × 45 m	2730 m^2 (390%)	29,500 m^2 (211%)

operation performance, and to lower the voltage and current stress applied on semiconductor devices and passive components. Because of the demand for accurate capacitor voltage and arm current detection and/or high-speed communication, these control schemes will introduce considerable expense and computing burden to the control unit.

13.2.5 Other Multilevel Inverter Structures

Besides the four basic multilevel inverter topologies discussed earlier, other multilevel converter topologies have been proposed; however, most of these are "hybrid" circuits that are combinations of two of the basic multilevel topologies or slight variations to them. In addition, the combination of multilevel power converters can be designed to match with a specific application based on the basic topologies. In the interest of completeness, some of these will be identified and briefly described.

13.2.4.1 Generalized Multilevel Topology

Existing multilevel converters such as diode-clamped and capacitor-clamped multilevel converters can be derived from the generalized converter topology called P2 topology proposed by Peng [57] as shown in Fig. 13.15. The generalized multilevel converter topology can balance each voltage level by itself regardless of load characteristics, active or reactive power conversion, and without any assistance from other circuits at any number of levels automatically. Thus, the topology provides a complete multilevel topology that embraces the existing multilevel converters in principle.

Fig. 13.15 shows the P2 multilevel converter structure per phase leg. Each switching device, diode, or capacitor's voltage is $1V_{dc}$, for instance, $1/(m-1)$ of the dc link voltage. Any converter with any number of levels, including the conventional bilevel converter, can be obtained using this generalized topology [1,57].

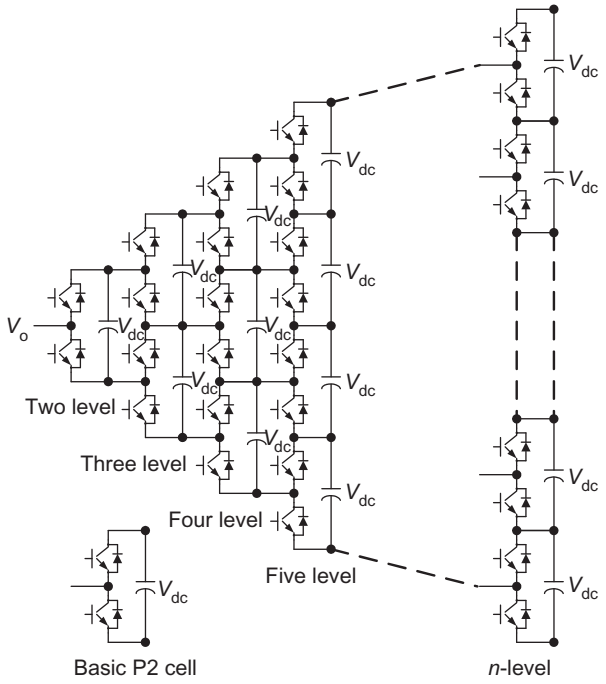


FIG. 13.15 Generalized P2 multilevel converter topology for one phase leg.

13.2.4.2 Mixed-Level Hybrid Multilevel Converter

To reduce the number of separate dc sources for high-voltage,-high-power applications with multilevel converters, diode-clamped or capacitor-clamped converters can be used to replace the full-bridge cell in a cascaded converter [58]. An example is shown in Fig. 13.16. The nine-level cascade converter incorporates a three-level diode-clamped converter as the cell. The original cascaded H-bridge multilevel converter requires four separate dc sources for one phase leg and 12 for a three-phase converter. If a five-level converter replaces the full-bridge cell, the voltage level is effectively doubled for each cell. Thus, to achieve the same nine voltage levels for each phase, only two separate dc sources are needed for one phase leg and six for a three-phase converter. The configuration has mixed-level hybrid multilevel units because it embeds multilevel cells as the building block of the cascade converter. The advantage of the topology is it needs less separate dc sources. The disadvantage for the topology is its control will be complicated due to its hybrid structure.

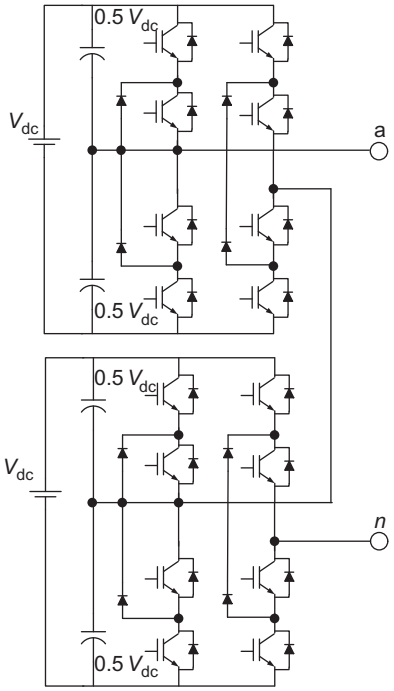


FIG. 13.16 Mixed-level hybrid unit configuration using the three-level diode-clamped converter as the cascaded converter cell to increase the voltage levels.

13.2.4.3 Soft-Switched Multilevel Converter

Some soft-switching methods can be implemented for different multilevel converters to reduce the switching loss and to increase efficiency. For the cascaded converter, because each converter cell is a bilevel circuit, the implementation of soft switching is not at all different from that of conventional bilevel converters. For capacitor-clamped or diode-clamped converters, soft-switching circuits have been proposed with different circuit combinations. One of the soft-switching circuits is a zero-voltage-switching type that includes auxiliary resonant commutated pole (ARCP), coupled inductor with zero-voltage transition (ZVT), and their combinations [1,59] as shown in Fig. 13.17.

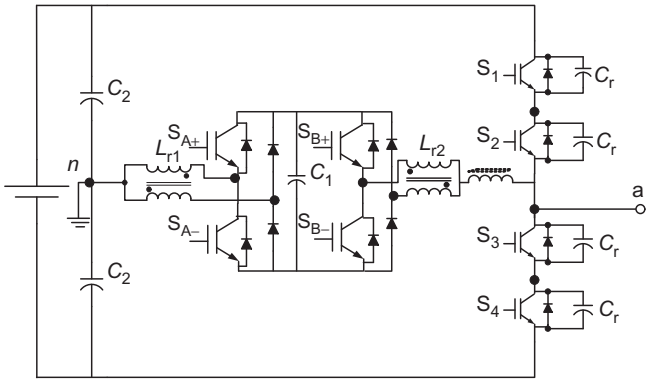


FIG. 13.17 Zero-voltage-switching capacitor-clamped inverter circuit.

13.2.4.4 Back-to-Back Diode-Clamped Converter

Two multilevel converters can be connected in a back-to-back arrangement, and then, the combination can be connected to the electric system in a series-parallel arrangement as shown in Fig. 13.18. Both the current demanded from the utility and the voltage delivered to the load can be controlled at the same time. This series-parallel active power filter has been referred to as a universal power conditioner [60–66] when used on electric distribution systems and as a universal power flow controller [67–71] when applied at the transmission level. Earlier, Lai and Peng [29] proposed the back-to-back diode-clamped topology shown in Fig. 13.19 for use as a high-voltage dc interconnection between two asynchronous ac systems or as a rectifier or inverter for an adjustable speed drive for high-voltage motors. The diode-clamped inverter has been chosen over the other two basic multilevel circuit topologies for use in a universal power conditioner for the following reasons:

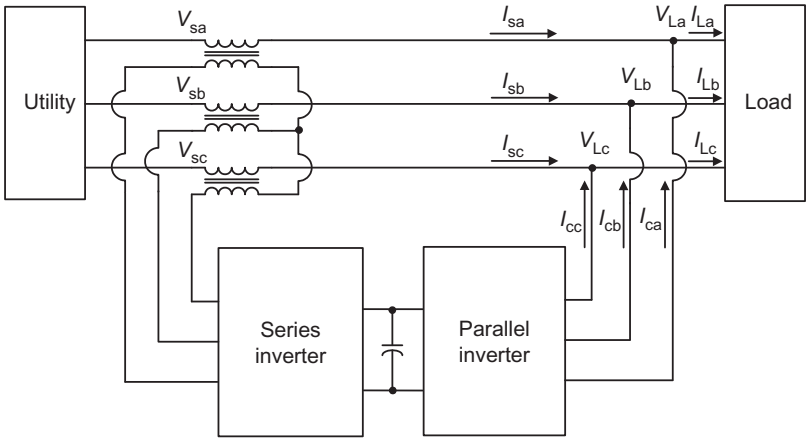


FIG. 13.18 Series-parallel connection to electric system of two back-to-back inverters.

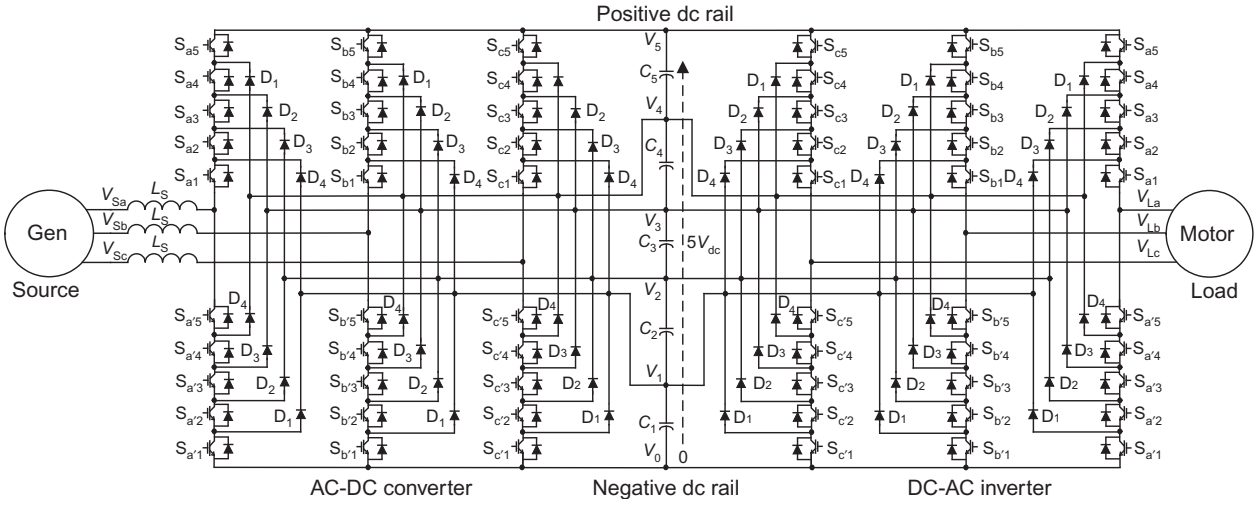


FIG. 13.19 Six-level diode-clamped back-to-back converter structure.

- All six phases (three on each inverter) can share a common dc link. Conversely, the cascade inverter requires that each dc level to be separate, and this is not conducive to a back-to-back arrangement.
- The multilevel flying-capacitor converter also shares a common dc link; however, each phase leg requires several additional auxiliary capacitors. These extra capacitors would add substantially to the cost and the size of the conditioner.

Because a diode-clamped converter acting as a universal power conditioner will be expected to compensate for harmonics and/or operate in low-amplitude modulation index regions, a more sophisticated higher frequency switch control than the fundamental frequency switching method will be needed. For this reason, multilevel space vector and carrier-based PWM approaches are compared in the next section and novel carrier-based PWM methodologies are given.

13.3 Multilevel Converter PWM Modulation Strategies

Pulse-width modulation strategies used in a conventional inverter can be modified to use in multilevel converters. The advent of the multilevel converter PWM modulation methodologies can be classified according to switching frequency as shown in Fig. 13.20. The three multilevel PWM methods most discussed in the literature have been multilevel carrier-based

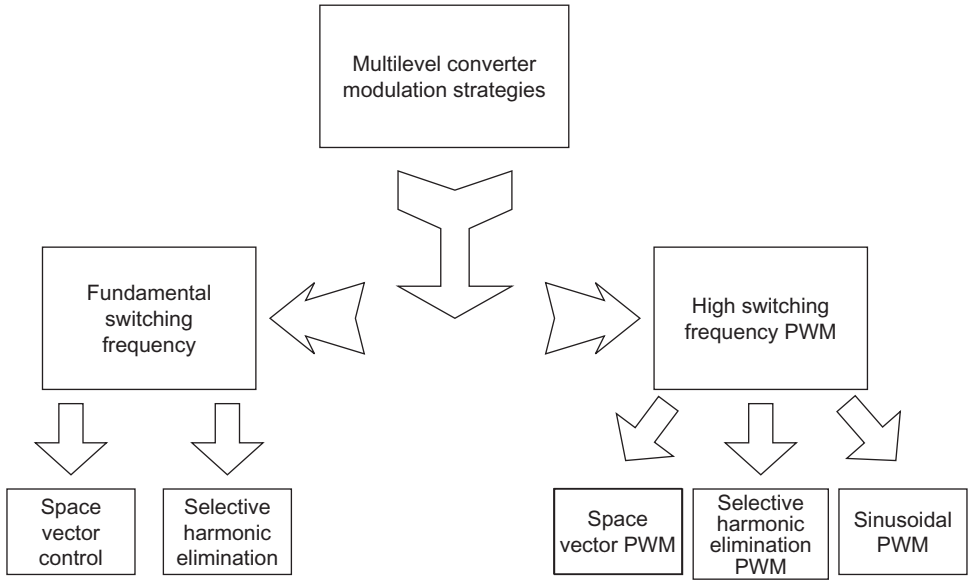


FIG. 13.20 Classification of PWM multilevel converter modulation strategies.

PWM, selective harmonic elimination, and multilevel space vector PWM, which are all extensions of traditional two-level PWM strategies to several levels. Other multilevel PWM methods have been used to a much lesser extent by researchers; therefore, only the three major techniques will be discussed in detail in this chapter.

On the other hand, for MMC with tens to hundreds of SMs, new modulation schemes, for example, nearest level control (NLC), have been proposed for lower switching frequency and easy implementation, which will also be introduced in this chapter.

13.3.1 Multilevel Carrier-Based PWM

Several different two-level, carrier-based PWM techniques have been extended to multiple levels as a means for controlling the active devices in a multilevel converter. The most popular and easiest technique to implement uses several triangle carrier signals and one reference, or modulation, signal per phase. Fig. 13.21 illustrates three major techniques used in a conventional inverter that can be applied in a multilevel inverter: sinusoidal PWM (SPWM), third-harmonic injection PWM (THPWM), and space vector PWM (SVM). SPWM is a very popular method in industrial applications.

In order to achieve better dc link utilization at high modulation indexes, the sinusoidal reference signal can be injected by a third harmonic with a magnitude equal to 15% of the fundamental; its line-line output voltage is shown in Fig. 13.21B. As can be seen in Fig. 13.21B and C, the reference signals have some margin at unity amplitude modulation index. Obviously, the dc utilization of THPWM and SVM are better than SPWM in the linear modulation region. The dc utilization means the ratio of the output fundamental voltage to the dc link voltage. Other interesting carrier-based multilevel PWM are subharmonic PWM (SH-PWM) and switching frequency optimal PWM (SFO-PWM). Some particular aspects of these carrier-based methods are discussed as follows.

13.3.1.1 Subharmonic PWM

Carrara et al. [72] extended SH-PWM to multiple levels as follows: for an m-level inverter, $m-1$ carriers with the same frequency f_c and the same amplitude A_c are disposed such that the bands they occupy are contiguous. The reference waveform has peak-to-peak amplitude A_m, a frequency f_m, and its zero centered in the middle of the carrier set. The reference signal is continuously compared with each of the carrier signals. If the reference signal is greater than a carrier signal, then the active device corresponding to that carrier is switched on, and if the reference signal is lesser than a carrier signal, then the active device corresponding to that carrier is switched off.

In multilevel inverters, the amplitude modulation index, m_a, and the frequency ratio, m_f, are defined as

$$m_a = \frac{A_m}{(m-1)\cdot A_c} \tag{13.10}$$

$$m_f = \frac{f_c}{f_m} \tag{13.11}$$

Fig. 13.22 shows a set of carriers $(m_f = 21)$ for a six-level diode-clamped inverter and a sinusoidal reference or modulation waveform, with an amplitude modulation index of 0.8. Fig. 13.22 also shows the resulting output voltage of the inverter.

13.3.1.2 Switching Frequency Optimal PWM

Another carrier-based method that was extended to multilevel applications by Menzies et al. is termed *SFO-PWM*, and it is similar to SH-PWM except that a zero-sequence (triplen harmonic) voltage is added to each of the carrier waveforms [73]. This method takes the instantaneous average of the maximum and minimum of the three reference voltages $\left(V_a^*, V_b^*, V_c^*\right)$ and subtracts this value from each of the individual reference voltages, that is,

$$V_{offset} = \frac{\max\left(V_a^*, V_b^*, V_c^*\right) + \min\left(V_a^*, V_b^*, V_c^*\right)}{2} \tag{13.12}$$

$$V_{aSFO}^* = V_a^* - V_{offset} \tag{13.13}$$

$$V_{bSFO}^* = V_b^* - V_{offset} \tag{13.14}$$

$$V_{cSFO}^* = V_c^* - V_{offset} \tag{13.15}$$

The addition of this triplen-offset voltage centers all of the three reference waveforms in the carrier band, which is equivalent to using space vector PWM [74,75]. The analog equivalent of Eqs. (13.12)–(13.15) is shown in Fig. 13.23 [76]. The SFO-PWM is shown in Fig. 13.24 for the same reference voltage waveform that was used in Fig. 13.22. The resulting output voltage of the inverter is also shown in Fig. 13.24. The SFO-PWM technique enables the modulation index to be increased by 15% before the overmodulation region is reached.

For the SH-PWM and SFO-PWM techniques shown in Figs. 13.22 and 13.24, the top and bottom switches are switched much more often than the intermediate devices. Methods to balance or reduce the device switchings without an adverse effect on a multilevel inverter's output voltage total harmonic distortion would be beneficial. The development of such methods is discussed in [77]. A novel method to balance device switchings for all of the levels in a diode-clamped inverter has been demonstrated for SH-PWM and SFO-PWM by varying the frequency for the different triangle wave carrier bands as shown in Fig. 13.25 [77].

13.3.1.3 Modulation Index Effect on Level Utilization

For low-amplitude modulation indexes, a multilevel inverter will not make use of all of its levels, and at very low modulation indexes, it operates as if it is a traditional two-level inverter.

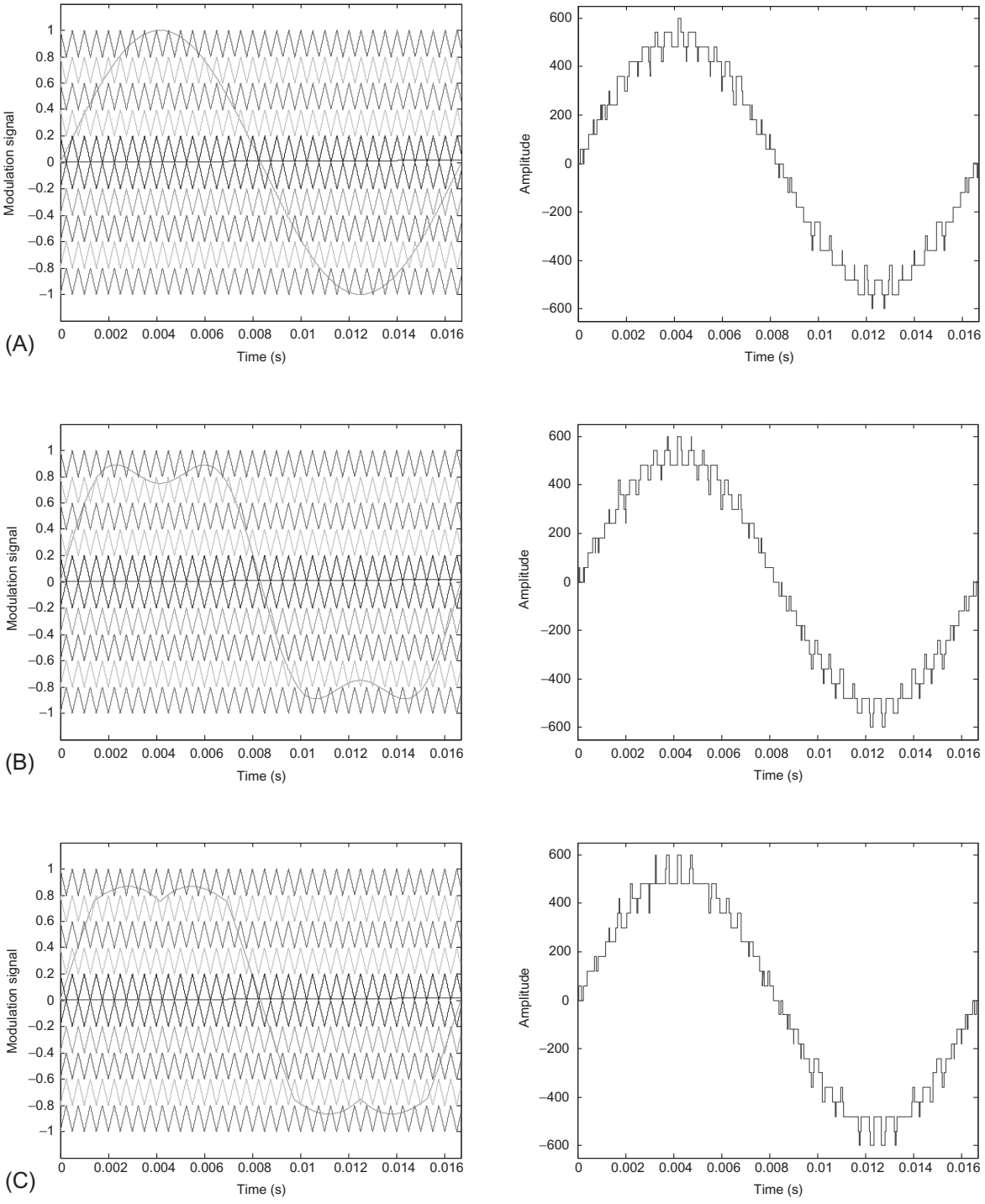


FIG. 13.21 Simulation of modulation signals and their line-line output voltage using five separate dc source (60 V for each dc source) cascaded multilevel inverter with three major conventional carrier-based PWM techniques at unity modulation index and 2 kHz switching frequency: (A) SPWM, (B) THPWM, and (C) SVM.

Fig. 13.26 shows two simulation results of what the output voltage waveform looks like at amplitude modulation indexes of 0.5 and 0.15. Fig. 13.26A shows how the bottom and top switches ($S_{a1} - S_{a'1}$, $S_{a5} - S_{a'5}$ in Fig. 13.5) are unused for amplitude modulation indexes less than 0.6 in a six-level inverter. Fig. 13.26B shows how only the middle switches ($S_{a3} - S_{a'3}$ in Fig. 13.5) change states when a six-level inverter is operated at an amplitude modulation index less than 0.2. The output waveform in Fig. 13.26B appears to be that of a traditional two-level inverter rather than a multilevel inverter.

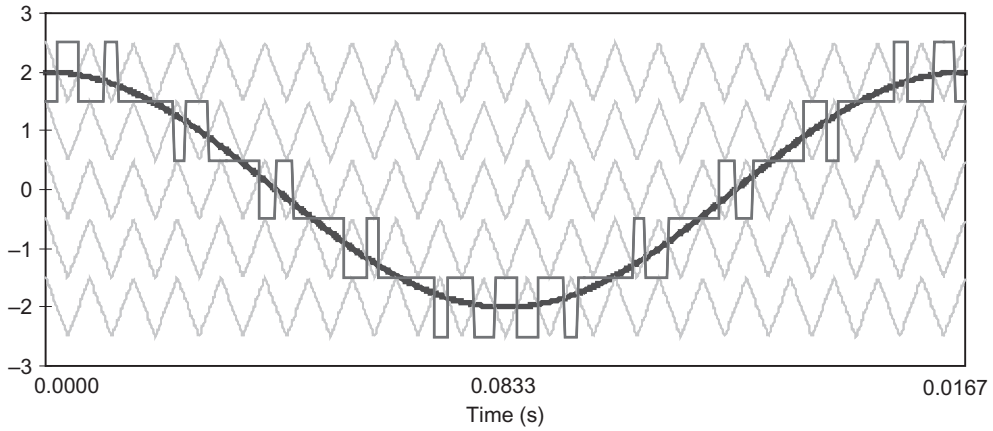


FIG. 13.22 Multilevel carrier-based SH-PWM showing carrier bands, modulation waveform, and inverter output waveform ($m = 6, m_f = 21, m_a = 0.8$).

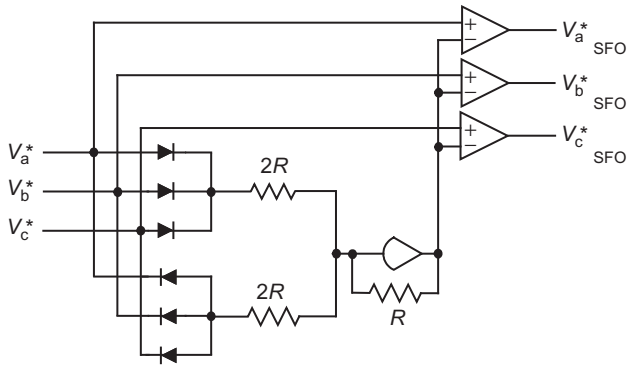


FIG. 13.23 Analog circuit for zero-sequence addition in SFO-PWM.

The minimum modulation index m_{amin}, for which a multilevel inverter controlled with SH-PWM makes use of all of its levels, m, is

$$m_{amin} = \frac{m-3}{m-1} \tag{13.16}$$

Table 13.4 lists the minimum modulation index in which a multilevel inverter uses all its constituent levels for both SH-PWM and SFO-PWM techniques. Table 13.4 also shows that the maximum modulation index before pulse dropping (overmodulation) occurs is 1.000 for SH-PWM and 1.155 for SFO-PWM. As shown in Table 13.4, when a multilevel inverter operates at modulation indexes much less than 1.000, not all of its levels are involved in the generation of the output voltage and simply remain in an unused state until the modulation index increases sufficiently. The table also shows that level usage is more likely to suffer to a greater extent as the number of levels in the inverter increases.

One way to make use of the multiple levels, even during low modulation periods, is to take advantage of the redundant output voltage states by rotating level usage in the inverter after each modulation cycle. This will reduce the switching stresses on some of the inner levels by making use of those outer voltage levels that otherwise would go unused.

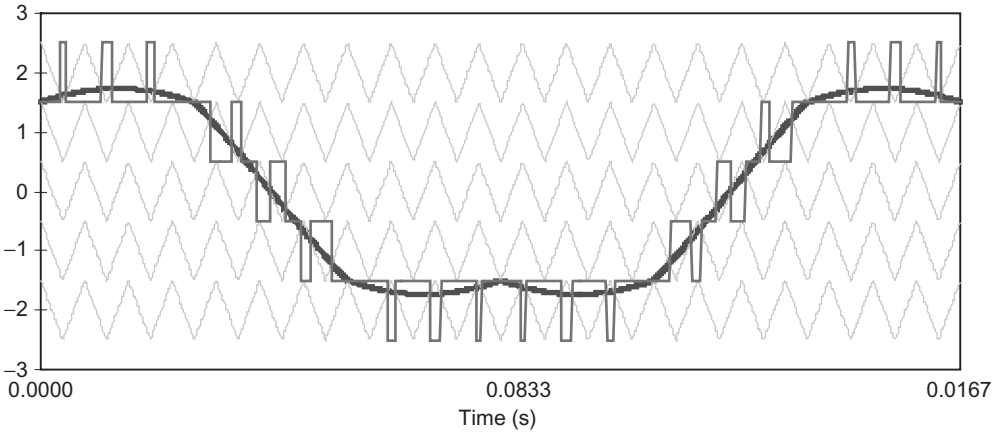


FIG. 13.24 Multilevel carrier-based SFO-PWM showing carrier bands, modulation waveform, and inverter output waveform ($m = 6, m_f = 21, m_a = 0.8$).

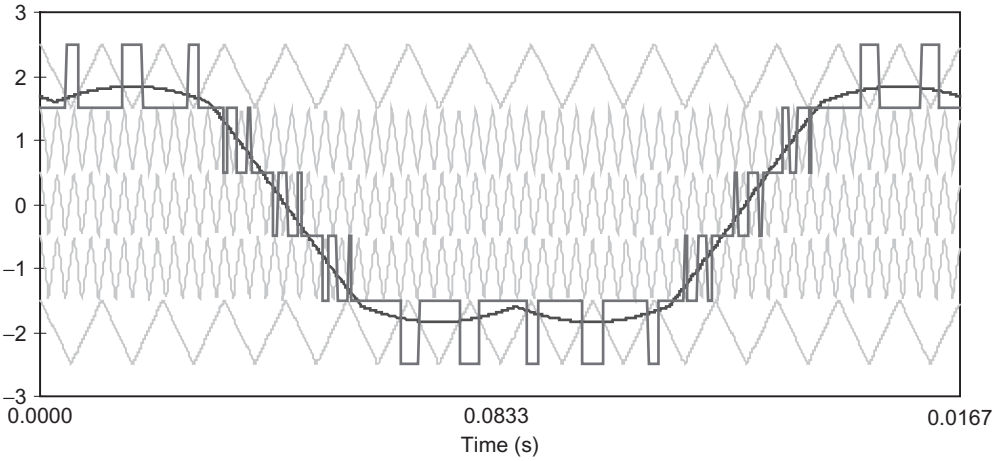


FIG. 13.25 SFO-PWM where carriers have different frequencies ($m_a = 0.85, m_f = 15$ for $Band_2$, $Band_{-2}$; $m_f = 55$ for $Band_1$, $Band_{-1}$; $Band_0$, $\phi = 0.10$ rad).

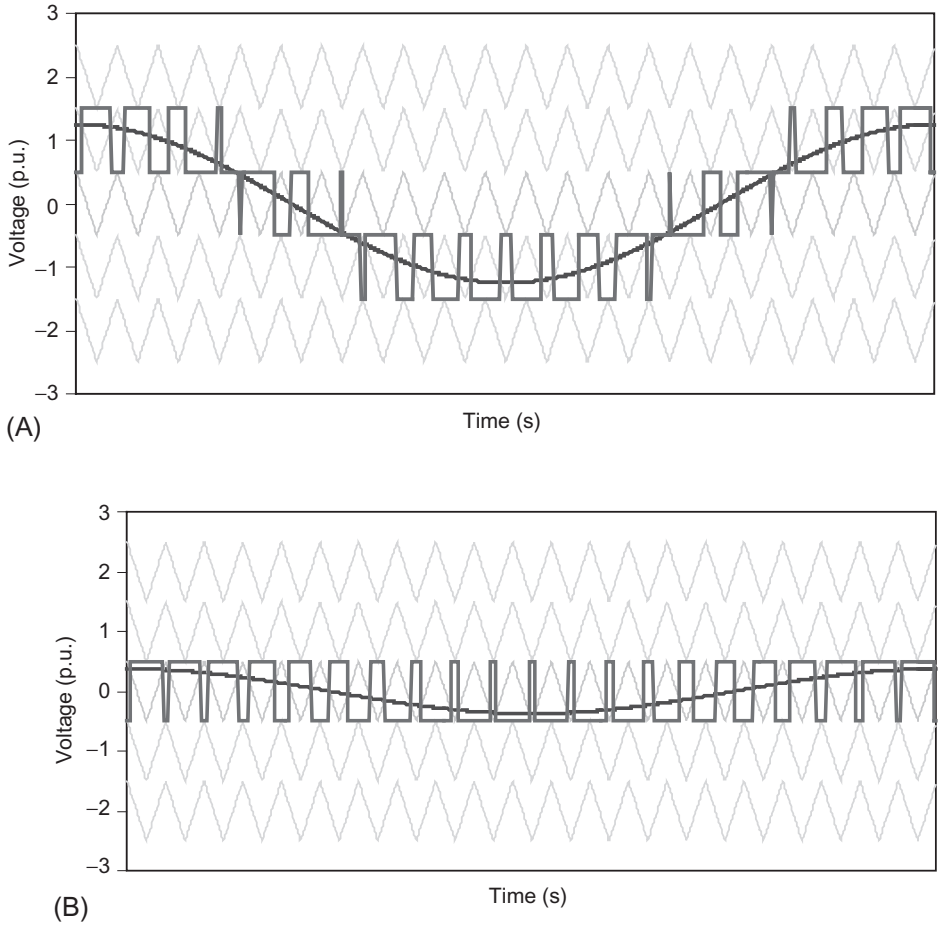


FIG. 13.26 Level reduction in a six-level inverter at low modulation indexes: (A) SH-PWM, $m = 6, m_a = 0.5$ and (B) SH-PWM, $m = 6, m_a = 0.15$.

TABLE 13.4 Modulation index ranges without level reduction (min) or pulse dropping because of overmodulation (max)

	SH-PWM		SFO-PWM	
Levels	Min	Max	Min	Max
3	0.000	1.000	0.000	1.155
4	0.333	1.000	0.385	1.155
5	0.500	1.000	0.578	1.155
6	0.600	1.000	0.693	1.155
7	0.667	1.000	0.770	1.155
8	0.714	1.000	0.825	1.155
9	0.750	1.000	0.866	1.155
10	0.778	1.000	0.898	1.155
11	0.800	1.000	0.924	1.155
12	0.818	1.000	0.945	1.155
13	0.833	1.000	0.962	1.155

As mentioned earlier, diode-clamped inverters have redundant line-line voltage states for low modulation indexes but have no phase redundancies [78]. For an output voltage state (i,j,k) in an m-level diode-clamped inverter, the number of redundant states available is given by

$$N_{\substack{\text{redundancies}\\\text{available}}} = m - 1 - [\max(i,j,k) - \min(i,j,k)] \qquad (13.17)$$

As the modulation index decreases, more redundant states are available. Table 13.5 shows the number of distinct and redundant line-line voltage states available in a six-level inverter for different output voltages.

In the next section, a carrier-based method is given that uses line-line redundancies in a diode-clamped inverter operating at a low modulation index so that active device usage is more balanced among the levels.

13.3.1.4 Increasing Switching Frequency at Low Modulation Indexes

For amplitude modulation indexes less than 0.5, the level usage in odd-level inverters can be sufficiently rotated so that the switching frequency can be doubled and still keep the thermal losses within the limits of the device. For inverters with an even number of levels, the modulation index at which frequency doubling can be accomplished varies with the levels as shown in Table 13.6. This increase in switching frequency enables the inverter to compensate for higher frequency harmonics and yields a waveform that more closely tracks a reference.

As an example of how to accomplish this doubling of inverter frequency, an analysis of a seven-level diode-clamped inverter with an amplitude modulation index of 0.4 is conducted. During the first cycle, the reference waveform is centered in the upper three carrier bands, and during the next cycle, the reference waveform is centered in the lower three carrier bands as shown in Fig. 13.27. This technique enables half of the switches to "rest" every other cycle and does not incur any switching losses. With this method, the switching frequency (or carrier frequency f_c in the case of multilevel inverters) can effectively be doubled to $2f_c$, but the switches will have the same thermal losses as if they were switching at f_c but every cycle.

This method is possible only for three-wire systems because the diode-clamped inverter has line-line redundancies and no phase redundancies. This means that at the discontinuity where the reference moves from one carrier band set to another, the

TABLE 13.5 Six-level inverter line-line voltage redundancies

$\max(i,j,k) - \min(i,j,k)$	Number of distinct states	Number of redundancies per distinct state	Total number of states
0	1	5	6
1	6	4	30
2	12	3	48
3	18	2	54
4	24	1	48
5	30	0	30
Total	91	—	216

TABLE 13.6 Increased switching frequency possible at lower modulation indexes

	Modulation index, m_a		
Inverter levels	Min	Max	Frequency multiplier
3	0.000	0.500	2×
4	0.000	0.333	3×
5	0.250	0.500	2×
	0.000	0.250	4×
6	0.200	0.400	2×
	0.000	0.200	5×
7	0.333	0.500	2×
	0.167	0.333	3×
	0.000	0.167	6×
8	0.285	0.428	2×
	0.142	0.285	3×
	0.000	0.142	7×
9	0.25	0.500	2×
	0.125	0.250	4×
	0.000	0.125	8×
10	0.333	0.444	2×
	0.222	0.333	3×
	0.111	0.222	4×
	0.000	0.111	9×
11	0.333	0.500	2×
	0.200	0.333	3×
	0.000	0.200	5×
12	0.272	0.454	2×
	0.181	0.272	3×
	0.090	0.181	5×
	0.000	0.090	11×
13	0.333	0.500	2×
	0.250	0.333	3×
	0.167	0.250	4×
	0.0833	0.167	6×
	0.000	0.0833	12×

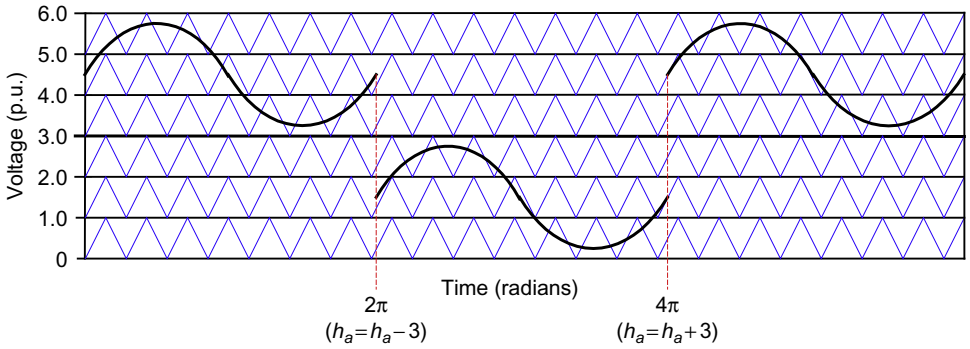


FIG. 13.27 Reference rotation among carrier bands at low modulation indexes ($m_a < 0.5$).

transition has to be synchronized such that all three phases are moved from one carrier set to the next set at the same time. In the case of frequency doubling, all three phases add or subtract the following number of states (or levels) every other reference cycle:

$$h_a(j+1) = h_a(j) + (-1)^j \cdot \frac{\lfloor m-1 \rfloor}{2} \tag{13.18}$$

At modulation indexes closer to zero, the switching frequency can be increased even more. This is possible because the reference waveform can be rotated among the carrier bands for a few cycles before returning to a previous set of switches for use. The switches are allowed to "rest" for a few cycles and thus are able to absorb higher losses during the cycle they are switched. Table 13.6 shows the possible increased switching frequencies available at lower amplitude modulation indexes for several different inverter levels.

Some additional switching loss is associated with the redundant switchings of the three phases at the end of each modulation cycle when rotating among carrier bands. For instance, for Fig. 13.28, each of the three phases in the seven-level inverter will have three switch pairs that change states at the end of every reference cycle. However, compared with the switching loss associated with just the normal PWM switchings, this redundant switching loss is quite small, typically less than 5% of the total switching loss.

Figs. 13.28 and 13.29 show two different methods of rotating the reference waveform among three different regions (top, middle, and bottom) for modulation indexes less than 0.333 in a seven-level inverter to enable the carrier frequency to be increased by a factor of three. The method shown in Fig. 13.28 is preferred over that shown in Fig. 13.29 because of less redundant state switching. The method shown in Fig. 13.28 requires only four redundant state switchings for every three reference cycles, whereas the method shown in Fig. 13.29 requires eight redundant switchings for every three reference cycles. In general, for any multilevel inverter regardless of the number of levels or number of rotation regions, using the preferred reference rotation method will have half of the redundant switching losses that the alternate method would have.

Unlike the diode-clamped inverter, the cascaded H-bridge inverter has phase redundancies in addition to the aforementioned line-line redundancies. Phase redundancies are much easier to exploit than line-line redundancies because the output voltage in each phase of a three-phase inverter can be generated independently of the other two phases when only phase redundancies are used. A method was given in [18] that makes use of

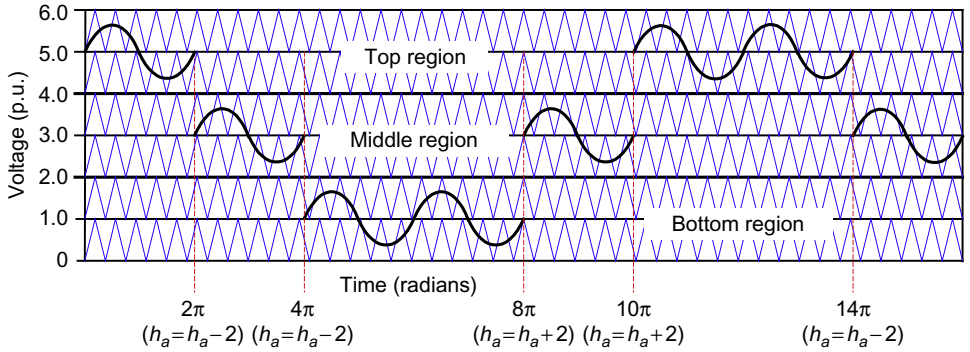


FIG. 13.28 Preferred method of reference rotation among carrier bands with 3× carrier frequency at very low modulation indexes.

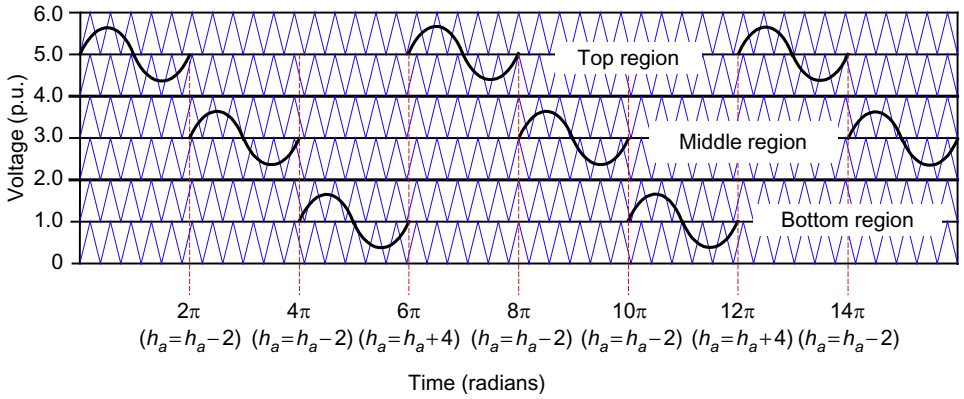


FIG. 13.29 Alternate method of reference rotation among carrier bands with 3× carrier frequency at very low modulation indexes.

these phase redundancies in a cascaded inverter so that duty cycle of each active device is balanced over $(m-1)/2$ modulation waveform cycles regardless of the modulation index. The same pulse rotation technique used for fundamental frequency switching of cascade inverters was used but with a PWM output voltage waveform [79], which is a much more effective means of controlling a driven motor at low speeds than continuing to do fundamental frequency switching. The effect of this control is that the output waveform can have a high switching frequency, but the individual levels can still switch at a constant switching frequency of 60 Hz if desired.

13.3.1.5 Multicarrier Modulation Techniques for MMC

The multicarrier techniques have also been successfully extended for MMC by using multiple carriers to control power switches of the converter topologies. It is mainly divided into two types: (1) carrier phase-shifted PWM (CPS-PWM) and (2) carrier level-shifted PWM (CLS-PWM) [80,81].

(1) *CPS-PWM*

For an MMC with 2N cells, the carrier waves (either sawtooth or triangular waveforms) with a phase shift of 360 degrees/N or 180 degrees/N can be employed to generate the staircase multilevel output waveform with low distortion. The modulation and output voltage waveforms for $N+1$ and $2N+1$ levels ($N=4$) are given in Figs. 13.30 and 13.31, respectively.

With $N+1$ level modulation scheme (phase shift of 360 degrees/N among carriers), N SMs per phase are inserted at all times, leading to a balanced capacitor voltage. In contrast, if $2N+1$ level modulation scheme (phase shift of 180 degrees/N among carriers) is used, $N+1$ or $N-1$ SMs will be inserted at certain time, causing issues with the capacitor voltage self-balancing algorithm and requiring additional balancing control. Using PS-PWM modulation algorithm, the effective switching frequency of the load voltage will be much higher that of each cell (Nf_c for $N+1$ level and $2Nf_c$ for $2N+1$ level, f_c is the carrier frequency). This property allows low switching frequency of each SM, thus reducing switching losses. In addition, it enables a high degree of linearity, outstanding control performance, and other advantages.

(2) *CLS-PWM*

The carriers can also be arranged with shifts in amplitude, relating each carrier with the corresponding output voltage level generated by the multilevel inverter, which is the so-called level-shifted PWM (LS-PWM). Depending on the disposition of the carriers, three types of CLS-PWM have been developed: phase disposition (PD), phase opposition disposition (POD), and alternate phase opposition disposition (APOD), as shown in Fig. 13.32.

The PD-PWM method is realized through a comparison between a sinusoidal reference wave with vertically shifted carrier waves. N carrier signals will be created to generate an output voltage with $N+1$ levels. The carrier signals have the same amplitude and frequency, and all signals are in phase. In the POD-PWM method, all carrier signals above the zero axis (positive region) are in phase, and those below zero axis (negative region) are also in phase but 180 degrees phase shifted from the carrier waves in positive region. The APOD-PWM scheme requires N − 1 carrier signals with phase shift of 180 degrees from each other.

The LS-PWM methods can be adopted for any multilevel converter topology. However, they are not very suitable for CHB (cascaded H-bridge converter) and MMC inverters. According to the modulation principle, the uppermost SMs will be inserted for a short time, while the middle ones insert for most of the time during a fundamental cycle, producing an uneven power dissipation and large capacitor voltage differences among the SMs.

13.3.2 Multilevel Space Vector PWM

Choi et al. [82] were the first authors to extend the two-level space vector PWM technique to more than three levels for

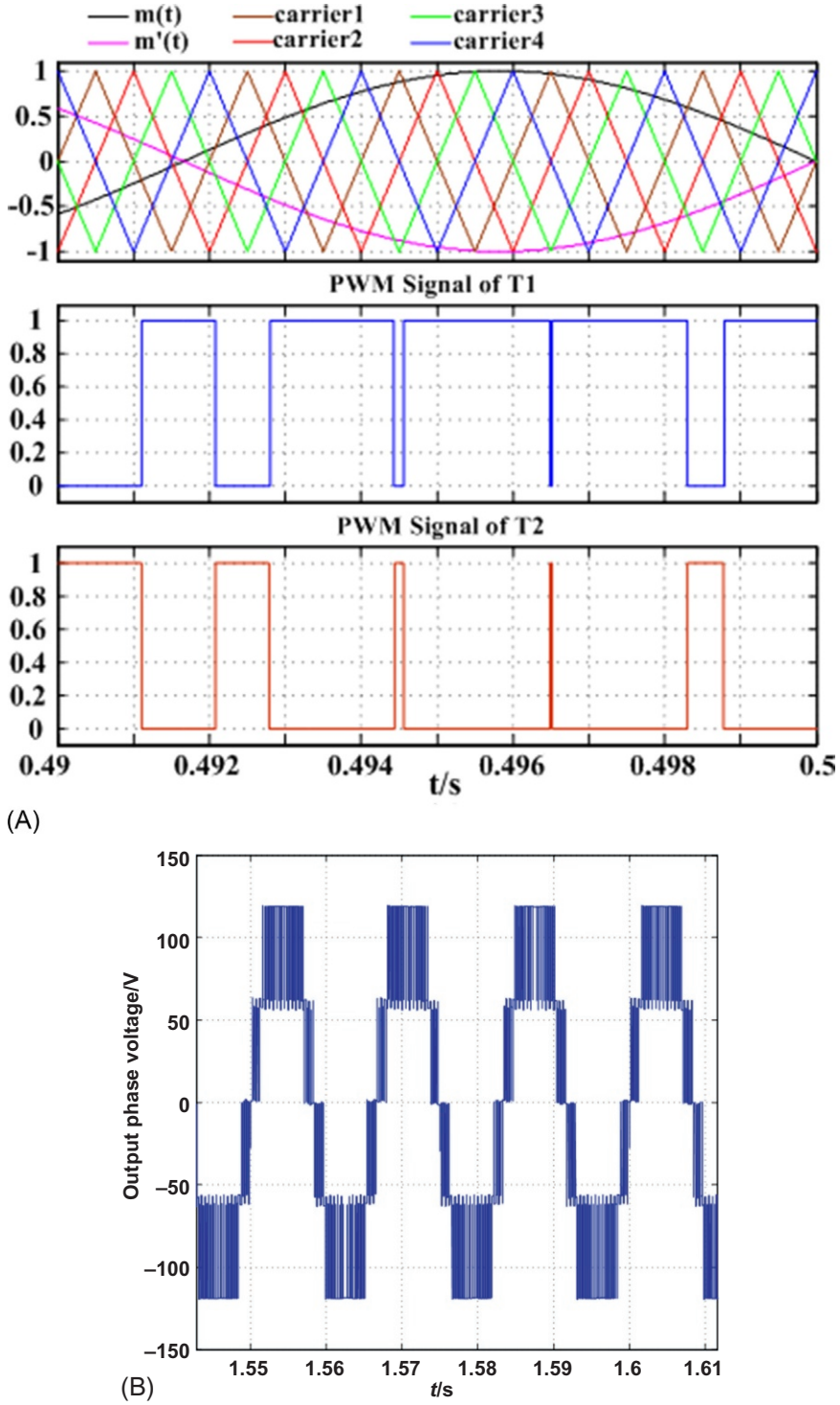
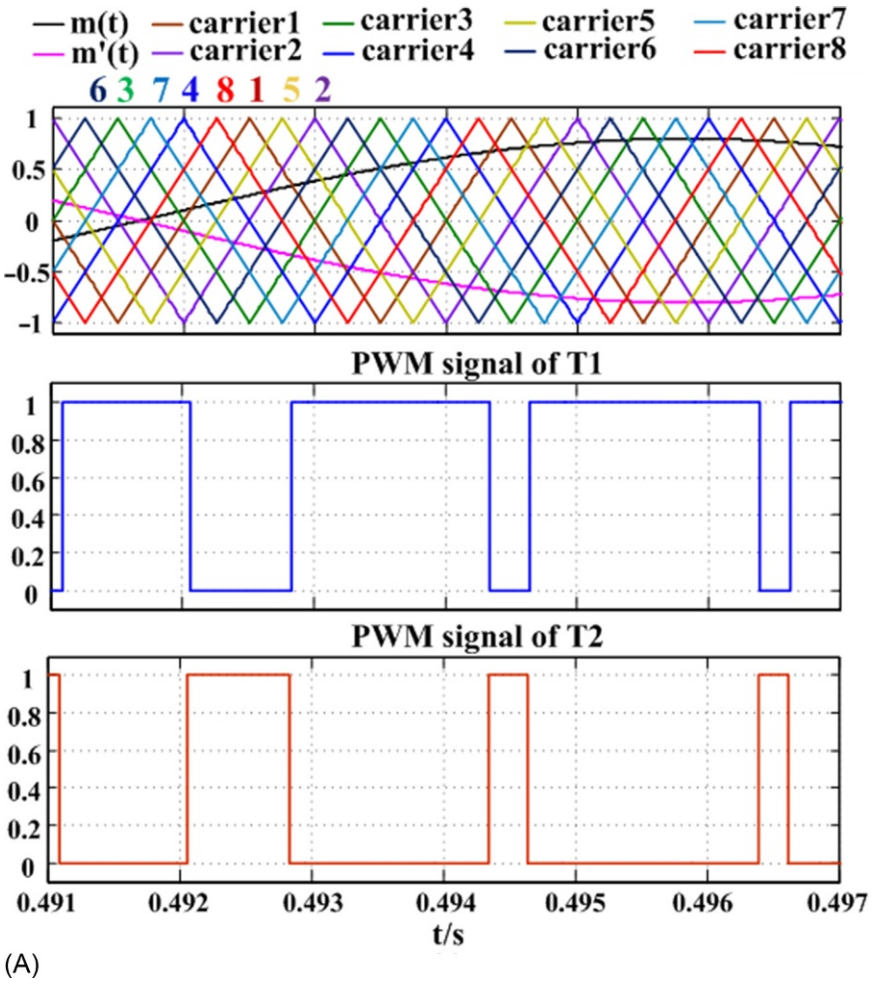


FIG. 13.30 Four cells in series connection with 360 degrees/*N* phase displacement in the carriers: (A) modulation waves and PWM signal for switches of the first SM and (B) simulation waveform of the output phase voltage.

the diode-clamped inverter. Fig. 13.33 shows how the space vector d-q plane looks like for a six-level inverter. Fig. 13.34 represents the equivalent dc link of a six-level inverter as a multiplexer that connects each of the three output phase voltages to one of the dc link voltage tap points [83]. Each integral point on the space vector plane represents a particular three-phase output voltage state of the inverter. For instance, the point (3, 2, and 0) on the space vector plane means that with respect to ground, "a" phase is at $3V_{dc}$, "b" phase is at $2V_{dc}$, and "c" phase is at $0V_{dc}$. The corresponding connections between the dc link



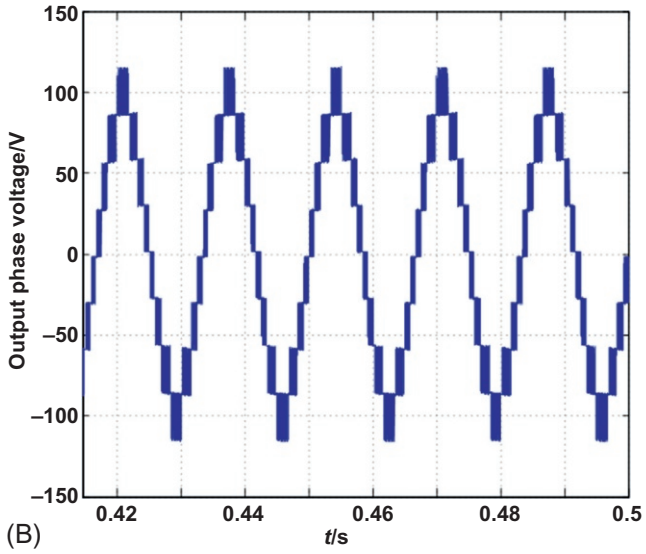


FIG. 13.31 Four cells in series connection with 180 degrees/*N* phase displacement in the carriers: (A) modulation waves and PWM signal for switches of the first SM and (B) simulation waveform of the output phase voltage.

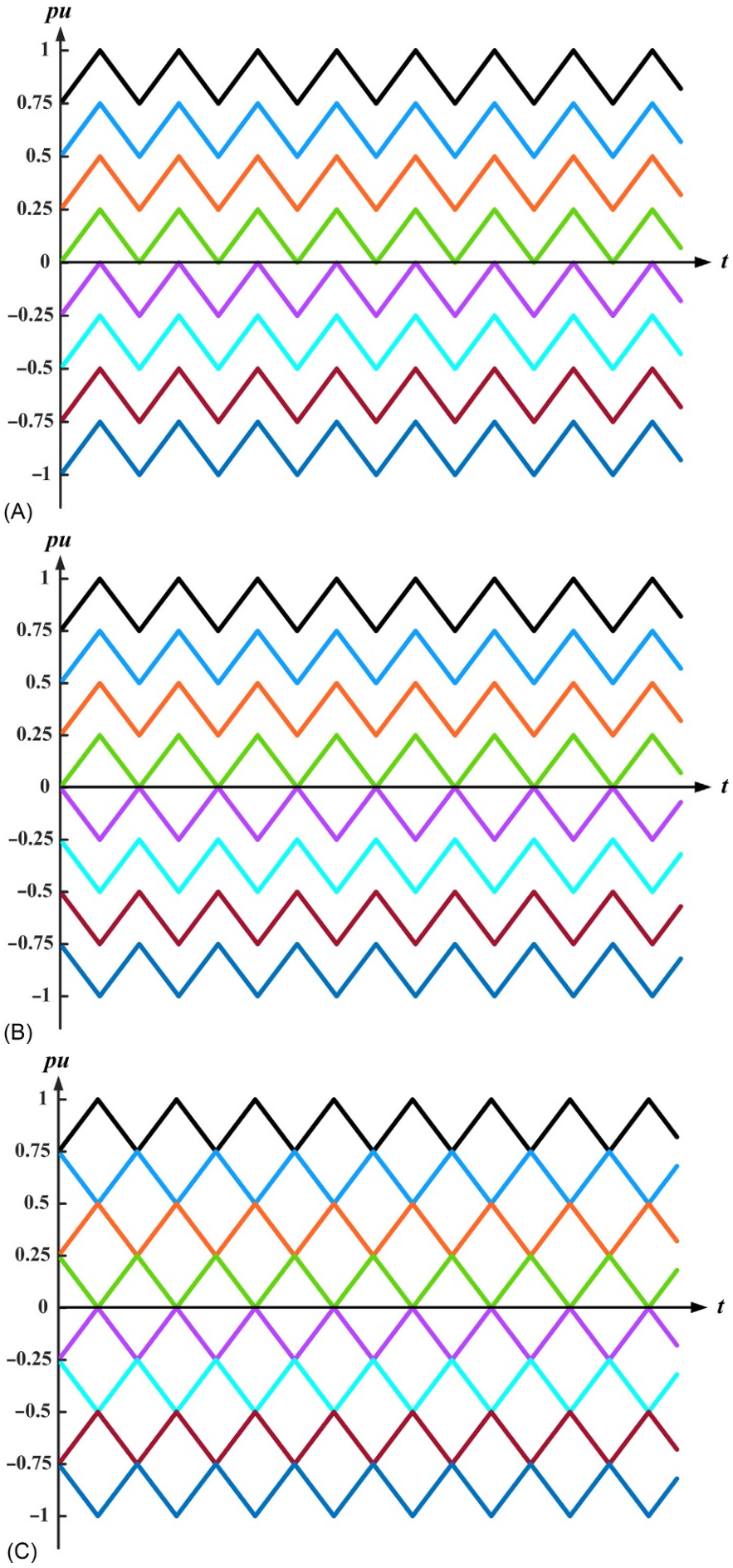


FIG. 13.32 Carrier waveforms for CLS-PWM: (A) PD, (B) POD, and (C) APOD.

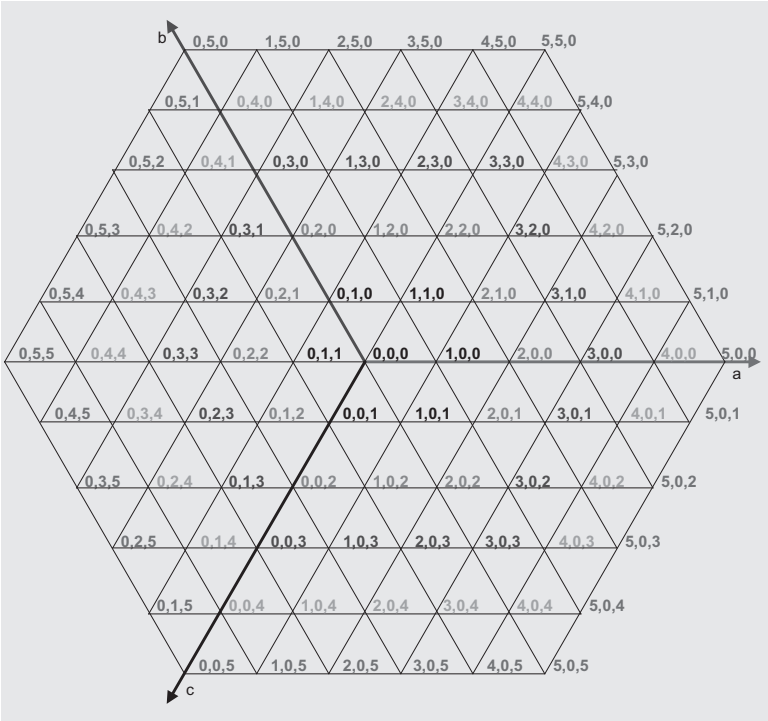


FIG. 13.33 Voltage space vectors for a six-level inverter.

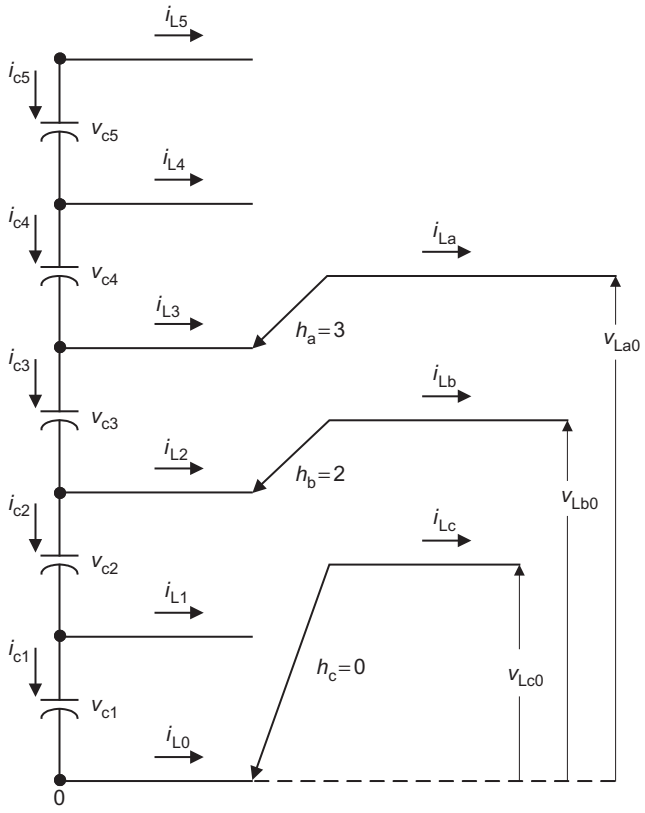


FIG. 13.34 Multiplexer model of diode-clamped six-level inverter.

and the output lines for the six-level inverter are also shown in Fig. 13.34 for the point (3, 2, 0). An algebraic way to represent the output voltages in terms of the switching states and dc link capacitors is described in the following [84]. For $n = m - 1$, where m is the number of levels in the inverter,

$$V_{abc0} = H_{abc} V_c \tag{13.19}$$

where

$$V_c = [V_{c1}\ V_{c2}\ V_{c3} \cdots V_{cn}]^T;$$
$$H_{abc} = \begin{bmatrix} h_{a1} & h_{a2} & h_{a3} & \dots & h_{an} \\ h_{b1} & h_{b2} & h_{b3} & \dots & h_{bn} \\ h_{c1} & h_{c2} & h_{c3} & \dots & h_{cn} \end{bmatrix};\quad V_{abc0} = \begin{bmatrix} V_{a0} \\ V_{b0} \\ V_{c0} \end{bmatrix}$$

and

$$h_{aj} = \sum_{j}^{n} \delta(h_a - j)$$

where h_a is the switch state and j is an integer from 0 to n and where $\delta(x) = 1$ if $x \geq 0, \delta(x) = 0$ if $x < 0$.

Besides the output voltage state, the point (3, 2, 0) on the space vector plane can also represent the switching state of the converter. Each integer indicates how many upper switches in each phase leg are on for a diode-clamped converter. As an example, for $h_a = 3, h_b = 2, h_c = 0$, the H_{abc} matrix for this particular switching state of a six-level inverter would be

$$H_{abc} = \begin{bmatrix} 0 & 0 & 1 & 1 & 1 \\ 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

Redundant switching states are those states for which a particular output voltage can be generated by more than one switch combination. Redundant states are possible at lower modulation indexes or at any point other than those on the outermost hexagon shown in Fig. 13.33. Switch state (3, 2, 0) has redundant states (4, 3, 1) and (5, 4, 2). Redundant switching states differ from each other by an identical integral value, that is, (3, 2, 0) differs from (4, 3, 1) by (1, 1, 1) and from (5, 4, 2) by (2, 2, 2).

For an output voltage state (x,y,z) in an m-level diode-clamped inverter, the number of redundant states available is given by $m-1-\max(x,y,z)$. As the modulation index decreases (or the voltage vector in the space vector plane gets closer to the origin), more redundant states are available. The number of possible zero states is equal to the number of levels, m. For a six-level diode-clamped inverter, the zero-voltage states are (0, 0, 0), (1, 1, 1), (2, 2, 2), (3, 3, 3), (4, 4, 4), and (5, 5, 5).

The number of possible switch combinations is equal to the cube of the level (m^3). For this six-level inverter, there are 216 possible switching states. The number of distinct or unique states for an m-level inverter can be given by

$$m^3-(m-1)^3=\left[6\sum_{n=1}^{m-1}n\right]+1. \tag{13.20}$$

Therefore, the number of redundant switching states for an m-level inverter is $(m-1)^3$. Table 13.7 summarizes the available redundancies and distinct states for a six-level diode-clamped inverter.

In two-level PWM, a reference voltage is tracked by selecting the two nearest voltage vectors and a zero vector and then by calculating the time required to be at each of these three vectors such that their sum equals the reference vector. In multilevel PWM, generally, the nearest three triangle vertices, V_1, V_2, and V_3, to a reference point V^* are selected to minimize the harmonic components of the output line-line voltage [85]. The respective time duration, T_1, T_2, and T_3, required for these vectors is then solved from the following equations:

$$\vec{V}_1T_1+\vec{V}_2T_2+\vec{V}_3T_3=V^*T_s \tag{13.21}$$

$$T_1+T_2+T_3=T_s \tag{13.22}$$

where T_s is the switching period. Eq. (13.21) actually represents two equations, one with the real part of the terms and one with the imaginary part of the terms:

$$V_{1d}T_1+V_{2d}T_2+V_{3d}T_3=V_d^*T_s \tag{13.23}$$

$$V_{1q}T_1+V_{2q}T_2+V_{3q}T_3=V_q^*T_s \tag{13.24}$$

Eqs. (13.22)–(13.25) can then be solved for T_1, T_2, and T_3 as follows:

$$\begin{bmatrix} T_1 \\ T_2 \\ T_3 \end{bmatrix} = \begin{bmatrix} V_{1d} & V_{2d} & V_{3d} \\ V_{1q} & V_{2q} & V_{3q} \\ 1 & 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} V_d^*T_s \\ V_q^*T_s \\ T_s \end{bmatrix} \tag{13.25}$$

Others have proposed space vector methods that did not use the nearest three vectors, but these methods generally add complexity to the control algorithm. Fig. 13.35 shows what a sinusoidal reference voltage (circle of points) and the inverter output voltages look like in the d-q plane.

TABLE 13.7 Line-line redundancies of six-level three-phase diode-clamped inverter

Redundancies	Distinct states	Redundant states	Unique state coordinates, (a,b,c), where $0 \le a,b,c \le 5$
5	1	5	(0,0,0)
4	6	24	(0,0,1),(0,1,0),(1,0,0),(1,0,1), (1,1,0),(0,0,1)
3	12	36	(p,0,2),(p,2,0),(0,p,2),(2,p,0), (0,2,p),(2,0,p), where $p \le 2$
2	18	36	(0,3,p),(3,0,p),(p,3,0),(p,0,3), (3,p,0),(0,p,3), where $p \le 3$
1	24	24	(0,4,p),(4,0,p),(p,4,0),(p,0,4), (4,p,0),(0,p,4), where $p \le 4$
0	30	0	(0,5,p),(5,0,p),(p,5,0),(p,0,5), (5,p,0),(0,p,5), where $p \ge 5$
Total	91	125	216 total states

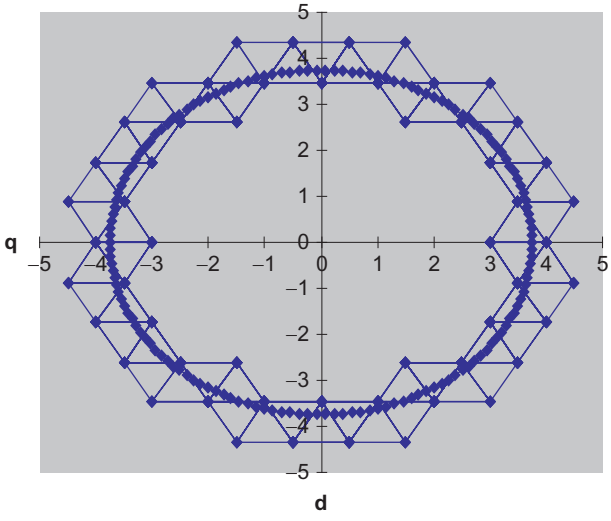


FIG. 13.35 Sinusoidal reference and inverter output voltage states in d-q plane.

Redundant switch levels can be used to help manage the charge on the dc link capacitors [86]. Generalizing from Fig. 13.34, the equations for the currents through the dc link capacitors can be given as

$$i_{cn} = -i_{Ln} \tag{13.26}$$

and

$$i_{c(n-j)} = -i_{L(n-j)} + i_{c(n-j+1)}, \quad \text{where } j = 1,2,3\ldots,n-1 \tag{13.27}$$

The dc link currents for $h_a = 3, h_b = 2, h_c = 0$ would be $i_{c5} = i_{c4} = 0, i_{c3} = -i_a, i_{c2} = -i_a - i_b, i_{c1} = -i_a - i_b$. To see how redundant states affect the dc link currents, consider the two redundant states for (3, 2, 0). In state (4, 3, 1), the dc link currents would be $i_{c5} = 0, i_{c4} = -i_a, i_{c3} = -i_a - i_b, i_{c2} = -i_a - i_b$, $i_{c1} = -i_a - i_b - i_c = 0$; and for the state (5, 4, 2), the dc link currents would be $i_{c5} = -i_a, i_{c4} = -i_a - i_b, i_{c3} = -i_a - i_b$, $i_{c2} = i_{c1} = -i_a - i_b - i_c = 0$.

From this example, one can see that the choice of redundant switching states can be used to determine which capacitors will be charged/discharged or unaffected during the switching period. Although this control is helpful in balancing the individual dc voltages across the capacitors that make up the dc link, this method is quite complicated in selecting which of the redundant states to use. Constant use of redundant switching states also results in a higher switching frequency and lower efficiency of the inverter because of the extra switchings. Optimized space vector switching sequences for multilevel inverters have been proposed in [87].

13.3.3 Selective Harmonic Elimination

13.3.3.1 Fundamental Switching Frequency

The selective harmonic elimination method is also called fundamental switching frequency method based on the harmonic elimination theory proposed by Patel and Hoft [88,89]. A typical 11-level multilevel converter output with fundamental frequency switching scheme is shown in Fig. 13.2. The Fourier series expansion of the output voltage waveform as shown in Fig. 13.2 is expressed in Eqs. (13.1) and (13.2).

The conducting angles, $\theta_1, \theta_2, \ldots, \theta_s$, can be chosen such that the voltage total harmonic distortion is a minimum. Normally, these angles are chosen so as to cancel the predominant lower frequency harmonics [19].

For the 11-level case in Fig. 13.2, the fifth, seventh, eleventh, and thirteenth harmonics can be eliminated with the appropriate choice of the conducting angles. One degree of freedom is used so that the magnitude of the fundamental waveform corresponds to the reference waveform's amplitude or modulation index, m_a, which is defined as V_L^*/V_{Lmax}. V_L^* is the amplitude command of the inverter for a sine wave output phase voltage, and V_{Lmax} is the maximum attainable amplitude of the converter, that is, $V_{Lmax} = s \cdot V_{dc}$. The equations from Eq. (13.2) will now be as follows:

$$\begin{aligned}
&\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) + \cos(5\theta_4) + \cos(5\theta_5) = 0\\
&\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) + \cos(7\theta_4) + \cos(7\theta_5) = 0\\
&\cos(11\theta_1) + \cos(11\theta_2) + \cos(11\theta_3) + \cos(11\theta_4) + \cos(11\theta_5) = 0\\
&\cos(13\theta_1) + \cos(13\theta_2) + \cos(13\theta_3) + \cos(13\theta_4) + \cos(13\theta_5) = 0\\
&\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4) + \cos(\theta_5) = 5m_a
\end{aligned} \tag{13.28}$$

The above equations are nonlinear transcendental equations that can be solved by an iterative method such as the Newton-Raphson method. For example, using a modulation index of 0.8 obtains the following: $\theta_1 = 6.57$ degrees, $\theta_2 = 18.94$ degrees, $\theta_3 = 27.18$ degrees, $\theta_4 = 45.14$ degrees, $\theta_5 = 62.24$ degrees. Thus, if the inverter output is symmetrically switched during the positive half cycle of the fundamental voltage to $+V_{dc}$ at 6.57 degrees, $+2V_{dc}$ at 18.94 degrees, $+3V_{dc}$ at 27.18 degrees, $+4V_{dc}$ at 45.14 degrees and $+5V_{dc}$ at 62.24 degrees and similarly in the negative half cycle to $-V_{dc}$ at 186.57 degrees, $-2V_{dc}$ at 198.94 degrees, $-3V_{dc}$ at 207.18 degrees, $-4V_{dc}$ at 225.14 degrees, $-5V_{dc}$ at 242.24 degrees, the output voltage of the 11-level inverter will not contain the 5th, 7th, 11th, and 13th harmonic components [18]. Other methods to solve these equations include using genetic algorithms [90] and resultant theory [91,92].

Practically, the precalculated switching angles are stored as the data in memory (lookup table). Therefore, a microcontroller could be used to generate the PWM gate-drive signals. More recent methods have been developed that can generate the switching angles in real time using genetic algorithms.

13.3.3.2 Selective Harmonic Elimination PWM

In order to achieve a wide range of modulation indexes with minimized THD for the synthesized waveforms, a generalized selective harmonic modulation method [93,94] was proposed, which is called virtual stage PWM [90]. An output waveform is shown in Fig. 13.36. The virtual stage PWM is a combination of the unipolar programmed PWM and the fundamental frequency switching scheme. The output waveform of unipolar

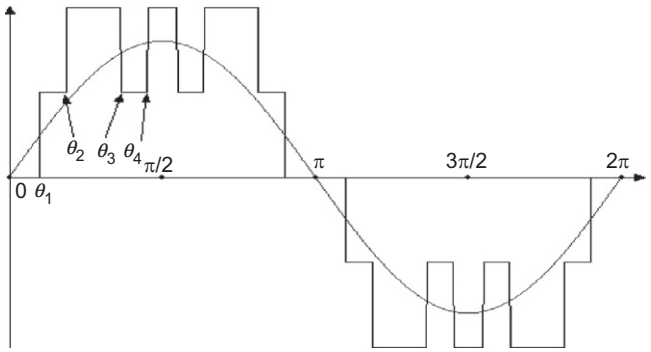


FIG. 13.36 Output waveform of virtual stage PWM control.

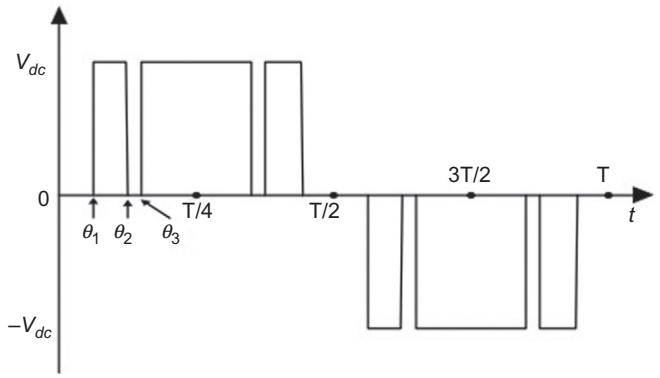


FIG. 13.37 Unipolar switching output waveform.

programmed PWM is shown in Fig. 13.37. When unipolar programmed PWM is employed on a multilevel converter, typically one dc voltage is involved, where the switches connected to the dc voltage are switched "on" and "off" several times per fundamental cycle. The switching pattern decides what the output voltage waveform looks like.

For fundamental switching frequency method, the number of switching angles is equal to the number of dc sources. However, for the virtual stage PWM method, the number of switching angles is not equal to the number of dc voltages. For example, in Fig. 13.36, only two dc voltages are used, whereas there are four switching angles.

Bipolar programmed PWM and unipolar programmed PWM could be used for modulation indexes too low for the applicability of the multilevel fundamental frequency switching method. Virtual stage PWM can also be used for low modulation indexes. Virtual stage PWM will produce output waveforms with a lower THD most of the time [90]. Therefore, virtual stage PWM provides another alternative to bipolar programmed PWM and unipolar programmed PWM for low modulation index control.

The major difficulty for selective harmonic elimination methods, including the fundamental switching frequency method and the virtual stage PWM method, is to solve the transcendental Eq. (13.28) for switching angles. Newton's method can be used to solve Eq. (13.28), but it needs good initial guesses, and solutions are not guaranteed. Therefore, Newton's method is not feasible to solving equations for large number of switching angles if good initial guesses are not available [95].

The resultant method has been proposed in [91,92,96] to solve the transcendental equations for switching angles. The transcendental equations characterizing the harmonic content can be converted into polynomial equations. Elimination resultant theory has been employed to determine the switching angles to eliminate specific harmonics, such as the 5th, 7th, 11th, and 13th. However, as the number of dc voltages or the number of switching angles increases, the degrees of the polynomials in these equations become bulky.

To overcome this problem, the fundamental frequency switching angle computation is solved by Newton's method. The initial guess can be provided by the results of lower order transcendental equations by the resultant method [95].

13.3.4 Other Modulation Strategies for Modular Multilevel Inverter

Space vector control (SVC) fully utilizes the large number of voltage vectors generated by multilevel converters, which approximates the voltage reference to the closest available state vector. This principle enables SVC with fundamental switching frequency and thus lower switching losses. Meanwhile, different from SHE PWM, the switching sequence can be produced online, resulting in a relatively easy implementation of SVC in closed-loop and high-bandwidth applications. The time domain version of SVC is the nearest level control (NLC), which approximates the closet voltage level instead of vector that can be generated by the converter, as illustrated in Fig. 13.38, where the inserted SM number equals to an integer closest to voltage reference v^* over SM capacitor voltage v_c. The basic idea of NLC is to first calculate how many SMs should be inserted and which SMs will be determined by the capacitors' voltage sorting and the direction of the arm current.

Based on an approximation instead of a modulation, both SVC and NLC are suitable for inverters with a high number of levels. On the other hand, due to the low and variable switching frequency, these two methods suffer high total harmonic distortion (THD) when the voltage levels and/or modulation indexes are low.

In summary, each multilevel modulation scheme has its own uniqueness, making it more suitable for specific converter topologies and applications. In general, low switching frequency modulation methods are preferred for high-power applications

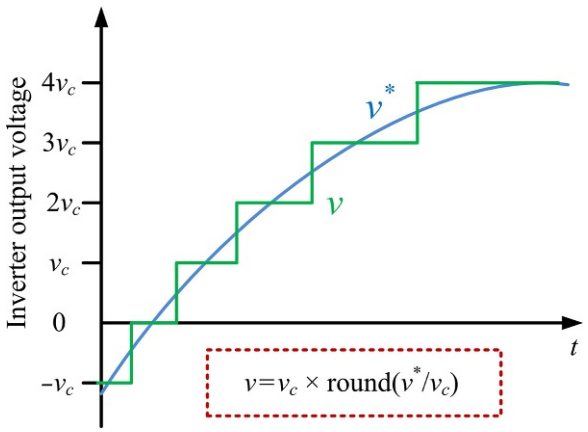


FIG. 13.38 Waveform synthesis using NLC.

due to lower switching loss, while high switching frequency algorithms enable better output power quality and higher bandwidth and thus are more suitable for high-dynamic-range applications.

13.4 Conclusion

This chapter has demonstrated the state of the art of multilevel power converter technology. Fundamental multilevel converter structures and modulation paradigms including the pros and cons of each technique have been discussed. Most of the chapter focuses on modern and more practical industrial applications of multilevel converters. The possible future enlargements of multilevel converter technology such as fault diagnosis system and renewable energy sources have been noted in earlier literature [97]. The development of wide bandgap power devices, especially medium-voltage SiC MOSFETs, IGBTs, diodes, and thyristors, in the next several years is expected to open more applications for multilevel converters. It should be noted that this chapter could not cover all multilevel, power converter-related applications; however, the basic principles of different multilevel converters have been discussed methodically. The main objective of this chapter is to provide a general notion to readers who are interested in multilevel power converters and their applications.

References

[1] J. Rodriguez, J.S. Lai, F.Z. Peng, Multilevel inverters: survey of topologies, controls, and applications, IEEE Trans. Ind. Appl. 49 (4) (2002) 724–738.

[2] J.S. Lai, F.Z. Peng, Multilevel converters—a new breed of power converters, IEEE Trans. Ind. Appl. 32 (1996) 509–517.

[3] L.M. Tolbert, F.Z. Peng, T. Habetler, Multilevel converters for large electric drives, IEEE Trans. Ind. Appl. 35 (1999) 36–44.

[4] R. H. Baker, L. H. Bannister, Electric power converter, U.S. Patent 3,867,643, February 1975.

[5] A. Nabae, I. Takahashi, H. Akagi, A new neutral-point clamped PWM inverter, IEEE Trans. Ind. Appl. IA-17 (1981) 518–523.

[6] R.H. Baker, Bridge converter circuit, U.S. Patent 4,270,163, May 1981.

[7] P.W. Hammond, Medium voltage PWM drive and method, U.S. Patent 5,625,545, April 1977.

[8] F.Z. Peng, J.S. Lai, Multilevel cascade voltage-source inverter with separate DC source, U.S. Patent 5,642,275, June 24, 1997.

[9] P.W. Hammond, Four-quadrant AC-AC drive and method, U.S. Patent 6,166,513, December 2000.

[10] M.F. Aiello, P.W. Hammond, M. Rastogi, Modular multi-level adjustable supply with series connected active inputs, U.S. Patent 6,236,580, May 2001.

[11] M.F. Aiello, P.W. Hammond, M. Rastogi, Modular multilevel adjustable supply with parallel connected active inputs, U.S. Patent 6,301,130, October 2001.

[12] J.P. Lavieville, P. Carrere, T. Meynard, Electronic circuit for converting electrical energy and a power supply installation making use thereof, U.S. Patent 5,668,711, September 1997.

[13] T. Meynard, J.-P. Lavieville, P. Carrere, J. Gonzalez, O. Bethoux, Electronic circuit for converting electrical energy, U.S. Patent 5,706,188, January 1998.

[14] E. Cengelci, S.U. Sulistijo, B.O. Woom, P. Enjeti, R. Teodorescu, F. Blaabjerg, A new medium voltage PWM inverter topology for adjustable speed drives, in: Conf. Rec., IEEE Industry Applications Society Annual Meeting, St. Louis, MO, October, 1998, pp. 1416–1423.

[15] M.F. Escalante, J.C. Vannier, A. Arzande, Flying capacitor multilevel inverters and DTC motor drive applications, IEEE Trans. Ind. Electron. 49 (4) (2002) 809–815.

[16] L.M. Tolbert, F.Z. Peng, Multilevel converters as a utility interface for renewable energy systems, in: Proceedings of 2000 IEEE Power Engineering Society Summer Meeting, vol. 1, 2000, pp. 1271–1274.

[17] L.M. Tolbert, F.Z. Peng, T.G. Habetler, A multilevel converter-based universal power conditioner, IEEE Trans. Ind. Appl. 36 (2) (2000) 596–603.

[18] L.M. Tolbert, F.Z. Peng, T.G. Habetler, Multilevel inverters for electric vehicle applications, in: IEEE Workshop on Power Electronics in Trans., WPET, Dearborn, MI, October 22–23, 1998, pp. 1424–1431.

[19] R.W. Menzies, Y. Zhuang, Advanced static compensation using a multilevel GTO thyristor inverter, IEEE Trans. Power Del. 10 (2) (1995) 732–738.

[20] F.Z. Peng, J.S. Lai, J.W. McKeever, J. VanCoevering, A multilevel voltage-source inverter with separate DC sources for static var generation, IEEE Trans. Ind. Appl. 32 (5) (1996) 1130–1138.

[21] F.Z. Peng, J.S. Lai, Dynamic performance and control of a static var generator using cascade multilevel inverters, IEEE Trans. Ind. Appl. 33 (3) (1997) 748–755.

[22] F.Z. Peng, J.W. McKeever, D.J. Adams, A power line conditioner using cascade multilevel inverters for distribution systems, in: Conf. Record—IEEE Industry Applications Society 32nd Annual Meeting, vol. 2, 1997, pp. 1316–1321.

[23] F.Z. Peng, J.W. McKeever, D.J. Adams, Cascade multilevel inverters for utility applications, in: Proceedings of the 23rd International Conference on Industrial Electronics, Control, and Instrumentation, vol. 2, 1997, pp. 437–442.

[24] G. Joos, X. Huang, B.T. Ooi, Direct-coupled multilevel cascaded series VAR compensators, in: Conf. Record—IEEE Industry Applications Society 32nd Annual Meeting, vol. 2, 1997, pp. 1608–1615.

[25] L.M. Tolbert, F.Z. Peng, T. Cunnyngham, J.N. Chiasson, Charge balance control schemes for multilevel converter in hybrid electric vehicles, IEEE Trans. Ind. Electron. 49 (5) (2002) 1058–1065.

[26] M.D. Manjrekar, T.A. Lipo, A hybrid multilevel inverter topology for drive applications, in: IEEE Applied Power Electronics Conference, vol. 2, 1998, pp. 523–529.

[27] M.D. Manjrekar, T.A. Lipo, A generalized structure of multilevel power converter, in: IEEE Conf. Power Electronics, Drives, and Energy Systems, PEDES, Australia, 1998, pp. 62–67.

[28] C. Hochgraf, R. Lasseter, D. Divan, T.A. Lipo, Comparison of multilevel inverters for static var compensation, in: Conf. Record—IEEE Industry Applications Society 29th Annual Meeting, vol. 2, 1994, pp. 921–928.

[29] J.S. Lai, F.Z. Peng, Multilevel converters—a new breed of power converters, IEEE Trans. Ind. Appl. 32 (3) (1996) 509–517.

[30] K. Corzine, Y. Familiant, A new cascaded multilevel H-bridge drive, IEEE Trans. Power Electron. 17 (1) (2002) 125–131.

[31] T.A. Meynard, H. Foch, Multi-level conversion: high voltage choppers and voltage-source inverters, in: IEEE Power Electronics Specialists Conference, vol. 1, 1992, pp. 397–403.
[32] G. Sinha, T.A. Lipo, A new modulation strategy for improved DC bus utilization in hard and soft switched multilevel inverters, in: IECON, vol. 2, 1997, pp. 670–675.
[33] R. Marquardt, Stromrichterschaltungen mit verteilten Energiespeichern, German Patent DE 10,103,031/24.01. 2001, January 24, 2001.
[34] X. Shi, L. Tolbert, F. Wang, Modular multilevel converters with integrated arm inductors for high quality current waveforms, in: Proceedings of the IEEE Energy Conversion Congress and Exposition Asia, 2013, pp. 636–642.
[35] J. Kolb, F. Kammerer, M. Braum, Dimensioning and design of a modular multilevel converter for drive applications, in: Proceedings of the IEEE 15th International Power Electronics and Motion Control Conference, 2012, pp. 1–8.
[36] N. Thitichaiworakorn, M. Hagiwara, H. Akagi, Experimental verification of a modular multilevel cascade inverter based on double-star bridge-cells (MMCI-DSBC), IEEE Trans. Ind. Appl. 50 (1) (2014) 509–519.
[37] H. Akagi, New trends in medium-voltage power converters and motor drives, in: Proceedings of the IEEE International Symposium on Industrial Electronics (ISIE), 2011, pp. 5–14.
[38] R. Marquardt, Modular multilevel converter topologies with dc-short circuit current limitation, in: Proceedings of the IEEE 8th International Conference on Power Electronics and ECCE Asia (ICPE & ECCE), 2011, pp. 1425–1431.
[39] List of HVDC Projects, Wikipedia, https://en.wikipedia.org/wiki/List_of_HVDC_projects.
[40] D. Siemaszko, A. Antonopoulos, K. Ilves, M. Vasiladiotis, L. Ängquist, H.P. Nee, Evaluation of control and modulation methods for modular multilevel converters, in: IEEE International Power Electronics Conference, 2010, pp. 746–753.
[41] M. Hagiwara, H. Akagi, Control and experiment of pulsewidth-modulated modular multilevel converters, IEEE Trans. Power Electron. 24 (7) (2009) 1737–1746.
[42] S. Rohner, S. Bernet, M. Hiller, R. Sommer, Modulation, losses, and semiconductor requirements of modular multilevel converters, IEEE Trans. Ind. Electron. 57 (8) (2010) 2633–2642.
[43] N. Chaudhuri, B. Chaudhuri, R. Majumder, A. Yazdani, Multi-Terminal Direct-Current Grids: Modeling, Analysis, and Control, Wiley-IEEE Press, 2014.
[44] M. Dommaschk, Drive for a phase module branch of a multilevel converter, Int. Patent WO2008/086760A1, July 2008.
[45] K. Ilves, A. Antonopoulos, L. Harnefors, S. Norrga, H.-P. Nee, Steady-state analysis of interaction between harmonic components of arm and line quantities of modular multilevel converters, IEEE Trans. Power Electron. 27 (1) (2012) 57–68.
[46] S. Rohner, S. Bernet, M. Hiller, R. Sommer, Analysis and simulation of a 6 kV, 6 MVA modular multilevel converter, in: Proceedings of the IEEE Annual Conference Industrial Electronics, 2009, pp. 225–230.
[47] Q. Tu, Z. Xu, L. Xu, Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters, IEEE Trans. Power Del. 26 (3) (2013) 2009–2017.
[48] K. Ilves, A. Antonopoulos, L. Harnefors, S. Norrga, H.-P. Nee, Circulating current control in modular multilevel converters with fundamental switching frequency, in: Proceedings of the 7th Power Electronics and Motion Control Conference, 2012.
[49] A. Antonopoulos, L. Angquist, H.-P. Nee, On dynamics and voltage control of the modular multilevel converter, in: Proceedings of the European Conference Power Electronics and Applications (EPE), 2009, pp. 1–10.
[50] L. Angquist, A. Antonopoulos, D. Siemaszko, K. Ilves, M. Vasiladiotis, H.-P. Nee, Open-loop control of modular multilevel converters using estimation of stored energy, IEEE Trans. Ind. Appl. 47 (6) (2011) 2516–2524.
[51] X. Shi, Z. Wang, B. Liu, Y. Liu, L. Tolbert, F. Wang, Characteristic investigation and control of modular multilevel converter based HVDC system under single-line-to-ground fault conditions, IEEE Trans. Power Electron. 30 (1) (2015) 408–421.
[52] Z. Li, P. Wang, Z. Chu, H. Zhu, Y. Luo, Y. Li, An inner current suppressing method for modular multilevel converters, IEEE Trans. Power Electron. 28 (11) (2013) 4873–4879.
[53] J.-W. Moon, C.-S. Kim, J.-W. Park, D.-W. Kang, J.-M. Kim, Circulating current control in mmc under the unbalanced voltage, IEEE Trans. Power Del. 28 (3) (2013) 1952–1959.
[54] B. Jacobson, P. Karlsson, G. Asplund, et al., VSC-HVDC transmission with cascaded two-level converters, in: Cigre 2010 Session. Paris, France, 2010.
[55] J. Dorn, H. Gambach, J. Strauss, et al., Trans bay cable—a breakthrough of VSC multilevel converters in HVDC transmission, in: Cigre San Francisco Colloquium, 2012.
[56] R.L. Sellick, M. Åkerberg, Comparison of HVDC light (VSC) and HVDC classic (LCC) site aspects, for a 500 MW 400kV HVDC transmission scheme, in: Proceedings of the IET AC and DC Power Transmission, 2012, pp. 1–6.
[57] F.Z. Peng, A generalized multilevel converter topology with self voltage balancing, IEEE Trans. Ind. Appl. 37 (2) (2001) 611–618.
[58] W.A. Hill, C.D. Harbourt, Performance of medium voltage multilevel converters, in: Conf. Rec. IEEE Industry Applications Society Annual Meeting, Phoenix, AZ, 1999, pp. 1186–1192.
[59] B.M. Song, J.S. Lai, A multilevel soft-switching inverter with inductor coupling, IEEE Trans. Ind. Appl. 37 (2001) 628–636.
[60] H. Fujita, H. Akagi, The unified power quality conditioner: the integration of series- and shunt-active filters, IEEE Trans. Power Electron. 13 (2) (1998) 315–322.
[61] S.-J. Jeon, G.-H. Cho, A series-parallel compensated uninterruptible power supply with sinusoidal input current and sinusoidal output voltage, in: IEEE Power Electronics Specialists Conference, vol. 1, 1997, pp. 297–303.
[62] F. Kamran, T.G. Habetler, A novel on-line UPS with universal filtering capabilities, in: IEEE Power Electronics Specialists Conference, vol. 1, 1995, pp. 500–506.
[63] F. Kamran, T.G. Habetler, Combined deadbeat control of a series-parallel converter combination used as a universal power filter, IEEE Trans. Power Electron. 13 (1) (1998) 160–168.
[64] L. Moran, G. Joos, Principles of active power filters, in: IEEE Industry Applications Society Annual Meeting, 1998. Tutorial Course Notes.
[65] S. Muthu, J.M.S. Kim, Steady-state operating characteristics of unified active power filters, in: IEEE Applied Power Electronics Conference, vol. 1, 1997, pp. 199–205.
[66] A. van Zyl, J.H.R. Enslin, R. Spee, A new unified approach to power quality management, IEEE Trans. Power Electron. 11 (5) (1996) 691–697.
[67] Y. Chen, B. Mwinyiwiwa, Z. Wolanski, B.-T. Ooi, Unified power flow controller (UPFC) based on chopper stabilized multilevel converter, in: IEEE Power Electronics Specialists Conference, 1997, pp. 331–337.

[68] J.H.R. Enslin, J. Zhao, R. Spee, Operation of the unified power flow controller as harmonic isolator, IEEE Trans. Power Electron. 11 (6) (1996) 776–784.
[69] H. Fujita, Y. Watanabe, H. Akagi, Control and analysis of a unified power flow controller, in: IEEE Power Electronics Specialists Conference, vol. 1, 1998, pp. 805–811.
[70] L. Gyugyi, Dynamic compensation of AC transmission lines by solid-state synchronous voltage sources, IEEE Trans. Power Del. 9 (2) (1994) 904–911.
[71] L. Gyugi, C.D. Schauder, S.L. Williams, T.R. Reitman, D. R. Torgerson, A. Edris, The unified power flow controller: a new approach to power transmission control, IEEE Trans. Power Del. 10 (2) (1995) 1085–1093.
[72] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, G. Sciutto, A new multilevel PWM method: a theoretical analysis, IEEE Trans. Power Electron. 7 (3) (1992) 497–505.
[73] R.W. Menzies, P. Steimer, J.K. Steinke, Five-level GTO inverters for large induction motor drives, IEEE Trans. Ind. Appl. 30 (4) (1994) 938–944.
[74] S. Halasz, G. Csonka, A.A.M. Hassan, Sinusoidal PWM techniques with additional zero-sequence harmonics, in: Proceedings of the 20th International Conf. Industrial Electronics, Control, and Instrumentation, vol. 1, 1994, pp. 85–90.
[75] D.G. Holmes, The significance of zero space vector placement for carrier based PWM schemes, in: Conf. Record—IEEE Industry Applications Society 30th Annual Meeting, vol. 3, 1995, pp. 2451–2458.
[76] S. Bhattacharya, D.G. Holmes, D.M. Divan, Optimizing three phase current regulators for low inductance loads, in: Conf. Record—IEEE Industry Applications Society 30th Annual Meeting, vol. 3, 1995, pp. 2357–2364.
[77] L.M. Tolbert, T.G. Habetler, Novel multilevel inverter carrier-based PWM method, IEEE Trans. Ind. Appl. 25 (5) (1999) 1098–1107.
[78] F.Z. Peng, J.S. Lai, A static var generator using a staircase waveform multilevel voltage-source converter, in: PCIM/Power Quality Conference Dallas, TX, 1994, pp. 58–66.
[79] L.M. Tolbert, F.Z. Peng, T.G. Habetler, Multilevel PWM methods at low modulation indices, IEEE Trans. Power Electron. 15 (4) (2000) 719–725.
[80] C. Zang, Z. Pei, J. He, T. Guo, J. Zhu, W. Sun, Research on the application of CPS-SPWM technology in cascaded multilevel inverter, in: IEEE International Conference on Electrical Machines and Systems (ICEMS), 2009, pp. 1–4.
[81] B.P. McGrath, D.G. Holmes, Multicarrier PWM strategies for multilevel inverters, IEEE Trans. Ind. Electron. 49 (4) (2002) 858–867.
[82] N.S. Choi, J.G. Cho, G.H. Cho, A general circuit topology of multilevel inverter, in: IEEE Power Electronics Specialists Conference, 1991, pp. 96–103.
[83] G. Sinha, T.A. Lipo, A four-level inverter drive with passive front end, in: IEEE Power Electronics Specialists Conference, 1997, pp. 590–596.
[84] G. Sinha, T.A. Lipo, A four-level rectifier-inverter system for drive applications, in: Conf. Record—IEEE Industry Applications Society 31st Annual Meeting, vol. 2, 1996, pp. 980–987.
[85] H.L. Liu, N.S. Choi, G.H. Cho, DSP based space vector PWM for three-level inverter with DC-link voltage balancing", in: Proc. IECON '91 17th International Conf. Industrial Electronics, Control, and Instrumentation, vol. 1, 1991, pp. 197–203.
[86] G. Sinha, T.A. Lipo, A new modulation strategy for improved DC bus utilization in hard and soft switched multilevel inverters, in: IECON, vol. 2, 1997, pp. 670–675.
[87] B.P. McGrath, D.G. Holmes, T. Lipo, Optimized space vector switching sequences for multilevel inverters, IEEE Trans. Power Electron. 18 (6) (2003) 1293–1301.
[88] H.S. Patel, R.G. Hoft, Generalized harmonic elimination and voltage control in thyristor converters: part I—harmonic elimination, IEEE Trans. Ind. Appl. 9 (1973) 310–317.
[89] H.S. Patel, R.G. Hoft, Generalized harmonic elimination and voltage control in thyristor converters: part II—voltage control technique, IEEE Trans. Ind. Appl. 10 (1974) 666–673.
[90] K.J. McKenzie, Eliminating Harmonics in a Cascaded H-bridges Multilevel Converter using Resultant Theory, Symmetric Polynomials, and Power Sums, Master Thesis, The University of Tennessee, Knoxville, Tennessee, USA, 2004.
[91] J.N. Chiasson, L.M. Tolbert, K.J. McKenzie, Z. Du, A complete solution to the harmonic elimination problem, IEEE Trans. Power Electron. 19 (2) (2004) 491–499.
[92] J.N. Chiasson, L.M. Tolbert, K.J. McKenzie, Z. Du, A new approach to solving the harmonic elimination equations for a multilevel converter, in: IEEE Industry Applications Society Annual Meeting. IAS, Salt Lake City, UT, October 12–16, 2003, pp. 640–645.
[93] L. Li, D. Czarkowski, Y. Liu, P. Pillay, Multilevel selective harmonic elimination PWM technique in series-connected voltage converters, IEEE Trans. Ind. Appl. 36 (1) (2000) 160–170.
[94] S. Sirisukprasert, J.S. Lai, T.H. Liu, Optimum harmonic reduction with a wide range of modulation indexes for multilevel converters, IEEE Trans. Ind. Electron. 49 (4) (2002) 875–881.
[95] Z. Du, Active Harmonic Elimination in Multilevel Converters, Ph.D. Dissertation. The University of Tennessee, Knoxville, Tennessee, USA, pp. 33–36, 2005.
[96] J.N. Chiasson, L.M. Tolbert, K.J. McKenzie, Z. Du, Control of a multilevel converter using resultant theory, IEEE Trans. Control System Theory 11 (3) (2003) 345–354.
[97] S. Khomfoi, L.M. Tolbert, Multilevel Power Converters, in: Power Electronics Handbook, third ed., Elsevier, 2011, ISBN 978-0-12-382036-5, pp. 455–486, Chapter 17.

14

AC-AC Converters

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14.1 Introduction

A power electronic ac-ac converter, in generic form, accepts electric power from one system and converts it for delivery to another ac system with waveforms of different amplitude, frequency, and phase. Conventionally, the input system is of single-phase or three-phase type depending on the power ratings of the load, and the output system is of single-phase or three-phase type. However, recent research trend shows considerable orientation toward multiphase systems as they exhibit decrement in time and space harmonics, reduction in per phase current, increment in fault tolerance and reliability, etc. The ac-ac converters employed to vary the rms voltage across the load at constant frequency are known as *ac voltage controllers or ac regulators*. The voltage control is accomplished either by (1) *phase control* under natural commutation using pairs of silicon-controlled rectifiers (SCRs) or triacs or (2) by *on/off control* under forced commutation/self-commutation using fully controlled self-commutated switches, such as gate turn-off thyristors (GTOs), power transisto/rs, integrated-gate bipolar transistor (IGBTs), MOS-controlled thyristors (MCTs), and integrated-gate-commutated thyristor (IGCTs). Employment of switches depends on the power that is to be delivered (and thus on the switching frequency range of the device). The ac-ac power converters in which ac power at one frequency is directly converted to ac power at another frequency without any intermediate dc conversion link (as in the case of conventionally employed rectifier-inverter or back-to-back configurations) are known as *cycloconverters*, the majority of which uses naturally commutated SCRs for their operation when the maximum output frequency is limited to a fraction of the input frequency. With rapid advancements of fast-acting fully controlled switches, forced commutated cycloconverters, or *matrix converters* with bidirectional on/off control switches

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provide independent control of the magnitude and the frequency of the generated output voltage, as well as sinusoidal modulation of output voltage and current.

Although typical applications of ac voltage controllers include lighting and heating control, online transformer tap changing, soft starting, and speed control of pump and fan drives, the cycloconverters are mainly used for high-power, low-speed, large ac motor drives for application in cement kilns, rolling mills, and ship propellers. The power circuits, control methods, and the operation of the ac voltage controllers, cycloconverters, and matrix converters are introduced in this chapter. A brief review is also made regarding their applications.

14.2 Single-Phase AC-AC Voltage Controller

The basic power circuit of a single-phase ac-ac voltage controller, as shown in Fig. 14.1A, comprises a pair of SCRs connected back-to-back (also known as inverse-parallel or antiparallel) between the ac supply and the load. This connection provides a *bidirectional full-wave symmetrical* control, and the SCR pair can be replaced by a triac (Fig. 14.1B) for low-power applications. Alternate arrangements are shown in Fig. 14.1C with two diodes and two SCRs to provide a common cathode connection for simplifying the gating circuit without requiring isolation and in Fig. 14.1D with one SCR and four diodes to reduce the device cost but with increased device conduction loss. An SCR and diode combination known as *thyrode controller*, as shown in Fig. 14.1E, provides a *unidirectional half-wave asymmetrical voltage* control with device economy but introduces dc component and more harmonics, and thus, it is not so practical to use except for very low-power-heating load.

With phase control, the switches conduct the load current for a chosen period of each input cycle of voltage, and with on/off control, either the switches connect the load for a few cycles of input voltage and disconnect it for the next few cycles (*integral cycle control*) or the switches are turned on and off several times within

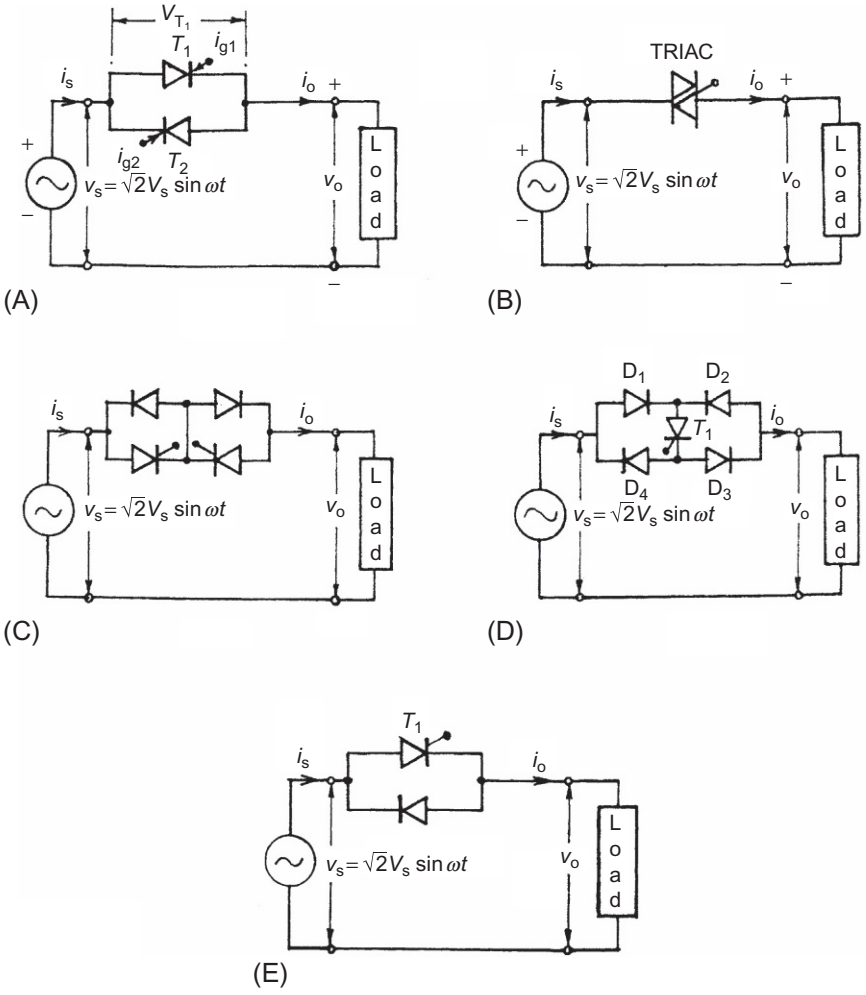


FIG. 14.1 Single-phase ac voltage controllers: (A) full wave, two SCRs in inverse-parallel; (B) full wave with triac; (C) full wave with two SCRs and two diodes; (D) full wave with four diodes and one SCR; and (E) half wave with one SCR and one diode in antiparallel.

alternate half cycles of input voltage (*ac chopper or pulse-width modulated* (*PWM*) *ac voltage controller*).

14.2.1 Phase-Controlled Single-Phase AC Voltage Controller

For a full-wave symmetrical phase control, the SCRs T_1 and T_2 in Fig. 14.1A are gated at α and $\pi+\alpha$, respectively, from the zero crossing of the input voltage; by varying α, the power flow to the load is controlled through voltage control in alternate half cycles. As long as one SCR is carrying current, the other SCR remains reverse-biased by the voltage drop across the conducting SCR. The principle of operation in each half cycle is similar to that of the controlled half-wave rectifier, and one can use the same approach for analysis of the circuit.

Operation with R-load. Fig. 14.2 shows the typical voltage and current waveforms for the single-phase bidirectional phase-controlled ac voltage controller of Fig. 14.1A with a resistive load. The output voltage and current waveforms have half-wave symmetry and so no dc component.

If $v_s = \sqrt{2}V_s \sin \omega t$ is the source voltage, the rms output voltage with T_1 triggered at α can be found from the half-wave symmetry as

$$V_o = \left[\frac{1}{\pi}\int_{\alpha}^{\pi} 2V_s^2 \sin^2 \omega t d(\omega t)\right]^{\frac{1}{2}} = V_s\left[1 - \frac{\alpha}{\pi} + \frac{\sin 2\alpha}{2\pi}\right]^{\frac{1}{2}} \quad (14.1)$$

Note that V_o can be varied from V_s to 0 by varying α from 0 to π:

$$\text{The rms value of load current, } I_o = \frac{V_o}{R} \quad (14.2)$$

$$\text{The input power factor} = \frac{P_o}{VA} = \frac{V_o}{V_s} = \left[1 - \frac{\alpha}{\pi} + \frac{\sin 2\alpha}{2\pi}\right]^{\frac{1}{2}} \quad (14.3)$$

$$\text{The average SCR current, } I_{A,\,SCR} = \frac{1}{2\pi R}\int_{\alpha}^{\pi} \sqrt{2}V_s \sin \omega t \mathrm{d}(\omega t) \quad (14.4)$$

Since each SCR carries half the line current, the rms current in each SCR is

$$I_{o,\,SCR} = \frac{I_o}{\sqrt{2}} \quad (14.5)$$

Operation with RL Load. Fig. 14.3 shows the voltage and current waveforms for the controller in Fig. 14.1A with RL load. Due to the inductance, the current carried by the SCR T_1 may not fall to zero at $\omega t = \pi$ when the input voltage goes

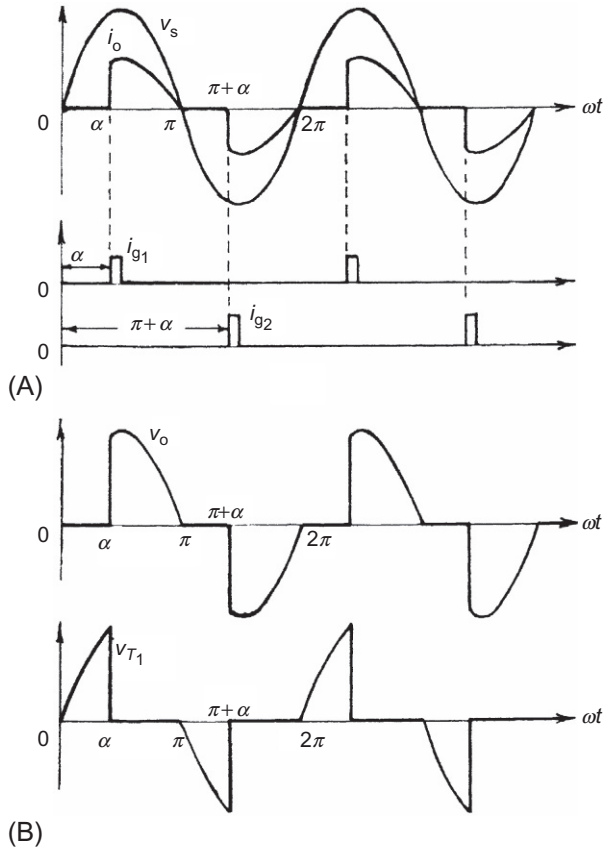


FIG. 14.2 Waveforms for single-phase ac full-wave voltage controller with R-load.

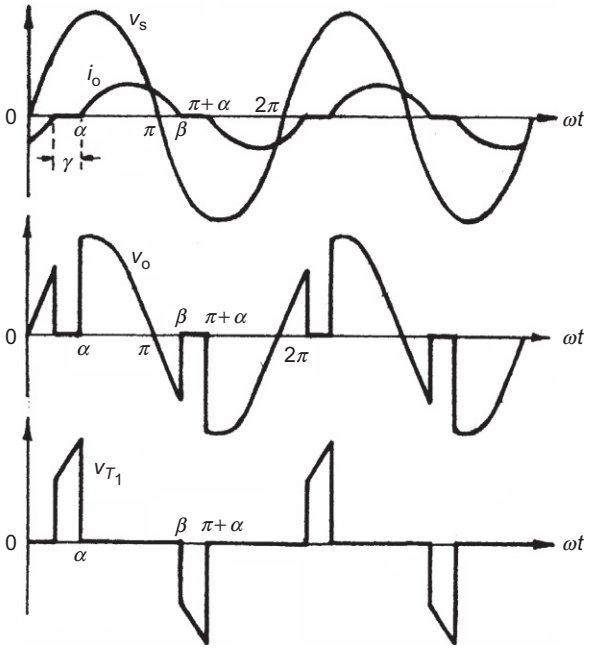


FIG. 14.3 Typical waveforms of single-phase ac voltage controller with an RL load.

negative and may continue till $\omega t = \beta$, the extinction angle, as shown. The conduction angle,

$$\theta = \beta - \alpha \tag{14.6}$$

of the SCR depends on the firing delay angle α and the load impedance angle ϕ.

The expression for the load current $I_o(\omega t)$, when conducting from α to β, can be derived in the same way as that used for a phase-controlled rectifier in a discontinuous mode by solving the relevant Kirchhoff's voltage equation:

$$i_o(\omega t) = \frac{\sqrt{2}V}{Z}\left[\sin(\omega t - \phi) - \sin(\alpha - \phi)e^{(\alpha - \omega t)/\tan\phi}\right], \quad \alpha < \omega t < \beta \tag{14.7}$$

where $Z = (R^2 + \omega^2 L^2)^{\frac{1}{2}} = \text{load impedance}$ and $\phi = \text{load impedance angle} = \tan^{-1}(\omega L/R)$.

The angle β, when the current i_o falls to zero, can be determined from the following transcendental equation resulted by using $i_o(\omega t = \beta) = 0$ in Eq. (14.7):

$$\sin(\beta - \phi) = \sin(\alpha - \phi) - \sin(\alpha - \phi)e^{(\alpha - \beta)/\tan\phi} \tag{14.8}$$

From Eqs. (14.6) and (14.8), one can obtain a relationship between θ and α for a given value of ϕ, as shown in Fig. 14.4, which shows that as α is increased, the conduction angle θ decreases, and thus, the rms value of the current decreases.

The rms output voltage

$$V_o = \left[\frac{1}{\pi}\int_{\alpha}^{\beta} 2V_s^2 \sin^2\omega t d(\omega t)\right]^{\frac{1}{2}} = \frac{V_s}{\pi}\left[\beta - \alpha + \frac{\sin 2\alpha}{2} - \frac{\sin 2\beta}{2}\right]^{\frac{1}{2}} \tag{14.9}$$

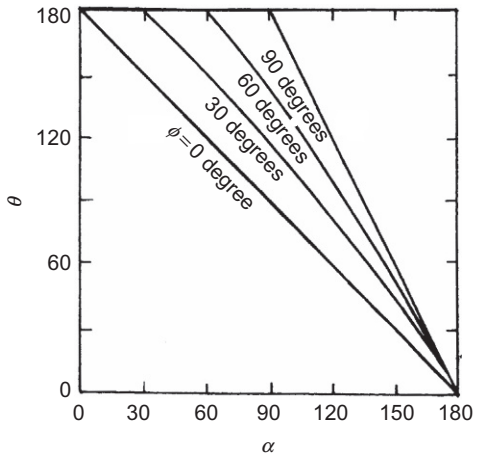


FIG. 14.4 θ versus α curves for single-phase ac voltage controller with RL load.

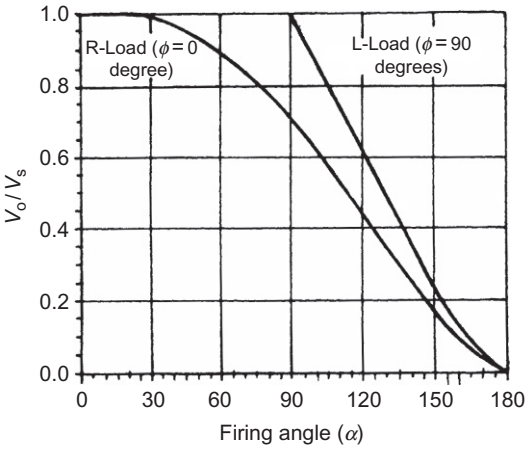


FIG. 14.5 Envelope of control characteristics of a single-phase ac voltage controller with RL load.

V_o can be evaluated for two possible extreme values of $\phi = 0$ when $\beta = \pi$, and $\phi = \pi/2$ when $\beta = 2\pi - \alpha$, and the envelope of the voltage control characteristics for this controller is shown in Fig. 14.5.

The rms SCR current can be obtained from Eq. (14.7) as follows:

$$I_{o,\,SCR} = \left[\frac{1}{2\pi}\int_{\alpha}^{\beta} i_o^2 d(\omega t)\right]^{\frac{1}{2}} \tag{14.10}$$

$$\text{The rms load current, } I_o = \sqrt{2}I_{o,\,SCR} \tag{14.11}$$

$$\text{The average value of SCR current, } I_{A,\,SCR} = \frac{1}{2\pi}\int_{\alpha}^{\beta} i_o d(\omega t) \tag{14.12}$$

Gating Signal Requirements. For the inverse-parallel SCRs as shown in Fig. 14.1A, the gating signals of SCRs must be isolated from one another because there is no common cathode. For R-load, each SCR stops conducting at the end of each half cycle and under this condition, single short pulses may be used for gating as shown in Fig. 14.2. With RL load, however, this single short pulse gating is not suitable as shown in Fig. 14.6. When SCR T_2 is triggered at $\omega t = \pi + \alpha$, SCR T_1 is still conducting due to the load inductance. By the time the SCR T_1 stops conducting at β, the gate pulse for SCR T_2 has already ceased and T_2 will fail to turn on resulting the converter to operate as a single-phase rectifier with conduction of T_1 only. This necessitates the application of a sustained gate pulse in the form of either a continuous signal for the half-cycle period or better a train of pulses (carrier frequency gating) as the former results in increased dissipation in SCR gate circuit, and a large isolating pulse transformer is required.

Operation with $\alpha < \phi$. If $\alpha = \phi$, then from Eq. (14.8),

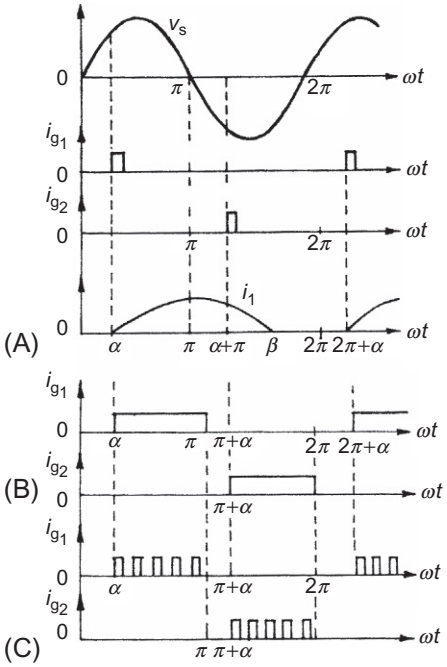


FIG. 14.6 Single-phase full-wave controller with RL load: gate pulse requirements.

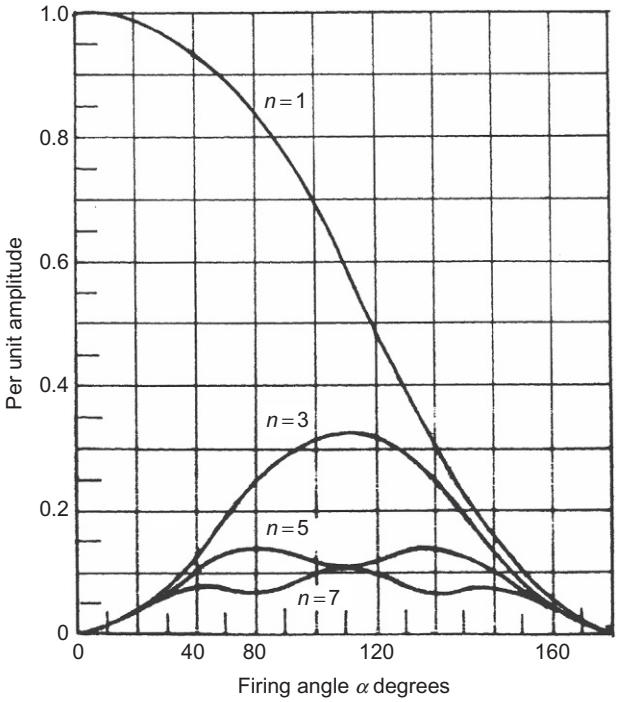


FIG. 14.7 Harmonic content as a function of the firing angle for a single-phase voltage controller with RL load.

$$\sin(\beta-\phi)=\sin(\beta-\alpha)=0 \tag{14.13}$$

and

$$\beta-\alpha=\theta=\pi \tag{14.14}$$

As the conduction angle θ cannot exceed π and the load current must pass through zero, the control range of the firing angle is $\phi \le \alpha \le \pi$. With narrow gating pulses and $\alpha < \phi$, only one SCR will conduct resulting in a rectifier action as shown. Even with a train of pulses, if $\alpha < \phi$, the changes in the firing angle will not change the output voltage and current but both the SCRs will conduct for the period π with T_1 becoming on at $\omega t = \pi$ and T_2 at $\omega t + \pi$.

The duration of this *dead zone* ($\alpha = 0$ to ϕ), which varies with the load impedance angle ϕ, is not a desirable feature in closed-loop control schemes. An alternative approach to the phase control with respect to the input voltage zero crossing has been visualized in which the firing angle is defined with respect to the instant when it is the load current, not the input voltage, that reaches zero, this angle being called *the hold-off angle* (γ) *or the control angle* (as marked in Fig. 14.3). This method needs sensing the load current, which may otherwise be required in a closed-loop controller for monitoring or control purposes.

Power Factor and Harmonics. As in the case of phase-controlled rectifiers, the important limitations of the phase-controlled ac voltage controllers are the poor power factor and the introduction of harmonics in the source currents. As seen from Eq. (14.3), the input power factor depends on α, and as α increases, the power factor decreases.

The harmonic distortion increases and the quality of the input current decreases with increase of firing angle. The variations of low-order harmonics with the firing angle as computed by Fourier analysis of the voltage waveform of Fig. 14.2 (with R-load) are shown in Fig. 14.7. Only odd harmonics exist in the input current because of half-wave symmetry.

14.2.2 Single-Phase AC-AC Voltage Controller with On/Off Control

Integral Cycle Control. As an alternative to the phase control, the method of integral cycle control or burst firing is used for systems with large time constants, for example, heating loads. Here, the switch is turned on for a time t_n with n integral cycles and turned off for a time t_m with m integral cycles (Fig. 14.8). As the SCRs or triacs used here are turned on at the zero crossing of the input voltage and turn off occurs at zero current, supply harmonics and radio-frequency interference are very low.

However, subharmonic frequency components may be generated, which are undesirable because they may set up subharmonic resonance in the power supply system, cause lamp flicker, and may interfere with the natural frequencies of motor loads causing shaft oscillations.

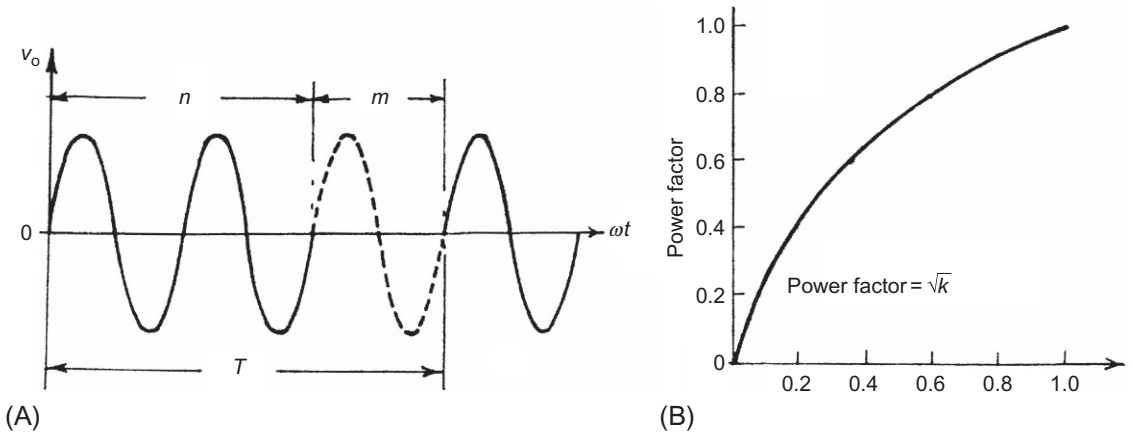


FIG. 14.8 Integral cycle control: (A) typical load voltage waveforms and (B) power factor with the duty cycle k.

For sinusoidal input voltage, $v = \sqrt{2}V_s \sin \omega t$, the rms output voltage

$$V_o = V_s\sqrt{k} \text{ where } k = n/(n+m) = \text{duty cycle and } V_s = \text{rms phase voltage} \quad (14.15)$$

$$\text{The power factor} = \sqrt{k} \quad (14.16)$$

which is poorer for lower values of the duty cycle k.

PWM AC Chopper. As in the case of controlled rectifier, the performance of ac voltage controllers can be improved in terms of harmonics, quality of output current, and input power factor by PWM control in PWM ac choppers; the circuit configuration of one such single-phase unit is shown in Fig. 14.9. Here, fully controlled switches S_1 and S_2 connected in antiparallel are turned on and off many times during the positive and negative half cycles of the input voltage, respectively. S_1' and S_2' provide the freewheeling paths for the load current when S_1 and S_2 are off. An input capacitor filter may be provided to attenuate the high switching frequency currents drawn from the supply and also to improve the input power factor. Fig. 14.10 shows the typical output voltage and load current waveform for a single-phase PWM ac chopper. It can be shown that the control characteristics of an ac chopper depend on the *modulation index M*, which theoretically varies from 0 to 1.

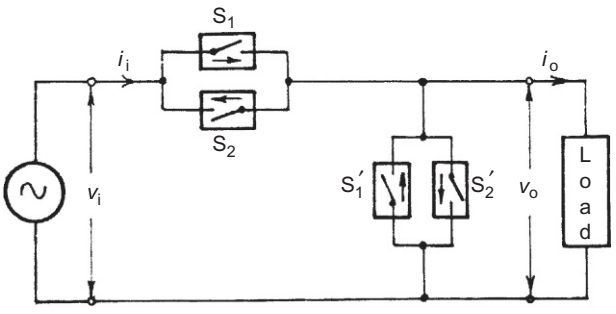


FIG. 14.9 Single-phase PWM ac chopper circuit.

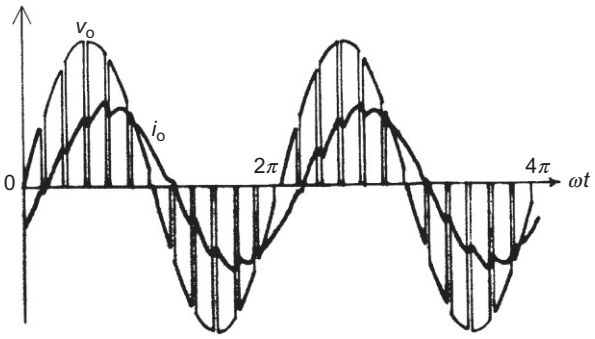


FIG. 14.10 Typical output voltage and current waveforms of a single-phase PWM ac chopper.

Three-phase PWM choppers consist of three single-phase choppers connected in either delta or four-wire (star) configuration.

14.3 Three-Phase AC-AC Voltage Controllers

14.3.1 Phase-Controlled Three-Phase AC Voltage Controllers

Various Configurations. Several possible circuit configurations for three-phase phase-controlled ac regulators with star- or delta-connected loads are shown in Fig. 14.11A–H.

The configurations in (A) and (B) can be realized by three single-phase ac regulators operating independently of each other, and they are easy to analyze. In (A), the SCRs are to be rated to carry line currents and withstand phase voltages, whereas in (B) they should be capable to carry phase currents and withstand the line voltage. In (B), the line currents are free from triplen harmonics while these are present in the closed

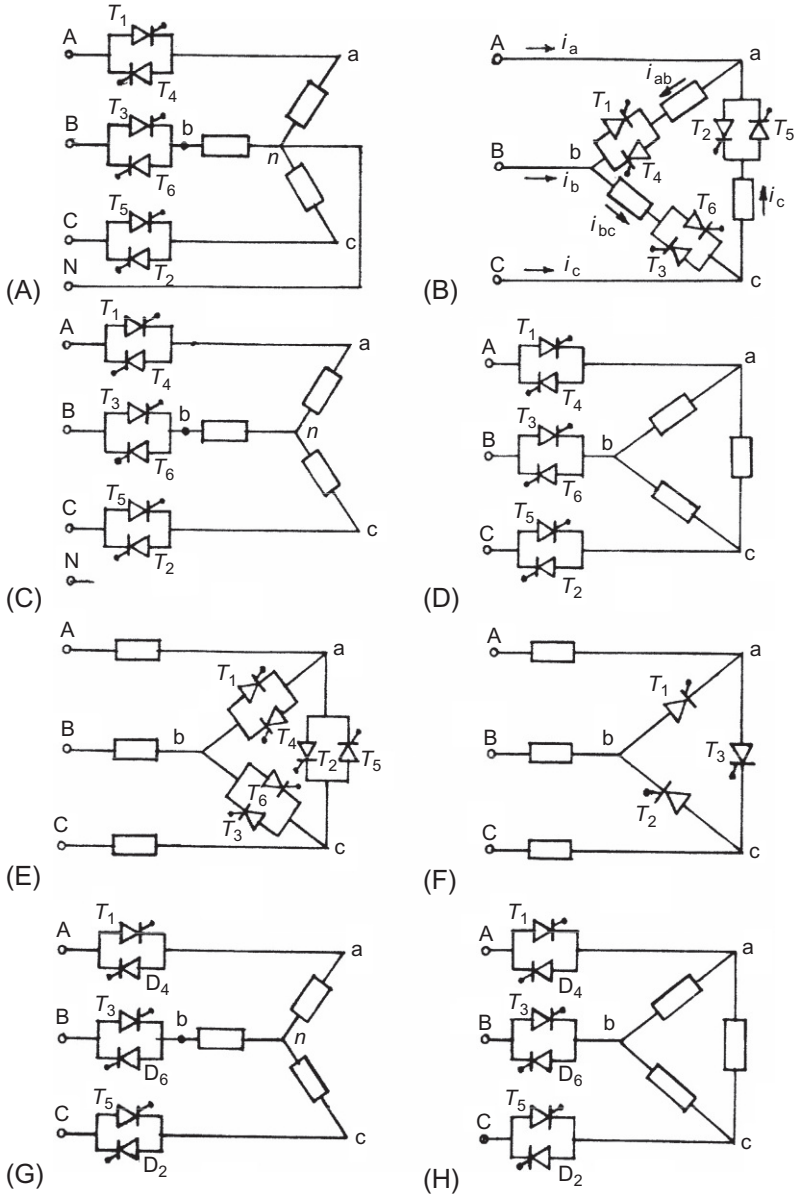


FIG. 14.11 Three-phase ac voltage controller circuit configurations.

delta. The power factor in (B) is slightly higher. The firing angle control range for both these circuits is 0–180 degrees for R-load.

The circuits in (C) and (D) are three-phase three-wire circuits and are complicated to analyze. In both these circuits, at least two SCRs, one in each phase, must be gated simultaneously to get the controller started by establishing a current path between the supply lines. This necessitates two firing pulses spaced at 60 degrees apart per cycle for firing each SCR. The operation modes are defined by the number of SCRs conducting in these modes. The firing control range is 0–150 degrees. The triplen harmonics are absent in both these configurations.

Another configuration is shown in (E) when the controllers are connected in delta and the load is connected between the supply and the converter. Here, current can flow between two lines even if one SCR is conducting so each SCR requires one firing pulse per cycle. The voltage and current ratings of SCRs are nearly the same as that of the circuit (B). It is also possible to reduce the number of devices to three SCRs in delta as shown in (F), connecting one source terminal directly to one load circuit terminal. Each SCR is provided with gate pulses in each cycle spaced at 120 degrees apart. In both (E) and (F), each end of each phase must be accessible. The number of devices in (F) is less, but their current ratings must be higher.

As in the case of single-phase phase-controlled voltage regulator, the total regulator cost can be reduced by replacing six SCRs by three SCRs and three diodes, resulting in three-phase *half-wave controlled* unidirectional ac regulators as shown in (G) and (H) for star- and delta-connected loads. The main drawback of these circuits is the large harmonic content in the output voltage—particularly, the second harmonic because of the asymmetry. However, the dc components are absent in the line. The maximum firing angle in the half-wave controlled regulator is 210 degrees.

14.3.2 Fully Controlled Three-Phase Three-Wire AC Voltage Controller

Star-connected Load with Isolated Neutral. The analysis of operation of the full-wave controller with isolated neutral as shown in Fig. 14.11C is, as mentioned, quite complicated in comparison with that of a single-phase controller, particularly for an RL or motor load. As a simple example, the operation of this controller with a simple star-connected R-load is considered here. The six SCRs are turned on in the sequence 1-2-3-4-5-6 at 60 degrees intervals, and the gate signals are sustained throughout the possible conduction angle.

The output phase voltage waveforms for $\alpha = 30$, 75, and 120 degrees for a balanced three-phase R-load are shown in Fig. 14.12. At any interval, either three SCRs or two SCRs or no SCRs may be on, and the instantaneous output voltages to the load are either a line-to-neutral voltage (three SCRs on) or one-half of the line-to-line voltage (two SCRs on) or zero (no SCR on).

Depending on the firing angle α, there may be *three* operating modes:

Mode I (*also known as Mode 2/3*). 0 degrees $\leq \alpha \leq$ 60 degrees; There are periods when *three* SCRs are conducting, one in each phase for either direction, and there are periods when just *two* SCRs conduct.

For example, with $\alpha = 30$ degrees in Fig. 14.12A, assume that at $\omega t = 0$, SCRs T_5 and T_6 are conducting, and the current through the R-load in a-phase is zero making $v_{an} = 0$. At $\omega t = 30$ degrees, T_1 receives a gate pulse and starts conducting; T_5 and T_6 remain on, and $v_{an} = v_{AN}$. The current in T_5 reaches zero at 60 degrees, turning T_5 off. With T_1 and T_6 staying on, $v_{an} = \frac{1}{2}v_{AB}$. At 90 degrees, T_2 is turned on, the three SCRs T_1, T_2, and T_6 are then conducting, and $v_{an} = v_{AN}$. At 120 degrees, T_6 turns off, leaving T_1 and T_2 on, so $v_{an} = \frac{1}{2}v_{AC}$. Thus, with the progress of firing in sequence till $\alpha = 60$ degrees, the number of SCRs conducting at a particular instant alternates between two and three.

Mode II (*also known as Mode 2/2*). 60 degrees $\leq \alpha \leq$ 90 degrees; Two SCRs, one in each phase, always conduct.

For $\alpha = 75$ degrees as shown in Fig. 14.12B, just prior to $\alpha = 75$ degrees, SCRs T_5 and T_6 were conducting, and $v_{an} = 0$. At 75 degrees, T_1 is turned on, and T_6 continues to conduct, whereas T_5 turns off as v_{CN} is negative. $v_{an} = \frac{1}{2}v_{AB}$. When

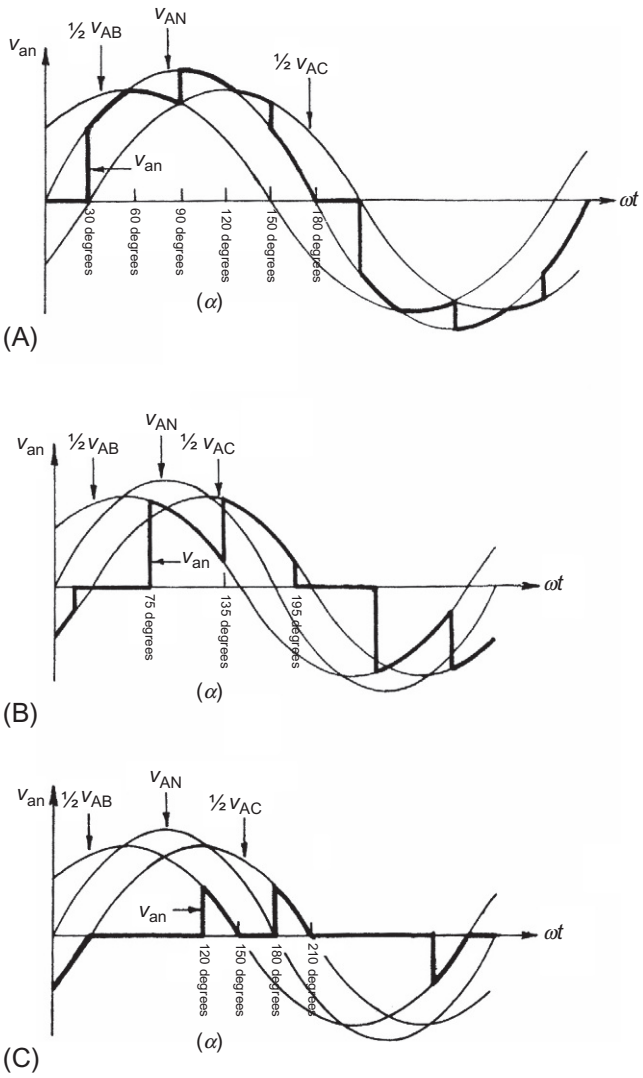


FIG. 14.12 Output voltage waveforms for a three-phase ac voltage controller with star-connected R-load: (A) v_{an} for $\alpha = 30°$, (B) v_{an} for $\alpha = 75°$, and (C) $v_{an} = 120°$.

T_2 is turned on at 135 degrees, T_6 is turned off, and $v_{an} = \frac{1}{2}v_{AC}$. The next SCR to turn on is T_3, which turns off T_1, and $v_{an} = 0$. One SCR is always turned off when another is turned on in this range of α, and the output voltage is either one-half line-to-line voltage or zero.

Mode III (*also known as Mode 0/2*). 90 degrees $\leq \alpha \leq$ 150 degrees, when *none* or *two* SCRs conduct.

For $\alpha = 120$ degrees, Fig. 14.12C, earlier, no SCRs were on, and $v_{an} = 0$. At $\alpha = 120$ degrees, SCR T_1 is given a gate signal, whereas T_6 has a gate signal already applied. Since v_{AB} is positive, T_1 and T_6 are forward-biased, and they begin to conduct, and $v_{an} = \frac{1}{2}v_{AB}$. Both T_1 and T_6 turn off when v_{AB} becomes negative. When a gate signal is given to T_2, it turns on, and T_1 turns on again.

For $\alpha > 150$ degrees, there is no period when two SCRs are conducting and the output voltage is zero at $\alpha = 150$ degrees.

Thus, the range of the firing angle control is 0 degrees $\leq \alpha \leq$ 150 degrees.

For *star-connected R-load*, assuming the instantaneous phase voltages as

$$\begin{aligned} v_{AN} &= \sqrt{2}V_s \sin \omega t \\ v_{BN} &= \sqrt{2}V_s \sin \omega t - 120 \text{ degrees} \\ v_{CN} &= \sqrt{2}V_s \sin \omega t - 240 \text{ degrees} \end{aligned} \tag{14.17}$$

the expressions for the rms output phase voltage V_o can be derived for the three modes as follows:

$$0 \text{ degrees} \leq \alpha \leq 60 \text{ degrees} \quad V_o = V_s \left[1 - \frac{3\alpha}{2\pi} + \frac{3}{4\pi} \sin 2\alpha\right]^{\frac{1}{2}} \tag{14.18}$$

$$60 \text{ degrees} \leq \alpha \leq 90 \text{ degrees} \quad V_o = V_s \left[\frac{1}{2} + \frac{3}{4\pi} \sin 2\alpha + \sin(2\alpha + 60 \text{ degrees})\right]^{\frac{1}{2}} \tag{14.19}$$

$$90 \text{ degrees} \leq \alpha \leq 150 \text{ degrees} \quad V_o = V_s \left[\frac{5}{4} - \frac{3\alpha}{2\pi} + \frac{3}{4\pi} \sin(2\alpha + 60 \text{ degrees})\right]^{\frac{1}{2}} \tag{14.20}$$

For *star-connected pure L-load*, the effective control starts at $\alpha >$ 90 degrees, and the expressions for two ranges of α are as follows:

$$90 \text{ degrees} \leq \alpha \leq 120 \text{ degrees} \quad V_o = V_s \left[\frac{5}{2} - \frac{3\alpha}{\pi} + \frac{3}{2\pi} \sin 2\alpha\right]^{\frac{1}{2}} \tag{14.21}$$

$$120 \text{ degrees} \leq \alpha \leq 150 \text{ degrees} \quad V_o = V_s \left[\frac{5}{2} - \frac{3\alpha}{\pi} + \frac{3}{2\pi} \sin(2\alpha + 60 \text{ degrees})\right]^{\frac{1}{2}} \tag{14.22}$$

The control characteristics for these two limiting cases ($\phi = 0$ for R-load and $\phi =$ 90 degrees for L-load) are shown in Fig. 14.13. Here also, like the single-phase case, the dead zone may be avoided by controlling the voltage with respect to the control angle or hold-off angle (γ) from the zero crossing of current in place of the firing angle α.

RL Load. The analysis of the three-phase voltage controller with star-connected RL load with isolated neutral is quite complicated, since the SCRs do not cease to conduct at voltage zero, and the extinction angle β is to be known by solving the transcendental equation for the case. In this case, the mode II operation disappears [1], and the operation shift from mode I to mode III depends on the so-called critical angle α_{crit} [2,3], which can be evaluated from a numerical solution of the relevant transcendental equations. Computer simulation by either PSPICE program [4,5] or switching-variable approach coupled

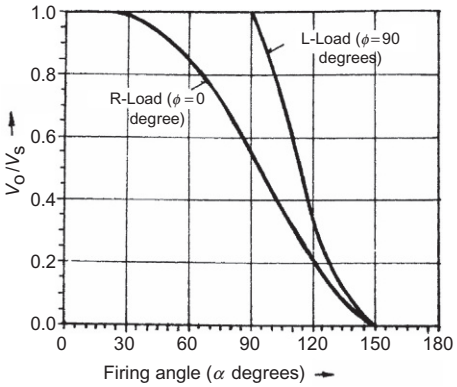


FIG. 14.13 Envelope of control characteristics for a three-phase full-wave ac voltage controller.

with an iterative procedure [6] is a practical means of obtaining the output voltage waveform in this case. Fig. 14.14 shows typical simulation results using the later approach [6] for a three-phase voltage controller-fed RL load for $\alpha =$ 60, 90, and 105 degrees, which agree with the corresponding practical oscillograms given in [7].

Delta-Connected R-Load. The configuration is shown in Fig. 14.11B. The voltage across an R-load is the corresponding line-to-line voltage when one SCR in that phase is on. Fig. 14.15 shows the line and phase currents for $\alpha =$ 130 and 90 degrees with an R-load. The firing angle α is measured from the zero crossing of the line-to-line voltage, and the SCRs are turned on in the sequence as they are numbered. As in the single-phase case, the range of firing angle is $0 \leq \alpha \leq$ 180 degrees. The line currents can be obtained from the phase currents as follows:

$$\begin{aligned} i_a &= i_{ab} - i_{ca} \\ i_b &= i_{bc} - i_{ab} \\ i_c &= i_{ca} - i_{bc} \end{aligned} \tag{14.23}$$

The line currents depend on the firing angle and may be discontinuous as shown. Due to the delta connection, the triplen harmonic currents flow around the closed delta and do not appear in the line. The rms value of the line current varies between the range

$$\sqrt{2}I_\Delta \leq I_{L,\,rms} \leq \sqrt{3}I_{\Delta,\,rms} \tag{14.24}$$

as the conduction angle varies from very small (large α) to 180 degrees ($\alpha = 0$).

14.4 Cycloconverters

In contrast to the ac voltage controllers operating at constant frequency discussed so far, a cycloconverter operates as a direct ac-ac frequency changer with inherent voltage control feature. The basic principle of this converter to construct an alternating voltage wave of lower frequency from successive segment of

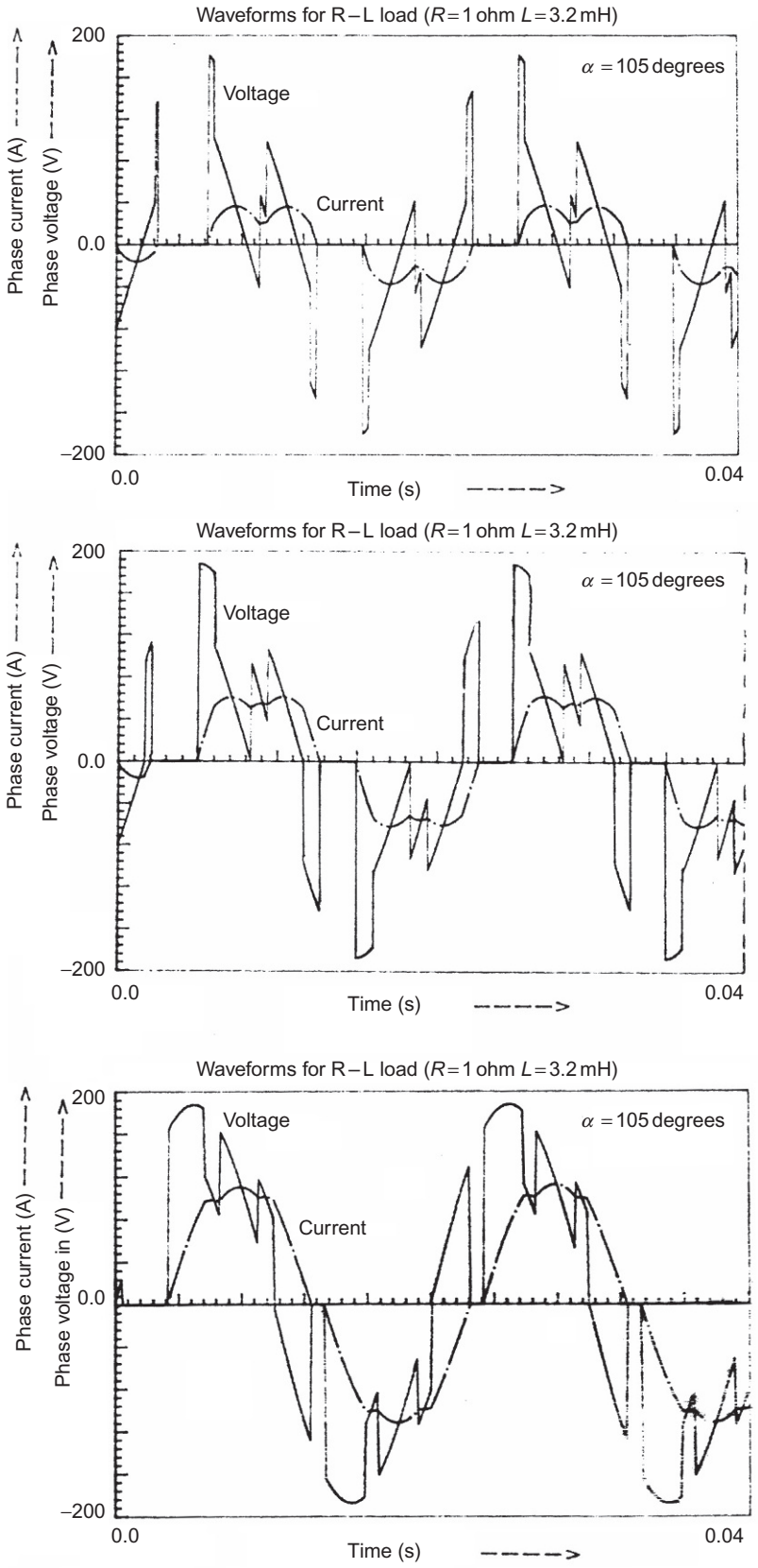


FIG. 14.14 Typical simulation results for three-phase ac voltage controller-fed RL load ($R = 1\,\Omega, L = 3.2\,\text{mH}$) for $\alpha = 60°$, 90°, and 105°.

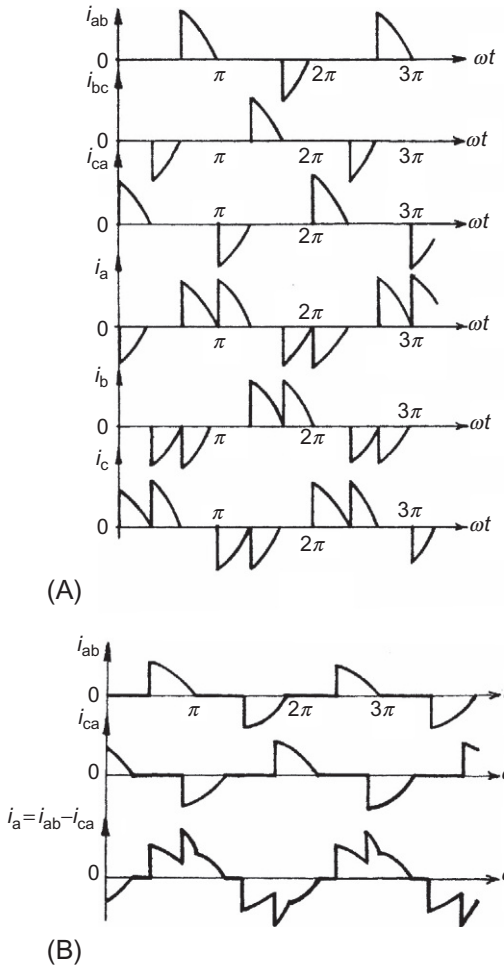


FIG. 14.15 Waveforms of a three-phase ac voltage controller with a delta-connected R-load: (A) $\alpha = 120°$ and (B) $\alpha = 90°$.

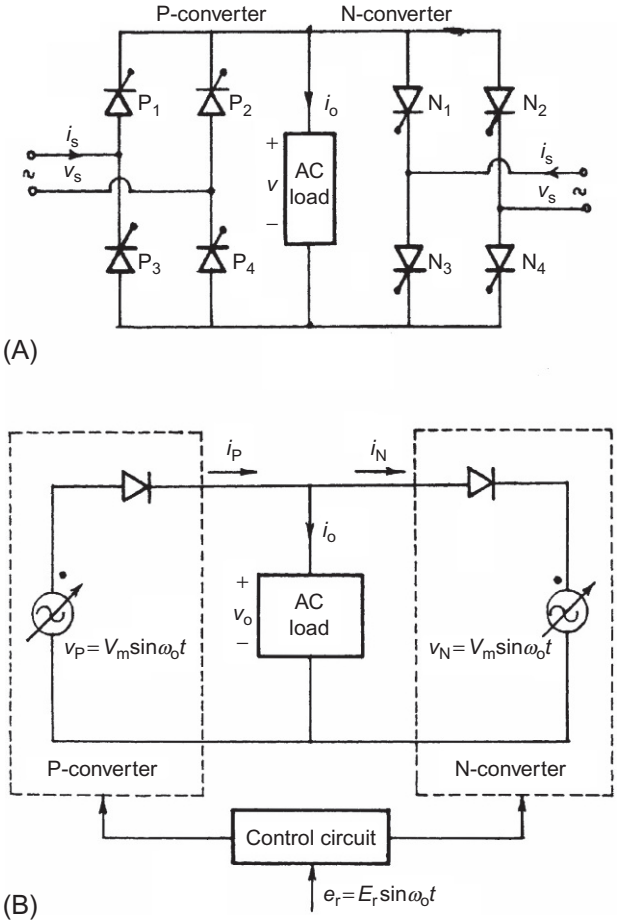


FIG. 14.16 (A) Power circuit for a single-phase bridge cycloconverter and (B) simplified equivalent circuit of a cycloconverter.

voltage waves of higher frequency ac supply by a switching arrangement was conceived and patented in the 1920s. Grid-controlled mercury-arc rectifiers were used in these converters installed in Germany in the 1930s to obtain $16\frac{2}{3}-$ Hz single-phase supply for ac series traction motors from a three-phase 50 Hz system, while at the same time, a cycloconverter using 18 thyratrons supplying a 400 hp synchronous motor was in operation for some years as a power station auxiliary drive in the United States. However, the practical and commercial utilization of these schemes waited till the SCRs became available in the 1960s. With the development of large-power SCRs and microprocessor-based control, the cycloconverter today is a matured practical converter for application in large-power low-speed variable-voltage variable-frequency (VVVF) ac drives in cement and steel rolling mills and in variable-speed constant-frequency (VSCF) systems in aircrafts and naval ships.

A cycloconverter is a naturally commuted converter with inherent capability of bidirectional power flow, and there is no real limitation on its size unlike an SCR inverter with commutation elements. Here, the switching losses are considerably low, the regenerative operation at full power over complete speed range is inherent and it delivers a nearly sinusoidal waveform resulting in minimum torque pulsation and harmonic heating effects. It is capable of operating even with blowing out of individual SCR fuse (unlike inverter), and the requirements regarding turn-off time, current rise time, and *dv*/*dt* sensitivity of SCRs are low. The main limitations of a naturally commutated cycloconverter are (1) limited frequency range for subharmonic free and efficient operation and (2) poor input displacement/power factor, particularly at low-output voltages.

14.4.1 Single-Phase to Single-Phase Cycloconverter

Though rarely used, the operation of a single-phase to single-phase cycloconverter is useful to demonstrate the basic principle involved. Fig. 14.16A shows the power circuit of a single-phase bridge type of cycloconverter, which has the same

arrangement as that of a single-phase dual converter. The firing angles of the individual two-pulse two-quadrant bridge converters are continuously modulated here, so that each ideally produces the same fundamental ac voltage at its output terminals as marked in the simplified equivalent circuit in Fig. 14.16B. Because of the unidirectional current-carrying property of the individual converters, it is inherent that the positive half cycle of the current is carried by the P-converter and the negative half cycle of the current by the N-converter regardless of the phase of the current with respect to the voltage. This means that for a reactive load, each converter operates in both rectifying and inverting region during the period of the associated half cycle of the low-frequency output current.

Operation with R-Load. Fig. 14.17 shows the input and output voltage waveforms with a pure R-load for a $50-16\frac{2}{3}-$ Hz cycloconverter. The P- and N-converters operate for alternate $T_o/2$ periods. The output frequency $(1/T_o)$ can be varied by varying T_o and the voltage magnitude by varying the firing angle α of the SCRs. As shown in the figure, three cycles of the ac input wave are combined to produce one cycle of the output frequency to reduce the supply frequency to one-third across the load.

If α_P is the firing angle of the P-converter, the firing angle of the N-converter α_N is $\pi-\alpha_P$, and the average voltage of the P-converter is equal and opposite to that of the N-converter.

The inspection of Fig. 14.17 shows that the waveform with α remaining fixed in each half cycle generates a square wave having a large low-order harmonic content. A near approximation to sine wave can be synthesized by a phase modulation of the firing angles as shown in Fig. 14.18 for a 50–10 Hz cycloconverter. The harmonics in the load voltage waveform are less compared with earlier waveform. The supply current, however, contains a subharmonic at the output frequency for this case as shown.

Operation with RL Load. The cycloconverter is capable of supplying loads of any power factor. Fig. 14.19 shows the idealized output voltage and current waveforms for a lagging power factor load where both the converters are operating as rectifier and inverter at the intervals marked. The load current lags the output voltage, and the load current direction determines

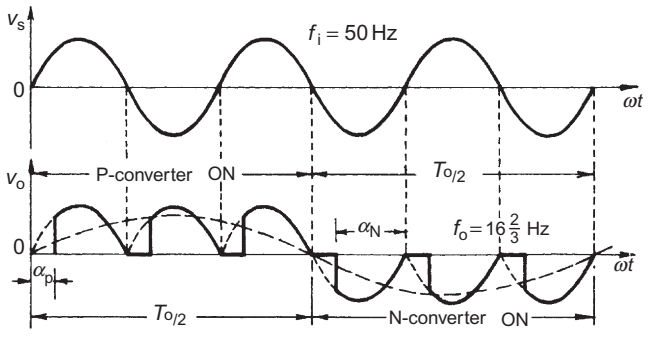


FIG. 14.17 Input and output waveforms of a $50-16\frac{2}{3}-$ Hz cycloconverter with RL load.

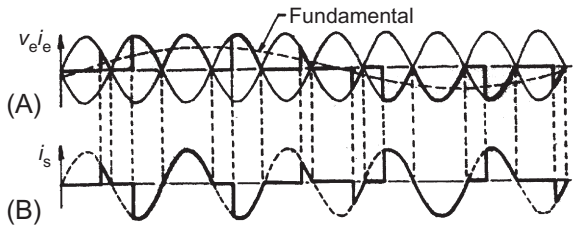


FIG. 14.18 Waveforms of a single-phase to single-phase cycloconverter (50–10 Hz) with RL load: (A) load voltage and load current and (B) input supply current.

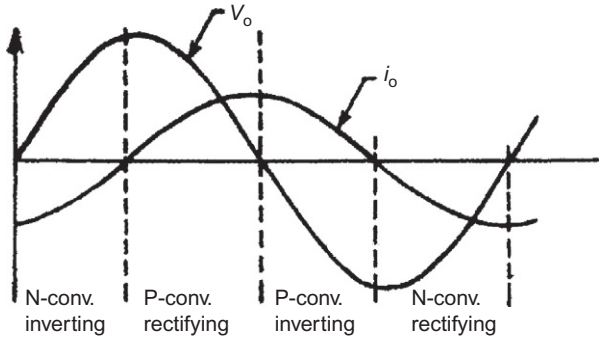


FIG. 14.19 Idealized load voltage and current waveform for a cycloconverter with RL load.

which converter is conducting. Each converter continues to conduct after its output voltage changes polarity, and during this period, the converter acts as an inverter, and the power is returned to the ac source. Inverter operation continues till the other converter starts to conduct. By controlling the frequency of oscillation and the *depth of modulation* of the firing angles of the converters (as shown later), it is possible to control the frequency and the amplitude of the output voltage.

The load current with RL load may be continuous or discontinuous depending on the load phase angle, ϕ. At light load inductance or for $\phi \le \alpha \le \pi$, there may be discontinuous load current with short zero-voltage periods. The current wave may contain even harmonics and subharmonic components. Further, as in the case of dual converter, although the mean output voltage of the two converters is equal and opposite, the instantaneous values may be unequal and a circulating current can flow within the converters. This circulating current can be limited by having a center-tapped reactor connected between the converters or can be completely eliminated by logical control similar to the dual converter case when the gate pulses to the converter remaining idle are suppressed, when the other converter is active. In practice, a zero-current interval of short duration is needed, in addition, between the operation of the P- and N-converters to ensure that the supply lines of the two converters are not short-circuited. With circulating current-free operation, the control scheme becomes complicated if the load current is discontinuous.

In the case of the circulating current scheme, the converters are kept in virtually continuous conduction over the whole range, and the control circuit is simple. To obtain reasonably good sinusoidal voltage waveform using the line-commutated two-quadrant converters and eliminate the possibility of the short circuit of the supply voltages, the output frequency of the cycloconverter is limited to a much lower value of the supply frequency. The output voltage waveform and the output frequency range can be improved further by using converters of higher pulse numbers.

14.4.2 Three-Phase Cycloconverters

14.4.2.1 Three-Phase Three-Pulse Cycloconverter

Fig. 14.20A shows the schematic diagram of a three-phase half-wave (three-pulse) cycloconverter feeding a single-phase load and Fig. 14.20B the configuration of a three-phase half-wave (three-pulse) cycloconverter feeding a three-phase load. The basic process of a three-phase cycloconversion is illustrated in Fig. 14.20C at 15 Hz, 0.6 power factor lagging load from a 50 Hz supply. As the firing angle α is cycled from zero at "a" to 180 degrees at "j," half a cycle of output frequency is produced (the gating circuit is to be suitably designed to introduce this oscillation of the firing angle). For this load, it can be seen that although the mean output voltage reverses at X, the mean output current (assumed sinusoidal) remains positive until Y. During XY, the SCRs A, B, and C in P-converter are "inverting."

A similar period exists at the end of the negative half cycle of the output voltage when D, E, and F SCRs in N-converter are "inverting." Thus, the operation of the converter follows in the order of "rectification" and "inversion" in a cyclic manner; the relative durations are dependent on load power factor. The output frequency is that of the firing angle oscillation about a quiescent point of 90 degrees (condition when the mean output voltage, given by $V_o = V_{do} \cos \alpha$, is zero). For obtaining the positive half cycle of the voltage, firing angle α is varied from 90 to 0 degrees, and then to 90 degrees and, for the negative half cycle, from 90, to 180 degrees, and back to 90 degrees. Variation of α within the limits of 180 degrees automatically provides for

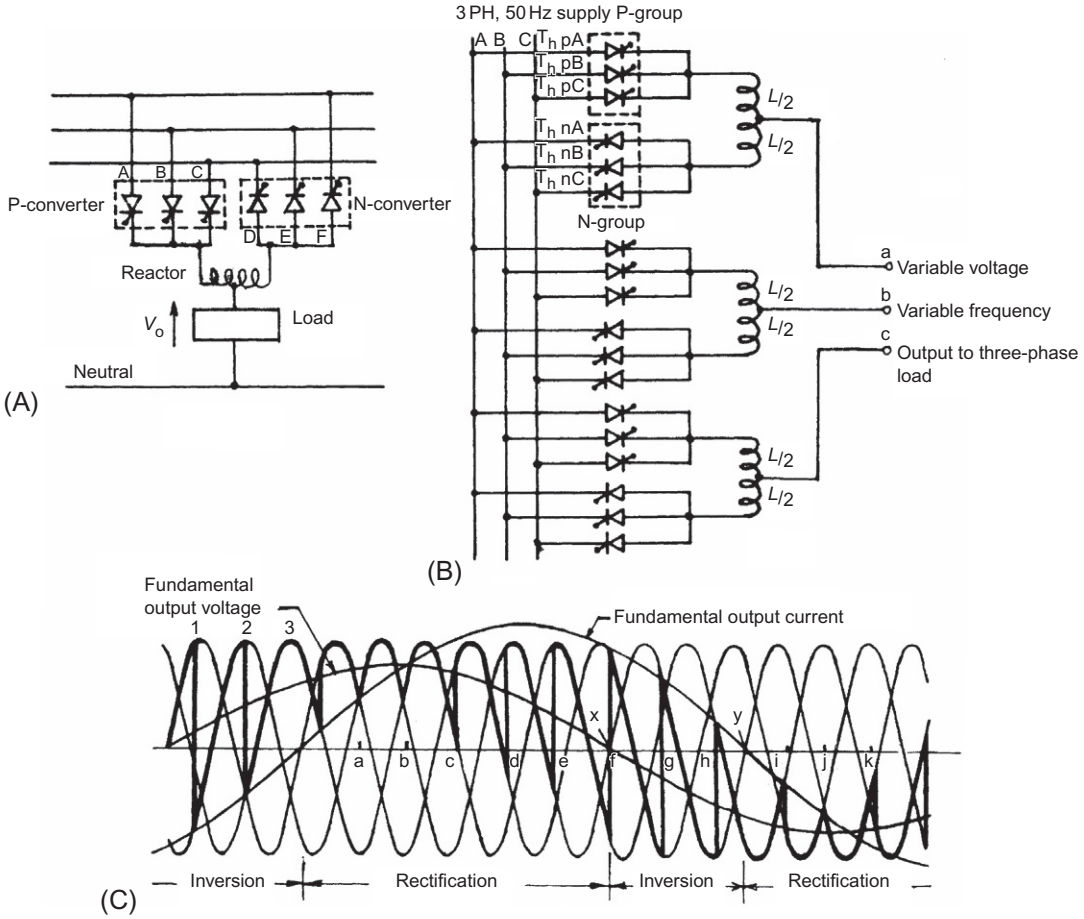


FIG. 14.20 (A) Three-phase half-wave (three-pulse) cycloconverter supplying a single-phase load, (B) three-pulse cycloconverter supplying a three-phase load, and (C) output voltage waveform for one phase of a three-pulse cycloconverter operating at 15 Hz from a 50 Hz supply and 0.6 power factor lagging load.

"natural" line commutation of the SCRs. It is shown that a complete cycle of low-frequency output voltage is fabricated from the segments of the three-phase input voltage by using the phase-controlled converters. The P-converter or N-converter SCRs receive firing pulses, which are timed such that each converter delivers the same mean output voltage. This is achieved, as in the case of single-phase cycloconverter or the dual converter, by maintaining the firing angle constraints of the two groups as $\alpha_P = 180\,\text{degrees} - \alpha_N$. However, the instantaneous voltages of two converters are not identical, and large circulating current may result unless limited by intergroup reactor as shown (*circulating current cycloconverter*) or completely suppressed by removing the gate pulses from the nonconducting converter by an intergroup blanking logic (*circulating current-free cycloconverter*).

Circulating-Current Mode Operation. Fig. 14.21 shows typical waveforms of a three-pulse cycloconverter operating with circulating current. Each converter conducts continuously with rectifying and inverting modes as shown, and the load is supplied with an average voltage of two converters reducing some of the ripple in the process, the intergroup reactor behaving as a potential divider. The reactor limits the circulating current; the value of its inductance to the flow of load current is one-fourth of its value to the flow of circulating current as the inductance is proportional to the square of the number of turns. The fundamental wave produced by both the converters is the same. The reactor voltage is the instantaneous difference between the converter voltages, and the time integral of this voltage divided by the inductance (assuming negligible circuit resistance) is the circulating current. For a three-pulse cycloconverter, it can be observed that this current reaches its peak when $\alpha_P = 60\,\text{degrees}$ and $\alpha_N = 120\,\text{degrees}$.

Output Voltage Equation. A simple expression for the fundamental rms output voltage of the cycloconverter and the required variation of the firing angle α can be derived with the following assumptions: (1) the firing angle α in successive half cycles is varied slowly resulting in a low-frequency output, (2) the source impedance and the commutation overlap are neglected, (3) the SCRs are ideal switches, and (4) the current is continuous and ripple-free. The average dc output voltage of a p-pulse dual converter with fixed α is

$$V_{do} = V_{domax}\cos\alpha, \quad \text{where } V_{domax} = \sqrt{2}V_{ph}\frac{p}{\pi}\sin\frac{\pi}{p} \tag{14.25}$$

For the p-pulse dual converter operating as a cycloconverter, the average phase voltage output at any point of the low frequency should vary according to the equation

$$V_{o,\,av} = V_{o1,\ \max}\sin\omega_o t \tag{14.26}$$

where $V_{o1,max}$ is the desired maximum value of the fundamental output of the cycloconverter.

Comparing Eq. (14.25) with Eq. (14.26), the required variation of α to obtain a sinusoidal output is given by

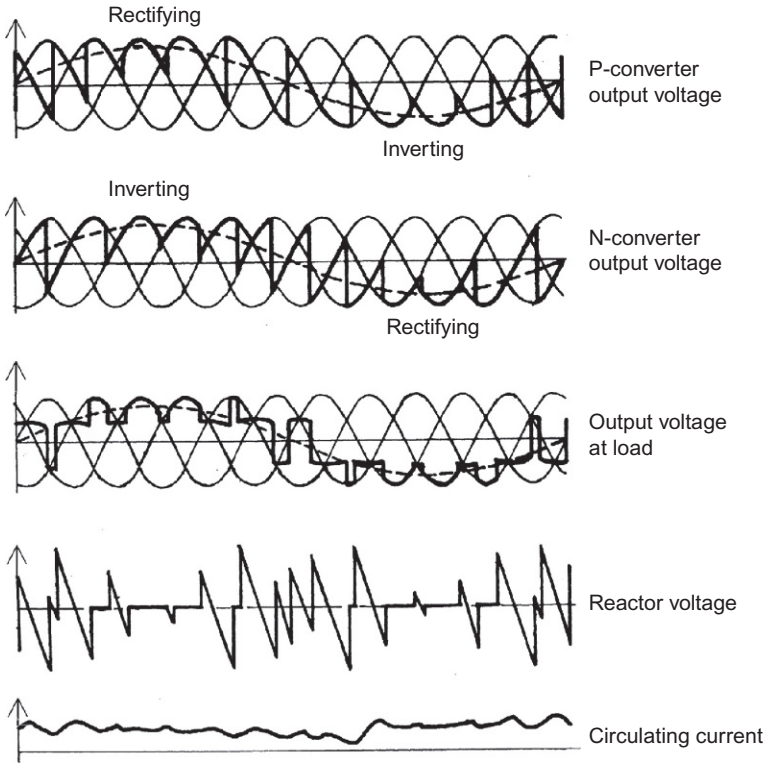


FIG. 14.21 Waveforms of a three-pulse cycloconverter with circulating current.

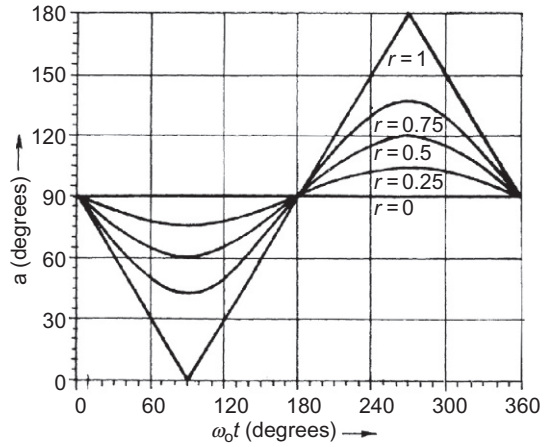


FIG. 14.22 Variations of the firing angle (α) with r in a cycloconverter.

$$\alpha = \cos^{-1}[(V_{o1,\ \max}/V_{domax})\sin\omega_o t] = \cos^{-1}[r\sin\omega_o t] \tag{14.27}$$

where r is the ratio ($V_{o1,max}/V_{domax}$), the *voltage magnitude control ratio*.

Eq. (14.27) shows α as a nonlinear function with r (≤ 1) as shown in Fig. 14.22.

However, the firing angle α_P of the P-converter cannot be reduced to 0 degrees as this corresponds to $\alpha_N = 180$ degrees for the N-converter, which, in practice, cannot be achieved because of allowance for commutation overlap and finite turn-off time of the SCRs. Thus, the firing angle α_P can be reduced to a certain finite value α_{min}, and the maximum output voltage is reduced by a factor cos α_{min}.

The fundamental rms voltage per phase of either converter is

$$V_{or} = V_{oN} = V_{op} = rV_{ph}\frac{p}{\pi}\sin\frac{\pi}{p} \tag{14.28}$$

Though the rms values of the low-frequency output voltage of the P-converter and that of the N-converter are equal, the actual waveforms differ, and the output voltage at the midpoint of the circulating current-limiting reactor (Fig. 14.21), which is the same as the load voltage, is obtained as the mean of the instantaneous output voltages of the two converters.

Circulating Current-free Mode Operation. Fig. 14.23 shows the typical waveforms for a three-pulse cycloconverter operating in this mode with RL load assuming *continuous-current* operation. Depending on the load current direction, only one converter operates at a time, and the load voltage is the same as the output voltage of the conducting converter. As explained earlier in the case of single-phase cycloconverter, there is a possibility of short circuit of the supply voltages at the crossover points of the converter unless taken care of in the control circuit. The waveforms drawn also neglect the effect of overlap due to the ac supply inductance. A reduction in the output voltage is possible by retarding the firing angle gradually at the points a, b, c, d, and e in Fig. 14.23. (This can be easily implemented by reducing the magnitude of the reference voltage in the control circuit.) The circulating current is completely suppressed by blocking all the SCRs in the converter, which is not delivering the load current. A current sensor is incorporated in each output phase of the cycloconverter, which detects the direction of the output current and feeds an appropriate signal to the control circuit to inhibit or blank the gating pulses to the nonconducting converter in the same way as in the case of a dual converter for dc drives. The circulating current-free

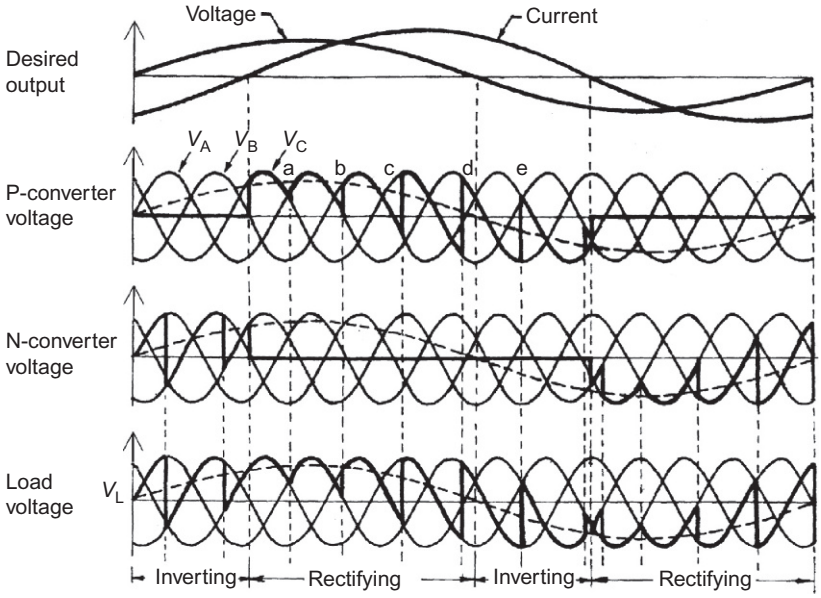


FIG. 14.23 Waveforms for a three-pulse circulating current-free cycloconverter with RL load.

operation improves the efficiency and the displacement factor of the cycloconverter and also increases the maximum usable output frequency. The load voltage transfers smoothly from one converter to the other.

14.4.2.2 Three-Phase Six-Pulse and Twelve-Pulse Cycloconverter

A six-pulse cycloconverter circuit configuration is shown in Fig. 14.24. Typical load voltage waveforms for 6-pulse (with 36 SCRs) and 12-pulse (with 72 SCRs) cycloconverters are shown in Fig. 14.25, the 12-pulse converter being obtained by connecting two six-pulse configurations in series and appropriate transformer connections for the required phase shift. It may be seen that the higher pulse numbers will generate waveforms closer to the desired sinusoidal form and thus permit higher frequency output. The phase loads may be isolated from each other as shown or interconnected with suitable secondary winding connections.

14.4.3 Cycloconverter Control Scheme

Various possible control schemes, analog and digital, for deriving trigger signals and for controlling the basic cycloconverter have been developed over the years.

Out of the several possible signal combinations, it has been shown [8] that a sinusoidal reference signal ($e_r = E_r \sin \omega_o t$) at desired output frequency f_o and a cosine modulating signal ($e_m = E_m \cos \omega_i t$) at input frequency f_i is the best combination possible for comparison to derive the trigger signals for the SCRs (Fig. 14.26 [9]), which produces the output waveform with the lowest total harmonic distortion. The modulating voltages can be obtained as the phase-shifted voltages (B-phase for

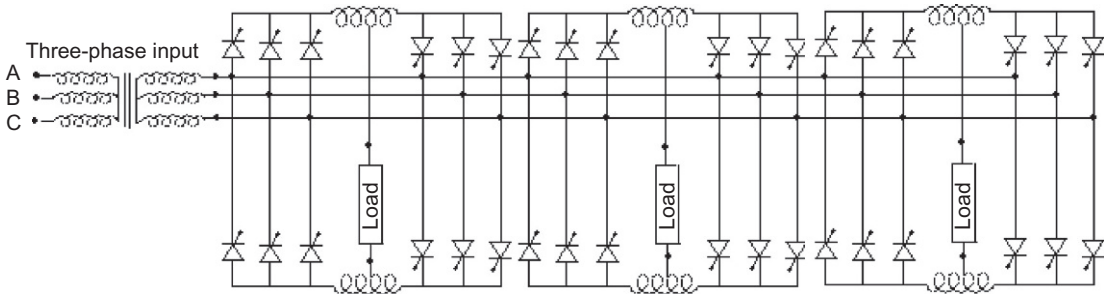


FIG. 14.24 Three-phase six-pulse cycloconverter with isolated loads.

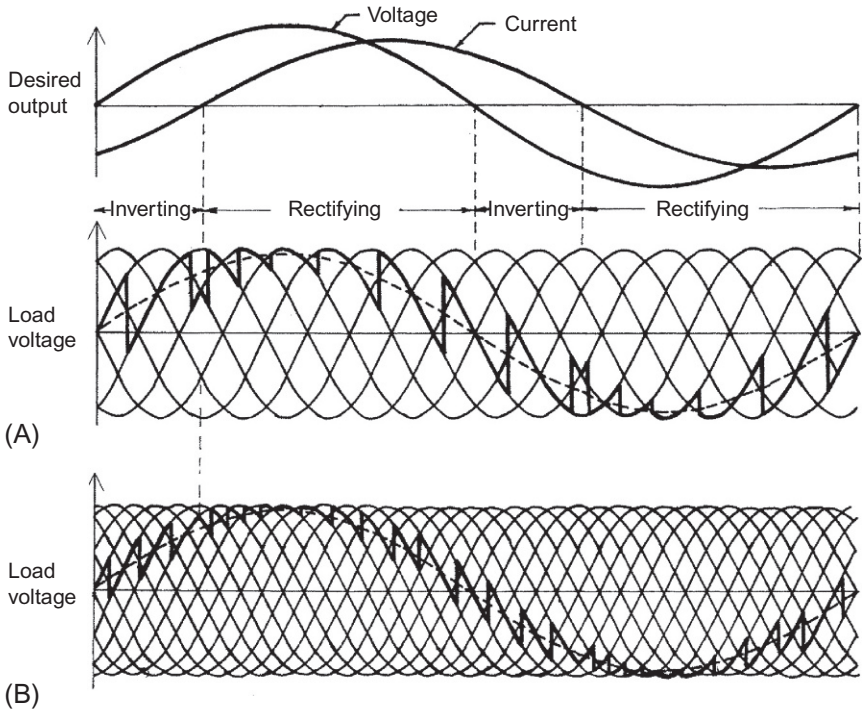


FIG. 14.25 Cycloconverter load voltage waveforms with lagging power factor load: (A) six-pulse connection and (B) twelve-pulse connection.

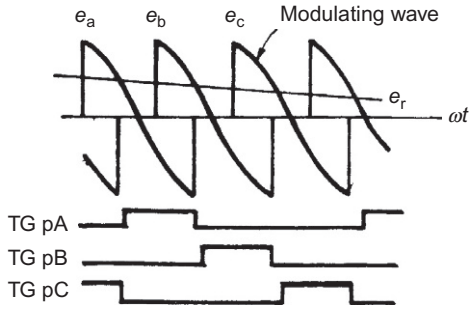


FIG. 14.26 Deriving firing signals for one converter group of a three-pulse cycloconverter.

A-phase SCRs, C-phase voltage for B-phase SCRs, and so on) as explained in Fig. 14.27, where at the intersection point "a"

$$E_m \sin(\omega_i t - 120 \text{ degrees}) = -E_r \sin(\omega_o t - \phi)$$
$$\text{or } \cos(\omega_i t - 30 \text{ degrees}) = (E_r/E_m)\sin(\omega_o t - \phi)$$

From Fig. 14.27, the firing delay for A-phase SCR, $\alpha = (\omega_i t - 30 \text{ degrees})$

$$\text{So, } \cos\alpha = (E_r/E_m)\sin(\omega_o t - \phi)$$

The cycloconverter output voltage for continuous-current operation,

$$V_o = V_{do}\cos\alpha = V_{do}(E_r/E_m)\sin(\omega_o t - \phi) \qquad (14.29)$$

in which the equation shows that the amplitude, frequency, and phase of the output voltage can be controlled by controlling corresponding parameters of the reference voltage, thus making the transfer characteristic of the cycloconverter linear. The derivation of the two complimentary voltage waveforms for the P-group or N-group converter "banks" in this way is illustrated in Fig. 14.28. The final cycloconverter output wave shape is composed of alternate half-cycle segments of the complementary P-converter and the N-converter output voltage waveforms that coincide with the positive and negative current half cycles, respectively.

Control Circuit Block Diagram. Fig. 14.29 [10] shows a simplified block diagram of the control circuit for a circulating current-free cycloconverter implemented with ICs in the early

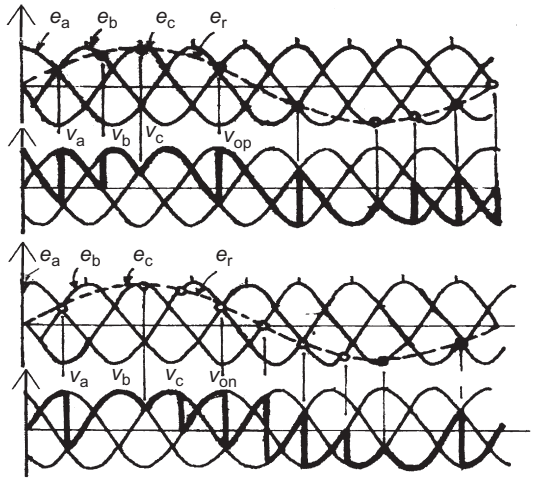


FIG. 14.28 Derivation of P-converter and N-converter output voltages.

seventies in the Power Electronics Laboratory at IIT Kharagpur in India. The same circuit is also applicable to a circulating current cycloconverter with the omission of the *converter group selection and blanking* circuit.

The *synchronizing circuit* produces the modulating voltages ($e_a = -Kv_b$, $e_b = -Kv_c$, $e_c = -Kv_a$), synchronized with the mains through step-down transformers and proper filter circuits.

The *reference source* produces variable-magnitude variable-frequency three-phase voltages (e_{ra}, e_{rb}, e_{rc}) for comparison with the modulation voltages. Various ways, analog or digital, have been developed to implement this reference source as in the case of the PWM inverter. In one of the early analog schemes, Fig. 14.30 [10], for a three-pulse cycloconverter, a variable-frequency UJT relaxation oscillator of frequency $6f_d$ triggers a ring counter to produce a three-phase square-wave output of frequency f_d that is used to modulate a single-phase fixed frequency (f_c) variable amplitude sinusoidal voltage in a three-phase full-wave transistor chopper. The three-phase output contains ($f_c - f_d$), ($f_c + f_d$), ($3f_d + f_c$), etc. frequency components from where the "wanted" frequency component ($f_c - f_d$) is filtered out for each phase using a low-pass filter. For example, with $f_c = 500$ Hz and frequency of the relaxation oscillator

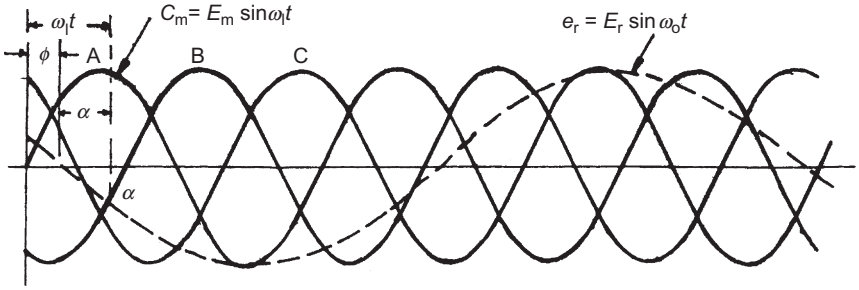


FIG. 14.27 Derivation of the cosine modulating voltages.

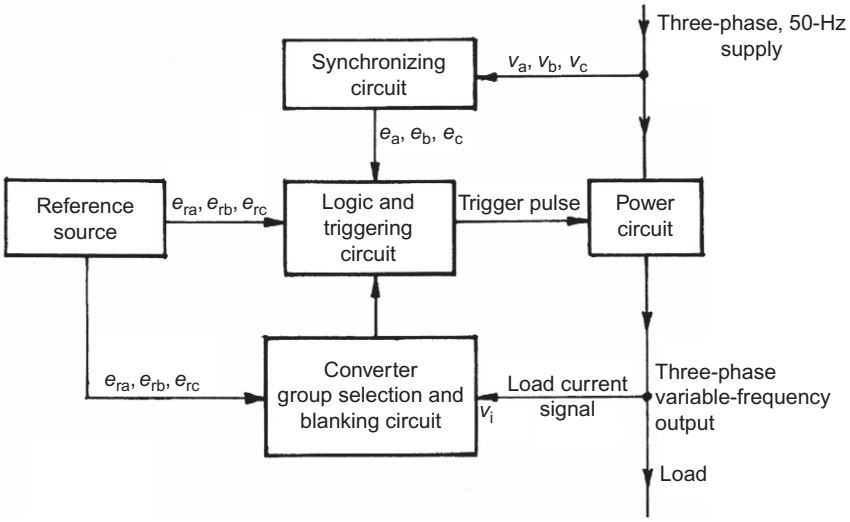


FIG. 14.29 Block diagram for a circulating current-free cycloconverter control circuit.

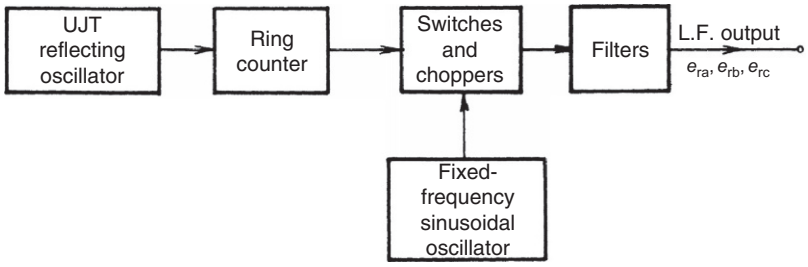


FIG. 14.30 Block diagram of a variable-voltage variable-frequency three-phase reference source.

varying between 2820 and 3180 Hz, a three-phase 0–30 Hz reference output can be obtained with the facility for phase sequence reversal.

The *logic and trigger circuit* for each phase involves comparators for comparison of the reference and modulating voltages and inverters acting as buffer stages. The outputs of the comparators are used to clock the flip-flops or latches whose outputs in turn feed the SCR gates through AND gates and pulse amplifying and isolation circuits; the second input to the AND gates is from the *converter group selection and blanking circuit*.

In the *converter group selection and blanking circuit*, the zero crossing of the current at the end of each half cycle is detected and is used to regulate the control signals to either P-group or N-group converters depending on whether the current goes to zero from negative to positive or positive to negative, respectively. However, in practice, the current being discontinuous passes through multiple zero crossings while changing direction, which may lead to undesirable switching of the converters. So, in addition to the current signal, the reference voltage signal is also used for the group selection, and a *threshold* band is introduced in the current signal detection to avoid inadvertent switching of the converters. Further, a delay circuit provides a blanking period of appropriate duration between the converter groups switching to avoid line-to-line short circuits [10]. In some schemes, the delays are not introduced when a small circulating current is allowed during crossover instants limited by reactors of limited size, and this scheme operates in the so-called "dual mode"—circulating current and circulating current-free mode for minor and major portions of the output cycle, respectively. A different approach to the converter group selection, based on the closed-loop control of the output voltage where a bias voltage is introduced between the voltage transfer characteristics of the converters to reduce circulating current, is discussed in [8].

Improved Control Schemes. With the development of microprocessors and PC-based systems, digital software control has taken over many tasks in modern cycloconverters, particularly in replacing the low-level reference waveform generation and analog signal comparison units. The reference waveforms can be easily generated in the computer, stored in the EPROMs, and accessed under the control of a stored program and microprocessor clock oscillator. The analog signal voltages can be converted to digital signals by using analog-to-digital converters (ADCs). The waveform comparison can then be made with the comparison features of the microprocessor system.

The addition of time delays and intergroup blanking can also be achieved with digital techniques and computer software. A modification of the cosine firing control using communication principles, such as *regular sampling* in preference to the *natural sampling* (discussed so far) of the reference waveform, yielding a stepped sine wave before comparison with the cosine wave [11] has been shown to reduce the presence of *subharmonics* (discussed later) in the circulating current cycloconverter and facilitate microprocessor-based implementation, as in the case of PWM inverter.

For a six-pulse noncirculating current cycloconverter-fed synchronous motor drive with a vector control scheme and a flux observer, a PC-based hybrid control scheme (a combination of analog and digital control) has been reported in [12]. Here, the functions such as comparison, group selection, blanking between the groups and triggering signal generation, and filtering and phase conversion are left to the analog controller and digital controller that take care of more serious tasks such as voltage decoupling for current regulation; flux estimation using observer; speed, flux and field current regulators using PI-controllers; and position and speed calculation leading to an improvement of sampling time and design accuracy.

14.4.4 Cycloconverter Harmonics and Input Current Waveform

The exact wave shape of the output voltage of the cycloconverter depends on (1) the pulse number of the converter, (2) the ratio of the output to input frequency (f_o/f_i), (3) the relative level of the output voltage, (4) the load displacement angle, (5) the circulating current or circulating current-free operation, and (6) the method of control of the firing instants. The harmonic spectrum of a cycloconverter output voltage is different and more complex than that of a phase-controlled converter. It has been revealed [8] that because of the continuous "to-and-fro" phase modulation of the converter firing angles, the harmonic distortion components (known as *necessary distortion terms*) have frequencies that are sums and differences between multiples of output and input supply frequencies.

Circulating Current-Free Operation. A derived general expression for the output voltage of a cycloconverter with circulating current-free operation [8] shows the following spectrum of harmonic frequencies for the 3-pulse, 6-pulse, and 12-pulse cycloconverters employing cosine modulation technique:

$$\begin{aligned} 3-\text{pulse}: f_{oH} &= |3(2k-1)f_i \pm 2nf_o| \quad \text{and} \quad |6kf_i \pm (2n+1)f_o| \\ 6-\text{pulse}: f_{oH} &= |6kf_i \pm (2n+1)f_o| \\ 12-\text{pulse}: f_{oH} &= |6kf_i \pm (2n+1)f_o| \end{aligned} \tag{14.30}$$

where k is any integer from 1 to infinity and n is any integer from 0 to infinity.

It may be observed that for certain ratios of f_o/f_i, the order of harmonics may be less or equal to the desired output frequency. All such harmonics are known as *subharmonics*, since they are not higher multiples of the input frequency. These subharmonics may have considerable amplitudes (e.g., with a 50 Hz input frequency and 35 Hz output frequency, a subharmonic of frequency $3 \times 50 - 4 \times 35 = 10$ Hz is produced whose magnitude is 12.5% of the 35 Hz component [11]) and are difficult to filter and so objectionable. Their spectrum increase with the increase of the ratio f_o/f_i and so limits its value at which a tolerable waveform can be generated.

Circulating-Current Operation. For circulating current operation with continuous current, the harmonic spectrum in the output voltage is the same as that of the circulating current-free operation except that each harmonic family now terminates at a definite term, rather than having infinite number of components. They are

$$\begin{aligned} 3-\text{pulse}: f_{oH} &= |3(2k-1)f_i \pm 2nf_o|, \quad n \le 3(2k-1)+1 \\ &\text{and} \quad |6kf_i \pm (2n+1)f_o|, \quad (2n+1) \le (6k+1) \\ 6-\text{pulse}: f_{oH} &= |6kf_i \pm (2n+1)f_o|, \quad (2n+1) \le (6k+1) \\ 12-\text{pulse}: f_{oH} &= |6kf_i \pm (2n+1)f_o|, \quad (2n+1) \le (12k+1) \end{aligned} \tag{14.31}$$

The amplitude of each harmonic component is a function of the output voltage ratio for the circulating current cycloconverter and the output voltage ratio and the load displacement angle for the circulating current-free mode.

From the point of view of maximum useful attainable output-to-input frequency ratio (f_i/f_o) with the minimum amplitude of objectionable harmonic components, a guideline is available in [8] for it as 0.33, 0.5, and 0.75 for 3-, 6-, and 12-pulse cycloconverter, respectively. However, with the modification of the cosine-wave modulation timings like *regular sampling* [11] in the case of circulating current cycloconverters only and using a *subharmonic detection and feedback control concept* [13,14] for both circulating and circulating current-free cases, the subharmonics can be suppressed, and useful frequency range for the naturally commutated cycloconverters can be increased.

Other Harmonic Distortion Terms. Besides the harmonics as mentioned, other harmonic distortion terms consisting of frequencies of integral multiples of desired output frequency appear if the transfer characteristic between the output and reference voltages is not linear. These are called *unnecessary distortion terms* that are absent when the output frequencies are much less than the input frequency. Further, some *practical distortion terms* may appear due to some practical nonlinearities and imperfections in the control circuits of the cycloconverter, particularly at relatively lower levels of output voltage.

Input Current Waveform. Although the load current, particularly for higher pulse cycloconverters can be assumed to be sinusoidal, the input current is more complex being made of

pulses. Assuming the cycloconverter to be an ideal switching circuit without losses, it can be shown from the instantaneous power balance equation that in cycloconverter supplying a single-phase load, the input current has harmonic components of frequencies ($f_1 \pm 2f_o$) called *characteristic harmonic frequencies* that are independent of pulse number, and they result in an oscillatory power transmittal to the ac supply system. In the case of cycloconverter feeding a balanced three-phase load, the net instantaneous power is the sum of the three oscillating instantaneous powers when the resultant power is constant, and the net harmonic component is much reduced compared with that of a single-phase load case. In general, the total rms value of the input current waveform consists of three components: in-phase, quadrature, and the harmonic. The in-phase component depends on the active power output, while the quadrature component depends on the net average of the oscillatory firing angle and is always lagging.

14.4.5 Cycloconverter Input Displacement/ Power Factor

The input supply performance of a cycloconverter such as displacement factor or fundamental power factor, input power factor, and the input current distortion factor is defined similar to those of the phase-controlled converter. The harmonic factor for the case of a cycloconverter is relatively complex as the harmonic frequencies are not simple multiples of the input frequency but are sums and differences between multiples of output and input frequencies.

Irrespective of the nature of the load, leading, lagging, or unity power factor, the cycloconverter requires reactive power decided by the average firing angle. At low-output voltage, the average phase displacement between the input current and the voltage is large, and the cycloconverter has a low input displacement and power factor. Besides load displacement factor and output voltage ratio, another component of the reactive current arises due to the modulation of the firing angle in the fabrication process of the output voltage [8]. In a phase-controlled converter supplying dc load, the maximum displacement factor is unity for maximum dc output voltage. However, in the case of the cycloconverter, the maximum input displacement factor is 0.843 with unity power factor load [8,15]. The displacement factor decreases with reduction in the output voltage ratio. The distortion factor of the input current is given by (I_1/I), which is always less than 1, and the resultant power factor (= distortion factor × displacement factor) is thus much lower (around 0.76 maximum) than the displacement factor, and this is a serious disadvantage of the naturally commutated cycloconverter (NCC).

14.4.6 Effect of Source Impedance

The source inductance introduces commutation overlap and affects the external characteristics of a cycloconverter similar to the case of a phase-controlled converter with the dc output. It introduces delay in transfer of current from one SCR to another and results in a voltage loss at the output and a modified harmonic distortion. At the input, the source impedance causes "rounding off" of the steep edges of the input current waveforms, resulting in reduction in the amplitudes of higher order harmonic terms and a decrease in the input displacement factor.

14.4.7 Simulation Analysis of Cycloconverter Performance

The nonlinearity and discrete time nature of practical cycloconverter systems, particularly for discontinuous-current conditions, make an exact analysis quite complex, and a valuable design and analytic tool is a digital computer simulation of the system. Two general methods of computer simulation of the cycloconverter waveforms for RL and induction motor loads with circulating current and circulating current-free operation have been suggested in [16] where one of the methods that is very fast and convenient is the *crossover point method* that gives the crossover points (intersections of the modulating and reference waveforms) and the conducting phase numbers for both P- and N-converters from which the output waveforms for a particular load can be digitally computed at any interval of time for a practical cycloconverter.

14.4.8 Power Quality Issues

Degradation of power quality (PQ) in a cycloconverter-fed system due to subharmonics/interharmonics in the input and the output has been a subject of recent studies [14,17]. In [17], the study includes the impact of cycloconverter control strategies on the total harmonic distortion (THD), distribution transformers, and communication lines, while in [14], the PQ indices are suitably defined and the effect on THD, input/output displacement factor, and input/output power factor for a cycloconverter-fed synchronous motor drive is studied together with a development of a simple feedback method of reduction of subharmonics/low-frequency interharmonics for the improvement of the power quality. The implementation of this scheme, detailed in [14], requires a simple modification of the control circuit of the cycloconverter in contrast to the expensive power level active filters otherwise required for suppression of such harmonics [18].

14.4.9 Forced Commutated Cycloconverter

The naturally commutated cycloconverter (NCC) with SCRs as devices, so far discussed, is sometimes referred to as a *restricted frequency changer*; in view of the allowance on the output voltage quality ratings, the maximum output voltage frequency is restricted ($f_o \ll f_i$), as mentioned earlier. With devices replaced

by fully controlled switches like forced commutated SCRs, power transistors, IGBTs, and GTOs, a forced commutated cycloconverter can be built where the desired output frequency is given by $f_o = |f_s - f_i|$, where f_s is the switching frequency, which may be larger or smaller than the f_i. In the case when $f_o \geq f_i$, the converter is called *unrestricted frequency changer* (*UFC*) and when $f_o \leq f_i$, it is called a *slow switching frequency changer* (*SSFC*). The early FCC structures have been comprehensively treated in [15]. It has been shown that in contrast with the NCC, where the input displacement factor (IDF) is always lagging, in UFC, it is leading when the load displacement factor is lagging and vice versa, and in SSFC, it is identical to that of the load. Further, with proper control in an FCC, the input displacement factor can be made unity displacement factor frequency changer (UDFFC) with concurrent composite voltage waveform or controllable displacement factor frequency changer (CDFFC), where P-converter and N-converter voltage segments can be shifted relative to the output current wave for control of IDF continuously from lagging via unity to leading.

In addition to allowing bilateral power flow, UFCs offer an unlimited output frequency range, offer good input voltage utilization, do not generate input current and output voltage subharmonics, and require only nine bidirectional switches (Fig. 14.31) for a three-phase to three-phase conversion. The main disadvantage of the structures treated in [15] is that they generate large unwanted low-order input current and output voltage harmonics that are difficult to filter out, particularly for low-output voltage conditions. This problem has largely been solved with an introduction of an imaginative PWM voltage control scheme in [19], which is the basis of the newly designated converter called the *matrix converter* (*also known as PWM cycloconverter*) that operates as a *generalized solid-state transformer* with significant improvement in voltage and input current waveforms resulting in sine-wave input and sine-wave output as discussed in the next section.

14.5 Matrix Converter

The matrix converter (MC) is a development of the FCC that employs bidirectional fully controlled switches, incorporating PWM voltage control, as mentioned earlier. With the initial

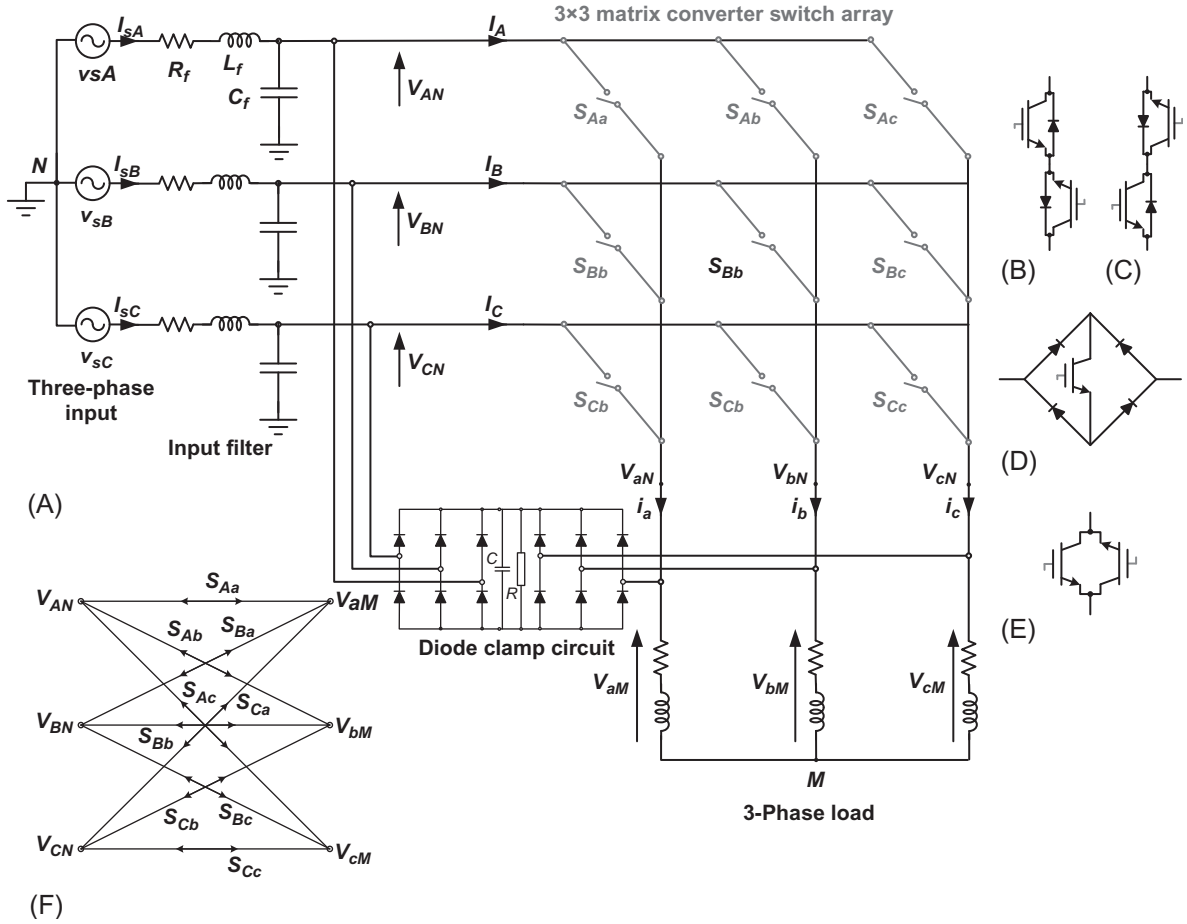


FIG. 14.31 (A) $3\varphi \times 3\varphi$ matrix converter circuit with input filter and clamp circuit; bidirectional switch configuration as (B) common emitter, (C) common collector, (D) transistor-diode bridge configuration, and (E) reverse blocking IGBT (RB-IGBT); and (F) switching matrix symbol for converter in (A).

progress made by Venturini [19–21], it has received considerable attention in recent years as it provides a good alternative to the conventionally employed rectifier-inverter topology or the back-to-back topology, having the advantages of being a single-stage converter with only nine switches for three-phase to three-phase conversion and inherent bidirectional power flow, sinusoidal input/output waveforms with moderate switching frequency, possibility of a compact design due to the absence of bulky dc link reactive components, and controllable input power factor independent of the output load current. Along with these theoretical advantages, [22] has mentioned advantages of MCs over conventional dc link variant as exhibition of better operation under high-temperature conditions, less voltage stress per switch, and less maintenance. The main disadvantages of the matrix converters developed so far are the inherent restriction of the *voltage transfer ratio* (0.866); more complex control, commutation, and protection strategy; and, above all, commercial nonavailability of a fully controlled bidirectional high frequency switch integrated in a silicon chip.

The power circuit diagram of the most practical three-phase to three-phase ($3\phi - 3\phi$) matrix converter is shown in Fig. 14.31A, which uses nine bidirectional switches so arranged that any of the three-input phases can be connected to any output phase as is shown symbolically in the switching matrix in Fig. 14.31F. The circuit is called a *matrix converter* as it provides exactly one switch for each of the possible connections between the input and the output. The voltage at any input terminal may be made to appear at any output terminal or terminals, while the current in any phase of the load may be drawn from any phase or phases of the input supply under following restrictions:

(a) *Only one* switch of the output leg can be closed due to the presence of capacitors.
(b) *At least one* switch in the output leg must be closed, as the inductive nature of the load makes it impossible to interrupt the load current suddenly.

Thus, *one and only one switch* in the output leg is to be closed. With these constraints, it can be visualized that out of the possible 512 $(=2^9)$ states of the converter, only 27 switch combinations are allowed as given in Table 14.1, which includes the resulting output line voltages and input phase currents. These combinations are divided into three groups. Group I consists of six combinations when each output phase is connected to a different input phase. In group II, there are three subgroups each having six combinations with two-output phases short-circuited (connected to the same input phase). Group III includes three combinations with all output phases short-circuited. For the switches, the inverse-parallel combination of reverse blocking self-controlled devices like power MOSFETs or IGBTs or transistor-embedded diode bridge as shown in Fig 14.3B–E has been used so far. Fig. 14.31B

TABLE 14.1 Three-phase/three-phase matrix converter switching combinations

Group	a	b	c	v_{ab}	v_{bc}	v_{ca}	i_A	i_B	i_C	S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}
I	A	B	C	v_{AB}	v_{BC}	v_{CA}	i_a	i_b	i_c	1	0	0	0	1	0	0	0	1
	A	C	B	$-v_{CA}$	$-v_{BC}$	$-v_{AB}$	i_a	i_c	i_b	1	0	0	0	0	1	0	1	0
	B	A	C	$-v_{AB}$	$-v_{CA}$	$-v_{BC}$	i_b	i_a	i_c	0	1	0	1	0	0	0	0	1
	B	C	A	v_{BC}	v_{CA}	v_{AB}	i_c	i_a	i_b	0	1	0	0	0	1	0	1	0
	C	A	B	v_{CA}	v_{AB}	v_{BC}	i_b	i_c	i_a	0	0	1	1	0	0	0	1	0
	C	B	A	$-v_{BC}$	$-v_{AB}$	$-v_{CA}$	i_c	i_b	i_a	0	0	1	0	1	0	1	0	0
II-A	A	C	C	$-v_{CA}$	0	v_{CA}	i_a	0	$-i_a$	1	0	0	0	0	1	0	0	1
	B	C	C	v_{BC}	0	$-v_{BC}$	0	i_a	$-i_a$	0	1	0	0	0	1	0	0	1
	B	A	A	$-v_{AB}$	0	$-v_{AB}$	$-i_a$	i_a	0	0	1	0	1	0	0	1	0	0
	C	A	A	v_{CA}	0	$-v_{CA}$	$-i_a$	0	i_a	0	0	1	1	0	0	1	0	0
	C	B	B	$-v_{BC}$	0	v_{BC}	0	$-i_a$	i_a	0	0	1	0	1	0	0	1	0
	A	B	B	v_{AB}	0	$-v_{AB}$	i_a	$-i_a$	0	1	0	0	0	1	0	0	1	0
II-B	C	A	C	$-v_{CA}$	$-v_{CA}$	0	i_b	0	$-i_b$	0	0	1	1	0	0	0	0	1
	C	B	C	$-v_{BC}$	v_{BC}	0	0	i_b	$-i_b$	0	0	1	0	1	0	0	0	1
	A	B	A	v_{AB}	$-v_{AB}$	0	$-i_b$	i_b	0	1	0	0	0	1	0	1	0	0
	A	C	A	$-v_{CA}$	v_{CA}	0	$-i_b$	0	i_b	1	0	0	0	0	1	1	0	0
	B	C	B	v_{BC}	$-v_{BC}$	0	0	$-i_b$	i_b	0	1	0	0	0	1	0	1	0
	B	A	B	$-v_{AB}$	v_{AB}	0	i_b	$-i_b$	0	0	1	0	1	0	0	0	1	0
II-C	C	C	A	0	v_{CA}	$-v_{CA}$	i_c	0	$-i_c$	0	0	1	0	0	1	1	0	0
	C	C	B	0	$-v_{BC}$	v_{BC}	0	i_c	$-i_c$	0	0	1	0	0	1	0	1	0
	A	A	B	0	v_{AB}	$-v_{AB}$	$-i_c$	i_c	0	1	0	0	1	0	0	0	1	0
	A	A	C	0	$-v_{CA}$	v_{CA}	$-i_c$	0	i_c	1	0	0	1	0	0	0	0	1
	B	B	C	0	v_{BC}	$-v_{BC}$	0	$-i_c$	i_c	0	1	0	0	1	0	0	0	1
	B	B	A	0	$-v_{AB}$	v_{AB}	i_c	$-i_c$	0	0	1	0	0	1	0	1	0	0
III	A	A	A	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0
	B	B	B	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0
	C	C	C	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

and C are the conventionally employed common emitter and common collector configurations, respectively. These configurations allow *soft switching* from one bidirectional switch to other. The latter has an advantage that it requires less number of insulated power supplies to drive the switches than the former configuration [23]. New perspective configuration of the bidirectional switch is to use two RB-IGBTs with reverse blocking capability in antiparallel (symbol of which is shown in Fig 14.31E). This configuration leads to elimination of external diodes, which results in reduction in conduction losses and the transistor size [24].

With a given set of input three-phase voltages, any desired set of three-phase output voltages can be synthesized by adopting a suitable switching strategy. However, it has been shown [21,25,26] that regardless of the switching strategy, there are physical limits on the achievable output voltage with these converters as the maximum peak-to-peak output voltage cannot be greater than the minimum voltage difference between two phases of the input. To have complete control of the synthesized output voltage, the envelope of the three-phase reference or target voltages must be fully contained within the continuous envelope of the three-phase input voltages. Initial strategy with the output frequency voltages as references reported the limit as 0.5 of the input as shown in Fig. 14.32A. This can be increased to 0.866 by adding a third harmonic voltage of input frequency $(V_i/4)\cos 3\omega_i t$ to all target output voltages and subtracting from them a third harmonic voltage of output frequency $(V_o/6)\cos 3\omega_o t$ as shown in Fig. 14.32B [21,25]. The increase in amplitude is shown through line voltages (v_{ab}) in Fig. 14.32C. In fact, it is shown in [26] that the above optimization can be extended to m × n matrix converter (where m and n are both odd) by adding mth and subtracting the nth harmonic from all the target output voltages. Details on multiphase matrix converters are given in Chapter 16. However, this process involves considerable amount of additional computations in synthesizing the output voltages. The other alternative is to use the space vector modulation (SVM) strategy as used in PWM inverters without adding third harmonic components, but it also yields the maximum voltage transfer ratio as 0.866.

An ac input LC filter is used to eliminate the switching ripples generated in the converter, and the load is assumed to be sufficiently inductive to maintain continuity of the output currents. Work on input side filters can be seen in [27–29].

14.5.1 Operation and Control of Matrix Converter

The converter in Fig. 14.31 connects any input phase (A, B, and C) to any output phase (a, b, and c) at any instant. When connected, the voltages v_{an}, v_{bn}, and v_{cn} at the output terminals are related to the input voltages V_{Ao}, V_{Bo}, and V_{Co} as

$$\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} = \begin{bmatrix} S_{Aa} & S_{Ba} & S_{Ca} \\ S_{Ab} & S_{Bb} & S_{Cb} \\ S_{Ac} & S_{Bc} & S_{Cc} \end{bmatrix} \begin{bmatrix} v_{Ao} \\ v_{Bo} \\ v_{Co} \end{bmatrix} \tag{14.32}$$

where S_{Aa} through S_{Cc} are the switching variables of the corresponding switches shown in Fig. 14.31. For a balanced linear star-connected load at the output terminals, the input phase currents are related to the output phase currents by

$$\begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = \begin{bmatrix} S_{Aa} & S_{Ab} & S_{Ac} \\ S_{Ba} & S_{Bb} & S_{Bc} \\ S_{Ca} & S_{Cb} & S_{Cc} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{14.33}$$

Note that the matrix of the switching variables in Eq. (14.33) is a transpose of the respective matrix in Eq. (14.32). The matrix converter should be controlled using a specific and appropriately timed sequence of the values of the switching variables, which will result in balanced output voltages having the desired frequency and amplitude, while the input currents are balanced and in phase (for unity IDF) or at an arbitrary angle (for controllable IDF) with respect to the input voltages. As the matrix converter, in theory, can operate at any frequency and at the output or input, including zero, it can be employed as a three-phase ac-dc converter, dc/three-phase ac converter, or even a buck/boost dc chopper and thus as a *universal power converter*.

The control methods adopted so far for the matrix converter are quite complex and are subjects of continuing research [21–39]. Out of several methods proposed for independent control of the output voltages and input currents, two methods are of wide use and will be briefly reviewed here: (1) the *Venturini* method based on a mathematical approach of transfer function analysis and (2) the *space vector modulation* (SVM) approach (as has been standardized now in the case of PWM control of the dc link inverter).

Venturini Method. Given a set of three-phase input voltages with constant amplitude V_i and frequency $f_i = \omega_i/2\pi$, this method calculates a switching function involving the duty cycles of each of the nine bidirectional switches and generates the three-phase output voltages by sequential piecewise sampling of the input waveforms. These output voltages follow a predetermined set of reference or target voltage waveforms and with a three-phase load connected, a set of input currents I_i and angular frequency ω_i should be in phase for unity IDF or at a specific angle for controlled IDF.

A transfer function approach is used in [36] to achieve the abovementioned features by relating the input and output voltages and the output and input currents as

$$\begin{bmatrix} V_{o1}(t) \\ V_{o2}(t) \\ V_{o3}(t) \end{bmatrix} = \begin{bmatrix} m_{11}(t) & m_{12}(t) & m_{13}(t) \\ m_{21}(t) & m_{22}(t) & m_{23}(t) \\ m_{31}(t) & m_{32}(t) & m_{33}(t) \end{bmatrix} \begin{bmatrix} V_{i1}(t) \\ V_{i2}(t) \\ V_{i3}(t) \end{bmatrix} \tag{14.34}$$

$$\begin{bmatrix} I_{i1}(t) \\ I_{i2}(t) \\ I_{i3}(t) \end{bmatrix} = \begin{bmatrix} m_{11}(t) & m_{21}(t) & m_{31}(t) \\ m_{12}(t) & m_{22}(t) & m_{32}(t) \\ m_{13}(t) & m_{23}(t) & m_{33}(t) \end{bmatrix} \begin{bmatrix} I_{o1}(t) \\ I_{o2}(t) \\ I_{o3}(t) \end{bmatrix} \tag{14.35}$$

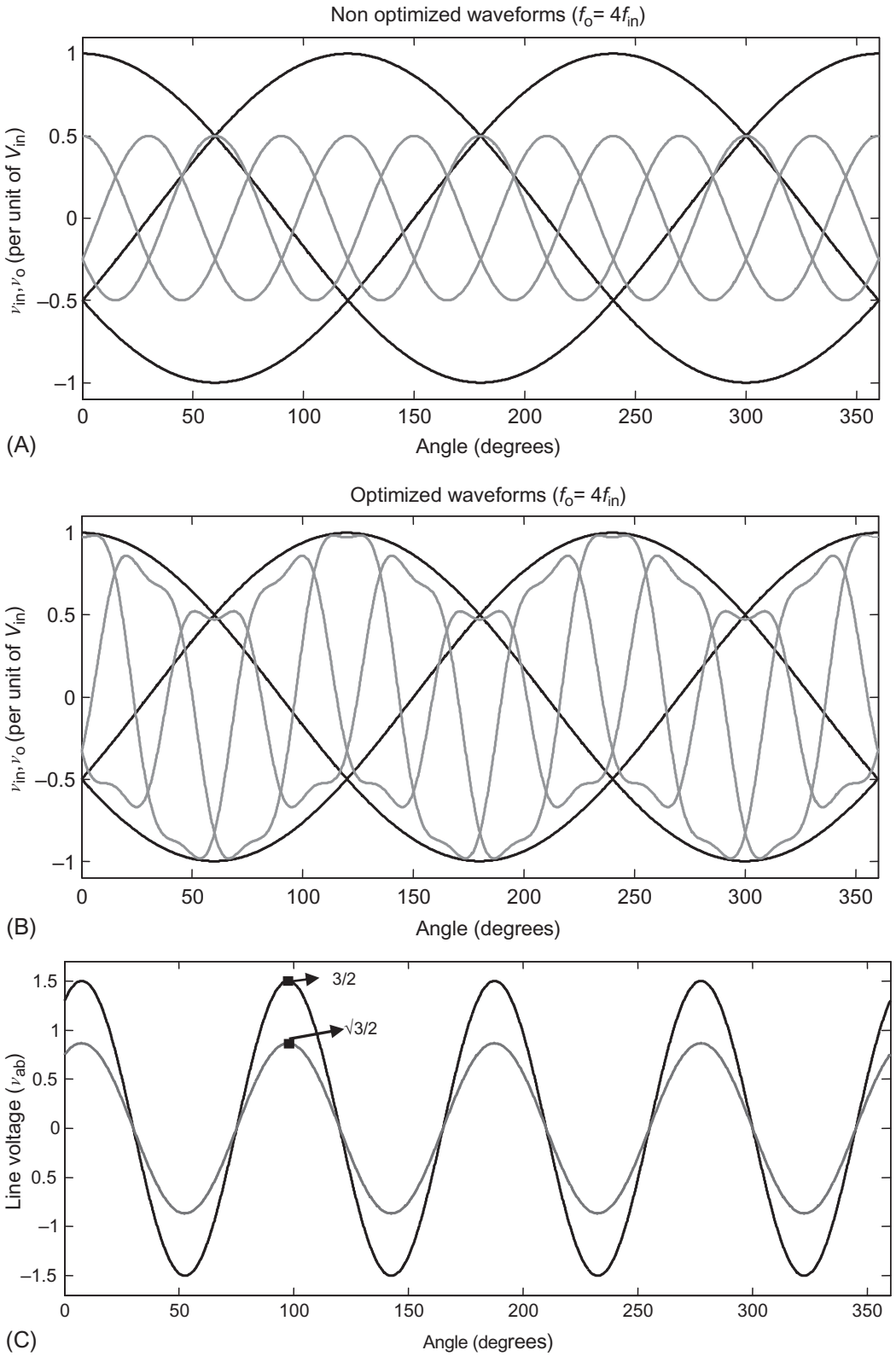


FIG. 14.32 Output phase voltage waveforms for three-phase ac-ac matrix converter: (A) without the addition of harmonics, (B) with inclusion of third harmonic voltages of input and output frequency to the target voltages, and (C) output line voltages (v_{ab}) of (A) and (B).

where the elements of the modulation matrix, $m_{ij}(t)$, $(i,j=1,2,3)$ represent the duty cycles of a switch connecting output phase i to input phase j within a sample switching interval. The elements of $m_{ij}(t)$ are limited by the constraints discussed above and are mathematically written as

$$0 \le m_{ij}(t) \le 1 \quad \text{and} \quad \sum_{j=1}^{3} m_{ij}(t) = 1 \quad (i=1,2,3)$$

The set of three-phase target or reference voltages to achieve the maximum voltage transfer ratio for unity IDF is

$$\begin{bmatrix} v_{o1} \\ v_{o2} \\ v_{o3} \end{bmatrix} = V_{om} \begin{bmatrix} \cos\omega_o t \\ \cos(\omega_o t - 120) \\ \cos(\omega_o t - 240) \end{bmatrix} + \frac{V_{im}}{4} \begin{bmatrix} \cos(3\omega_i t) \\ \cos(3\omega_i t) \\ \cos(3\omega_i t) \end{bmatrix} - \frac{V_{om}}{6} \begin{bmatrix} \cos(3\omega_o t) \\ \cos(3\omega_o t) \\ \cos(3\omega_o t) \end{bmatrix} \tag{14.36}$$

where V_{om} and V_{im} are the magnitudes of output and input fundamental voltages of angular frequencies ω_{o} and ω_{i}, respectively. With $V_{\text{om}} \le 0.866\, V_{\text{im}}$, a general formula for the duty cycles $m_{ij}(t)$ is derived in [36]. For unity IDF condition, a simplified formula is

$$\begin{aligned} m_{ij} = \frac{1}{3}\{1 + 2q\cos(\omega_1 t - 2(j-1)60\,\text{degrees}) \\ \times\left[\cos(\omega_{\text{o}} t - 2(i-1)60\,\text{degrees}) + \frac{1}{2\sqrt{3}}\cos(3\omega_{\text{i}} t) - \frac{1}{6}\cos(3\omega_{\text{o}} t)\right] \\ - \frac{2q}{3\sqrt{3}}[\cos(4\omega_{\text{i}} t - 2(j-1)60\,\text{degrees}) \\ - \cos(2\omega_{\text{i}} t - 2(1-j)60\,\text{degrees})]\} \end{aligned} \tag{14.37}$$

where $i,j=1,2,3$ and $q = V_{\text{om}}/V_{\text{im}}$.

The method developed as above is based on a *direct transfer function* (*DTF*) approach using a single modulation matrix for the matrix converter, employing the switching combinations of all the three groups in Table 14.1. Another approach called *indirect transfer function* (*ITF*) approach [30,31] considers the matrix converter as a combination of PWM voltage source rectifier-PWM voltage source inverter (VSR-VSI) and employs the already well-established VSR and VSI PWM techniques for MC control utilizing the switching combinations of group II and group III only of Table 14.1. The drawback of this approach is that the IDF is limited to unity, and the method also generates higher and fractional harmonic components in the input and the output waveforms. This method can also be found in [40].

A **simplified direct transfer function approach** at unity IDF can be developed. Eq. (14.34) and the constraint equations can be rewritten as follows:

$$\underbrace{\begin{bmatrix} v_{o1} \\ v_{o1} \\ v_{o1} \\ 1 \\ 1 \\ 1 \end{bmatrix}}_{Y_{6\times1}} = \underbrace{\begin{bmatrix} v_{in1} & v_{in1} & v_{in1} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & v_{in1} & v_{in1} & v_{in1} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & v_{in1} & v_{in1} & v_{in1} \\ 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 \end{bmatrix}}_{A_{6\times9}} \underbrace{\begin{bmatrix} m_{11} \\ m_{12} \\ m_{13} \\ m_{21} \\ m_{22} \\ m_{23} \\ m_{31} \\ m_{32} \\ m_{33} \end{bmatrix}}_{X_{9\times1}} \tag{14.38}$$

X is the modulation vector, and the elements can be derived as

$$X = A^{\text{T}}\left(AA^{\text{T}}\right)^{-1} Y \tag{14.39}$$

AA^{T} when solved will have terms $\sum_{i=1}^{3} v_{\text{in}_i}^2$ and $\sum_{i=1}^{3} v_{\text{in}_i}$, so, let $\sum_{i=1}^{3} v_{\text{in}_i}^2 = L$ and $\sum_{i=1}^{3} v_{\text{in}_i} = M$. Each term of X, when (14.39) is solved, is of similar pattern and can be shown as

$$m_{ji} = \frac{1}{(3L - M^2)}\left[v_{\text{o}_j}(3v_{\text{in}_i} - M) - Mv_{\text{in}_i} + L\right] \tag{14.40}$$

where M_{ji} is the time-based index corresponding to the switch S_{ji} that connects j-th output to the i-th input. The time duration for which this switch is on, is calculated by multiplying this index with sampling time. Further solving by considering m balanced input phases, and finally neglecting the terms with denominators with high value, solution for $m \times n$ matrix converter is written as

$$m_{ji} = \frac{1}{3}\left(1 + \frac{2v_{\text{in}_i} v_{\text{o}_j}}{V_{\text{in}}^2}\right) \tag{14.41}$$

A detailed simulation with this modulation scheme can be seen in [41].

SVM Method. The space vector modulation is a well-documented inverter PWM control technique that yields high-voltage gain and less harmonic distortion compared with the other modulation techniques. Here, the three-phase input currents and output voltages are represented as space vectors, and SVM is simultaneously applied to the output voltage and input current space vectors, while the matrix converter is modeled as a rectifying and inverting stage by the *indirect modulation method* (Fig. 14.33). Applications of SVM algorithm to control of matrix converters have appeared extensively in the literature [33–38,42–47] and shown to have inherent capability to achieve full control of the instantaneous output voltage vector and the instantaneous current displacement angle even under supply voltage disturbances. The algorithm is based on the concept that the MC output line voltages for each switching combination can be represented as a voltage space vector defined by

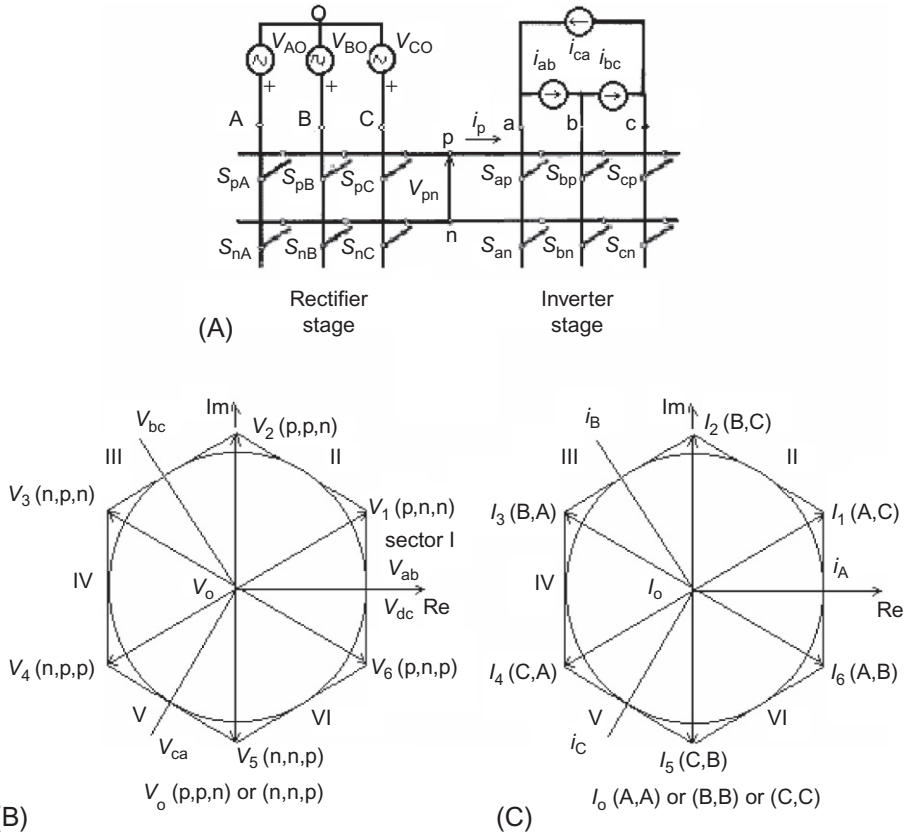


FIG. 14.33 Indirect modulation model of a matrix converter: (A) VSR-VSI conversion, (B) output voltage switching vector hexagon, and (C) input current switching vector hexagon.

$$v_o = \frac{2}{3}[v_{ab} + v_{bc}\exp(j120\,\text{degrees}) + v_{ca}\exp(-j120\,\text{degrees})] \tag{14.42}$$

Out of the three groups in Table 14.1, only the switching combinations of group II and group III are employed for the SVM method. Group II consists of switching state voltage vectors having constant angular positions and are called *active* or *stationary* vectors. Each subgroup of group II determines the position of the resulting output voltage space vector and the six-state space voltage vectors form a six-sextant hexagon used to synthesize the desired output voltage vector. Group III comprises the *zero* vectors positioned at the center of the output voltage hexagon, and these are suitably combined with the active vectors for the output voltage synthesis.

The modulation method involves selection of the vectors and their on-time computation. At each sampling period T_s, the algorithm selects four active vectors related to any possible combinations of output voltage and input current sectors in addition to the zero vector to construct a desired reference voltage. The amplitude and the phase angle of the reference voltage vector are calculated, and the desired phase angle of the input current vector is determined in advance. For computation of the on-time periods of the chosen vectors, these are combined into two sets leading to two new vectors adjacent to the reference voltage vector in the sextant and having the same direction as the reference voltage vector. Applying the standard SVM theory, the general formulas derived for the vector on-times that satisfy, at the same time, the reference output voltage and input current displacement angle in [36] are

$$t_1 = \frac{2qT_s}{\sqrt{3}\cos\phi_i}\sin(60\,\text{degrees} - \theta_o)\cdot\sin(60\,\text{degrees} - \theta_i)$$

$$t_2 = \frac{2qT_s}{\sqrt{3}\cos\phi_i}\sin(60\,\text{degrees} - \theta_o)\cdot\sin\theta_i$$

$$t_3 = \frac{2qT_s}{\sqrt{3}\cos\phi_i}\sin\theta_o\cdot\sin(60\,\text{degrees} - \theta_i)$$

$$t_4 = \frac{2qT_s}{\sqrt{3}\cos\phi_i}\sin\theta_o\cdot\sin\theta_i \tag{14.43}$$

where q is voltage transfer ratio, ϕ_i is the input displacement angle chosen to achieve the desired input power factor (with $\phi_i = 0$, a maximum value of $q = 0.866$ is obtained), and θ_o and θ_i are the phase displacement angles of the output voltage and input current vectors, respectively, whose values are limited within the 0–60 degrees range. The on-time of the zero vector is

$$t_o = T_s - \sum_{i=1}^{4} t_i \tag{14.44}$$

The integral value of the reference vector is calculated over one sample time interval as the sum of the products of the two adjacent vectors and their on-time ratios, and the process is repeated at every sample instant.

Control Implementation and Comparison of the Two Methods. Both the methods need a digital signal processor (DSP)-based system for their implementation. In one scheme [36] for the Venturini method, the programmable timers, as available, are used to time out the PWM gating signals. The processor calculates the six-switch duty cycles in each sampling interval, converts them to integer counts, and stores them in the memory for the next sampling period. In the SVM method, an erasable programmable read-only memory (EPROM) is used to store the selected sets of active and zero vectors, and the DSP calculates the on-times of the vectors. Then, with an identical procedure as in the other method, the timers are loaded with the vector on-times to generate PWM waveforms through suitable output ports. The total computation time of the DSP for the SVM method has been found to be much less than that of the Venturini method. Comparison of the two schemes shows that while in the SVM method the switching losses are lower, the Venturini method shows better performance in terms of input current and output voltage harmonics.

A *direct control* method as used in conjunction with the voltage source converters has been developed recently and implemented with a 10 kVA matrix converter [48]. Moreover, the voltage transfer ratio can be increased by going into overmodulation. Enhanced methods employing SVM are discussed in [49,50] in which VTR of 0.92 is achieved.

14.5.2 Commutation and Protection Issues in a Matrix Converter

As the matrix converter has no dc link energy storage, any disturbance in the input supply voltage will affect the output voltage immediately, and a proper protection mechanism has to be incorporated, particularly against overvoltage from the supply and overcurrent in the load side. As mentioned, two types of bidirectional switch configurations have hitherto been used: one, the transistor (now IGBT) embedded in a diode bridge and, the other, the two IGBTs in antiparallel with reverse voltage blocking diodes (shown in Fig. 14.31B and C). In the latter configuration, each diode and IGBT combination operates in two quadrants only, which eliminates the circulating currents otherwise built up in the diode bridge configuration that can be limited by only bulky commutation inductors in the lines.

Commutation. The MC does not contain freewheeling diodes that usually achieve safe commutation in the case of other converters. To maintain the continuity of the output current as each switch turns off, the next switch in sequence must be immediately turned on. In practice, with bidirectional switches, a momentary short circuit may develop between the input phases when the switches cross over, and one solution for the configurations shown in Fig. 14.31B, C, and E is to use a *semisoft current commutation* using a multistepped switching procedure to ensure safe commutation [51–53]. This method requires independent control of each two-quadrant switches, sensing the direction of the load current and introducing a delay during the change of switching states. The switching rule for proper commutation from S_1 to S_2 of the arrangement shown in Fig. 14.34 for $i_L > 0$ with the two-quadrant switches for *four-stepped commutation* [51,53] is (a) turn off S_{1B}, (b) turn on S_{2A}, (c) turn off S_{1A}, and (d) turn on S_{2B}.

Analogously, for $i_L < 0$, the switching rule will be (a) turn off S_{1A}, (b) turn on S_{2B}, (c) turn off S_{1B}, and (d) turn on S_{2A}. These steps for both the cases are shown diagrammatically in Fig. 14.35.

Typically, these commutation strategies are now implemented using programmable logic devices such as field-programmable gate array (FPGA) and programmable logic device (PLD) [53,54]. Also, it is worth mentioning that the configuration shown in Fig 14.31D has to stick to two-step commutation that despite of having a considerable advantage of employing less number of switches will produce more spikes in the output voltages.

A robust voltage commutation scheme without sacrificing the line side current waveform quality and with minimal information requirement has been reported recently [55]. Another way to achieve better commutation is by Z-sourcing the input of the matrix converter [56].

Protection Strategies. A clamp capacitor (typically 2 μF for a 3 kW permanent magnet (PM) motor) connected through two three-phase full-bridge diode rectifiers involving additional

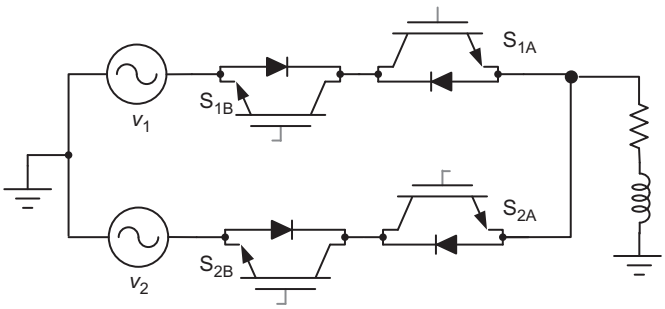


FIG. 14.34 Safe commutation scheme.

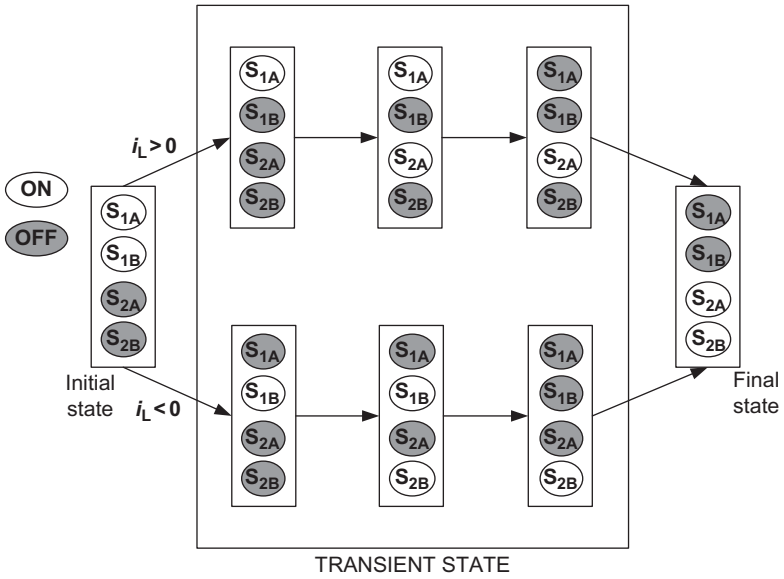


FIG. 14.35 Transition from one bidirectional switch to other employing *semisoft commutation*.

12 diodes as shown in Fig. 14.31A (a new configuration has been reported in [57] where the number of additional diodes is reduced to six using the antiparallel switch diodes at the input and output lines of the MC) serves as a voltage clamp for possible voltage spikes under normal and fault conditions. A new passive protection strategy involving suppressor diodes and varistors for excellent overvoltage protection is discussed recently in [58], which allows the removal of the large and expensive diode clamp. A snubberless solution for overvoltage protection is presented in [59].

Input Filter. A three-phase single-stage LC filter at the input consisting of three capacitors in star and three inductors in the line is used to adequately attenuate the higher order harmonics and render sinusoidal input current. Typical values of L and C based on a 415 V converter with a maximum line current of 6.5 A and a switching frequency of 20 kHz are 3 mH and 1.5 μF only [60]. The filter may cause minor phase shift in the input displacement angle that needs correction. Another filter designs can be seen in [28,29]. Ref. [61] lately has employed the input filter capacitors as an energy exchange devices to enhance the *ride-through capability* of the matrix converter. Ref. [62] discusses the designing of an EMI filter for matrix converter applications.

Fig. 14.36 shows typical experimental waveforms of output line voltage and line current of an MC. The output line current is mostly sinusoidal except a small ripple, when the switching frequency is around 1 kHz only.

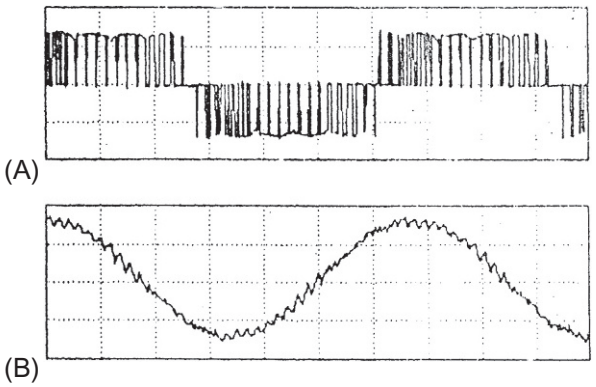


FIG. 14.36 Experimental waveforms for a matrix converter at 30 Hz frequency from a 50 Hz input: (A) output line voltage and (B) output line current.

14.5.3 Multilevel Matrix converter

Erickson and Al-Naseem [63] introduced a multilevel matrix converter with four-quadrant dc link H-bridge switching cells as shown in Fig 14.37 in 2001. These are suitable for medium- or high-voltage ac-to-ac power conversion. The use of four transistors in the switch cell of Fig. 14.37A allows the average current to be doubled, relative to the conventional matrix converter whose four-quadrant switches are realized using two transistors and two diodes. With dc capacitor, the switch cell is capable of producing instantaneous voltages +V, 0, −V. These converters can both increase and decrease the voltage amplitude with arbitrary power factors. With series connection of switch cells in each branch of the matrix, multilevel switching can be attained with device voltages locally clamped to dc capacitor voltages. Several types of multilevel matrix converter topologies have been proposed over the years, including a novel capacitor-clamped one and with a space vector modulation [64,65]. In [65], the converter utilizes flying capacitors to

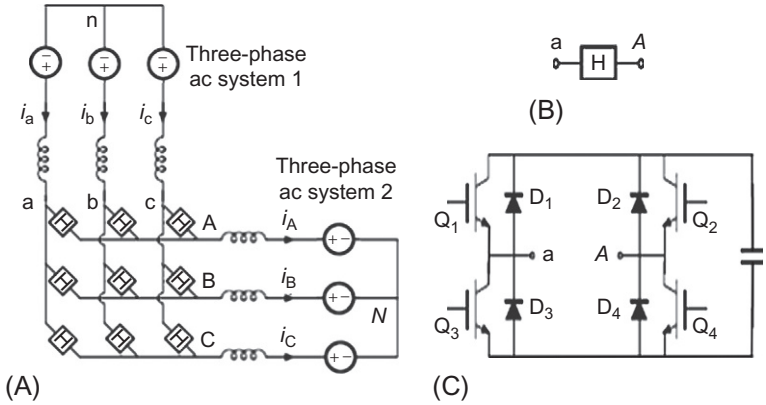


FIG. 14.37 Multilevel matrix converter: (A) configuration, (B) switch symbol, and (C) switch realization.

balance voltage distribution of series-connected bidirectional switches and provide middle-voltage levels.

Recently, with cascaded combination of multiple matrix converter (MC) modules, principles of high-power multimodular matrix converters (MMMCs) built from three-input two-output matrix converter (3×2 MC) have been presented in [66] with modulation schemes to synthesize sinusoidal waveforms on both sides of the converters. Recent work on modulation strategies on MMMCs can be seen in [67–69]. The circuit shown in Fig. 14.38 is known as MMMC-I. Another structure is discussed in these papers in which nine modules of 3×2 MCs are employed. This is an extension of the first topology and attains a multilevel structure for higher power output and better line side harmonic performance. These topologies feature modular design and bidirectional power flow and enable the use of low-voltage power devices. They may serve as potential candidates for high-power applications where regenerative capability and power density are of importance. However,

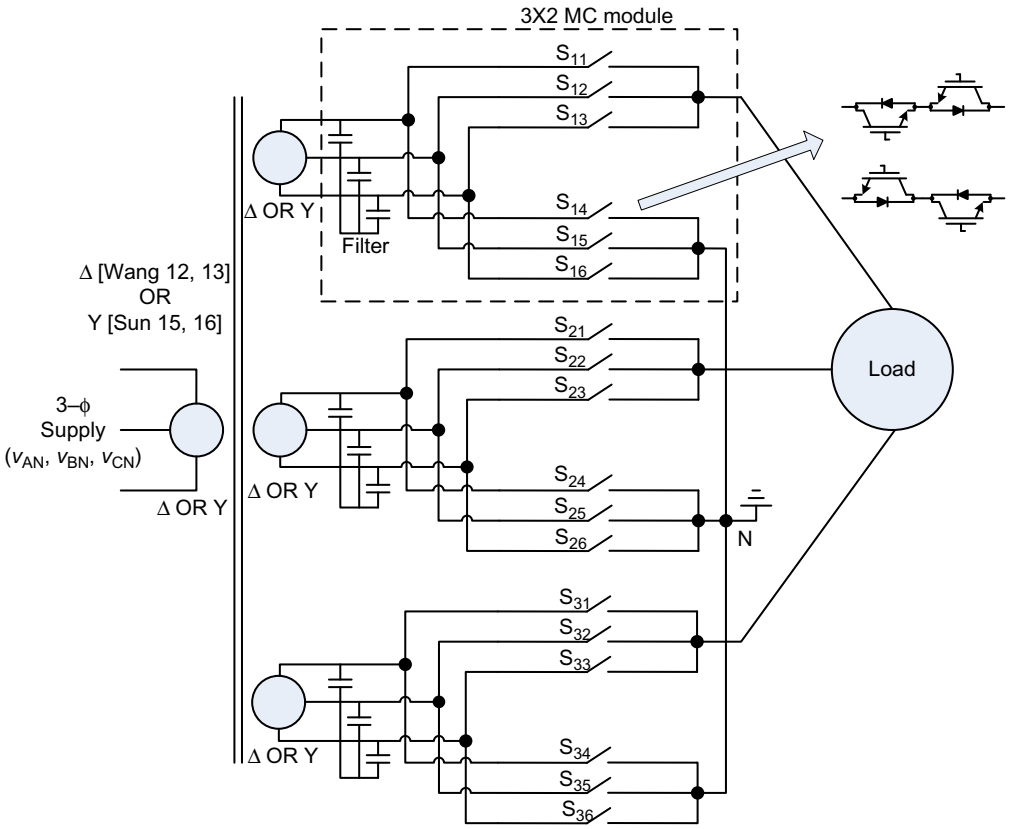


FIG. 14.38 Multimodular matrix converter (MMMC-I) topology.

the drawbacks of them are large number of devices and the use of the input transformer.

14.5.4 Indirect Matrix Converters

A conventional matrix converter (CMC) as shown in Fig. 14.31A requires nine bidirectional switches, usually constructed using 18 IGBTs, to switch the three-input phases between the three-output phases. The indirect matrix converters (IMCs), as seen in Fig. 14.40A also have 18 controllable switches. The difference lies in the control of such a converter. This configuration is easier to implement as the control strategies of controlled rectifiers, and inverters can be directly implemented. This topology was first introduced in [70] and later discussed in [71]. It employs 18 controllable switches out 12 are used in rectification and 6 in inversion process. The sparse matrix converter (SMC) (Fig. 14.39) is derived from the IMC that is split into an input stage and output stage without any capacitance in the dc link. The input stage is arranged so that only nine switches are required, while the output stage has a standard six-switch configuration. Thus, the SMC has a total of 15 switches compared with 18 for a CMC and IMC. The functional equivalence, the controllability, and the operating range of the SMC are the same as CMC despite the reduced number of unipolar turn-off power switches [72]. Further reduction of the number of IGBTs is possible with ultra sparse matrix converter (USMC) [73], Fig. 14.40 having 12 IGBTs, with restricted operation to a unidirectional power flow and controllability of the phase displacement of input voltage and current fundamental to $\pm\pi/6$ [73]. Very recently, a space vector modulation scheme for an indirect three-level sparse matrix converter (I3 SMC), which is a combination of a three-level neutral-clamped voltage source inverter and an indirect matrix converter, has been discussed in [74]. A 100 kHz SiC sparse matrix converter using 1300 V and 4 A SiC JFET cascade devices has been reported in [75], which is suitable for aircraft applications where a low-volume/low-weight converter is desired. Ref. [76] also introduced a topology with 12 switches employing unidirectional switches in the rectification process. Real-time implementation of an IMC employing SVM algorithms can be seen in [77].

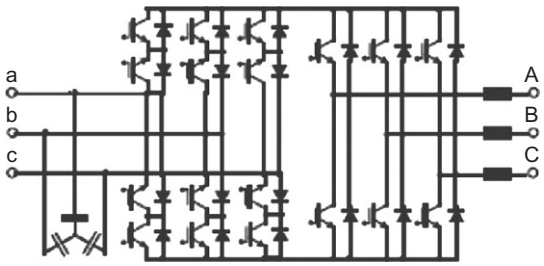


FIG. 14.39 Indirect matrix converter (IMC).

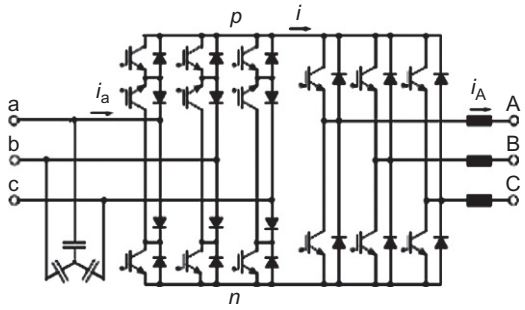


FIG. 14.40 Sparse matrix converter (SMC).

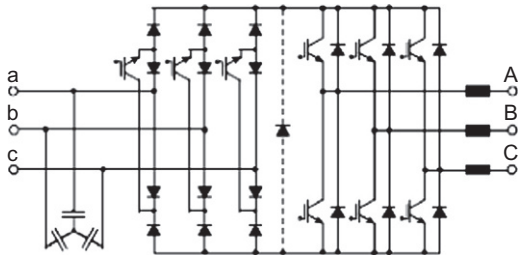


FIG. 14.41 Single-phase Z-source matrix converter.

14.5.5 Single-Phase Matrix Converters

The first single-phase matrix converter was studied by Zuckerberger in [78]. In this paper, converter operation was shown to step down the voltage and step up the frequency. Later in [79], step-up/down frequency operation with safe commutation strategy was developed. The limitation of above schemes lied in boosting of output voltages beyond input voltage. This was overcome by introducing single-phase Z-source matrix converter by Nguyen et al. shown in Fig. 14.41, and step-up/step-down of both voltage and frequency was achieved [80]. A family of high-frequency isolated single-phase Z-source matrix converter with safe commutation strategy is discussed in [81]. Another single-phase matrix converter can be seen in [82–86]. An ac Z-source converter based on gamma structure with safe commutation is discussed in [87]. A novel T-type single-phase ac-ac converter is proposed in [88]. A single-phase ac-ac modular multilevel converter is discussed for railway traction purpose in [89].

14.6 High Frequency Linked Single-Phase to Three-Phase Matrix Converters

Several kinds of single-phase to three-phase high frequency (typically, 20 kHz) cycloconverters (actually, matrix converters with MCT switches) using "soft switching" were reported for ac motor drive applications [90–92]. Fig. 14.42 [90] shows a typical configuration of such a converter in which an H-bridge inverter produces a high-frequency single-phase voltage, which

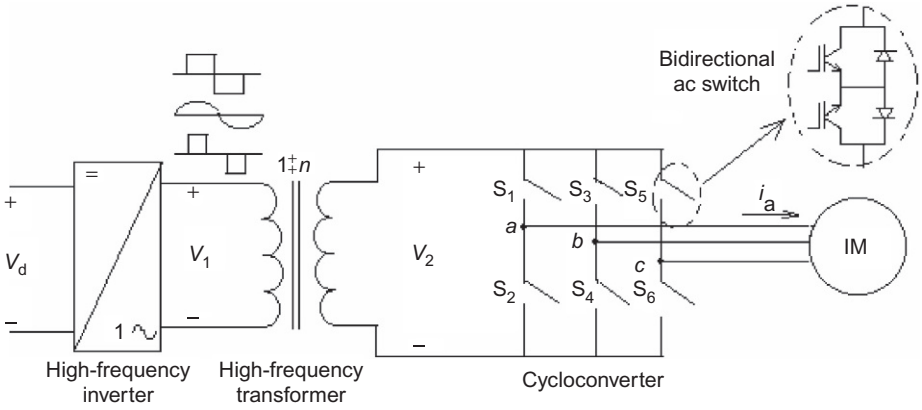


FIG. 14.42 Ultra sparse matrix converter (USMC).

is fed to the cycloconverter through a high-frequency transformer. The high frequency ac may be either sinusoidal generated by a resonant link inverter or quasisquare wave as shown. These systems have been developed at laboratories but not yet available commercially Fig. 14.43 [90].

14.6.1 High Frequency Integral-Pulse Cycloconverter

The input to these converters may be sinusoidal or quasi square wave, and it is possible to use integral half-cycle pulse-width modulation (IPM) principle to synthesize the output voltage waves. The advantage is that the devices can be switched at zero voltage reducing the switching loss. This converter can only work at output frequency, which are multiples of the input frequency [90].

14.6.2 High-Frequency Phase-Controlled Cycloconverter

Here, phase control principle as explained earlier is used to synthesize the output voltage. A sawtooth carrier wave is compared with the sine modulating wave to generate the firing instants of the switches. The phase control provides switching at zero current reducing switching loss, but this scheme has more complex control circuit compared with the previous one. However, it can work at any frequency [91].

14.7 Applications of AC-AC Converters

14.7.1 Applications of AC Voltage Controllers

AC voltage controllers are used either for control of the rms value of voltage or current in lighting control, domestic and industrial heating, speed control of fan, pump or hoist drives, soft starting of induction motors, etc. or as *static ac switches* (*on/off control*) in transformer tap changing, temperature control, speed stabilization of high-inertia induction motor drives like centrifuge, capacitor switching in static reactive power compensation, etc.

In *fan or pump drives* with induction motors, the torque varies as the square of the speed. So, the speed control is required in a narrow range, and an ac voltage controller is suitable for an induction motor with a full load slip of 0.1–0.2 in such applications. For these drives, braking or reverse operations are not

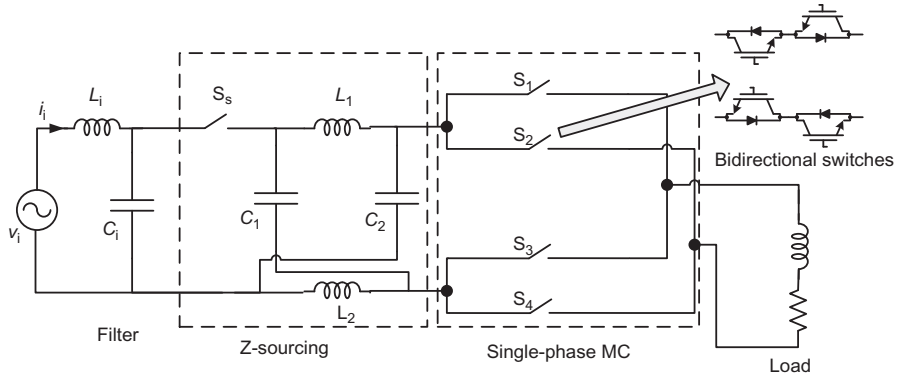


FIG. 14.43 High-frequency-linked single-phase to three-phase matrix converter.

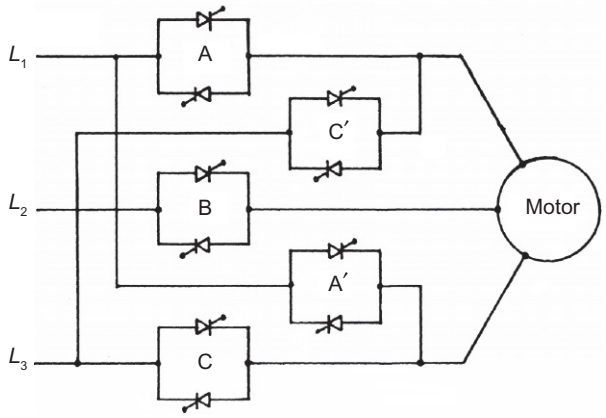


FIG. 14.44 Four-quadrant ac voltage controller.

needed, but for the crane hoist drive, both motoring and braking are needed, and a four-quadrant ac voltage controller can be obtained by a modification of the ac voltage controller circuit as shown in Fig. 14.44. SCR pairs A, B, and C provide operation in quadrants I and IV and A, B, and C in quadrants II and III. While changing from one set of SCR pairs to another, care should be taken to ensure that the incoming pair is activated only after the outgoing pair is fully turned off.

Ac voltage controllers are being increasingly used for *soft starting* of induction motors, as they have a number of advantages over the conventional starters such as smooth acceleration and deceleration, ease in implementation of current control, simple protection against single-phasing or unbalanced operation, reduced maintenance and losses, and the absence of current inrush. Even for the fixed-speed industrial applications, the voltage controllers can be used to provide a reduced stator voltage to an induction motor to improve its efficiency at light load and result in energy saving. Operation at an optimum voltage reduces the motor flux which, in turn, reduces the core loss and the magnetizing component of the stator copper loss. Considerable savings in energy can be obtained in applications where a motor operates at no load for a significant time such as in drills, machine tools, woodworking machines, and reciprocating air compressors. A popular approach to find an optimum operating voltage is to maximize the motor power factor by maintaining a minimum phase shift between the voltage and current after sensing them.

The ac switch with on/off control used in driving a high-inertia centrifuge involves switching on of the motor when the speed of the centrifuge drops below the minimum allowable level and switching off when the speed reaches the maximum allowable level—thus maintaining a constant average speed. An identical scheme of control is used with an ac switch for temperature control of an electric heater or air conditioner.

Integral cycle control is well suited to heating control while it may cause flicker in normal incandescent lighting control and speed fluctuations in motor control. However, with this control, less voltage distortion is produced in the ac supply system, and less radio-frequency interference is propagated when compared with the phase-controlled system.

14.7.2 Applications of Cycloconverters

Cycloconverters as frequency changers essentially find well-established applications in (1) high-power low-speed reversible ac motor drives with constant-frequency input and (2) constant-frequency power supplies with a variable-frequency input as in variable-speed constant frequency (VSCF) system, whereas they find potential applications in (3) controllable volt-ampere reactive (VAR) generators for power factor correction, and (4) ac system interties linking two independent power systems as demonstrated in [15].

Variable Speed AC Drives. In this category, the applications of cycloconverter-controlled induction motor and synchronous motor drives have been adequately reviewed in [9]. Cycloconverter-fed synchronous motors are well suited for low-speed drives with high torque at standstill, and high-capacity gear-less cement mills (tube or ball mill above 5 MW) have been the first applications of these drives.

Since the 1960s, as developed by Siemens and Brown Boveri, one of the early installations employs a motor rating of 6.4 MW having a rotor diameter of 5 m and length of 18.5 m, whereas the stator construction is similar to that of a hydroelectric generator with 44 poles requiring 5.5 Hz for maximum speed of 15 rpm. The motor is flanged with the mill cylinder without additional bearings or "wrapped" directly around it, known as a *ring motor* [93]. With the evolution of *field orientation* or *vector control*, cycloconverter-fed synchronous motors have replaced or are replacing the dc drives in the reversing rolling mills (2/4 MW) with extreme high-dynamic requirements for torque and speed control [94–96], in mine winders and haulage [96,97] of similar high ratings and in icebreakers and ships equipped with diesel generators with power ratings of about 20 MW/unit [98]. In these applications, the cycloconverter-fed synchronous motor is in *self-controlled* mode and known as *ac commutatorless motor* when the cycloconverter firing signals are derived from a rotor shaft position sensor, so that the frequency is slaved to the rotor speed and not vice versa with the result that the hunting and stability problems are eliminated, and the torque is not limited to pullout value. Further, with field control, the motor can be operated at leading power factor when the cycloconverter can operate with *load commutation* from the motor side at high speed in addition to the line commutation from the supply at low speed, thus providing speed control over a wide range. A cycloconverter-fed ac commutatorless motor is reported in [99] where the cycloconverter is operated both in sinusoidal and trapezoidal mode—the latter is attractive for better system power factor and higher voltage output at the cost of increased harmonic content [1]. A stator-flux-oriented vector control scheme for a six-pulse circulating current-free cycloconverter-fed synchronous motor with a flux

observer suitable for a rolling mill drive (300–0–300 rpm) is reported in [12]. A 12-pulse, 9.64 MVA, and 120/33.1 Hz cycloconverter-linear synchronous motor combination for Maglev Vehicle ML-500, a high-speed train, (517 km/h) is in the process of development in Japan since the early 1980s [100]. Several recent projects involving very high-power (larger than 15 MW) semiautogenous grinding (SAG) mills with cycloconverter-fed synchronous motor drives in mining applications in Peru and Brazil are reported in [101]. Latest technological advances, applications, and future trends of cycloconverters in industrial medium-voltage drives have been discussed in [102].

Regarding cycloconverter-fed induction motors, early applications were for control of multiple run-out table motors of a hot strip mill, high-performance servo drives, and controlled slip-frequency drive for diesel electric locomotives. Slip-power-controlled drives in the form of static Scherbius drives with very high ratings using cycloconverter in the rotor of a doubly fed slip ring induction motor have been in operation for high-capacity pumps, compressors [103], and even in a proton-synchrotron accelerator drive in CERN, Geneva [104]. Though synchronous motors have been preferred for very high-capacity low-speed drives because of their high rating, ability to control power factor, and precisely set speed independent of supply voltage and load variations, induction motors, because of their absence of excitation control loop, simple structure, easy maintainability, and quick response, have been installed for cycloconverter-fed drives in Japan. For example, a seamless tube piercing mill [105] where a squirrel cage six-pole 3 MW, 188/300 rpm, 9.6/15.38 Hz, and 2700 V motor is controlled by a cycloconverter bank of capacity 3750 KVA and output voltage 3190 V.

Constant Frequency Power Supplies. Some applications such as aircraft and naval ships need a well-regulated constant-frequency power output from a variable-frequency ac power source. For example, in aircraft power conversion, the alternator connected to the engine operating at a variable speed of 10,000–20,000 rpm provides a variable-frequency output power over 1200–2400 Hz range that can be converted to an accurately regulated fixed frequency output power at 400 Hz through a cycloconverter with a suitable filter placed within a closed loop. The output voltages of the cycloconverter are proportional to the fixed frequency (400 Hz) sine-wave reference voltage generator in the loop.

Both synchronous and induction motors can be used for VSCF generation. The static Scherbius system can be modified (known as Kramer drive) by feeding slip power through a cycloconverter to a shaft-mounted synchronous machine with a separate exciter for VSCF generation. A new application in very high power ratings of constant frequency variable speed motor generators with cycloconverter is in pumped storage schemes using reversible pump turbines for adaptation of the generated power to varying loads or keeping the ac system frequency constant. In 1993, a 400 MW variable speed pumped storage system was commissioned by Hitachi at Okhawachi hydropower plant [106] in Japan where the field windings of a 20-pole generator/motor are excited with three-phase low-frequency ac current via slip rings by a 72 MVA, three-phase 12-pulse line-commuted cycloconverter. The armature terminals rated at 18 kV are connected to a 500 kV utility grid through a step-up transformer. The output frequency of the circulating current-free cycloconverter is controlled within ± 5 Hz, and the line frequency is 60 Hz. The variable speed system has a synchronous speed of 360 rpm with a speed range $330 - 390$ rpm. The operational system efficiency in the pump mode is improved by 3% when compared with the earlier constant speed system.

Static VAR Generation. Cycloconverters with a high-frequency (HF) base, either an HF generator or an oscillating LC tank, can be used for reactive power generation and control, replacing synchronous condensers or switched capacitors as demonstrated in [15]. If the cycloconverter is controlled to generate output voltage waves whose wanted components are in phase with the corresponding system voltages, reactive power can be supplied in either direction to the ac system by amplitude control of the cycloconverter output voltages. The cycloconverter will draw leading current from (i.e., it will supply lagging current to) the ac system when its output voltage is greater than that of the system voltage and vice versa.

Interties between AC Power Systems. The naturally commutated cycloconverter (NCC) was originally developed for this application to link a three-phase, 50-Hz ac system with a single-phase $16\frac{2}{3} -$ Hz railway supply system in Germany in the 1930s. Applications involve slip-power-controlled motors with subsynchronous and supersynchronous speeds. The stator of the motor is connected to 50-Hz supply, which is connected to the rotor and through a cycloconverter, and the motor drives a single-phase synchronous generator feeding to $16\frac{2}{3} -$ Hz system [107,108]. A static asynchronous intertie between two different systems of different frequency can be obtained by using two NCCs in tandem, each with its input terminals connected to a common HF base. As long as the base frequency is appropriately higher than that of the either system, two system frequencies can be either same or different. The power factor at either side can be maintained at any desired level [15].

14.7.3 Applications of Matrix Converters and New Developments

The practical applications of the matrix converters, as of now, are very limited. The main reasons are (1) nonavailability of the bilateral fully controlled monolithic switches capable of high-frequency operation, (2) complex control law implementation, (3) an intrinsic limitation of the output/input voltage ratio, and (4) commutation and protection of the switches. The switches are assembled from existing discrete devices resulting in increased cost and complexity, and only experimental circuits of conventional matrix converters (CMC) of capacity up to

150 kVA [109] for a single unit have been built. However, with the advances in device technology, it is hoped that the problems will be solved eventually, and the MC will not only replace the NCCs in all the applications mentioned under Section 14.7.2 but also take over from the PWM rectifier-inverters as well. Yaskawa has introduced several drives based on matrix converters, most of which are for industrial purposes. U1000 [110] (Fig 14.45) is an industrial drive available in 200/400 V and power ranging from 5 to 500 hp. Another drive Z1000U [112] is an HVAC drive available between 7.5 and 350 hp. AC7 [111] is yet another smaller version with power range of 7.5–125 hp. AC7 is not commissioned in the Americas. Another interesting applications of multilevel and multicell matrix converters for medium-voltage high-power drives have been developed [113] Super energy-saving multicell medium-voltage matrix converters (FSDrive-MX1S) of rating 3 kV, 200–3000 kVA or 6 kV, and 400–6000 kVA have been built by Yaskawa Electric, Japan [114], where by intelligently phase shifting the carrier of each cell and combining them in the motor windings, medium voltages are achievable as shown in Fig. 14.46. The salient features of these medium-voltage converters are as follows:

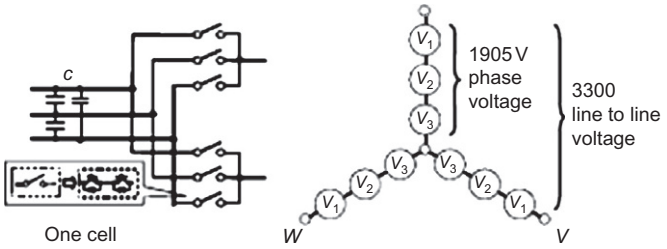


FIG. 14.46 Schematic of a multicell matrix converter with three cells in series in each phase.

- Four-quadrant operation;
- Excellent input current waveform due to multiple phase shifting winding of the input transformer;
- Flexible design, three cells in series yielding 3.3 kV and 200–3000 kVA and six cells in series yielding 6 kV and 400–6000 kVA system;
- Excellent output voltage waveform due to multistep configuration.

The applications for these drives as recommended are as follows: with heavy loads that require regenerative energy such as steel manufacturing process lines or cargo handling machinery, and also that need power regeneration for a long period such as winders for paper Fig. 14.47.

Recently, reverse blocking IGBTs have opened up the possibility of bidirectional switch (BDS) construction for a practical matrix converter with just two back-to-back devices [116–118]. A compact full matrix converter power module EconoMac



FIG. 14.45 An industrial matrix converter variant by Yaskawa (U1000, variants available between 5 and 500 hp, [111]).

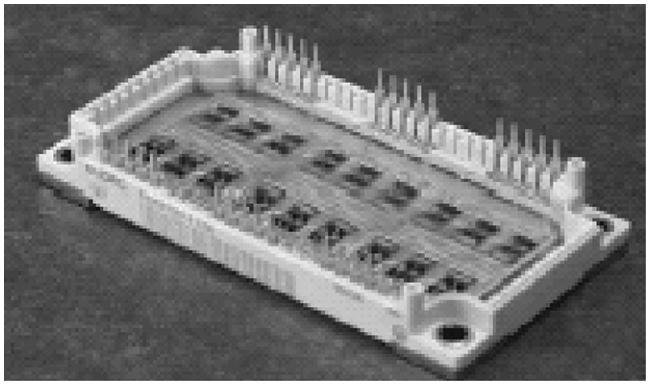


FIG. 14.47 EconoMac matrix converter module by Eupec [115].

[115] in a single package using 18 IGBT devices (35 A and 1200 V) and diodes in the common collector configuration (Fig. 14.44) is available with Eupec/Siemens, Germany. This packaging minimizes the stray inductance in the current commutation paths. Fuji and Powerex have developed engineering samples for matrix converter output leg in a module using RB-IGBTs. A new power electronic building block (PEBB) configuration for a low-cost MC has been proposed in [119]. Recently, an efficient approach to design discrete packaging of bidirectional resonant power switch for matrix converters has been proposed by computing the magnetic field orientation inside the switching cell [120]. Several new concepts in protection, commutation, switch design, and modulation strategy have been presented in [121].

Several new methods like overmodulation [122], adaptive rate regulation [123], and two-side modulation control [124] have been introduced with experimental results to achieve *higher voltage transfer ratio*. A matrix converter-based three-phase open-end winding ac machine drive having matrix converters, one at each side of the open-end winding with space vector PWN has been recently described in [125] to achieve several simultaneous benefits, such as converter voltage gain up to 1.5, controllable grid power factor, and elimination of the high-frequency common-mode voltage at the machine terminals. A generalized scalar PWM (GSPWM) technique to reduce the common-mode voltage in matrix converter without degrading the input currents' quality has been studied in a recent paper [126].

Design and loss comparison of matrix converters and dc link voltage source converters (VSC) have been discussed in [127,128]. It is shown that although MC requires 50% more semiconductors and gate drives excluding clamp circuit, the active silicon area and the number of gate unit power supplies are comparable with that of VSC of the same power rating. The losses of both converter systems are roughly the same at the typical range of 40%–70% of rated torque and speed and a switching frequency of 10 kHz. The MC realizes a distinct better efficiency (92.5%–96%) at 100% torque compared with VSC for the same IGBT modules. Also, the maximum switching frequency of the MC (30 kHz at 250% rated torque) is also substantially higher. The low losses allow a reduction of current ratings (by 33%) of IGBT modules in MC. The extra harmonic losses due to use of a matrix converter for a motor drive with two commonly used modulation techniques have been computed and compared in [129].

Various potential applications of matrix converters have been proposed, and experiments conducted in the field of VSCF systems such as wind turbine and microturbine [130], switched mode power supplies [131], doubly fed induction motor [132,133] including wind power system applications [134], and marine propulsion [135]. Few modern solutions for industrial matrix converter applications including a new integrated matrix converter motor (MCM) have been reported [136,137]. The range of published practical implementations varies from a 2 kW matrix converter using silicon carbide devices and switching at 150 kHz for aerospace applications built at ETH in Zurich, Switzerland, to a 150 kVA converter using 600 A IGBTs built at US army research labs in collaboration with the University of Nottingham, the United Kingdom [54,109]. A matrix converter using MCTs with enhanced commutation times is described in [138].

The complex control schemes of matrix converter demand higher test requirements, and one of the modern means of testing the controllers before final integration on actual apparatus is to make hardware-in-the-loop (HIL) real-time simulation tests as developed recently [139].

Matrix converter-fed adjustable speed drives (ASDs) have the advantages of inherent four-quadrant operation, the absence of bulky dc link electrolytic capacitors, clean input power characteristics with high input power factor, and increased power density with the possibilities of operating at higher temperatures. However, due to the absence of the dc link, these are more susceptible to input power disturbances, and a *ride-through module* is needed to be added for these drives under short-term power interruption. Such a module as developed with minimal addition of hardware and software into a matrix converter (230 V and 3 kVA) has been reported in [140]. A PWM modulation strategy for fault tolerant operation of the matrix-converter-based drives against opened switch, opened phase faults, and shorted winding failures has been proposed in [141]. This can improve the reliability of the matrix converter drives as it is possible to keep continuous by regulating the two remaining phases after isolating the faulted phase.

A novel application of a three-phase matrix converter as the static conversion unit for a ground power supply unit for aircraft servicing has been presented in [142] to provide a compact solution with no dc link and the capability to generate a high quality 400-Hz sinusoidal waveform in the steady state. Three-phase Z-source matrix converter is under consideration. The benefit of Z-sourcing is that firstly, a VTR more than 0.866, can be achieved. Ref. [143] discusses a family of Z-sourced DMCs in which a VTR of 0.992 is achieved. Secondly, it helps in overcoming the commutation problem. Work on Z-source IMC is also being done [144]. Comparative study on various Z-source and quasi-Z-source IMC is done in [145]. A detailed evaluation on various Z-source DMCs and IMCs is recently done in [56]. Z-source DMC and IMC are shown in Fig. 14.48. A direct ac-ac current source matrix converter for applications in industrial power systems is introduced in [146]. A dynamic voltage restorer (DVR) system employing matrix converter and flywheel storage has been proposed in [147] to cope with voltage sag problem in power system. The proposed topology eliminates the dc link passive components resulting in reduced maintenance requirement and improved power density.

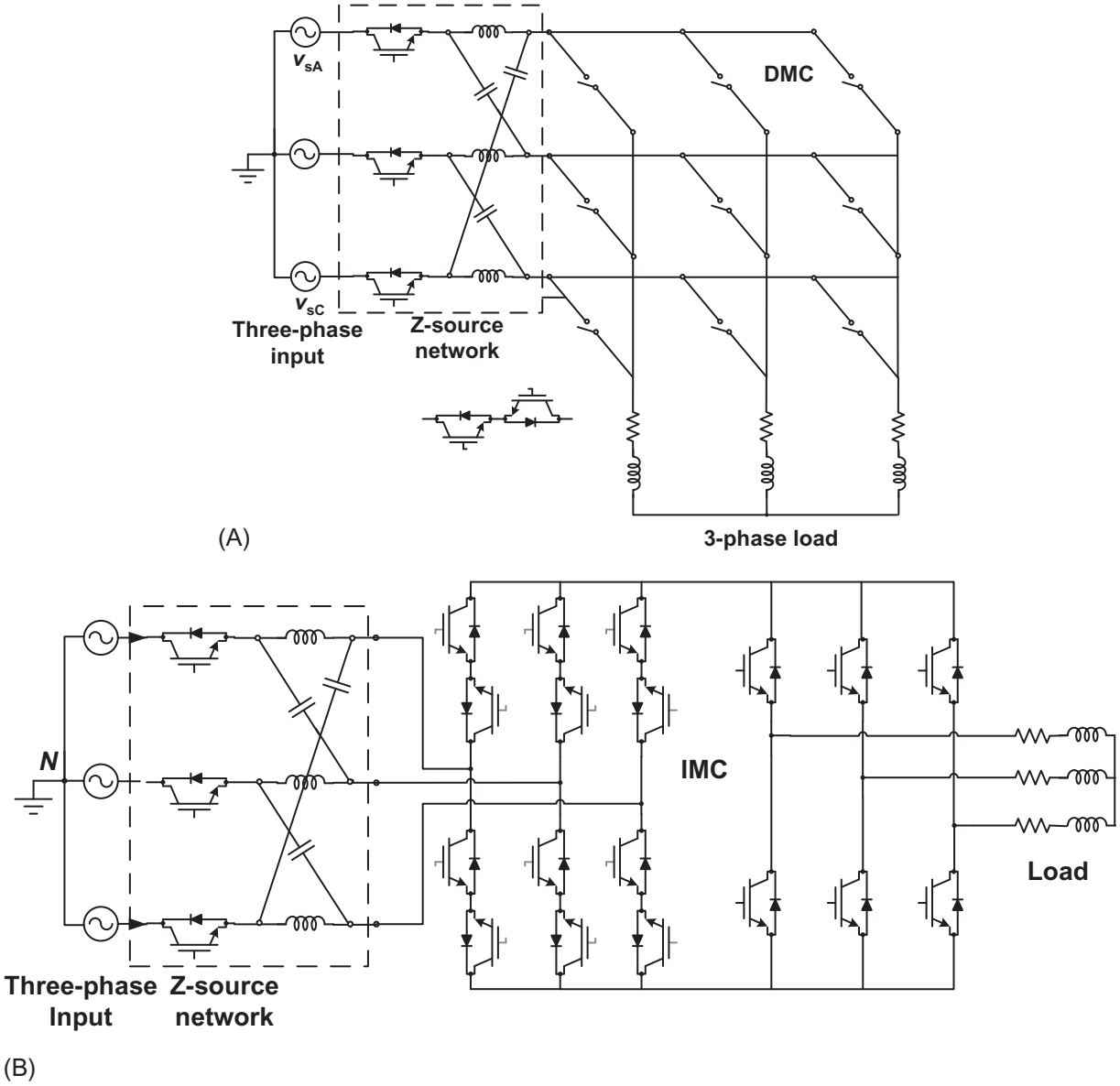


FIG. 14.48 Three-phase Z-source matrix converters: (A) Z-source DMC and (B) Z-source IMC.

References

[1] C. Rombaut, G. Seguier, R. Bausiere, Power Electronic Converters—AC/AC Conversion, McGraw-Hill, New York, NY, 1987.

[2] W. Shepherd, Thyristor Control of AC Circuits, Granada Publishing, Great Britain, 1975.

[3] A.M. Trzynadlowski, Introduction to Modern Power Electronics, John Wiley, New York, NY, 1998.

[4] M. Rashid, Power Electronics: Circuits, Devices and Applications, Prentice Hall, Upper Saddle River, NJ, 1993.

[5] D.W. Hart, Introduction to Power Electronics, Prentice Hall, Upper Saddle River, NJ, 1997.

[6] A.K. Chattopadhyay, S.P. Das, S. Karchowdhury, Computer simulation of three-phase thyristor regulator-fed static and induction motor loads-A generalised approach, Electr. Machin. Power Sys. 21 (1993) 329–342.

[7] S.B. Dewan, A. Straughen, Power Semiconductor Circuits, John Wiley, New York, NY, 1975.

[8] B.R. Pelly, Thyristor Phase-Controlled Converters and Cycloconverters, John Wiley, New York, NY, 1971.

[9] A.K. Chattopadhyay, Cycloconverters and cycloconverter-fed drives—a review, J. Indian Inst. Sci. 77 (1997) 397–419.

[10] A.K. Chattopadhyay, T.J. Rao, Simplified control electronics for a practical cycloconverter, Int. J. Electronics 43 (1977) 137–150.

[11] B.M. Bird, J.S. Ford, Improvements in phase-controlled circulating current cycloconverters using communication principles, in: Proc. IEEE, vol. 121, no. 10, 1974, pp. 1146–1149.

[12] S.P. Das, A.K. Chattopadhyay, Observer based stator flux oriented vector control of cycloconverter-fed synchronous motor drive, IEEE Trans. Ind. Appl. IA-33 (4) (1997) 943–955.
[13] P. Syam, P.K. Nandi, A.K. Chattopadhyay, An improvement feedback technique to suppress sub-harmonics in a naturally commutated cycloconverter, IEEE Trans. Ind. Electron. 45 (6) (1998) 950–952.
[14] P. Syam, P.K. Nandi, A.K. Chattopadhyay, Improvement in power quality and a simple method of subharmonic suppression for a cycloconverter-fed synchronous motor drive, IEEE Proc. Electr. Power Appl. 149 (4) (2002) 292–303.
[15] L. Gyugi, B.R. Pelly, Static Power Frequency Changers: Theory, Design and Applications, Wiley-Interscience, New York, NY, 1976.
[16] A.K. Chattopadhyay, T.J. Rao, Methods of digital computation of phase controlled cycloconverter performance, in: Conf. Rec. IEEEIAS Ann. Meet, 1978, pp. 432–439.
[17] Y. Lin, G.T. Heydt, R.F. Chu, The power quality impact of cycloconverter control strategies, IEEE Trans. Power Deliv. 2 (2) (2005) 1711–1718.
[18] M. Loskarn, K.D. Tost, C. Unger, R. Witzmann, Mitigation of Interharmonics due to large cycloconverter-fed mill drives, in: Proc. ICHQP'98. Athens, Greece, October, 1998, pp. 122–126.
[19] M. Venturini, A new sine-wave in sine-wave out converter technique eliminates reactor elements, in: Proc. POWERCON'80, E3-1 1980. E3-1–E3-15.
[20] A. Alesina, M. Venturini, The generalised transformer: a new bidirectional waveform frequency converter with continuously adjustable input power factor, in: Proc. IEEE -PESC'80, 1980, pp. 242–252.
[21] A. Alesina, M. Venturini, Analysis and design of optimum amplitude nine-switch direct ac-ac converters, IEEE Trans. Power Electron. 4 (1) (1989) 101–112.
[22] L. Empringham, J.W. Kolar, J. Rodriguez, P.W. Wheeler, J.C. Clare, Technological issues and industrial application of matrix converters: a review, IEEE Trans. Ind. Electron. 60 (10) (2013) 4260–4271.
[23] L. Zarri, Control of Matrix Converters, (Ph.D. thesis), University of Bologna, Bologna, Italy, 2007.
[24] A. Lindemann, A new IGBT with reverse blocking capability, in: Proc. 9th European Conference on Power Electronics, 2001.
[25] D.G. Holmes, T.A. Lipo, Implementation of a controlled rectifier using ac-ac matrix converter theory, IEEE Trans. Power Electron. 7 (1) (1992) 240–250.
[26] M. Ali, A. Iqbal, M.R. Khan, M. Ayyub, M.A. Anees, Generalized theory and analysis of scalar modulation techniques for a m x n matrix converter, IEEE Trans. Power Electron. 32 (6) (2017) 4864–4877.
[27] P. Wheeler, D. Grant, Optimised input filter design and low-loss switching techniques for a practical matrix converter, IEEE Proc. Electr. Power Appl. 144 (1) (1997) 53–60.
[28] A. Trentin, P. Zanchetta, J. Clare, P. Wheeler, Automated optimal design of input filters for direct ac/ac matrix converters, IEEE Trans. Ind. Electron. 59 (7) (2012) 2811–2823.
[29] A. Dasgupta, P. Sensarma, Filter design of direct matrix converter for synchronous applications, IEEE Trans. Ind. Electron. 61 (12) (2014) 6483–6493.
[30] P.D. Ziogas, S.I. Khan, M. Rashid, Some improved forced commutated cycloconverter structures, IEEE Trans. Ind. Appl. Ia-21 (1985) 1242–1253.
[31] P.D. Ziogas, S.I. Khan, M. Rashid, Analysis and design of forced commutated cycloconverter structures and improved transfer characteristics, IEEE Trans. Ind. Electron. IE-33 (3) (1986) 271–280.
[32] C.L. Neft, C.D. Schauder, Theory and design of a 30 HP matrix converter, in: Conf. Rec IEEE-IAS Ann. Meet, 1988, pp. 248–253.
[33] A. Ishiguru, T. Furuhashi, S. Okuma, A novel control method of forced commutated cycloconverters using instantaneous values of input line voltages, IEEE Trans. Ind. Electron. 38 (3) (1991) 166–172.
[34] L. Huber, D. Borojevic, N. Burany, Analysis, design and implementation of the space-vector modulator for forced commutated cycloconverters, IEEE Proc. B 139 (2) (1992) 103–113.
[35] L. Huber, D. Borojevic, Space vector modulated three-phase to three-phase matrix converter with input power factor correction, IEEE Trans. Ind. Appl. 31 (1995) 1234–1246.
[36] L. Zhang, C. Watthanasarn, W. Shepherd, Analysis and comparison of control strategies for ac-ac matrix converters, IEEE Proc. Power Electr. Appl. 145 (4) (1998) 284–294.
[37] D. Casadei, G. Serra, A. Tani, Reduction of the input current harmonic content in matrix converters under input/output unbalance, IEEE Trans. Ind. Appl. 45 (3) (1998) 401–411.
[38] L. Zhang, C. Watthanasarn, An efficient space vector modulation algorithm for ac-ac matrix converters: Analysis and implementation, in: IEEE Conf Proc. 6th PEVD '96, 1996, pp. 103–113.
[39] M.A. Sayed, A. Iqbal, Pulse width modulation technique for a three-to-five phase matrix converter with reduced commutations, IET Power Electron. 9 (3) (2016) 466–475.
[40] P. Szcześniak, Three-Phase AC-AC Power Converters Based on Matrix Converter Topology: Matrix-Reactance Frequency Converters Concept, Springer-Verlag, London, 2013.
[41] J. Rodríguez, E. Silva, F. Blaabjerg, P. Wheeler, J. Clare, J. Pontt, Matrix converter controlled with the direct transfer function approach: analysis, modelling and simulation, Int. J. Electron. 92 (2) (2005) 63–85.
[42] P.W. Wheeler, J. Rodriguez, J.C. Clare, L. Emperngen, A. Wenstein, Matrix converters: a technology review, IEEE Trans. Indust. Electron. 49 (2) (2002) 276–288.
[43] D. Casadei, G. Serra, A. Tani, L. Zarri, Matrix converter modulation strategies: a new general approach based on space vector representation of the switch state, IEEE Trans. Ind. Electron. 49 (2) (2002) 370–381.
[44] H.J. Cha, P.N. Enjeti, An approach to reduce common mode voltage in matrix converter, IEEE Trans. Ind. Appl, 39 (2003) 1151–1159.
[45] M. Jussila, M. Salo, H. Tuusa, Realization of a three-phase indirect matrix converter with an indirect vector modulation method, in: IEEE-PESC'2003, 2 2003, pp. 689–694.
[46] K. Sun, L. Huang, K. Matsuse, T. Ishida, Combined control of matrix converter fed induction motor drive system, in: Proc. IEEE-IAS Ann. Meet, vol. 3, 2003, pp. 1723–1729.
[47] R. Havrila, B. Dobrucky, P. Balazovic, Space vector modulated three-phase to three-phase matrix converter with unity power factor, in: EPE-PEMC2000 Conf. Rec., vol. 2. Kosice, 2000, pp. 103–108.
[48] P. Mutschler, M. Marcks, A direct control method for matrix converters, IEEE Trans. Ind. Electron. 49 (2) (2002) 362–369.
[49] D. Qiankun, G. Hongjuan, L. Guangquan, Over-modulation strategy of matrix converter based on multi-orbit vector weighted, Trans. China Electrotech. Soc. 26 (4) (2011) 100–106.

[50] Y. Xia, X. Zhang, M. Qiao, F. Yu, Y. Wei, P. Zhu, Research on a new indirect space-vector overmodulation strategy in matrix converter, IEEE Trans. Ind. Electron. 63 (2) (2016) 1130–1141.
[51] N. Burany, Safe control of four-quadrant switches, in: Conf. Rec IEEE-IAS Ann Meet, 1989, pp. 1190–1194.
[52] B.H. Kwon, B.D. Min, J.H. Kim, Novel commutation techniques of ac-ac converters, IEEE Proc. Electr. Power Appl. 145 (4) (1998) 295–300.
[53] Y. Sun, F. Xu, K. Sun, Design of matrix converter with bidirectional switches, in: Proc. IEEE-POWERCON'2002, 2 2002, pp. 1034–1038.
[54] J. Clare, P. Wheeler, New technology: matrix converters, Indust. Electron. Soc. Newslett. 52 (1) (2005) 10–12.
[55] L. Wei, T.A. Lipo, H. Chen, Robust voltage commutation of conventional matrix converter, in: Proc. IEEE-PESC'03, 2, 2003, pp. 717–722.
[56] O. Ellabban, H. Abu-Rub, S. Bayhan, Z-source matrix converter : an overview, IEEE Trans. Power Electron. 31 (11) (2016) 7436–7450.
[57] P. Nielson, F. Blabjerg, J.K. Pederson, New protection issues of a matrix converter: design considerations for adjustable-speed drives, in: IEEE Trans. Ind. Appl, 35 5, 1999, pp. 1150–1161.
[58] J. Mahlein, M. Bruckmann, M. Braun, Passive protection strategy for a drive system with a matrix converter and an induction machine, IEEE Trans. Ind. Electr. 49 (2) (2002) 297–303.
[59] O. Simon, M. Bruckmann, Control and protection strategies for matrix converters, in: Proc. PCIM Conf. Rec. Nuremberg, Germany, 2000.
[60] P. Wheeler, D. Grant, Optimized input filter design and low-loss switching techniques for a practical matrix converter, IEEE Proc. Electr. Power Appl. 144 (1) (1997) 53–59.
[61] D. Orser, N. Mohan, A matrix converter ride-through configuration using input filter capacitors as an energy exchange mechanism, IEEE Trans. Power Electron. 30 (8) (2015) 4377–4385.
[62] M. Degano, EMI Filter Design for Matrix Converters in Airspace Applications, (Ph.D. thesis), University of Nottingham; Nottingham, UK, 2012.
[63] R.W. Erickson, O.A. Al-Naseem, A new family of matrix converters, in: Proc. IEEE-IECON'01 Denver, Co, 2 2001, pp. 1515–1520.
[64] P. Wheeler, X. Lie, M.Y. Lee, L. Emperingham, C. Kunpner, J. Clare, A review of multi-level matrix converter technologies, in: Proc. IET-PEMD'08, 2008, pp. 286–290.
[65] Y. Shi, X. Yang, Q. He, Z. Wang, Research on a novel capacitor clamped multilevel matrix converter, IEEE Trans. Power Electron. 20 (5) (2005) 1055–1065.
[66] J. Wang, B. Wu, D. Xu, N.R. Zargari, Multimodular matrix converters with sinusoidal input and output waveforms, IEEE Trans. Ind. Electron. 59 (1) (2012) 17–26.
[67] J. Wang, B. Wu, D. Xu, N.R. Zargari, Indirect space-vector-based modulation techniques for high-power multimodular matrix converters, IEEE Trans. Ind. Electron. 60 (8) (2013) 3060–3071.
[68] Y. Sun, W. Xiong, M. Su, H. Dan, X. Li, J. Yang, Modulation strategies based on mathematical construction method for multimodular matrix converter, IEEE Trans. Power Electron. 31 (8) (2016) 5423–5434.
[69] Y. Sun, W. Xiong, M. Su, X. Li, H. Dan, J. Yang, Carrier-based modulation strategies for multimodular matrix converters, IEEE Trans. Ind. Electron. 63 (3) (2016) 1350–1361.
[70] J. Holtz, U. Boelkens, Direct frequency converter with sinusoidal line currents for speed-variable AC motors, IEEE Trans. Ind. Electron. 36 (4) (1989) 475–479.
[71] K. Iimori, K. Shinohara, O. Tarumi, Z. Fu, M. Muroya, New current- controlled PWM rectifier- voltage source inverter without DC link components, in: Proc. of PCC'97, 1997, pp. 783–786.
[72] J.W. Kolar, M. Baumann, F. Shafmeister, H. Ertl, Novel three-phase AC-DC-AC sparse matrix converter—part 1: derivation, basic principle of operation, space vector modulation, dimensioning, in: Proc IEEE-APEC'02, 2002, pp. 777–787.
[73] J.W. Kolar, F. Schafmeister, S.D. Round, H. Ertl, Novel three-phase AC-AC sparse matrix converters, IEEE Trans. Power Electron. 22 (5) (2007) 1649–1661.
[74] M.Y. Lee, P. Wheeler, C. Klumpner, Space vector modulated multilevel matrix converter, IEEE Trans. Ind. Electr. 57 (10) (2010) 3385–3394.
[75] T. Friedli, S.D. Round, J.W. Kolar, A 100 kHz SiC sparse matrix converter, in: Proc. IEEE -PESC'07, 2007, pp. 2148–2154.
[76] S. Kim, S. Sui, T.A. Lipo, AC to AC power conversion based on matrix converter topology with unidirectional switches, in: IEEE-APEC, 1998, pp. 301–307.
[77] M. Hamouda, H.F. Blanchette, K. Al-Haddad, F. Fnaiech, An efficient DSP-FPGA-based real-time implementation method of SVM algorithms for an indirect matrix converter, IEEE Trans. Ind. Electron. 58 (11) (2011) 5024–5031.
[78] A. Zuckerberger, D. Weinstock, A. Alexandrovitz, Single-phase matrix converter, IEEE Proc. Electr. Power Appl. 144 (4) (1997) 235–240.
[79] A.K. Gola, V. Agarwal, Implementation of an efficient algorithm for a single phase matrix converter, J. Power Electron. 9 (2) (2009) 198–206.
[80] M.-K. Nguyen, Y.-G. Jung, Y.-C. Lim, Y.-M. Kim, A single-phase Z-source buck—boost matrix converter, IEEE Trans. Power Electron. 25 (2) (2010) 453–462.
[81] H.F. Ahmed, H. Cha, A.A. Khan, H. Kim, A family of high-frequency isolated single-phase Z-source AC – AC converters with safe-commutation strategy, IEEE Trans. Power Electron. 31 (11) (2016) 7522–7533.
[82] C.B. Jacobina, T.M. Oliveira, E.R.C. da Silva, Control of the single-phase three-leg AC/AC converter, IEEE Trans. Ind. Electron. 53 (2) (2006) 467–476.
[83] I.R. Ferreira Moreno Pinheiro Da Silva, C. Brandão Jacobina, A. Cunha Oliveira, Single-phase AC-AC double-star chopper cells (DSCC) converter without common DC-link capacitor, IEEE Trans. Ind. Appl. 51 (6) (2015) 4642–4652.
[84] H.H. Shin, H. Cha, H.G. Kim, D.W. Yoo, Novel single-phase PWM AC-AC converters solving commutation problem using switching cell structure and coupled inductor, IEEE Trans. Power Electron. 30 (4) (2015) 2137–2147.
[85] H.F. Ahmed, H. Cha, A.A. Khan, J. Kim, J. Cho, A single-phase buck-boost matrix converter with only six switches and without commutation problem, IEEE Trans. Power Electron. 8993 (2016) 1–13.
[86] A.A. Khan, H. Cha, H.F. Ahmed, High-efficiency single-phase AC-AC converters without commutation problem, IEEE Trans. Power Electron. 31 (8) (2016) 5655–5665.
[87] M.R. Banaei, R. Alizadeh, N. Jahanyari, E. Seifi Najmi, An AC Z-source converter based on gamma structure with safe-commutation strategy, IEEE Trans. Power Electron. 31 (2) (2016) 1255–1262.
[88] M. Khodabandeh, M. Shahbazi, M.R. Zolghadri, N. Noroozi, T-type direct AC/AC converter structure, IET Power Electron. 9 (7) (2016) 1426–1436.

[89] X. Chen, K. Zhang, W. Liu, J. Xiong, Simplified model and submodule capacitor voltage balancing of single-phase AC/AC modular multilevel converter for railway traction purpose, IET Power Electron. 9 (5) (2016) 951–959.
[90] L. Hui, B. Ozpineci, B.K. Bose, A soft-switched high frequency non-resonant link integral pulse modulated dc-ac converter for ac motor drive, in: Proc. IEEE-IECON, vol. 2, Aachen, Germany, 1998, pp. 726–732.
[91] B. Ozpineei, B.K. Bose, Soft-switched performance based high frequency non-resonant link phase-controlled converter for ac motor drive, in: Proc. IEEE-IECON, vol. 2, Aachen, Germany, 1998, pp. 733–739.
[92] B.K. Bose, Modern Power Electronics and AC Drives, Pearson Education, New Delhi, 2002.
[93] E. Blauenstein, The first gearless drive for a tube mill, Brown Boveri Rev. 57 (1970) 96–105.
[94] W. Timpe, Cycloconverter for rolling mill drives, IEEE Trans. Ind. Appl. IA-18 (4) (1982) 401–404.
[95] R.P. Pallman, First use of cycloconverter-fed ac motors in an aluminium hot strip mill, Siemens Eng. Automat. XIV (2) (1992) 26–29.
[96] E.A. Lewis, Cycloconverter drive systems, in: IEE Conf. Proc. PEVD'96, 1996, pp. 382–389.
[97] K. Madisetti, M.A. Ramlu, Trends in electronic control of mine hoists, IEEE Trans. Ind. Appl. IA-22 (6) (1986) 1105–1112.
[98] A.W. Hill, R.A.V. Turton, R.L. Dunzan, C.L. Schwaln, A vector controlled cycloconverter drive for an ice-breaker, IEEE Trans. Ind. Appl. IA-23 (1987) 1036–1041.
[99] S.P. Das, A.K. Chattopadhyay, Comparison of simulation and test results for an ac commutatorless motor drive, in: IEE Conf. Proc. PEVD'96, 1996, pp. 294–299.
[100] T. Saijo, S. Koike, S. Takaduma, Characteristics of linear synchronous motor drive cycloconverter for Maglev Vehicle ML-500 at Miyazaki test track, IEEE Trans. Ind. Appl. IA-17 (1981) 533–543.
[101] J.R. Rodriguez, J. Pontt, P. Newman, R. Musalem, H. Miranda, L. Moran, G. Azamora, Technical evaluation and practical experience of high power grinding mill drives in mine applications, in: IEEE Trans. Ind. Appl., 41 3, 2005, pp. 866–873.
[102] B. Wu, J. Pontt, J. Rodriguez, S. Bernett, S. Kouro, Current source converter and cycloconverter topologies for industrial medium-voltage drives, IEEE Trans. Ind. Electr. 55 (7) (2008) 2786–2797.
[103] H.W. Weiss, Adjustable speed ac drive systems for pump and compressor applications, IEEE Trans. Ind. Appl. IA-10 (1) (1975) 162–167.
[104] R. Dirr, I. Neuffer, W. Schluter, H. Waldmann, New electronic control equipment for doubly-fed induction motors of high rating, Siemens Rev. 3 (1972) 121–126.
[105] K. Sugi, Y. Naito, P. Kurosawa, Y. Kano, S. Katayama, T. Yashida, A microcomputer based high capacity cycloconverter drive for main rolling mill, in: Proc. IPEC, Tokyo, 1983, pp. 744–755.
[106] S. Mori, E. Kita, H. Kojima, T. Sanematru, A. Shiboya, A. Bando, Commissioning of 400 MW adjustable speed pumped storage system at Okhawachi hydropower plant, in: Proc. 1995 CIGRE Symp., no. 520–04, 1995.
[107] H. Stemmler, High power industrial drives, Proc. IEEE 82 (8) (1994) 1266–1286.
[108] H. Stemmler, Active and reactive load control for converters interconnecting 50 and 16 2/3 Hz, using a static frequency changer cascade, Brown Boveri Rev. 65 (9) (1978) 614–618.
[109] T.F. Podlesak, D.C. Katsis, P.W. Wheeler, J.C. Clare, L. Empringham, M. Bland, A 150 -kVA vector controlled matrix converter induction motor drive, IEEE Trans. Ind. Appl. 41 (3) (2005) 841–847.
[110] https://www.yaskawa.com/pycprd/products/industrial-ac-drives/general-purpose-drives/u1000-industrial-matrix-drive/tab2/link20.
[111] https://www.yaskawa.com/pycprd/products/industrial-ac-drives/general-purpose-drives/ac7-matrix-drive/tab0/link02.
[112] https://www.yaskawa.com/pycprd/products/hvac-drives/drives/z1000u-matrix-drive/tab3/link32.
[113] M. Swamy, T. Kume, Present state and a Futuristic vision of motor drive technology, in: Proc. Conf Optimization of Electrical and Electronic Equipment (OPTIM), 2008, pp. XLV–LVI.
[114] http://www.yaskawa.eu.com/en/products/robotic/motoman-robots/productdetail/product/fsdrivemx1s/.
[115] M. Munzer, Economac-the first all in one IGBT module for matrix converters, in: Proc. Drives and Control Conf., Sec. 3. London, CD-ROM, 2001.
[116] C. Klumpner, F. Blaabjerg, Using reverse blocking IGBTs in power converters for adjustable speed drives, in: IEEE-IAS Conf. Rec, 2003, pp. 1516–1523.
[117] J. Itoh, I. Sato, A. Odaka, H. Ohguchi, H. Kodatchi, N. Eguchi, A novel approach to practical matrix converter motor drive system with reverse blocking IGBT, in: IEEE-PESC 2004, vol. 3. Aachen, Germany, 2004, pp. 2380–2385.
[118] J.I. Itoh, A. Odaka, I. Sato, High efficiency power conversion using a matrix converter, Fuji Electr. Rev. 50 (3) (2004) 94–98.
[119] C. Klumpner, P. Nielson, I. Boldea, F. Blaabjerg, New solutions for a low cost power electronic building block for matrix converters, IEEE Trans. Ind. Electr. 49 (2) (2002) 334–336.
[120] H.F. Blanchette, K. Al-Haddad, An efficient approach to design discrete packaging of Bidirectional resonant power switch for matrix converter applications, IEEE Trans. Power Electron. 23 (4) (2008) 2195–2200.
[121] J. Mahlein, J. Weigold, O. Simon, New concepts for matrix converter design, in: Proc. IEEE-Int. Conf. Ind. Electron., Control and Instrumentation, vol. 2, Denver, 2001, pp. 1044–1048.
[122] J. Mahlein, O. Simon, M. Braun, A matrix converter with space vector control enabling overmodulation, in: Conf. Proc. EPE'99, Lussanne, September, 1999, pp. 1–11.
[123] L. Wang, K. Sun, L. Huang, A novel method to enhance the voltage transfer ratio of matrix converter, in: Proc. 30th Ann. Meeting of IES. Busan, Korea: November 2–6, 2004, pp. 723–727.
[124] J. Chang, T. Sun, A. Wang, Highly compact ac-ac converter achieving a high voltage transfer ratio, IEEE Trans. Ind. Electr. 49 (2) (2002) 345–352.
[125] R.K. Gupta, K.K. Mohapatra, A. Somani, N. Mohan, Direct-Matrix-Converter based drive for a three-phase open-end–winding ac machine with advanced features, in: Proc IEEE-APEC 25th Annual Conf, 2010, pp. 901–908.
[126] F. Bradaschia, M.C. Cavalcanti, E. Ibarra, F.A.S. Neves, E. Bueno, Generalized pulse width modulation to reduce common voltage in matrix converters, in: Proc IEEE-ECCE, 2009, pp. 3274–3281.
[127] S. Bernett, S. Ponnaluri, R. Teichmann, Design and loss comparison of matrix converters and voltage-source converters for modern ac drives, IEEE Trans. Ind. Electr. 49 (2) (2002) 304–314.
[128] T. Matsuo, S. Bernet, T.A. Lipo, Application of matrix converter to field oriented induction motor drives, WISPERC Report, University of Wisconsin, January 1996.

[129] P.W. Wheeler, J.C. Clare, M. Apap, K.J. Bradley, Harmonic loss due to operation of induction machines from matrix converters, IEEE Trans. Ind. Electron. 55 (2) (2008) 809–816.
[130] H. Cha, P.N. Enjeti, A three-phase ac/ac high frequency link matrix converter for VSCF applications, in: IEEE-PESC 2003, vol. 4, 2003, pp. 1971–1976.
[131] S. Ratanapanaachote, H.J. Cha, P.N. Enjeti, A digitally controlled switch mode power supply, in: IEEE-PESC 2004. Aachen, Germany, 2004, pp. 2237–2243.
[132] E. Chekhet, V. Sobolev, I. Shapoval, The steady state analysis of a doubly-fed induction motor (DIFM) with matrix converter, in: Proc. EPE-PEMC 2000, vol. 5, Kosice, 2000, pp. 6–11.
[133] A.K. Dalal, P. Syam, A.K. Chattopadhyay, Use of matrix converter as slip-power regulator in a doubly-fed induction motor drive for improvement of power quality, in: Proc. IEEE Power India Conf. 2006, 10–12 April, 2006. 6 p, www.ieeexplore.ieee.org.
[134] J. Jeong, Y. Ju, B. Han, Wind power system using doubly–fed induction generator and matrix converter with simple modulation scheme, in: Proc. IEEE–PEMWA, 2009, pp. 1–6.
[135] K.M. Ciaramella, R.W.G. Bucknall, Potential Use of Matrix Converters in Marine Propulsion Applications, IMAREST, Edinburgh, 2003.
[136] C. Klumpner, P. Nielson, I. Boldea, F. Blaabjerg, A new matrix converter motor (MCM) for industry applications, IEEE Trans. Ind. Electron. 49 (2) (2002) 325–335.
[137] O. Simon, J. Mahlein, M.N. Muenzer, M. Bruckmann, Modern solutions for industrial matrix-converter applications, IEEE Trans. Ind. Electron. 49 (2) (2002) 401–406.
[138] P. Wheeler, J.C. Chan, L. Empringham, M. Bland, K.C. Kerris, A vector controlled MCT matrix converter induction motor with minimized commutation times and enhanced waveform quality, IEEE Ind. Appl. Magazine 10 (1) (2004) 59–65.
[139] C. Dufour, L. Wei, T. A. Lipo, Real-time simulation of matrix converter drives, WEMPEC Research Report. University of Wisconsin, 2005–14.
[140] H.J. Cha, P.N. Enjeti, Matrix converter-fed ASDs, IEEE Ind. Appl. Magazine 10 (4) (2004) 33–39.
[141] S. Kwak, H.A. Tolyat, An approach to fault-tolerant three-phase matrix converter drives, IEEE Trans. Energy Convers. 22 (4) (2007) 855–863.
[142] S.L. Arevalo, P. Zanchetta, P.W. Wheeler, A. Trentin, L. Empringham, Control and implementation of a matrix-converter-based AC ground power-supply unit for Aircraft servicing, IEEE Trans. Ind. Electron. 57 (6) (2010) 2076–2084.
[143] B. Ge, Q. Lei, W. Qian, F.Z. Peng, A family of Z-source matrix converters, IEEE Trans. Ind. Electron. 59 (1) (2012) 35–46.
[144] E. Karaman, M. Farasat, A.M. Trzynadlowski, A comparative study of series and cascaded z-source matrix converters, IEEE Trans. Ind. Electron. 61 (10) (2014) 5164–5173.
[145] S. Liu, B. Ge, X. Jiang, H. Abu-Rub, F.Z. Peng, Comparative evaluation of three z-source/quasi-z-source indirect matrix converters, IEEE Trans. Ind. Electron. 62 (2) (2015) 692–701.
[146] H. Nikkhajoei, A current source matrix converter for high-power applications, in: Proc. IEEE-PESC, 2007, pp. 2421–2516.
[147] B. Wang, G. Venkataramnan, Dynamic voltage restorer utilizing a matrix converter and flywheel energy storage, IEEE Trans. Ind. Appl. 45 (1) (2009) 222–231.

15

Multiphase Converters

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15.1 Introduction

Multiphase converters refer to converters with more than three phases and are the extension of three-phase converters by adding extra legs. From hardware point of view, there is least difference. However, control becomes more flexible and complex, and higher degrees of redundancies are available. Multiphase power converters have gained popularity in the last decade because of the developments in the field of high-power switching devices and computational platform such as high-speed digital signal processors and high-density field-programmable gate arrays. The major push in the area of multiphase converter is seen due to concern in developing clean transportation systems, renewable energy generation system (especially wind energy system), and developing high-reliability variable-speed electric drive system. Multiphase power converters are used in numerous applications depending upon their role so as to convert AC to DC, DC to AC, AC to AC, or DC to DC. The major applications of DC to AC converters are found in adjustable-speed drives, while AC to AC and AC to DC are employed in multiphase renewable energy generation system. Multiphase DC-DC converter finds its application in automotive industry.

Multiphase power converter (DC-AC and AC-AC) fed adjustable-speed drives offer numerous advantages when compared with three-phase drives. The major advantages offered are enhanced torque density (since in concentrated winding multiphase electric machine low-order harmonics also contribute to the torque production unlike three-phase machines where only fundamental current components generate torque), lower torque pulsation, and higher frequency pulsation. The electromagnetic torque of inverter-fed induction motor drive possesses a considerable amount of ripple especially at low speed [1,2]. This arises due to the interaction of higher-order current harmonics with fundamental air-gap flux and higher-order air-gap harmonics with fundamental current. Sixth-harmonic pulsating torque is dominant in a three-phase induction motor when inverter feeding the motor operated

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in six-step mode. In a five-phase drive the most dominant pulsating torque is a 10th harmonic and as such for n-phase it is $2n$th harmonic torque. Other advantages are lower per-leg current rating for the same voltage rating (due to lower current rating series and parallel switch combination is not required and hence cheaper solution is achieved), greater fault tolerance (machine can start and run even with loss of one or more phase supply), lower dc link current harmonics and lower harmonic losses.

Multiphase electric machines are becoming more popular in the range of medium- and high-power applications [1–5]. Considering an inverter-fed high-power electric motor with power rating exceeding the available rating of power semiconductor switches, the designer has to increase the number of feeding inverters. This implies higher number of phases on the stator of the electric motor as well. Two solutions can be sought for segmenting the power, either increase the number of phases in multiple of three (parallel-connected multiple three-phase inverters) or increase the number of legs of inverter with each leg handling a power of P/n (P is the total power, and n is the number of phases). The design solutions are shown in Fig. 15.1. The solutions given in Fig. 15.1B have n number of parallel-connected three-phase inverters each carrying power of P/n. The supplied motor has multiple three-phase windings with separate neutral points. The major advantage of these off-the-shelf standard three-phase inverters is to supply the motor with each inverter handling lower amount of power. However, the major issue of this drive topology is the circulating current due to the voltage mismatch of each three-phase inverter. The electric motor in this case is called asymmetrical or split-phase motor. This solution is preferred and most widely used in industries because of the fact that the three-phase system solution is well proved and a mature technology:

Solution of Fig. 15.1C, in contrast to the previous solution, works with a single inverter of n-phases supplying electric motor of n-phase. Each phase or leg now handles P/n power, and the circulating current is absent. The electric motor in this case is called symmetrical n-phase motor. This solution is also employed in high-power marine drive applications [6].

Reliability and fault tolerance are other driving forces leading to the development of multiphase system. Due to high phase number, fault tolerance is inherently guaranteed, which is of high importance in safety critical applications such as ship propulsion, more electric aircrafts, electric vehicles, and industrial setup where production loss is critical such as oil and gas plants and military. The multiphase motor drive guarantees continuous operation, however, with degraded performance under fault conditions. The higher the phase number, the better is the performance during faults. This make them highly attractive in applications mentioned above [7,8].

According to classical electric machine theory, the air-gap flux harmonic content improves and becomes close to sinusoidal with the increase in the number of phases. The improved flux density waveform leads to: (i) reduced rotor losses due to flux pulsation and eddy currents (this has importance for high-speed permanent magnet machines since the eddy current losses are very high at high speed in such kind of machines) and (ii) improved torque quality with reduced amplitude of torque pulsation that occurs at higher frequency (this is very important when machine is subjected to high distorted current, and limits are enforced on the maximum allowable torque pulsation).

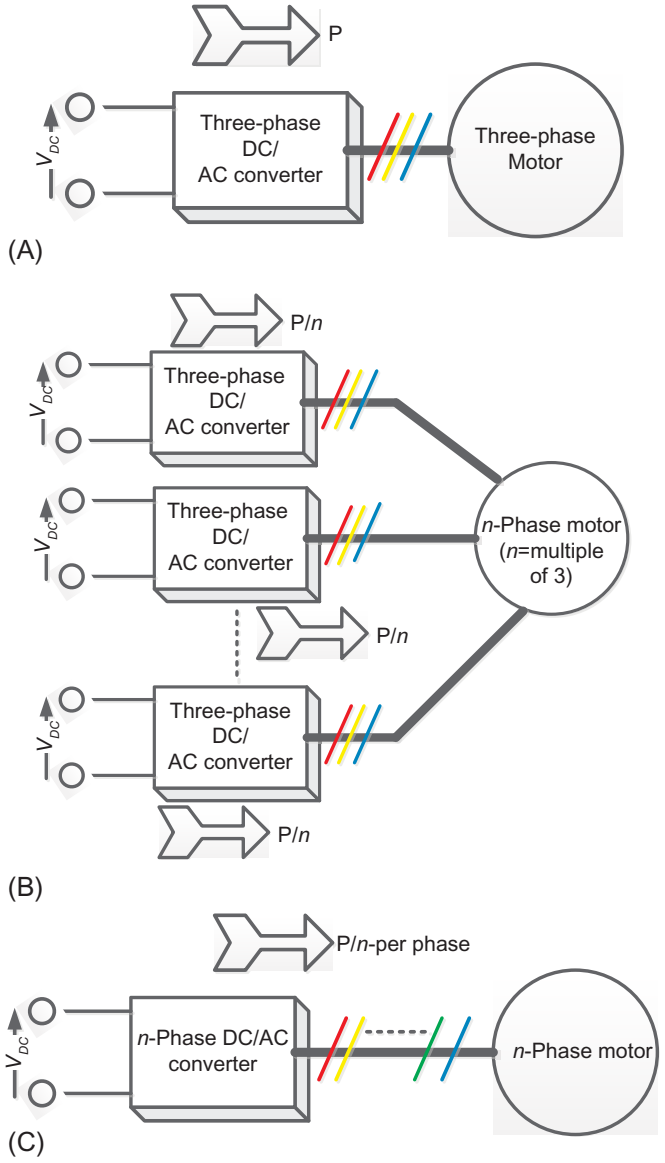


FIG. 15.1 (A) Three-phase drive, (B) multiple three-phase drive, and (C) multiphase drive.

Multiphase generators, specially five phases and more, have started to find a slot in the market due to their advantages over three-phase counterpart [9,10]. This multiphase system could be more suitable for direct drive wind energy, microturbines, and electric vehicle applications since the need for gears can be minimized. Multipulse rectifiers are employed, which have

the ability to reduce the line current harmonic distortion and normally do not require any LC filters or power factor improvement devices. Multipulse DC can be obtained either by increasing the number of phases of the converter or by the use of phase-shifting transformer along with special secondary winding connections in the conventional six-pulse rectifiers. In drive application, the use of phase-shifting transformer provides an effective means to block common-mode voltages generated by the rectifier and inverter, which would otherwise appear on motor terminals, leading to a premature failure of machine winding insulation. Normally AC-DC converters are classified into power factor control rectifiers operated at high switching frequency and line-commutated rectifiers (uncontrolled or controlled) operated at power frequency or generated frequency. The multiphase line-commutated converter normally offers simple control, simple construction, and low cost but suffers from poor input power factor, low input current THD, and unidirectional current flow. The shortcoming of line-commutated rectifiers is overcome by the use of high-switching-frequency PWM rectifiers, voltage-source rectifiers, or current-source rectifiers, but the switch current and voltage limitation may restrict the use of PWM rectifiers in high-power applications.

Multiphase DC-AC voltage-source inverter is obtained from three-phase voltage-source inverter by adding extra legs (each leg has two switches in two-level inverter and a higher number of switches for multilevel inverter). The two switches of the same leg are complimentary in operation (i.e., when upper switch is on, the lower switch must be off and vice versa). The power switches can assume only two states, that is, *on* (called level 1) or *off* (called level 0). Hence, as such for n-phase inverter, there can be 2^n number of switching states. Considering a three-phase inverter, the number of switching states are 8, and, for example, for a nine-phase inverter, the number of switching states are $2^9 = 512$ [5]. It is seen that the number of switching states increases significantly with the increase in the number of phases or legs. Higher numbers of switching states offer flexibility in devising control techniques. Thus, multiphase inverter control has several degrees of flexibility in control. Multiphase inverter can be controlled using different PWM techniques such as carrier-based sinusoidal PWM, harmonic injection PWM, selective harmonic PWM, hybrid PWM, and space-vector PWM. Each method can produce different output magnitudes. Simple carrier-based PWM for multiphase inverters works exactly the same as for three-phase inverters. The maximum possible output phase-to-neutral voltage is 0.5 V_{DC}, where V_{DC} is DC-link voltage magnitude for multiphase inverter [1]. However, the output phase-to-neutral voltage magnitude varies for different phase numbers when using space-vector PWM. Nevertheless, the output phase-to-neutral voltage of multiphase inverters is less than that of a three-phase inverter. Multiphase inverter space vectors are transformed into multiple orthogonal planes, and control is implemented in order to regulate each plane vectors. In multiphase variable-speed drives (with distributed winding multiphase machine), torque is controlled only from one plane vector (d-q), and the rest of the plane vectors produce distortion and hence need to be minimized using PWM techniques. When concentrated winding multiphase machines are supplied using multiphase voltage-source inverters, all plane vectors are used to enhance the torque production. This is a unique feature of concentrated winding multiphase machine not available in three-phase machines. When implementing high-performance control such as vector control and direct torque control, higher control flexibility is available, and different solutions can be implemented.

Multiphase AC-AC converter more popularly known as multiphase matrix converter (MPMC) is also formulated by adding extra legs in three-phase matrix converter configuration. They are classified as direct matrix converters (DMC) and indirect matrix converters (IMC). Each converter leg has three bidirectional power switches each connected to one phase of the utility grid system, and at the output, load is connected. The input is fixed voltage and fixed frequency supply, while the output is of variable voltage and variable frequency. There are configurations where the number of input phases is three while the output phase are more than three and vice versa [4,5]. The multiphase matrix converter encompasses the advantages of three-phase matrix converters and multiphase systems. The major application areas are envisaged in multiphase wind energy system. A matrix converter can be seen as an array of $m \times n$ bidirectional power semiconductor switches that can transform m-phase fixed voltage and fixed frequency input to n-phase variable voltage and variable frequency output without intermediate DC conversion stage. The input side of a matrix converter is voltage fed, while the output side is current fed, and hence, an inductive filter is required at the output side, and a capacitive filter is used at the input side. As the load is itself of inductive nature, the requirement of output filter diminishes. The size of the input filter used in matrix converter is significantly smaller than an equivalent voltage-source inverter.

Considering an $m \times n$ matrix converter, the number of switching states is $2^{m \times n}$. Large numbers of switching states are produced; however, not all of them are useful. Due to the nature of input (being voltage source) and output (being current source), the input should not short-circuited, and the output should not be open-circuited. As a consequence, only one switch in each leg conducts at one instant of time, and hence, a usable number of switching states are m^n. In matrix converter, the output (sinusoidal) is formed from input (sinusoidal), and hence, output can assume any level depending upon the instantaneous value of the input. This makes the switching logic of matrix converter quite complex. The output voltage of a three-phase input and three-phase output matrix converter is 86.6% of the input voltage. The output-voltage magnitude reduces for higher phase number of outputs; for example, for a three-phase input and five-phase output matrix converter, it is 78.86% [11], and this value decreases further with increase in the output number of phases. The output voltage becomes higher than the input for $m \times n$ matrix converter

for $m > n$; for example, for a five-phase input and three-phase output, it is 104.4%, and this value further increases as m is increased [4,12].

Multiphase matrix converters are constructed from bidirectional power switches that are realized in the same way as a three-phase matrix converter. The modulation strategies are complex and can be built upon the concept of three-phase matrix converter. However, significant challenges exist in obtaining proper modulation technique for a multiphase matrix converter. Some modulation strategies discussed in the literature are carrier-based PWM, space-vector PWM, and direct-duty-ratio-based PWM [13–19].

Multiphase matrix converters find its application in wind energy generation [20], power system [21,22], and ship propulsion [23]. When used in multiphase energy generation, usually the input side of the matrix converter is of higher phase, and the output side is three-phase connected to either utility grid or feeding isolated load. A 27-phase input and 3-phase output matrix converter of 100 MW power rating is presented in [24,25].

Present-day advancement in powering processors invariably uses multiphase buck converter topology because of higher output current and low-voltage requirement. Single-phase buck converter works well for low-voltage applications with currents up to 25 A. Higher filtering requirement and efficiency issue limits the use of single-phase topology in applications such as voltage regulator module (VRM). Interleaving as technically known reduces ripple currents at the input and output. A multiphase buck converter reduces considerably the i^2R current power dissipation in the controlled switches and inductors. The distribution of current in various paths in a multiphase converter reduces the current magnitude through the switches, thereby reducing the switching losses. The output filter requirement decreases in a multiphase implementation due to the higher frequency of ripple current as a result of ripple current cancelation in the power stage for each phase. The single-phase implementation has much higher ripple content. Load transient performance is also better because of the reduction in energy stored in each output inductor. The lower the ripple current is, the less the perturbation will be. The input capacitors supply all the input current to the buck converter if the input wire to the converter is inductive. Improvement in multiphase topologies and their control strategies promise improved performance compared to the conventional multiphase buck converter.

This chapter is organized into five different sections covering the topologies, operation, and control of different types of multiphase power converters. Section 15.2 describes the types and classifications of different multiphase power converters. Section 15.3 is dedicated to AC-DC converters considering multiphase and multipulse output. Section 15.4 is devoted to DC-AC converters especially focusing on five-phase and seven-phase voltage-source inverter. Section 15.5 covers the description of multiphase AC-AC converters, and multiphase DC-DC converters are discussed in Section 15.6.

15.2 Types and Topologies of Multiphase Converters

The requirements for the current and voltage continue to increase with an increase in power level, and systems become more and more complex. The amount of current/voltage of power source to meet such requirements usually needs a combination of several power controllers to improve the thermal stress of the individual power components. The driving mechanism for this combination leaves one with two choices: single phase or multiphase.

Multiphase converters reduce the input and output current ripples by interleaving the two or more stages of power converters. By increasing the phase number, the output-voltage ripple and the input capacitor size can be curtailed without increasing the switching frequency of the power devices. Load dynamic performance is significantly improved during transients due to lower-output-voltage ripple and smaller output inductors. The low switching losses and driver circuit losses of power semiconductor devices at relatively low switching frequency and the reduced power losses due to equivalent series resistance (ESR) of the capacitors help achieve overall high efficiency of converters. For multioutput applications, multiphase converters may also provide the benefit of smaller input side capacitors.

Single-phase versus multiphase converters are as follows:

(1) Single-phase converters work well for low voltages and up to certain amount of current say about 25 A, but power dissipation and efficiency start to become an issue at higher currents. One suitable approach is to develop multiphase converters [26].
(2) The output filter requirements decrease in multiphase implementation due to the reduced current in the power stage for each phase. Compared with single-phase approach, the inductance and inductor size are drastically reduced because of lower average current and lower saturation current.
(3) Ripple current cancelation in the output filter stage results in a reduced ripple voltage across the output capacitor compared with single-phase approach. This is another reason why a multiphase converter is preferred.
(4) Load transient performance is improved due to the reduction of energy stored in each output inductor. The reduction in ripple voltage as a result of current cancelation contributes to minimal output-voltage overshoot and undershoots because many cycles will pass before the loop responds. The lower the ripple current is, the less the perturbation will be.

Like single-phase or three-phase converters, multiphase converters are classified as AC-DC, DC-AC, DC-DC, and AC-AC converters. Multiphase converters are simple extension of three-phase converters. As far as hardware is concerned, there

is not much difference. However, the control complexity increases manyfold with the increase in the number of phases. There are further classifications in these converters. The classification of multiphase converters is shown in respective section.

15.2.1 Multiphase AC-DC Converters

A significant amount of work is done on developing novel topologies of multipulse AC-DC converters since they have huge potential applications for unidirectional and bidirectional power flow starting from six pulses to a large number of pulses. The major advantage of adopting a higher pulse number is the current ripple reduction.

The novel configurations in multiphase AC-DC converter were developed of unidirectional and bidirectional topologies with three or more number of phases. Classification of multiphase AC-DC converters is shown in Fig. 15.2, which is based on power flow, number of pulse used, isolated and nonisolated topologies, and various techniques used to improve AC current profile and output DC voltage waveform [27]. Based on the application and requirements, some systems require unidirectional power flow, and some require bidirectional power flow.

Unidirectional systems use diode rectifiers and transformer circuit configurations in isolated and nonisolated topologies. The unidirectional topologies have configurations of six pulses and its multiple. If the voltage difference is more between input and output, then isolated configuration is useful, and if the difference is less, nonisolated topologies are used. However, these are further classified as bridge and full-wave rectifiers. These types of full-wave multipulse converters (MPC) can also be further classified whether it uses double star or tapped polygon transformer secondary to create twelve phases to feed full-wave diode rectifiers. Both configurations have their own merits and demerits, but both MPC configurations show the same performance in terms of device and transformer utilization.

On the other hand, the bidirectional AC-DC converters have the power flow from AC mains to DC output or vice versa and normally use thyristors with phase angle control to obtain wide varying DC output voltages. These MPCs use multiple winding transformers to generate higher number of the phases. Like unidirectional, these MPCs are also divided as isolated and nonisolated. These are mainly used to feed DC motor drives and synchronous motor drives.

15.2.2 Multiphase DC-DC Converters

Multiphase topologies can be configured as a step-down (buck), step-up (boost), buck boost, and even forward converter. A multiphase DC/DC converter according to the present invention includes a plurality of DC/DC converters whose outputs are connected in common to supply electric power to a load and a load state detection portion that detects a state of the load connected to the plurality of DC/DC converters and outputs a detection result. Multiphase DC-DC converters classification is shown in Fig. 15.3.

15.2.3 Multiphase DC-AC Converters

Multiphase DC-AC converters are the main source of multiphase adjustable-speed drives. The major driving force behind the adoption of multiphase motor drive is due to the power segmentation in large number of converter legs. The power switching devices have limited voltage- and current-handling capabilities. Hence, when used in high-power application, series-and parallel combination of devices are required. This is cumbersome solution because of dynamic voltage sharing problem among the series-/parallel-connected power switching devices. Better solution is obtained when the power per phase or per leg is reduced by increasing the number of phases or number of legs, and this is termed as multiphase DC-AC

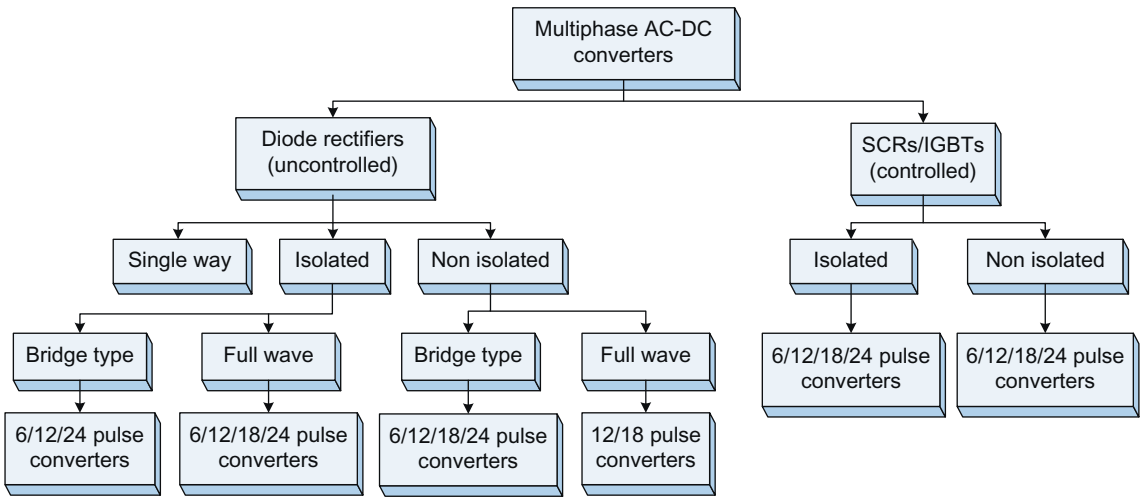


FIG. 15.2 Multiphase AC-DC converter classification.

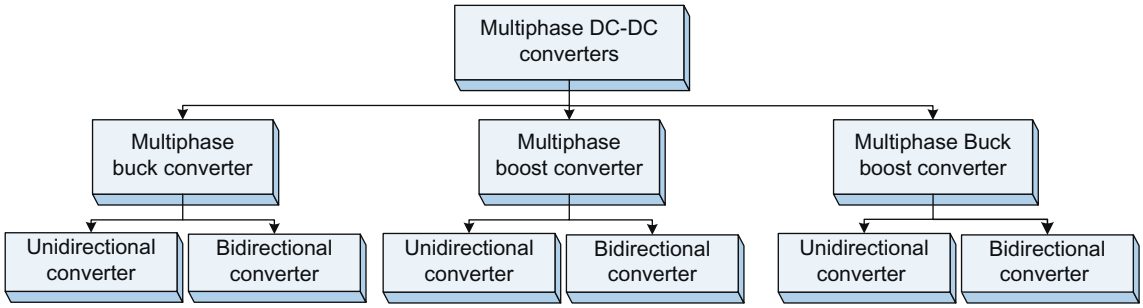


FIG. 15.3 Multiphase DC-DC converter classification.

inverters. Multiphase DC-AC inverters are simple in design as they are simple extension of three-phase DC-AC inverter. However, they offer large degree of switching redundancies and hence great flexibility in control. Although control becomes complex, the performance is improved manifold. Multiphase DC-AC inverters can be built in the same topologies as that of their three-phase counterparts and hence have the same calcifications and types. Multiphase AC-DC converters normally classified as shown in Fig. 15.4.

First version of multiphase inverter technology is five-phase VSI fed to star-connected five-phase load. Five-phase VSI configuration found application for five-phase induction machine and synchronous machine drives. Six-phase inverter configuration was built with two two-level standard three-phase VSIs, with two separate DC sources fed to dual three-phase induction motor. Seven-phase VSI fed to star-connected seven-phase load based on multiple space-vector modulation and seven-phase VSI configuration found applications for seven-phase permanent magnet synchronous and synchronous reluctance motor drives. Fig. 15.5 shows simple five-phase induction motor drive.

Multiphase inverters are also classified as cascaded H-bridge, diode clamped, and flying capacitor topologies. They can also be built in hybrid configuration. Multiphase impedance-source inverters (ZSI) and quasi impedance-source inverters (qZSI) are also reported in the literature [28]. ZSI and qZSI are special inverters that have the capability of boosting the source voltage and inverting DC to AC simultaneously. The boosting can be as high as 200%–300%. They are popular in solar PV applications

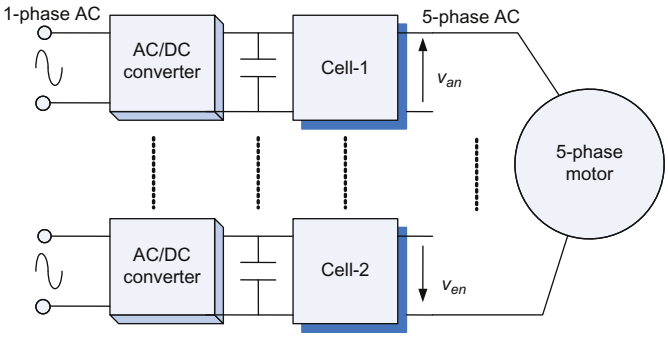


FIG. 15.5 Simplified five-phase drive.

since boosting and inversion is done in a single stage. Multiphase ZSI/qZSI is used to feed multiphase motor drives.

15.2.4 Multiphase AC-AC Converters

Multiphase AC-AC converters are generally classified as AC voltage controllers, matrix converters, and cycloconverters. Fig. 15.6 shows various topologies of multiphase AC-AC converters. AC voltage regulators are further classified as phase-controlled converters and fully controlled voltage converters.

Three-phase cycloconverters are of several types. For example, there are the 3-pulse cycloconverters, 6-pulse cycloconverters, and 12-pulse cycloconverters. Typically, the three-pulse converter is built with the three single, and the six-pulse converter is generally the combination of two three-pulse converters and

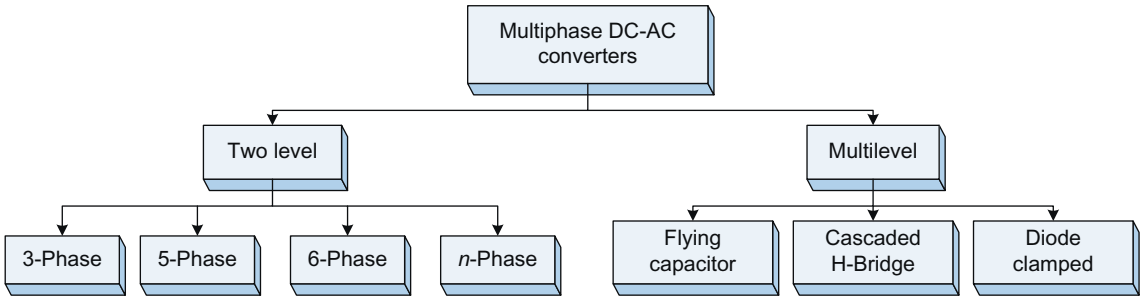


FIG. 15.4 Multiphase DC-AC converter classifications.

so on. The 12-pulse converter is obtained by connecting two six-pulse configurations in series and appropriate transformer connections for the required phase shifted. Multiphase AC-AC converter classification is shown in Fig. 15.6. By using the knowledge of constructing a DC-modulated single-stage AC/AC converter, a multistage AC/AC converter can be easily obtained. Examples with complex structures are Luo converter, superlift Luo converter, and multistage cascaded boost converter. Using the same technique, one can construct DC-modulated multiphase AC/AC converters where they are classified as multiphase AC/AC buck, boost, and buck-boost converter.

Cycloconverters are broadly classified as naturally commutated and forced commutated. The later one is also known as matrix converter. Multiphase matrix converters are in study and are being studied in detail [4]. Fig. 15.7 shows some of the possible configurations of frequency changers. The one

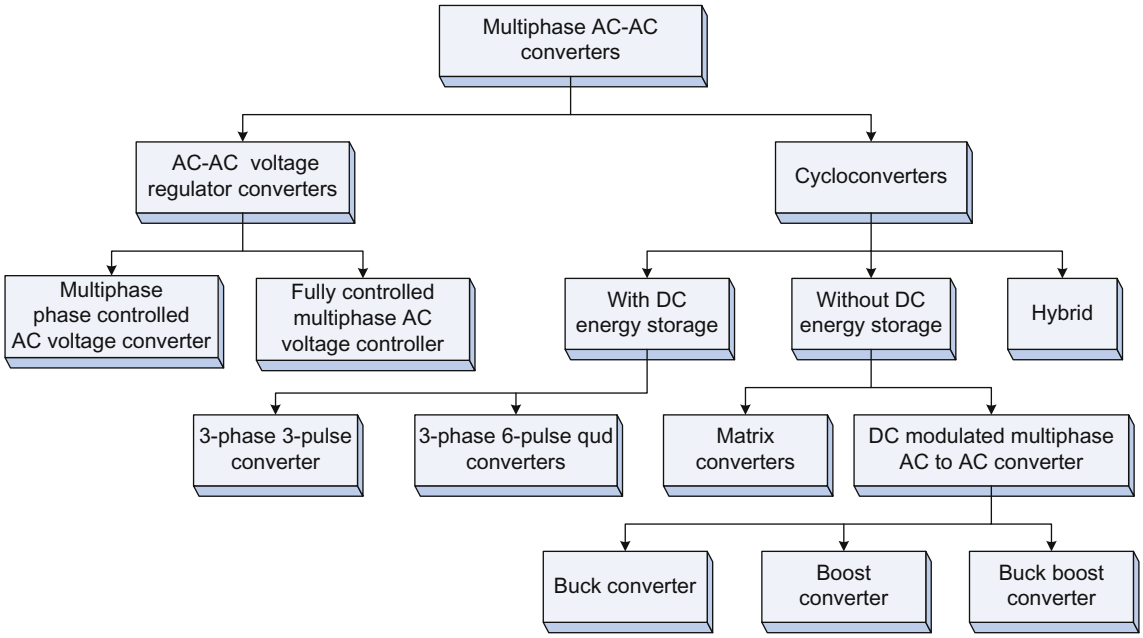


FIG. 15.6 Multiphase AC-AC converter classification.

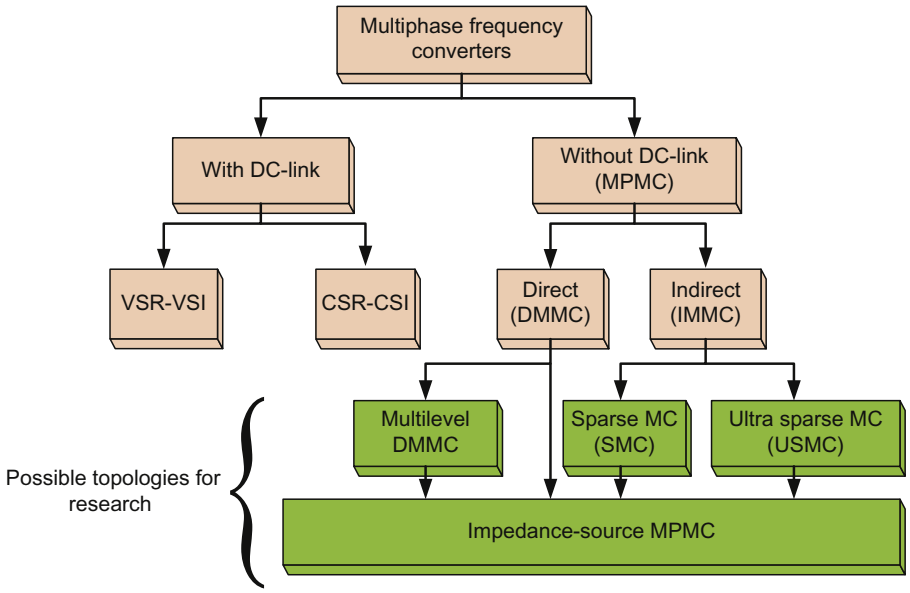


FIG. 15.7 Multiphase frequency changers. *VSR*, voltage source rectifier; *VSI*, voltage source inverter; *CSR*, current source rectifier; *CSI*, current source inverter; *MPMC*, multiphase matrix converter; *DMMC*, direct multiphase matrix converter; *IMMC*, indirect multiphase matrix converter; *SMC*, sparse matrix converter; *USMC*, ultra sparse matrix converter.

with a DC link is also commonly known as back-to-back (B2B) topology. Although B2B converter does the AC-AC conversion, it is sort of a paradigm to classify the topologies without the DC link under AC-AC converters. Also, the figure shows the possibility of research in the field of multiphase matrix converters.

15.3 Multiphase Multipulse AC-DC Converters

Solid-state AC-DC converters are widely used in a number of applications such as adjustable-speed drives (ASDs), high-voltage DC (HVDC) transmission, and electrochemical processes such as electroplating, telecommunication power supplies, battery charging, uninterruptible power supplies (UPS), high-capacity magnet power supplies, high-power induction heating equipment, aircraft converter systems, plasma power supplies, and converters for renewable energy conversion systems. These converters, which are also known as rectifiers, are generally fed from three-phase AC supply in power rating above few kilowatts. They exhibit the problems of power quality in terms of injected harmonics, resulting in poor power factor, AC voltage distortion, and rippled DC outputs. Because of these problems in AC-DC conversion, several standards and guidelines are laid down, which are to be referred by designers, manufacturers, and users. Therefore, various methods are used to mitigate these problems in AC-DC converters. Normally, filters are recommended in already existing installations, which may be passive, active, or hybrid types depending upon rating and economic considerations. These filters have been developed from small to large power ratings to reduce the power quality problems of AC-DC converters. However, in some cases, the ratings of these filters are close to the converter rating, which not only increases the cost but also increases the losses and component count, resulting in reduced reliability of the system. However, in future installations, it is preferred to modify the converter structure at design stage either using active or passive (magnetic) wave shaping of input currents or using multipulse AC-DC converters by using multiphase system or different connections of standard three-phase six-pulse AC-DC converters. At higher power level, generally, multiphase system is preferred. It reduces the ripples in the line current and load voltages drastically, and thus, EMI reduces, and the harmonic filter requirements also become very nominal.

15.3.1 Five Phase Uncontrolled Full Wave Bridge Rectifier

The circuit diagram of a simplified five-phase (ten pulses) uncontrolled rectifier consisting of 10 diodes (D1–D10) is shown in Fig. 15.8, where v_{an}, v_{bn}, v_{cn}, v_{dn}, and v_{en} are the supply phase voltages having peak value of V_m given by Eq (15.1):

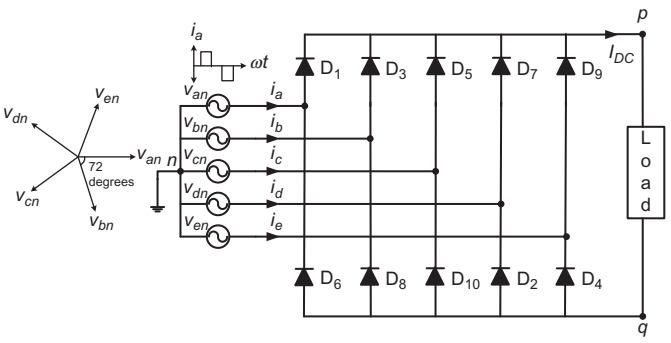


FIG. 15.8 Five-phase full-wave uncontrolled rectifier circuit.

$$\begin{aligned} v_{an} &= V_m \sin(\omega t) \\ v_{bn} &= V_m \sin(\omega t - 2\pi/5) \\ v_{cn} &= V_m \sin(\omega t - 4\pi/5) \\ v_{dn} &= V_m \sin(\omega t - 6\pi/5) \\ v_{an} &= V_m \sin(\omega t - 8\pi/5) \end{aligned} \tag{15.1}$$

The diodes are assumed ideal and are numbered according to their conduction sequence 1,2- ,3- 3,4- 4,5- 5,6- 6,7- 7,8- 8,9- 9,1.

The line voltages for adjacent phases will be different from that of nonadjacent phases. The line voltages for adjacent and nonadjacent phases can be obtained from the respective phasor diagrams shown in Figs. 15.9 and 15.10, respectively, as follows:

For adjacent phases,

$$\begin{aligned} v_{ab} &= v_{an} - v_{bn} \\ v_{ab} &= V_m \sin(\omega t) - V_m \sin(\omega t - 2\pi/5) \\ v_{ab} &= 2V_m \sin(\pi/5) \cos(\omega t - \pi/5) \\ &\left\{ \because \sin\alpha - \sin\beta = 2\cos\left(\frac{\alpha+\beta}{2}\right)\sin\left(\frac{\alpha-\beta}{2}\right) \right. \\ v_{ab} &= 1.1755\, V_m \sin(\omega t + 3\pi/10) \end{aligned} \tag{15.2}$$

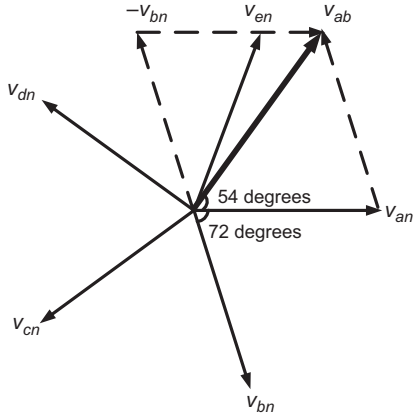


FIG. 15.9 Phasor diagram of the line voltages of adjacent phases.

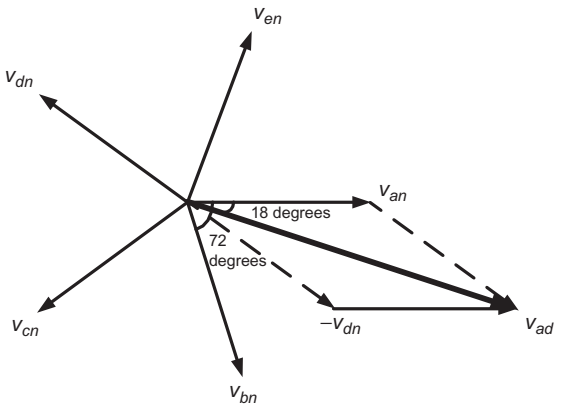


FIG. 15.10 Phasor diagram for the addition of nonadjacent phases.

For nonadjacent phases,

$$\begin{aligned} v_{ad} &= v_{an} - v_{dn} \\ &= V_m \sin(\omega t) - V_m \sin(\omega t - 6\pi/5) \\ &= 2V_m \sin(3\pi/5) \cos(\omega t - 6\pi/10) \\ v_{ad} &= 1.9021 V_m \sin(\omega t - \pi/10) \end{aligned} \tag{15.3}$$

Fig. 15.11A shows the waveforms of the maximum and minimum value of phase voltage in different intervals. The maximum phase voltage V_{pn} and minimum phase voltage V_{qn} described by Eq (15.4) will appear at the output terminals p and q. Both the diodes in the same leg never conduct simultaneously, which avoids direct short circuit in the leg. In the upper leg, the diodes (odd numbered) having its anode connected with phase voltage of highest value among phases will conduct. Similarly, in the bottom leg, the diodes (even numbered) having its cathode connected with lowest phase voltage will conduct at any instant of time:

$$\begin{aligned} V_{pn} &= \max(v_{an}, v_{bn}, v_{cn}, v_{dn}, v_{en}) \\ V_{qn} &= \min(v_{an}, v_{bn}, v_{cn}, v_{dn}, v_{en}) \end{aligned} \tag{15.4}$$

The output-voltage waveform shown in Fig. 15.11B is a 10-pulse waveform appearing across the load. For a purely resistive load, the waveform of the line current i_a shown in Fig. 15.11C has two humps per half cycle of the supply frequency. The other four line currents, i_b, i_c, i_d, and i_e, have the same waveform as i_a but lag from i_a by $2\pi/5$, $4\pi/5$, $6\pi/5$, and $8\pi/5$ radians, respectively. The average and rms value of output voltage at load can be calculated as

$$V_{DC} = \frac{1}{2\pi/10} \int_{\frac{\pi}{2}}^{\frac{7\pi}{10}} 1.902 V_m \sin(\omega t - \pi/10)\, d(\omega t) \tag{15.5}$$

$$V_{DC} = 1.87087 V_m$$

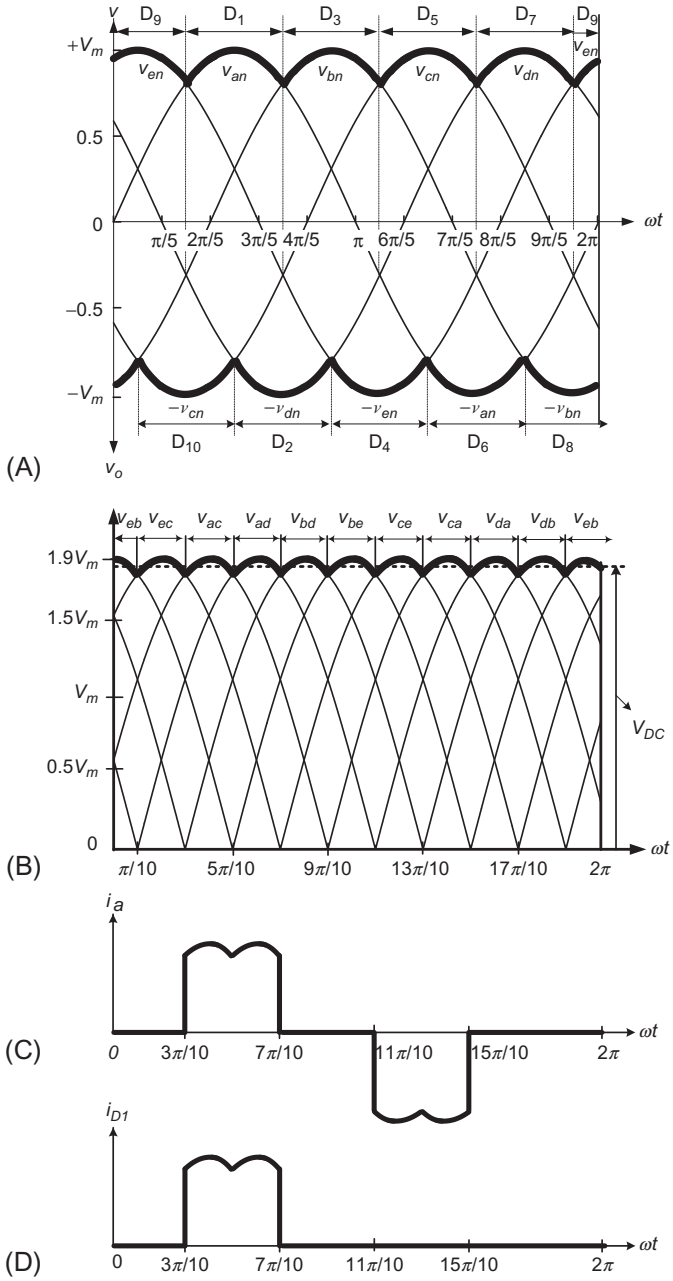


FIG. 15.11 (A) Phase voltages w.r.t p and q points, (B) output voltage across the load, (C) phase "a" current, and (D) diode current.

$$V_{rms} = \sqrt{\frac{1}{2\pi/10} \int_{\frac{\pi}{2}}^{\frac{7\pi}{10}} [1.902 V_m \sin(\omega t - \pi/10)]^2 d(\omega t)} \tag{15.6}$$

$$V_{rms} = 1.87107 V_m$$

For a resistive load, the harmonics of the output voltage can be found by using Fourier series analysis. To find the Fourier coefficients, we integrate v_{be} from $-\pi/10$ to $+\pi/10$. Considering the

half-wave symmetry, the Fourier coefficients will be calculated as follows:

$$b_n = 0 \tag{15.7}$$

$$a_n = \frac{1}{\pi/10}\int_{\frac{-\pi}{10}}^{\frac{\pi}{10}} 1.9021 V_m \cos(\omega t)\cos(n\omega t)\, d(\omega t)$$

$$= 6.067 V_m \left\{ \frac{(n+1)\sin\left[(n-1)\frac{\pi}{10}\right] + (n-1)\sin\left[(n+1)\frac{\pi}{10}\right]}{(n^2-1)} \right\}$$

$$a_n = \frac{12.134 V_m}{(n^2-1)}\left\{ n\sin\frac{n\pi}{10}\cos\frac{\pi}{10} - \cos\frac{n\pi}{10}\sin\frac{\pi}{10} \right\} \tag{15.8}$$

If the frequency of the source voltage is f, the output voltage has harmonics at $10f$, $20f$, $30f$ …etc. Eq. (15.8) is simplified as

$$a_n = -\frac{12.134 V_m}{(n^2-1)}\left\{ \cos\frac{n\pi}{10}\sin\frac{\pi}{10} \right\}$$
$$a_n = -\frac{3.75 V_m}{(n^2-1)}\cos\frac{n\pi}{10} \tag{15.9}$$

The DC component is found by putting $n = 0$ in Eq. (15.9), and its value is

$$V_{DC} = \frac{a_0}{2} = 1.87 V_m \tag{15.10}$$

This is the same value as calculated in Eq. (15.5). The Fourier series of the load voltage can be written as

$$v_L(t) = \frac{a_0}{2} + \sum_{n=10,20,\cdots}^{\infty} a_n \cos(n\omega t) \tag{15.11}$$

After substituting the values of the coefficients, we obtain

$$v_L(t) = 1.87 V_m \left(1 - \sum_{n=10,20,\cdots}^{\infty} \frac{2}{(n^2-1)}\cos\frac{n\pi}{10}\cos n\omega t \right) \tag{15.12}$$

$$v_L(t) = 1.87 V_m \left(1 + \frac{2}{99}\cos 10\omega t - \frac{2}{399}\cos 20\omega t + \cdots \right) \tag{15.13}$$

Fig. 15.12 shows the load voltage harmonics profile. Since each diode conducts one fifth of the time, the average diode current is given by Eq. (15.14).

$$I_{D,avg.} = \frac{1}{2\pi}\left[\int_{\frac{3\pi}{10}}^{\frac{7\pi}{10}} I_{DC}\, d(\omega t) \right] = 0.2 I_{DC} \tag{15.14}$$

Eq. (15.14) indicates that a five-phase rectifier will have switches with lower ratings as compared with the three-phase

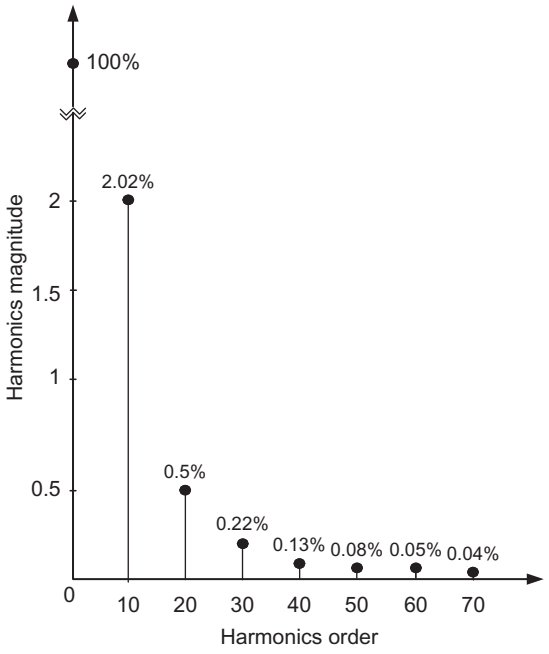


FIG. 15.12 Harmonics profile of output voltage.

counterpart, provided that both are feeding the same load as average value of switch current in three-phase system is 33.33% and in this case it is 20% [9,10]. The input phase current can be expressed as

$$i_s = \sum_{n=1,3,5....}^{\infty} \frac{4 I_{DC}}{n\pi}\sin\frac{n\pi}{5}\sin(n\omega t) \tag{15.15}$$

The fundamental component of input current is

$$i_{s1} = 0.7484 I_{DC}\sin(\omega t) \tag{15.16}$$

The rms value of the fundamental component of input current is

$$I_s = \sqrt{\frac{1}{\pi}\int_{\frac{3\pi}{10}}^{\frac{7\pi}{10}} I_{DC}^2\, d\omega t} = \sqrt{\frac{2}{5}} I_{DC} \tag{15.17}$$

Problem 15.1 A five-phase bridge rectifier delivers 60 A current at a voltage of 317.5 V to a purely resistive load. If the frequency of the source is 60 Hz, determine the following:

(a) Efficiency of rectification
(b) Form factor
(c) Ripple factor
(d) Peak inverse voltage (PIV) of each diode
(e) Peak current through a diode

Solution Since $V_{DC}=1.87087V_m$ and $V_{rms}=1.87101V_m$ and also $I_{DC}=V_{DC}/R$ and $I_{rms}=V_{rms}/R$,

(a) Efficiency of rectification $\eta=\dfrac{P_{ac}}{P_{DC}}=\dfrac{\frac{V_{rms}^2}{R}}{\frac{V_{DC}^2}{R}}=\dfrac{(1.87107)^2}{(1.87087)^2}=99.97\%$

(b) Form factor $FF=\dfrac{Vrms}{V_{DC}}=\dfrac{1.87107}{187087}=100.011\%$

(c) Ripple factor $RF=\sqrt{FF^2-1}=\sqrt{(1.00011)^2-1}=1.483\%$

(d) Peak inverse voltage of each diode $=1.902V_m$

Also, since $V_{DC}=1.87087\ V_m$ and peak value of phase voltage, $V_m=\dfrac{V_{DC}}{1.87087}=\dfrac{317.5}{1.87087}=169.70\,\text{V}$

Hence, $PIV=1.902\times169.70=322.78\,\text{V}$

(e) The average DC current through each diode is

$$I_{DC(Diode)}=\frac{I_{DC}}{5}=\frac{60}{5}=12\,\text{A}$$

$$\text{Also, } I_{DC(Diode)}=\frac{4}{\pi}\int_0^{\frac{\pi}{10}} I_m\cos\omega t\,d\omega t$$

$$I_{DC}=0.19673I_m$$

$$I_m=\frac{I_{DC}}{0.19673}=\frac{12}{0.19673}=61\,\text{A}$$

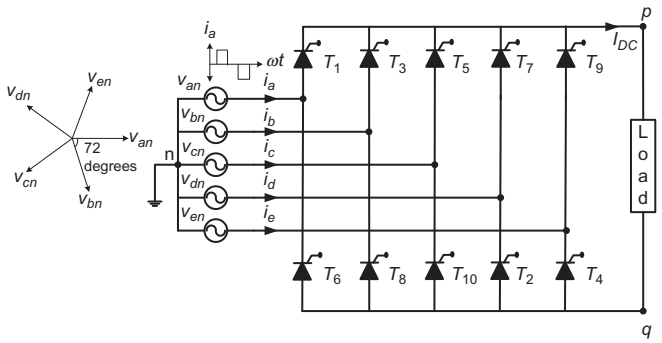


FIG. 15.13 Five-phase full-wave bridge rectifier basic circuit.

15.3.2 Five-Phase Controlled Full Wave Bridge Rectifier

Whenever a diode is in forward-biased condition, it conducts, but a thyristor (or controlled switch) requires a triggering signal for its conduction. If all the diodes of a 10-pulse full-wave uncontrolled converter are replaced by controlled switches (thyristors), it becomes a controlled converter. Fig. 15.13 shows the basic power circuit of a fully controlled 10-pulse 5-phase AC-DC converter. In this case, the thyristors are switched at an interval of 36 degrees sequentially as shown in Table 15.1. When T_1 and T_2 are conducting v_{an} and v_{bn} voltages with respect to neutral appear at the load, that is, $v_{ad}=v_{an}-v_{dn}$, which is the line voltage V_L ($v_{ad}=1.9021V_m\sin(\omega t-\pi/10)$). At $\omega t=\pi/2+\alpha$, T_1 is commutated, as on this instant of time $v_{bn}>v_{an}$, and the load current is transferred from T_1 to T_3. There are 10 voltage pulses, and the instantaneous output voltage may become negative for an RL load, but the V_{dc} will always have positive value, except for an active (RLE) load. It should be noted that the line voltage corresponding to the nonadjacent phase voltages is only appearing across the load. AC voltages applied to the rectifier is given by Eq. (15.1).

The delay angle reference is taken from the point the thyristor would begin to conduct if it were a diode. Thus, the delay angle is an interval from the thyristor being forward-biased and till the gate signal is applied. The corresponding waveforms are shown in Fig. 15.14A–H [9,10]. Since each voltage pulse corresponds to the line voltage and it appears for 1/10th period of the cycle $2\pi/10$, the average output voltage corresponding to v_{ad} shown in Table (15.1) is given by

$$V_{DC}=\frac{1}{2\pi/10}\int_{\frac{5\pi}{10}+\alpha}^{\frac{7\pi}{10}+\alpha}1.902V_m\sin(\omega t-\pi/10)\,d(\omega t)$$

$$V_{DC}=\frac{5\times1.902V_m}{\pi}[-\cos(\omega t-\pi/10)]_{\frac{5\pi}{10}+\alpha}^{\frac{7\pi}{10}+\alpha} \tag{15.18}$$

$$V_{DC}=1.87V_m\cos\alpha$$

TABLE 15.1 Thyristor firing instants and output voltage across the load

Time interval	Thyristor fired	Conducting thyristor	Output voltages across load
$[\pi/10+\alpha,\ 3\pi/10+\alpha]$	T_{10}	T_9 and T_{10}	$v_o=v_{ec}=1.902\,V_m\sin(\omega t+3\pi/10)$
$[3\pi/10+\alpha,\ 5\pi/10+\alpha]$	T_1	T_{10} and T_1	$v_o=v_{ac}=1.902\,V_m\sin(\omega t+\pi/10)$
$[5\pi/10+\alpha,\ 7\pi/10+\alpha]$	T_2	T_1 and T_2	$v_o=v_{ad}=1.902\,V_m\sin(\omega t-\pi/10)$
$[7\pi/10+\alpha,\ 9\pi/10+\alpha]$	T_3	T_2 and T_3	$v_o=v_{bd}=1.902\,V_m\sin(\omega t-3\pi/10)$
$[9\pi/10+\alpha,\ 1\pi/10+\alpha]$	T_4	T_3 and T_4	$v_o=v_{be}=1.902\,V_m\sin(\omega t-\pi/2)$
$[11\pi/10+\alpha,\ 13\pi/10+\alpha]$	T_5	T_4 and T_5	$v_o=v_{ce}=1.902\,V_m\sin(\omega t-7\pi/10)$
$[13\pi/10+\alpha,\ 15\pi/10+\alpha]$	T_6	T_5 and T_6	$v_o=v_{ca}=1.902\,V_m\sin(\omega t-9\pi/10)$
$[15\pi/10+\alpha,\ 17\pi/10+\alpha]$	T_7	T_6 and T_7	$v_o=v_{da}=1.902\,V_m\sin(\omega t+9\pi/10)$
$[17\pi/10+\alpha,\ 19\pi/10+\alpha]$	T_8	T_7 and T_8	$v_o=v_{db}=1.902\,V_m\sin(\omega t+7\pi/10)$
$[19\pi/10+\alpha,\ 21\pi/10+\alpha]$	T_9	T_8 and T_9	$v_o=v_{eb}=1.902\,V_m\sin(\omega t+5\pi/10)$

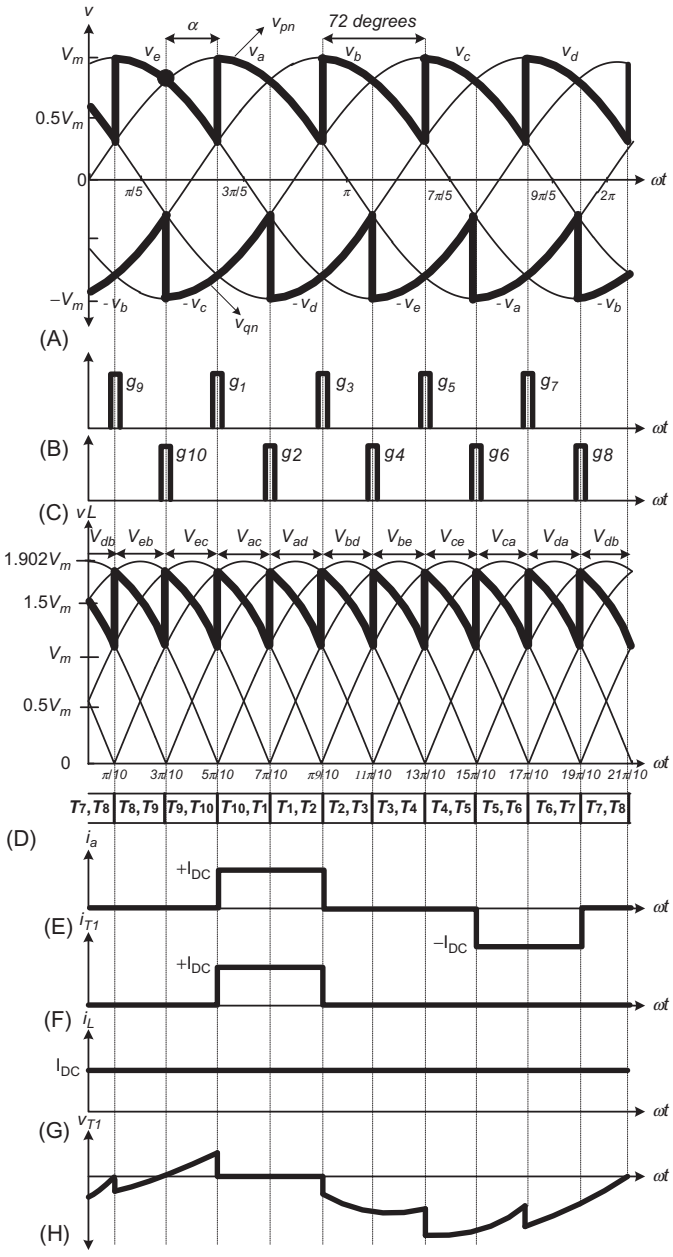


FIG. 15.14 (A) Supply voltage with positive and negative waveforms, (B) gate pulses for firing upper-leg switches, (C) gate pulses for firing lower-leg switches, (D) output-voltage waveform, (E) supply current of phase a, (F) switch 1 current, (G) load current, and (H) voltage across switch 1.

The rms output voltage is

$$V_{rms} = \sqrt{\frac{1}{2\pi/10}\int_{\frac{5\pi}{10}+\alpha}^{\frac{7\pi}{10}+\alpha} (1.902V_m \sin(\omega t - \pi/10))^2}$$

$$V_{rms} = \sqrt{\frac{5\times 1.902^2 \times V_m^2}{\pi}\int_{\frac{5\pi}{10}+\alpha}^{\frac{7\pi}{10}+\alpha}\left[\frac{1-\cos 2\left(\omega t-\frac{\pi}{10}\right)}{2}\right]d(\omega t)}$$

$$V_{rms} = \sqrt{\frac{5\times 1.902^2 \times V_m^2}{2\pi}\left[\omega t - \frac{1}{2}\sin 2\left(\omega t - \frac{\pi}{10}\right)\right]_{\frac{5\pi}{10}+\alpha}^{\frac{7\pi}{10}+\alpha}}$$

$$V_{rms} = 1.902V_m\sqrt{\frac{1}{2}+\frac{5}{2\pi}\sin(\pi/5)\cos 2\alpha} \tag{15.19}$$

It is evident from Fig. 15.14D that the instantaneous output voltage is continuous for $\alpha < \pi/5$; therefore, for any passive load, the load current will be continuous. For $3\pi/10 < \alpha > \pi/5$, the continuity of load current depends on the phase angle of load (φ) and discontinuous for purely resistive load ($\varphi = 0$). For $\alpha > 3\pi/10$, the load current will be always discontinuous for the passive load ($V_{dc} > 0$), whereas for active load (RLE), there will be fourth-quadrant operation ($V_{dc} < 0$ and $I_{dc} > 0$).

Fig. 15.14E shows the input phase current, which is a quasi-square wave. Since the instantaneous value of load current is assumed to be constant, so the phase current will be $+I_{DC}$ in the interval ($3\pi/10+\alpha$ and $7\pi/10+\alpha$) and $-I_{DC}$ in the interval ($13\pi/10+\alpha$ and $17\pi/10+\alpha$). Also, each phase currents will be displaced from each other by $2\pi/5$, irrespective of thyristor firing angles. The input phase current i_a can be expressed in Fourier series as

$$\begin{aligned} i_a &= I_{DC} + \sum_{n=1,2,3,\ldots}^{\infty}(a_n \cos n\omega t + b_n \sin n\omega t) \\ i_a &= I_{DC} + \sum_{n=1,2,3,\ldots}^{\infty}\sqrt{2}I_n \sin(n\omega t + \varphi_n) \end{aligned} \tag{15.20}$$

where I_n is the rms value of nth harmonic component of the input current and is given by

$$I_n = \frac{1}{\sqrt{2}}\left(a_n^2 + b_n^2\right)^{\frac{1}{2}} \tag{15.21}$$

The φ_n is the nth harmonic phase shift and is given by

$$\varphi_n = \tan^{-1}\left(\frac{a_n}{b_n}\right) \tag{15.22}$$

Also, due to the symmetry of waveform,

$$I_{DC} = \frac{1}{2\pi}\int_0^{2\pi} i(\omega t)\, d\omega t = 0 \tag{15.23}$$

$$a_n = \frac{1}{\pi}\int_0^{2\pi} i_a \cos n\omega t \, d\omega t$$

$$a_n = \frac{1}{\pi}\left[\int_{\frac{3\pi}{10}+\alpha}^{\frac{7\pi}{10}+\alpha} I_{DC}\cos n\omega t \, d\omega t - \int_{\frac{13\pi}{10}+\alpha}^{\frac{17\pi}{10}+\alpha} I_{DC}\cos n\omega t \, d\omega t\right]$$

$$a_n = -\frac{4I_{DC}}{n\pi}\sin\frac{n\pi}{5}\sin n\alpha, \quad n = 1,3,5,\ldots \tag{15.24}$$

Similarly,

$$b_n = \frac{1}{\pi}\int_0^{2\pi} i_a \sin n\omega t \, d\omega t$$

$$b_n = \frac{1}{\pi}\left[\int_{\frac{3\pi}{10}+\alpha}^{\frac{7\pi}{10}+\alpha} I_{DC}\sin n\omega t \, d\omega t - \int_{\frac{13\pi}{10}+\alpha}^{\frac{17\pi}{10}+\alpha} I_{DC}\sin n\omega t \, d\omega t\right]$$

$$b_n = \frac{4I_{DC}}{n\pi}\sin\frac{n\pi}{5}\cos n\alpha, \quad n = 1,3,5,\ldots \tag{15.25}$$

Therefore, the rms value of *nth* harmonics current will be given by

$$I_n = \frac{1}{\sqrt{2}}\left(a_n^2 + b_n^2\right)^{\frac{1}{2}} = \frac{2\sqrt{2}}{n\pi} I_{DC}\sin\frac{n\pi}{5} \tag{15.26}$$

and

$$\varphi_n = \tan^{-1}\left(\frac{a_n}{b_n}\right) = -n\alpha \tag{15.27}$$

$n = 1$ will give the rms value of fundamental component of the input current:

$$I_1 = \frac{2\sqrt{2}}{\pi} I_{DC}\sin\frac{\pi}{5} = 0.529 I_{DC} \tag{15.28}$$

Hence, the input current can be given by

$$i_s = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4I_{DC}}{n\pi}\sin\frac{n\pi}{5}\sin(n\omega t - n\alpha) \tag{15.29}$$

The fundamental input current, (substituting, $n = 1$), is

$$i_{s1} = \frac{4I_{DC}}{\pi}\sin\frac{\pi}{5}\sin(\omega t - \alpha) = 0.7484 I_{DC}\sin(\omega t - \alpha) \tag{15.30}$$

The rms value of the input current can be calculated as

$$\begin{aligned} I_{rms} &= \left[\frac{1}{2\pi}\int_0^{2\pi} i^2 d\omega t\right]^{\frac{1}{2}} \\ &= \left[\frac{2}{2\pi}\int_{\frac{3\pi}{10}+\alpha}^{\frac{7\pi}{10}+\alpha} I_{DC}^2 d\omega t\right]^{\frac{1}{2}} \\ &= \sqrt{\frac{2}{5}} I_{DC} = 0.6324 I_{DC} \end{aligned} \tag{15.31}$$

The total harmonic distortion (THD) is given by

$$THD = \sqrt{\frac{I^2}{I_1^2} - 1} = \sqrt{\frac{(0.634 I_{DC})^2}{(0.529 I_{DC})^2} - 1} = 65.5\% \tag{15.32}$$

Displacement factor

$$DF = \cos(\varphi_1) = \cos(-\alpha) = \cos\alpha \tag{15.33}$$

Power factor

$$PF = \frac{\cos\alpha}{\sqrt{1 + THD^2}} = \frac{I_1}{I}\cos\alpha = \frac{0.529 I_{DC}}{0.634 I_{DC}}\cos\alpha = 0.8365\cos\alpha \tag{15.34}$$

The load current is constant as the load is considered highly inductive; from Fig. 15.14F, it is clear that each switch operates for $2\pi/5$ period of time in one cycle; accordingly, the switch average current can be calculated as

$$I_{sw_avg.} = \frac{1}{2\pi}\left[\int_{\frac{3\pi}{10}+\alpha}^{\frac{7\pi}{10}+\alpha} I_{DC} d\omega t\right] = 0.2 I_{DC} \tag{15.35}$$

When calculated, the switch current is only 20% of DC-link current [10]. The harmonic factor (HF_n) is defined as the normalized harmonic current of the supply with respect to the fundamental component (I_n/I_1) and is calculated using Eq. (6.36):

$$HF_n = \sqrt{\left(\frac{I_n}{I}\right)^2 - 1} \tag{15.36}$$

Problem 15.2 A five-phase full-wave bridge-controlled rectifier has an AC input of 120 V rms at 60 Hz and 100 Ω load resistor. The delay angle is $\alpha = \pi/12$ radians. Determine the following:

(a) Average current in the load
(b) Power absorbed by the load

(c) Efficiency of the rectifier
(d) The expression for the input current
(e) THD
(f) Power factor of the rectifier
(g) Form factor and ripple factor

Solution

(a) Average load voltage $V_{DC} = 1.87 V_m \cos\alpha = 1.87 \times \sqrt{2} \times 120 \times \cos(\pi/12) = 306.53\,\text{V}$

$$\text{Average load current } I_{DC} = \frac{V_{DC}}{R} = \frac{306.53}{100} = 3.06\,\text{A}$$

(b) Power absorbed by the load $P_{DC} = V_{DC} \times I_{DC} = 306.53 \times 3.06 = 938\,\text{W}$

(c) The rms value of the output voltage $V_{rms} = 1.902 V_m \sqrt{\frac{1}{2} + \frac{5}{2\pi} \sin\left(\frac{\pi}{5}\right) \cos 2\alpha}$

$$V_{rms} = 1.902 \times 120\sqrt{2}\sqrt{\frac{1}{2} + \frac{5}{2\pi} \sin\left(\frac{\pi}{5}\right) \cos\left(2 \times \frac{\pi}{12}\right)}$$

$$V_{rms} = 307.08\,\text{V}$$

$$\text{and } I_{rms} = \frac{V_{rms}}{R} = \frac{307.08}{100} = 3.071\,\text{A}$$

Therefore, efficiency $\eta = \frac{P_{DC}}{P_{ac}} = \frac{V_{DC} I_{DC}}{V_{rms} I_{rms}} = \frac{306.53 \times 3.06}{307.08 \times 3.071} = 99.46\%$

(d) The expression for the input current $i_s = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4 I_{DC}}{n\pi} \sin\frac{n\pi}{5} \sin(n\omega t - n\alpha)$

$$i_s = \sum_{n=1,3,5,\ldots}^{\infty} \frac{3.9}{n} \sin\frac{n\pi}{5} \sin(n\omega t - n\pi/12)$$

(e) The rms value of the input current $I = \sqrt{\frac{2}{5}} I_{DC} = \sqrt{\frac{2}{5}} \times 3.06 = 1.935\,\text{A}$

The rms value of fundamental component of the input current

$$I_1 = \frac{2\sqrt{2}}{\pi} \sin\frac{\pi}{5} I_{DC} = 0.529 \times 3.06 = 1.6187$$

$$THD = \sqrt{\frac{I^2}{I_1^2} - 1} = \sqrt{\frac{(1.935)^2}{(1.6187)^2} - 1} = 65.5\%$$

(f) The power factor $PF = \frac{\cos\alpha}{\sqrt{1 + THD^2}} = \frac{\cos(\pi/15)}{\sqrt{1 + (0.655)^2}} = 0.818$

(g) Form factor $FF = \frac{V_{rms}}{V_{DC}} = \frac{307.08}{306.53} = 1.0018 = 100.18\%$

Ripple factor $RF = \sqrt{FF^2 - 1} = \sqrt{(1.0018)^2 - 1} = 0.06 = 6\%$

15.3.3 Multipulse Rectifiers

The multipulse uncontrolled rectifiers are suitable for VSI-fed drives, while the controlled rectifiers are employed for CSI drives. As the number of pulses per cycle increases, the output waveform gets improved. There are identical multipulse rectifiers connected in either parallel, series, or separate modes to achieve higher pulses in the output. Fig. 15.15 shows general layout of 12-, 18-, and 24-pulse rectifier circuits [29,30]. If we employ 10-pulse rectifiers, then we can obtain 20, 30, and 40 pulses in the output.

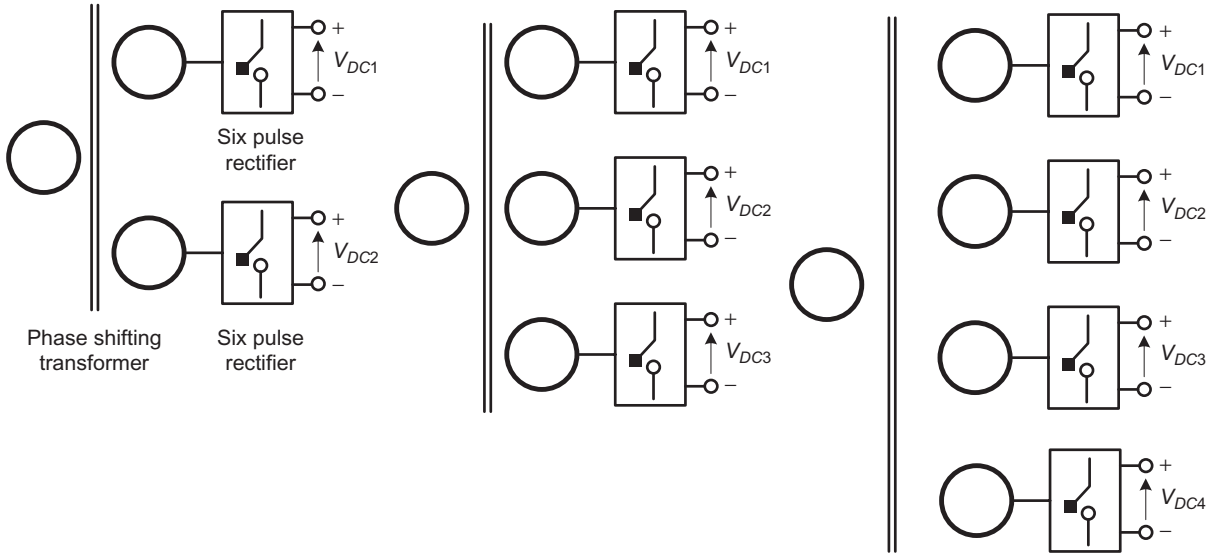


FIG. 15.15 Multipulse uncontrolled/controlled rectifier's arrangement.

15.3.3.1 12-Pulse Series Type Controlled Rectifier

Two six-pulse controlled rectifiers are powered by a phase-shifting transformer with two secondary windings in delta and star connections. Therefore, the phase angle between both secondary windings shifts 30 degrees each. In this case with 12 pulses per cycle, the quality of output-voltage waveform would definitely be improved with low ripple content [29].

Fig. 15.15 shows circuit configuration of a 12-pulse series-type controlled rectifier. A three-phase transformer with two secondary and one delta-connected primary feeds the two identical six-pulse controlled rectifiers. The upper three-phase bridge is fed from Y-connected secondary winding while lower with Δ-connected secondary winding. Therefore, this arrangement will result in the phase angle shifts between both secondary windings by 30 degrees. The outputs of the two six-pulse rectifiers are connected in series, and the conduction period of the line current for each converter is 120 degrees.

Consider an idealized 12-pulse rectifier where the line inductance L_s and the total leakage inductance L_{lk} of the transformer are assumed to be zero and the magnitude of the current is constant (ripple-free) [29]. In practical case, the ripple in the DC current will be relatively low due to the series connection of the two six-pulse rectifiers, where the leakage inductances of the secondary windings can be considered in series.

For the purpose of eliminating the dominate lower-order harmonics in the line current i_a, the line-to-line voltage v_{a1b1} of the Y-connected secondary winding (N_2 turns) is in phase with the primary winding (N_1 turns) voltage v_{ab}, while the Δ-connected secondary winding (N_3 turns) voltage v_{a2b2} leads v_{ab} by [29]:

$$\delta = \angle v_{a_2b_2} - \angle v_{ab} = 30 \text{ degrees} \tag{15.37}$$

For the sake of simplicity, let $N_1 = N, N_2 = N/2$ and $N_3 = \sqrt{3}/2N$ (i.e., N_1-N_2-N_3 = 1:0.5:0.866).

Therefore, the rms line-to-line voltage of each secondary winding will become

$$V_{a1b1} = V_{a2b2} = V_{ab}/2 \tag{15.38}$$

Since the two rectifiers are series-connected, net output, or load, voltage $V_{dc} = V_{dc1} + V_{dc2}$; since the waveforms of V_{dc1} and V_{dc2} are phase shifted from each other by 30 degrees , therefore, the waveform of output voltage V_{dc} consists of 12 pulses per cycle of supply voltage. The current waveforms are illustrated in Fig. 15.16, where i_{a1} and i_{c2a2} are the phase currents of secondary Y and Δ windings, respectively, and i'_{a1} and i'_{c2a2} are the currents referred from secondary side to the primary side. The waveforms of reflected current to primary side of secondary Y-connected winding i'_{a1} will be identical to that of i_{a1} except that the magnitude is changed in ratio of the number of turns of the two windings. However, when i_{a2} is referred to the primary side, the reflected waveform does not keep the same waveform and magnitude. This is due to phase displacements of the harmonic current when they are referred from Δ-Y windings. This phase displacement is advantageous as it will lead to the cancelation of low-order predominant fifth and seventh harmonics from the currents of transformer primary winding and does not appear in the line current, which is given by Eq. (15.39):

$$i_a = i'_{a1} + i'_{a2} \tag{15.39}$$

The secondary (Y-connected) line current i_{a1} can be expressed by Eq. (15.40):

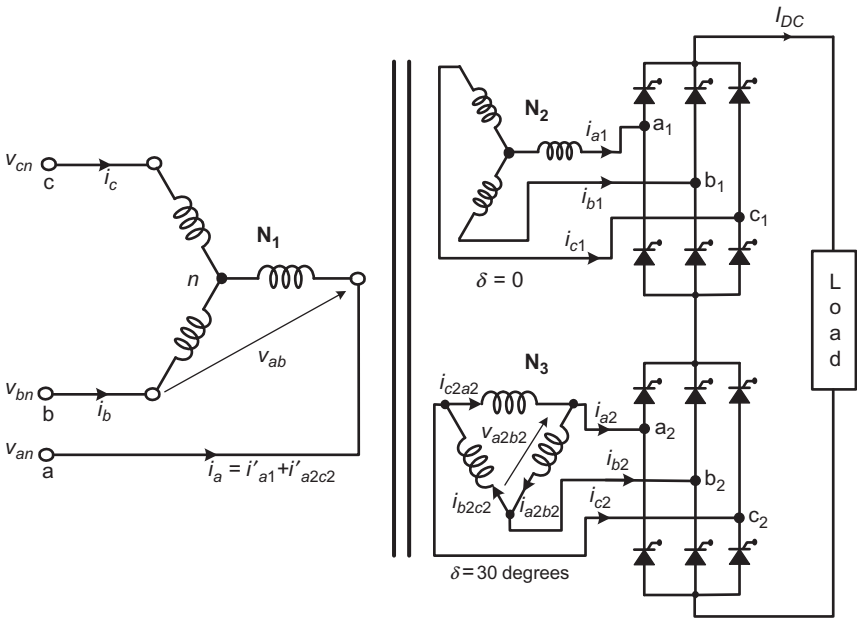


FIG. 15.16 Twelve-pulse series-type controlled rectifier connection circuit.

$$i_{a1}=\frac{2\sqrt{3}}{\pi}I_{dc}\left[\begin{array}{l}\sin\omega t-\frac{1}{5}\sin 5\omega t-\frac{1}{7}\sin 7\omega t+\frac{1}{11}\sin 11\omega t\\ +\frac{1}{13}\sin 13\omega t-\frac{1}{17}\sin 17\omega t-\frac{1}{19}\sin 19\omega t+\ldots\end{array}\right] \tag{15.40}$$

Since the waveform of current i_{a1} is of half-wave symmetry, it does not contain any even-order harmonics. Current i_a does not contain any triple harmonics either due to the consideration of balanced three-phase system. The line current in Δ-connected secondary winding such as i_{a2} leads i_{a1} by 30 degrees, and the Fourier expression of current i_{a2} is given by Eq. (15.41):

$$i_{a2}=\frac{2\sqrt{3}}{\pi}I_{dc}\left[\begin{array}{l}\sin(\omega t+30\,\text{degrees})-\frac{1}{5}\sin 5(\omega t+30\,\text{degrees})\\ -\frac{1}{7}\sin 7(\omega t+30\,\text{degrees})\\ +\frac{1}{11}\sin 11(\omega t+30\,\text{degrees})\\ +\frac{1}{13}\sin 13(\omega t+30\,\text{degrees})\\ -\frac{1}{17}\sin 17(\omega t+30\,\text{degrees})\\ -\frac{1}{19}\sin 19(\omega t+30\,\text{degrees})+\ldots\end{array}\right] \tag{15.41}$$

Similar equations for i_{b2} and i_{c2} can be obtained. The current i'_{a1}, which is identical to i_{a1} in wave shape, can be expressed in Fourier series by Eq. (15.42):

$$i'_{a1}=\frac{\sqrt{3}}{\pi}I_{dc}\left(\sin\omega t-\frac{1}{5}\sin 5\omega t-\frac{1}{7}\sin 7\omega t+\frac{1}{11}\sin 11\omega t+\frac{1}{13}\sin 13\omega t\ldots\right) \tag{15.42}$$

The phase currents in the Δ-connected secondary windings i_{a2b2}, i_{b2c2}, and i_{c2a2} can be obtained from its line currents using the transformation given in Eq. (15.43):

$$\begin{bmatrix}i_{a2b2}\\ i_{b2c2}\\ i_{c2a2}\end{bmatrix}=\frac{1}{3}\begin{bmatrix}-1 & 1 & 0\\ 0 & -1 & 1\\ 1 & 0 & -1\end{bmatrix}\begin{bmatrix}i_{a2}\\ i_{b2}\\ i_{c2}\end{bmatrix} \tag{15.43}$$

The phase currents in the Δ-connected secondary winding i_{a2b2}, i_{b2c2}, and i_{c2a2} have a stepped waveform, each step being of 60 degrees in width whereas $I_d/3$ and $2I_d/3$ the heights. The expression for phase current in the Δ-connected secondary winding can be written as Eq. (15.44).

$$i_{c2a2}=\frac{2}{\pi\sqrt{3}}I_{dc}\left[\begin{array}{l}\sin(\omega t+30\,\text{degrees})-\frac{1}{5}\sin 5(\omega t+30\,\text{degrees})\\ -\frac{1}{7}\sin 7(\omega t+30\,\text{degrees})\\ +\frac{1}{11}\sin 11(\omega t+30\,\text{degrees})+\cdots\\ -\sin(\omega t+150\,\text{degrees})\\ +\frac{1}{5}\sin 5(\omega t+150\,\text{degrees})\\ +\frac{1}{7}\sin 7(\omega t+150\,\text{degrees})\\ -\frac{1}{11}\sin 11(\omega t+150\,\text{degrees})\cdots\end{array}\right] \tag{15.44}$$

On simplification of Eq. (15.44), we have

$$i_{c2a2}=\frac{2}{\pi}I_{dc}\left[\begin{array}{l}\sin\omega t+\frac{1}{5}\sin 5\omega t+\frac{1}{7}\sin 7\omega t+\frac{1}{11}\sin 11\omega t\\ +\frac{1}{17}\sin 17\omega t+\frac{1}{19}\sin 19\omega t+\cdots\end{array}\right] \tag{15.45}$$

Similarly, the expressions for the currents i_{a2b2} and i_{b2c2} can be obtained. The corresponding reflected current to the primary side can be obtained from Eq. (15.45); by multiplying with turn ratio ($N_3:N_1=\sqrt{3}:2$), we can obtain Eq. (15.46) [31]:

$$i'_{c2a2}=\frac{\sqrt{3}}{\pi}I_{dc}\left[\begin{array}{l}\sin\omega t+\frac{1}{5}\sin 5\omega t+\frac{1}{7}\sin 7\omega t+\frac{1}{11}\sin 11\omega t\\ +\frac{1}{13}\sin 13\omega t+\frac{1}{17}\sin 17\omega t+\frac{1}{19}\sin 19\omega t\\ +\frac{1}{23}\sin 23\omega t+\frac{1}{25}\sin 25\omega t+\cdots\end{array}\right] \tag{15.46}$$

Therefore, the line current $i_a=i'_{a1}+i'_{c2a2}$ can be written as given in Eq. (15.47):

$$i_a=\frac{2\sqrt{3}}{\pi}I_{dc}\left[\begin{array}{l}\sin\omega t+\frac{1}{11}\sin 11\omega t+\frac{1}{13}\sin 13\omega t\\ +\frac{1}{23}\sin 23\omega t+\frac{1}{25}\sin 25\omega t+\cdots\end{array}\right] \tag{15.47}$$

Different current waveforms are shown in Fig. 15.17. It is evident from Eq. (15.47) that the two dominant harmonics, 5th and 7th, are absent along with 17th and 19th, which improves the THD of this type of converter configuration drastically.

15.3.3.2 Pulse Parallel-Type Controlled Rectifier

In this case, the outputs of the two six-pulse rectifiers are connected in parallel. Fig. 15.18 shows circuit configuration of a 12-pulse parallel-type controlled rectifier. The circuit in the figure simply uses an isolation transformer with a Δ-connected primary, a Y-connected secondary, and a second Δ-connected secondary to obtain 30 degrees (electrical degrees) phase shift. Since the instantaneous outputs of the two rectifiers are not

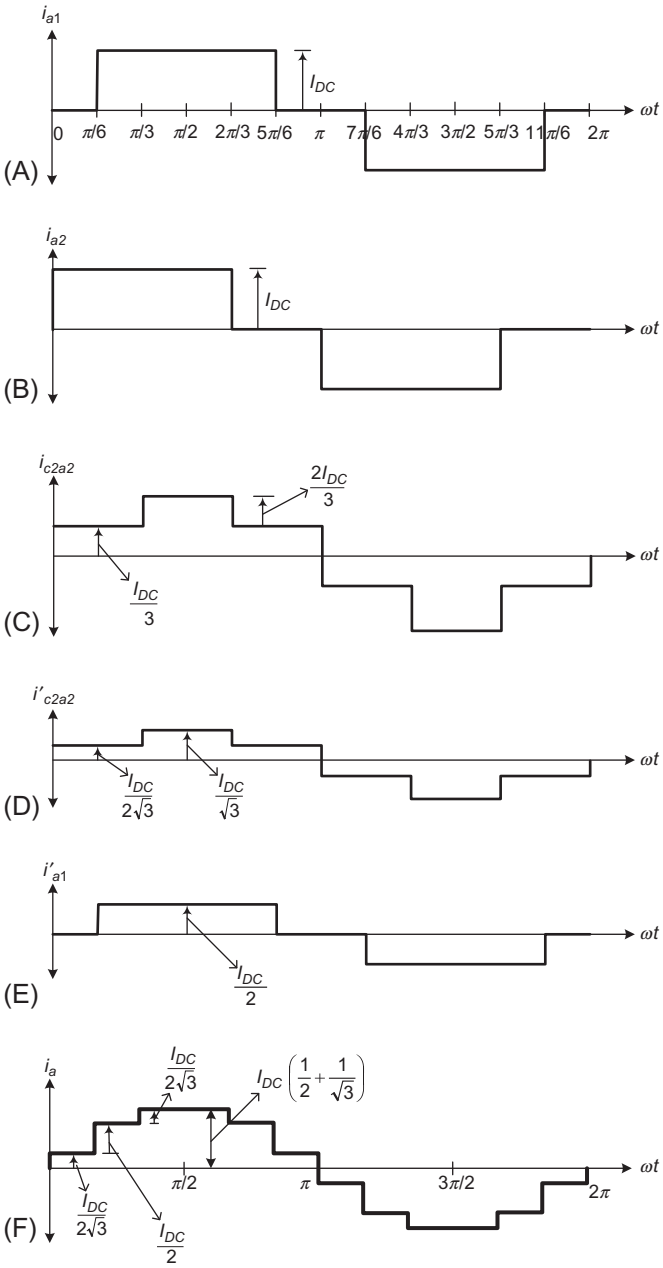


FIG. 15.17 Current waveforms of the 12-pulse series-connected controlled rectifier ($Ls = Llk = 0$). (A) Output line/phase current in star-connected secondary winding. (B) Output line current in delta-connected secondary winding. (C) Output phase current in delta-connected secondary winding. (D) Delta-connected secondary winding phase current reflected to primary side. (E) Star-connected secondary winding phase current reflected to primary side. (F) Total current in the primary side.

equal, an interphase reactor is necessary to support the difference in instantaneous rectifier output voltages and permit each rectifier to operate independently [29]. The line current in primary winding of the transformer is the sum of reflected currents from the two secondary windings, and it becomes stepped due to 30 degrees phase shift in two secondary currents

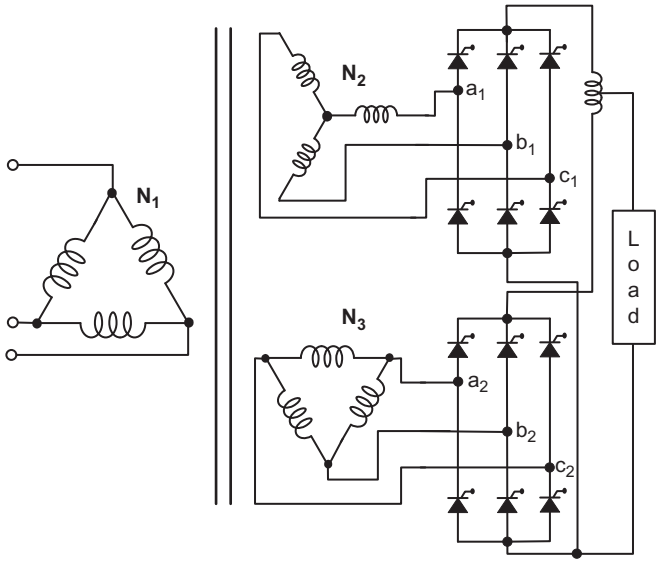


FIG. 15.18 Twelve-pulse parallel-type controlled rectifier connection circuit.

as discussed in Section 15.3.3.1. Therefore, the harmonics and requirement of filter circuit parameters are reduced. Theoretically, input current harmonics for rectifier circuit is a function of pulse number and can be expressed as

$$H = \left(N_p \pm 1\right) \tag{15.48}$$

where $N = 1, 2, 3\ldots$ and p is pulse number.

For example, in a three-phase six-pulse rectifier, the input current will have harmonic components at 5, 7, 11, 13, 17, 19, 23, 25, 29, 31, etc. multiples of the fundamental frequency. For the 12-pulse system shown in Fig. 15.16, the input current will have theoretical harmonic components at 11, 13, 23, 25, 35, 37, etc. multiples of the fundamental frequency as derived and discussed in Section 15.3.3.1. Since the magnitude of each harmonic is proportional to the reciprocal of the harmonic order, the 12-pulse system naturally has a lower harmonic distortion in input current.

The problem with the parallel connection of the rectifiers is that the two rectifiers must share exactly equal current to achieve the desired reduction in harmonics. This would be achieved if output voltages of both secondary windings matches exactly. Because of the differences in the transformer secondary impedances and open-circuit output voltages, this can be practically accomplished for a given fixed load (typically rated load), but not for loads varying over a range. This is the main problem of the parallel 12-pulse configuration connection. Whereas in the case of series connection of two rectifiers, the problems associated with current sharing are avoided, and an interphase reactor is not required. Parallel connections are normally preferred for applications where high current ratings rather than harmonics are the issue [32]. Generally, series connection of rectifiers is much simpler to implement than the parallel connection.

15.3.4 Single-Way Multiphase Systems Topologies

The structure of single-way, m-phase rectifier is shown in Fig. 15.19. In single-way structures, only one diode conducts for single stage, and the remaining diodes are blocked. Due to this, single-way structures are more convenient while increasing the number of phases. In an m-phase, the diodes used in the rectifier circuits are divided into a number of groups in star connection. Each group will have three diodes, that is, for a six-diode rectifier, there will be two groups, and for a 12-diode rectifier, there will be four groups [31]. In a normal connection, the star points will be connected together. But in this circuit, each group will have its all secondary windings, and instead of a direct connection, the star points will be connected through an interphase transformer. The common neutral point serves as the negative terminal of the DC output circuit.

For single-way topologies, the number of output pulses is equal to the number of phases, that is, $p=m$, and the number of diodes are equal to m. Each diode is conducting for $2\pi/m$ electric radians. Fig. 15.19 shows few pulses of output-voltage waveform for m-phase half-wave uncontrolled rectifier. In general, for an m-phase system, the average and rms value of the output voltage is expressed by Eqs. (15.49) and (15.50), respectively:

$$V_{DC}=\frac{V_m}{2\pi/m}\int_{-\frac{\pi}{m}}^{\frac{\pi}{m}}\cos\omega t\,d(\omega t)=\frac{V_m\sin\left(\frac{\pi}{m}\right)}{\pi/m} \tag{15.49}$$

$$\text{rms voltage } V_{rms}=\sqrt{\frac{1}{2\pi/m}\int_{-\frac{\pi}{m}}^{\frac{\pi}{m}}(V_m\cos\omega t\,d\omega t)^2}$$

$$V_{rms}=V_m\sqrt{\frac{1}{2}\left[1+\frac{\sin\left(\frac{2\pi}{m}\right)}{\frac{2\pi}{m}}\right]} \tag{15.50}$$

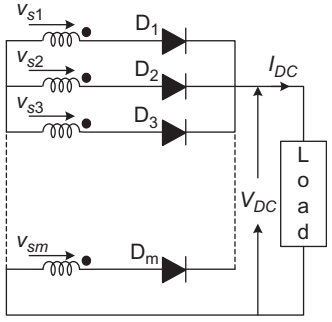


FIG. 15.19 m-Phase, single-way rectifier.

The form factor and ripple factors are expressed by Eqs. (15.51) and (15.52), respectively. From these equations, it is evident that if $m\to\infty\Rightarrow FF\to 1$ and $RF\to 0$,

$$FF=\frac{V_{rms}}{V_{DC}}=\frac{\sqrt{\frac{1}{2}\left[1+\frac{\sin\left(\frac{2\pi}{m}\right)}{\frac{2\pi}{m}}\right]}}{\frac{\sin\left(\frac{\pi}{m}\right)}{\frac{\pi}{m}}} \tag{15.51}$$

$$RF=\sqrt{1-(FF)^2} \tag{15.52}$$

which implies that by increasing the number of phases in a multiphase, single-way rectifier, the output voltage is improved, that is, it becomes smoother. By connecting to a conventional three-phase mains distribution, it is possible to increase the number of "phases" by using transformers with m separated secondary coils. The secondary coils can be connected in a large number of ways. Also, by increasing the number of phases (as stated before, in single-way topologies, $m=p$), the ripple frequency increases, and its amplitude decreases. This fact simplifies the filter design to reduce the ripple in the load [31,32]. The output waveform for m-phase half-wave diode rectifier is shown in Fig. 15.20. For highly inductive load, the output DC current may be considered as constant (I_{DC}).

The diode average current, rms current, and form factor can be obtained by Eqs. (15.53)–(15.55):

$$I_{D(avg.)}=\frac{I_{DC}}{m} \tag{15.53}$$

$$I_{D(rms)}=\frac{I_{DC}}{\sqrt{m}} \tag{15.54}$$

$$K_f=\frac{I_{D(rms)}}{I_{D(avg)}}=\sqrt{m} \tag{15.55}$$

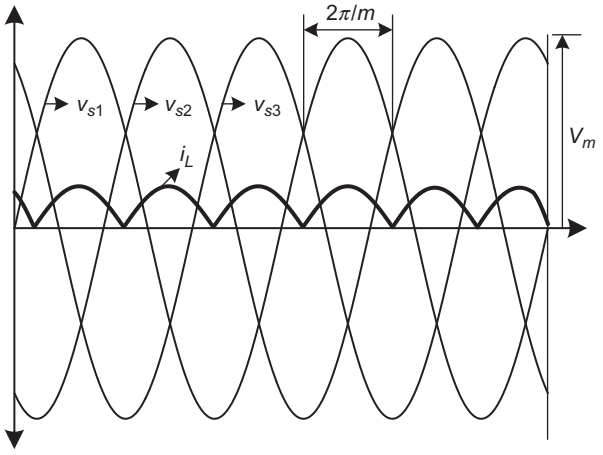


FIG. 15.20 Output waveform for m-phase half-wave diode rectifier.

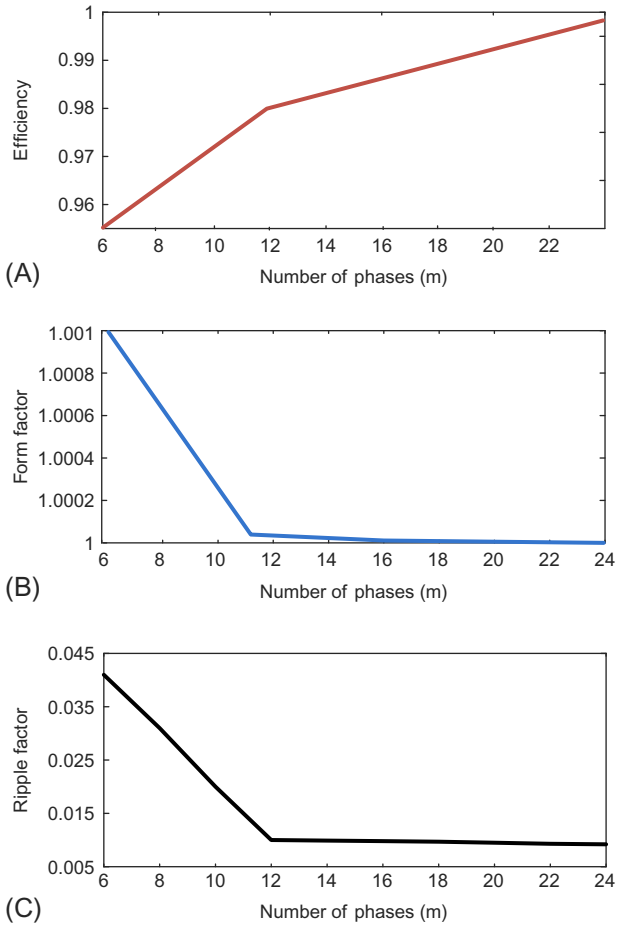


FIG. 15.21 Characteristics of the number of phases versus (A) efficiency, (B) form factor, and (C) ripple factor.

The values for V_{DC} and some of the parameters have been calculated for $m=6$, $m=12$, and $m=24$ and are reported in Fig. 15.21. It is clear from the figure (A)–(C) that the frequency of the ripple on the output is p times the mains frequency. As can be seen, passing from 6 to 12 pulses, one gets a 3.5% improvement in the rectified voltage, while passing from 12 to 24 pulses this improvement is less than 1%.

In practice, for single-way connections, the maximum number of pulses is normally limited to 12 because of the growing complexity of the connections of the transformer's secondary windings. Higher number of pulses can be obtained by using the combination of bridge structures. The best transformer utilization factor (*TUF*) that can be achieved with a single-way connection is 0.79, while with a bridge configuration it is possible to reach higher values, up to 0.955.

15.3.5 Six-Phase AC to DC Converters

Six-phase half-wave rectifiers generally have two configurations, namely, six phase with a neutral line circuit and double antistar with a balance-choke circuit.

15.3.5.1 Six-Phase Half Wave With a Neutral Line Circuit

The power supply of a six-phase balanced voltage source is given by Eq. (15.56), and the waveform is shown in Fig. 15.22; in this case, each phase is shifted by 60 degrees:

$$\begin{aligned} v_{an} &= V_m \sin \omega t \\ v_{bn} &= V_m \sin(\omega t - \pi/3) \\ v_{cn} &= V_m \sin(\omega t - 2\pi/3) \\ v_{dn} &= V_m \sin(\omega t - \pi) \\ v_{en} &= V_m \sin(\omega t - 4\pi/3) \\ v_{bn} &= V_m \sin(\omega t - 5\pi/3) \end{aligned} \tag{15.56}$$

The six-phase half-wave rectifiers are shown in Fig. 15.23. The first circuit is called a Y-Y circuit, and the second circuit is called a Δ/Y circuit. Each diode conducts for 60 degrees in a cycle.

$$V_{DC} = \frac{1}{\pi/3} \int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} V_m \sin \omega t \, d\omega t = \frac{3V_m}{\pi} \tag{15.57}$$

$$V_{rms} = \sqrt{\frac{1}{\pi/3} \left[\int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} (V_m \sin \omega t)^2 d\omega t \right]} = V_m \sqrt{\frac{1}{2} + \frac{3\sqrt{3}}{4\pi}} \tag{15.58}$$

$$FF = \frac{V_{rms}}{V_{dc}} = 1.0008 \tag{15.59}$$

$$RF = \sqrt{1.0008^2 - 1^2} = 0.04 \tag{15.60}$$

$$PF = 0.55 \tag{15.61}$$

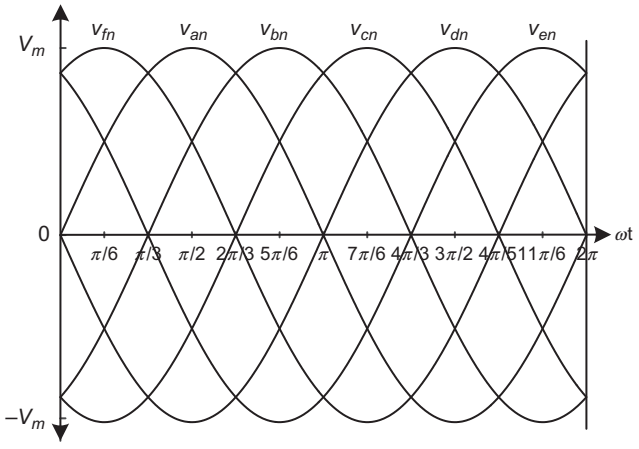


FIG. 15.22 Six-phase supply waveforms.

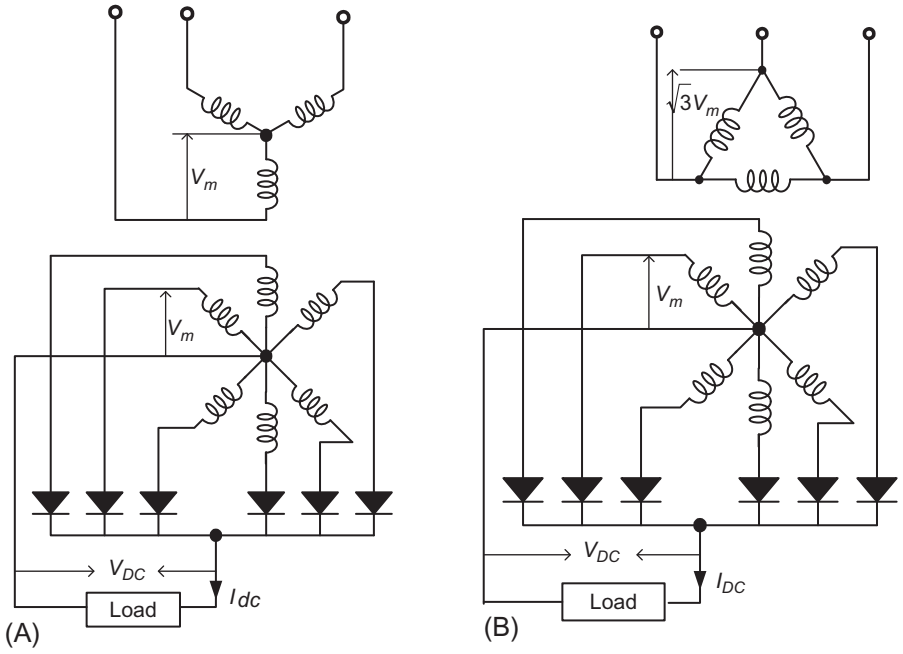


FIG. 15.23 Six-phase half-wave diode rectifiers: (A) Y/Y circuit and (B) Δ/Y circuit.

15.3.5.2 Six-Phase Double-Bridge Full-Wave Uncontrolled Rectifiers

Two circuits of the six-phase bridge full-wave diode rectifiers are shown in Fig. 15.24 and are called as a six-phase bridge circuit and hexagon bridge circuit [31]. In this case, each diode conducts for 60 degrees in a cycle. The average output voltage is given by Eq. (15.62):

$$V_{DC} = \frac{2}{\pi/3}\int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} V_m \sin\omega t\, d\omega t = \frac{6V_m}{\pi} \tag{15.62}$$

15.3.5.3 Six-Phase Half-Wave Controlled Rectifiers

The six-phase half-wave controlled rectifiers are shown in Fig. 15.25 [31]. Each thyristor conducts for $\pi/3$ radians in a cycle. The firing angle $\alpha = \omega t - \pi/3$ in the range of 0–$2\pi/3$. The average output voltage is

$$V_{DC} = \frac{1}{\pi/3}\int_{\frac{\pi}{3}+\alpha}^{\frac{2\pi}{3}+\alpha} V_m \sin\omega t\, d\omega t = \frac{3V_m}{\pi}\cos\alpha \tag{15.63}$$

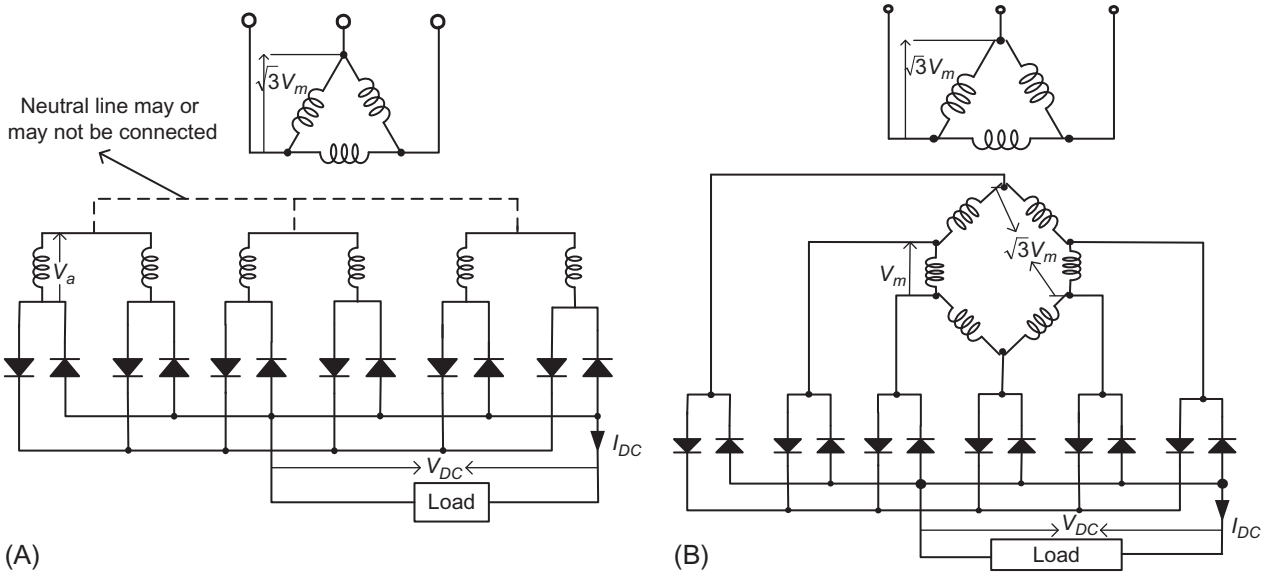


FIG. 15.24 Six-phase full-wave uncontrolled rectifiers: (A) six-phase bridge circuit and (B) six-phase hexagon bridge circuit.

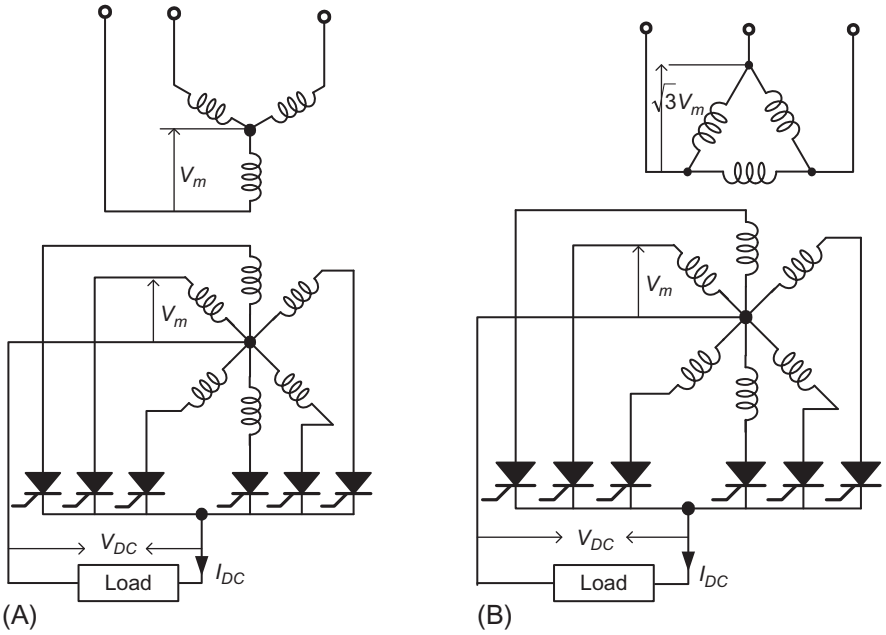


FIG. 15.25 Six-phase half-wave controlled rectifiers: (A) Y/Y circuit and (B) Δ/Y circuit.

$$V_{rms} = \sqrt{\frac{1}{\pi/3}\left[\int_{\frac{\pi}{3}+\alpha}^{\frac{2\pi}{3}+\alpha} (V_m \sin\omega t)^2 d\omega t\right]} = V_m\sqrt{\frac{1}{2} + \frac{3\sqrt{3}}{4\pi}\cos\alpha} \tag{15.64}$$

$$FF = \frac{V_{rms}}{V_{dc}} = 1.0008 \tag{15.65}$$

$$RF = \sqrt{1.0008^2 - 1^2} = 0.042 \tag{15.66}$$

$$PF = 0.956 \tag{15.67}$$

From Eq. (15.63), it is clear that the output voltage can have positive ($\alpha < \pi/2$) and negative ($\alpha > \pi/2$) values. When $\alpha < \pi/2$, the output current is ($I_{DC} = V_{DC}/R$), and when the firing angle α is $>\pi/2$, the output voltage can have negative values, but the output current can only have positive values.

15.4 Multiphase DC-AC Converters

15.4.1 Modeling and Control of a Five-Phase Voltage Source Inverter

This section is devoted to the development of a comprehensive model of a five-phase voltage-source inverter based on space-vector theory [32,33]. Proper modeling of voltage-source inverters is important in devising appropriate control algorithm. The complete model is broadly classified into two groups, namely, square-wave and PWM modes based on the operation of the inverter. The leg voltages and line voltages along with phase voltages are illustrated. The Fourier analysis of output phase-to-neutral voltages and nonadjacent voltages is performed for square-wave mode. The output phase-to-neutral voltage is shown to be essentially identical to those obtainable with a three-phase voltage-source inverter. At each step, simulation results are provided to support the analytic approach results. The relationship between the phase and line voltages for a five-phase system is also established.

For high-power application, stepped operation of inverter is preferred over PWM mode to avoid switching losses. Square-wave mode of operation is elaborated for 180 degrees conduction mode, and the performance is evaluated in terms of harmonic content of phase-to-neutral voltages.

15.4.1.1 Modeling of a Five-Phase VSI

Power circuit topology of a five-phase VSI is shown in Fig. 15.26. Each switch in the circuit consists of two power semiconductor devices, connected in antiparallel. One of these is a fully controllable semiconductor, such as a bipolar transistor, MOSFET, or IGBT, while the second one is a diode. The input of the inverter is a DC voltage, which is regarded further on as being constant. The inverter outputs are denoted in Fig. 15.26 with lowercase symbols (*a*, *b*, *c*, *d*, and *e*), while the points of connection of the outputs to inverter legs have symbols in capital letters (*A*,*B*,*C*,*D*,*E*). The basic operating principles of the five-phase VSI are developed in what follows assuming the ideal commutation and zero forward voltage drops.

15.4.1.2 Square Wave Mode of Operation

Discrete switching of power switches in an inverter leads to stepped wave output termed as square-wave operation of the inverter. Conventionally, 180 degrees conduction mode is considered leading to 10-step output phase voltages from the inverter. Each switch conducts for half of the fundamental cycle,

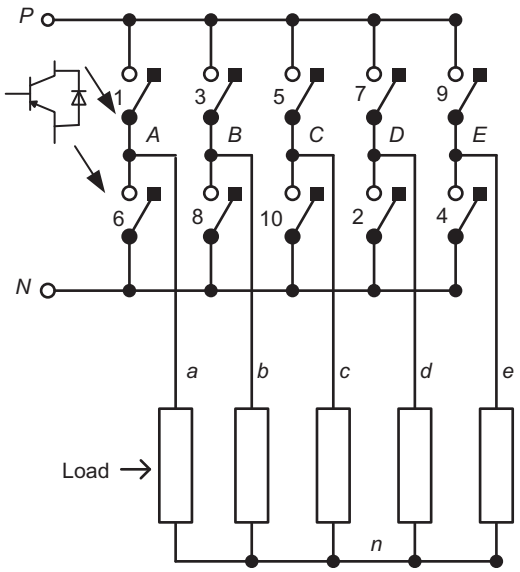


FIG. 15.26 Five-phase voltage-source inverter power circuit.

that is, 180 degrees. The operation of upper and lower switches is complimentary in operation, that is, when upper switch is on, the lower switch is off and vice versa. In real-time application, a dead time is provided between the turning on of lower switch and turning off of upper switch and vice versa. The incoming power switch cannot be turned on unless the outgoing switch is completely turned off. There is a finite time for complete turnoff of a power switching device, and hence, a dead time is to be provided. This is done in order to avoid short circuit of the source side.

180 degrees conduction mode

Each switch is assumed to conduct for 180 degrees(half of the fundamental cycle), and the phase delay between firing of two switches in any subsequent two phases is equal to 360/5 degrees = 72 degrees. The driving control gate/base signals for the 10 switches of the inverter in Fig. 15.26 are illustrated in Fig. 15.27. One complete cycle of operation of the inverter can be divided into 10 distinct modes indicated in Fig. 15.27 and summarized in Table 15.2. It follows from these that at any instant in time there are five switches that are "ON" and five switches that are "OFF." In the 10-step mode of operation, there are two conducting switches from the upper five and three from the lower five or vice versa.

Space vector of phase voltages in stationary reference frame is defined, using power variant transformation [33]:

$$\underline{v} = \frac{2}{5}\left(v_a + \underline{a}v_b + \underline{a}^2 v_c + \underline{a}^{*2} v_d + \underline{a}^* v_e\right) \tag{15.68}$$

where $\underline{a} = \exp(j2\pi/5)$, $\underline{a}^2 = \exp(j4\pi/5)$, $\underline{a}^* = \exp(-j2\pi/5)$, $\underline{a}^{*2} = \exp(-j4\pi/5)$, and * stands for a complex conjugate.

Leg voltages (i.e., voltages between points *A*,*B*,*C*,*D*, and *E* and the negative rail of the DC bus N in Fig. 15.26) are considered first. The leg voltages from Fig. 15.27 are substituted in expression (15.68) to obtain their corresponding space vectors given as in Eq. (15.69):

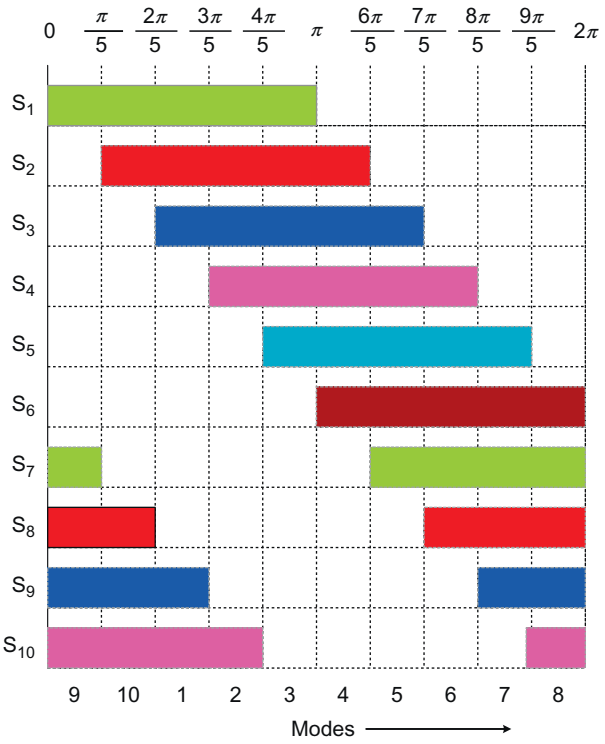


FIG. 15.27 Gating signals of a five-phase voltage-source inverter in square-wave mode.

TABLE 15.2 Modes of operation of the five-phase voltage-source inverter (10-step operation)

Mode	Switches ON	Terminal polarity
1	9,10,1,2,3	$A^+B^+C^-D^-E^+$
2	10,1,2,3,4	$A^+B^+C^-D^-E^-$
3	1,2,3,4,5	$A^+B^+C^+D^-E^-$
4	2,3,4,5,6	$A^-B^+C^+D^-E^-$
5	3,4,5,6,7	$A^-B^+C^+D^+E^-$
6	4,5,6,7,8	$A^-B^-C^+D^+E^-$
7	5,6,7,8,9	$A^-B^-C^+D^+E^+$
8	6,7,8,9,10	$A^-B^-C^-D^+E^+$
9	1,7,8,9,10	$A^+B^-C^-D^+E^+$
10	8,9,10,1,2	$A^+B^-C^-D^-E^+$

$$\begin{bmatrix} \vec{v}_{1leg} \\ \vec{v}_{2leg} \\ \vec{v}_{3leg} \\ \vec{v}_{4leg} \\ \vec{v}_{5leg} \\ \vec{v}_{6leg} \\ \vec{v}_{7leg} \\ \vec{v}_{8leg} \\ \vec{v}_{9leg} \\ \vec{v}_{10leg} \end{bmatrix} = \frac{2}{5} V_{DC}\left(2\cos\frac{\pi}{5}\right) \begin{bmatrix} e^{j0} \\ e^{j\pi/5} \\ e^{j2\pi/5} \\ e^{j3\pi/5} \\ e^{j4\pi/5} \\ e^{j\pi} \\ e^{j6\pi/5} \\ e^{j7\pi/5} \\ e^{j8\pi/5} \\ e^{j9\pi/5} \end{bmatrix} \tag{15.69}$$

It is seen that the leg voltages have magnitude of $\frac{2}{5}V_{DC}2\cos(\pi/5)$ and are 36 degrees apart forming a decagon. There are in total $2^5=32$ switching states (base is taken as 2 because the switching states can only assume two values either 0 (indicate off state) or 1 (indicate on state)). The first 10 states are described above, and the remaining 22 switching states are discussed in the next section.

Phase-to-neutral voltages are discussed next. Phase-to-neutral voltages of the star-connected load are most easily found by defining a voltage difference between the star point n of the load and the negative rail of the DC bus N. The following correlation then holds true:

$$\begin{aligned} v_A &= v_a + v_{nN} \\ v_B &= v_b + v_{nN} \\ v_C &= v_c + v_{nN} \\ v_D &= v_d + v_{nN} \\ v_E &= v_e + v_{nN} \end{aligned} \tag{15.70}$$

Since the phase voltages in a star-connected load sum to zero (sum of five-phase sine wave at one instant of time is zero), the summation of Eq. (15.70) produces

$$v_{nN} = (1/5)(v_A + v_B + v_C + v_D + v_E) \tag{15.71}$$

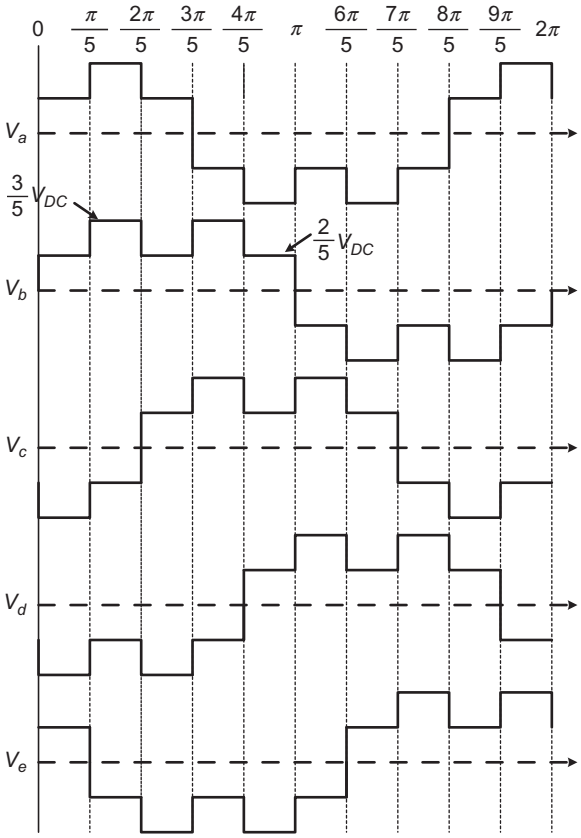


FIG. 15.28 Phase-to-neutral voltages of the five-phase VSI in the square-wave mode of operation.

Substitution of (15.71) into (15.70) produces phase-to-neutral voltages of the load in the following form:

$$\begin{aligned} v_a &= (4/5)v_A - (1/5)(v_B + v_C + v_D + v_E) \\ v_b &= (4/5)v_B - (1/5)(v_A + v_C + v_D + v_E) \\ v_c &= (4/5)v_C - (1/5)(v_A + v_B + v_D + v_E) \\ v_d &= (4/5)v_D - (1/5)(v_A + v_B + v_C + v_E) \\ v_e &= (4/5)v_E - (1/5)(v_A + v_B + v_C + v_D) \end{aligned} \tag{15.72}$$

The phase voltages in different modes are obtained by substituting leg voltages into Eq. (15.72), and their space vectors are determined using Eq. (15.68). The space vectors of phase-to-neutral voltage are identical to the leg voltage space vectors. The phase-to-neutral voltages for various modes are given in Fig. 15.28.

Fourier analysis of the voltage waveforms, which relates DC link voltage of the inverter with the output, is elaborated.

Using the definition of the Fourier series for a periodic waveform,

$$v(t) = V_o + \sum_{n=1}^{\infty}(A_n \cos n\omega t + B_n \sin n\omega t) \tag{15.73}$$

where the coefficients of the Fourier series are given with

$$\begin{aligned} V_o &= \frac{1}{T}\int_0^T v(t)dt = \frac{1}{2\pi}\int_0^{2\pi} v(\theta)d\theta \\ A_n &= \frac{2}{T}\int_0^T v(t)\cos n\omega t\,dt = \frac{1}{\pi}\int_0^{2\pi} v(\theta)\cos n\theta\,d\theta \\ B_n &= \frac{2}{T}\int_0^T v(t)\sin n\omega t\,dt = \frac{1}{\pi}\int_0^{2\pi} v(\theta)\sin n\theta\,d\theta \end{aligned} \tag{15.74}$$

Observing that the waveforms possess quarter-wave symmetry and can be conveniently taken as odd functions, one can represent phase-to-neutral voltages with the following expressions:

$$\begin{aligned} v(t) &= \sum_{n=1}^{\infty} B_{2n-1}\sin(2n-1)\omega t \quad \text{where} \quad B_{2n-1} \\ &= \frac{4}{\pi}\int_0^{\frac{\pi}{2}} v(\theta)\sin(2n-1)\theta\,d\theta \quad \text{and} \quad n = 1,2,3,\ldots \end{aligned} \tag{15.75}$$

In the case of the phase-to-neutral voltage v_b, shown in Fig. 15.28, one further has for the coefficients of the Fourier series:

$$B_{2n-1} = \frac{8V_{DC}}{5\pi(2n-1)}\left[1 + \cos(2n-1)\frac{3\pi}{5}\cos(2n-1)\frac{4\pi}{5}\right]$$

where $k = 1,2,3,\ldots$ (15.76)

The expression in brackets of Eq. (15.76) equals zero for all the harmonics whose order is divisible by five. For all the other harmonics, it equals 2.5. Hence, one can write the Fourier series of the phase-to-neutral voltage as

$$v(t)=\frac{2}{\pi}V_{DC}\left[\sin\omega t+\frac{1}{3}\sin 3\omega t+\frac{1}{7}\sin 7\omega t+\frac{1}{9}\sin 9\omega t+\frac{1}{11}\sin 11\omega t+\frac{1}{13}\sin 13\omega t+\ldots\right] \tag{15.77}$$

From (15.77), it follows that the fundamental component of the output phase-to-neutral voltage has an rms value equal to

$$V_1=\frac{\sqrt{2}}{\pi}V_{DC}=0.45V_{DC} \tag{15.78}$$

From Fig. 15.28, mean square value is determined as

$$\text{Mean square value}=\frac{1}{\pi}\left[\left(\frac{2}{5}V_{DC}\right)^2\times\frac{3\pi}{5}+\left(\frac{3}{5}V_{DC}\right)^2\times\frac{2\pi}{5}\right]=\frac{6}{25}V_{DC}^2 \tag{15.79}$$

$$V_{rms}=\frac{\sqrt{6}}{5}V_{DC} \tag{15.80}$$

Total harmonic rms voltage (per unit) is given by

$$V_{Hrms}=\sqrt{(V_{rms})^2-(V_1)^2}=\sqrt{\left(\frac{\sqrt{6}}{5}\right)^2-\left(\frac{\sqrt{2}}{\pi}\right)^2}=0.193281227 \tag{15.81}$$

Hence, total harmonic distortion is

$$THD=\frac{\text{r.m.s. total harmonic voltage}}{\text{r.m.s. total voltage}}=\frac{0.193281227}{\sqrt{6}/5}=0.3945336525 \text{ or } 39.45\% \tag{15.82}$$

This is the same voltage as obtainable with a three-phase VSI operating in six-step mode. It is important to note at this stage that the space vectors described by (15.68) provides mapping of inverter voltages into a two-dimensional space. However, since five-phase inverter essentially requires description in a five-dimensional space, not all the harmonics contained in (15.77) will be encompassed by the space vector of (15.68). In particular, space vectors calculated using (15.68) will only represent harmonics of the order $10k\pm1$, $k=0,1,2,3\ldots$, that is, the first, the ninth, the eleventh, and so on. Harmonics of the order $5k$, $k=1,2,3\ldots$ cannot appear due to the isolated neutral point. However, harmonics of the order $5k\pm2$, $k=1,3,5\ldots$ are present in (15.77) but are not encompassed by the space-vector definition of (15.68). These harmonics in essence appear in the second two-dimensional space, which requires introduction of the second space vector for the five-phase system.

Simulation is performed to obtain the harmonic spectrum of inverter phase voltage in 10-step mode of operation, shown in Fig. 15.29. The DC voltage is kept at 1 p.u. The harmonic spectrum is in compliance with the expression (15.77) and (15.78).

The fundamental component is equal to 0.4504 pu, which is the same as what is obtainable with a three-phase VSI. The subharmonic components are third and seventh in Fig. 15.29, and their magnitudes are 33.33% and 14.3%, respectively. These

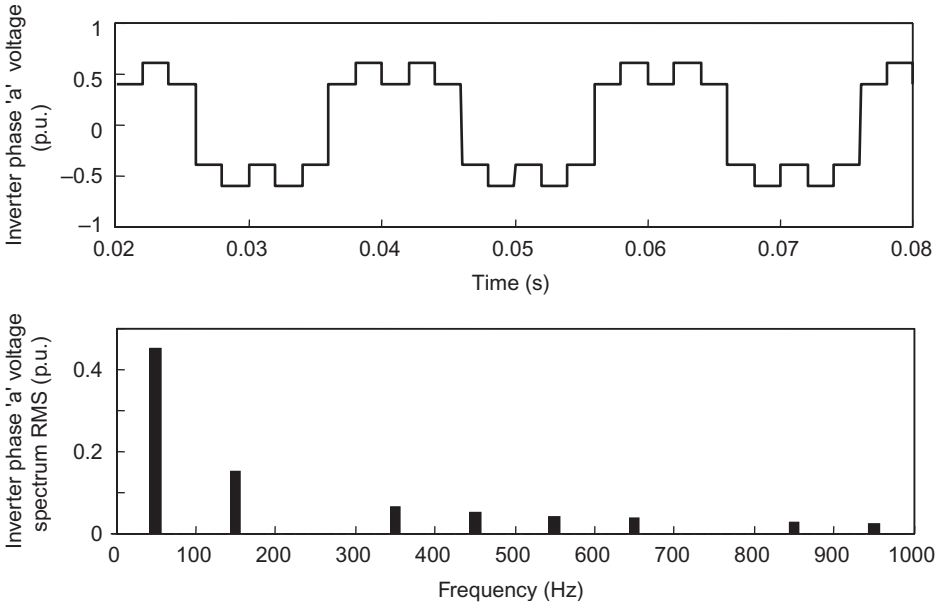


FIG. 15.29 Inverter phase "a" voltage time-domain waveform and its harmonic spectrum in frequency domain (fundamental frequency is 50 Hz, fundamental voltage 0.4504 (pu)).

subharmonics will appear in the *x-y* plane and will cause distortion in the stator currents and consequently increase the losses in the machine. The lowest harmonic appearing on *d-q* plane are 9th and 11th with their magnitude as 11.1% and 9.1%, respectively. These harmonic will further add to the losses in addition to 10th-harmonic pulsating torque under steady-state conditions.

The line-to-line voltages are expanded next. There are two systems of line-to-line voltage, adjacent and nonadjacent, in contrast to a three-phase system where only one line-to-line voltage is defined. The adjacent line-to-line voltages at the output of the five-phase inverter are defined in Fig. 15.30, for a fictitious load. Since each line-to-line voltage is a difference of corresponding two leg voltages, the values of nonadjacent line-to-line voltages will produce higher magnitude compared with the adjacent line voltages; hence, only former case is taken up in the thesis and later is omitted from further consideration.

There are two sets of nonadjacent line-to-line voltages. Due to symmetry, these two sets lead to the same values of the line-to-line voltage space vectors, with a different phase order. Only the set $v_{ac}, v_{bd}, v_{ce}, v_{da}, v_{eb}$ is analyzed for this reason. Table 15.3 lists the states and the values for these line-to-line voltages.

Space vectors of nonadjacent line-to-line voltages are determined once more using the defining expression (15.68) and are summarized as

$$\begin{bmatrix} \underline{v}_{1ll} \\ \underline{v}_{2ll} \\ \underline{v}_{3ll} \\ \underline{v}_{4ll} \\ \underline{v}_{5ll} \\ \underline{v}_{6ll} \\ \underline{v}_{7ll} \\ \underline{v}_{8ll} \\ \underline{v}_{9ll} \\ \underline{v}_{10ll} \end{bmatrix} = \frac{8}{5} V_{DC} \cos\left(\frac{\pi}{5}\right) \cos\left(\frac{\pi}{10}\right) \begin{bmatrix} e^{j\pi/10} \\ e^{j3\pi/10} \\ e^{j\pi/2} \\ e^{j7\pi/10} \\ e^{j9\pi/10} \\ e^{j11\pi/10} \\ e^{j13\pi/10} \\ e^{j15\pi/10} \\ e^{j17\pi/10} \\ e^{j19\pi/10} \end{bmatrix} \tag{15.83}$$

Time-domain waveforms of nonadjacent line-to-line voltages are illustrated in Fig. 15.31.

The Fourier analysis is further carried out for nonadjacent line-to-line voltage following the same procedure outlined in conjunction with Fourier analysis of phase voltages. The nonadjacent line voltages waveform possess quarter-wave odd symmetry; hence, the Fourier coefficient can be evaluated as

$$B_{2n-1} = \frac{4V_{DC}}{(2n-1)\pi}\left(\cos(2n-1)\frac{\pi}{10}\right) \quad \text{where} \quad n = 1,2,3,\ldots$$

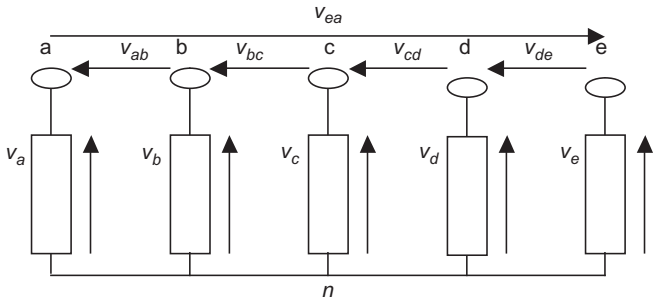


FIG. 15.30 Adjacent line-to-line voltages of a five-phase star-connected load.

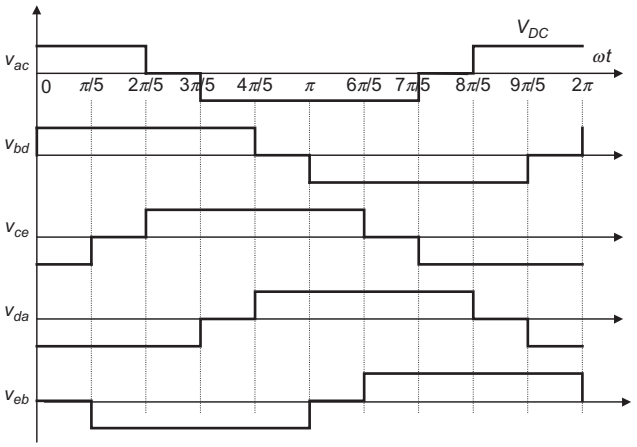


FIG. 15.31 Nonadjacent line-to-line voltages for 10-step operation of a five-phase VSI.

TABLE 15.3 Nonadjacent line-to-line voltages for 180 degrees conduction mode

Switching state	Switches ON	Space vector	v_{ac}	v_{bd}	v_{ce}	v_{da}	v_{eb}
1	9,10,1,2,3	$\underline{v}_{1ll}$	V_{DC}	V_{DC}	$-V_{DC}$	$-V_{DC}$	0
2	10,1,2,3,4	$\underline{v}_{2ll}$	V_{DC}	V_{DC}	0	$-V_{DC}$	$-V_{DC}$
3	1,2,3,4,5	$\underline{v}_{3ll}$	0	V_{DC}	V_{DC}	$-V_{DC}$	$-V_{DC}$
4	2,3,4,5,6	$\underline{v}_{4ll}$	$-V_{DC}$	V_{DC}	V_{DC}	0	$-V_{DC}$
5	3,4,5,6,7	$\underline{v}_{5ll}$	$-V_{DC}$	0	V_{DC}	V_{DC}	$-V_{DC}$
6	4,5,6,7,8	$\underline{v}_{6ll}$	$-V_{DC}$	$-V_{DC}$	V_{DC}	V_{DC}	0
7	5,6,7,8,9	$\underline{v}_{7ll}$	$-V_{DC}$	$-V_{DC}$	0	V_{DC}	V_{DC}
8	6,7,8,9,10	$\underline{v}_{8ll}$	0	$-V_{DC}$	$-V_{DC}$	V_{DC}	V_{DC}
9	7,8,9,10,1	$\underline{v}_{9ll}$	V_{DC}	$-V_{DC}$	$-V_{DC}$	0	V_{DC}
10	8,9,10,1,2	$\underline{v}_{10ll}$	V_{DC}	0	$-V_{DC}$	$-V_{DC}$	V_{DC}

And the Fourier series of nonadjacent line-to-line voltage can be written as

$$v_{ll}(t)=\frac{4}{\pi}V_{DC}\left[\begin{array}{c}\cos\left(\frac{\pi}{10}\right)\sin(\omega t)+\frac{1}{3}\cos\left(\frac{3\pi}{10}\right)\sin(3\omega t)\\ +\frac{1}{7}\cos\left(\frac{7\pi}{10}\right)\sin(7\omega t)+\ldots\end{array}\right] \tag{15.84}$$

Thus, the peak of the fundamental is

$$V_{ll}=\frac{4}{\pi}V_{DC}\cos\left(\frac{\pi}{10}\right)=1.211V_{DC} \tag{15.85}$$

From Fig. 15.31, mean square value is determined as

$$\text{Mean square value}=\frac{1}{\pi}\left[(V_{DC})^2\times\frac{4\pi}{5}\right]=\frac{4}{5}V_{DC}^2 \tag{15.86}$$

$$V_{rms}=\frac{2}{\sqrt{5}}V_{DC}=0.894427191V_{DC} \tag{15.87}$$

Total harmonic rms voltage (pu) is given by

$$V_{Hrms}=\sqrt{(V_{rms})^2-(V_1)^2}=\sqrt{\left(\frac{2}{\sqrt{5}}\right)^2-\left(\frac{2\sqrt{2}}{\pi}\cos\left(\frac{\pi}{10}\right)\right)^2}$$
$$=0.2585208456 \tag{15.88}$$

Hence, total harmonic distortion is

$$THD=\frac{\text{r.m.s. total harmonic voltage}}{\text{r.m.s. total voltage}}=\frac{0.2585208456}{2/\sqrt{5}}$$
$$=0.2890350922\ \text{ or }\ 28.9\%\ \text{ Or }\ 28.9035\% \tag{15.89}$$

15.4.1.3 Pulse Width Modulation Mode of Operation

If a five-phase voltage-source inverter is operated in PWM mode, apart from the already described 10 states, there are additional 22 switching states. These remaining 22 switching states encompass three possible situations: all the states when four switches from upper (or lower) half and one from the lower (or upper) half of the inverter are on (states 11–20), two states when either all the five upper (or lower) switches are "on" (states 31 and 32), and the remaining states with three switches from the upper (lower) half and two switches from the lower (upper) half in conduction mode (states 21–30). The corresponding space vectors for 11–30 are obtained using Eq. (15.68), and it is seen that the total of 32 space vectors, available in the PWM operation, fall into four distinct categories regarding the magnitude of the available output phase voltages. The phase voltage space vectors are summarized in Table 15.4 for all 32 switching states and are shown in Fig. 15.32.

Since adjacent line voltage yields lower output value, only nonadjacent line voltages are elaborated as well:

TABLE 15.4 Phase-to-neutral voltage space vectors for states 1–32

Space vectors	Value of the space vectors
$\underline{v}_{1phase}$ to $\underline{v}_{10phase}$	$2/5\,V_{DC}2\cos(\pi/5)\exp(jk\pi/5)$ for $k=0,1,2\ldots9$
$\underline{v}_{11phase}$ to $\underline{v}_{20phase}$	$2/5\,V_{DC}\exp(jk\pi/5)$ for $k=0,1,2\ldots9$
$\underline{v}_{21phase}$ to $\underline{v}_{30phase}$	$2/5\,V_{DC}2\cos(2\pi/5)\exp(jk\pi/5)$ for $k=0,1,2\ldots9$
$\underline{v}_{31phase}$ to $\underline{v}_{32phase}$	0

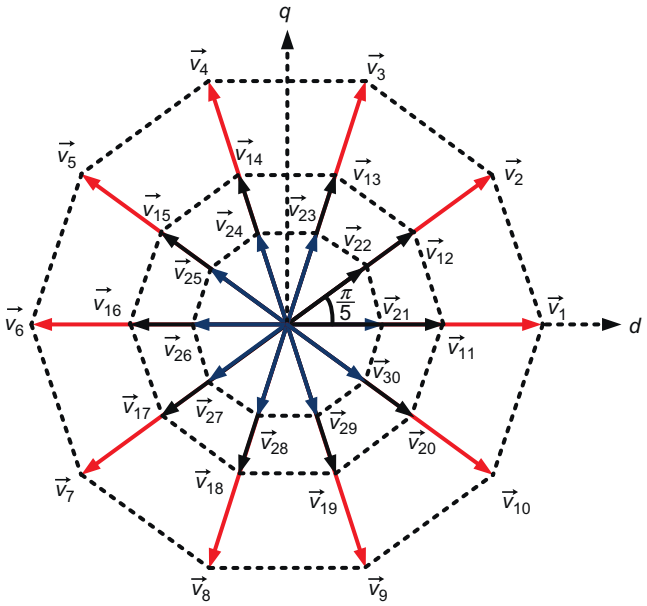


FIG. 15.32 Phase-to-neutral voltage space vectors for states 1–32 (states 31–32 are at origin) in *d*-*q* plane.

$$\begin{bmatrix}\vec{v}_{11ll}\\ \vec{v}_{12ll}\\ \vec{v}_{13ll}\\ \vec{v}_{14ll}\\ \vec{v}_{15ll}\\ \vec{v}_{16ll}\\ \vec{v}_{17ll}\\ \vec{v}_{18ll}\\ \vec{v}_{19ll}\\ \vec{v}_{20ll}\end{bmatrix}=\frac{2}{5}V_{DC}2\cos\left(\frac{\pi}{10}\right)\begin{bmatrix}e^{j\pi/10}\\ e^{j3\pi/10}\\ e^{j5\pi/10}\\ e^{j7\pi/10}\\ e^{j9\pi/10}\\ e^{j11\pi/10}\\ e^{j13\pi/10}\\ e^{j15\pi/10}\\ e^{j17\pi/10}\\ e^{j19\pi/10}\end{bmatrix} \tag{15.90}$$

$$\begin{bmatrix}\vec{v}_{21ll}\\ \vec{v}_{22ll}\\ \vec{v}_{23ll}\\ \vec{v}_{24ll}\\ \vec{v}_{25ll}\\ \vec{v}_{26ll}\\ \vec{v}_{27ll}\\ \vec{v}_{28ll}\\ \vec{v}_{29ll}\\ \vec{v}_{30ll}\end{bmatrix}=\frac{2}{5}V_{DC}2\cos\left(\frac{3\pi}{10}\right)\begin{bmatrix}e^{j\pi/10}\\ e^{j3\pi/10}\\ e^{j5\pi/10}\\ e^{j7\pi/10}\\ e^{j9\pi/10}\\ e^{j11\pi/10}\\ e^{j13\pi/10}\\ e^{j15\pi/10}\\ e^{j17\pi/10}\\ e^{j19\pi/10}\end{bmatrix} \tag{15.91}$$

15.4.1.4 Model Transformation Using Decoupling Matrix

Since the system under discussion is a five-phase one, the complete model can be only be elaborated in five-dimensional space. The first two-dimensional spaces are *d-q*, the second one is named as *x-y*, and the last is zero-sequence components that are absent due to the assumption of isolated neutral. On the basis of the general decoupling transformation matrix for an *n*-phase system, inverter voltage space vectors in the second two-dimensional subspace (*x-y*) are determined with Eq. (15.92):

$$\underline{v}_{xy}^{INV} = \frac{2}{5}\left(v_a + \underline{a}^2 v_b + \underline{a}^4 v_c + \underline{a} v_d + \underline{a}^3 v_e\right) \tag{15.92}$$

Thus, 32 space vectors of phase-to-neutral voltage in the *x-y* plane are obtained using Eq. (15.92) and are demonstrated in Fig. 15.33.

It can be seen from Figs. 15.32 and 15.33 that the outer decagon space vectors of the $d-q$ plane map into the innermost decagon of the *x-y* plane, the innermost decagon of *d-q* plane forms the outer decagon of *x-y* plane while the middle decagon space vector map into the same region. Further, it is observed from the above mapping that the phase sequence *a,b,c,d,e* of $d-q$ plane corresponds to *a,c,e,b,d* in *x-y* that are basically the third harmonic voltages.

15.4.1.5 Hardware Implementation of a Five-Phase VSI in 180 Conduction Mode

Hardware can be developed to implement the square-wave operation of a five-phase voltage-source inverter. The hardware can be developed using available power switch modules from different manufacturers such as Semikron, Mitsubishi, and Fairchild. The power switches are available in discrete form to implement inverter system. The gate driver circuit is also available from different manufacturers. The control can be implemented using microcontroller, digital signal processors (DSP), dSpace, and field-programmable gate arrays (FPGA). The control codes can be written in C/C++. Some of the DSPs and FPGAs are compatible with Matlab/Simulink, and hence, control codes can be implemented directly. In FPGA, system generator is used for writing the control code. System generator is a library in Matlab/Simulink software. The coding is done in the form of drag and drop in system generator.

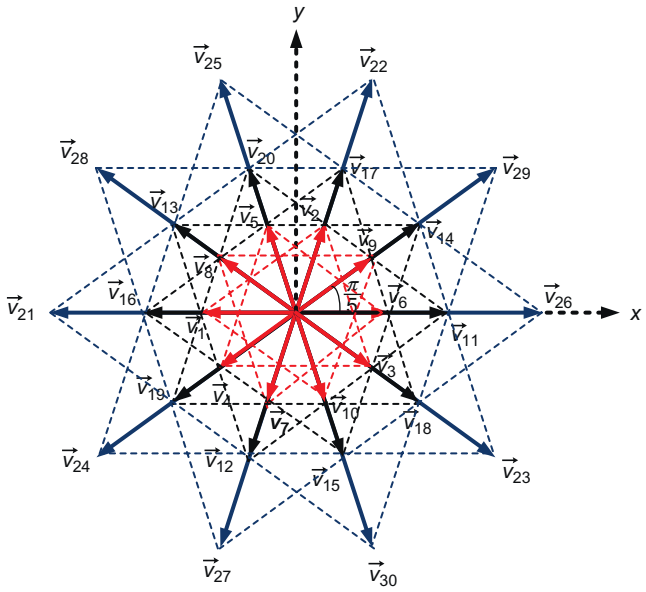


FIG. 15.33 Phase-to-neutral voltage space vectors for states 1–32 (states 31–32 are at origin) in *x-y* plane.

15.4.1.6 Hardware Set-up

The control of inverter can be implemented using sophisticated controllers such as microcontroller, digital signal processors (DSP), dSpace, and field-programmable gate arrays (FPGA). The output voltages from these controllers are generally 3.3 V that is not enough for turning on the IGBTs/MOSFETs/BJT. Further to turn off the power switching devices, the gate capacitors are to be fully and rapidly discharged. Gate drive circuit is thus required to match the voltage level requirement of turning on the power switches (about 15 V), and a discharge path for the gate capacitor is needed. Hence, a gate drive circuit is needed to successfully turn on and turn off the power devices. The following section describes the implementation of the control, gate drive, and power circuit using analog devices. The complete block diagram is shown in Fig. 15.34.

Power supply is obtained from a single-phase grid and is converted to 9-0-9 V using a transformer. The converted voltage of (9-0-9 V) is fed to the phase-shifting circuit shown in Fig. 15.35, to provide appropriate phase shift for operation at various conduction angle (the conduction angle refers to the conduction modes of inverter, e.g., 180, 144, and 108 degrees). The phase-shifted signal is then fed to the inverting/noninverting Schmitt trigger circuit and wave-shaping circuit (Figs. 15.36 and 15.37). The processed signal is then fed to the isolation and driver circuit shown in Fig. 15.38. This is then finally given to the gate of IGBTs. There are two separate circuits for upper and lower legs of the inverter.

The power circuit is made up of IGBT SGW20N60 having a rating of 20 A and 600 V DC, with snubber circuit consisting of the series combination of a resistance and a capacitor with a diode in parallel with the resistance.

15.4.1.7 Hardware Results

Experiment can be conducted for stepped operation of inverter with 180 degrees conduction modes for star-connected five-phase resistive load. A single-phase supply can be given to the control circuit through the phase-shifting network. The output of the phase-shifting circuit provides the required five-phase output voltage by appropriately tuning it. These five-phase signals are then further processed to generate the gate drive circuit.

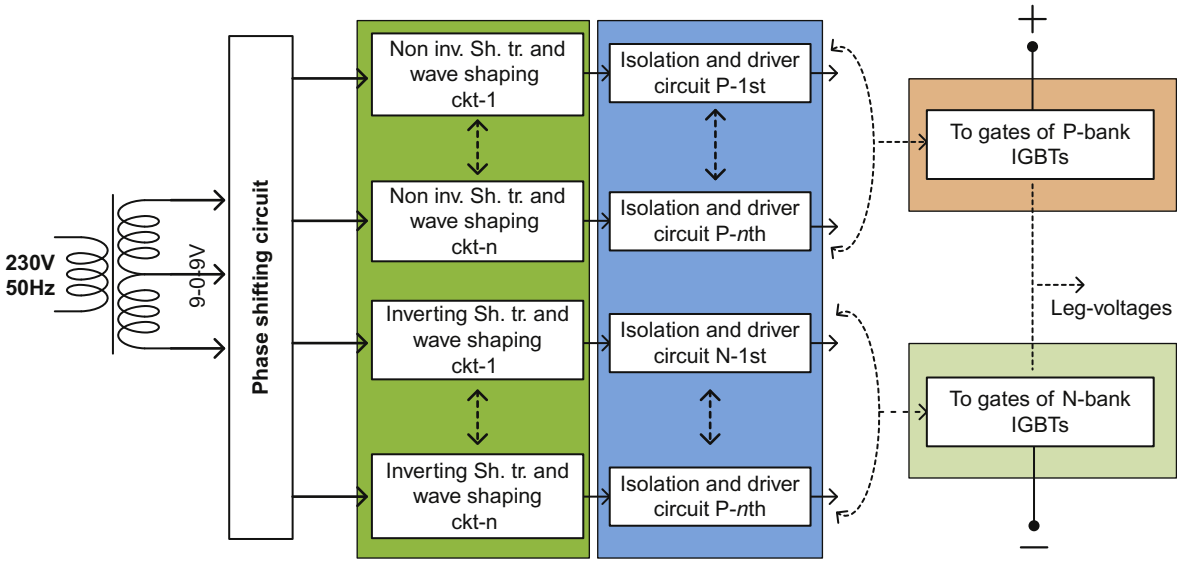


FIG. 15.34 Block diagram of the control circuit.

15.4.1.8 Results of 180 Degrees Conduction Mode

The output from the Schmitt trigger circuit is presented in Fig. 15.39. The driving control gate/base signals for the 10-step mode for legs A–B of the inverter are illustrated in Fig. 15.40. The corresponding phase voltage thus obtained is shown in Fig. 15.41, keeping the DC-link voltage at 60 V. The output phase voltage is called 10 step in one fundamental cycle ($1/5V_{dc}$, $2/5V_{dc}$, $1/5V_{dc}$, $2/5V_{dc}$, $1/5V_{dc}$, $-1/5V_{dc}$, $-2/5V_{dc}$, $-1/5V_{dc}$, $-2/5V_{dc}$, and $-1/5V_{dc}$).

Nonadjacent line voltage obtained is shown in Fig. 15.42. All currents are measured using AC/DC current probe giving the output of 100 mV/A.

The AC side input current is also measured and is depicted in Fig. 15.43. The analysis is presented in the last subsection.

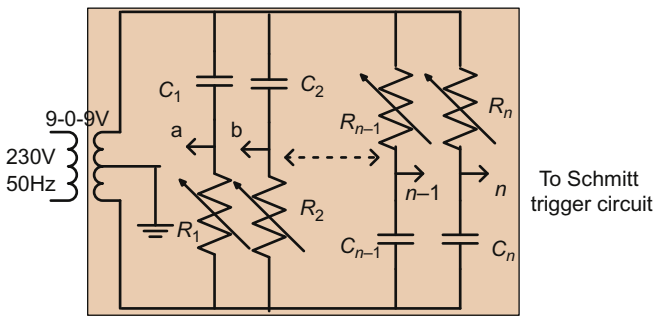


FIG. 15.35 Phase-shifting circuit (PSC).

15.4.1.9 DSP Implementation of Step Mode of Operation

The results obtained in Section 15.4.1.9 are verified using implementation through TMS320F2812 DSP under the same operating conditions. Control code is written in C++ and run in PC. It is transferred to the DSP using serial communication cable RS232. The DSP generate 10 gating signals that are fed to the power module of the inverter. The detail experimental setup is provided in Section 15.4.1.10. All the three conduction angles are implemented. The developed algorithm

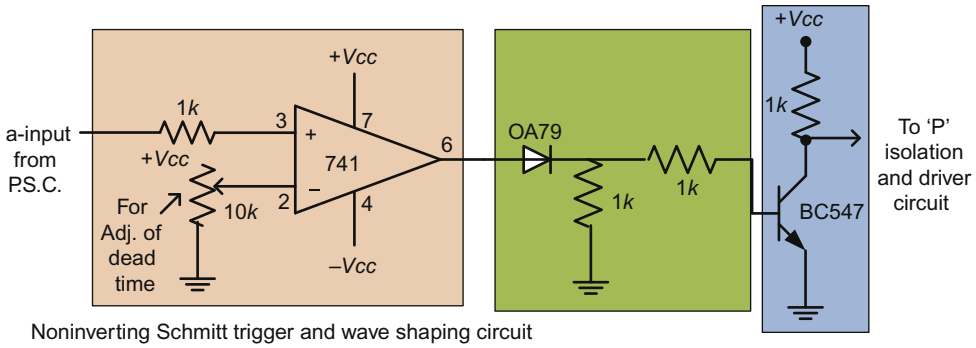


FIG. 15.36 Noninverting Schmitt trigger and wave-shaping circuit.

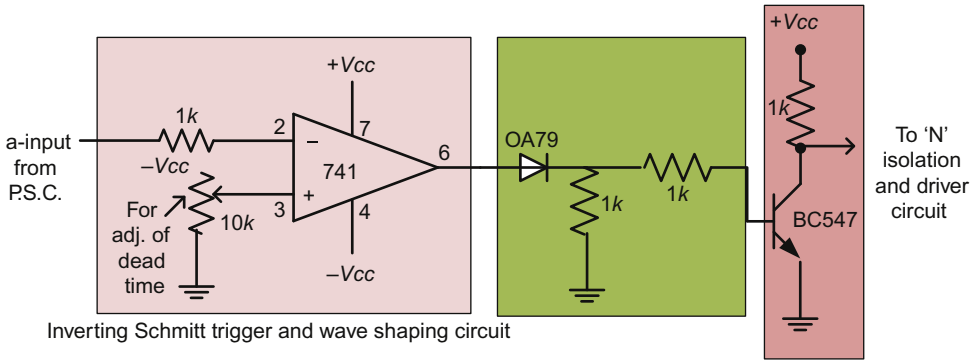


FIG. 15.37 Inverting Schmitt trigger and wave-shaping circuit.

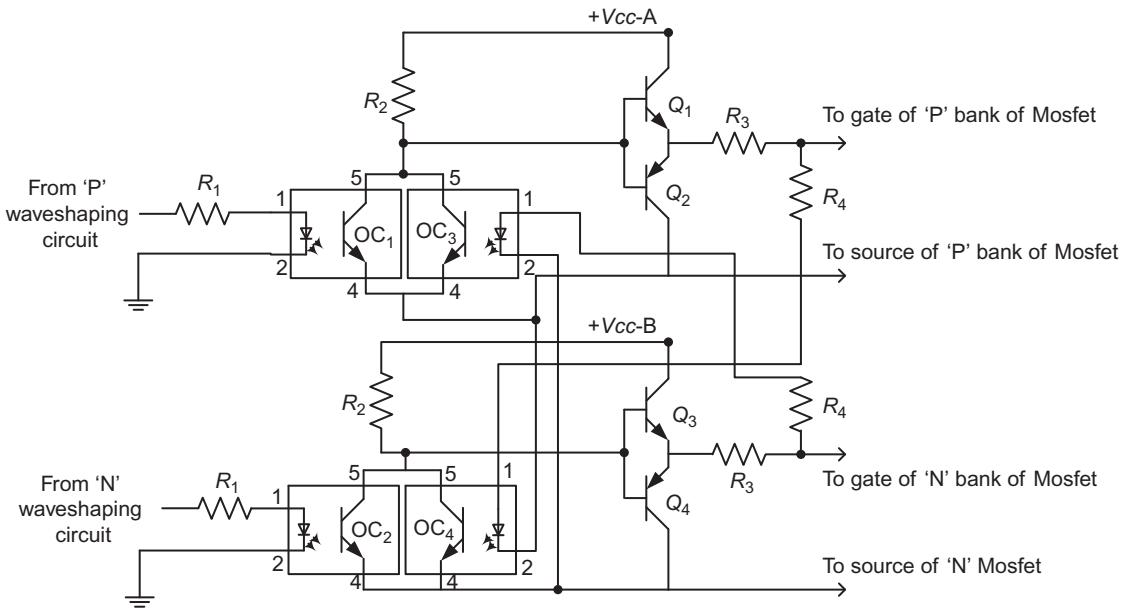


FIG. 15.38 Gate driver circuit.

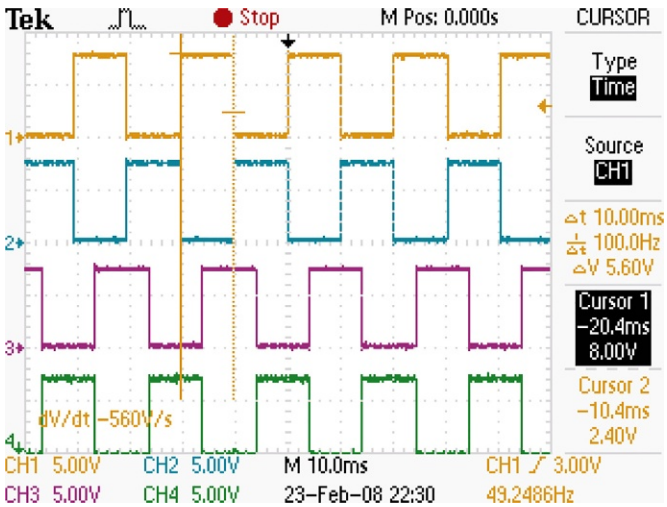


FIG. 15.39 Output of wave-shaping circuit for 180 degrees conduction mode for leg A–B.

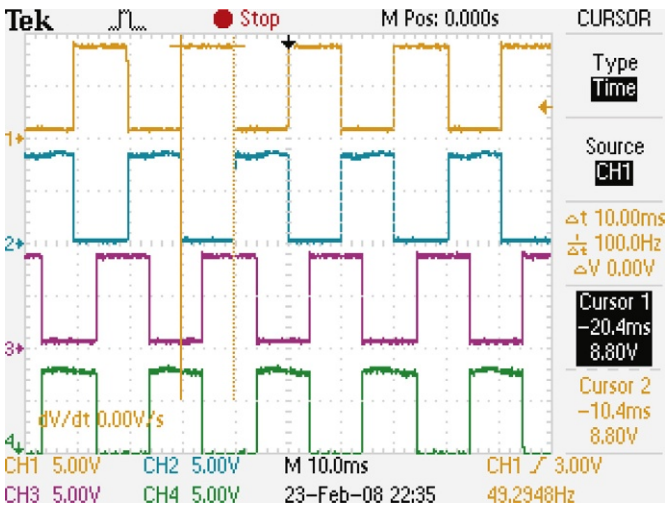


FIG. 15.40 Gate drive signals for legs A–B for 180 degrees conduction mode.

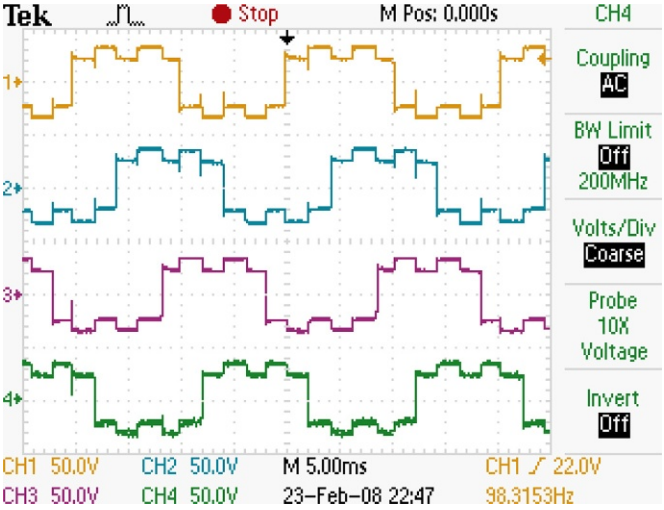


FIG. 15.41 Output phase "a–d" voltages for 180 degrees conduction mode.

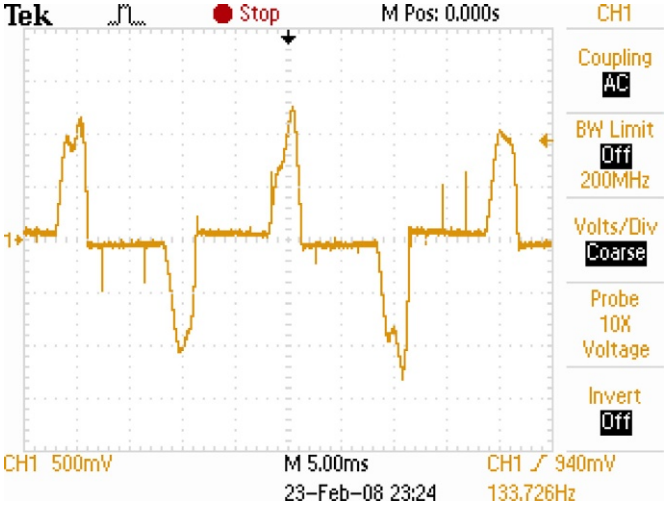


FIG. 15.43 AC side input current for 180 degrees conduction mode.

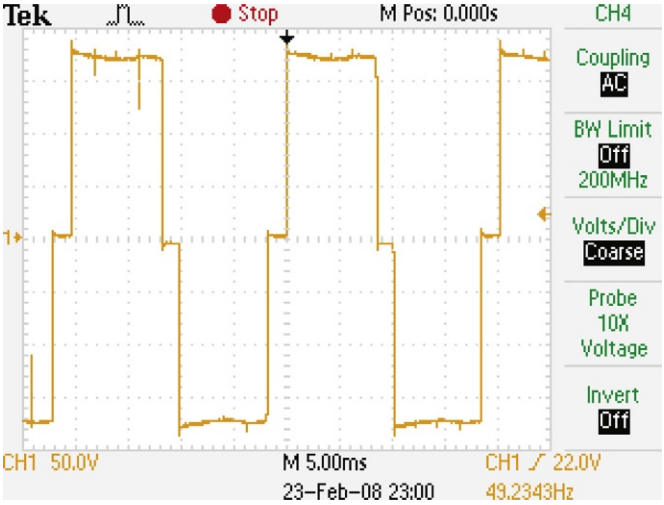


FIG. 15.42 Nonadjacent line voltage for 180 degrees conduction mode with DC-link voltage equal to 180 V.

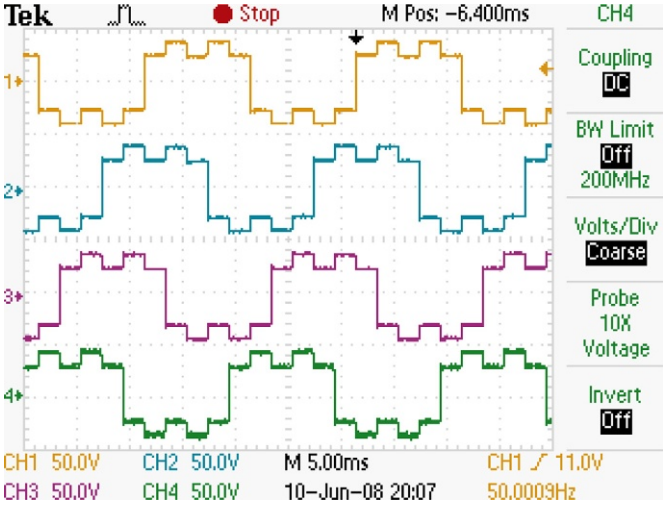


FIG. 15.44 Output phase voltage for 180 degrees conduction mode.

is verified using a star-connected resistive load and a five-phase induction machine.

15.4.1.10 180 Degrees Conduction Mode

The inverter is operated in 180 degrees conduction mode, and a five-phase star-connected resistive load is connected across the output terminal. The resulting phase voltage, nonadjacent line voltages are illustrated in Figs. 15.44 and 15.45, respectively.

It is observed that the phase voltage generated using cheap analog-circuit-based inverter shown in Fig. 15.41 is identical to the one obtained using DSP as shown in Fig. 15.44. Similarly, the nonadjacent line voltage of Fig. 15.42 is identical to the one shown in Fig. 15.45. This verifies the correct design of the analog-based inverter and also verifies the DSP code. The same study is carried out using a five-phase induction motor as a load. The resulting voltage and stator current waveforms are presented in Fig. 15.46. The waveform is typical for such load.

15.4.2 Carrier-Based PWM

15.4.2.1 With Zero Sequence Signal

Carrier-based sinusoidal PWM is the most popular and widely used PWM technique because of their simple implementation in both analog and digital realization [32,34]. The principle of carrier-based PWM true for a three-phase VSI is also applicable to a multiphase VSI. The PWM signal is generated by comparing a sinusoidal modulating signal with a triangular (double edge) or a saw-tooth (single edge) carrier signal. The frequency of the carrier is normally kept much higher compared to the

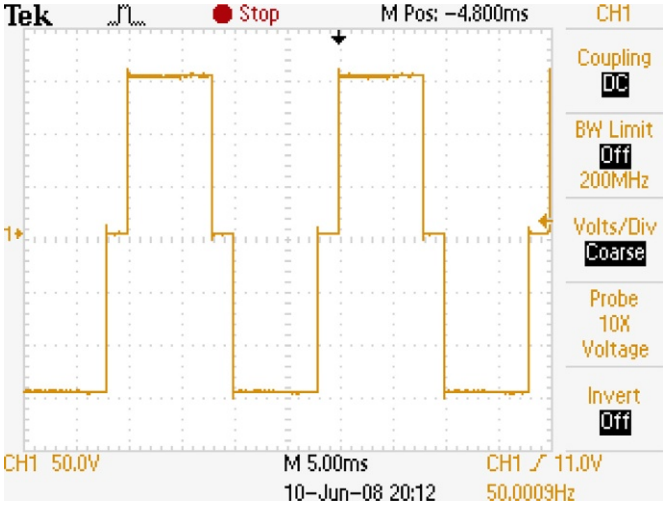


FIG. 15.45 Nonadjacent line voltage for 180 degrees conduction mode.

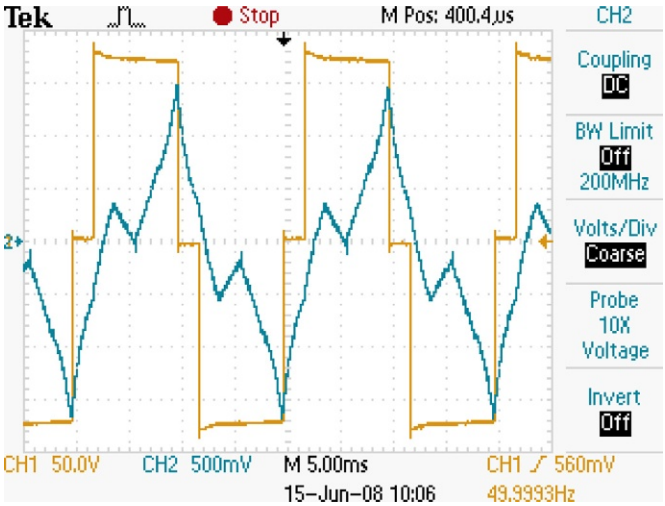


FIG. 15.46 Nonadjacent line voltage and stator current.

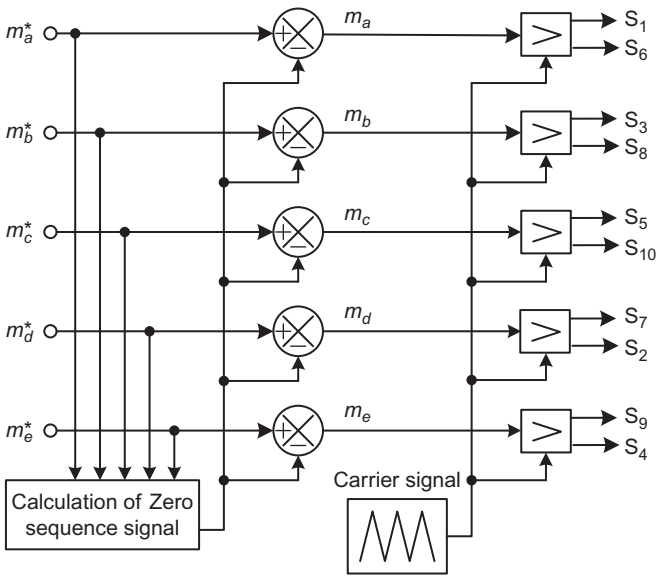


FIG. 15.47 Principle of carrier-based PWM technique.

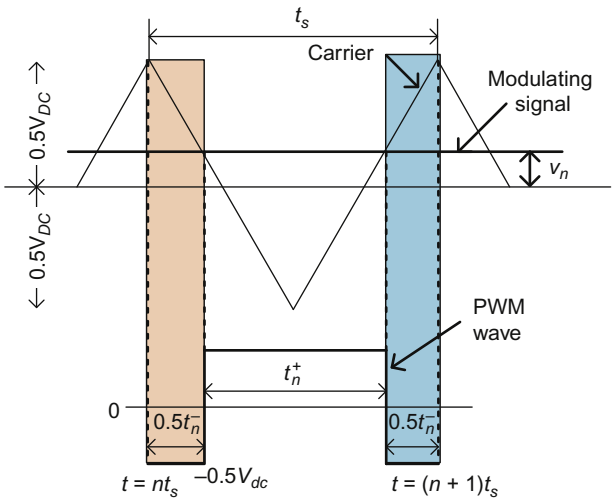


FIG. 15.48 PWM waveform generation in carrier-based sinusoidal method.

modulating signal. The principle of operation of a carrier-based PWM modulator is shown in Fig. 15.47, and generation of PWM waveform is illustrated in Fig. 15.48. Modulation signals are obtained using five fundamental sinusoidal signals (displaced in time by $\alpha = 2\pi/5$), which are summed with an appropriate zero-sequence signal. These modulation signals are compared with high-frequency carrier signal (saw-tooth or triangular shape), and all five switching functions for inverter legs are obtained directly. In general, modulation signal can be expressed as

$$v_i(t) = v_i^*(t) + v_{nN}(t) \tag{15.93}$$

where $i = a,b,c,d,e$ and v_{nN} represents zero-sequence signal and v_i^* is fundamental sinusoidal signals. Zero-sequence signal represents a degree of freedom that exits in the structure of a carrier-based modulator, and it is used to modify modulation signal waveforms and thus to obtain different modulation schemes. Continuous PWM schemes are characterized by the presence of switching activity in each of the inverter legs over the carrier signal period, as long as peak value of the modulation signal does not exceed the carrier magnitude.

The following relationship holds true in Fig. 15.48:

$$t_n^+ - t_n^- = v_n t_s \tag{15.94}$$

where

$$t_n^+ = \left(\frac{1}{2} + v_n\right) t_s \tag{15.95}$$

$$t_n^- = \left(\frac{1}{2} - v_n\right) t_s \tag{15.96}$$

where t_n^+ and t_n^- are the positive and negative pulse widths in the nth sampling interval, respectively, and v_n is the normalized amplitude of modulation signal. The normalization is done with respect to V_{dc}. Eqs. (15.95) and (15.96) are referred as the equal volt-second principle as applied to a three-phase inverter [32,35,36]. The normalized peak value of the triangular carrier wave is ±0.5 in linear region of operation. Modulator gain has the unity value while operating in the linear region, and peak value of inverter output fundamental voltage is equal to the peak value of the fundamental sinusoidal signal. Thus, the maximum output phase voltages from a five-phase VSI are limited to 0.5 p.u. This is also evident in [32,37]. Thus, the output phase voltage from a three-phase and a five-phase VSI are the same when utilizing carrier-based PWM.

15.4.2.2 Sinusoidal Pulse Width Modulation (SPWM)

The simplest continuous carrier-based PWM is obtained with the selection of the zero-sequence signal as $v_{vN}(t) = 0$. Modulation signals for all five inverter legs are equal to five sinusoidal fundamental signals. Thus, while operating in the linear region, maximum value of the modulation index of the SPWM has the unity value, $M_{SPWM} = 1$. Modulation index is defined as the ratio of the fundamental component amplitude of the line-to-neutral inverter output voltage to one-half of the available DC bus voltage. Thus,

$$M = \frac{V_1}{0.5 V_{dc}} \tag{15.97}$$

where V_1 is the fundamental output phase voltage.

15.4.2.3 Fifth Harmonic Injection PWM

The effect of the addition of harmonic with reverse polarity in any signal is to reduce the peak of the reference signal. Aim here is to bring the amplitude of the reference as low as possible, so that the reference can then be pushed to make it equal to the carrier, resulting in the higher output voltage and better DC bus utilization. Using this principle, third harmonic injection PWM scheme is used in a three-phase VSI that results in increase in the fundamental output voltage to $0.575 V_{dc}$ [32,35]. Third harmonic voltages do not appear in the output phase voltages and are restricted to the leg voltages only. Following the same principle, fifth harmonic injection PWM scheme can be developed to increase the modulation index of a five-phase VSI.

The reference leg voltages are given as

$$\begin{aligned}
V_{ao}^* &= 0.5 M_1 V_{dc} \cos(\omega t) + 0.5 M_5 V_{dc} \cos(5\omega t) \\
V_{bo}^* &= 0.5 M_1 V_{dc} \cos(\omega t - 2\pi/5) + 0.5 M_5 V_{dc} \cos(5\omega t) \\
V_{co}^* &= 0.5 M_1 V_{dc} \cos(\omega t - 4\pi/5) + 0.5 M_5 V_{dc} \cos(5\omega t) \\
V_{do}^* &= 0.5 M_1 V_{dc} \cos(\omega t + 4\pi/5) + 0.5 M_5 V_{dc} \cos(5\omega t) \\
V_{eo}^* &= 0.5 M_1 V_{dc} \cos(\omega t + 2\pi/5) + 0.5 M_5 V_{dc} \cos(5\omega t)
\end{aligned} \tag{15.98}$$

It is to be noted that fifth harmonic has no effect on the value of the reference waveform when $\omega t = (2k+1)\pi/10$, since $\cos(5(2k+1)\pi/10) = 0$ for all odd k. Thus, M_5 is chosen to make the peak magnitude of the reference of (15.98) that occurs where the fifth harmonic is zero. This ensures the maximum possible value of the fundamental component. The reference voltage reaches a maximum when

$$\frac{dV_{ao}^*}{dt} = -0.5 M_1 V_{dc} \sin \omega t - 0.5 \cdot 5 M_5 V_{dc} \sin 5\omega t = 0 \tag{15.99}$$

This yield

$$M_5 = -M_1 \frac{\sin(\pi/10)}{5} \quad \text{for} \quad \omega t = \pi/10 \tag{15.100}$$

Thus, the maximum modulation index can be determined from

$$\begin{aligned}
\left|V_{ao}^*\right| &= \left|0.5 M_1 V_{dc} \cos(\omega t) - 0.5 \frac{\sin(\pi/10)}{5} M_1 V_{dc} \cos(3\omega t)\right| \\
&= 0.5 V_{dc}
\end{aligned} \tag{15.101}$$

The above equation gives

$$M_1 = \frac{1}{\cos(\pi/10)} \quad \text{for} \quad \omega t = \pi/10 \tag{15.102}$$

Thus, the output fundamental voltage is increased by 5.15% higher than the value obtainable using simple carrier-based PWM by injecting 6.18% fifth harmonic in fundamental. The fifth harmonic is in opposite phase to that of the fundamental.

15.4.2.4 Offset or Triangular Zero-Sequence Injection PWM

Another way of increasing the modulation index is to add an offset voltage to the references. This will effectively do the same function as above. The offset voltage is given as

$$V_{offest} = -\frac{V_{\max} + V_{\min}}{2} \tag{15.103}$$

where $v_{\max} = \max(v_a, v_b, v_c, v_d, v_e)$ and $v_{\min} = \min(v_a, v_b, v_c, v_d, v_e)$. Note that this is the same as for a three-phase inverter.

In case of three-phase VSI, the offset voltage is simply third harmonic triangular wave of 25% magnitude of fundamental. The peak of the fundamental is 0.575 p.u., (0.406 p.u. rms), the peak of the resultant modulating signal is 0.5 p.u. (0.353 p.u. rms), and the peak of the offset is 0.147 p.u. (0.104 p.u. rms). Hence, offset peak is 25% of the fundamental peak.

In a five-phase VSI, the offset is found as the fifth-harmonic triangular wave of 9.55% of the fundamental input reference. This value has been established by simulations. Offset addition requires only addition operation and hence is suitable for practical implementation.

A generalized formula of offset voltage is obtained, which is to be injected along with the fundamental in case of five-phase VSI. The expression is

$$V_{no} = -0.5528(V_{\max} - V_{\min}) + 3/5(1-2\mu)V_{DC}/2 - 3/5(1-2\mu)(V_{\max} - V_{\min})$$

where $V_{\max}$ is the maximum of the five-phase references, $V_{\min}$ is the minimum of the five-phase references, and μ is the factor that decides the placement of the two zero-vector states. If it is 0.5, then the two zero states are placed equally, and this corresponds to symmetrical zero-vector placement.

It is important to note that not only the fifth harmonic but also all the additional $5k$ ($k=1,3,5\ldots$) harmonics are included in the modulation signal in this technique. Maximum modulation index has the same value as in the previous case, $M_{TIPWM} = 1.0515$. To illustrate the effects of fifth-harmonic and triangular signal injection, the overall modulating signals are shown in Fig. 15.49.

In general, an extension of the linear region is obtained through the repositioning of the peak value of the modulating signal. While sinusoidal fundamental signals have peak values at $\frac{l\pi}{2}$, zero sequence modifies this, and now, peak values of the modulating signals occur at $\frac{l\pi}{2} \pm \frac{\pi}{2n}$, $l=1,3,5,\ldots$ Hence, for five-phase carrier-based continuous PWM methods with zero-sequence signal addition, new peak values of modulating signals appear at angles $\frac{l\pi}{2} \pm \frac{\pi}{10}$. This allows the peak value of the fundamental signal to exceed unity, up to the value when peak of the modulating signal reaches saturation level ($\pm 0.5V_{dc}$, in accordance with (15.97)). It is obvious from Fig. 15.49 that fifth-harmonic injection and offset injection have the same maximum value of the modulation index in the limit of the linear region.

15.4.2.5 Space Vector Pulse Width Modulation

Space-vector pulse-width modulation has become one of the most popular PWM techniques because of its easier digital implementation and higher DC bus utilization, when compared with the sinusoidal PWM method. The principle of SVPWM lies in the switching of inverter in a special way to apply a set of space vector for specific time. There is a lot of flexibility available in choosing the proper space-vector combination for an effective control of multiphase VSIs because of the large numbers of space vectors available in multiphase power converters.

Advantages of space vector PWM:

i. SVPWM increases fundamental output without distorting line-to-line waveform.
ii. The fundamental output of SVPWM is 94.02% that is 15.47% greater than sinusoidal PWM of 78.55% fundamental.
iii. SVPWM compares a single modulating wave with a carrier instead of using three waves.
iv. When the neutral of the load is connected to a DC supply voltage, SVPWM considers interaction among phases, whereas other PWM method does not.

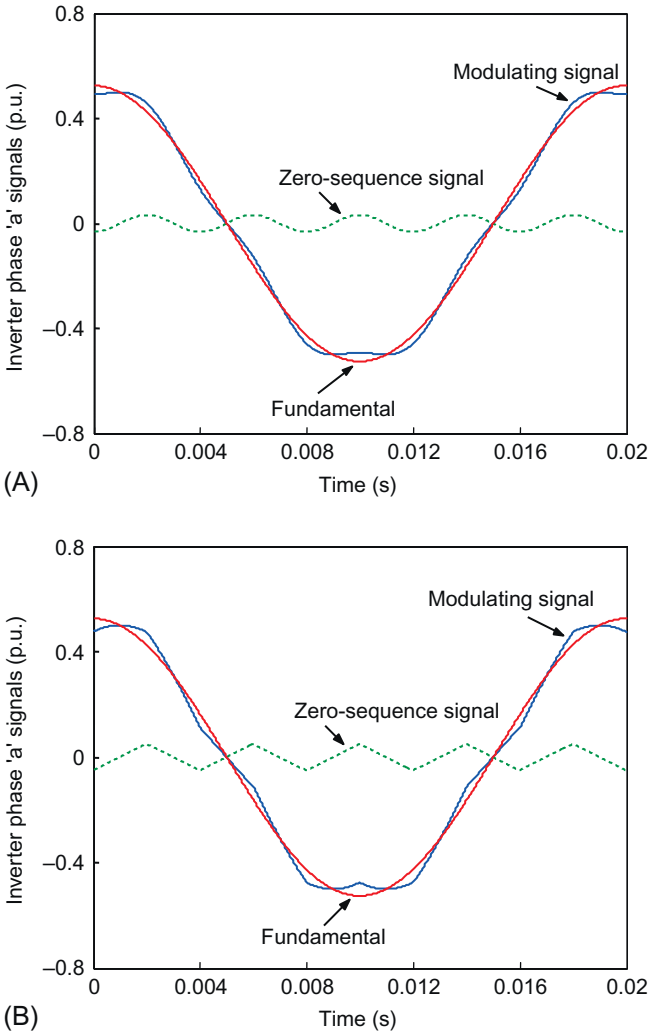


FIG. 15.49 Characteristics signals of carrier-based PWM (A) with fifth-harmonic injection and (B) with triangular harmonic injection.

v. Designing of heat sinks is an important factor for power dissipation. Power dissipation includes conduction and switching loss. Switching losses in sine PWM is difficult to compute that depend on modulation index, while computation is easier in space-vector PWM.
vi. SVPWM implementation is completely digital.
vii. Vector control implementation is completely digital, and thus, it is easy to implement SVPWM-based vector control scheme.
viii. Over modulation can easily be implemented.
ix. For high modulation index, the harmonics of current and torque of space-vector PWM will be much less than sine PWM.

In the case of a five-phase VSI, there are a total of $2^5 = 32$ space vectors available, of which 30 are active state vectors and two are zero state vectors forming three concentric decagons. For the implementation of space-vector PWM in linear range, two different approaches can be adopted. One approach is the

simple extension of method used in a three-phase inverter (use of two adjacent large length vectors) and second approach where four adjacent vectors are used (two large and two medium lengths). The first approach gives higher output voltage; however, the output voltages contain lower-order harmonics, more specifically, the third and seventh. The second approach offers sinusoidal output voltage; however, the magnitude is lower.

The first approach used only 10 outer large length vectors to implement the symmetrical SVPWM. Two neighboring active space vectors and two zero space vectors are utilized in one switching period to synthesize the input reference voltage. In total, 20 switchings take place in one switching period, so that the state of each switch is changed twice. The switching is done in such a way that, in the first switching half period, the first zero vector is applied, followed by two active state vectors and then by the second zero state vector. The second switching half period is the mirror image of the first one. The symmetrical SVPWM is achieved in this way. This method is the simplest extension of space-vector modulation of three-phase VSIs.

An ideal SVPWM of a five-phase inverter should satisfy a number of requirements. Firstly, in order to keep the switching frequency constant, each switch can change state only twice in the switching period (once "on" to "off" and once "off" to "on" or vice versa). Secondly, the rms value of the fundamental phase voltage of the output must be equal to the rms of the reference space vector. Thirdly, the scheme must provide full utilization of the available DC bus voltage. Finally, since the inverter is aimed at supplying the load with sinusoidal voltages, the low-order harmonic content needs to be minimized (this especially applies to the third and seventh harmonic). These criteria are used in assessing the merits and demerits of various SVPWM.

15.4.2.6 Space Vector PWM for Sinusoidal Output

The purpose here is to generate sinusoidal output phase voltages using space-vector PWM. Application of two neighboring medium active space vectors together with two large active space vectors in each switching period makes it possible to maintain zero average value in the second plane and consequently providing sinusoidal output. Use of four active space vectors per switching period requires the calculation of four application times, labeled here $t_{ab}, t_{bb}, t_{am}, t_{bm}$. The expressions used for the calculation of dwell times of various space vector are [32,38]

$$
\begin{aligned}
t_{al} &= \frac{|v_s^*|}{V_m \sin(\pi/5)} \left(\frac{\tau}{1+\tau^2}\right) t_s \sin\left(\frac{\pi}{5}k - \alpha\right) \\
t_{bl} &= \frac{|v_s^*|}{V_m \sin(\pi/5)} \left(\frac{\tau}{1+\tau^2}\right) t_s \sin\left(\alpha - (k-1)\frac{\pi}{5}\right) \\
t_{am} &= \frac{|v_s^*|}{V_m \sin(\pi/5)} \left(\frac{1}{1+\tau^2}\right) t_s \sin\left(\frac{\pi}{5}k - \alpha\right) \\
t_{bm} &= \frac{|v_s^*|}{V_m \sin(\pi/5)} \left(\frac{1}{1+\tau^2}\right) t_s \sin\left(\alpha - (k-1)\frac{\pi}{5}\right) \\
t_0 &= t_s - t_{al} - t_{bl} - t_{am} - t_{bm}
\end{aligned}
\tag{15.104}
$$

where $t_a = t_{al} + t_{am}$; $t_b = t_{bl} + t_{bm}$. This is in essence allocates 61.8% more dwell times to large space vectors compared with medium space vector, thus satisfying the constraints of producing zero average voltage in the x-y plane. This can be more clearly seen from Fig. 15.50.

It is seen from Fig. 15.50 that the vectors in x-y plane are in such a position to cancel each other by using the dwell time Eq. (15.104). The applications of active and zero space vectors are arranged in such a way as to obtain a symmetrical SVPWM. The space-vector disposition in sector I is illustrated in Fig. 15.51. Modulation signals of SVPWM are identical to those obtained with offset addition. Switching pattern is a symmetrical PWM with two commutations per inverter leg. The space vectors are applied in odd sectors using sequence $[\underline{v}_{31}, \underline{v}_{al}, \underline{v}_{bm}, \underline{v}_{am}, \underline{v}_{bl}, \underline{v}_{32}, \underline{v}_{bl}, \underline{v}_{am}, \underline{v}_{bm}, \underline{v}_{al}, \underline{v}_{31}]$, while the sequence is $[\underline{v}_{31}, \underline{v}_{bl}, \underline{v}_{am}, \underline{v}_{bm}, \underline{v}_{al}, \underline{v}_{32}, \underline{v}_{al}, \underline{v}_{bm}, \underline{v}_{am}, \underline{v}_{bl}, \underline{v}_{31}]$ in even sectors.

It can be easily observed from Eq. (15.104) that the zero-vector application time remains positive for $0 \leq |v_s^*| \leq 0.5257 V_{dc}$. Thus, the output phase voltage from a VSI using this Space Vector PWM scheme is $0.5257 V_{dc}$, which is 5.15% higher compared with the output obtainable with carrier-based sinusoidal PWM without harmonic injection and equal to the output obtainable with zero-sequence (fifth-harmonic) signal injection.

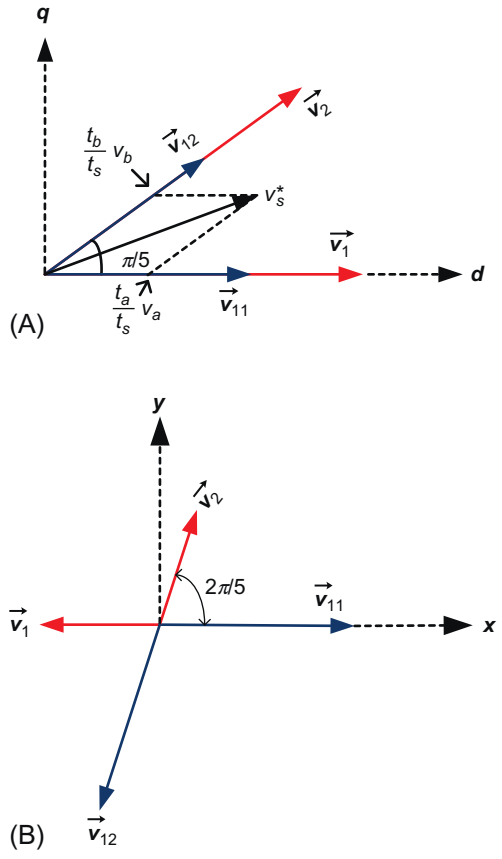


FIG. 15.50 Principle of the calculation of vector application times, (A) d-q plane and (B) x-y plane.

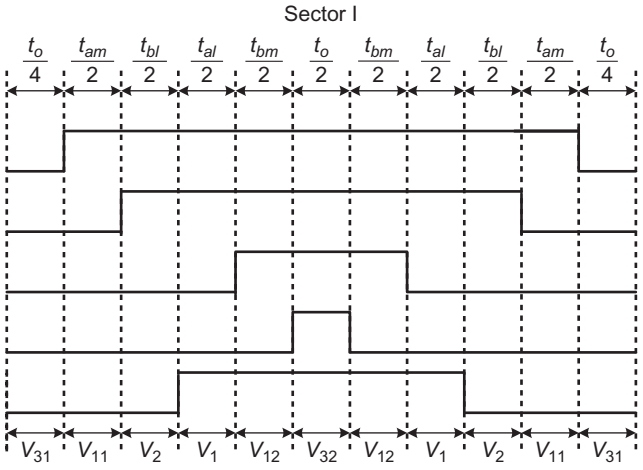


FIG. 15.51 Switching pattern in sector I using large and medium space vectors.

Simulation is carried out using Matlab/Simulink to implement the SVPWM with application of four active and a zero vector. The resulting waveform and harmonic spectrum are shown in Fig. 15.52. The average leg voltage is depicted in Fig. 15.51, and it is observed that the leg voltage is now quite similar to one obtained in three-phase VSI. The phase voltage is completely sinusoidal without any low-order harmonics. The spectrum of phase voltage shows the maximum achievable output equals to 0.5257 p.u. (keeping DC-link voltage equals to unity).

15.4.2.7 Experimental Implementation

Experimental setup is prepared in the laboratory to implement the carrier-based and space-vector PWM techniques discussed in the previous section. A five-phase voltage-source inverter is developed using intelligent power module. Texas Instrument DSP TMS320F2812 is used as the processor to implement the control algorithm. Since this DSP can be coded in C or C ++, it is more user-friendly, and they have dedicated 16 hardware PINS to generate the desired PWM signals. The PWM circuits associated with compare units make it possible to generate up to eight PWM output channels (per Event Manger) with programmable dead band and polarity. This DSP is specifically meant for use in motor drive purposes, and it can control up to eight-phase two-level inverter. The control code is written in C ++ language in Code composer studio 3.1 that runs in a PC. The control signal generated by PC is transferred to the DSP board through RS 232 cable connected in parallel printer port of the PC. The DSP board is connected to the power module through dedicated control cable. The DSP interfacing circuit along with required A/D and D/A converter is built on the DSP board itself procured from VI Microsystems.

Five-phase carrier-based PWM is implemented keeping the switching frequency equal to 10 kHz. The resulting waveform of leg voltage and corresponding phase voltage along with phase 'a', 'b', and 'c' are shown in Figs. 15.53 and 15.54, respectively.

Fifth-harmonic injection scheme is also implemented using DSP coding with fifth-harmonic signal equal to 0.0618 p.u. The resulting waveform of leg and corresponding phase voltage (unfiltered) are shown in Figs. 15.55 and 15.56, respectively.

Triangular zero sequence injection PWM (TIPWM) is also implemented. The resulting waveform of phase voltage along with phase 'a', 'b', and 'c' currents and triangular zero-sequence injection are shown in Figs. 15.57 and 15.58, respectively.

15.4.3 Modeling and Control of a Seven-Phase VSI-Square Wave Mode

This section details the modeling and control of a seven-phase VSI. The modeling of seven-phase VSI is done for 14-step operation using space-vector approach [39]. The PWM operation

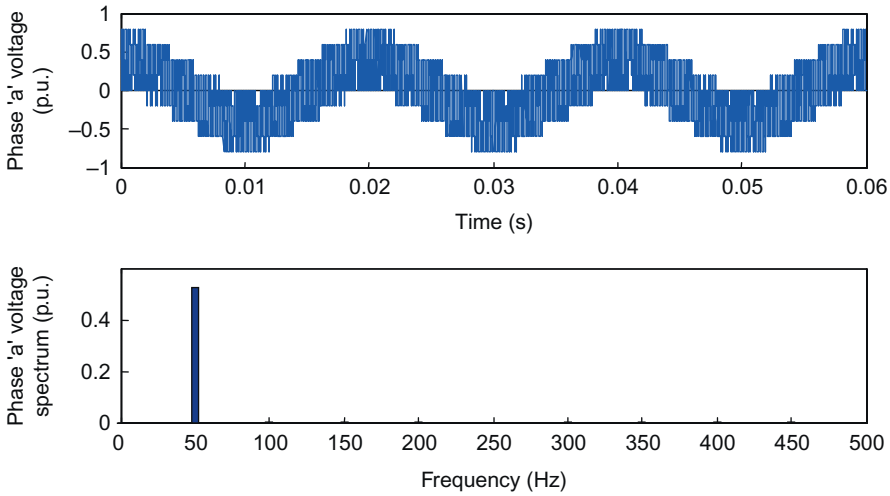


FIG. 15.52 Spectrum of phase "a" voltage for sinusoidal output of SVPWM.

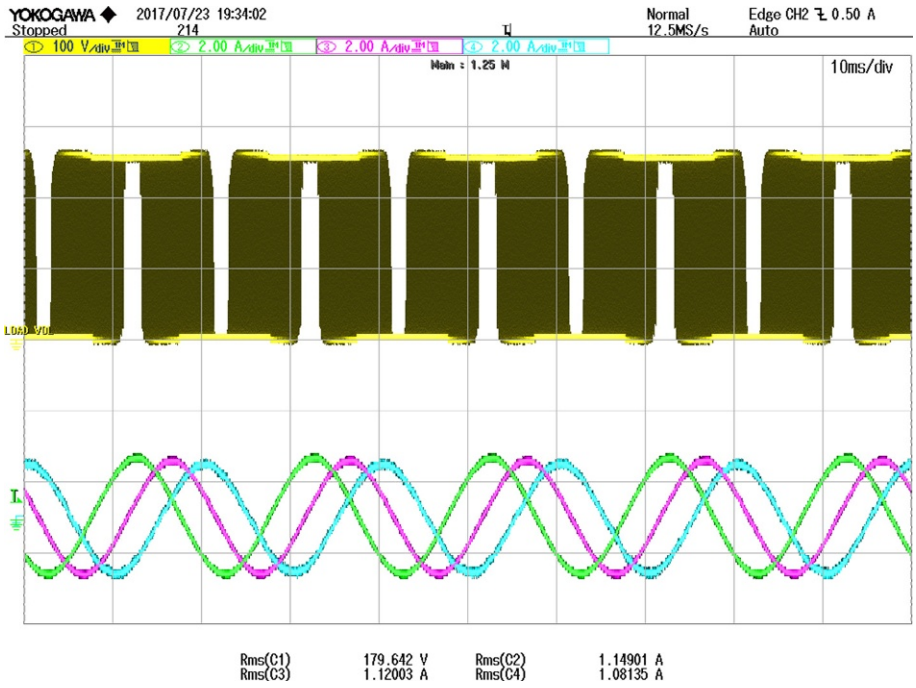


FIG. 15.53 Unfiltered leg "A" voltage along with phase 'a', 'b', and 'c' currents using carrier-based PWM.

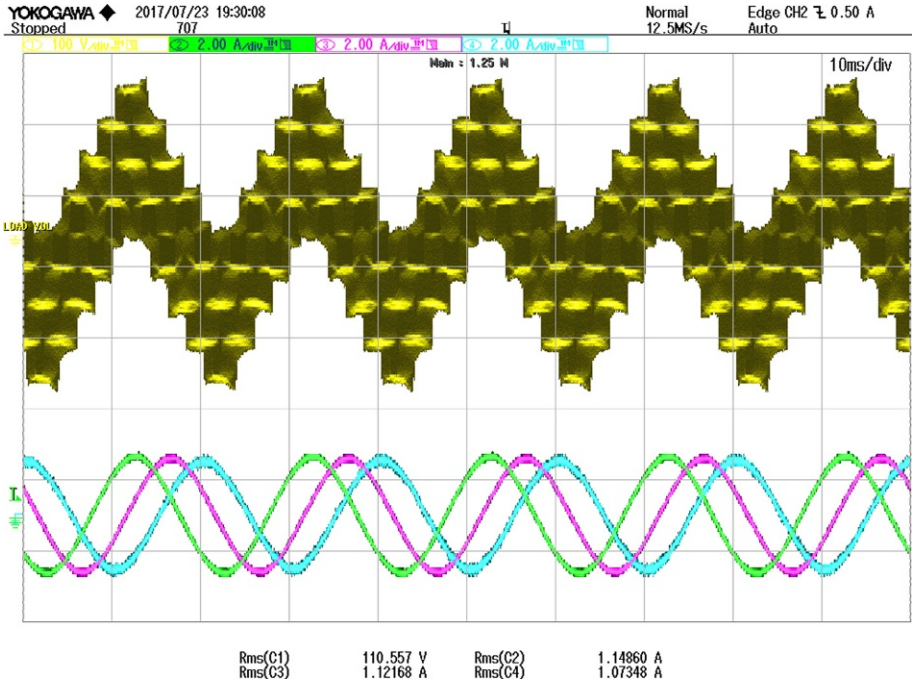


FIG. 15.54 Unfiltered phase "a" voltage along with phase 'a', 'b', and 'c' currents using carrier-based PWM.

mode is elaborated in Section 15.4.4 [40,41]. Conventional 180 degrees conduction mode is considered. The procedure adopted here follows from Section 15.4.1. The analytic expressions for harmonic components and THD are derived for phase voltages and second nonadjacent line voltages. The same is then verified using simulation and experimental results.

Section 15.4.3.2 deals with the modeling and control of a seven-phase voltage-source inverter in pulse-width modulation mode. There are a total of 128 switching state where the first 14 states lead to 14-step mode of operation and the rest of 114 switching states fall in PWM mode. Out of total 128 space vectors, two space vectors corresponding to the switching states

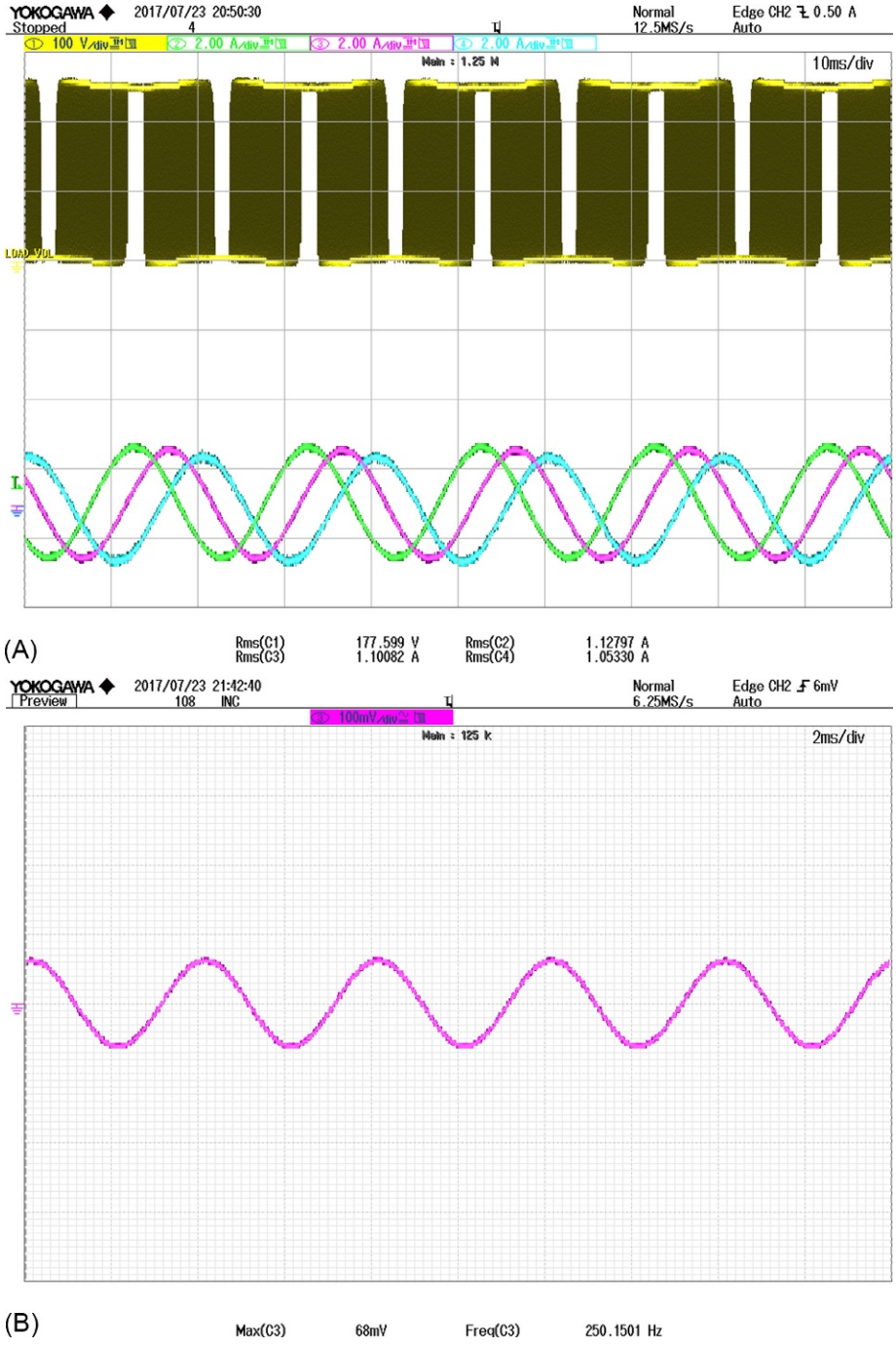


FIG. 15.55 (A) Unfiltered leg "A" voltage along with phase 'a', 'b', and 'c' currents using carrier-based PWM with fifth-harmonic injection. (B) Fifth harmonic signal injected in the carrier.

0000000 and 1111111 yield null vectors, and the rest 126 that produce finite length vectors are called active vectors. The model obtained is transformed into three different planes, namely, d-q, x_1-y_1, and x_2-y_2. Out of these three planes, only d-q produces torque in the machines supplied by the inverter, while the space vectors of other planes produce distortion in the stator currents. The complete model using space-vector approach is elaborated. The simulation results are included to validate the modeling procedure.

15.4.3.1 Fourteen-Step Operation of a Seven-Phase Voltage Source Inverter

Power circuit topology of a seven-phase VSI is shown in Fig. 15.59. Each switch in the circuit consists of two power

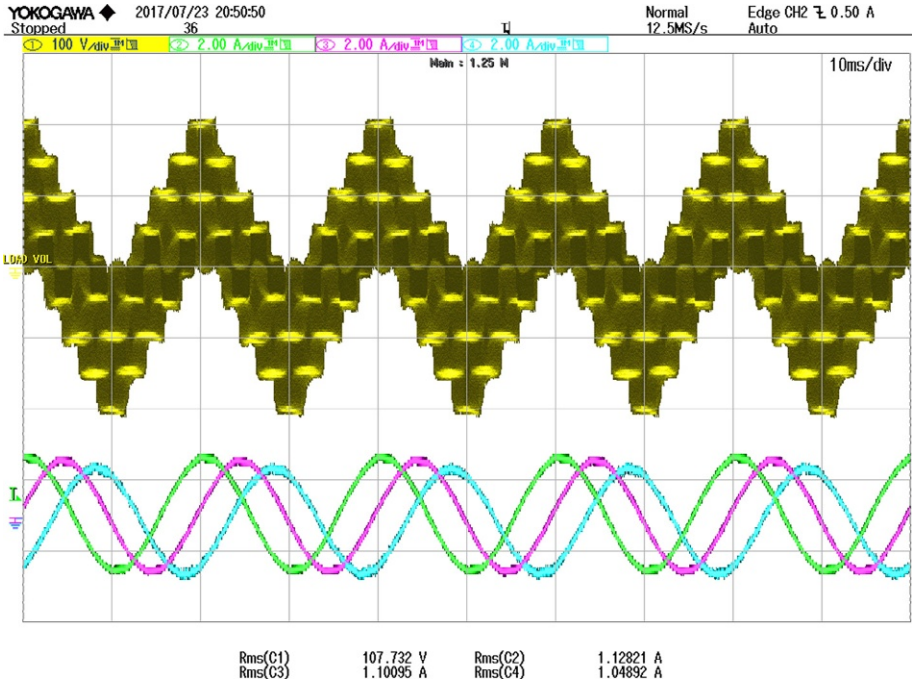


FIG. 15.56 Unfiltered phase "a" voltage along with phase 'a', 'b', and 'c' currents using fifth-harmonic signal injected in the carrier.

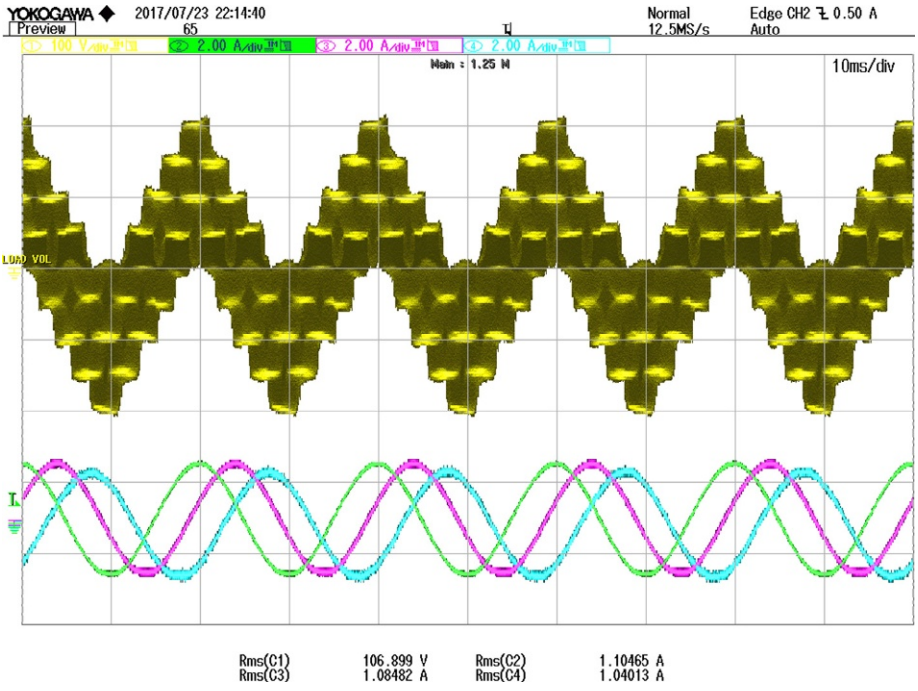


FIG. 15.57 Phase voltage along with phase 'a', 'b', and 'c' currents using triangular zero sequence injection PWM (TIPWM).

semiconductor devices, connected in antiparallel. One of these is a fully controllable semiconductor, such as a bipolar transistor or IGBT, while the second one is a diode. The input of the inverter is a DC voltage, which is regarded further on as being constant. The inverter outputs are denoted in Fig. 15.59 with lowercase symbols (*a*,*b*,*c*,*d*,*e*,*f*,*g*), while the points of connection of the outputs to inverter legs have symbols in capital letters (*A*,*B*,*C*,*D*,*E*,*F*,*G*). The basic operating principles of the seven-

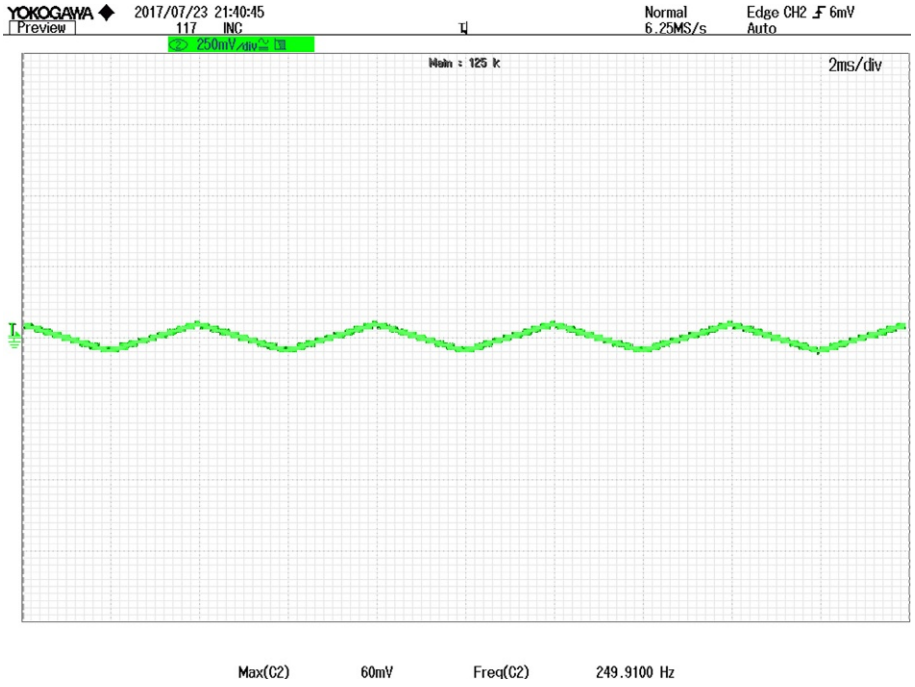


FIG. 15.58 Triangular fifth harmonic zero sequence injected signal.

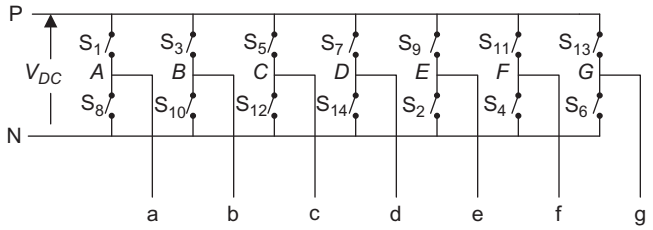


FIG. 15.59 Seven-phase voltage-source inverter power circuit.

phase VSI are developed in what follows assuming the ideal commutation and zero forward voltage drops. Each switch is assumed to conduct for 180 degrees, leading to the operation in the 14-step mode. Phase delay between firing of two switches in any subsequent two phases is equal to 360/7 degrees = 51.43 degrees (approx.).

The driving control gate/base signals for the 14 switches of the inverter in Fig. 15.59 are illustrated in Fig. 15.60. One complete cycle of operation of the inverter can be divided into 14 distinct modes indicated in Fig. 15.60 and summarized in Table 15.5. It follows from Fig. 15.60 and Table 15.5 that at any instant of time there are seven switches that are "on" and seven switches that are "off." In the 14-step mode of operation, there are three conducting switches from the upper 7 and 4 from the lower 7 or vice versa.

Leg voltages (i.e., voltages between points *A*,*B*,*C*,*D*,*E*,*F*,*G* and the negative rail of the DC bus N in Fig. 15.59) are considered first. The leg voltages obtained from the gate drive signal of Fig. 15.60.

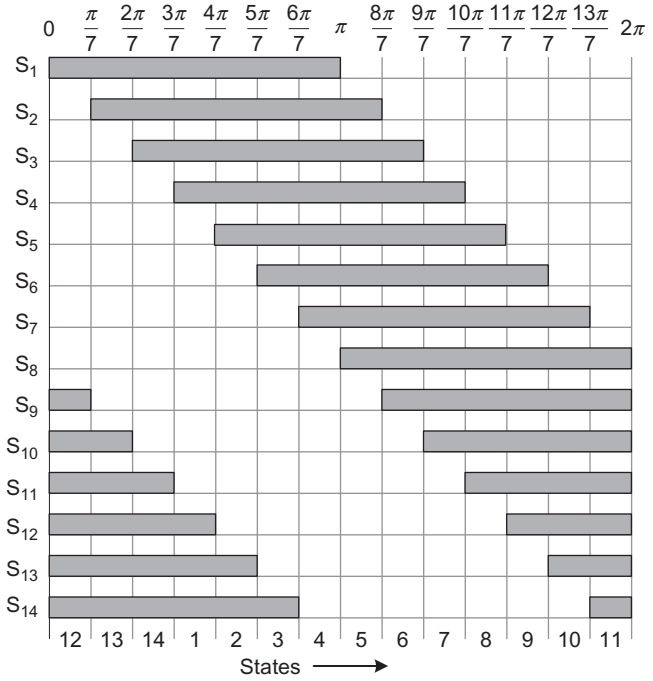


FIG. 15.60 Driving switch signals for the 14-step mode.

Space-vector model of the inverter is developed in the following subsection. Space vector of phase voltages in stationary reference frame is defined, using power invariant transformation, as

TABLE 15.5 Fourteen-step operation of a seven-phase VSI

States	Switches ON	Terminal polarity
12	1,9,10,11,12,13,14	$A^+ B^- C^- D^- E^+ F^+ G^+$
13	10,11,12,13,14,12	$A^+ B^- C^- D^- E^- F^+ G^+$
14	11,12,13,14,1,2,3	$A^+ B^+ C^- D^- E^- F^+ G^+$
1	12,13,14,1,2,3,4	$A^+ B^+ C^- D^- E^- F^- G^+$
2	13,14,1,2,3,4,5	$A^+ B^+ C^+ D^- E^- F^- G^+$
3	14,1,2,3,4,5,6	$A^+ B^+ C^+ D^- E^- F^- G^-$
4	1,2,3,4,5,6,7	$A^+ B^+ C^+ D^+ E^- F^- G^-$
5	2,3,4,5,6,7,8	$A^- B^+ C^+ D^+ E^- F^- G^-$
6	3,4,5,6,7,8,9	$A^- B^+ C^+ D^+ E^+ F^- G^-$
7	4,5,6,7,8,9,10	$A^- B^- C^+ D^+ E^+ F^- G^-$
8	5,6,7,8,9,10,11	$A^- B^- C^+ D^+ E^+ F^+ G^-$
9	6,7,8,9,10,11,12	$A^- B^- C^- D^+ E^+ F^+ G^-$
10	7,8,9,10,11,12,13	$A^- B^- C^- D^+ E^+ F^+ G^+$
11	8,9,10,11,12,13,14	$A^- B^- C^- D^- E^+ F^+ G^+$

$$\underline{v} = \frac{2}{7}\left(v_a + \underline{a}v_b + \underline{a}^2 v_c + \underline{a}^3 v_d + \underline{a}^{*3} v_e + \underline{a}^{*2} v_f + \underline{a}^* v_g\right) \quad (15.105)$$

where $\underline{a} = \exp(j2\pi/7)$, $\underline{a}^2 = \exp(j4\pi/7)$, $\underline{a}^3 = \exp(j6\pi/7)$, $\underline{a}^* = \exp(-j2\pi/5)$, $\underline{a}^{*2} = \exp(-j4\pi/5)$, $\underline{a}^{*3} = \exp(-j6\pi/7)$, and * stands for a complex conjugate.

Space vectors of leg voltages are obtained using Fig. 15.60 and Eq. (15.105) and are given as in Eq. (15.106).

$$\begin{bmatrix} \vec{v}_1 \\ \vec{v}_2 \\ - \\ - \\ \vec{v}_{14} \end{bmatrix} = \left(\frac{2}{7}\right) \frac{V_{DC}}{2\cos(3\pi/7)} \begin{bmatrix} e^{j0} \\ e^{j\pi/7} \\ - \\ - \\ e^{j13\pi/7} \end{bmatrix} \quad (15.106)$$

It is seen that the leg voltages have magnitude of $(2/7)V_{DC}(2\cos(\pi/7))$ and are 25.7142857 degrees spatially apart.

Phase-to-neutral voltages of the star-connected load are most easily found by defining a voltage difference between the star point n of the load and the negative rail of the DC bus N. The following correlation then holds true:

$$\begin{aligned} v_A &= v_a + v_{nN} \\ v_B &= v_b + v_{nN} \\ v_C &= v_c + v_{nN} \\ v_D &= v_d + v_{nN} \\ v_E &= v_e + v_{nN} \\ v_F &= v_f + v_{nN} \\ v_G &= v_g + v_{nN} \end{aligned} \quad (15.107)$$

Since the phase voltages in a star-connected load sum to zero, the summation of Eq. (15.107) yields

$$v_{nN} = (6/7)(v_A + v_B + v_C + v_D + v_E + v_F + v_G) \quad (15.108)$$

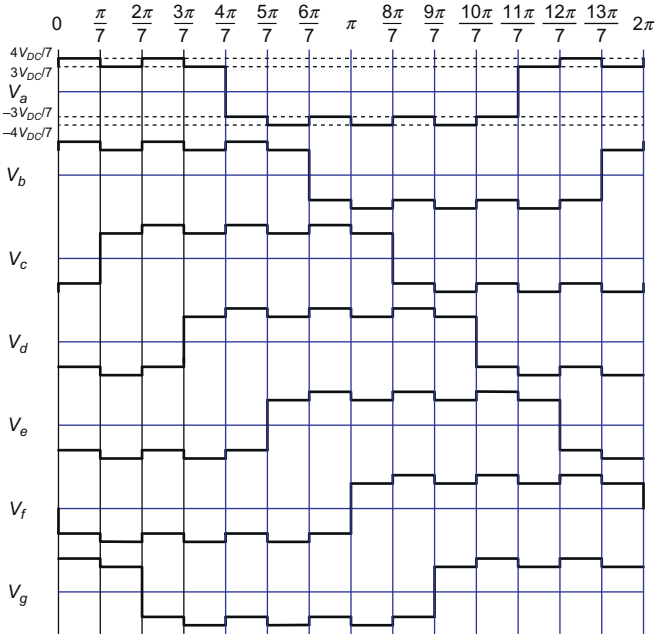


FIG. 15.61 Phase-to-neutral voltages of the seven-phase VSI in the 14-step mode of operation.

Substitution of (15.107) into (15.108) yields phase-to-neutral voltages of the load in the following form:

$$\begin{aligned} V_a &= (6/7)V_A - (1/7)(V_B + V_C + V_D + V_E + V_F + V_G) \\ V_b &= (6/7)V_B - (1/7)(V_A + V_C + V_D + V_E + V_F + V_G) \\ V_c &= (6/7)V_C - (1/7)(V_A + V_B + V_D + V_E + V_F + V_G) \\ V_d &= (6/7)V_D - (1/7)(V_A + V_B + V_C + V_E + V_F + V_G) \\ V_e &= (6/7)V_E - (1/7)(V_A + V_B + V_C + V_D + V_F + V_G) \\ V_f &= (6/7)V_F - (1/7)(V_A + V_B + V_C + V_D + V_E + V_G) \\ V_g &= (6/7)V_G - (1/7)(V_A + V_B + V_C + V_D + V_E + V_F) \end{aligned} \quad (15.109)$$

The phase voltages in different modes are obtained by substituting leg voltages into Eq. (15.109), and their space vectors are determined using Eq. (15.105). The waveform of phase voltages for seven phases is shown in Fig. 15.61. The space vectors for the first 14 states are obtained as

$$\begin{bmatrix} \vec{v}_{1phase} \\ - \\ - \\ - \\ \vec{v}_{14phase} \end{bmatrix} = \left(\frac{2}{7}\right) \frac{V_{DC}}{2\cos(3\pi/7)} \begin{bmatrix} e^{j0} \\ - \\ - \\ - \\ e^{j13\pi/7} \end{bmatrix} \quad (15.110)$$

The Fourier analysis can be carried out, recognizing the quarter-wave symmetry; the waveform may be considered as odd function. The Fourier coefficients are obtained as

$$B_{2n-1}=\sum_{n=1}^{\infty}\left(\frac{4}{7\pi}\right)\left(\frac{V_{DC}}{2n-1}\right)\left[3+\cos(2n-1)\frac{\pi}{7}+\cos(2n-1)\frac{3\pi}{7}-\cos(2n-1)\frac{2\pi}{7}\right] \tag{15.111}$$

The expression in third bracket of Eq. (15.111) equals to zero for all the harmonics whose order is divisible by seven. Hence, one can write the phase-to-neutral voltages as

$$V(t)=\left(\frac{2V_{DC}}{\pi}\right)\left(\begin{array}{c}\sin\omega t+\frac{1}{3}\sin(3\omega t)+\frac{1}{5}\sin(5\omega t)+\frac{1}{9}\sin(9\omega t)\\+\frac{1}{11}\sin(11\omega t)+\frac{1}{13}\sin(13\omega t)+\ldots\end{array}\right) \tag{15.112}$$

From (15.112), it follows that the fundamental component of the output phase-to-neutral voltages has an rms value equal to

$$V_a=\frac{\sqrt{2}}{\pi}V_{DC}=0.45V_{DC} \tag{15.113}$$

From Fig. 15.61, the mean square value is determined as

$$\text{Mean square value}=\frac{1}{\pi}V_{DC}^2\left[\left(\frac{3}{7}\right)^2+\left(\frac{4}{7}\right)^2+\left(\frac{3}{7}\right)^2+\left(\frac{4}{7}\right)^2+\left(\frac{3}{7}\right)^2+\left(\frac{4}{7}\right)^2+\left(\frac{3}{7}\right)^2\right]\times\frac{\pi}{7}=\frac{12}{49}V_{DC}^2 \tag{15.114}$$

$$V_{rms}=\sqrt{\text{Mean square value}}=\frac{2\sqrt{3}}{7}V_{DC} \tag{15.115}$$

Total harmonic rms voltage (p.u.) is given by

$$V_{Hrms}=\sqrt{(V_{rms})^2-(V_1)^2}=\sqrt{\left(\frac{2\sqrt{3}}{7}\right)^2-\left(\frac{\sqrt{2}}{\pi}\right)^2}=0.2055616499 \tag{15.116}$$

Hence, total harmonic distortion is

$$THD=\frac{\text{r.m.s. total harmonic voltage}}{\text{r.m.s. total voltage}}=\frac{0.2055616499}{2\sqrt{3}/7}=0.4153837586 \text{ or } 41.54\% \tag{15.117}$$

There are three systems of line-to-line voltage: adjacent, first nonadjacent and second nonadjacent, in contrast to a three-phase system where only one line-to-line voltage is defined and five-phase system where two systems of line voltages exist. The second nonadjacent line voltages yield highest magnitude, and hence, it is taken up for discussion, and the other two types are omitted. The values of line voltages are obtained as the difference between the leg voltages and are plotted in Fig. 15.62.

The second nonadjacent line-line voltage space vectors are calculated by substituting the values from Table 15.6 into the defining expression (15.105) and are

$$\begin{bmatrix}\vec{v}_{1lll}\\-\\-\\-\\\vec{v}_{14lll}\end{bmatrix}=\left(\frac{2}{7}\right)8V_{DC}\cos\left(\frac{2\pi}{7}\right).\cos\left(\frac{\pi}{7}\right).\cos\left(\frac{\pi}{14}\right)\begin{bmatrix}e^{j\pi/14}\\e^{j3\pi/14}\\-\\-\\-\\e^{j27\pi/14}\end{bmatrix} \tag{15.118}$$

Fourier analysis can be done, and the resulting coefficients of the Fourier series for second nonadjacent line-to-line voltages, by considering odd quarter-wave symmetry, are

$$B_{2n-1}=\frac{4V_{Dc}}{\pi(2n-1)}\left[\cos(2n-1)\frac{\pi}{14}\right] \tag{15.119}$$

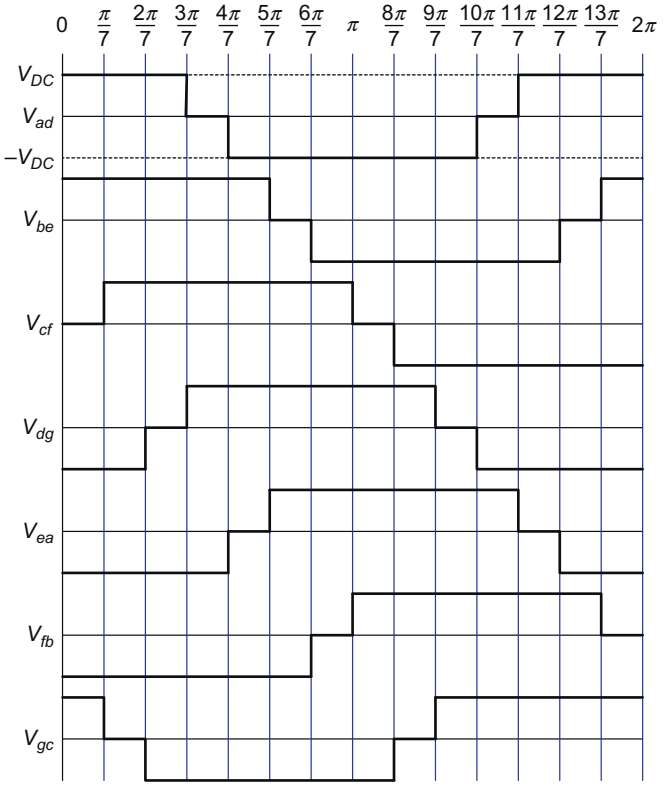


FIG. 15.62 The second nonadjacent line-to-line voltages of seven-phase VSI for various modes.

TABLE 15.6 Second nonadjacent line-to-line voltages of seven-phase VSI

States	Switches ON	Space vectors	V_{ad}	V_{be}	V_{cf}	V_{dg}	V_{ea}	V_{fb}	V_{gc}
1	12,13,14,1,2,3,4	$\vec{v}_{1III}$	V_{DC}	V_{DC}	0	$-V_{DC}$	$-V_{DC}$	$-V_{DC}$	V_{DC}
2	13,14,1,2,3,4,5	$\vec{v}_{2III}$	V_{DC}	V_{DC}	V_{DC}	$-V_{DC}$	$-V_{DC}$	$-V_{DC}$	0
3	14,1,2,3,4,5,6	$\vec{v}_{3III}$	V_{DC}	V_{DC}	V_{DC}	0	$-V_{DC}$	$-V_{DC}$	V_{DC}
4	1,2,3,4,5,6,7	$\vec{v}_{4III}$	0	V_{DC}	V_{DC}	V_{DC}	$-V_{DC}$	$-V_{DC}$	$-V_{DC}$
5	2,3,4,5,6,7,8	$\vec{v}_{5III}$	$-V_{DC}$	V_{DC}	V_{DC}	V_{DC}	0	$-V_{DC}$	$-V_{DC}$
6	3,4,5,6,7,8,9	$\vec{v}_{6III}$	$-V_{DC}$	0	V_{DC}	V_{DC}	V_{DC}	$-V_{DC}$	$-V_{DC}$
7	4,5,6,7,8,9,10	$\vec{v}_{7III}$	$-V_{DC}$	$-V_{DC}$	V_{DC}	V_{DC}	V_{DC}	0	$-V_{DC}$
8	5,6,7,8,9,10,11	$\vec{v}_{8III}$	$-V_{DC}$	$-V_{DC}$	0	V_{DC}	V_{DC}	V_{DC}	$-V_{DC}$
9	6,7,8,9,10,11,12	$\vec{v}_{9III}$	$-V_{DC}$	$-V_{DC}$	$-V_{DC}$	V_{DC}	V_{DC}	V_{DC}	0
10	7,8,9,10,11,12,13	$\vec{v}_{10III}$	$-V_{DC}$	$-V_{DC}$	$-V_{DC}$	0	V_{DC}	V_{DC}	V_{DC}
11	8,9,10,11,12,13,14	$\vec{v}_{11III}$	0	$-V_{DC}$	$-V_{DC}$	$-V_{DC}$	V_{DC}	V_{DC}	V_{DC}
12	1,9,10,11,12,13,14	$\vec{v}_{12III}$	V_{DC}	$-V_{DC}$	$-V_{DC}$	$-V_{DC}$	0	V_{DC}	V_{DC}
13	10,11,12,13,14,12	$\vec{v}_{13III}$	V_{DC}	0	$-V_{DC}$	$-V_{DC}$	$-V_{DC}$	V_{DC}	V_{DC}
14	11,12,13,14,1,2,3	$\vec{v}_{14III}$	V_{DC}	V_{DC}	$-V_{DC}$	$-V_{DC}$	$-V_{DC}$	0	V_{DC}

The series will be

$$V(t)=\sum_{n=1}^{\infty}\frac{4V_{Dc}}{\pi(2n-1)}\left[\cos(2n-1)\frac{\pi}{14}\right]\sin(2n-1)\omega t \tag{15.120}$$

From (15.120), it follows that the fundamental component of the output phase-to-neutral voltages has an rms value equal to

$$V_a=0.8777435064V_{DC} \tag{15.121}$$

From Fig. 15.62, the mean square value is determined as

$$\text{Mean square value}=\frac{1}{\pi}\left[V_{DC}^2\right]\times\frac{6\pi}{7}=\frac{6}{7}V_{DC}^2 \tag{15.122}$$

$$V_{rms}=\sqrt{\text{Mean square value}}=\frac{\sqrt{42}}{7}V_{DC} \tag{15.123}$$

Total harmonic rms voltage (p.u.) is given by

$$V_{Hrms}=\sqrt{(V_{rms})^2-(V_1)^2}=\sqrt{\left(\frac{\sqrt{42}}{7}\right)^2-(0.8777435064)^2}$$
$$=0.2944642493 \tag{15.124}$$

Hence, total harmonic distortion is

$$THD=\frac{\text{r.m.s. total harmonic voltage}}{\text{r.m.s. total voltage}}$$
$$=\frac{0.2944642493}{\sqrt{42}/7}=0.3180577408 \quad \text{or} \quad 31.81\% \tag{15.125}$$

The distortion in the line voltages is quite high.

It is important to note at this stage that the space vectors described by (15.105) provide mapping of inverter voltages into a two-dimensional space. However, since seven-phase inverter essentially requires description in a seven-dimensional space, not all the harmonics contained in (15.111) and (15.112) will be encompassed by the space vector of (15.105). In particular, space vectors calculated using (15.105) will only represent harmonics of the order $14k\pm1$, $k=0,1,2,3\ldots..$, that is, the 1st, the 13th, the 15th, and so on. Harmonics of the order $7k$, $k=1,2,3,\ldots$, cannot appear due to the isolated neutral point. However, harmonics of the order $7k\pm2$ and $7k\pm4$, $k=1,3,5,\ldots$ are present in (15.111) and (15.112) but are not encompassed by the space-vector definition of (15.105). These harmonics in essence appear in the second and third two-dimensional space, which requires introduction of the second and third space vectors for the seven-phase system. This issue is addressed in Section 15.4.3.3.

15.4.3.2 PWM Mode of Operation

If a seven-phase VSI is operated in PWM mode, apart from the already described 14 states, there will be additional 114 switching states. The number of possible switching states is in general equal to 2^n, where n is the number of inverter legs (i.e., output phases). This correlation is valid for any two-level VSI. Table 15.7 summarizes the additional switching states that are associated with PWM mode of operation and are absent in the 14-step mode of operation. Switches that are "on" and the corresponding terminal polarity are included in Table 15.7 As can be seen from Table 15.7, the remaining 114 switching states encompass four possible situations: all the states when four switches from upper (or lower) half and three from the lower (or upper) half of the inverter are "on" (states 1–14, 29–42, 43–56, 85–99, and 98–112); two states when either all the seven upper (or lower) switches are "on" (states 127 and 128); all the states when five

TABLE 15.7 Modes of operation of seven-phase voltage-source inverter

States	Switches ON	Polarity of terminal	States	Switches ON	Polarity of terminal
15	1,2,3,5,11,13,14	A+B+C+D−E−F+G+	72	1,2,3,5,7,11,13	A+B+C+D+E−F+G+
16	1,2,3,4,6,12,14	A+B+C−D−E−F−G−	73	2,3,4,6,8,12,14	A−B+C−D−E−F−G−
17	1,2,3,4,5,7,13	A+B+C+D+E−F−G+	74	1,3,4,5,7,9,13	A+B+C+D+E+F−G+
18	2,3,4,5,6,8,14	A−B+C+D−E−F−G−	75	2,4,5,6,8,10,14	A−B−C+D−E−F−G−
19	1,3,4,5,6,7,9	A+B+C+D+E+F−G−	76	1,3,5,6,7,9,11	A+B+C+D+E+F+G−
20	2,4,5,6,7,8,10	A−B−C+D+E−F−G−	77	2,4,6,7,8,10,12	A−B−C−D+E−F−G−
21	3,5,6,7,8,9,11	A−B+C+D+E+F+G−	78	3,5,7,8,9,11,13	A−B+C+D+E+F+G+
22	4,6,7,8,9,10,12	A−B−C−D+E+F−G−	79	4,6,8,9,10,12,14	A−B−C−D−E+F−G−
23	5,7,8,9,10,11,13	A−B−C+D+E+F+G+	80	1,5,7,9,10,11,13	A+B−C+D+E+F+G+
24	6,8,9,10,11,12,14	A−B−C−D−E+F+G−	81	2,6,8,10,11,12,14	A−B−C−D−E−F+G−
25	7,9,10,11,12,13	A+B−C−D+E+F+G+	82	1,3,7,9,11,12,13	A+B+C−D+E+F+G+
26	2,8,10,11,12,13,14	A−B−C−D−E−F+G+	83	2,4,8,10,12,13,14	A−B−C−D−E−F−G+
27	1,3,9,11,12,13,14	A+B+C−D−E+F+G+	84	1,3,5,9,11,13,14	A+B+C+D−E+F+G+
28	1,2,4,10,12,13,14	A+B−C−D−E−F−G+	85	2,35,8,11,13,14	A−B+C+D−E−F+G+
29	1,2,4,5,10,13,14	A+B−C+D−E−F+G+	86	1,3,4,6,9,12,14	A+B+C−D−E+F−G−
30	1,2,3,5,6,11,14	A+B+C+D−E−F+G−	87	1,2,4,5,7,10,13	A+B−C+D+E−F−G+
31	1,2,3,4,6,7,12	A+B+C−D+E−F−G−	88	2,3,5,6,8,11,14	A−B+C+D−E−F+G−
32	2,3,4,5,7,8,13	A−B+C+D+E−F−G+	89	1,3,4,6,7,9,12	A+B+C−D+E+F−G−
33	3,4,5,6,8,9,14	A−B+C+D−E+F−G−	90	2,4,5,7,8,10,13	A−B−C+D+E−F−G+
34	1,4,5,6,7,9,10	A+B−C+D+E+F−G−	91	3,5,6,8,9,11,14	A−B+C+D−E+F+G−
35	2,5,6,7,8,10,11	A−B−C+D+E−F+G−	92	1,4,6,7,9,10,12	A+B−C−D+E+F−G−
36	3,6,7,8,9,11,12	A−B+C−D+E+F+G−	93	2,5,7,8,10,11,13	A−B−C+D+E−F+G+
37	4,7,8,9,10,12,13	A−B−C−D+E+F−G+	94	3,6,8,9,11,12,14	A−B+C−D−E+F+G−
38	5,8,9,10,11,13,14	A−B−C+D−E+F+G+	95	1,4,7,9,10,12,13	A+B−C−D+E+F−G+
39	1,6,9,10,11,12,14	A+B−C−D−E+F+G−	96	2,5,8,10,11,13,14	A−B−C+D−E−F+G+
40	1,2,7,10,11,12,13	A+B−C−D+E−F+G+	97	1,3,6,9,11,12,14	A+B+C−D−E+F+G−
41	2,3,8,11,12,13,14	A−B+C−D−E−F+G+	98	1,2,4,7,10,12,13	A+B−C−D+E−F−G+
42	1,3,4,9,12,13,14	A+B+C−D−E+F−G+	99	1,2,5,6,10,11,14	A+B−C+D−E−F+G−
43	1,2,3,4,7,12,13	A+B+C−D+E−F−G+	100	1,2,3,6,7,11,12	A+B+C−D+E−F+G−
44	2,3,4,5,8,13,14	A−B+C+D−E−F−G+	101	2,3,4,7,8,12,13	A−B+C−D+E−F−G+
45	1,3,4,5,6,9,14	A+B+C+D−E+F−G−	102	3,4,5,8,9,13,14	A−B+C+D−E+F−G+
46	1,2,4,5,6,7,10	A+B−C+D+E−F−G−	103	1,4,5,6,9,10,14	A+B−C+D−E+F−G−
47	2,3,5,6,7,8,11	A−B+C+D+E−F+G−	104	1,2,5,6,7,10,11	A+B−C+D+E−F+G−
48	3,4,6,7,8,9,12	A−B+C−D+E+F−G−	105	2,3,6,7,8,11,12	A−B+C−D+E−F+G−
49	4,5,7,8,9,10,13	A−B−C+D+E+F−G+	106	3,4,7,8,9,12,13	A−B+C−D+E+F−G+
50	5,6,8,9,10,11,14	A−B−C+D−E+F+G−	107	4,5,8,9,10,13,14	A−B−C+D−E+F−G+
51	1,6,7,9,10,11,12	A+B−C−D+E+F+G−	108	1,5,6,9,10,11,14	A+B−C+D−E+F+G−
52	2,7,8,10,11,12,13	A−B−C−D+E−F+G+	109	1,2,6,7,10,11,12	A+B−C−D+E−F+G−
53	3,8,9,11,12,13,14	A−B+C−D−E+F+G+	110	2,3,7,8,11,12,13	A−B+C−D+E−F+G+
54	1,4,9,10,12,13,14	A+B−C−D−E+F−G+	111	3,4,8,9,12,13,14	A−B+C−D−E+F−G+
55	1,2,5,10,1,13,14	A+B−C+D−E−F+G+	112	1,4,5,9,10,13,14	A+B−C+D−E+F−G+
56	1,2,3,6,11,12,14	A+B+C−D−E−F+G−	113	1,3,4,7,9,12,13	A+B+C−D+E+F−G+
57	2,3,4,8,12,13,14	A−B+C−D−E−F−G+	114	2,4,5,8,10,13,14	A−B−C+D−E−F−G+
58	1,3,4,5,9,13,14	A+B+C+D−E+F−G+	115	1,3,5,6,9,11,14	A+B+C+D−E+F+G−
59	1,2,4,5,6,10,14	A+B−C+D−E−F−G−	116	1,2,4,6,7,10,12	A+B−C−D+E−F−G−
60	1,2,3,5,6,7,11	A+B+C+D+E−F+G−	117	2,3,5,7,8,11,13	A−B+C+D+E−F+G+
61	2,3,4,6,7,8,12	A−B+C−D+E−F−G−	118	3,4,6,8,9,12,14	A−B+C−D−E+F−G−
62	3,4,5,7,8,9,13	A−B+C+D+E+F−G+	119	1,4,5,7,9,10,13	A+B−C+D+E+F−G+
63	4,5,6,8,9,10,14	A−B−C+D−E+F−G−	120	2,5,6,8,10,11,14	A−B−C+D−E−F+G−
64	1,5,6,7,9,10,11	A−B−C+D+E+F+G−	121	1,3,6,7,9,11,12	A+B+C−D+E+F+G−
65	2,6,7,8,10,11,12	A−B−C−D+E−F+G+	122	2,4,7,8,10,12,13	A−B−C−D+E−F−G+
66	3,7,8,9,11,12,13	A−B+C−D+E+F+G+	123	3,5,8,9,11,13,14	A−B+C+D−E+F+G+
67	4,8,9,10,12,13,14	A−B−C−D−E+F−G+	124	1,4,6,9,10,12,14	A+B−C−D−E+F−G−
68	1,5,9,10,11,13,14	A+B−C+D−E+F+G+	125	1,2,5,7,10,11,13	A+B−C+D+E−F+G+
69	1,2,6,10,11,12,14	A+B−C−D−E−F+G−	126	2,3,6,8,11,12,14	A−B+C−D−E−F+G−
70	1,2,3,7,11,12,13	A+B+C−D+E−F+G+	127	2,4,6,8,10,12,14	A−B−C−D−E−F−G−
71	1,2,4,6,10,12,14	A+B−C−D−E−F−G−	128	1,3,5,7,9,11,13	A+B+C+D+E+F+G+

switches from upper (or lower) and two from upper (or lower) half of the inverter are "on" (states 15–28, 57–70, and 113–126); and remaining states with six switches from the upper (or lower) half and one switch from the lower (or upper) half in conduction mode (states 71–84). The phase-to-neutral voltages are described using the same approach as that of the previous sections.

The phase voltage values are listed in Table 15.8, and the corresponding space vectors for 15–126 can be obtained using Eq. (15.105) and are given by expressions (15.126)–(15.133). The complete space-vector model of phase voltage is shown in Fig. 15.63.

$$\begin{bmatrix} \vec{v}_{15phase} \\ - \\ - \\ - \\ \vec{v}_{28phase} \end{bmatrix} = 2(2/7)V_{DC}\cos\left(\frac{\pi}{7}\right)\begin{bmatrix} e^{j0} \\ - \\ - \\ - \\ e^{j13\pi/7} \end{bmatrix} \tag{15.126}$$

$$\begin{bmatrix} \vec{v}_{29phase} \\ - \\ - \\ - \\ \vec{v}_{42phase} \end{bmatrix} = \sqrt{2}(2/7)V_{DC}\begin{bmatrix} e^{j0.3052\pi/7} \\ - \\ - \\ - \\ e^{j13.3052\pi/7} \end{bmatrix} \tag{15.127}$$

$$\begin{bmatrix} \vec{v}_{43phase} \\ - \\ - \\ - \\ \vec{v}_{56phase} \end{bmatrix} = \sqrt{2}(2/7)V_{DC}\begin{bmatrix} e^{j0.6948\pi/7} \\ - \\ - \\ - \\ e^{j13.6948\pi/7} \end{bmatrix} \tag{15.128}$$

$$\begin{bmatrix} \vec{v}_{57phase} \\ - \\ - \\ - \\ \vec{v}_{70phase} \end{bmatrix} = 2(2/7)V_{DC}\cos\left(\frac{2\pi}{7}\right)\begin{bmatrix} e^{j0} \\ - \\ - \\ - \\ e^{j13\pi/7} \end{bmatrix} \tag{15.129}$$

$$\begin{bmatrix} \vec{v}_{71phase} \\ - \\ - \\ - \\ \vec{v}_{84phase} \end{bmatrix} = (2/7)V_{DC}\begin{bmatrix} e^{jo} \\ - \\ - \\ - \\ e^{j13\pi/7} \end{bmatrix} \tag{15.130}$$

$$\begin{bmatrix} \vec{v}_{85phase} \\ - \\ - \\ - \\ \vec{v}_{98phase} \end{bmatrix} = (2/7)\frac{V_{DC}}{2\cos(2\pi/7)}\begin{bmatrix} e^{j0} \\ - \\ - \\ - \\ e^{j13\pi/7} \end{bmatrix} \tag{15.131}$$

$$\begin{bmatrix} \vec{v}_{99phase} \\ - \\ - \\ - \\ \vec{v}_{112phase} \end{bmatrix} = (2/7)\frac{V_{DC}}{2\cos(\pi/7)}\begin{bmatrix} e^{j0} \\ - \\ - \\ - \\ e^{j13\pi/7} \end{bmatrix} \tag{15.132}$$

$$\begin{bmatrix} \vec{v}_{113phase} \\ - \\ - \\ - \\ \vec{v}_{126phase} \end{bmatrix} = 2(2/7)V_{DC}\cos\left(\frac{3\pi}{7}\right)\begin{bmatrix} e^{j0} \\ - \\ - \\ - \\ e^{j13\pi/7} \end{bmatrix} \tag{15.133}$$

It can be seen that the total of 128 space vectors, available in the PWM operation, fall into 10 distinct categories regarding the magnitude of the available output phase voltages. The phase voltage space vectors are summarized in Table 15.9 for all 128 switching states including 14-step operation.

15.4.3.3 Model Transformation using Decoupling Matrix

Since the system under discussion is a seven-phase one, the complete model can only be elaborated in seven-dimensional space. The first two-dimensional spaces are d-q, the second one is x_1-y_1, the third one is x_2-y_2, and the last is zero-sequence component that is absent due to the assumption of isolated neutral. On the basis of the general decoupling transformation matrix for an n-phase system, inverter voltage space vectors in the second two-dimensional subspace (x_1-y_1) and third two-dimensional subspace (x_2-y_2) are determined as

$$\begin{aligned} \underline{v}_{x1y1}^{INV} &= \frac{2}{7}\left(v_a + \underline{a}^2 v_b + \underline{a}^4 v_c + \underline{a}^6 v_d + \underline{a} v_e + \underline{a}^3 v_f + \underline{a}^5 v_g\right) \\ \underline{v}_{x2y2}^{INV} &= \frac{2}{7}\left(v_a + \underline{a}^3 v_b + \underline{a}^6 v_c + \underline{a}^2 v_d + \underline{a}^5 v_e + \underline{a} v_f + \underline{a}^4 v_g\right) \end{aligned} \tag{15.134}$$

Thus, 128 space vectors of phase-to-neutral voltage in the x_1-y_1 and x_2-y_2 planes are obtained using Eq. (15.134) and are illustrated in Figs. 15.64 and 15.65. It can be seen from Figs. 15.63–15.65 that the outermost, that is, first (black), second (pink), third (orange), fourth (green), fifth (turquoise), sixth (blue), seventh (gray 80%), eighth (violet), and ninth (red) tetradecagon space vectors of the d-q plane map into the eighth (violet), fifth (turquoise), fourth (green), third (orange), ninth (red), sixth (blue), first (black), seventh (gray 80%), and second (pink) of the tetradecagon (violet) of the x_1-y_1 plane, respectively, and seventh (gray 80%), ninth (red), fourth (green), third (orange), second (pink), sixth (blue), eighth (violet), first (black), and fifth (turquoise) of the tetradecagon (violet) of the x_2-y_2 plane, respectively. Further, it is observed from the above mapping that the phase sequence a,b,c,d,e,f,g of d-q plane corresponds to a,c,e,g, b,d,f of x_1-y_1 plane and a,d,g,c,f,b,e of x_2-y_2 plane, respectively. In the black and white version of Figs. 15.63–15.65, they can be distinguished by the vector numbers of d-q plane mapped into x_1-y_1 and x_2-y_2 planes.

It is important to note at this stage that the harmonics of the order $14k \pm 1$, $k = 0, 1,2,3\ldots$, (1, 13, 15…) map into the d-q plane (Fig. 15.63), harmonics of the order $7k \pm 2$, $k = 1,3,5\ldots$, (5, 9, 19…) map into the x_1-y_1 plane (Fig. 15.64), and

TABLE 15.8 Phase voltages (p.u.) values for PWM mode

Switching states	Switches ON	Space vectors	V_a	V_b	V_c	V_d	V_e	V_f	V_g
15	1,2,3,5,11,13,14	$\vec{v}_{15phase}$	2/7	2/7	2/7	−5/7	−5/7	2/7	2/7
16	1,2,3,4,6,12,14	$\vec{v}_{16phase}$	5/7	5/7	−2/7	−2/7	−2/7	−2/7	−2/7
17	1,2,3,4,5,7,13	$\vec{v}_{17phase}$	2/7	2/7	2/7	2/7	−5/7	−5/7	2/7
18	2,3,4,5,6,8,14	$\vec{v}_{18phase}$	−2/7	5/7	5/7	−2/7	−2/7	−2/7	−2/7
19	1,3,4,5,6,7,9	$\vec{v}_{19phase}$	2/7	2/7	2/7	2/7	2/7	−5/7	−5/7
20	2,4,5,6,7,8,10	$\vec{v}_{20phase}$	−2/7	−2/7	5/7	5/7	−2/7	−2/7	−2/7
21	3,5,6,7,8,9,11	$\vec{v}_{21phase}$	−5/7	2/7	2/7	2/7	2/7	2/7	−5/7
22	4,6,7,8,9,10,12	$\vec{v}_{22phase}$	−2/7	−2/7	−2/7	5/7	5/7	−2/7	−2/7
23	5,7,8,9,10,11,13	$\vec{v}_{23phase}$	−5/7	−5/7	2/7	2/7	2/7	2/7	2/7
24	6,8,9,10,11,12,14	$\vec{v}_{24phase}$	−2/7	−2/7	−2/7	−2/7	5/7	5/7	−2/7
25	7,9,10,11,12,13	$\vec{v}_{25phase}$	2/7	−5/7	−5/7	2/7	2/7	2/7	2/7
26	2,8,10,11,12,13,14	$\vec{v}_{26phase}$	−2/7	−2/7	−2/7	−2/7	−2/7	5/7	5/7
27	1,3,9,11,12,13,14	$\vec{v}_{27phase}$	2/7	2/7	−5/7	−5/7	2/7	2/7	2/7
28	1,2,4,10,12,13,14	$\vec{v}_{28phase}$	5/7	−2/7	−2/7	−2/7	−2/7	−2/7	5/7
29	1,2,4,5,10,13,14	$\vec{v}_{29phase}$	4/7	−3/7	4/7	−3/7	−3/7	−3/7	4/7
30	1,2,3,5,6,11,14	$\vec{v}_{30phase}$	3/7	3/7	3/7	−4/7	−4/7	3/7	−4/7
31	1,2,3,4,6,7,12	$\vec{v}_{31phase}$	4/7	4/7	−3/7	4/7	−3/7	−3/7	−3/7
32	2,3,4,5,7,8,13	$\vec{v}_{32phase}$	−4/7	3/7	3/7	3/7	−4/7	−4/7	3/7
33	3,4,5,6,8,9,14	$\vec{v}_{33phase}$	−3/7	4/7	4/7	−3/7	4/7	−3/7	−3/7
34	1,4,5,6,7,9,10	$\vec{v}_{34phase}$	3/7	−4/7	3/7	3/7	3/7	−4/7	−4/7
35	2,5,6,7,8,10,11	$\vec{v}_{35phase}$	−3/7	−3/7	4/7	4/7	−3/7	4/7	−3/7
36	3,6,7,8,9,11,12	$\vec{v}_{36phase}$	−4/7	3/7	−4/7	3/7	3/7	3/7	−4/7
37	4,7,8,9,10,12,13	$\vec{v}_{37phase}$	−3/7	−3/7	−3/7	4/7	4/7	−3/7	4/7
38	5,8,9,10,11,13,14	$\vec{v}_{38phase}$	−4/7	−4/7	3/7	−4/7	−3/7	−3/7	−3/7
39	1,6,9,10,11,12,14	$\vec{v}_{39phase}$	4/7	−3/7	−3/7	−3/7	4/7	4/7	−3/7
40	1,2,7,10,11,12,13	$\vec{v}_{40phase}$	3/7	−4/7	−4/7	3/7	−4/7	3/7	3/7
41	2,3,8,11,12,13,14	$\vec{v}_{41phase}$	−3/7	4/7	−3/7	−3/7	−3/7	4/7	4/7
42	1,3,4,9,12,13,14	$\vec{v}_{42phase}$	3/7	3/7	−4/7	−4/7	3/7	−4/7	3/7
43	1,2,3,4,7,12,13	$\vec{v}_{43phase}$	3/7	3/7	−4/7	3/7	−4/7	−4/7	3/7
44	2,3,4,5,8,13,14	$\vec{v}_{44phase}$	−3/7	4/7	4/7	−3/7	−3/7	−3/7	4/7
45	1,3,4,5,6,9,14	$\vec{v}_{45phase}$	3/7	3/7	3/7	−4/7	3/7	−4/7	−4/7
46	1,2,4,5,6,7,10	$\vec{v}_{46phase}$	4/7	−3/7	4/7	4/7	−3/7	−3/7	−3/7
47	2,3,5,6,7,8,11	$\vec{v}_{47phase}$	−4/7	3/7	3/7	3/7	−4/7	3/7	−4/7
48	3,4,6,7,8,9,12	$\vec{v}_{48phase}$	−3/7	4/7	−3/7	4/7	4/7	−3/7	−3/7
49	4,5,7,8,9,10,13	$\vec{v}_{49phase}$	−4/7	−4/7	3/7	3/7	3/7	−4/7	3/7
50	5,6,8,9,10,11,14	$\vec{v}_{50phase}$	−3/7	−3/7	4/7	−3/7	4/7	4/7	−3/7
51	1,6,7,9,10,11,12	$\vec{v}_{51phase}$	3/7	−4/7	−4/7	3/7	3/7	3/7	−4/7
52	2,7,8,10,11,12,13	$\vec{v}_{52phase}$	−3/7	−3/7	−3/7	4/7	−3/7	4/7	4/7
53	3,8,9,11,12,13,14	$\vec{v}_{53phase}$	−4/7	3/7	−4/7	−4/7	3/7	3/7	3/7
54	1,4,9,10,12,13,14	$\vec{v}_{54phase}$	4/7	−3/7	−3/7	−3/7	4/7	−3/7	4/7
55	1,2,5,10,1,13,14	$\vec{v}_{55phase}$	3/7	−4/7	3/7	−4/7	−4/7	3/7	3/7
56	1,2,3,6,11,12,14	$\vec{v}_{56phase}$	4/7	4/7	−3/7	−3/7	−3/7	4/7	−3/7
57	2,3,4,8,12,13,14	$\vec{v}_{57phase}$	−2/7	5/7	−2/7	−2/7	−2/7	−2/7	5/7
58	1,3,4,5,9,13,14	$\vec{v}_{58phase}$	2/7	2/7	2/7	−5/7	2/7	−5/7	2/7
59	1,2,4,5,6,10,14	$\vec{v}_{59phase}$	5/7	−2/7	5/7	−2/7	−2/7	−2/7	−2/7
60	1,2,3,5,6,7,11	$\vec{v}_{60phase}$	2/7	2/7	2/7	2/7	−5/7	2/7	−5/7
61	2,3,4,6,7,8,12	$\vec{v}_{61phase}$	−2/7	5/7	−2/7	5/7	−2/7	−2/7	−2/7
62	3,4,5,7,8,9,13	$\vec{v}_{62phase}$	−5/7	2/7	2/7	2/7	2/7	−5/7	2/7
63	4,5,6,8,9,10,14	$\vec{v}_{63phase}$	−2/7	−2/7	5/7	−2/7	5/7	−2/7	−2/7

Continued

TABLE 15.8 Phase voltages (p.u.) values for PWM mode—cont'd

Switching states	Switches ON	Space vectors	V_a	V_b	V_c	V_d	V_e	V_f	V_g
64	1,5,6,7,9,10,11	$\vec{v}_{64phase}$	2/7	−5/7	2/7	2/7	2/7	2/7	−5/7
65	2,6,7,8,10,11,12	$\vec{v}_{65phase}$	−2/7	−2/7	−2/7	5/7	−2/7	5/7	−2/7
66	3,7,8,9,11,12,13	$\vec{v}_{66phase}$	−5/7	2/7	−5/7	2/7	2/7	2/7	2/7
67	4,8,9,10,12,13,14	$\vec{v}_{67phase}$	−2/7	−2/7	−2/7	−2/7	5/7	−2/7	5/7
68	1,5,9,10,11,13,14	$\vec{v}_{68phase}$	2/7	−5/7	2/7	−5/7	2/7	2/7	2/7
69	1,2,6,10,11,12,14	$\vec{v}_{69phase}$	5/7	−2/7	−2/7	−2/7	−2/7	5/7	−2/7
70	1,2,3,7,11,12,13	$\vec{v}_{70phase}$	2/7	2/7	−5/7	2/7	−5/7	2/7	2/7
71	1,2,4,6,10,12,14	$\vec{v}_{71phase}$	6/7	−1/7	−1/7	−1/7	−1/7	−1/7	−1/7
72	1,2,3,5,7,11,13	$\vec{v}_{72phase}$	1/7	1/7	1/7	1/7	−6/7	1/7	1/7
73	2,3,4,6,8,12,14	$\vec{v}_{73phase}$	−1/7	6/7	−1/7	−1/7	−1/7	−1/7	−1/7
74	1,3,4,5,7,9,13	$\vec{v}_{74phase}$	1/7	1/7	1/7	1/7	1/7	−6/7	1/7
75	2,4,5,6,8,10,14	$\vec{v}_{75phase}$	−1/7	−1/7	6/7	−1/7	−1/7	−1/7	−1/7
76	1,3,5,6,7,9,11	$\vec{v}_{76phase}$	1/7	1/7	1/7	1/7	1/7	1/7	−6/7
77	2,4,6,7,8,10,12	$\vec{v}_{77phase}$	−1/7	−1/7	−1/7	6/7	−1/7	−1/7	−1/7
78	3,5,7,8,9,11,13	$\vec{v}_{78phase}$	−6/7	1/7	1/7	1/7	1/7	1/7	1/7
79	4,6,8,9,10,12,14	$\vec{v}_{79phase}$	−1/7	−1/7	−1/7	−1/7	6/7	−1/7	−1/7
80	1,5,7,9,10,11,13	$\vec{v}_{80phase}$	1/7	−6/7	1/7	1/7	1/7	1/7	1/7
81	2,6,8,10,11,12,14	$\vec{v}_{81phase}$	−1/7	−1/7	−1/7	−1/7	−1/7	6/7	−1/7
82	1,3,7,9,11,12,13	$\vec{v}_{82phase}$	1/7	1/7	−6/7	1/7	1/7	1/7	1/7
83	2,4,8,10,12,13,14	$\vec{v}_{83phase}$	−1/7	−1/7	−1/7	−1/7	−1/7	−1/7	6/7
84	1,3,5,9,11,13,14	$\vec{v}_{84phase}$	1/7	1/7	1/7	−6/7	1/7	1/7	1/7
85	2,35,8,11,13,14	$\vec{v}_{85phase}$	−4/7	3/7	3/7	−4/7	−4/7	3/7	3/7
86	1,3,4,6,9,12,14	$\vec{v}_{86phase}$	4/7	4/7	−3/7	−3/7	4/7	−3/7	−3/7
87	1,2,4,5,7,10,13	$\vec{v}_{87phase}$	3/7	−4/7	3/7	3/7	−4/7	−4/7	3/7
88	2,3,5,6,8,11,14	$\vec{v}_{88phase}$	−3/7	4/7	4/7	−3/7	−3/7	4/7	−3/7
89	1,3,4,6,7,9,12	$\vec{v}_{89phase}$	3/7	3/7	−4/7	3/7	3/7	−4/7	−4/7
90	2,4,5,7,8,10,13	$\vec{v}_{90phase}$	−3/7	−3/7	4/7	4/7	−3/7	−3/7	4/7
91	3,5,6,8,9,11,14	$\vec{v}_{91phase}$	−4/7	3/7	3/7	−4/7	3/7	3/7	−4/7
92	1,4,6,7,9,10,12	$\vec{v}_{92phase}$	4/7	−3/7	−3/7	4/7	4/7	−3/7	−3/7
93	2,5,7,8,10,11,13	$\vec{v}_{93phase}$	−4/7	−4/7	3/7	3/7	−4/7	3/7	3/7
94	3,6,8,9,11,12,14	$\vec{v}_{94phase}$	−3/7	4/7	−3/7	−3/7	4/7	4/7	−3/7
95	1,4,7,9,10,12,13	$\vec{v}_{95phase}$	3/7	−4/7	−4/7	3/7	3/7	−4/7	3/7
96	2,5,8,10,11,13,14	$\vec{v}_{96phase}$	−3/7	−3/7	4/7	−3/7	−3/7	4/7	4/7
97	1,3,6,9,11,12,14	$\vec{v}_{97phase}$	3/7	3/7	−4/7	−4/7	3/7	3/7	−4/7
98	1,2,4,7,10,12,13	$\vec{v}_{98phase}$	4/7	−3/7	−3/7	4/7	−3/7	−3/7	4/7
99	1,2,5,6,10,11,14	$\vec{v}_{99phase}$	4/7	−3/7	4/7	−3/7	−3/7	4/7	−3/7
100	1,2,3,6,7,11,12	$\vec{v}_{100phase}$	3/7	3/7	−4/7	3/7	−4/7	3/7	−4/7
101	2,3,4,7,8,12,13	$\vec{v}_{101phase}$	−3/7	4/7	−3/7	4/7	−3/7	−3/7	4/7
102	3,4,5,8,9,13,14	$\vec{v}_{102phase}$	−4/7	3/7	3/7	−4/7	3/7	−4/7	3/7
103	1,4,5,6,9,10,14	$\vec{v}_{103phase}$	4/7	−3/7	4/7	−3/7	4/7	−3/7	−3/7
104	1,2,5,6,7,10,11	$\vec{v}_{104phase}$	3/7	−4/7	3/7	3/7	−4/7	3/7	−4/7
105	2,3,6,7,8,11,12	$\vec{v}_{105phase}$	−3/7	4/7	−3/7	4/7	−3/7	4/7	−3/7
106	3,4,7,8,9,12,13	$\vec{v}_{106phase}$	−4/7	3/7	−4/7	3/7	3/7	−4/7	3/7
107	4,5,8,9,10,13,14	$\vec{v}_{107phase}$	−3/7	−3/7	4/7	−3/7	4/7	−3/7	4/7
108	1,5,6,9,10,11,14	$\vec{v}_{108phase}$	3/7	−4/7	3/7	−4/7	3/7	3/7	−4/7
109	1,2,6,7,10,11,12	$\vec{v}_{109phase}$	4/7	−3/7	−3/7	4/7	−3/7	4/7	−3/7
110	2,3,7,8,11,12,13	$\vec{v}_{110phase}$	−4/7	3/7	−4/7	3/7	−4/7	3/7	3/7
111	3,4,8,9,12,13,14	$\vec{v}_{111phase}$	−3/7	4/7	−3/7	−3/7	4/7	−3/7	4/7
112	1,4,5,9,10,13,14	$\vec{v}_{112phase}$	3/7	−4/7	3/7	−4/7	3/7	−4/7	3/7

TABLE 15.8 Phase voltages (p.u.) values for PWM mode—cont'd

Switching states	Switches ON	Space vectors	V_a	V_b	V_c	V_d	V_e	V_f	V_g
113	1,3,4,7,9,12,13	$\vec{v}_{113phase}$	2/7	2/7	−5/7	2/7	2/7	−5/7	2/7
114	2,4,5,8,10,13,14	$\vec{v}_{114phase}$	−2/7	−2/7	5/7	−2/7	−2/7	−2/7	5/7
115	1,3,5,6,9,11,14	$\vec{v}_{115phase}$	2/7	2/7	2/7	−5/7	2/7	2/7	−5/7
116	1,2,4,6,7,10,12	$\vec{v}_{116phase}$	5/7	−2/7	−2/7	5/7	−2/7	−2/7	−2/7
117	2,3,5,7,8,11,13	$\vec{v}_{117phase}$	−5/7	2/7	2/7	2/7	−5/7	2/7	2/7
118	3,4,6,8,9,12,14	$\vec{v}_{118phase}$	−2/7	5/7	−2/7	−2/7	5/7	−2/7	−2/7
119	1,4,5,7,9,10,13	$\vec{v}_{119phase}$	2/7	−5/7	2/7	2/7	2/7	−5/7	2/7
120	2,5,6,8,10,11,14	$\vec{v}_{120phase}$	−2/7	−2/7	5/7	−2/7	−2/7	5/7	−2/7
121	1,3,6,7,9,11,12	$\vec{v}_{121phase}$	2/7	2/7	−5/7	2/7	2/7	2/7	−5/7
122	2,4,7,8,10,12,13	$\vec{v}_{122phase}$	−2/7	−2/7	−2/7	5/7	−2/7	−2/7	5/7
123	3,5,8,9,11,13,14	$\vec{v}_{123phase}$	−5/7	2/7	2/7	−5/7	2/7	2/7	2/7
124	1,4,6,9,10,12,14	$\vec{v}_{124phase}$	5/7	−2/7	−2/7	−2/7	5/7	−2/7	−2/7
125	1,2,5,7,10,11,13	$\vec{v}_{125phase}$	2/7	−5/7	2/7	2/7	−5/7	2/7	2/7
126	2,3,6,8,11,12,14	$\vec{v}_{126phase}$	−2/7	5/7	−2/7	−2/7	−2/7	5/7	−2/7

TABLE 15.9 Phase-to-neutral voltage space vectors for states 1–128

	Set number in planes			
Space vectors	d-q	x_1-y_1	x_2-y_2	Value of the space vectors in d-q plane
$\underline{v}_{1phase}$ to $\underline{v}_{14phase}$	1	8	7	$(2/7)V_{DC}/(2\cos(3\pi/7))\exp(jk\pi/7)$ for $k=0,1,2,\ldots,13$
$\underline{v}_{15phase}$ to $\underline{v}_{28phase}$	2	5	9	$2(2/7)V_{DC}\cos(\pi/7)\exp(jk\pi/7)$ for $k=0,1,2,\ldots,13$
$\underline{v}_{29phase}$ to $\underline{v}_{42phase}$	3	3	4	$\sqrt{2}(2/7)V_{DC}\exp(j0.3052k\pi/7)$ for $k=0,1,2,\ldots,13$
$\underline{v}_{43phase}$ to $\underline{v}_{56phase}$	4	4	3	$\sqrt{2}(2/7)V_{DC}\exp(j0.6948k\pi/7)$ for $k=0,1,2,\ldots,13$
$\underline{v}_{57phase}$ to $\underline{v}_{70phase}$	5	9	2	$2(2/7)V_{DC}\cos(2\pi/7)\exp(jk\pi/7)$ for $k=0,1,2,\ldots,13$
$\underline{v}_{71phase}$ to $\underline{v}_{84phase}$	6	6	6	$(2/7)V_{DC}\exp(jk\pi/7)$ for $k=0,1,2,\ldots,13$
$\underline{v}_{85phase}$ to $\underline{v}_{98phase}$	7	1	8	$(2/7\,V_{DC})/(2\cos(2\pi/7))\exp(jk\pi/7)$ for $k=0,1,2,\ldots,13$
$\underline{v}_{99phase}$ to $\underline{v}_{112phase}$	8	7	1	$(2/7\,V_{DC})/(2\cos(\pi/7))\exp(jk\pi/7)$ for $k=0,1,2,\ldots,13$
$\underline{v}_{113phase}$ to $\underline{v}_{126phase}$	9	2	5	$2(2/7)V_{DC}\cos(3\pi/7)\exp(jk\pi/7)$ for $k=0,1,2,\ldots,13$
$\underline{v}_{127phase}$ to $\underline{v}_{128phase}$	–	–	–	0

harmonics of the order $7k\pm4$, $k=1,3,5\ldots$, (3, 11, 17…) are encompassed by x_2-y_2 plane (Fig. 15.65) space vectors.

The second nonadjacent line voltages are elaborated next. The same procedure as that of 14-step mode is adopted to determine the line voltage space vectors for states 15–126 and are given by the expressions (15.135)–(15.142):

$$\begin{bmatrix}\vec{v}_{15lll}\\-\\-\\-\\\vec{v}_{28lll}\end{bmatrix}=\left(\frac{2}{7}\right)4V_{DC}\cos\left(\frac{\pi}{7}\right).\cos\left(\frac{\pi}{14}\right)\begin{bmatrix}e^{j\pi/14}\\e^{j5\pi/14}\\-\\-\\e^{j27\pi/14}\end{bmatrix}\quad(15.135)$$

$$\begin{bmatrix}\vec{v}_{29lll}\\-\\-\\-\\\vec{v}_{42lll}\end{bmatrix}=\left(\frac{2}{7}\right)2.7575V_{DC}\begin{bmatrix}e^{j0.8052\pi/7}\\-\\-\\-\\e^{j13.8052\pi/7}\end{bmatrix}\quad(15.136)$$

$$\begin{bmatrix}\vec{v}_{43lll}\\-\\-\\-\\\vec{v}_{56lll}\end{bmatrix}=\left(\frac{2}{7}\right)2.7575V_{DC}\begin{bmatrix}e^{j1.1948\pi/7}\\-\\-\\e^{j13.1948\pi/7}\\e^{j0.1948\pi/7}\end{bmatrix}\quad(15.137)$$

$$\begin{bmatrix}\vec{v}_{57lll}\\-\\-\\-\\\vec{v}_{70lll}\end{bmatrix}=\left(\frac{2}{7}\right)4V_{DC}\cos\left(\frac{2\pi}{7}\right).\cos\left(\frac{\pi}{14}\right)\begin{bmatrix}e^{j\pi/14}\\e^{j5\pi/14}\\-\\-\\e^{j27\pi/14}\end{bmatrix}\quad(15.138)$$

$$\begin{bmatrix}\vec{v}_{71lll}\\-\\-\\-\\\vec{v}_{84lll}\end{bmatrix}=\left(\frac{2}{7}\right)2V_{DC}\cos\left(\frac{\pi}{14}\right)\begin{bmatrix}e^{j\pi/14}\\e^{j5\pi/14}\\-\\-\\e^{j27\pi/14}\end{bmatrix}\quad(15.139)$$

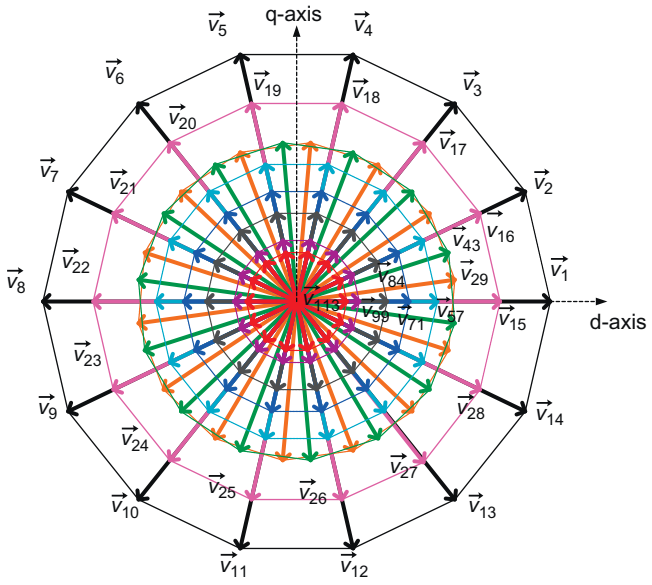


FIG. 15.63 Phase-to-neutral voltage space vectors for states 1–128 (states 127–128 are at origin) in d-q plane.

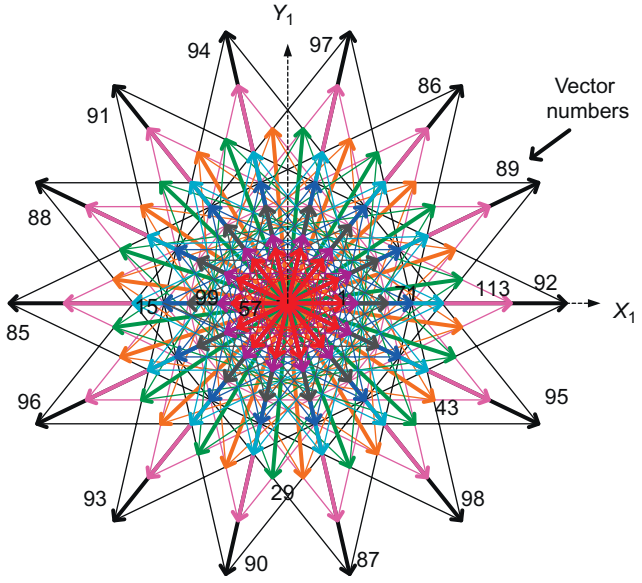


FIG. 15.64 Phase-to-neutral voltage space vectors for states 1–128 (states 127–128 are at origin) in x_1-y_1 plane.

$$\begin{bmatrix} \vec{v}_{85lll} \\ - \\ - \\ - \\ \vec{v}_{98lll} \end{bmatrix} = \left(\frac{2}{7}\right) 2V_{DC} \cos\left(\frac{3\pi}{14}\right) \begin{bmatrix} e^{j\pi/14} \\ e^{j5\pi/14} \\ - \\ - \\ e^{j27\pi/14} \end{bmatrix} \tag{15.140}$$

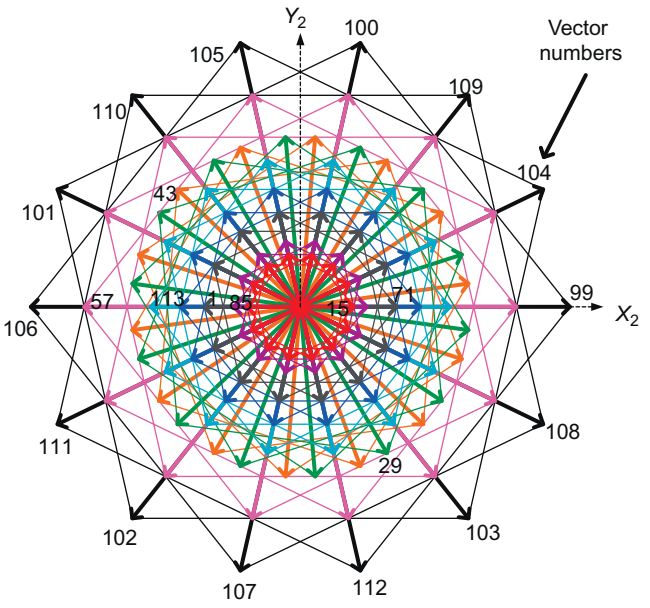


FIG. 15.65 Phase-to-neutral voltage space vectors for states 1–128 (states 127–128 are at origin) in x_2-y_2 plane.

$$\begin{bmatrix} \vec{v}_{99lll} \\ - \\ - \\ - \\ \vec{v}_{112lll} \end{bmatrix} = \left(\frac{2}{7}\right) 4V_{DC} \cos\left(\frac{2\pi}{7}\right) . \cos\left(\frac{5\pi}{14}\right) \begin{bmatrix} e^{j\pi/14} \\ e^{j5\pi/14} \\ - \\ - \\ e^{j27\pi/14} \end{bmatrix} \tag{15.141}$$

$$\begin{bmatrix} \vec{v}_{113lll} \\ - \\ - \\ - \\ \vec{v}_{126lll} \end{bmatrix} = \left(\frac{2}{7}\right) 2V_{DC} \cos\frac{5\pi}{14} \begin{bmatrix} e^{j\pi/14} \\ e^{j5\pi/14} \\ - \\ - \\ e^{j27\pi/14} \end{bmatrix} \tag{15.142}$$

15.4.4 Space Vector PWM Techniques for a Seven-Phase Voltage Source Inverter

This section is devoted to the development of space-vector PWM for a seven-phase voltage-source inverter. The aim of this section is to describe a set of continuous SVPWM in linear modulation range. Four different schemes are defined with the aim to reduce or eliminate the low-order harmonics in the output phase voltages. The outer large length space vectors are used to implement the SVPWM method at first followed by using four and then six active space vectors. Two methods are devised with four active vectors, eliminating certain set of low-order harmonics in each method. The six active vector applications yield sinusoidal output voltages, and the other two methods produce low-order harmonics. The analysis is done in terms of quality of output voltages and the range of applicability of each space-vector PWM methods.

Simulation results are provided to support the analytic and theoretical findings. It is demonstrated in Section 15.4.3 that there are a total of 14 distinct sectors with 25.714286 degrees ($\pi/7$ radians) spacing. The innermost space vectors in d-q plane are redundant and are therefore omitted from further discussion. This is in full compliance with observation where it is stated that only subset with maximum length vectors has to be used for any given combination of the switches that are "on" and "off" (3–4 and 4–3 in this case). The middle region space vectors correspond to two switches being "on" from upper (lower) set and five switches being "off" from lower (upper) set or vice versa and one switch being "on" from upper (lower) set and six switches being "off" from lower (upper) set or vice versa. It follows that, there are nine, 14sided regular polygons are formed by the vectors. The "*set number*" of vectors forming these polygons is already defined in Table 15.9.

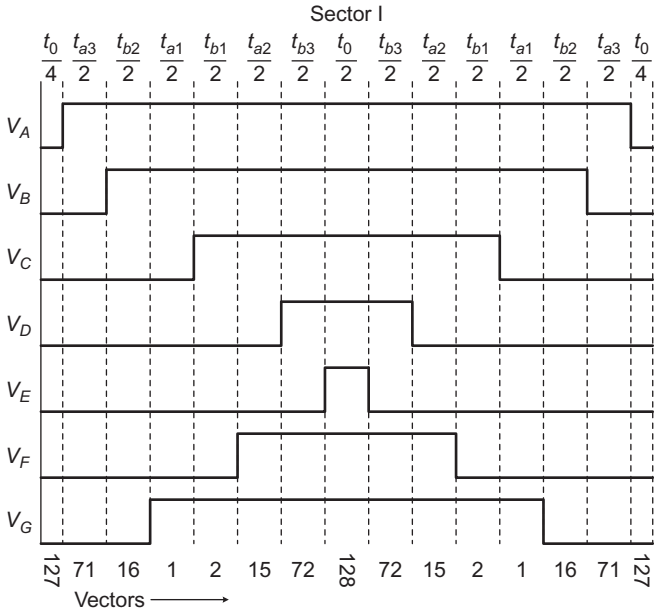


FIG. 15.66 Switching pattern and space-vector disposition for one cycle of operation.

15.4.4.1 Space Vector Pulse Width Modulation (SVPWM) With Sinusoidal Output

This section develops SVPWM schemes for a seven-phase VSI. At first, the conventional method of using only set-1 vectors is taken up followed by set-1 plus set-2 and set-1 plus set-2 plus set-6 vectors (SVPWM with sinusoidal output) schemes.

The methods discussed in the preceding sections generate low-order harmonic since they utilize either two or four active vectors in one switching period. As emphasized in [40], the number of applied active space vectors for multiphase VSI with an odd phase number should be equal to $(n-1)$, n is the number of phases of inverter, for sinusoidal output. This means that one needs to apply six active vectors in each switching period, rather than two or four for obtaining sinusoidal output. Moreover, the dwell time of each vector should be chosen in such a way as to eliminate vectors of both x_1-y_1 and x_2-y_2 planes. Thus, six active vectors (in sector 1, active vectors no. 1, 2, 15, 16, 71, and 72 are used) and one zero vector are chosen to implement the SVPWM. The chosen vectors belong to the first, second, and sixth sets.

The switching pattern and the sequence of the space vectors for this scheme are illustrated in Fig. 15.66. It is observed from the switching pattern of Fig. 15.66 that the switching in all the phases is staggered, that is, all switches change state at different instants of time. The total number of switching in each switching period is still 28, thus preserving the requirement that each switch changes state only twice in a switching period. The selection of space vectors for other sectors is listed in Table 15.10.

The vector disposition of sector I is shown in Fig. 15.67 in all the three planes.

TABLE 15.10 Sector-wise switching sequence when the first, second, and sixth set of vectors are applied

Sector number	Sequence of vectors in operation														
I	127	71	16	1	2	15	72	128	72	15	2	1	16	71	127
II	127	73	16	3	2	17	72	128	72	17	2	3	16	73	127
III	127	73	18	3	4	17	74	128	74	17	4	3	18	73	127
IV	127	75	18	5	4	19	74	128	74	19	4	5	18	75	127
V	127	75	20	5	6	19	76	128	76	19	6	5	20	75	127
VI	127	77	20	7	6	21	76	128	76	21	6	7	20	77	127
VII	127	77	22	7	8	21	78	128	78	21	8	7	22	77	127
VIII	127	79	22	9	8	23	78	128	78	23	8	9	22	79	127
IX	127	79	24	9	10	23	80	128	80	23	10	9	24	79	127
X	127	81	24	11	10	25	80	128	80	25	10	11	24	81	127
XI	127	81	26	11	12	25	82	128	82	25	12	11	26	81	127
XII	127	83	26	13	12	27	82	128	82	27	12	13	26	83	127
XIII	127	83	28	13	14	27	84	128	84	27	14	13	28	83	127
XIV	127	71	28	1	14	15	84	128	84	15	14	1	28	71	127

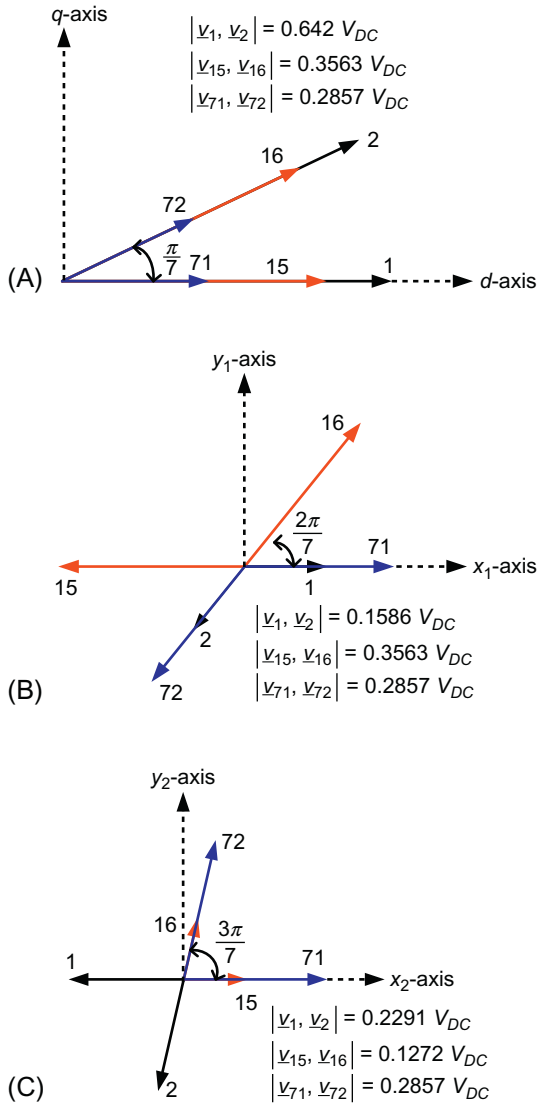


FIG. 15.67 Space-vector disposition in sector I: (A) d-q plane, (B) x_1-y_1 plane, and (C) x_2-y_2 plane.

Using equal volt-second criterion, for sector I, the following is obtained:

$$\begin{aligned} v_{d-q} &= 0.642\delta_1 + 0.5148\delta_{15} + 0.2857\delta_{71} \\ v_{x1-y1} &= 0.1586\delta_1 - 0.3563\delta_{15} + 0.2857\delta_{71} \\ v_{x2-y2} &= -0.2291\delta_1 + 0.1272\delta_{15} + 0.2857\delta_{71} \end{aligned} \tag{15.143}$$

Or the above equations can be represented as

$$\begin{bmatrix} \underline{v}_d \\ \underline{v}_{x1} \\ \underline{v}_{x2} \end{bmatrix} = [K] * \begin{bmatrix} \delta_1 \\ \delta_{15} \\ \delta_{71} \end{bmatrix}$$
$$\begin{bmatrix} \underline{v}_q \\ \underline{v}_{y1} \\ \underline{v}_{y2} \end{bmatrix} = [K] * \begin{bmatrix} \delta_2 \\ \delta_{16} \\ \delta_{72} \end{bmatrix}$$

where

$$[K] = \begin{bmatrix} 0.642 & 0.5148 & 0.2857 \\ 0.15686 & -0.3563 & 0.2857 \\ -0.2291 & 0.1272 & 0.2857 \end{bmatrix}$$

and δ_1, δ_{15}, δ_{71}, δ_2, δ_{16}, and δ_{72} are duty cycles of vector numbers 1, 15, 71, 2, 16, and 72, respectively; their coefficiants are the respective magnitudes of the vectors and negative sign showing the opposite to normal direction.

Since [K] is nonsingular matrix, its inverse is existing (det $[K] = -0.1634$). Therefore, expressions for duty cycles can be written as

$$\begin{bmatrix} \delta_1 \\ \delta_{15} \\ \delta_{71} \end{bmatrix} = [K]^{-1} * \begin{bmatrix} \underline{v}_d \\ \underline{v}_{x1} \\ \underline{v}_{x2} \end{bmatrix}$$
$$\begin{bmatrix} \delta_2 \\ \delta_{16} \\ \delta_{72} \end{bmatrix} = [K]^{-1} * \begin{bmatrix} \underline{v}_q \\ \underline{v}_{y1} \\ \underline{v}_{y2} \end{bmatrix} \tag{15.144}$$

where $[K]^{-1} = \begin{bmatrix} 0.8455 & 0.6792 & -1.5248 \\ 0.6792 & -1.5248 & 0.8455 \\ 0.3754 & 1.2209 & 1.9002 \end{bmatrix}$

Solving for δ_1, δ_{15}, δ_{71}, δ_2, δ_{16}, and δ_{72} by assuming $\underline{v}_{x1} = \underline{v}_{x2} = \underline{v}_{y1} = \underline{v}_{y2} = 0$, from (15.144), one gets

$$\begin{bmatrix} \delta_1 \\ \delta_{15} \\ \delta_{71} \end{bmatrix} = \underline{v}_d * \begin{bmatrix} 0.8455 \\ 0.6792 \\ 0.3754 \end{bmatrix}$$
$$\begin{bmatrix} \delta_2 \\ \delta_{16} \\ \delta_{72} \end{bmatrix} = \underline{v}_q * \begin{bmatrix} 0.8455 \\ 0.6792 \\ 0.3754 \end{bmatrix} \tag{15.145}$$

Expression for duty cycle of zero is given as

$$\delta_0 = 1 - (\delta_1 + \delta_{15} + \delta_{71} + \delta_2 + \delta_{16} + \delta_{72}) \tag{15.146}$$

Since $\delta_0 \geq 0$, therefore,

$$(\delta_1 + \delta_{15} + \delta_{71} + \delta_2 + \delta_{16} + \delta_{72}) \leq 1 \tag{15.147}$$

Subtituting the values of duty cycles from (15.145) in (15.147), one gets

$$\underline{v}_d + \underline{v}_q = 0.526288$$

Hence,

$$\left|v_s^*\right|_{\max} = \left|\underline{v}_d + \underline{v}_q\right| \cos\left(\frac{\pi}{14}\right) = 0.513 \tag{15.148}$$

where δ_1, δ_{15}, and δ_{71} are duty cycles and suffixes denote the vector numbers; their coefficiants are their respective

magnitudes and negative sign showing their directions that are opposite to normal direction. Solving Eq. (15.143) for δ_1, δ_{15}, and δ_{71} by assuming $v_{d-q} = 0.513$ p.u. (maxium achievable output voltage) and v_{x1-y1} and v_{x2-y2} equal to zero, one gets $\delta_1 = 0.43338$, $\delta_{15} = 0.3484$, and $\delta_{71} = 0.1926$. Same duty-cycles can be applied for vector numbers 2, 16, and 72, respectively.

The time of application of zero space vectors is now given as $t_0 = t_s - t_{a1} - t_{a2} - t_{a3} - t_{b1} - t_{b2} - t_{b3}$ where t_{a1}, t_{a2}, and t_{a3} are timings of vector number 1, 15, and 71, respectively, and t_{b1}, t_{b2}, and t_{b3} are timings of vector number 2, 16, and 72, respectively.

Once again, the same procedure as that of previous section can be adopted to determine the range of applicibility of proposed method. It is seen that the maximum available output voltage with this SVPWM method is $0.513 V_{dc}$. The simulation is done to obtain the maximum acheivable output value (0.513 p.u. peak), with the commanded input equal to 0.6259 p.u., thus ensuring the equality of the fundamental output magnitude and the reference magnitude. The other simulation conditions are identical to those in application of large medium vectors. The filtered phase voltages are shown in Fig. 15.68 along with the harmonic spectrum for maximum achievable fundamental voltage shown in Fig. 15.69.

It is seen from Fig. 15.69 that the spectrum contains fundamental (0.363551 p.u. rms or 0.514 p.u. peak, 50 Hz) component and harmonic only at multiple of switching frequency and low-order harmonics are completely eliminated. The ouptut is sinusoidal because of the fact that the proportion of time of application of the chosen space vectors is such that it cancels all the undesirable x_1-y_1 and x_2-y_2 components (as can be seen from Fig. 15.67). It is to be noted here that for lower values of the input reference phase voltage, the output phase voltages preserve the shape, while there will be a correponding reduction in amplitude.

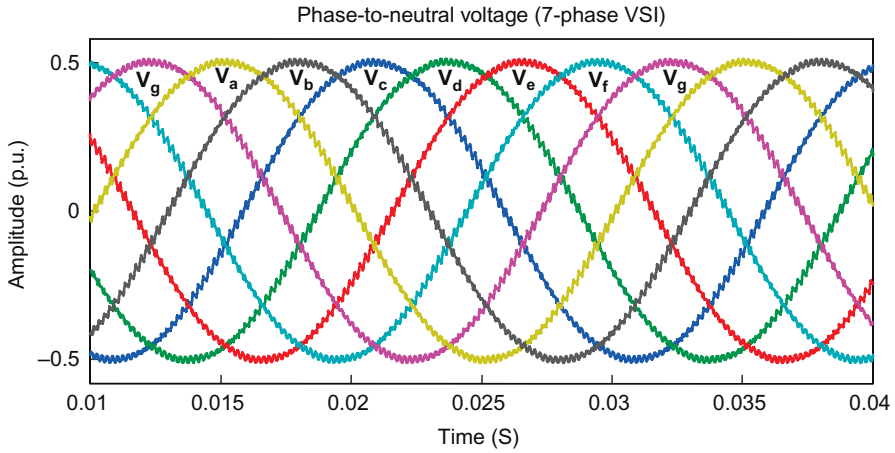


FIG. 15.68 Output filtered phase voltage of VSI for the maximum achievable output fundamental voltage (82.14% of the one obtainable with set-1 vectors only).

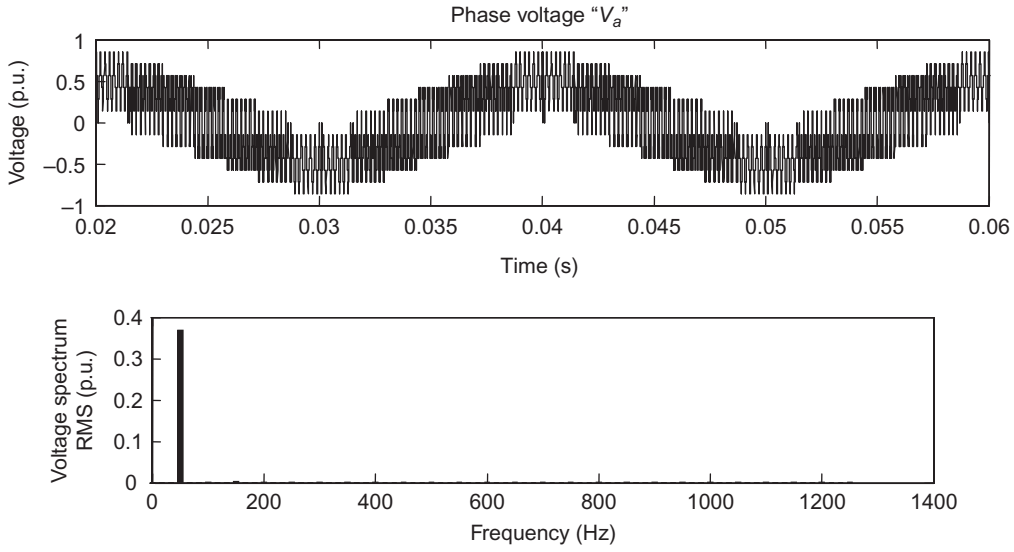


FIG. 15.69 Time-domain and frequency-domain phase "a" voltage waveform for maximum output 0.513 p.u.

15.4.4.2 Summary

Section 15.4.1 develops a space-vector model of a five-phase voltage-source inverter, and it is shown that two sets of space vectors exist, namely, *d-q* and *x-y*. The second set of space vectors termed here as *x-y* space is essentially third harmonic of the space vector in *d-q* plane. Altogether, there exist 32 space vectors out of which 30 are active and 2 are zero vectors. Complete mapping of the space vectors are provided in Section 15.4.1. Step operation of the inverter is elaborated in terms of different conduction mode, that is, 180 degrees is taken up as conduction angle. Fourier analysis is presented in terms of analytic expressions, and simulation results are provided to support the analytic expressions.

Carrier-based PWM and space-vector PWM schemes for a five-phase VSI are analyzed and compared using analytic, simulation and experimental approach. Relationship between modulation signal (fundamental and zero-sequence signal) and space vector is established, which indicates a transformation between arbitrary carrier-based PWM and space-vector modulation. A direct relationship is formulated between line-to-line voltage and space vector. It is found that the line-to-line voltage is determined by only active vectors and is independent of zero vectors. Relationship between modulation signals and space-vector sectors is identified. Analytic expressions of distribution of zero-vector application times for sinusoidal, fifth-harmonic injection, and triangular zero-sequence injection are determined. Equivalence between switching pattern of space-vector PWM and carrier type is highlighted. Performance of modulator in terms of THD of output phase voltages is determined for triangular and saw-tooth carrier signals, and the poor performance of saw-tooth carrier is indicated.

Four different space-vector PWM schemes for a seven-phase voltage-source inverter are described. At first, the conventional technique of using the largest set of space vectors is extended to a seven-phase inverter. This technique provides maximum DC bus utilization (0.6259), but the output phase voltages are distorted with significant amount of low-order harmonics especially third and fifth. These harmonics are due to free flow of x_1-y_1 and x_2-y_2 plane vectors. The second proposed method cancels the x_1-y_1 plane space vectors, and thus, the low-order harmonic more than three is eliminated in the output phase voltage waveform. Third method is investigated that eliminates vectors of x_2-y_2 plane. The modulation index is the same for the second and third methods with the elimination of different set of harmonics. The DC bus utilization is intermediate. The last method cancels all the space vectors x_1-y_1 and x_2-y_2 planes, thus providing a sinusoidal output voltage with least DC bus utilization. The experimental setup and the results are also provided.

15.5 Multiphase AC-AC Converter

15.5.1 Introduction

AC-AC converter refers to a topology of converters in which the amplitude, frequency, and phase of the AC supply can be altered according to the requirement of the load without employing reactive DC link in between. As discussed in Chapter 14, polyphase AC-AC converters can be classified as naturally commutated cycloconverters (NCC) and forced commutated cycloconverters (FCC). FCCs when implemented for low- and medium-power drives by employing high switching semiconductor bidirectional switches result in what is commonly known as *matrix converter* (MC). This section deals with the multiphase matrix converters (with phase numbers more than three) and the theory that pertains to it. It is observed that as number of phases increase, the number of vectors to be dealt with in space-vector modulation-based techniques is quite large. For an $m \times n$ MC, the *useful* number of states is m^n [4]. Thus, for a 3×7 MC, 2187 vectors are to be handled. Other way is to resort to classical methods in which output target voltages are defined and friendly harmonics are added to the target phase voltages such that the sinusoidal nature of line voltages are not altered. These target voltages are then fabricated from the input side voltages such that the average in one time sample follows the target voltage sample.

Multiphase matrix converters (MPMC) (Fig. 15.70) can be broadly classified into direct multiphase matrix converters (DMMC) and indirect multiphase matrix converters (IMMC). Although the maximum output voltage achievable is the same for both, the advantage with the indirect multiphase matrix converters is that the established modulation strategies employed for controlled rectifiers and inverters are readily applicable. In this section, the target is to present the theory on DMMC. The bidirectional switches that are employed for the multiphase matrix converters are the same as employed for conventional 3×3 matrix converter. Although the work on MPMCs is still in research domain and a statement of encouragement can be given to young researchers, possible applications of MPMCs can be wind energy systems (WES) employing multiphase generator sets, or multiphase motors can be interfaced with the existing three-phase grid using MPMCs.

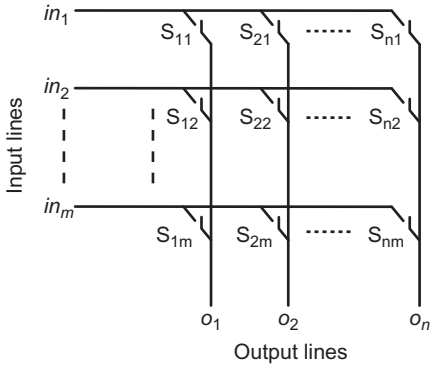


FIG. 15.70 DMMC with m input lines and n input lines.

15.5.2 Brief Review

A time line of research in the field of MPMC is shown in Fig. 15.71. The first theory addressing MPMC for odd number of input and output phases was given way back in 1989 [42]. The theory was recently extended to all configurations in [12]. This paper also extends the Venturini method to $3 \times n$ case, where n can be even or odd. Further, it also presents a simplified modulation strategy for MPMC for any number of phases. The first work on the modulation strategy of MPMC was reported in [18]. In this work, the authors use a continuous carrier and the predetermined duty ratio signals to directly generate the gating signals. This explains the origin of the name, that is, the "direct-duty-ratio-based PWM." A duty ratio is calculated for each switch, and since this applies to each output phase independently, it can be used to supply multiphase loads. The input number of phases is restricted to three since the modulation requires identification of the values of the input voltages as the maximum, medium, and minimum. Another approach applied on 3×9 MC is shown by the same authors in [16], named as carrier-based PWM scheme. Venturini method is also explored for 3×5 MC in [11,43]. Space-vector approach is the most explored approach and is discussed for various configurations in [17,44–47]. Multiphase open-end loads can also be supplied through dual MPMCs and are practically assessed in [48,49]. A 3×5 MC is discussed in [50], in which a least number of commutations are employed in one time sample. This leads to the reduction in common-mode voltage. IMMC has recently received commendable attention in [51,52]. The former paper gives carrier-based approach for a 3×5 MC that can also be realized employing space-vector approach. The later one discussed space-vector-based approach for a 3×5 MC in the overmodulation range and achieves a VTR of 0.923, which otherwise is 0.7886.

15.5.3 Defining the Voltage Transfer Ratio

All modulation strategies whether scalar or space-vector-based require the understanding of maximum achievable output voltage, that is, the maximum voltage transfer ratio (VTR_{max}) and its implementation. In scalar methods, the output reference voltages are maneuvered by the addition of friendly harmonics in order to achieve VTR_{max}. For this, a detailed understanding of how to manipulate the sinusoids is required. Thus, in this section, the theory of VTR_{max} that is achievable in an MPMC is discussed, and expressions for all the possible cases are derived. The approach will be general for any number of input and output phases until and unless specified. Illustrations are mainly done for 3×5 MC.

15.5.3.1 The Unutilized Region

Consider initially, an $m \times 1$ converter. The m-phase input voltage set is defined as

$$\begin{aligned} \underline{v}_{in}(t) &= [v_{in_1}(t), v_{in_2}(t), \ldots, v_{in_m}(t)] \\ &= V_{in}\left\{ \cos\left(\omega_{in} t + (i-1)\frac{2\pi}{m}\right)\right\}_{i=1}^{m} \end{aligned} \tag{15.149}$$

Let the duty cycles for which the output is connected to the inputs through switches S_1, S_2,…,S_m be

$$[M(t)] = [M_1(t), M_2(t), \ldots, M_m(t)] \tag{15.150}$$

The actual output voltage (w.r.t. input neutral) is obtained as

$$v_o(t) = [M(t)] \cdot \underline{v}_{in}^{T}(t) \tag{15.151}$$

The duty cycle of each switch is such calculated that in one time sample, the average of the actual output voltages follows the reference voltage. Thus, for all arbitrary output frequencies, the VTR for a three-input system can have a maximum reach up to 0.5. Generalizing this for multiple input phases, the VTR_{max} is given as

$$V_o \leq \cos\left(\frac{\pi}{m}\right) \tag{15.152}$$

This leaves a region of $1 - \cos(\pi/m)$ unutilized. This region decreases with the increase in the number of input lines. The utilized and unutilized regions are shown for three-phase input case in Fig. 15.72.

For five-phase input set, according to (15.151), approximately 19.1% of the input voltage space still remains unutilized.

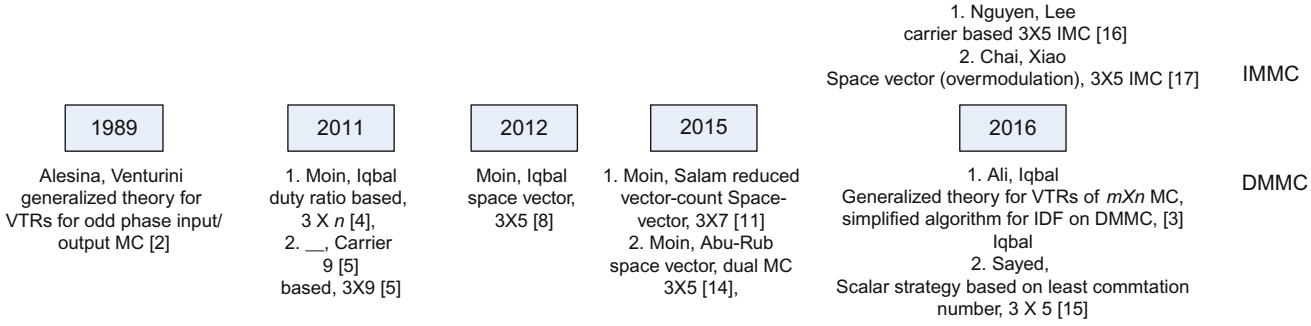


FIG. 15.71 Year-wise development of MPMC.

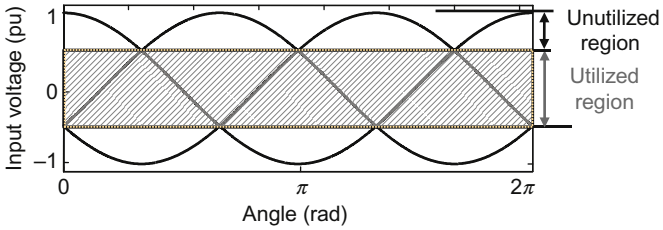


FIG. 15.72 Region (shaded) in three-phase input MC where output-voltage references are defined.

Now, consider an MPMC whose n output reference voltage set with respect to input neutral is expressed as

$$\begin{aligned}\underline{v}_o(t) &= [v_{o_1}(t), v_{o_2}(t), \ldots, v_{o_m}(t)] \\ &= V_o \left\{ \cos\left(\omega_o t + (j-1)\frac{2\pi}{n}\right) \right\}_{j=1}^{n} \end{aligned} \tag{15.153}$$

where V_o is limited by (15.152). A periodic function is such added to (15.152) that the amplitude of the output reference phase voltages and thus the line voltages increases, line voltages retain their sinusoidal nature, and the phase difference between voltages do not change. Let this function be $f_h(t)$. As this function is common to all the reference output voltages given in (15.5.5), the new output-voltage vector is expressed as

$$\begin{aligned}\underline{v}_o(t) &= [v_{o_1}(t), v_{o_2}(t), \ldots, v_{o_n}(t)] \\ &= \left\{ V_o \cos\left(\omega_o t + (j-1)\frac{2\pi}{n}\right) + f_h(t) \right\}_{j=1}^{n} \end{aligned} \tag{15.154}$$

Maximum utilizable region

After acknowledging the fact that there is space in which the output phase voltages can expand, it is desirable to know maximum output-voltage level attainable. Before addressing the issue, terms pertaining to the discussion ahead are described. These terms are exhibited in Fig. 15.73 as upper and lower bounds of input voltage set and upper and lower bounds of output-voltage set (v_{iu}, v_{il}, v_{ou}, and v_{ol}, respectively). It is seen in Fig. 15.73 that at every instant of time

$$v_{il}(t) \le v_{ol}(t) \le v_{ou}(t) \le v_{iu}(t) \tag{15.155}$$

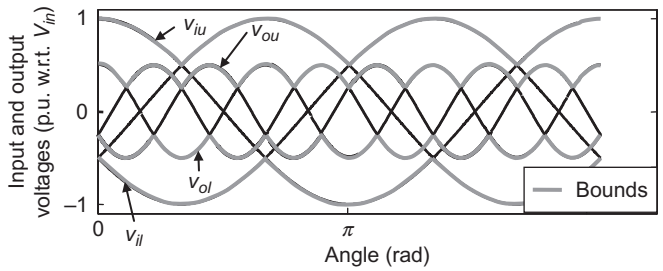


FIG. 15.73 Bounds of input and output voltages ($f_o = 3f_{in}$).

Thus, the input voltage set creates an envelope in which the output target voltage has to remain. Also, as $f_h(t)$ is a common term, the difference between $v_{ou}(t)$ and $v_{ol}(t)$ does not contain $f_h(t)$. The maximum output voltage is attained when the minima of input voltage range coincide with the maxima of output-voltage range. If the maxima of the output-voltage range are more than the minima of the input voltage range, the condition of over modulation occurs. This condition is mathematically expressed as

$$\min_{0 \le \omega_{in} t \le 2\pi} \{v_{iu}(t) - v_{il}(t)\} = \max_{0 \le \omega_o t \le 2\pi} \{v_{ou}(t) - v_{ol}(t)\} \tag{15.156}$$

Next step is to find out how the waves are optimized. The conditions differ for odd and even number of phases. The analysis of both waves is shown one by one subsequently. The analysis given below is done on a set of phases, *ignoring the input/output terminology*.

The region of 0 to 2π for x odd phases is divided into $2x$ sectors. Six sectors of three-phase set are shown in Fig. 15.74. The difference of the upper limit and lower limit generates the same wave in each sector exhibited by $v_u(t) - v_l(t)$ with the same min$\{v_u(t) - v_l(t)\}$ and max$\{v_u(t) - v_l(t)\}$ values. According to the sequence of phases in (15.153), the voltage that defines $v_u(t)$ is the first phase and $v_l(t)$ is defined by the $\left(\frac{x+1}{2}\right)^{\text{th}}$ phase:

$$\begin{aligned} v_1 - v_{\frac{x+1}{2}} &= V\left\{ \cos\omega t - \cos\left(\omega t + \left(\frac{x+1}{2} - 1\right)\frac{2\pi}{x}\right) \right\} \\ &= V\left\{ \cos\omega t - \cos\left(\omega t + \frac{(x-1)\pi}{x}\right) \right\} \end{aligned} \tag{15.157}$$

Now, the minimum value occurs at $\omega t = 0$; thus,

$$\min\left\{ v_1 - v_{\frac{x+1}{2}} \right\} = V\left\{ 1 - \cos\left(\frac{(x-1)\pi}{x}\right) \right\} \tag{15.158}$$

And as x is odd, $x-1$ is even, thus, $\cos\left(\frac{(x-1)\pi}{x}\right) = -\cos\frac{\pi}{x}$, and so,

$$\min\left\{ v_1 - v_{\frac{x+1}{2}} \right\} = V\left\{ 1 + \cos\left(\frac{\pi}{x}\right) \right\} = \min_{0 \le \omega t \le 2\pi} \{v_u(t) - v_l(t)\} \tag{15.159}$$

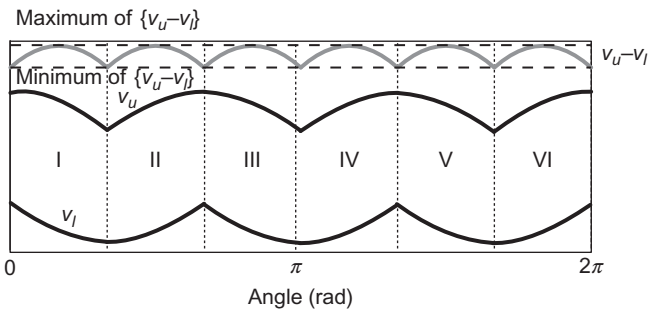


FIG. 15.74 Sectors for odd number of phases (three-phase set).

Now, the $\max\{v_u(t)-v_l(t)\}$ occurs at $\pi/2x$. Thus,

$$\max\left\{v_1 - v_{\frac{x+1}{2}}\right\} = 2V\cos\left(\frac{\pi}{2x}\right) = \max_{0\le\omega t\le 2\pi}\{v_u(t)-v_l(t)\} \tag{15.160}$$

Now, particularization of (15.158) and (15.159) in terms of m inputs and n outputs and substitution in (15.155) results in $\text{VTR}_{\max}$ as

$$\frac{V_o}{V_{in}} = \frac{1+\cos(\pi/m)}{2\cos(\pi/2n)} \tag{15.161}$$

Now, if the analysis is done for even-phase set in similar fashion as above, x-phase set is furcated into x sectors, and this is exhibited for six-phase set in Fig. 15.75. In the first sector, $v_u(t)$ is defined by the first phase, and $v_l(t)$ is defined by $v_{\frac{x+2}{2}}$. This leads to

$$v_1 - v_{\frac{x+2}{2}} = 2V\cos(\omega t) \tag{15.162}$$

The $\max\{v_u(t)-v_l(t)\}$ in this case in the first sector occurs at $\omega t = 2\pi/x$ and the $\min\{v_u(t)-v_l(t)\}$ is at $\omega t = \pi/x$. Thus,

$$\max\left\{v_1 - v_{\frac{x+2}{2}}\right\} = 2V = \max_{0\le\omega t\le 2\pi}\{v_u(t)-v_l(t)\} \tag{15.163}$$

and

$$\min\left\{v_1 - v_{\frac{x+2}{2}}\right\} = 2V\cos\pi/x = \min_{0\le\omega t\le 2\pi}\{v_u(t)-v_l(t)\} \tag{15.164}$$

Thus, if the analysis is extended to MC having both even input and output sets, then substituting (15.162) and (15.163) in (15.155) will result in

$$\frac{V_o}{V_{in}} = \cos\frac{\pi}{m} \tag{15.165}$$

MC having odd input phase set and even output phase set, substituting (15.158) and (15.162) in (15.155) results in

$$\frac{V_o}{V_{in}} = \frac{1}{2}\cdot\left(1+\cos\frac{\pi}{m}\right) \tag{15.166}$$

For a 3×6 converter, $V_o = 0.75V_{in}$.

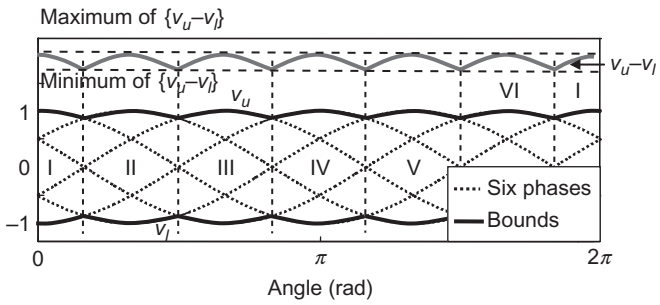


FIG. 15.75 Sectors for even number of phases (six-phase set).

Lastly, if MC has even input phase set and odd output phase set, then employing (15.159) and (15.163) in (15.155), $\text{VTR}_{\max}$ is expressed as

$$\frac{V_o}{V_{in}} = \frac{\cos(\pi/m)}{\cos(\pi/2n)} \tag{15.167}$$

For a 6×3 converter $V_o = V_{in}$. Hence, unity VTR is achievable in a six-phase input and three-phase output MC. The $\text{VTR}_{\max}$ for various configurations of MCs are shown in Table 15.11.

15.5.3.2 Target Output Voltages

After analyzing the maximum output voltage achievable, it is necessary for one to derive the derivation of the expression for $f_h(t)$ described in (15.153). This function depends on input and output frequencies. Analyzing Fig. 15.75, it is easy to realize that *odd phase can only be manipulated*. This is because the occurrence of the $\min\{v_{ul}\}$ and the $\max\{v_{ul}\}$ is at different time instances. This aspect is beneficial in defining a periodic function such that the $\min\{v_{ul}\}$ is pulled up and the $\max\{v_{ul}\}$ is pulled down, as exhibited for three-phase set in Fig. 15.76. On the contrary, the even-phase set is unalterable as the occurrence of the above stated condition occurs at the same time instant and, thus, cannot be pulled up or down employing a periodic function and hence extra region cannot be generated. Considering these facts, first of all, synthesis is done for $f_h(t)$ for the case when both input and output phase set is odd and for illustration 3×5 MC is considered. As both the voltage sets are to be optimized, the harmonic voltage, $f_h(t)$, contains a term that depends on input frequency and the other that depends

TABLE 15.11 Maximum voltage transfer ratios for various configurations of MPMC

Outputs→	3	4	5	6	7	8	9
Inputs↓							
3	0.866	0.750	0.788	0.750	0.769	0.750	0.762
4	0.816	0.707	0.743	0.707	0.750	0.707	0.718
5	1.044	0.904	0.951	0.905	0.928	0.904	0.918
6	1.000	0.866	0.911	0.866	0.888	0.866	0.879
7	1.098	0.950	0.999	0.950	0.975	0.950	0.965
8	1.067	0.924	0.971	0.924	0.948	0.924	0.938
9	1.120	0.970	1.020	0.970	0.995	0.970	0.985

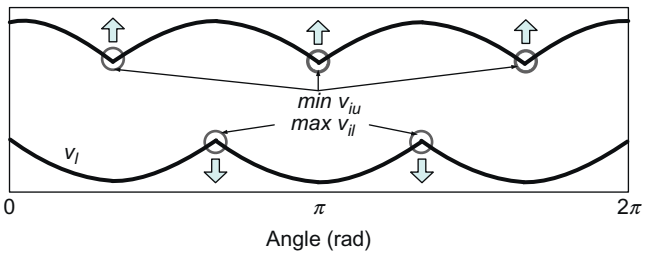


FIG. 15.76 Illustration of $\min\{v_{iu}\}$ and $\max\{v_{iu}\}$for odd number of phases (three-phase set).

on output frequency. Hence, $f_h(t)$ is written as $f_h(t) = f_{h_{in}}(t) + f_{h_o}(t)$, where $f_{h_{in}}(t)$ and $f_{h_o}(t)$ are optimizing functions for input and output voltages, respectively.

15.5.3.3 Input Voltage Optimization

As stated, $\min\{v_{iu}\}$ and $\max\{v_{il}\}$ are at different time instances, as shown for the three-phase set in Fig. 15.76. Therefore, the difference between upper and lower limit is not symmetrical, and thus, optimization is needed so that symmetrical output waveforms are developed. Clamping up of $\max\{v_{il}\}$ and clamping down of $\max\{v_{il}\}$ are done and are exhibited in Fig. 15.77. This is done by superimposing a periodic function whose frequency is m times the input frequency. Now, the amplitude of this harmonic is equal to the offset by which the *points* (*encircled in* Fig. 15.76) *are displaced*. Offset for three-phase set is 0.25 p.u., as it is the maximum to which the input voltage *points* must displace. For m input phases, the offset is

$$\text{offset} = 0.5\left(1 - \cos\left(\frac{\pi}{m}\right)\right) \tag{15.168}$$

This leads to the following expression for $f_{h_{in}}(t)$:

$$f_{h_{in}}(t) = 0.5\left(1 - \cos\left(\frac{\pi}{m}\right)\right) \cdot \cos\left(m \cdot \omega_{in} t\right) \tag{15.169}$$

For three-phase input, $f_{h_{in}}(t) = 0.25\cos(3\omega_{in}t)$. When this function is added to the input voltages, changes occur as illustrated in Fig. 15.77.

It is seen that after *subtracting* $f_{h_{in}}(t)$ from the input voltages, the output voltage with $0.75V_{in}$ is accommodated instead of $0.5V_{in}$. For m-phase input set, the condition of the peak is derived as

$$V_o = (1 - \text{offset})V_{in} \tag{15.170}$$

As the input-voltage set is unalterable, the modification is done to output-voltage set by the *addition* of $f_{h_{in}}(t)$ to the reference output-voltage equations of (15.152). So, new odd output reference voltage set, with the consideration of odd input phase set is given as

$$\underline{v}_o(t) = \left\{ V_o \cos\left(\omega_o t + (j-1)\frac{2\pi}{n}\right) + 0.5\left(1 - \cos\left(\frac{\pi}{m}\right)\right) \cdot V_{in} \cdot \cos\left(m \cdot \omega_{in} t\right) \right\}_{j=1}^{n} \tag{15.171}$$

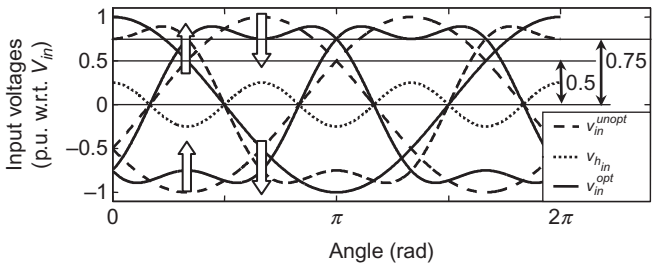


FIG. 15.77 Optimization of three-phase input voltage set.

where, V_o is given by (15.169). For 3×7 MC, (15.170) is written as

$$\underline{v}_o(t) = \left\{ V_o \cos\left(\omega_o t + (j-1)\frac{2\pi}{7}\right) + 0.25 \cdot V_{in} \cdot \cos\left(3 \cdot \omega_{in} t\right) \right\}_{j=1}^{7}$$

and $V_o = 0.75\ V_{in}$. Phase-1 voltage (v_{o1}) of the above equation is illustrated in Fig. 15.78A. It is found that v_{o1} is going beyond input voltage envelope. Thus, further optimization is needed in this case that is achieved by defining $f_{h_o}(t)$.

Output voltage optimization

A periodic function is such defined that $\min\{v_{ou}\}$ is lifted upward and $\max\{v_{ol}\}$ is dragged downward. Obviously, the frequency of this function is n times the output frequency, where f_o is the frequency of the reference output-voltage set. For five-phase output set, this must be $5f_o$. Let this function be defined as

$$f_{h_o}(t) = a \cdot \cos n\omega_o t \tag{15.172}$$

In order to calculate the amplitude of the function, consider the output voltage (v_{o1}) with the addition of (15.171) that is written as

$$u(\omega_o t) = V_o \cos\omega_o t + a \cdot \cos n\omega_o t = 0 \tag{15.173}$$

The value of the offset a is chosen such that a minimum value of $\max\{u(\omega_o t)\}$ is achieved. Also, the coefficient a is negative to clamp down $\max\{v_{ou}\}$. To find the magnitude of a, a condition that $\max\{u(\omega_o t)\}$ is located where $\cos(n\omega_o t) = 0$ is imposed. This is done as follows:

$$\frac{d}{d\omega_o t}u(\omega_o t) = -V_o \sin(\omega_o t) - a \cdot \sin(n\omega_o t) = 0 \tag{15.174}$$

Now, taking $\cos(n\omega_o t) = 0$, $\omega_o t = \pi/2n$, it is found that

$$a = -\frac{1}{n}\sin\left(\frac{\pi}{2n}\right)V_o \tag{15.175}$$

For five-phase output, $a = -0.0618V_o$. Substituting this value in (15.171),

$$f_{h_o} = -\frac{1}{n}\sin\left(\frac{\pi}{2n}\right)V_o \cos n\omega_o t \tag{15.176}$$

Now, $\max\{u(\omega_o t)\}$ occurs when $\omega_o t = \pi/2n$; therefore,

$$\max\{u(\omega_o t)\} = V_o \cos\frac{\pi}{2n} \tag{15.177}$$

This value is $0.951V_o$ for five-phase output. Fig. 15.78B exhibits the optimization of five-phase output waves. It is seen, as derived in (15.173), the maximum of the new wave occurs at $\omega_o t = \pi/10$. As the optimization of input and output phase sets is done one by one, that is, while considering the

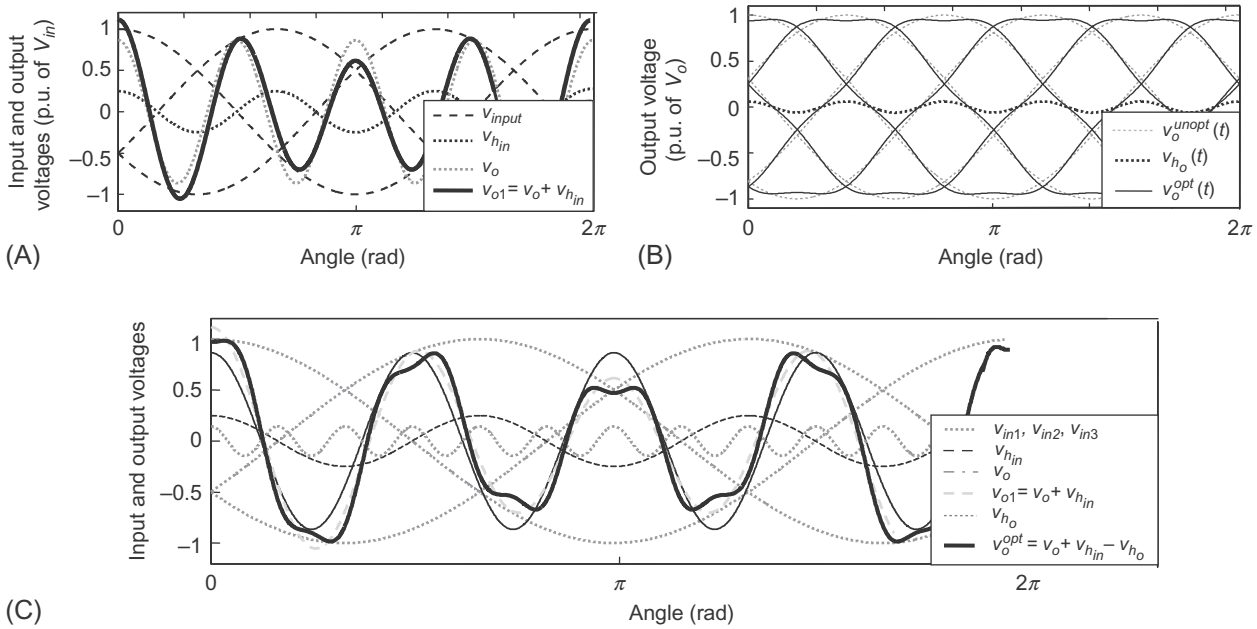


FIG. 15.78 (A) Optimization of input voltages extended to v_{o1} of five-phase set ($f_o = 4f_{in}$), (B) optimization of output voltages (five-phase set) at 50 Hz, and (C) final optimized phase voltage (v_{o1}) of a five-phase set, $f_o = 4f_{in}$.

output waves, it is considered that the input waves are unoptimized. That is why the output waves shown in Fig. 15.78B are shown with respect to V_o. Therefore, by considering input-voltage set as unoptimized and output-voltage set optimized, the condition for peak values by applying (15.176) on (15.155) is stated as

$$V_o \cos\left(\frac{\pi}{2n}\right) = 0.5 V_{in} \tag{15.178}$$

For five-phase output $V_o = 0.526 V_{in}$.

Now, considering input-voltage set and output-voltage set optimization, the peak value, by combining (15.155), (15.168), and (15.176), is expressed as

$$V_o \cos\frac{\pi}{2n} \le \left\{0.5\left(1 + \cos\left(\frac{\pi}{m}\right)\right)\right\} V_{in} \tag{15.179}$$

$$\Rightarrow V_{o_{\max}} = \frac{0.5\left(1 + \cos\left(\frac{\pi}{m}\right)\right)}{\cos\left(\frac{\pi}{2n}\right)} V_{in} \tag{15.180}$$

The $\text{VTR}_{\max}$ achievable for 3×5 MC from (15.179) is 0.78859, which is in accordance with values shown in Table 15.11.

The optimized output-voltage set is finally given by combining (15.153), (15.167), (15.168), and (15.175) as

$$\underline{v}_o(t) = \left\{ \begin{array}{l} V_o \cos\left(\omega_o t + (j-1)\frac{2\pi}{n}\right) \\ +0.5\left(1 - \cos\frac{\pi}{m}\right) \cdot V_{in} \cdot \cos\left(m \cdot \omega_{in} t\right) \ldots \\ \ldots - \frac{1}{n} \sin\left(\frac{\pi}{2n}\right) V_o \cos n\omega_o t \end{array} \right\}_{j=1}^{n} \tag{15.181}$$

where V_o is given by (15.79). Fig. 15.78C exhibits the implementation of (15.180) for 3×5 converter for output phase 1 with respect to input neutral (v_o^{opt}). All the phases of five-phase voltage set are shown in Fig. 15.79.

15.5.3.4 Other Cases

This section deals with the remaining cases of MPMCs. As discussed in previous sections, the even-phase set cannot be optimized as its $\min\{v_{iu}\}$ and $\max\{v_{il}\}$ occur at the same time, and hence, a periodic function that pushes both the points at the same instant is not feasible to obtain. Considering the configurations one by one, we have the following:

Odd-phase input and even-phase output MC

For this type of configuration of MC, only input-voltage set can be optimized, and thus, the even-phase output reference voltages are expressed as

$$\underline{v}_o(t) = \left\{ V_o \cos\left(\omega_o t + (j-1)\frac{2\pi}{n}\right) + 0.5\left(1 - \cos\left(\frac{\pi}{m}\right)\right) \cdot V_{in} \cdot \cos\left(m \cdot \omega_{in} t\right) \right\}_{j=1}^{n} \tag{15.182}$$

where $V_o = (\text{VTR}_{\max}) V_{in}$ is according to (15.169). Taking 3×6 converter for illustration, the reference output voltages of (15.181) for 3×6 MC is written as

$$\underline{v}_o(t) = \left\{ V_o \cos\left(\omega_o t + (j-1)\frac{2\pi}{n}\right) + 0.25 \cdot V_{in} \cdot \cos\left(3 \cdot \omega_{in} t\right) \right\}_{j=1}^{6}$$

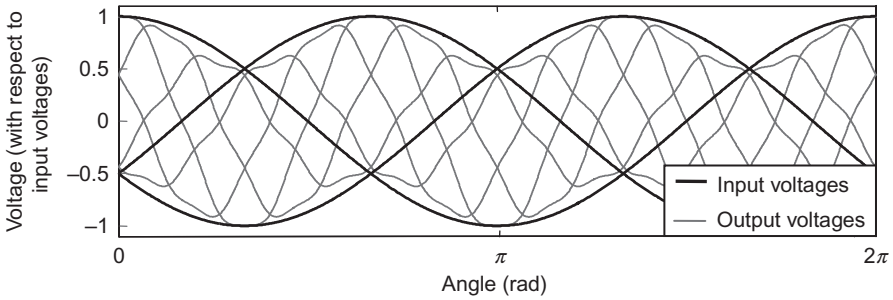


FIG. 15.79 Optimized output voltages for 3×5 matrix converter ($q=0.7886$, $f_o=3f_{in}$).

where $V_o=(\text{VTR}_{\max})V_{in}$, and $\text{VTR}_{\max}=0.75$. The optimized output voltages for this case are seen in Fig. 15.80.

Even-phase input and odd-phase output MC

When inputs are even and outputs are odd, only output-voltage optimization is done. So in accordance with (15.175), the reference output voltages are written as

$$\underline{v}_o(t)=\left\{V_o\cos\left(\omega_o t+(j-1)\frac{2\pi}{n}\right)-\frac{1}{n}\sin\left(\frac{\pi}{2n}\right)V_o\cos n\omega_o t\right\}_{j=1}^{n} \tag{15.183}$$

where $V_o=(\text{VTR}_{\max})V_{in}$ and $\text{VTR}_{\max}$ is defined by (15.166). For 6×3 MC, (15.182) is written as

$$\underline{v}_o(t)=\left\{V_o\cos\left(\omega_o t+(j-1)\frac{2\pi}{n}\right)-\frac{1}{6}V_o\cos 3\omega_o t\right\}_{j=1}^{n}$$

$V_o=qV_{in}$ and $\text{VTR}_{\max}=1$. This is illustrated in Fig. 15.81. The appreciable fact is that $\text{VTR}_{\max}$ is unity, which is 0.7321 only, if optimization is not done.

15.5.4 Simplified Modulation Strategy

This method is discussed in [12] lately. It is simple and is applicable to any MC configuration. Moreover, unity input displacement factor (IDF) is achieved. The results clearly exhibit the IDF.

Matrix operations are done to derive the modulation matrix $[M]_{n\times m}$. Considering matrix $m\times n$ converter shown in Fig. 15.70 and applying Kirchhoff's voltage law, combining with constraint equation is derived as

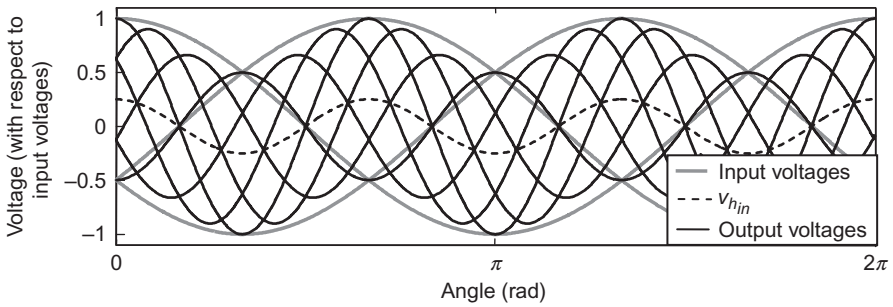


FIG. 15.80 Optimized output voltages for 3×6 matrix converter ($q=0.75$, $f_o=3f_{in}$).

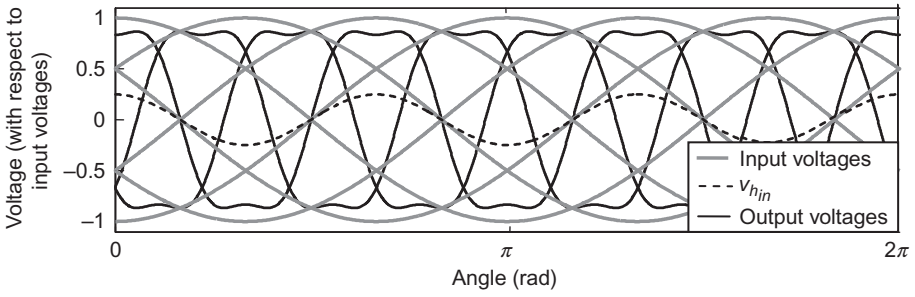


FIG. 15.81 Optimized output voltages for 6×3 matrix converter ($q=1$, $f_o=3f_{in}$).

$$\underbrace{\begin{bmatrix} v_{o1} \\ v_{o2} \\ v_{o3} \\ \vdots \\ v_{on} \\ 1 \\ 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix}}_{Y}_{2n\times 1} = \underbrace{\begin{bmatrix} \overbrace{v_{in1}\ v_{in2}\ \dots\ v_{inm}}^{1}\ \overbrace{0\ 0\ \dots\ 0}^{2}\ \overbrace{0\ 0\ \dots\ 0}^{3}\ \cdots\ \overbrace{0\ 0\ \dots\ 0}^{n} \\ 0\ 0\ \dots\ 0\ v_{in1}\ v_{in2}\ \dots\ v_{inm}\ 0\ 0\ \dots\ 0\ \cdots\ 0\ 0\ \dots\ 0 \\ 0\ 0\ \dots\ 0\ 0\ 0\ \dots\ 0\ v_{in1}\ v_{in2}\ \dots\ v_{inm}\ \cdots\ 0\ 0\ \dots\ 0 \\ \vdots \\ 0\ 0\ \dots\ 0\ 0\ 0\ \dots\ 0\ 0\ 0\ \dots\ 0\ \cdots\ v_{in1}\ v_{in2}\ \dots\ v_{inm} \\ 1\ 1\ \dots\ 1\ 0\ 0\ \dots\ 0\ 0\ 0\ \dots\ 0\ \cdots\ 0\ 0\ \dots\ 0 \\ 0\ 0\ \dots\ 0\ 1\ 1\ \dots\ 1\ 0\ 0\ \dots\ 0\ \ 0\ 0\ \dots\ 0 \\ \vdots \\ 0\ 0\ \dots\ 0\ 0\ 0\ \dots\ 0\ 0\ 0\ \dots\ 0\ \ 1\ 1\ \dots\ 1 \end{bmatrix}}_{A}_{2n\times nm} \underbrace{\begin{bmatrix} [M_{11}\ M_{12}\ M_{13}\ \cdots\ M_{1m}]^T \\ [M_{21}\ M_{22}\ M_{23}\ \cdots\ M_{2m}]^T \\ [M_{31}\ M_{32}\ M_{33}\ \cdots\ M_{3m}]^T \\ \vdots \\ [M_{n1}\ M_{n2}\ M_{n3}\ \cdots\ M_{nm}]^T \end{bmatrix}}_{X}_{nm\times 1} \tag{15.184}$$

X denotes the modulation vector, and Y is the vector of desired output voltages. Now, X is derived as

$$X = A^T\left(AA^T\right)^{-1}Y \tag{15.185}$$

AA^T when solved will have terms $\sum_{i=1}^{m} v_{in_i}^2$ and $\sum_{i=1}^{m} v_{in_i}$, so, let $\sum_{i=1}^{m} v_{in_i}^2 = L$ and $\sum_{i=1}^{m} v_{in_i} = M$. Each term of X when Eq. (15.184) is solved is of similar pattern and can be shown as

$$M_{ji} = \frac{1}{(mL - M^2)}\left[v_{o_j}(mv_{in_i} - M) - Mv_{in_i} + L\right] \tag{15.186}$$

where M_{ji} is the time-based index corresponding to the switch S_{ji} that connects jth output to the ith input. The time duration for which this switch is on is calculated by multiplying this index with sampling time. Further solving by considering m balanced input phases and finally neglecting the terms with denominators with high value, solution for $m \times n$ matrix converter is written as

$$M_{ji} = \frac{1}{m}\left(1 + \frac{2v_{in_i}v_{o_j}}{V_{in}^2}\right) \tag{15.187}$$

This formula is general for all input and output cases and does not carry any discrimination of odd or even. v_{oj} is the target output voltage, which for optimum output voltages are referred to expressions derived in previous sections. Experimental prototype of 3×9 MC is shown in Fig. 15.82, and experimental results for 3×5 matrix converter obtained are shown in Fig. 15.83.

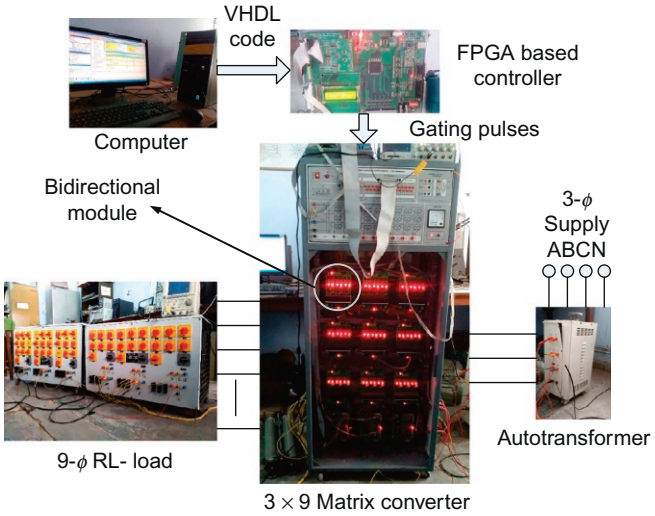


FIG. 15.82 Experimental prototype of a 3×9 MC.

15.5.5 Other Control Techniques

Other modulation strategies that are discussed for MPMCs are space-vector modulation [17], sinusoidal carrier-based modulation [16], and direct-duty-ratio-based method [18]. Novel methods like reduced commutation method [50] is also considered.

Space-vector PWM technique is highly recommended for VSIs as it increases the DC bus utilization and is easily digitally realized. This method is extended to multiphase matrix converters and is realized for 3×5 MC in [17]. In this algorithm, the input currents and output line voltages are represented on space-vector planes as shown in Fig. 15.84. The number of switching states for an $m \times n$ MC is $2^{m\times n}$. However, after applying the constraints discussed in Chapter 14, these reduce to m^n. For example, for a 3×5 MC, a total number of combinations can be 2^{15}, that is, 32,768, and with constraints, this figure reduces to 3^5, that is, 243 combinations. However, in [17], only 93 active and three zero vectors are utilized and are further categorized into 4 groups, namely, large vectors (30 vectors), medium vectors (30 vectors), small vectors (30 vectors), and zero vectors (3 vectors). Fig. 15.84 exhibits input current and output line voltage space vectors in which only large (L) and medium (M) vectors are shown. The detailed calculations of the dwelling times can be seen in [17]:

A new modulation technique is introduced in [50], where least *commutation number* is achieved. According to normal SVPWM, Venturini or the method discussed in Section 15.5.5, in one switching time cycle, the output voltage must ride on all input voltage, and the average of these samples must be equal to the reference output voltage. This leads to $(m-1) \times n$

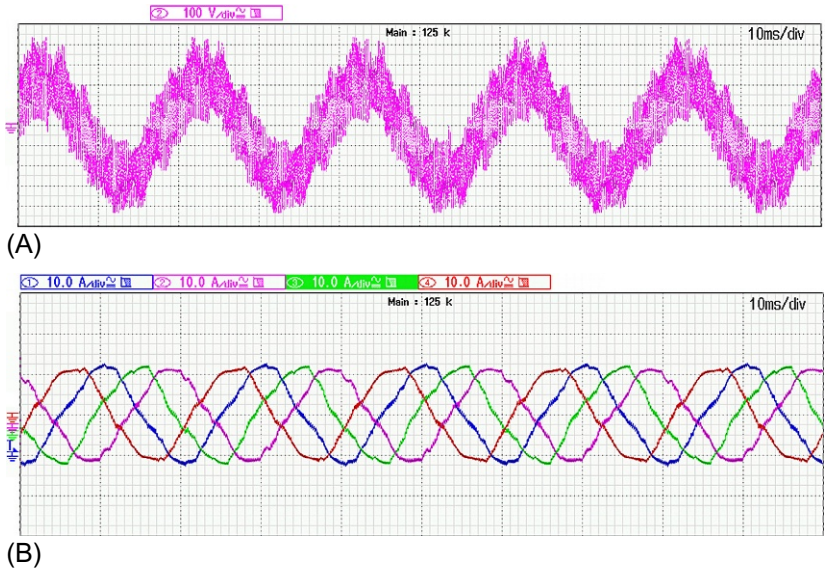


FIG. 15.83 Experimental output (A) phase voltage and (B) currents ($f_o = 50$ Hz).

commutations per switching cycle. For 3×5 MC, this will be 10 commutations and are shown in Fig. 15.85A. However, the method proposed in [50] employs only five commutations per cycle, as shown in Fig 15.85B. This provides low THD in output voltages and reduction in the stress on the switches.

15.5.6 Future Prospects

In the above sections, the main focus was on DMMC; however, IMMC is now getting considerable attention [51,52]. Research on MPMCs is still under progress, and there is a lot of scope left in this area. The possible areas of research are summarized, which in conjunction with one another may create a new area of research:

In Terms of Topology

- Z-source DMMC and IMMC
- Multiphase multilevel MC
- Multiphase multimodular matrix converters
- Sparse and ultrasparse multiphase MC

In Terms of Control

- Overmodulation in DMMC
- Enhanced SVPWM techniques
- Reactive power control
- Predictive control
- Periodic control
- Low-switching-frequency PWM

There are many more areas to be considered. Moreover, filter design, EMI considerations, and consideration of faults and unbalanced supplies for MPMCs are also the areas of research.

15.6 Multiphase DC-DC Converter

A multiphase DC-DC converter consists of two or more DC-DC converters operating in parallel at the same frequency with a proper phase shift existing between each other. The parallel operating converters has a common DC source (battery, PV panel, etc.) that feeds power to a common load. Consequently, this type of circuit configuration enables the load to be subjected to an effective frequency that is a multiple of the converter frequency (f), thereby increasing the ripple frequency of the supply harmonic current. The filter requirement is reduced compared with a single-level implementation. The multiphase DC-DC step-down converter or buck converter offers a viable solution for the voltage regulator module (VRM), which is used to power the microprocessors in computers and other applications. At present, VRMs require output voltage less than 1 V and an output current of more than 100 A [53].

Various topologies have been reported in literature with varying control strategy [53,54]. The most common topologies are as follows:

1. Multiphase interleaved buck topology
2. Multiphase synchronous buck topology
3. Multiphase tapped-inductor buck topology
4. Multiphase interleaved boost topology

15.6.1 Multiphase Interleaved Buck Topology

Fig. 15.86 shows an n phase multiphase interleaved buck converter. The individual phase ripple frequency is added to obtain an output current with high ripple frequency. The ripple cancellation of inductor current for a three phase converter

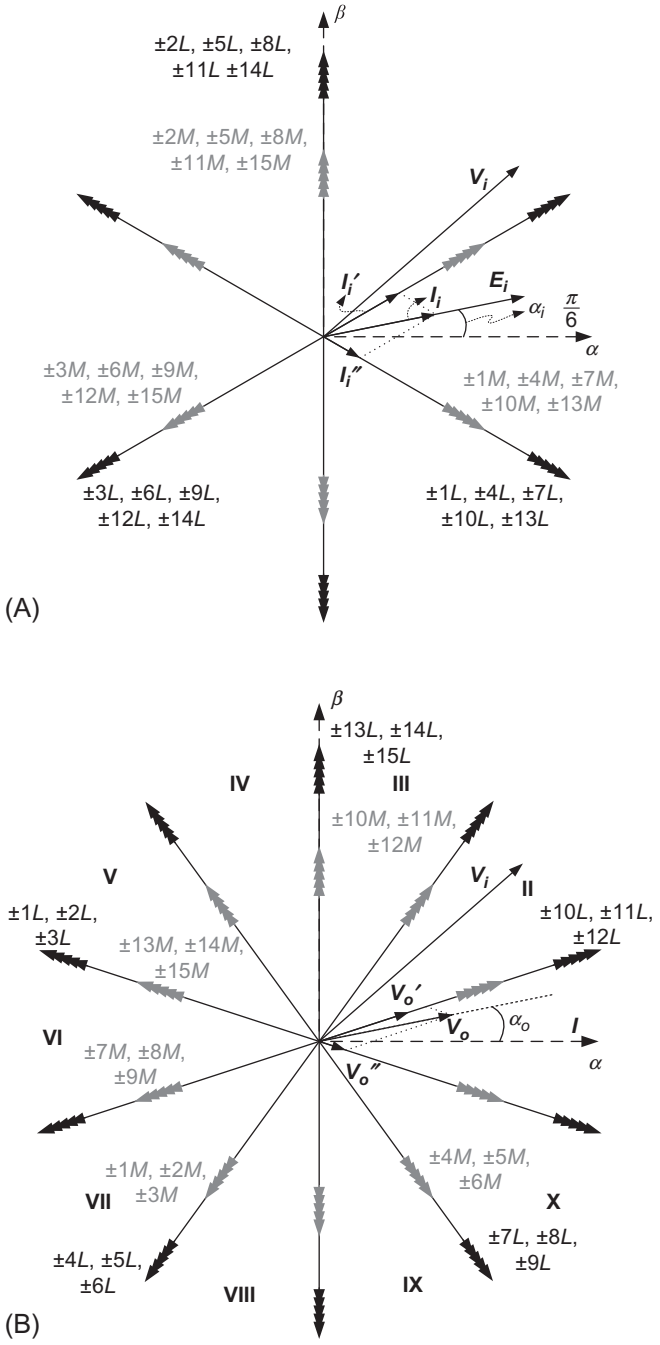


FIG. 15.84 (A) Input current and (B) output-voltage space vectors corresponding to large and medium vectors [17].

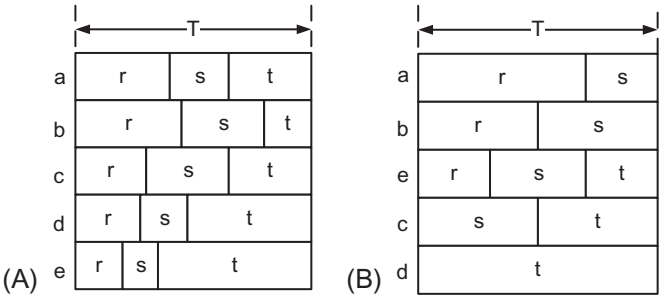


FIG. 15.85 (A) Commutation in one time cycle with conventional schemes [43] and (B) commutation in one time cycle observed in [50].

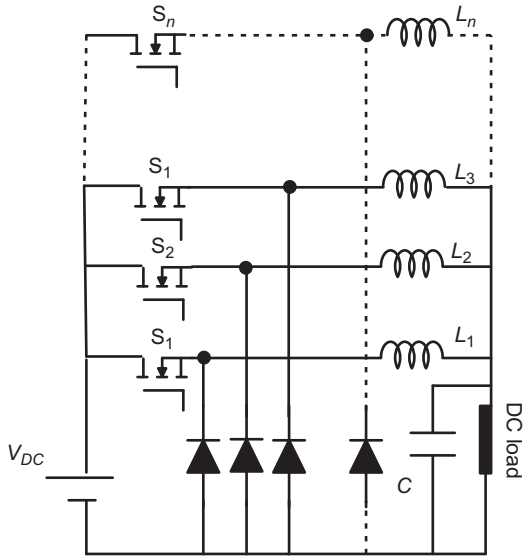


FIG. 15.86 *n*-Phase interleaved buck converter.

is shown in Fig. 15.87A. The inductor current ripples add up to give three times the ripple frequency with respect to the converter operating individually. The magnitude of output current also increases. The ripple cancellation of the output inductor current reduces the requirement of the output capacitance and consequently lowers the cost and reduces the power dissipation. The increased input ripple current frequency causes the multiphase buck converter to have reduced input ripple current magnitude (Fig. 15.87B), thereby reducing the size requirement of input capacitor and cost reduction of the overall system.

15.6.1.1 Operation of Multiphase Buck Converter

The operation of a two-phase interleaved buck converter (Fig. 15.88) has been discussed in detail. The operating principle remains the same in all higher phases of the converter. Inductors ensure that continuous current flows through the load and the resultant current through output is the sum of the current through each inductor. The frequency of ripples in the current through load is twice that of frequency of ripple current through each inductor. The sum of duty ratios of the two switches is less than or equal to 1.

15.6.1.2 Modes of Operation

Mode 1. S_1 is on and S_2 is off (T_1)

When S_1 is on, current flows through the circuit as shown in Fig. 15.89. The diode D_1 is reverse-biased because of the

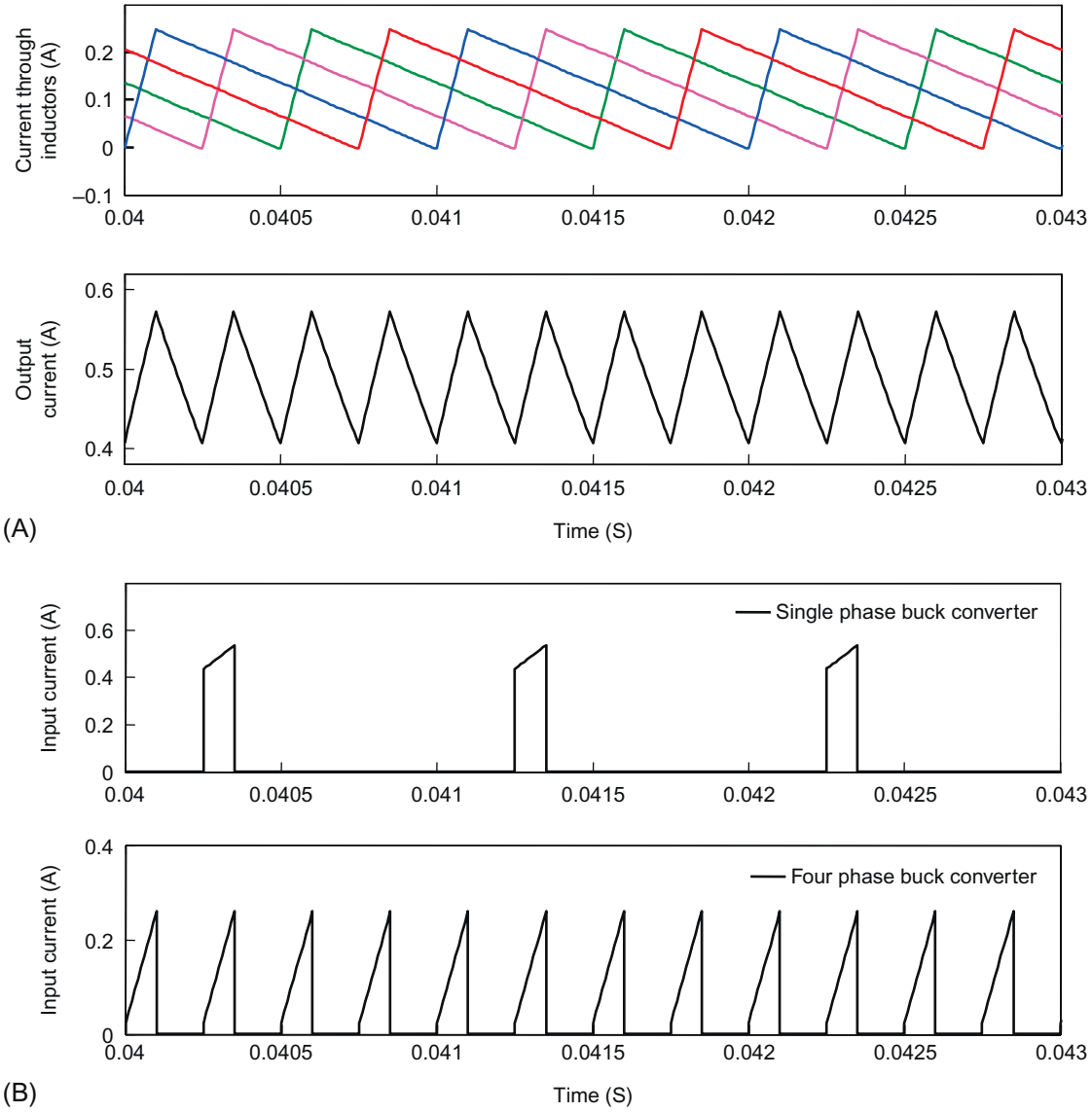


FIG. 15.87 (A) Inductor current cancelation in a four-phase converter (simulation result) and (B) comparison of single-phase and four-phase input current (simulation result).

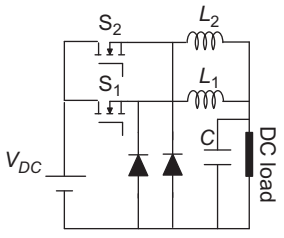


FIG. 15.88 Two-phase buck converter topology.

polarity of inductor L_1 and does not conduct, whereas the diode D_2 is forward-biased and freewheels the current through L_2. During the interval when S_1 is turned on (T_1), the current through L_1 increases while the current through L_2 decreases linearly. i_{L_1} and i_{L_2} varies according to the following relations:

$$\Delta i_{L_1} = \frac{(v_{DC} - v_o)}{L_1} T_1 \tag{15.188}$$

$$\Delta i_{L_2} = \frac{(-v_o)}{L_1} T_1 \tag{15.189}$$

where V_{DC} is the input side voltage and v_O is the output side voltage.

Mode 2. Both S_1 and S_2 are off (T_2)

The duty ratio for each phase of the converter operation is less than 0.5 which reduces for higher phase converter. During transition of switching from S_1 to S_2 both the switches will be off. In this mode, diodes D_1 and D_2 conduct. Inductors L_1 and L_2 release the energy stored in the previous modes to the

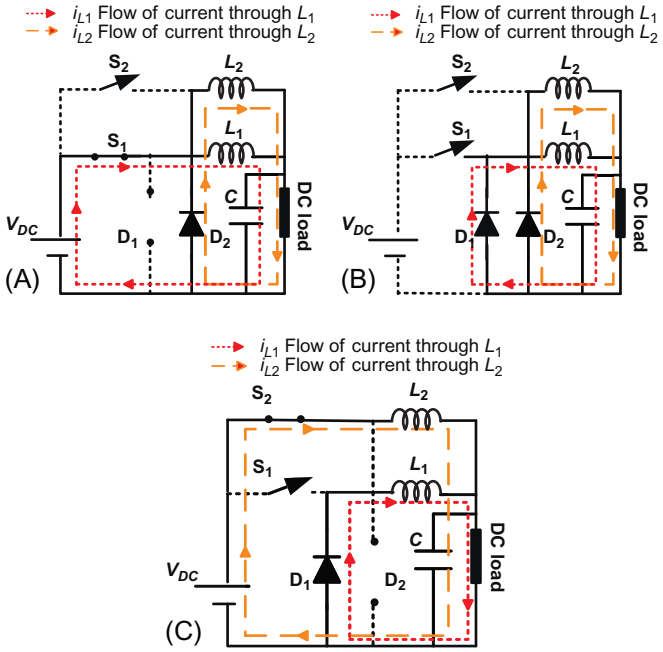


FIG. 15.89 Switching diagrams under various modes of operation for a two-phase buck converter: (A) Mode 1, (B) Mode 2, and (C) Mode 3.

load through the freewheeling diodes D_1 and D_2. The current through inductors L_1 and L_2, i.e. i_{L_1} and i_{L_2} decrease linearly. i_{L_1} and i_{L_2} varies according to the following relations:

$$\Delta i_{L_1} = \frac{(-v_o)}{L_1} T_2 \tag{15.190}$$

$$\Delta i_{L_2} = \frac{(-v_o)}{L_2} T_2 \tag{15.191}$$

Mode 3. S_2 is on and S_1 is off (T_3)

When S_2 is on, current flows in the circuit as shown in Fig. 15.89C. The diode D_2 is reverse-biased because of the polarity of inductor L_2 and does not conduct, whereas the diode D_1 is forward-biased and freewheels the current through L_1. While S_2 is on, the inductor L_2 gets charged while inductor L_1 discharges through load. i_{L_1} and i_{L_2} (currents flowing through L_1 and L_2, respectively) during T_3 are given by the equations:

$$\Delta i_{L_1} = \frac{(-v_o)}{L_1} T_3 \tag{15.192}$$

$$\Delta i_{L_2} = \frac{(v_{DC} - v_o)}{L_2} T_3 \tag{15.193}$$

State space analysis

The converter system can be expressed in state equation of the form

$$\dot{X} = AX + BU \tag{15.194}$$

$$V = C^T X \tag{15.195}$$

where the state-space variables are defined as

$$\dot{X} = \begin{bmatrix} \frac{di_{L_1}}{dt} & \frac{di_{L_2}}{dt} & \frac{dv_C}{dt} \end{bmatrix}^T$$

$$X = \begin{bmatrix} i_{L_1} & i_{L_2} & v_C \end{bmatrix}^T$$

$$U = \begin{bmatrix} v_{DC} & 0 & 0 \end{bmatrix}^T$$

V is the output-voltage vector.

15.6.1.3 Modes of Operation

Mode 1

$$\begin{bmatrix} \frac{di_{L_1}}{dt} \\ \frac{di_{L_2}}{dt} \\ \frac{dv_C}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-1}{L_1} \\ 0 & 0 & 0 \\ \frac{1}{C} & 0 & \frac{-1}{RC} \end{bmatrix} \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_{DC} \\ 0 \\ 0 \end{bmatrix} \tag{15.196}$$

$$\dot{X} = A_1 X + B_1 U$$

Mode 2

$$\begin{bmatrix} \frac{di_{L_1}}{dt} \\ \frac{di_{L_2}}{dt} \\ \frac{dv_C}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-1}{L_1} \\ 0 & 0 & \frac{-1}{L_2} \\ \frac{1}{C} & \frac{1}{C} & \frac{-1}{RC} \end{bmatrix} \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_C \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_{DC} \\ 0 \\ 0 \end{bmatrix} \tag{15.197}$$

$$\dot{X} = A_2 X + B_2 U$$

Mode 3

$$\begin{bmatrix} \frac{di_{L_1}}{dt} \\ \frac{di_{L_2}}{dt} \\ \frac{dv_C}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{L_2} \\ 0 & \frac{1}{C} & \frac{-1}{RC} \end{bmatrix} \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_C \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ \frac{-1}{L_2} & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_{DC} \\ 0 \\ 0 \end{bmatrix} \tag{15.198}$$

$$\dot{X} = A_3 X + B_3 U$$

15.6.1.4 State Space Averaging

State-space averaging can be done to replace the above sets of state-space equations by a single equation that describe the system over one switching period:

$$A = A_1 D_1 + (1 - D_1 - D_3) A_2 + A_3 D_3 \tag{15.199}$$

$$B = B_1D_1 + (1 - D_1 - D_3)B_2 + B_3D_3 \tag{15.200}$$

Assuming the duty ratio of mode 1 and 3 are same, then for mode 2, it is $1 - D$

Therefore,

$$A = (A_1 + A_3)D + (1 - 2D)A_2 \tag{15.201}$$

$$B = (B_1 + B_3)D + (1 - 2D)B_2 \tag{15.202}$$

15.6.1.5 Small Signal Analysis

In small-signal analysis, it is assumed that all variables are perturbed around steady-state operating point. Applying perturbations to above equation leads to

$$\begin{aligned}\dot{X}^- + \dot{x} = &\{(A_1 + A_3)(D + d) + 1 - 2(D + d)A_2\}\left(\bar{X} + x\right) \\ &+ \{(B_1 + B_3)(D + d) + 1 - 2(D + d)B_2\}\left(\bar{U} + u\right)\end{aligned} \tag{15.203}$$

Where average term is represented by a superscript while small signal term is represented by small letters. Neglecting the product of terms containing small signal and taking the derivative of steady-state component as zero simplify the above equation to

$$\begin{aligned}\dot{x} = &\{(A_1 + A_3)D + (1 - 2D)A_2\}x + [(B_1 + B_3)D \\ &+ (1 - 2D)B_2]u + [(A_1 + A_3 - 2A_2)X + (B_1 + B_3 - 2B_2)U]d\end{aligned} \tag{15.204}$$

Taking Laplace transform on both sides,

$$\begin{aligned}s\dot{x} = &\{(A_1 + A_3)D + (1 - 2D)A_2\}x(s) + [(B_1 + B_3)D \\ &+ (1 - 2D)B_2]u(s) + [(A_1 + A_3 - 2A_2)X \\ &+ (B_1 + B_2 - 2B_3)U]d(s)\end{aligned} \tag{15.205}$$

$$\begin{aligned}\dot{x} = &[SI - A]^{-1}\{[(B_1 + B_3)D + (1 - 2D)B_2]u(s) \\ &+ \left[M^{'}X + NU\right]d(s)\}\end{aligned} \tag{15.206}$$

where $M^{'} = (A_1 + A_3 - 2A_2)$ and $N = (B_1 + B_2 - 2B_3)$:

$$V_o(S) = C^T x(s) \tag{15.207}$$

Putting the value of Eq. (15.204) into Eq. (15.205), we have

$$\frac{v_o(s)}{v_{DC}(s)} = \frac{s(1 - D)(L_1 + L_2)}{s^3L_1L_2C + s\dfrac{L_1L_2}{R} + s(1 - D)^2(L_1 + L_2)} \tag{15.208}$$

$$\frac{v_o(s)}{d(s)} = \frac{s(1 - D)(L_1 + L_2) - s^2L_1L_2(i_{L_1} + i_{L_2})}{s^3L_1L_2C + s\dfrac{L_1L_2}{R} + s(1 - D)^2(L_1 + L_2)} \tag{15.209}$$

In the above analysis, ESR, ESL, and other parasitic parameters have been neglected. The detailed analysis including the parasitic parameters has been carried out by [55,56]. The waveform of current through the inductors and the output current for a two-phase buck converter are shown in Fig. 15.90. The frequency of ripple in output current is clearly seen to be twice compared with the single-phase counterpart.

Small signal analysis can be extended for an n phase converter. The time-interleaved control will ensure higher-frequency ripple pulses, thereby lesser requirement of filtering. Moreover, the cost and space requirement will also come down.

15.6.1.6 Discontinuous Conduction Mode

When the value of L_1 and L_2 is small, the current through load could be discontinuous. This is undesirable as the output voltage then becomes function of inductance complicating the control operation [55].

15.6.1.7 Variation of Output Current Ripple With Duty Ratio and Design Consideration

The main advantage of multiphase topology is the cancellation of ripple in the output current, which reduces the size of inductance and improves the transient response and the output capacitance requirement is minimized. The voltage tolerance criteria under varying load make multiphase buck converters working as VRMs use small inductance so that the power can be transferred quickly from the source side to the load side. However, small value of inductance causes large ripples in inductor current under steady state condition. So a compromise between the two has be taken into consideration while designing. The magnitude of inductor current ripples (considering inductance to be same in each buck converter loop) and the inductance value are related to each other by the equation:

$$\Delta i_L = \frac{d * v_{DC}(1 - d)}{L * f_s} \tag{15.210}$$

Multiphase buck converters interleave (alternate flow of current through the inductor in each of the converter cycle) the inductor currents in each converter operating in parallel, and hence drastically reduces the total ripples in the current which flows through the output capacitor. With the reduction in current ripple, the output voltage ripple is also greatly reduced. Therefore with lesser filter requirement, the transient response of the system improves. Hence, a smaller value of capacitance at the output can be used for meeting the transient requirement. Moreover, there is more space for variations in output voltage magnitude during load transient. Consequently, multiphase operation enhances the performance under load transient condition [57,58].

In multiphase converters, the current ripple cancelation effect K_i can be defined as the ratio of the magnitudes of output current ripple (Δi_O) and inductor current ripple (Δi_L). For n phase buck converter, the current ripple cancellation factor K_i is defined as [57]

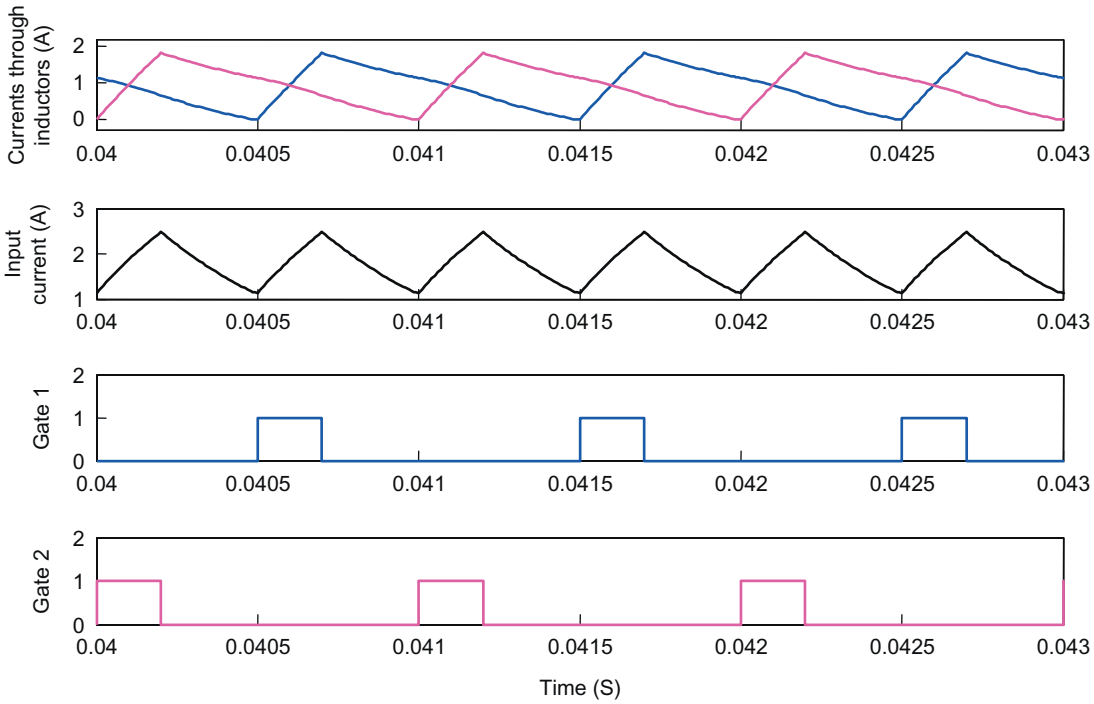


FIG. 15.90 Output current and gate pulses (simulated).

$$K_i = \frac{\Delta i_O}{\Delta i_L} = \left(1 - \frac{m}{n*d}\right)(1 + m - n*d) \tag{15.211}$$

where $m = \text{floor}\,(n*d)$, the maximum integer that does not exceed $n*d$.

For a small duty ratio, the current ripple cancellation is poor. The output current ripples increases for small duty ratios further because of the increase in the individual inductor current ripples, which can be seen from the Eq. (15.210). Substituting the Eq. (15.210) into Eq. (15.209), the output current ripples magnitude for multiphase buck converters can be derived, as follows [57]

$$\Delta i_O = \Delta i_L * K_i = \frac{d * v_{DC}(1-d)}{L * f_s} * \left(1 - \frac{m}{n*d}\right)(1 + m - n*d) \tag{15.212}$$

Fig. 15.91 shows the effect of duty ratio on the ripple of the output current for multiphase buck converters. Multiphase interleaved buck converters are basically governed by the same design equations as that of the single phase buck converter. There are n interleaved paths in a multiphase buck converter where the number of phases of the converter is represented by n. Each channel behaves as an independent buck converter. Let the output voltage and output current in a multiphase buck converter are denoted by v_o and i_o respectively. The relation of output frequency and output current of multiphase converter with one phase of multiphase buck converter is given by

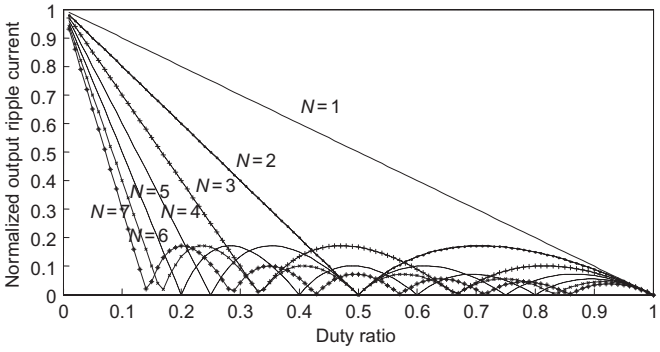


FIG. 15.91 Variation of ripple with duty ratio and phases.

$$f_O = N * f_S \tag{15.213}$$

where f_O represents is the output current ripple frequency and f_S represents the frequency of single phase ripple current. Volt second balance relationship can be used to develop the design equation for the inductor at the output.

$$V_L = L\frac{di}{dt} \tag{15.214}$$

or

$$L = V_L\frac{dt}{di} \tag{15.215}$$

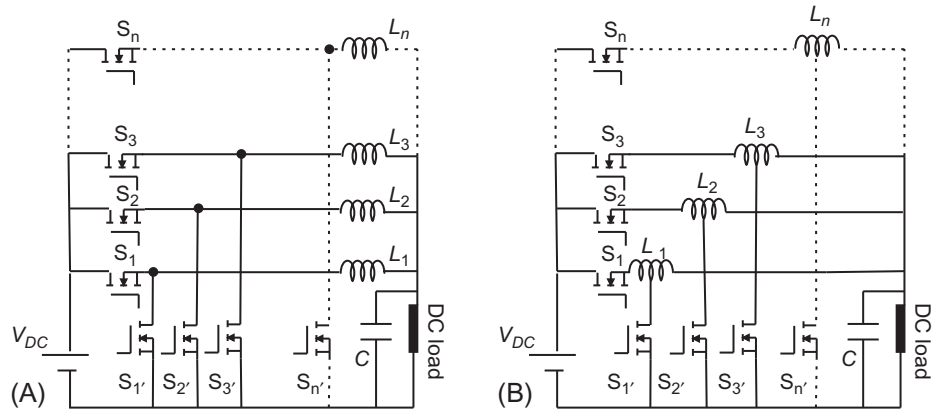


FIG. 15.92 (A) Synchronous multiphase buck converter and (B) synchronous tapped inductor multiphase buck converter.

where $di = \Delta i_L =$ the ripple current through the output inductor of each channel.

For small change in i_L we can comfortable consider $di = \Delta i_L =$ the ripple current flowing through inductor at the output of each interleaved channel. During off cycle $dt = (1-d)T_S$ where T_S represents the switching period and d represents the duty ratio of the individual switch,

Eq. (15.214) becomes

$$L = \frac{v_O(1-d)}{\Delta i_L * f_s} \tag{15.216}$$

or

$$L = \frac{d * v_{DC}(1-d)}{\Delta i_L * f_s} \tag{15.217}$$

The output voltage is kept almost constant with the selection of proper output capacitor. Equivalent series resistance (ESR) and an equivalent series inductance (ESL) are added to the output capacitor to represent a real model. At high frequency switching, ESR is dominant over ESL. So, for the purpose of analysis ESL can be neglected. The minimum capacitance for a multiphase converter can then be given by the following equation

$$C_O = \frac{\Delta i_O}{8 * f_S * \Delta v_O} \tag{15.218}$$

15.6.2 Synchronous Multiphase Buck Topology

The disadvantage of a conventional multiphase buck converter is the significant power loss during the diode conduction period, which is the product of the forward voltage drop and its current. Synchronous buck topology has a better efficiency than standard multiphase interleaved buck converter. This is obtained by replacing the diodes of multiphase buck converter by MOSFETs. Theoretical study done by [57] shows that the losses in a multiphase buck converter is more due to the forward conduction loss of the diode. The on-resistance ($R_{DS,ON}$) of MOSFET connected in place of diode is in the milliohm range during conduction hence the losses during conduction is quite less compared to its conventional counterpart thus efficiency improves.

As shown in Fig. 15.92A, a synchronous multiphase interleaved buck topology is obtained by replacing the diodes with MOSFET. Dead-times between (S_1, $S_{1'}$), (S_2, $S_{2'}$) and other switch pairs are introduced to prevent shoot-through. For a two phase synchronous converter, the current through the inductor continues to flow through internal body diode of MOSFET (S_2) during the dead time. On application of gate signal on MOSFET (S_2), the current through inductor flows through S_2. As mentioned earlier, with technological advancement there is a requirement for larger current by the processors to meet the growing diverse application demand. The multiphase synchronous buck topology has been adopted in industry to handle such high current processors. The majority of VRC for laptop processor and embedded system board are using synchronous topology today instead of conventional buck. The Intel roadmap suggests that the voltage will be reduced by 0.6 fraction with each passing generation of processor. Currently, the input supply voltage to microprocessors embedded system board is in the range of 0.8–1.6 V [58–60]. But to generate a very low output voltage from higher output voltage, the duty ratio for multiphase synchronous buck converters should be very small. This increases the losses across the switches and the overall converter efficiency reduces. So a synchronous tapped inductor multiphase buck converter topology has been proposed [57] to overcome this disadvantage. A synchronous tapped inductor multiphase buck converter is shown in Fig. 15.92B. To realize a tapped inductor buck converter, only a minor modification in the original buck converter circuit is required.

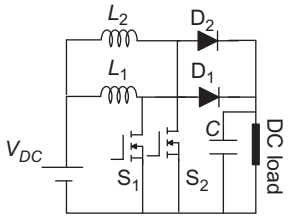


FIG. 15.93 Multiphase boost topology.

15.6.3 Multiphase Boost Converter

There is an increasing popularity for high power boost converters among power electronic designers in the industrial, automotive and telecom industries for high power application. For large power levels, efficiency becomes quite important in the power converter components. The multiphase boost converter is a viable option for such applications (Fig. 15.93). The ripple voltage and currents in both the input and output capacitors of a multiphase boost converter is very less. Therefore smaller components are required for filtering purpose. Thus, the requirement of bulky heat sinks and forced-air cooling is not there is case of multiphase boost converter [61,62]. Hence, the efficiency of such converters are quite high. The direction of power flow is different in a multiphase buck and boost converter which otherwise have same circuit topology. The input of the buck converter and the output of the boost converter are pulsating type current. On the other hand, the output of the buck converter and the input to the boost converter are continuous currents.

15.6.3.1 Modes of Operation

Mode 1

During mode 1, both the switches S_1 and S_2 are on, and the diodes D_1 and D_2 are in the off condition:

$$\frac{di_{L_1}}{dt}=\frac{V_{DC}}{L_1} \tag{15.219}$$

$$\frac{di_{L_2}}{dt}=\frac{V_{DC}}{L_2} \tag{15.220}$$

$$\frac{dv_O}{dt}=\frac{-V_O}{RC} \tag{15.221}$$

The coefficient matrix for this mode can be written as

$$A_1=\begin{bmatrix}0 & 0 & 0\\ 0 & 0 & 0\\ 0 & 0 & \frac{-1}{RC}\end{bmatrix} B_1=\begin{bmatrix}\frac{-1}{L_1}\\ \frac{-1}{L_2}\\ 0\end{bmatrix} \tag{15.222}$$

Mode 2

During mode 2, switch S_1 is in on condition, switch S_2 is in off condition, and the corresponding diodes are in the complementary switching states, that is, D_1 is in off condition and D_2 is in on condition, respectively:

$$\frac{di_{L_1}}{dt}=\frac{V_{DC}}{L_1} \tag{15.223}$$

$$\frac{di_{L_2}}{dt}=\frac{V_{DC}}{L_2}-\frac{V_O}{L_2} \tag{15.224}$$

$$\frac{dv_O}{dt}=\frac{i_{l_2}}{C}-\frac{-V_O}{RC} \tag{15.225}$$

$$A_2=\begin{bmatrix}0 & 0 & 0\\ 0 & 0 & \frac{-1}{L_2}\\ 0 & \frac{1}{C} & \frac{-1}{RC}\end{bmatrix} B_2=\begin{bmatrix}\frac{1}{L_1}\\ \frac{1}{L_2}\\ 0\end{bmatrix} \tag{15.226}$$

Mode 3

In mode 3, switch S_1 is in off condition, switch S_2 is in on condition, and the corresponding diodes D_1 and D_2 are in on and off conditions, respectively:

$$\frac{di_{L_1}}{dt}=\frac{V_{DC}}{L_1}-\frac{V_O}{L_1} \tag{15.227}$$

$$\frac{di_{L_2}}{dt}=\frac{V_S}{L_2} \tag{15.228}$$

$$\frac{dv_0}{dt}=\frac{i_{L_1}}{C}-\frac{-V_O}{RC} \tag{15.229}$$

$$A_3=\begin{bmatrix}0 & 0 & \frac{-1}{L_1}\\ 0 & 0 & 0\\ \frac{1}{C} & 0 & \frac{-1}{RC}\end{bmatrix} B_3=\begin{bmatrix}\frac{1}{L_1}\\ \frac{1}{L_2}\\ 0\end{bmatrix} \tag{15.230}$$

Mode 4

During mode 4, the semiconductor switches S_1 and S_2 are in off condition, and the diodes D_1 and D_2 are in on condition:

$$\frac{di_{L_1}}{dt}=\frac{V_{DC}}{L_1}-\frac{V_O}{L_1} \tag{15.231}$$

$$\frac{di_{L_2}}{dt}=\frac{V_{DC}}{L_2}-\frac{V_O}{L_2} \tag{15.232}$$

$$\frac{dv_O}{dt}=\frac{i_{l_1}}{c}+\frac{i_{l_2}}{c}-\frac{V_O}{RC} \tag{15.233}$$

$$A_4 = \begin{bmatrix} 0 & 0 & \frac{-1}{L_1} \\ 0 & 0 & \frac{-1}{L_2} \\ \frac{1}{C} & \frac{1}{C} & \frac{-1}{RC} \end{bmatrix} B_4 = \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \end{bmatrix} \quad (15.234)$$

The coefficient matrix for the two-phase boost converter are defined as

$$[A] = A_1 d_1 + A_2 d_2 + A_3 d_3 + A_4 d_4 \quad (15.235)$$

$$[B] = B_1 d_1 + B_2 d_2 + B_3 d_3 + B_4 d_4 \quad (15.236)$$

$$[U] = V_S \quad (15.237)$$

$$d_1 + d_2 + d_3 + d_4 = 1 \quad (15.238)$$

Expressions for A_1, A_2, A_3, and A_4 are defined above.

Output equation can be written as $y(t) = [0 \;\; 0 \;\; 1] \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_O \end{bmatrix}$

Fig. 15.94 shows switching diagram for a multiphase boost converter while Fig. 15.95 shows current through inductors and output current.

15.6.4 Coupled Inductor for Multiphase Buck

Ripple cancelation in the output or input current for buck and boost operation, respectively, is one of the major advantage of interleaving technique. But, there is reduction in total input current and output current ripple only while large ripples are still present in the individual inductor present in each interleaved converter [13]. Moreover, the large current ripples in the inductor causes large copper loss. These large conduction losses in inductors and switching losses in the switch cannot be resolved by interleaving technique. Therefore, in order to overcome this problem, multiphase interleaved buck and boost converters have coupled inductors. The equivalent inductances of the coupling inductor reduces in case of coupled inductor multiphase buck topology thereby reducing the ripple current in the coupled inductors. The transient response is not compromised. Fig. 15.96 shows a two level Coupled inductor multiphase boost converter. In Fig. 15.97, current flowing through inductors in case of coupled and uncoupled configuration has been compared.

15.6.4.1 Modes of Operation

Mode 1

During mode 1, the switches S_2 is on, and the diode D_1 is conducting:

$$v_{L_1} = L_1 \frac{di_{L_1}}{dt} + M \frac{di_{L_2}}{dt} = V_{DC} - V_O \quad (15.239)$$

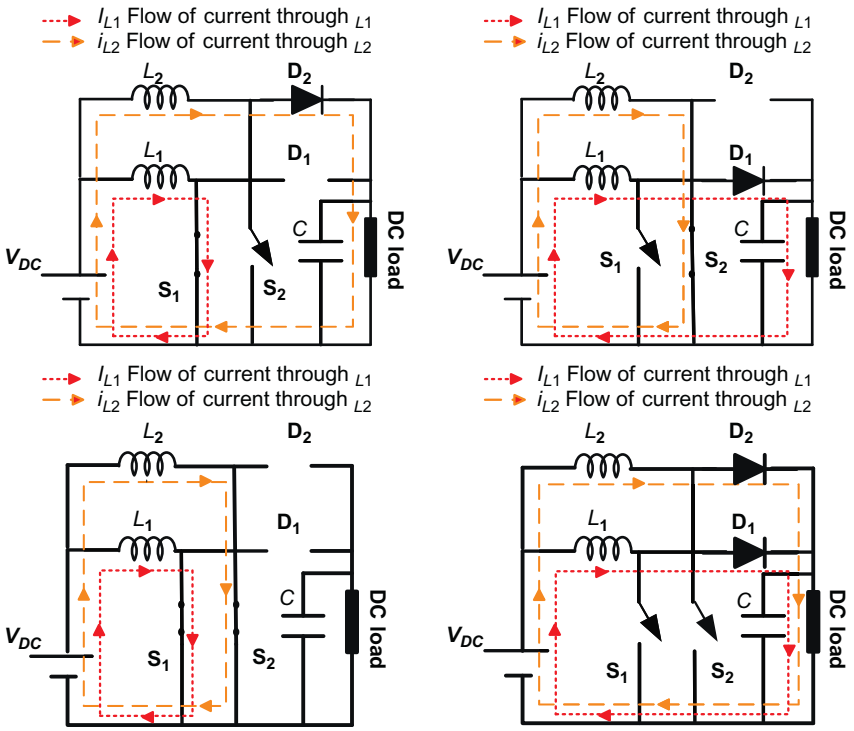


FIG. 15.94 Switching diagram for multiphase boost converter: (A) Mode 1 and Mode 2, (B) Mode 3 and Mode 4.

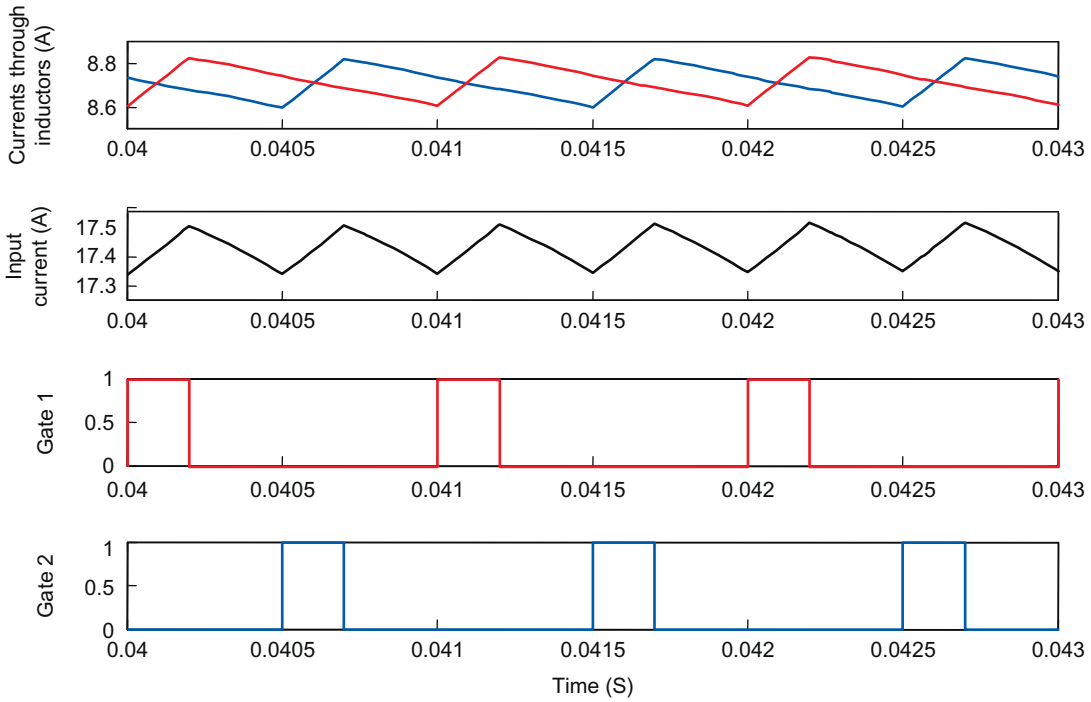


FIG. 15.95 Current through inductors and output with switching pulses.

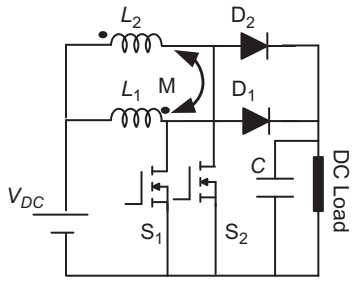


FIG. 15.96 Coupled inductor multiphase boost converter.

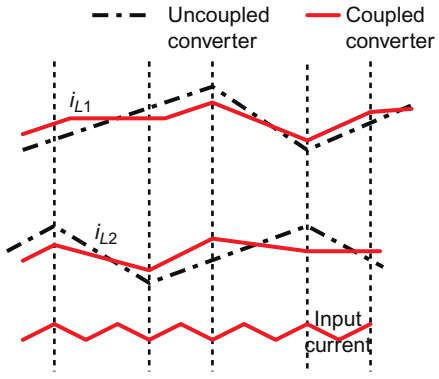


FIG. 15.97 Input current waveforms for coupled inductor multiphase buck converter.

$$v_{L_2} = L_2 \frac{di_{L_2}}{dt} + M \frac{di_{L_1}}{dt} = V_{DC} \tag{15.240}$$

In this case, inductances L_1 and L_2 are given by

$$L_{1,\text{ equiv.}} = \frac{L_1^2 - M^2}{L_1 - \frac{d}{d'}.M} \tag{15.241}$$

$$L_{2,\text{ equiv}} = \frac{L_2^2 - M^2}{L_2 - \frac{d}{d'}.M} \tag{15.242}$$

When $L_1 = L_2 = L$, equivalent inductance is

$$L_{\text{mode, 1}} = \frac{L^2 - M^2}{L - \frac{d}{d'}.M} \tag{15.243}$$

Mode 2

During mode 2, switch S_1 and switch S_2 are in off condition, and the corresponding diodes are in on condition.

In this case, the equivalent inductance is given by

$$L_{1,\text{equiv.}} = L_1 - M \tag{15.244}$$

$$L_{2,\text{equiv.}} = L_2 - M \tag{15.245}$$

When $L_1 = L_2 = L$, equivalent inductance is

$$L_{\text{mode},2} = L - M \tag{15.246}$$

Mode 3

During mode 3, switch S_1 is on, and the diode D_2 is conducting.

The equivalent inductance will be same as in mode 1.

Mode 4

During mode 4, switch S_1 and switch S_2 are in off condition, and the corresponding diodes are in on condition. The equivalent inductance will be the same as in mode 2.

The peak-to-peak current in the case of coupled and uncoupled converter topologies are given by

$$\Delta I_{ripple} = \frac{V_{DC} d}{L_{\text{mode},1} f_s} \tag{15.247}$$

$$\Delta I_{ripple} = \frac{V_{DC} d}{L f_s} \tag{15.248}$$

where f_s is the switching frequency and $L_{\text{mode},1}$ and L are inductances of coupled and uncoupled converter. Clearly, the peak variation of input current in the case of coupled inductor is less compared with uncoupled inductor topology.

15.6.5 Advantages of Multiphase DC-DC Converters

Some of the advantages associated with multiphase DC-DC converters are listed below:

- Output ripple increases in multiplicity, reducing the filter requirements
- Reduction in the size and cost of output inductor and capacitor
- Reduction in the size and cost of input capacitor
- Reduced overall loss in the circuit compared with same rated single-phase counterpart
- Ideally suited for application requiring tight current regulation like VRM
- High-power and load current application like DC motor drives

References

[1] E. Levi, R. Bojoi, F. Profumo, H.A. Tolyat, S. Williamson, Multiphase induction motor drives – a technology status review, Electr. Power Appl. IET 1 (2007) 489–516.

[2] E. Levi, Multiphase electric machines for variable-speed applications, IEEE Trans. Ind. Electron. 55 (2008) 1893–1909.

[3] B. Bose, Power electronics and motor drives: recent progress and perspective, IEEE Trans. Ind. Electron. 56 (Feb. 2009) 581–588.

[4] E. Levi, Advances in converter control and innovative exploitation of additional degrees of freedom for multiphase machines, IEEE Trans. Ind. Electron. 63 (1) (2016) 433–448.

[5] E. Levi, N. Bodo, O. Dordevic, M. Jones, Recent advances in power electronic converter control for multiphase drive systems, in: 2013 IEEE Workshop on Electrical Machines Design, Control and Diagnosis (WEMDCD), Paris, 2013. pp. 158–167.

[6] T.J. McCoy, Trends in ship electric propulsion, in: IEEE PES Summer Meeting, 25 July 2002, Chicago, IL, 2002, pp. 343–346.

[7] A. Tessarolo, G. Zocco, C. Tonello, Design and testing of a 45-MW 100-Hz quadruple-star synchronous motor for a liquefied natural gas turbo-compressor drive, IEEE Trans. Ind. Appl. 47 (3) (2011) 1210–1219.

[8] A. Tessarolo, Experimental performance assessment of multiphase alternators supplying multiple AC/DC power converters, J. Energy Power Eng. 4 (12) (2010) 43–50.

[9] M.I. Masoud, Five-phase uncontrolled line commutated rectifier: AC side compensation using shunt active power filter, in: The Proceedings of 8th GCC Conference, 1–4 February, Muscat, Oman, 2015.

[10] M.I. Masoud, Fully controlled 5-phase, 10-pulse, line commutated rectifier, Alex. Eng. J. 54 (4) (2015) 1091–1104.

[11] M. Ali, M.R. Khan, M. Ayyub, Analysis of three-phase input to five-phase output matrix converter using direct transfer function approach, in: IEEE RDCAPE, 2015, pp. 161–166.

[12] M. Ali, A. Iqbal, M.R. Khan, M. Ayyub, M.A. Anees, Generalized theory and analysis of scalar modulation techniques for a m x n matrix converter. IEEE Trans. Power Electron. (2017), https://doi.org/10.1109/TPEL.2016.2600034.

[13] P. Tenti, L. Malesani, L. Rossetto, Optimum control of N-input Koutputmatrix converters, IEEE Trans. Power Electron. 7 (4) (1992) 707–713.

[14] A. Iqbal, H. Abu-Rub, S.M. Ahmed, M.R. Khan, Carrier based PWM technique for a novel three-to-five phase matrix converter, in: Proc. Power Conversion Intelligent Motion PCIM Europe, Nuremberg, Germany, 2010, pp. 998–1003.

[15] S.M. Ahmed, A. Iqbal, H. Abu-Rub, M. Rizwan Khan, Carrier-based PWM technique for a novel three-to-seven phase matrix converter, in: Proc. Int. Conf. on Electrical Machines ICEM, Rome, Italy, CD-ROM paper RF 004944, 2010.

[16] S.M. Ahmed, A. Iqbal, H. Abu-Rub, J. Rodriguez, C.A. Rojas, M. Saleh, Simple carrier-based PWM technique for a three-to-nine-phase direct AC-AC converter, IEEE Trans. Ind. Electron. 58 (11) (2011) 5014–5023.

[17] A. Iqbal, S.K.M. Ahmed, H. Abu-Rub, Space vector PWM technique for a three-to-five phase matrix converter, IEEE Trans. Ind. Appl. 48 (2) (2012) 697–707.

[18] S.M. Ahmed, A. Iqbal, H. Abu-Rub, Generalized duty-ratio-based pulsewidth modulation technique for a three-to-k phase matrix converter, IEEE Trans. Ind. Electron. 58 (9) (2011) 3925–3937.

[19] Y. Li, N.-S. Choi, B.-M. Han, K.M. Kim, B. Lee, J.-H. Park, Direct duty ratio pulse width modulation method for matrix converters, Int. J Control Automat. Sys. 6 (5) (2008) 660–669.

[20] O. Ojo, M. Abreham, S. Karugaba, O.A. Komolafe, Carrier-based modulation of non-square multi-phase AC-AC matrix converters, in: Proc. IEEE Int. Symp. on Ind. Elec. ISIE, Bari, Italy, 2010, pp. 2141–2146.

[21] J. Szczepanik, T. Sienko, A new concept of application of multiphase matrix converter in power systems, in: Proc. The Int. Conf. on Computer as a Tool EUROCON, Warsaw, Poland, 2007, pp. 1535–1540.

[22] J. Szczepanik, Multiphase matrix converter for power systems application, in: Proc. Int. Symp. on Power Electronics, Electrical Drives, Automation and Motion SPEEDAM, Ischia, Italy, 2008, pp. 772–777.

[23] G. Yi, Y. Xuekui, Research on matrix converter control multiphase PMSM for all electric ship, in: Proc. Int. Conf. on Electrical and Control Engineering ICECE, Yichang, China, 2011, pp. 3120–3123.
[24] A. Beguin, A. Rufer, A. Lacaze, Poly-phased matrix converter for large synchronous generators—design of the voltage surge protection, in: Proc. 13th EPE, Barcelona, Spain, 2009, pp. 1–10. CD-ROM.
[25] A. Beguin, A. Rufer, Poly-phased matrix converter—A 27 input phases to 3 output phases experimental set-up running with hard and soft commutation, in: Proc. 14th EPE, Birmingham, 2011, pp. 1–10. CD-ROM.
[26] D. Baba, Benefits of a Multiphase Buck Converter, Analog Applications Journal, Texas Instruments Incorporated, 2012, pp. 8–13.
[27] B. Singh, S. Gairola, B.N. Singh, A. Chandra, K. Al-Haddad, Multipulse AC–DC converters for improving power quality: a review, IEEE Trans. Power Electron. 51 (3) (2008) 641–660.
[28] Y. Liu, H. Abu-Rub, B. Ge, F. Blaabjerg, O. Ellabban, P. Chiang Loh, Impedance Source Power Electronic Converters, IEEE-Wiley Press, Chichester, United Kingdom, 2016.
[29] B. Wu, High-Power Converters and AC Drives, IEEE Press, Wiley-Interscience, Piscataway, NJ, 2006.
[30] D.A. Paice, Power Electronic Converter Harmonics: Multipulse Methods for Clean Power, IEEE Press, New York, NY, 1996.
[31] F.L. Luo, H. Ye, Power Electronics Advanced conversion technologies, Taylor and Francis group, Boca Raton, FL. ISBN 978-1-4200-9429-9, 2010.
[32] A. Iqbal, S. Moinuddin, Comprehensive Relationship Between Carrier-Based PWM and Space Vector PWM In a Five-Phase VSI, IEEE Trans. Power Electron. 24 (10) (2009) 2379–2390.
[33] A. Iqbal Moinuddin, M.R. Khan, Space Vector Model of Five Phase Voltage Source Inverter, in: Proceedings of IEEE International Conference on Industrial Technology, (ICIT 2006), Mumbai, India, 2006, pp. 488–493.
[34] O. Ojo, G. Dong, Generalised discontinuous carrier-based PWM modulation scheme for multi-phase converter-machine systems, in: Proc. IEEE Industry Applications Conference, 2005. 40th IAS Annual Meeting. Conference Record of the 2005, Hong Kong, vol. 2, 2005, pp. 1374–1381.
[35] G.D. Holmes, T.A. Lipo, Pulse Width Modulation for Power Converters-Principle and Practice, IEEE Press-Series on Power Engineering, Wiley, Piscataway, NJ, 2003.
[36] V. Blasko, Analysis of a hybrid PWM based on modified space vector and triangle comparison method. IEEE Trans. Ind. Appl. 33 (3) (1997) 756–764, https://doi.org/10.1109/28.585866.
[37] A. Iqbal, E. Levi, M. Jones, S.N. Vukosavic, Generalised sinusoidal PWM with harmonic injection for multi-phase VSIs. in: Proc. IEEE Power Electron. Spec. Conf. (PESC), Jeju, Korea, 2006, pp. 2871–2877, https://doi.org/10.1109/PESC.2006.1712206.
[38] P.S.N. deSilva, J.E. Fletcher, B.W. Williams, Development of space vector modulation strategies for five-phase voltage source inverters, in: Proc. Inst. Electr. Eng. Power Electron., Mach. Drives Conf. (PEMD), Edinburgh, vol. 2, 2004, pp. 650–655, https://doi.org/10.1049/cp:20040365.
[39] J.W. Kelly, E.G. Strangas, J.M. Miller, Multiphase space vector pulse width modulation. IEEE Trans. Energy Convers. 18 (2) (2003) 259–264, https://doi.org/10.1109/TEC.2003.811725.
[40] S. Moinuddin, A. Iqbal, M.R. Khan, Space vector approach to model a seven-phase voltage source inverter, in: Proceedings of RACE, Bikaner, India, 2007, 2007, pp. 1050–1055.
[41] S. Moinuddin, A. Iqbal, Analysis of Space vector PWM for a seven-phase VSI, I-Manger J. Eng. Technol. 1 (2) (2007) 53–63 ISSN Print: 0973 – 8835, ISSN Online: 2230-7176.
[42] A. Alesina, M.G.B. Venturini, Analysis and design of optimum-amplitude nine-switch direct AC-AC converters, IEEE Trans. Power Electron. 4 (1) (1989) 101–112.
[43] M. Ali, M.R. Khan, M. Ayyub, Analysis of a three-to-five-phase matrix converter using DTFA, in: IEEE-INDICON, 2015, pp. 1–6.
[44] K. Rahman, A. Iqbal, R. Al-Ammari, Space vector model of a three-phase to five-phase AC/AC converter, in: IEEE-AFRICON, 2013.
[45] O. Abdelrahim, I.S. Member, H. Abu-rub, I.S. Member, S. M. Ahmed, Space vector PWM for a five to three matrix converter, in: IEEE-APEC, 2013, pp. 3246–3250.
[46] S.M. Ahmed, Z. Salam, H. Abu-Rub, An improved space vector modulation for a three-to-seven-phase matrix converter with reduced number of switching vectors, IEEE Trans. Ind. Electron. 62 (6) (2015) 3327–3337.
[47] A. Iqbal, K. Rahman, R. Alammari, H. Abu-Rub, Space Vector PWM for a Three-phase to Six- phase Direct AC/AC Converter, 2015. pp. 1179–1184.
[48] S.M. Ahmed, I. Member, H. Abu-rub, I. Senior, Z. Salam, Dual matrix converters based seven-phase open-end winding drive, in: IEEE-ISIE, 2014, pp. 2105–2110.
[49] S.M. Ahmed, H. Abu-rub, Z. Salam, Common-mode voltage elimination in a three-to-five-phase dual matrix converter feeding a five-phase open-end drive using space-vector modulation technique, IEEE Trans. Ind. Electron. 62 (10) (2015) 6051–6063.
[50] M.A. Sayed, A. Iqbal, Pulse width modulation technique for a three-to-five phase matrix converter with reduced commutations, IET Power Electron. 9 (3) (2016) 466–475.
[51] T.D. Nguyen, H. Lee, S. Member, Development of a three-to-five-phase indirect matrix converter with carrier-based pwm based on space-vector modulation analysis, IEEE Trans. Ind. Electron. 63 (1) (2016) 13–24.
[52] M. Chai, D. Xiao, R. Dutta, J.E. Fletcher, S. Member, Space vector PWM techniques for three-to-five-phase indirect matrix converter in the overmodulation region, IEEE Trans. Ind. Electron. 63 (1) (2016) 550–561.
[53] Xunwei Zhou, Pit-Leong Wong, Peng Xu, Fred C. Lee, Alex Q. Huang, Investigation of candidate VRM topologies for future microprocessors, IEEE Trans. Power Electron. 15 (6) (Nov 2000) 1172–1182.
[54] X. Zhang, A.Q. Huang, Investigation of VRM controllers, in: Proceedings of 16th International Symposium on Power Semiconductor Devices & ICs, 2004, pp. 51–54.
[55] N. Jantharamin, L. Zhang, Analysis of multiphase interleaved converter by using state-space averaging technique, in: ECTI-CON, 2009, pp. 288–291.
[56] A.C. Schittler, D. Pappis, C. Rech, A. Campos, M.A. Dalla Costa, Generalized state-space model for the interleaved buck converter, in: COBEP'11, 2011, pp. 451–457.
[57] H. Nguyen, Design, Analysis and Implementation of Multiphase Synchronous Buck DC-DC Converter for Transportable Processor, (Master of science thesis), Virginia Tech, 2004. April.
[58] D. Garinto, A novel multiphase multi-interleaving buck converters for future microprocessors, in: 12th International Power Electronics and Motion Control Conference, PEMC, 2006, pp. 82–87. Aug–Sep 2006.

[59] P.L. Wong, Performance Improvements of Multi-Channel Interleaving Voltage Regulator Modules with Integrated Coupling Inductors, (Ph.D. dissertation), Virginia Tech, 2001. March.
[60] P. Xu, J. Wei, F.C. Lee, Multiphase coupled-buck converter-a novel high efficient 12 V voltage regulator module, IEEE Trans. Power Electron. 18 (2003) 74–82.
[61] T. Soong, P. Lehn, A transformerless high boost dc-dc converter for use in medium / high voltage applications, in: IECON, 2012, pp. 174–179.
[62] C. Wang, Investigation on Interleaved Boost Converters and Applications, (Ph.D. dissertation), Virginia Tech, 2009. July.
[63] Peng Xu, Multiphase Voltage Regulator Modules with Magnetic Integration to Power Microprocessors (Ph.D. thesis), Virginia Polytechnic Institute and State University, 2002.

Further Reading

[1] Y. Panov, M.M. Jovanovic, Design considerations for 12-V/1.5-V, 50-A voltage regulator modules, IEEE Trans. Power Electron. 16 (6) (2001) 776–783.

16

Power Factor Correction Circuits

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16.1 Introduction

Today, there is an increased proliferation of power electronics converters, mainly in industrial and domestic applications due to their high inherent flexibility for ensuring the power conversion management at all power levels. Unfortunately, these converters are considered to be the major sources of power quality degradation in terms of current and voltage waveform distortion and power factor degradation. Indeed, power electronics converter is characterized by a nonlinear behavior which contributes to the pollution of the main utility power supply. On the other side, since ac electric energy is the most convenient form of energy to be generated, transmitted, and distributed through the main ac power systems, the stage of power conversion is primordial to ensure the required converted forms to the consumers in industry and residence applications. Therefore, the power electronics converter is unavoidable to be as an essential part of different power supply and a flexible control device in many applications. During the last years, large electricity consumers such as electrochemical and electrometallurgical industries applied capacitors as static var compensator (SVC) to their systems to ensure an effective cost solution by minimizing the demanded charges from utility companies and to ensure the dynamic voltage stabilization support, the efficiency, and the required reliability of the supply voltages. Indeed, this solution was highly recommended due to its low-cost, its high reliability, and its simple and easy integration within the existing and new infrastructures without the necessity of adding other new network extensions. As these capacitors present low impedance in the system, they contribute remarkably in drawing harmonic currents from the power supply. It is well evident that due to the nonzero system impedance along the lines, the circulating of the harmonic currents through these lines will create distorted drop voltages that will propagate. Consequently, the voltages at the points of different users' connection will be contaminated. The contaminative harmonics can decline power quality and affect the system performance in several ways [1–15]:

(a) The line *rms* current harmonics do not deliver any real power in watts to the load that is supplied by a sine waveform voltage, resulting in inefficient use of equipment capacity (i.e., low-power factor).
(b) Harmonics will increase conductor loss and iron loss in transformers of the transmission system. Therefore, the thermal problems will be increased, and the systems transmission system efficiency will be decreased.
(c) Beside the current unbalance in three-phase system, the odd harmonics are extremely harmful, contributing to the overload of the neutral conductor.
(d) The propagation of harmonics within the power system may cause oscillations that will absolutely affect the stability of system operation.
(e) High peak harmonic currents may cause automatic relay protection devices to mistrigger.

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(f) Harmonics could cause other problems such as electromagnetic interference to interrupt communication, degrading reliability of electric equipment, increasing product defective ratio, insulation failure, and audible noise.

Perhaps the greatest impact of harmonic pollution appeared in the early 1970s when SVCs were extensively used for electric arc furnaces, metal rolling mills, and other high-power appliances. The harmonic currents produced by partial conduction of SVC are odd order, which are especially harmful to three-phase power system, especially for the star connection; if the star connection point is connected to the neutral line, this line will be overloaded; otherwise, this point will be supporting nonzero voltage. Harmonics can affect operations of other devices that are connected to the same system and, in some situation, the operations of themselves that generate the harmonics.

The ever deteriorated supply environment did not become a major concern until the early 1980s when the first technical standard IEEE519-1981 with respect to harmonic control at point of common coupling (PCC) was issued [16]. The significance of issuing this standard was not only that it provided the technical reference for design engineers and manufactures but also that it opened the door of research area of harmonic reduction and power factor correction (PFC). These two main objectives are really meaning the input current shaping (ICS), although most researchers refer their work as PFC. This is why the term "PFC" is used through the whole chapter.

Stimulated by the harmonic control regulation, researchers and industry users started to develop low-cost devices and power electronic systems to reduce harmonics since it is neither economical nor necessary to eliminate the harmonics.

Research on harmonic reduction and PFC has become intensified in the early 1990s. With the rapid development in power semiconductor devices, power electronic systems have matured and expanded to new and wide application range from residential, commercial, and aerospace to military and others. Power electronic interfaces, such as switch-mode power supplies (SMPS), are now clearly superior over the traditional linear power supplies, resulting in more and more interfaces switched into power systems. While the SMPSs are highly efficient, but because of their nonlinear behavior, they draw distorted current from the line, resulting in high total harmonic distortion (THD) and low power factor (PF). To achieve a smaller output voltage ripple, practical SMPSs use a large electrolytic capacitor in the output side of the single-phase rectifier. Since the rectifier diodes conduct only when the line voltage is higher than the capacitor voltage, the power supply draws high *rms* pulsating line current. As a result, high THD and poor PF (usually less than 0.67) are present in such power systems [1,7,8,17–19].

Even though each device, individually, does not present much serious problem with the harmonic current, utility power supply condition could be deteriorated by the massive use of such systems. In recent years, declining power quality has become an important issue and continues to be recognized by government regulatory agencies. With the introduction of compulsory and more stringent technical standard such as IEC1000-3-2, more and more researchers from both industries and universities are focusing in the area of harmonic reduction and PFC, resulting in numerous circuit topologies and control strategies. Generally, the solution for harmonic reduction and PFC are classified into passive approach and active approach. The passive approach offers the advantages of high reliability, high-power-handling capability, and easy to design and maintain. However, the operation of passive compensation system is strongly dependent on the power system and does not achieve high PF. While the passive approach can be still the best choice in many high-power applications, the active approach dominates the low to medium power applications due to their extraordinary performance (PF and efficiency approach to 100%), regulation capabilities, and high density. With the power-handling capability of power semiconductor devices being extended to megawatts, the active power electronic systems tend to replace most of the passive power processing devices [1,3–5].

Actually, harmonics reduction and PFC techniques to improve the power quality within the network power supply are attracting very important researches in different applications for the lower power level, the medium power level, and the high-power level. Indeed power supply industries are undergoing the change of adopting more and more PFC techniques in all off-line power supplies. This chapter presents an overview of various active harmonic reduction and PFC techniques in the open literature up to date. The primary objective of writing this chapter is to give a brief introduction of these techniques and provide references for future researchers in this area. The discussion here includes definition of THD and PF, commonly used control strategies, and various types of converter topologies. Finally, the possible future research trends are stressed in the summary section.

16.2 Definition of PF and THD

Power factor is a very important parameter in power electronics because it gives a measure of how effective the real power utilization in the system is. It also represents a measure of distortion of the line voltage and the line current and phase shift between them. Referring to Fig. 16.1A, the input PF at terminals $a-a'$ is defined as the ratio of the average of the instantaneous power or the real instantaneous power and the apparent power measured at terminals $a-a'$ as described in Eq. (16.1) [1,16,18,19]:

$$\text{Power Factor(PF)} = \frac{\text{Real Power (Average)}}{\text{Apparent Power}} \tag{16.1}$$

where the apparent power is defined as the product of *rms* values of instantaneous voltage $v_s(t)$ and instantaneous current

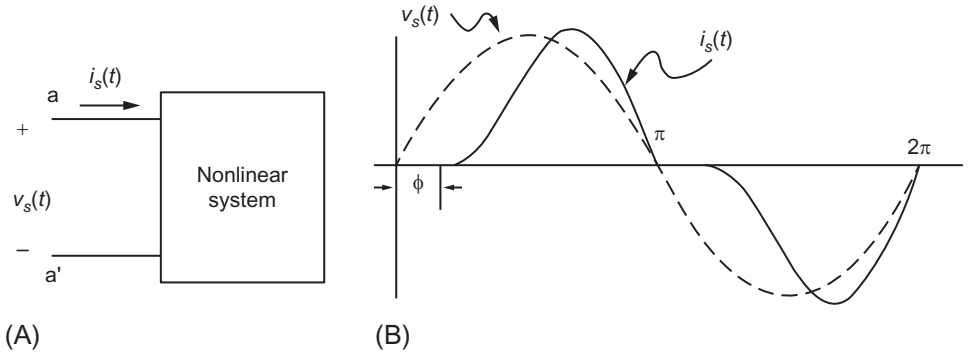


FIG. 16.1 Nonlinear load draws distorted line current.

$i_s(t)$. It is well-known that if the load is linear, it draws purely sinusoidal current under sinusoidal voltage. In this case, the PF is only determined by the phase shift between $v_s(t)$ and $i_s(t)$. Hence, Eq. (16.1) becomes

$$\mathrm{PF} = \frac{I_{s,rms} V_{s,rms} \cos\theta}{I_{s,rms} V_{s,rms}} = \cos\theta \tag{16.2}$$

where $I_{s,rms}$ and $V_{s,rms}$ are *rms* values of the current drawn by the load and the voltage applied to the load, respectively, and θ is the phase shift between instantaneous drawn current and instantaneous applied voltage. Hence, if the power system delivers a pure sine waveform voltage and the load is linear, the PF is simply equal to the cosine of the phase shift angle between the instantaneous current and instantaneous voltage. However, in power electronics system, due to the nonlinear behavior of active switching power devices, Eq. (16.2) is not valid anymore, and the phase-angle representation alone is not enough for the calculation of the PF which becomes more delicate. Fig. 16.1B shows a typical distorted current drawn from the pure sinusoidal power source. It is obvious that the calculation of the PF for distorted waveforms of the current or/and voltage is more complex when compared with the sinusoidal current and voltage waveforms. If both line voltage and line current are distorted, in this case Eqs. (16.3) and (16.4) give the Fourier expansion representations for the instantaneous drawn current and instantaneous power source voltage, respectively [1]:

$$\begin{aligned} i_s(t) &= I_{\mathrm{DC}} + \sum_{n=1}^{\infty} I_{sn} \sin(n\omega t + \theta_{\mathrm{in}}) \\ &= I_{\mathrm{DC}} + I_{s1} \sin(\omega t + \theta_{i1}) + \sum_{n=2}^{\infty} I_{sn} \sin(n\omega t + \theta_{\mathrm{in}}) \end{aligned} \tag{16.3}$$

$$\begin{aligned} v_s(t) &= V_{\mathrm{DC}} + \sum_{n=1}^{\infty} V_{sn} \sin(n\omega t + \theta_{vn}) \\ &= V_{\mathrm{DC}} + V_{s1} \sin(\omega t + \theta_{v1}) + \sum_{n=2}^{\infty} V_{sn} \sin(n\omega t + \theta_{vn}) \end{aligned} \tag{16.4}$$

Practically, the two DC (average value) of the instantaneous current and voltage that are expected to be seen from the power supply side are equal to zero due to the symmetry of the positive and negative parts of the voltage and current during one period; therefore, $I_{\mathrm{DC}} = V_{\mathrm{DC}} = 0$. Applying the definition of PF given in Eq. (16.1) to the distorted current and voltage waveforms of Eqs. (16.3) and (16.4), PF may be expressed as:

$$\mathrm{PF} = \frac{\sum_{n=1}^{\infty} I_{sn,rms} V_{sn,rms} \cos\theta_n}{I_{s,rms} V_{s,rms}} = \frac{\sum_{n=1}^{\infty} I_{sn,rms} V_{sn,rms} \cos\theta_n}{\sqrt{\sum_{n=1}^{\infty} I_{sn,rms}^2 \sum_{n=1}^{\infty} V_{sn,rms}^2}} \tag{16.5}$$

where $V_{sn,rms}$ and $I_{sn,rms}$ are the *rms* values of the nth harmonic voltage and current, respectively, and θ_n is the phase shift between the instantaneous voltage and current corresponding to the nth harmonic $(\theta_n = \theta_{in} - \theta_{vn})$.

Since most of power electronic systems draw their input voltage from a pure sine waveform power supply voltage $v_s(t)$, the above expression can be significantly simplified by assuming that the power supply voltage has a pure sine waveform and the distortion is only included in the instantaneous current $i_s(t)$, that is,

$$v_s(t) = V_s \sin\omega t \tag{16.6}$$

$$i_s(t) = \mathrm{distorted(nonsinusoidal)} \tag{16.7}$$

Then, it can be shown that the PF can be expressed as

$$\mathrm{PF} = \frac{I_{s1,rms}}{I_{s,rms}} \cos\theta_1 = k_{\mathrm{dist}} \times k_{\mathrm{disp}} \tag{16.8}$$

where

θ_1: the phase-angle between the voltage $v_s(t)$ and the fundamental component of $i_s(t)$,
$I_{s1,rms}$: *rms* value of the fundamental component in line current,
$I_{s,rms}$: total *rms* value of line current,
$k_{\mathrm{dist}} = I_{s1,rms}/I_{s,rms}$: distortion factor,
$k_{\mathrm{disp}} = \cos\theta_1$: displacement factor.

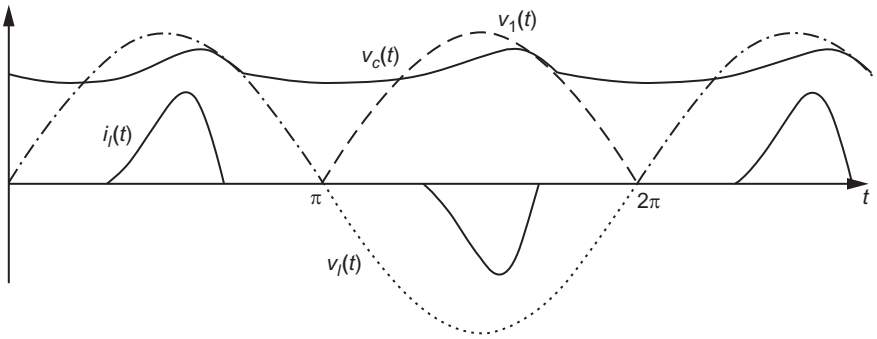


FIG. 16.2 Typical waveforms in a poor PF system.

Another important parameter which measures the percentage of current distortion is known as the current total harmonic distortion (THD_i), which is defined as follows:

$$THD_i = \sqrt{\frac{\sum_{n=2}^{\infty} I_{sn,rms}^2}{I_{s1,rms}^2}} = \sqrt{\frac{1}{k_{dist}^2} - 1} \tag{16.9}$$

Conventionally, SMPSs use capacitive rectifiers in front of the ac line that results in the capacitor voltage v_c and high *rms* pulsating line current $i_l(t)$ as shown in Fig. 16.2, when $v_l(t)$ is the line voltage. The typical input current harmonic distortion THD_i for this kind of rectification is usually in the range of 55%–65%, and the PF is about 0.65 [20,21]. It can be said also that the actual current wave shape and the resulting harmonics depend on the line impedance. This input current character creates several problems within the distribution network and consequently affecting the other electric apparatus in the vicinity of the rectifier. However, some solution has been proposed to overcome these drawbacks especially for high-power. The present chapter is focusing mainly on the study of the improvement of the current shape and PFC related to line current of single-phase rectifier followed by DC-DC converter that are mainly used for limited power level.

As we can see from Eqs. (16.8) and (16.9), PF and THD are related to distortion and displacement factors. Therefore, improvement in PF, that is, PFC, also implies harmonic reduction, especially the low order harmonics [1].

16.3 Power Factor Correction

16.3.1 Energy Balance in PFC Circuits

Fig. 16.3 shows a diagram of an AC-DC PFC unit. Let $v_i(t)$ and $i_l(t)$ be the line voltage (the power source voltage) and line current (the drawn current from the power source), respectively. For an ideal PFC unit (PF = 1), we assume

$$v_l(t) = V_{lm} \sin \omega_l t \tag{16.10a}$$

$$i_l(t) = I_{lm} \sin \omega_l t \tag{16.10b}$$

where V_{lm} and I_{lm} are amplitudes of line voltage and line current, respectively, and ω_l is the angular line frequency. The instantaneous input power is given by

$$p_{in}(t) = v_l(t) \cdot i_l(t) = V_{lm} I_{lm} \sin^2 \omega_l t = P_{in}(1 - \cos 2\omega_l t) \tag{16.11}$$

where $P_{in} = V_{in} \cdot I_{in}/2$ is constant value that is presenting the average of the instantaneous input power $p_{in}(t)$. It is important to clarify that only this part of power is contributing for the production of the effective energy that can be used by the load;

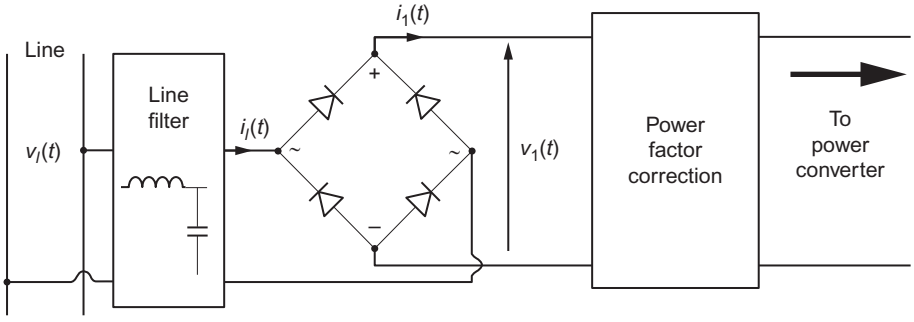


FIG. 16.3 Block diagram of ac-dc PFC unit.

therefore, it is often called the real power. On the other side, $p_{in}(t)$ possesses also an alternative component with frequency $2\omega_l$ as shown in Fig. 16.4 (i.e., 100 or 120 Hz, following the used power supply 50 or 60 Hz, respectively). Therefore, the operation principle of a PFC circuit is to process the input power in a certain way that it stores the excessive input energy when $p_{in}(t)$ is greater than $P_{in}(=P_o)$ and releases the stored energy when $p_{in}(t)$ is less than $P_{in}(=P_o)$, where a compensation is achieved between the stored energy and the released energy in these two stages (Fig. 16.4). The average value between these two terms of energy is equal to zero. We can estimate the instantaneous excessive power as

$$p_{ex}(t) = p_{in}(t) - P_0 = -P_0 \cos 2\omega_l t \tag{16.12}$$

Hence, the instantaneous excessive input energy, $w_{ex}(t)$, is given by

$$w_{ex}(t) = \int_{\frac{T_l}{8}}^{t} p_{ex}(t)dt = \frac{P_0}{2\omega_l}(1 - \sin 2\omega_l t) \tag{16.13}$$

At $t = T_l/8$ and $t = 5T_l/8$, the excessive input energy is null, and at $t = 3T_l/8$, the excessive input energy reaches the peak value

$$w_{ex,\max} = \frac{P_0}{2\omega_l}\left(1 - \sin\frac{3\pi}{2}\right) = \frac{P_0}{\omega_l} \tag{16.14}$$

To achieve this concept of the dynamic behavior of the excessive input energy variation, the PFC circuit has to ensure this both functionality of storing the excessive energy and realizing the stored excessive energy by integrating the basic dynamic components (inductor and capacitor) in the PFC circuit. Indeed, in most of the PFC circuits that have been used in such applications, an input inductor is used to carry the line current. To obtain a unity PF, it is well obvious that the inductor current (or averaged inductor current in switch-mode PFC circuit) must be a pure sinusoidal and in phase with the line voltage. The energy stored in the inductor ($1/2Li_L^2(t)$) cannot completely match the change of the excessive energy as shown in Fig. 16.4. Therefore, to maintain the output power constant, another energy storage component (usually the output capacitor) is needed [1].

16.3.2 Passive Power Factor Corrector

Because of their high reliability and high-power-handling capability, passive power factor correctors are normally used in

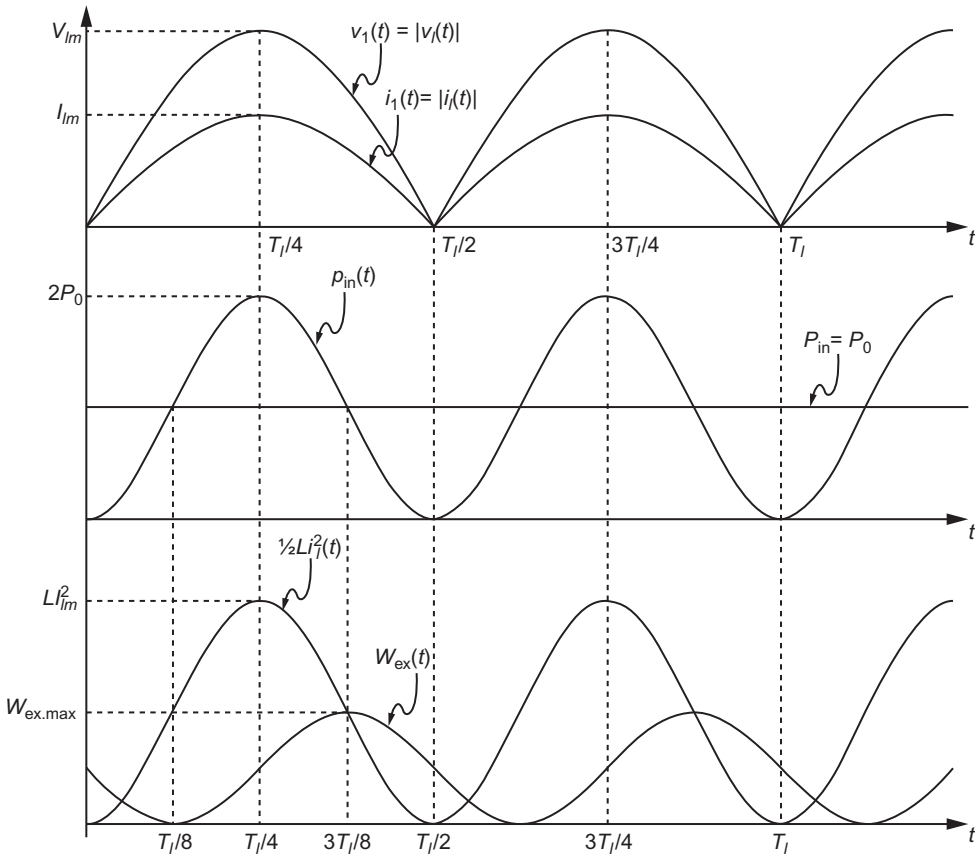


FIG. 16.4 Energy balance in PF corrector.

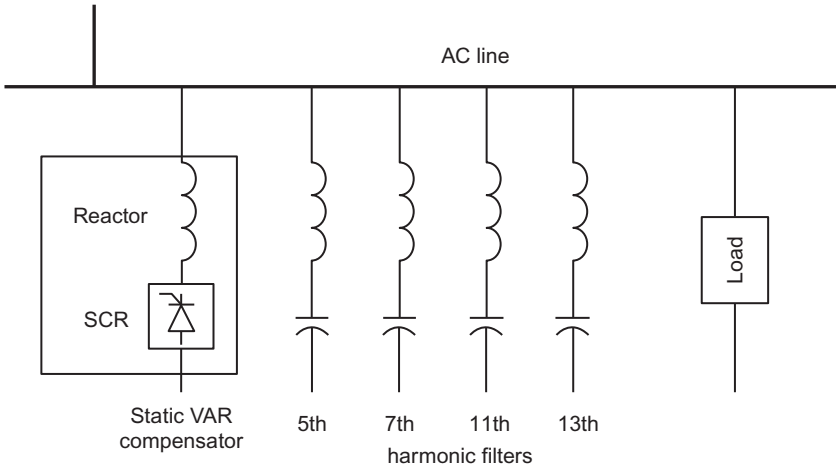


FIG. 16.5 Series-tuned *LC* harmonic filter PF corrector.

high-power-line applications. Series-tuned *LC* harmonic filter is commonly used for heavy plant loads such as arc furnaces, metal rolling mills, and electric locomotives [1]. Fig. 16.5 shows a connection diagram of a selective low frequency harmonic filter together with line frequency switched reactor SVC. By tuning the filter branches to odd harmonic of low frequencies, the filter shunts the harmonic currents. Since each branch presents capacitive at line frequency, the filter also provides capacitive SVC for the system, whereas the integration of the thyristor-controlled reactor (TCR) in parallel with this selected group of low frequency filters keeps an optimized static var compensation for the system so that higher PF can be maintained.

The design of the tuned filter PF corrector is particularly difficult because of the uncertainty of the system impedance and the characteristics of the harmonic sources. Besides, this method involves too many expensive components and takes huge space in comparison with the active PFC method.

For the applications where the power level is less than 10 kW, the tuned filter PF corrector may not be a better choice. The most common off-line passive PF corrector is the inductive-input filter, shown in Fig. 16.6. This filter can operate either in the continuous conduction mode (CCM), in which the rectifier bridge is always conducting, or in the discontinuous conduction mode (DCM) where the rectifier is off during a portion of the line period [22,23]. A conduction parameter K_l is defined in the literature based on the values of the filter parameters, the inductance L, the assumed resistor R, and the line input frequency ω_l as follows:

$$K_l = \frac{\omega_l L}{\pi R} = \frac{2L}{RT} \tag{16.15}$$

The assumed resistor represents the ratio between the average value of the voltage and the average value of the current at the output side of the filter.

For operation in CCM, the PF is defined as [22,23]:

$$\mathrm{PF} = \frac{2\sqrt{2}}{\pi} \frac{1}{\sqrt{1 + \left(\frac{5}{24} - \frac{2}{\pi^2}\right)/K_l^2}} = \frac{0.9}{\sqrt{1 + 0.075/K_l^2}} \tag{16.16}$$

Depending on the filter inductance, this circuit can achieve a maximum PF of 90%, which is corresponding to the theoretical value of $K_l = \infty$. On the other side, it was found in [22,23] that

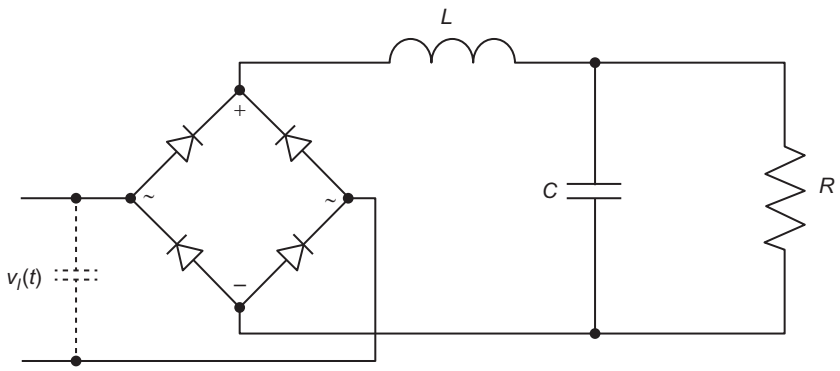


FIG. 16.6 Inductive-input PF corrector.

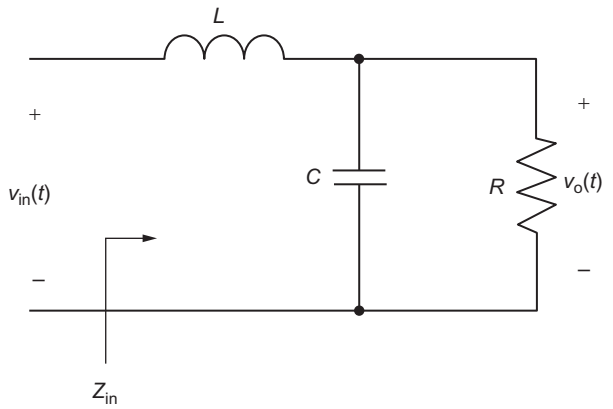


FIG. 16.7 Low-pass inductive filter.

the critical value of $K_l(K_{lcrit})$ that makes the minimum of the inductor current reach the zero value is $K_{lcrit} = 0.1053$; this value makes the PF to fall to the value of 73.2%. In case where $K \prec K_{lcrit}$, the current passes to the DCM [23].

The PF corrector is simply a low-pass inductive filter as shown in Fig. 16.7, whose transfer function and input impedance are given by [1]

$$H_0(s) = \frac{v_0(s)}{v_{in}(s)} = \frac{1}{s^2LC + sL/R + 1} \tag{16.17}$$

$$Z_{in0}(s) = \frac{v_{in}(s)}{i_{in}(s)} = R\frac{s^2LC + sL/R + 1}{sRC + 1} \tag{16.18}$$

This kind of filter shown in Fig. 16.6 is characterized by the following main advantages:

(a) It has a simple structure.
(b) It is reliable.
(c) The cost is very low because only a filter is required.
(d) The high-frequency switching losses are absent, and it is not sensitive to noises and surges.
(e) The equipments used in this circuit do not generate high-frequency EMI.

The above equations show that the unavoidable phase displacement is incurred in the inductive filter corrector. Because the filter frequency of operation is low (line frequency), large value inductor and capacitor have to be used. As a result, the following main disadvantages are presented in the most passive PF correctors:

(a) Only less than 0.9 PF can be achieved.
(b) The output voltage cannot be regulated under uncontrolled rectifier.
(c) The efficiency is low.
(d) THD is high.
(e) It cannot provide satisfactory results for wide load range.
(f) They are heavy and bulky, because, for achieving a better power factor, the size of the filter increases.
(g) The output is unregulated.
(h) The dynamic response is poor due to the time lag associated with the passive elements.
(i) They are sensitive to circuit parameters.
(j) Although by filtering the harmonics that can be filtered out, the fundamental component may get phase-shifted, thus reducing the power factor.
(k) The shape of input current is dependent upon what kind of load is connected.
(l) Optimization of the design is difficult.

16.3.3 Basic Circuit Topologies of Active Power Factor Correctors

In recent years, using the switched-mode topologies, many circuits and control methods are developed up to date to comply with certain standard (such as IEEE Std 519 and IEC1000-3-2). To achieve this, high-frequency switching techniques have been used to shape the input current waveform successfully [1]. Basically, the active PF correctors that are used to accomplish the PFC function in single-phase power supply are based on the well-known basic converter topologies or their developed versions.

16.3.3.1 The Buck Corrector

Fig. 16.8A shows the buck PF corrector. By using PWM switch modeling technique [24], the circuit topology can be modeled by the equivalent circuit shown in Fig. 16.8B. It should be pointed out that the circuit model is a large signal model; therefore, analysis of PF performance based on this model is valid. It can be shown that the transfer function and input impedance are given by [1]

$$H(s) = \frac{v_0(s)}{v_{in}(s)} = \frac{d}{s^2LC + sL/R + 1} = d \cdot H_0(s) \tag{16.19}$$

$$Z_{in}(s) = \frac{v_{in}(s)}{i_{in}(s)} = \frac{R}{d^2}\frac{s^2LC + sL/R + 1}{sRC + 1} = \frac{Z_{in0}(s)}{d^2} \tag{16.20}$$

where d is the duty ratio of the switching signal.

Notice that Eqs. (16.18) and (16.19) are different from Eqs. (16.16) and (16.17), in that they have introduced the control variable d. By properly controlling the switching duty ratio to modulate the input impedance and the transfer function, a pure resistive input impedance and constant output voltage can be approached [1]. Thereby, unity PF and output regulation can both be achieved. These control techniques will be discussed in the next section.

Comparing with the other type of high-frequency PFC circuits, the buck corrector offers inrush-current limiting, overload or short-circuit protection, and overvoltage protection for the converter due to the existence of the power switch in front of the line. Another advantage is that the output voltage is lower than the peak of the line voltage, which is usually the

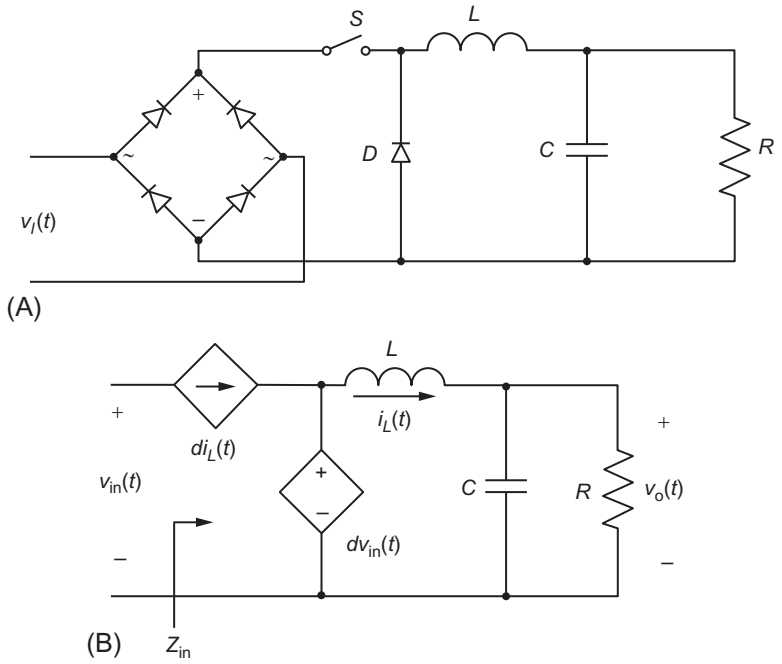


FIG. 16.8 (A) Buck corrector and (B) PWM switch model for buck corrector.

case normally desired. The drawbacks of using buck corrector may be summarized as follows [1]:

(a) When the output voltage is higher than the line voltage, the converter draws no current from the line, resulting in significant line current distortion near the zero-across of the line voltage.
(b) The input current is discontinuous, leading to high differential mode EMI.
(c) The current stress on the power switch is high.
(d) The power switch needs a floating drive.

16.3.3.2 The Boost Corrector

The boost corrector and its equivalent PWM switch modeling circuit are shown in Fig. 16.9A and B. Its transfer function and input impedance are given by [1]

$$H(s) = \frac{1/d'}{s^2\left(L/d'^2\right)C + s\left(L/d'^2\right)/R + 1} \tag{16.21}$$

$$Z_{in}(s) = d'^2 R \frac{s^2\left(L/d'^2\right)C + s\left(L/d'^2\right)/R + 1}{sRC + 1} \tag{16.22}$$

where $d' = 1 - d$.

Unlike in the buck case, it is interesting to note that in the boost case, the equivalent inductance is controlled by the switching duty ratio. Consequently, both the magnitude and the phase of the impedance, and both the dc gain and the pools of the transfer function are modulated by the duty ratio, which implies a tight control of the input current and the output voltage. Other advantages of boost corrector include less EMI and lower switch current and grounded drive. The shortcomings with the boost corrector are summarized as [1]

(a) the output voltage must be higher than the peak of line voltage;
(b) inrush-current limiting, overload, and overvoltage protections are not available.

16.3.3.3 The Buck-Boost Corrector

The buck-boost corrector and its equivalent circuit are shown in Fig. 16.10A and B. The expressions for transfer function and input impedance are [1]

$$H(s) = \frac{d/d'}{s^2\left(L/d'^2\right)C + s\left(L/d'^2\right)/R + 1} \tag{16.23}$$

$$Z_{in}(s) = \left(\frac{d'}{d}\right)^2 R \frac{s^2\left(L/d'^2\right)C + s\left(L/d'^2\right)/R + 1}{sRC + 1} \tag{16.24}$$

The buck-boost corrector combines some advantages of the buck corrector and the boost corrector. Like a buck corrector, it can provide circuit protections and step-down output voltage, and like a boost corrector its input current waveform and output voltage can be tightly controlled. However, the buck-boost corrector has the following disadvantages [1]:

(a) The input current is discontinued by the power switch, resulting in high differential mode EMI.
(b) The current stress on the power switch is high.
(c) The power switch needs a floating drive.
(d) The polarity of output voltage is reversed.

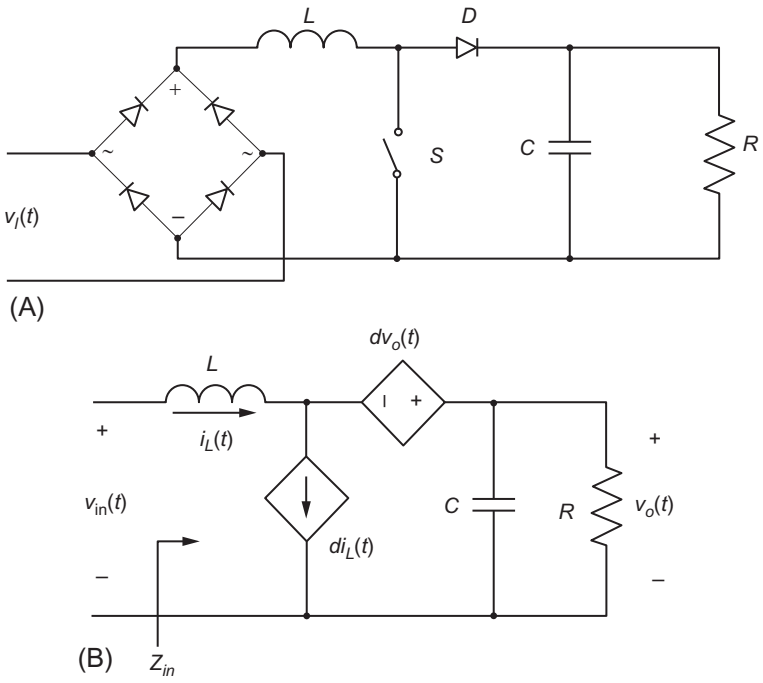


FIG. 16.9 (A) Boost corrector and (B) PWM switch model of boost corrector.

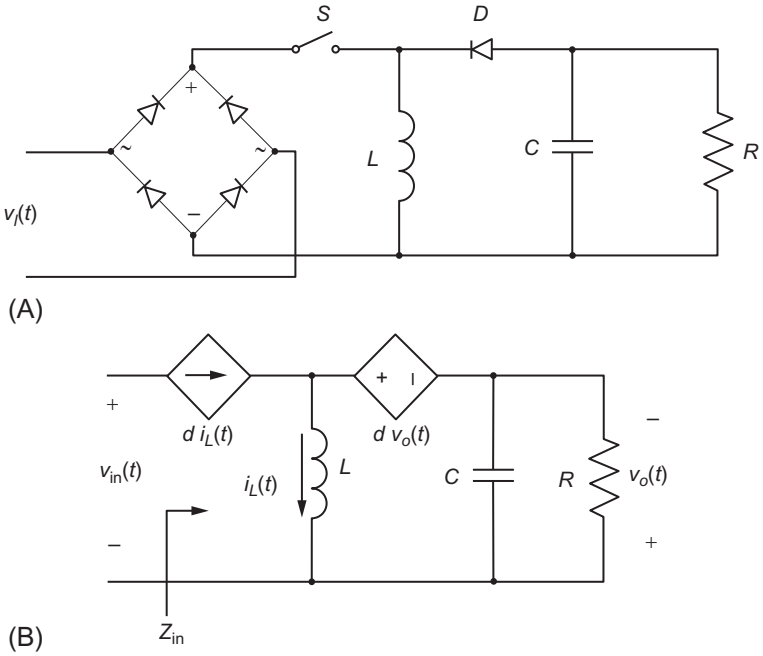


FIG. 16.10 (A) Buck-boost corrector and (B) PWM switch model of buck-boost corrector.

16.3.3.4 The Cuk, Sepic, and Zeta Correctors

Unlike the previous converters, the Cuk, Sepic, and Zeta converters are fourth-order switching-mode circuits. Their circuit topologies for PFC are shown in Fig. 16.11A–C, respectively. Because there are four energy storage components available to handle the energy balancing involved in PFC, second-harmonic output voltage ripples of these correctors are smaller when compared with the second-order buck, boost, and buck-boost topologies. These PF correctors are also able to provide overload protection. However, the increased count of components and current stress are undesired [1].

16.3.3.5 Flyback Corrector

The flyback corrector allows to the input current to be shaped into a rectified sine wave, which is in phase with the input voltage, thus achieving a high PF and low harmonics content. Indeed, it is one of the most used active PFC converters, which has been widely used as an isolated front-stage PFC converter [25,26] and as a single-stage PFC [27–32]. Indeed, this topology presents many advantages such as isolation between input and output, low-cost, and simple structure. However, the large voltage stress on the primary switch and the large current stress through the output diode have limited its application to low-power level Fig. 16.12 [33–39].

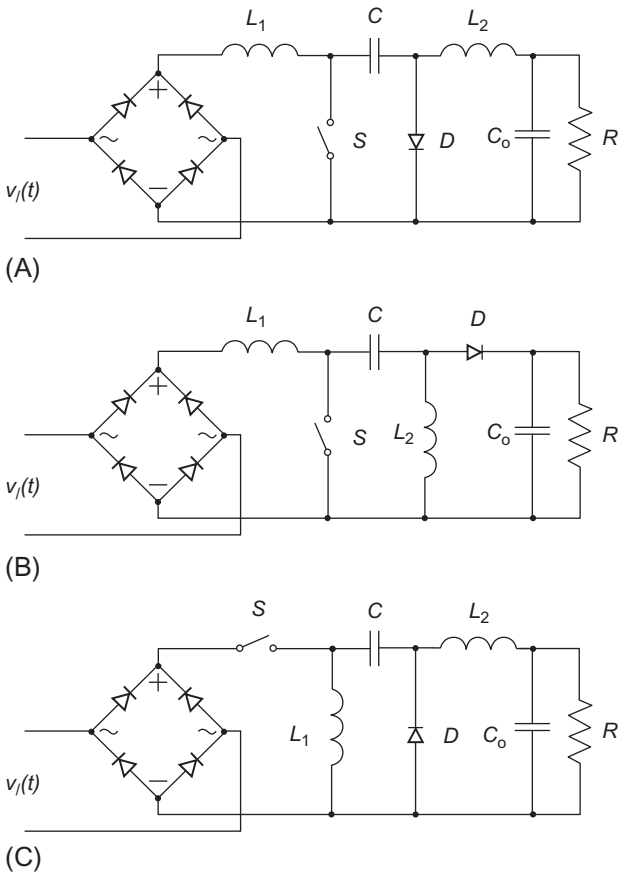


FIG. 16.11 Fourth-order corrector: (A) Cuk corrector, (B) Sepic corrector, and (C) Zeta corrector.

The flyback PFC topology can operate under the three modes: continuous current mode (CCM), discontinuous current mode (DCM), and critical conduction mode (CRM). The operating mode is chosen upon the behavior of the freewheeling diode at the isolating transformer secondary side when the main switch "S" is turned off in one switch period.

The CCM operation of the flyback PFC converter requires two control loops. The first control loop is used to control the current to ensure the line current wave shape and a zero shift phase between the line voltage and line current, consequently a unity PF, can be obtained. The second control loop is used to control the output voltage to achieve its regulation. For DCM and CRM flyback PFC converters, only voltage control loop is required, which allows to obtained circuits that are simpler than that of CCM flyback PFC converter, this makes the DCM and CRM flyback PFC converters to be more widely used [35–42].

16.3.3.6 Forward, Forward-Flyback Correctors

The forward converter is presenting the simplest isolated buck-type converter, which has been widely applied for DC/DC conversions. The use of the basic topology and the practical topology shown in Fig. 16.13A and B of the forward converter for PFC applications include several disadvantages: (1) The typical single-ended forward converter requires a third additional auxiliary winding to ensure the transformer energy reset demagnetization [43], (2) it has the same drawbacks and limits of the basic topology of the buck PFC converter [43–45], and (3) as shown in Fig. 16.13A, when the output voltage V_0 is greater than the input rectified voltage V_{in}, dead zones appear in the input current waveforms i_{in}, that can degrade the PF and contribute to the increase of the harmonics content. These main disadvantages make the basic topology forward PFC difficult to be used in PFC applications. However, many works have presented improved topologies of this kind of converter to fulfill the requirement of decreased input current harmonics distortion and higher PF. One of such topologies that was proposed to overcome the main disadvantages of the basic

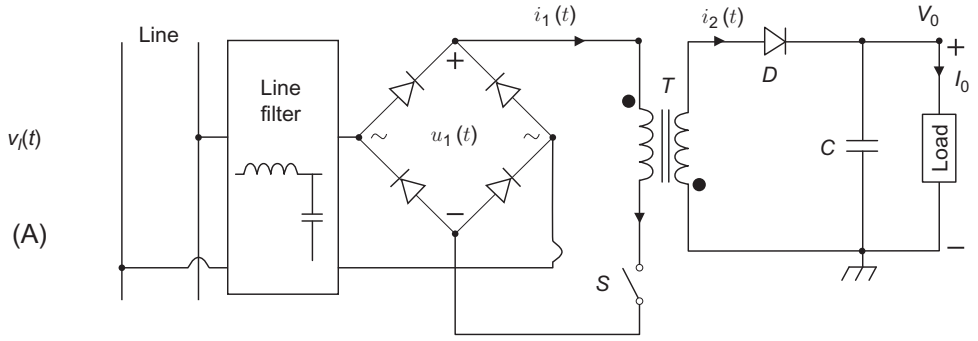


FIG. 16.12 Flyback corrector.

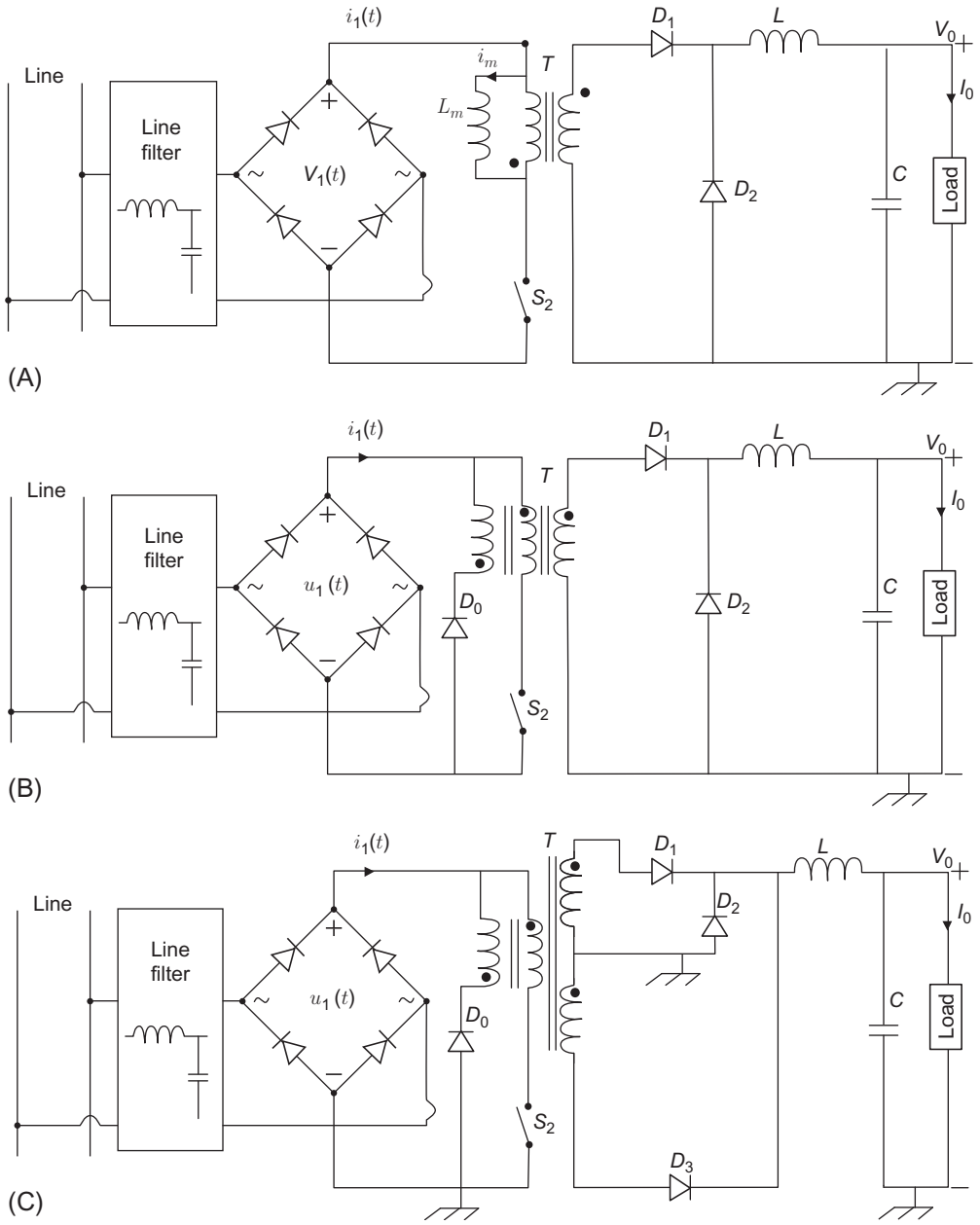


FIG. 16.13 Forward converter topology, (A) forward converter basic topology, (B) forward converter practical topology, and (C) forward-flyback converter topology.

topology of the forward converter is the forward-flyback PFC topology that combines the basic forward topology and the basic flyback topology, where only one common switch and one common transfer are used as shown in Fig. 16.13C [46–50]. In this topology, when the input voltage is not large enough to enable the forward operation, the flyback converter contributes to the power transfer. The main advantages of the proposed topology are the following [24,46–50]:

1. The dead zones existing in the convention forward PFC topology are eliminated.
2. The transformer is reset during the flyback converter operation.
3. The additional reset winding for the forward converter is no more needed.

16.3.3.7 A Single-Stage Quasi *Z*-Source Corrector

The quasi-Z-Source (qZS) topology and their different improved topologies have been introduced recently in several DC-DC converter applications [51–53]. The single-stage qZS converter topology was proposed to ensure the PFC converter in single-phase application [54,55]. This topology, even it is different from the other topologies DC-DC converter topologies previously presented, but it has several features such as low-voltage stress on switches; lossless clamping, without using

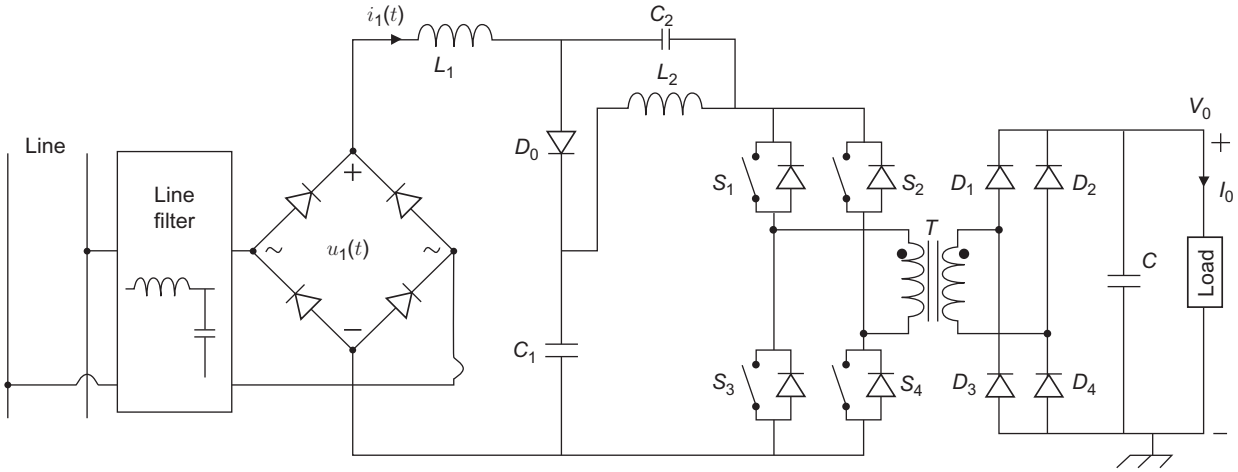


FIG. 16.14 A single-stage quasi-Z-source corrector.

auxiliary switch; and duty-cycle-control scheme and improved efficiency. The circuit of this PFC converter is shown in Fig. 16.14. The single-phase power supply provides the line input to the load via the qZS, the full-bridge diode rectifier, and the transformer and the second full-bridge diode rectifier. The same control strategies that are used for the other DC-DC converter topologies are used for these topologies with more or less modifications, where the main aim is to shape the input line current into a sinusoidal wave and in phase with the input line voltage to obtain a unity PF.

16.3.4 System Configurations of PFC Power Supply

The most common configurations of AC-DC power supply with PFC are two-stage scheme and one-stage (or single-stage) scheme. In two-stage scheme as shown in Fig. 16.15A, a non-isolated PFC AC-DC converter is connected to the line to create an intermediate DC bus. This DC bus voltage is usually full of second-harmonic ripple and which is followed by a cascaded DC-DC converter to provide electric isolation and tight voltage regulation. The advantage of two-stage structure PFC circuits is that the two power stages can be controlled separately, and thus, it makes it possible to have both converters optimized. The drawbacks of this scheme are lower efficiency due to twice processing of the input power, two control systems which leads to complex control circuits, higher cost, bulky due to the used intermediary circuits between the two stages, and low reliability. Although the two-stage scheme approach is commonly adopted in several industrial applications, it received limited attention by the common research, since the input stage and the output stage can be studied independently. One-stage scheme possesses a simplified structure that combines the PFC circuit and the

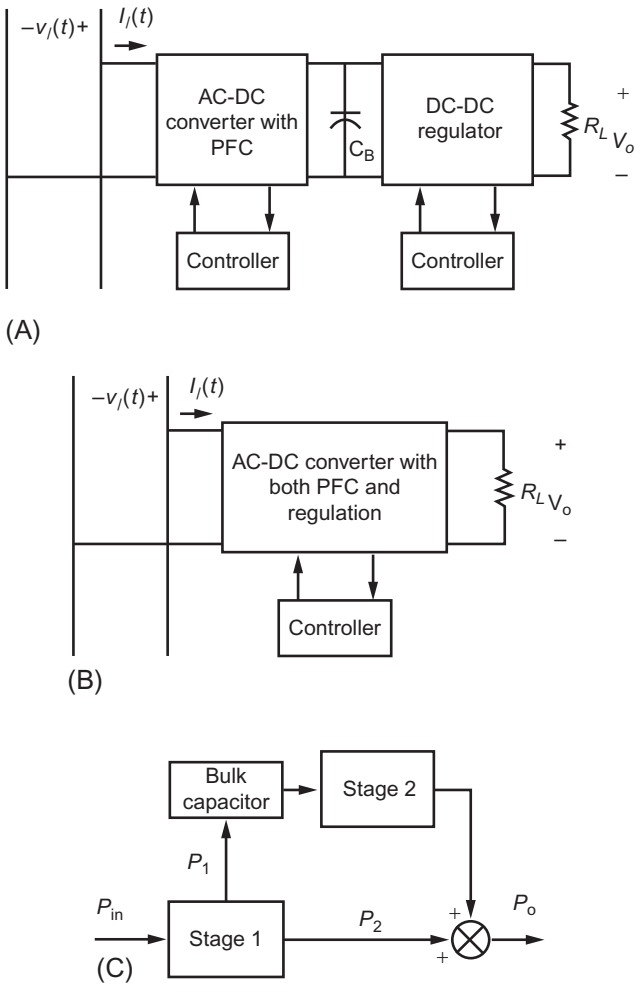


FIG. 16.15 System configurations of PFC power supply: (A) two-stage scheme, (B) one-stage scheme, and (C) parallel scheme.

power conversion circuit in one-stage as shown in Fig. 16.15B. Therefore, this topology is potentially more efficient and is very attractive in low to medium power level applications, particularly in those cost-sensitive applications. The one-stage scheme, therefore, becomes the main stream of contemporary research due to the ever-increasing demands for inexpensive power supply applications, such as residential and office appliance [1].

For many single-stage PFC converters, one of the most important issues is the slow dynamic response under line and load changes. To remove the low frequency ripple caused by the line (120 or 100 Hz) from the output and keep a nearly constant operation duty ratio, a large volume output capacitor is normally used. Consequently, a low frequency pole (typically less than 20 Hz) must be introduced into the feedback loop. This results in very slow dynamic response of the system [1,56,57].

The behavior of energy transfer in single-phase PFC converter and the behavior of the required storage decoupling element can be understood through the representation of the converter instantaneous input power and the average output power waveforms in more details as shown in Fig. 16.17. It can be seen clearly that the converter has to transfer a peak power equals to twice the average output power, whereas this power has to be stored and then restored to the converter output side. Typically, an output capacitor (placed at the output side of the converter) is not the desired solution to store this energy for two reasons. Firstly, the output voltage possesses voltage fluctuation with double line frequency because tight output voltage regulation will require a small output capacitor. Secondly, the converter requires a holdup time. Therefore, the right solution is the use of a decoupling capacitor to ensure the main operation of storing and restoring the energy during the two stages. The location of the energy storage element becomes critical and general configuration of the topology will play an important role [58]. The waveform presented in Fig. 16.17 can be used to find the relation between P_1 *and* P_2 based on the calculation of the areas corresponding to each power:

$$S_{P_2} = \int_{\pi/4\omega_l}^{3\pi/4\omega_l} (p_{\text{in}}(t) - P_0)\, dt = P_0 \int_{\pi/4\omega_l}^{3\pi/4\omega_l} -\cos(2\omega_l t)\, dt = \frac{P_0}{\omega_l} \tag{16.25}$$

$$S_{P_1} = \int_0^{\pi/\omega_l} (p_{in}(t))\, dt - S_{P_1} = P_0 \int_0^{\pi/\omega_l} (1 - \cos(2\omega_l t))\, dt - S_{P_1}$$
$$= P_0 \left(\frac{\pi}{\omega_l}\right) - \frac{P_0}{\omega_l} = \frac{P_0}{\omega_l}(\pi - 1) \tag{16.26}$$

It is found that 68.17% $\left(\frac{S_{P_1}}{S_{P_1}+S_{P_2}}\%\right)$ of the energy can be transferred directly to the output, and only 31.83% $\left(\frac{S_{P_2}}{S_{P_1}+S_{P_2}}\%\right)$ of the energy has to be stored and then reprocessed to the output.

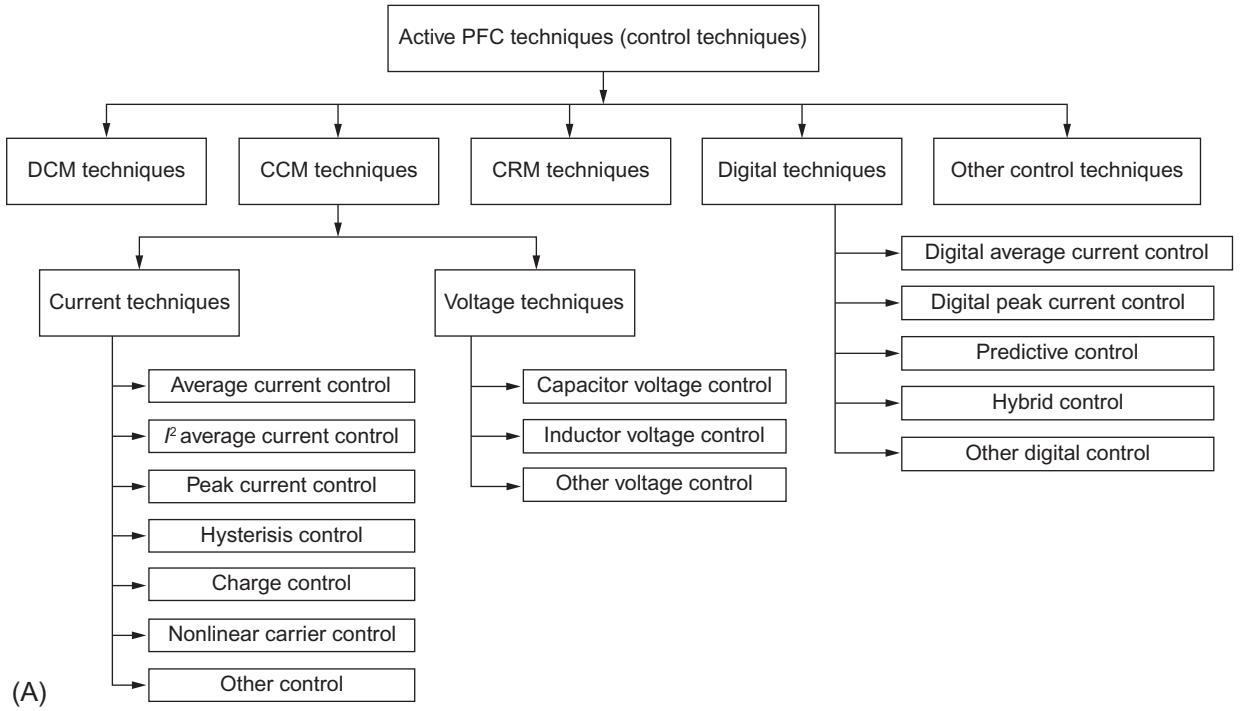
It is obvious that the double frequency will be hidden from the output voltage ripple if P_1 energy is directly transferred to the output due to the power storage excesses. Based on this analysis, improved and modified topologies of the basic converter topologies can be attained to achieve the direct energy transfer topology and the parallel energy transfer topology. Indeed, several works have been presented focusing mainly on the improvement of the PFC converter topology structure to ensure reduced number of components while delivering maximum energy directly to the output under enhanced efficiency [58–65].

To avoid twice power process in two-stage scheme, two converters can be connected in parallel to form so-called parallel PFC scheme (PPFC) as shown in Fig. 16.18 [66,67]. In parallel PFC circuit, power from the ac main to the load flows through two parallel paths, shown in Fig. 16.15C. The main path is a rectifier, in which power is not processed twice for PFC (about 68% of the average input power), whereas the other path processes the input power twice for PFC purpose. It is shown that to achieve both unity PF and tight output voltage regulation, only the difference between the input and output power within a half cycle (about 32% of the average input power) needs to be processed twice [1,66,67]. Therefore, high efficiency can be obtained by this method. In the PPFC topology, the common connection point of the two parallel paths appears at the output, where an isolation transformer is required for each stage (Fig. 16.18). Hence, this converter can be used effectively for the applications where the power level is high enough to justify the using of two isolations transformers that are too expensive and add more complexity to the converter topology [67].

An improved topology has been used to avoid the main disadvantages of the presented PPFC of Fig. 16.18. It combines the auxiliary stage with the main stage, and, therefore, only one isolation transformer is required. This used PPFC topology power process transfer principle is shown in Fig. 16.19, where only one power stage is used to transfer the input power (P_{in}) and the extra 32% power (P_2). Two application have been presented based on this PPFC topology, single-stage flyback PPFC converter and single-stage boost PPFC as shown in Fig. 16.20A and B; both topologies are using only one isolation transformer [67].

The continuous research in improving system PF up to date has resulted in countless circuit topologies and control strategies. Classified by their principles to realize PFC, they can be mainly categorized into three categories depending especially on the conduction current behavior of the input current of the converter that is related generally to the inductance of the equalizer PFC:

- Continuous conduction mode (CCM) that is based on the techniques of current shaping (current shaping technique (CST)) in Fig. 16.21
- Discontinuous conduction mode (DCM) that is based on current input control technique (CICT) in Fig. 16.22
- Critical conduction mode (CRM) that is similar to boundary conduction mode (BCM) or transition mode (TM) in Fig. 16.23



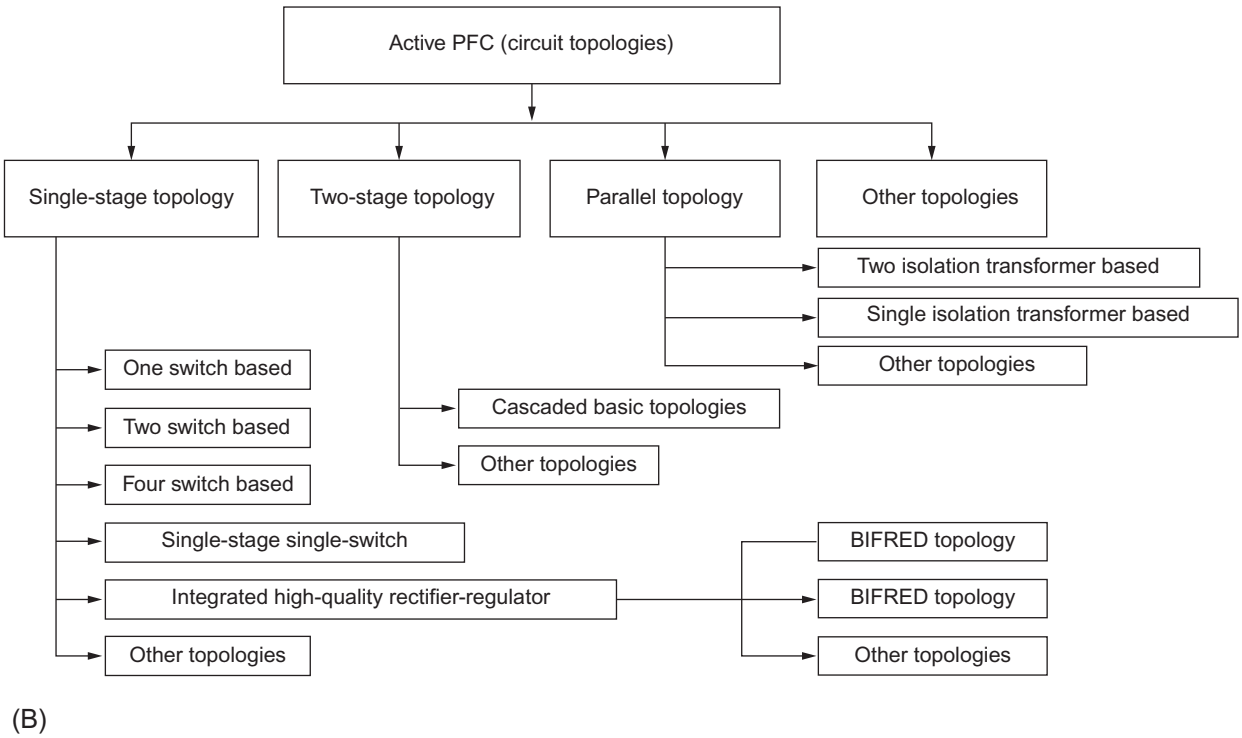


FIG. 16.16 Overview of (A) PFC control techniques and (B) PFC circuit topologies.

The recent research interest in DCM input technique is focused on developing PFC circuit topologies with a single power switch, result in single-stage single-switch converter (so-called S^4-converter) [1]. The CCM shaping technique emphasizes on the used control strategies and on the improved topologies to achieve high input PF for medium and high-power levels. When this technique is applied for the control of a continuous flow of current, a fixed or a variable switching frequency can be used [68].

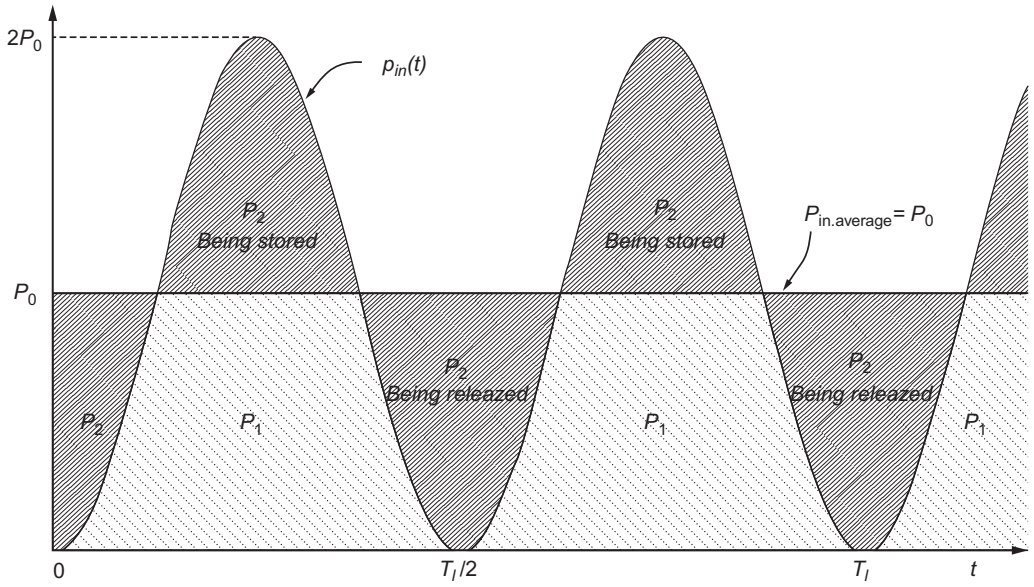


FIG. 16.17 The instantaneous single-phase input power waveform.

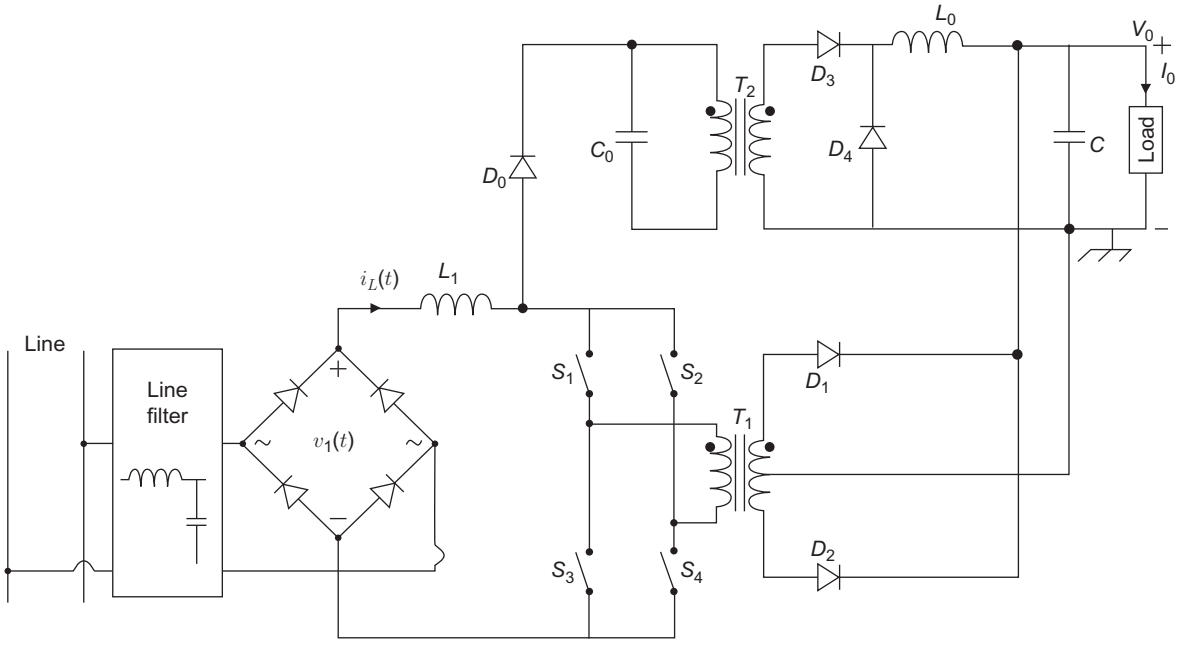


FIG. 16.18 The parallel power factor corrector (PPFC).

The CRM technique is on the boundary between CCM and DCM techniques. It was proved that it can ensure moderate switch losses, and in the same time, it can reduce the eventual diode reverse-recovery problems. The two main CRM PFC controller strategies of voltage mode and current mode can be used; however, the need to the voltage or the current sensors, depending on the used control strategy, adds more complexity to the used circuits [69].

The hot topics in this line of research are concentrated on degrading complexity of the control circuit and enhancing dynamic response of the system, resulting in some new control methods. Fig. 16.16 shows an overview of these techniques based on conduction mode and system configuration types [1]. It is obvious that the new developed and improved topologies based on the existing classical basic topologies can achieve the main objective of higher PF and lower THD than those of traditional topologies; this can be fulfilled by improving at the same time the control strategies for different modes of conduction.

16.4 CCM Shaping Technique

Like other power electronic apparatus, the core of a PFC unit is its converter, which can operate either in DCM, in CCM, or in CRM. As shall be discussed in the next section, the benefit from DCM technique is that low-cost power supply can be achieved because of its simplified control circuit. However, the peak input current of a DCM converter is at least twice as high as its corresponding average input current, which causes higher current stresses on switches than that in a CCM converter, resulting in intolerable conduction and switching losses and transformer copper losses in high-power applications. In practice, DCM technique is only suitable for low- to medium-level power application, whereas CCM is used in high-power cases. However, a converter operating in CCM does not have PFC ability inherently, that is, unless a certain control strategy is applied, the input current will not follow the waveform of line voltage. This is why most of the research activities in improving PF under CCM condition have been focused on developing new current shaping control strategies. Depending on the system variable being controlled (either current or voltage), PFC control techniques may be classified as current control and voltage control. Current control is the most common control strategy since the primary objective of PFC is to force the input current to trace the shape of line voltage [1].

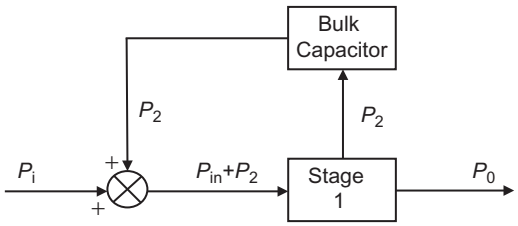


FIG. 16.19 The power process transfer principle under the improved PPFC topology.

To achieve both PFC and output voltage regulation by using a converter operating in CCM, multiloop controls are generally used. Fig. 16.24 shows the block diagram of AC-DC PFC converter with CCM shaping technique, where H_l is a line voltage compensator, H_x is a controlled variable compensator, and $x(t)$ is the control variable that can be either current or voltage [1].

Normally, in order to obtain a sinusoidal line current and a constant dc output voltage, line voltage $v_l(t)$, output voltage V_o, and a controlled variable $x(t)$ need to be sensed. Depending on whether the controlled variable $x(t)$ is a current (usually the line current or the switch current) or a voltage (related

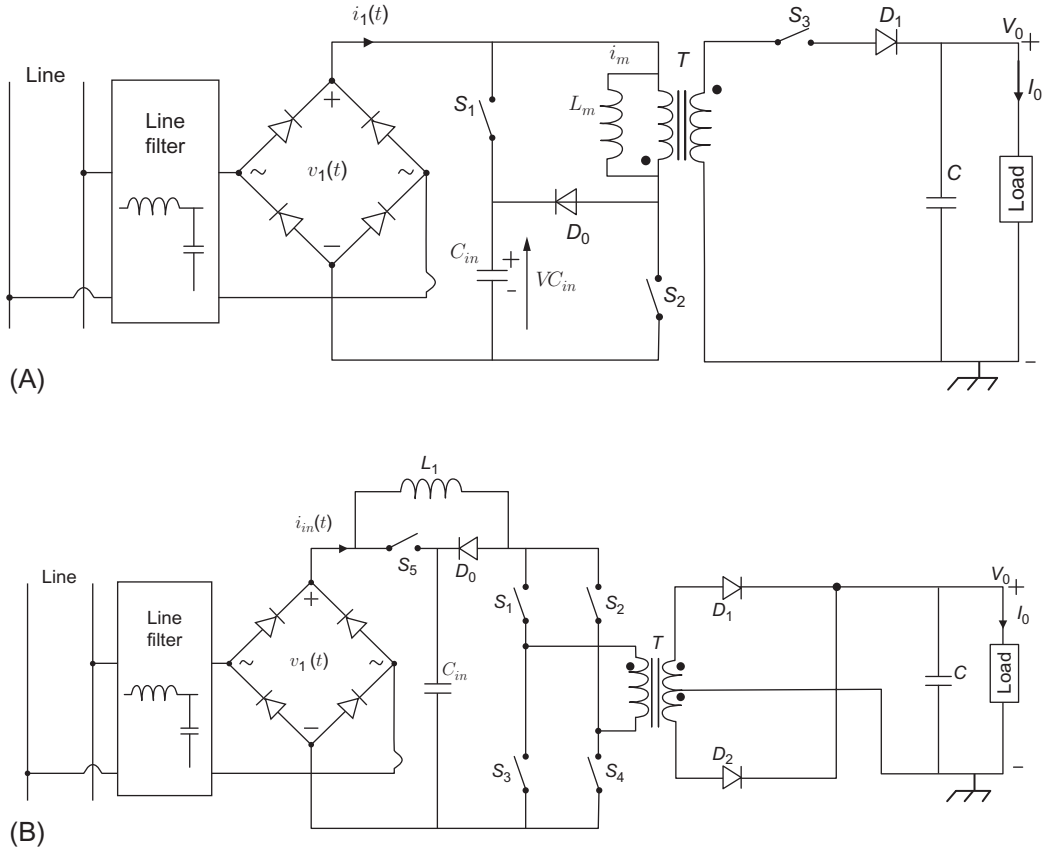


FIG. 16.20 PPFC converters improved topologies, (A) single-stage flyback PPFC converter and (B) single-stage boost PPFC converter.

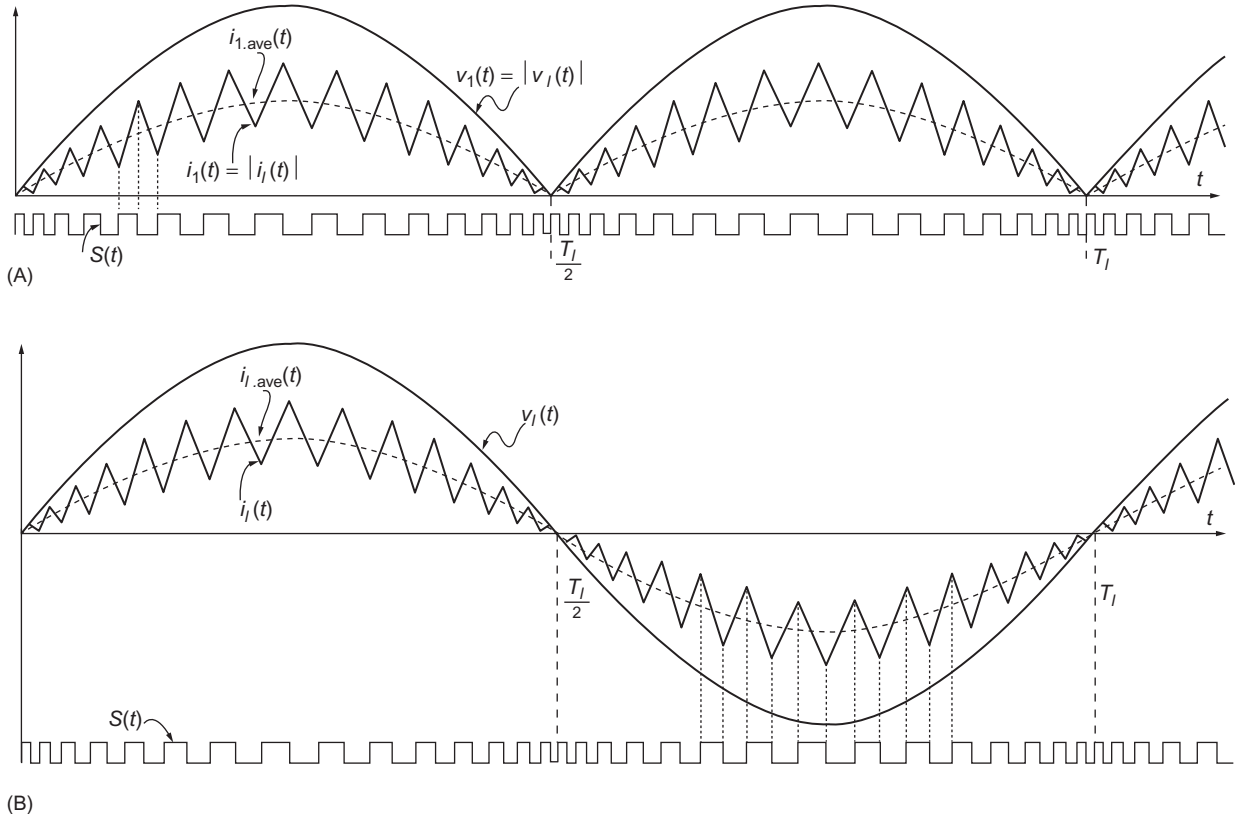


FIG. 16.21 Continuous conduction mode (CCM) principle: (A) the input current waveform of the PFC circuit and (B) the line current waveform.

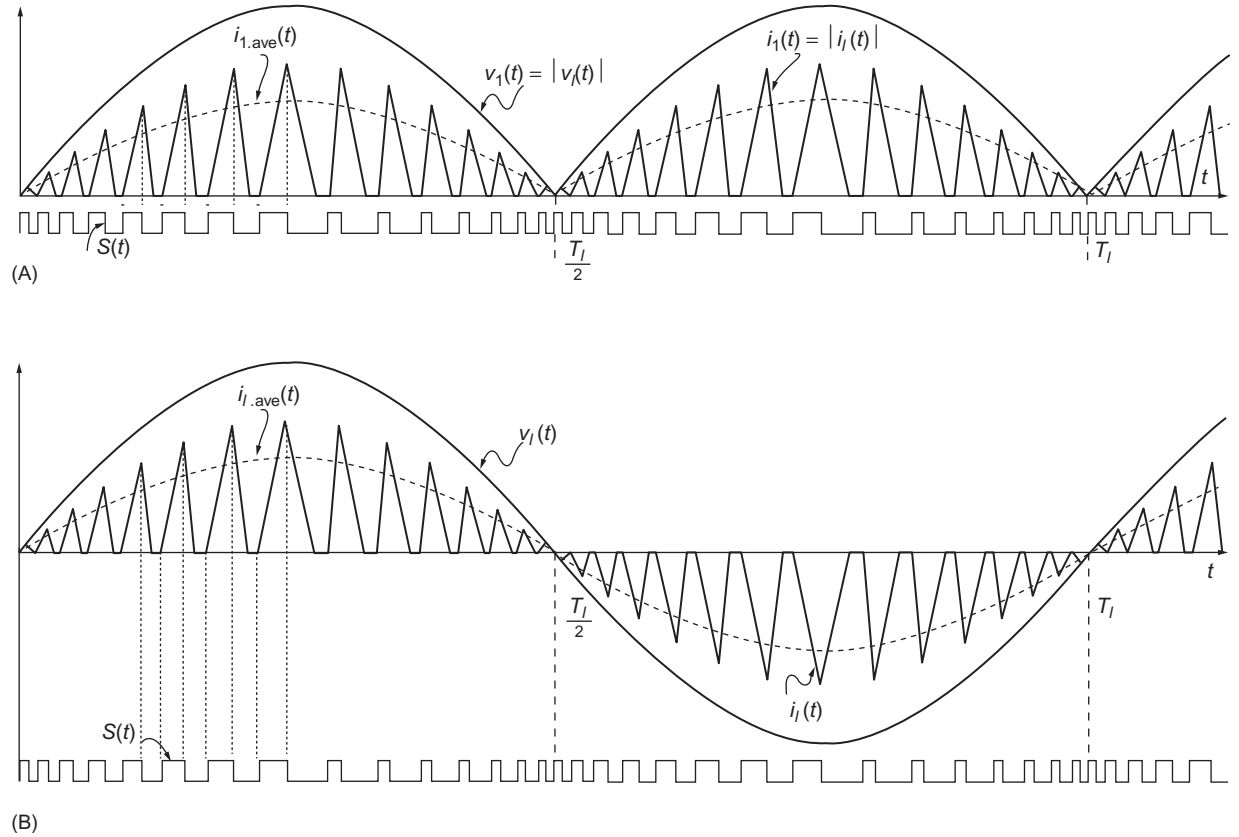


FIG. 16.22 Discontinuous conduction mode (DCM) principle: (A) the input current waveform of the PFC circuit and (B) the line current waveform.

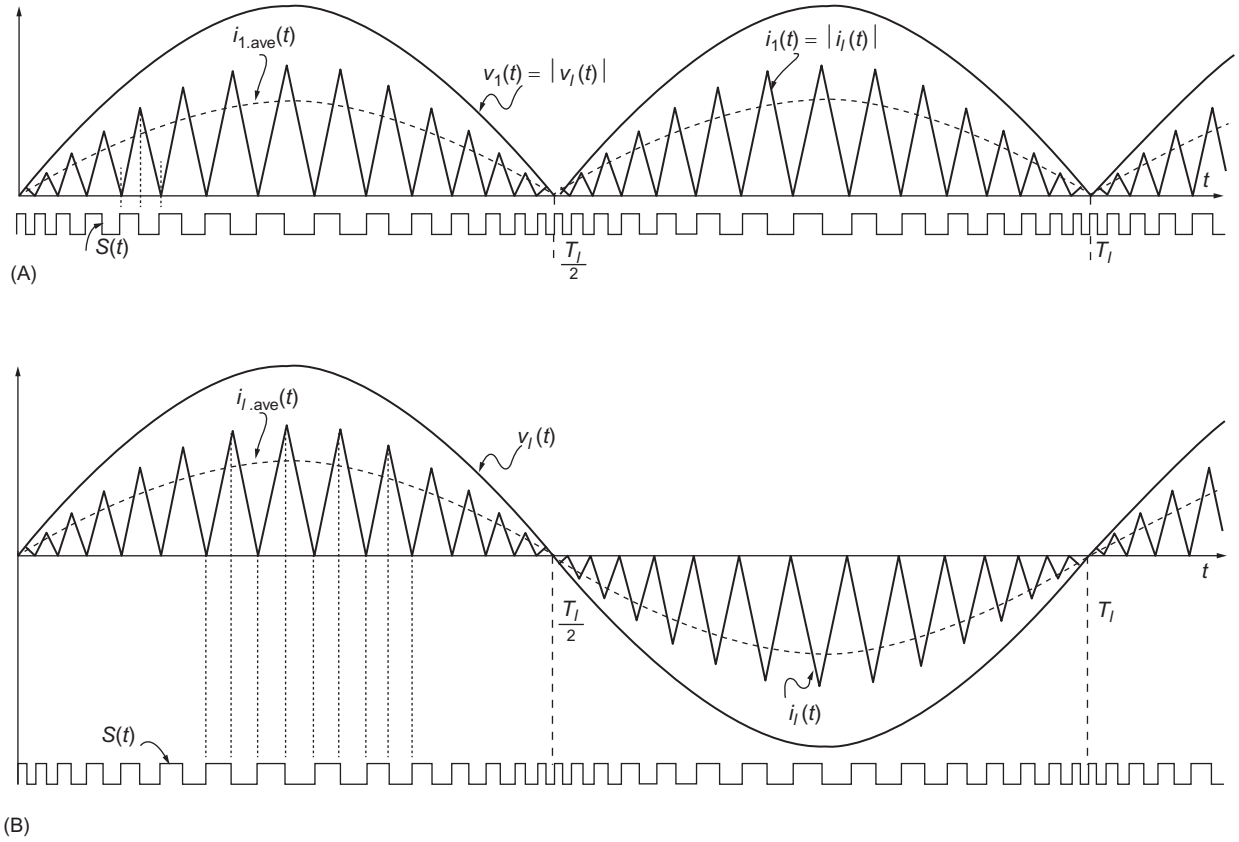


FIG. 16.23 Critical conduction mode (CRM) principle: (A) the input current waveform of the PFC circuit and (B) the line current waveform.

to the line voltage or rectified line voltage), the control technique is called "current mode control" or "voltage mode control," respectively. In Fig. 16.24, two control loops have been applied: the feedforward loop and the feedback loops. The feedforward loop is also called "inner loop," which keeps the line current to follow the line voltage in shape and phase, while the feedback loop (also called "outer loop") keeps the output voltage to be tightly controlled. These two loops share the same control command generated by the product of output voltage error signal and the line voltage (or rectified line voltage) signal [1].

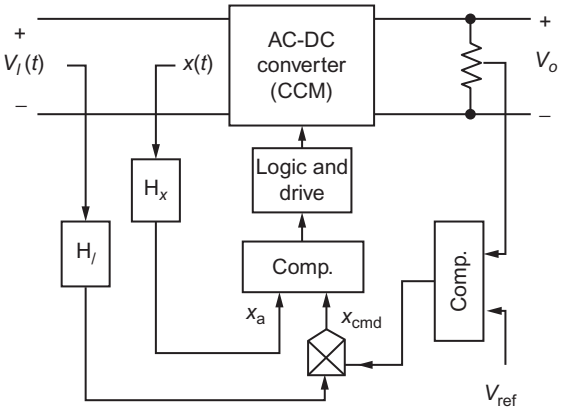


FIG. 16.24 Block diagram of PFC converter with CCM shaping technique.

16.4.1 Current Mode Control

Over many years, different current mode control techniques were developed. In this section, we will review several known methods.

16.4.1.1 Average Current Control

In average current control (ACM) strategy, the average line current of the converter is controlled to be shaped to a sine waveform which in phase with the line voltage. It is more desired than the other control strategies because the line current in a SMPS can be approximated by the average current (per switching cycle) through an input EMI filter. This control strategy is widely used in several industries due to the improved noise immunity, the lower input ripple, and the stable operation [56,70–73].

Fig. 16.22 shows a boost PFC circuit using ACM strategy. In the feedforward loop, a low value resistor R_s is used to sense the line current. Through the op-amp network formed by R_i, R_{imo}, R_f, C_p, C_z, and A_2, average line current is detected and compared with the command current signal, i_{cmd}, which is generated by the product of line voltage signal and the output voltage error signal.

There is a common issue in CCM shaping technique, that is, when the line voltage increases, the line voltage sensor provides an increased sinusoidal reference for the feedforward loop. Since the response of feedback loop is much slow than the feedforward loop, both the line voltage and the line current increase, that is, the line current is heading to wrong changing direction (with the line voltage increasing, the line current should decrease). This results in excessive input power, causing overshoot in the output voltage. The square block, x^2, in the line voltage-sensing loop shown in Fig. 16.25 provides a typical solution for this problem. It squares the output of the low-pass filter (LPF), which is in proportion to the amplitude of the line voltage and provides the divider $(A \times B)/C$ with a squared line voltage signal for its denominator. As a result, the amplitude of the sinusoidal reference i_{cmd} is negatively proportional to the line voltage, that is, when the line voltage changes, the control circuit leads the line current to change in the opposite direction, which is the desired situation. The detailed analysis and design issues can be found in [1,70–72].

As it can be seen, the ACM is a very complicated control strategy. It requires sensing the inductor current, the input voltage, and the output voltage. An amplifier for calculating the average current and a multiplier are needed. Actually, due to the advances made in IC technology, these circuits are integrated in a single chip, where many control ICs are available from different manufacturers.

16.4.1.2 I^2 Average Current Mode Control

This control technique is proposed to improve the transient response and the light load efficiency of the existing average current mode control [74]. The main principle of this control technique is applied to buck converter as shown in Fig. 16.26.

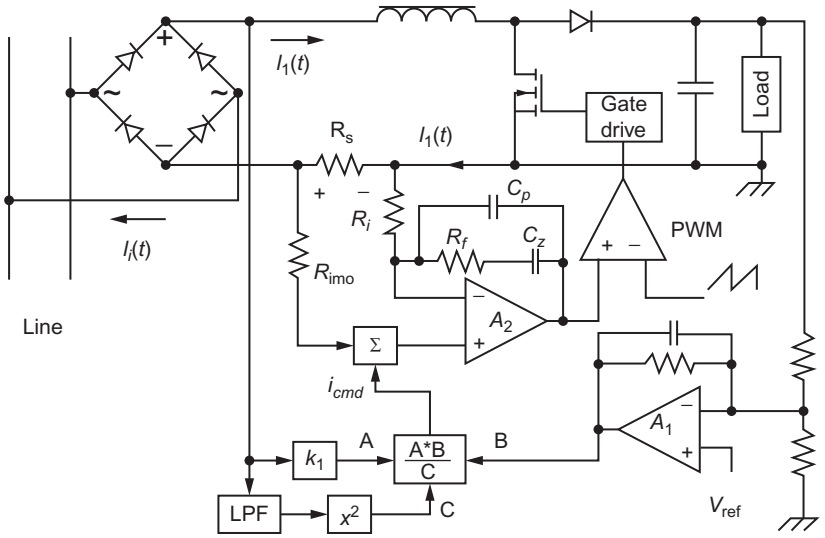


FIG. 16.25 Boost corrector using average current control.

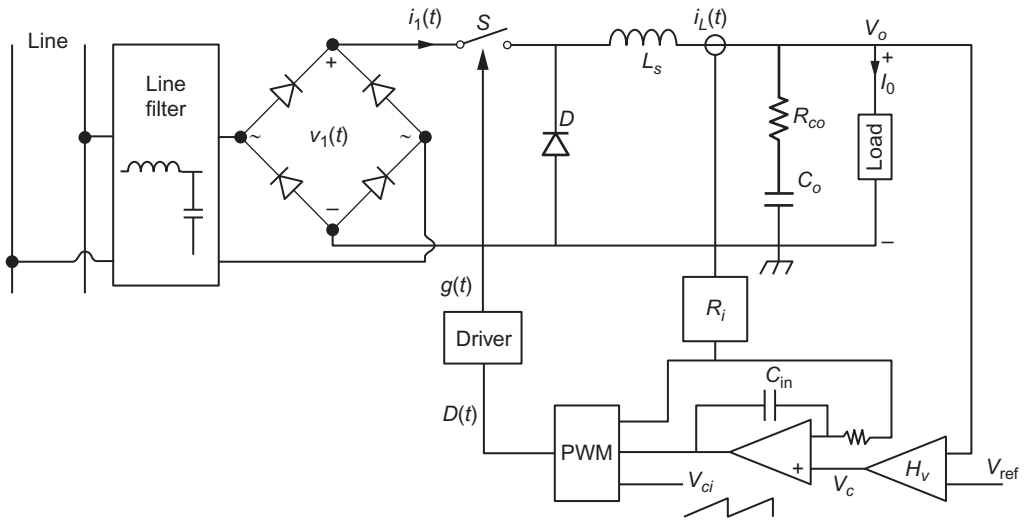


FIG. 16.26 The concept of I^2 average current mode control.

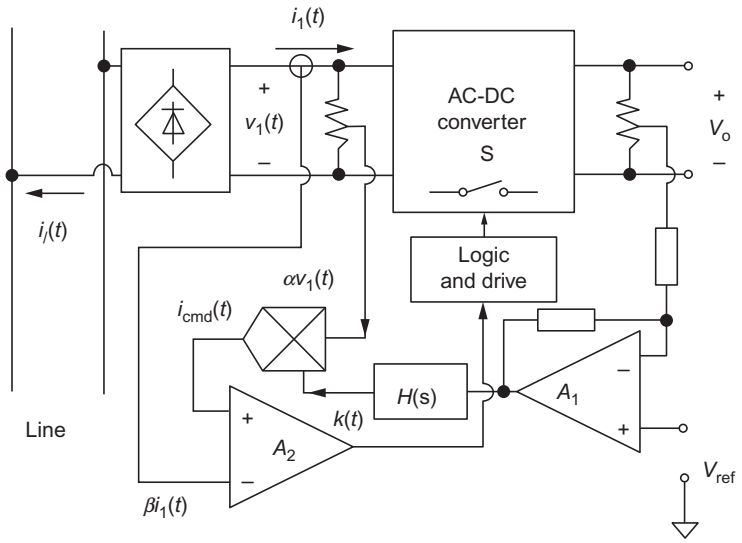


FIG. 16.27 Block diagram for variable frequency peak current control.

It is based on the use of three loops, two current inner loops and one voltage outer loop. The first current loop presents a slow integral feedback that integrates the error between the output voltage of the voltage loop V_c and the current through L_s. The second current loop presents a fast direct feedback of the current through L_s without LPF that is compared with the integrator output of the first current loop to generate the PWM signal. The third loop is dedicated to ensure the output voltage regulation. As the current through L_s is measured once and it is used twice in the two control loops, the proposed control technique is named as I^2 control. In general, this concept is applicable to constant frequency modulations and variable frequency modulations [74,75].

16.4.1.3 Variable Frequency Peak Current Control

Although the ACM is a more desired strategy, the peak current control has been widely accepted because it improves the converter efficiency and has a simpler control circuit [57,76–80]. In variable frequency peak control strategy, shown in Fig. 16.27, the output error signal $k(t)$ is fed back through its outer loop. This signal is multiplied by the line voltage signal $\alpha v_1(t)$ to form a line current command signal $i_{cmd}(t)$ $(i_{cmd}(t) = \alpha k(t) \cdot v_1(t))$. The command signal $i_{cmd}(t)$ is the desired line current shape since it follows the shape of the line voltage. The actual line current is sensed by a transducer, resulting in signal $\beta i_1(t)$ that must be reshaped to follow $i_{cmd}(t)$ by feeding it back through the inner loop. After comparing the line current signal $\beta i_1(t)$ with the command signal $i_{cmd}(t)$, the following control strategies can be realized, depending on its logic circuit [1]:

Constant on-time control: Its input current waveform is given in Fig. 16.28A. Letting the fixed on time to be T_s, the control rules are the following:

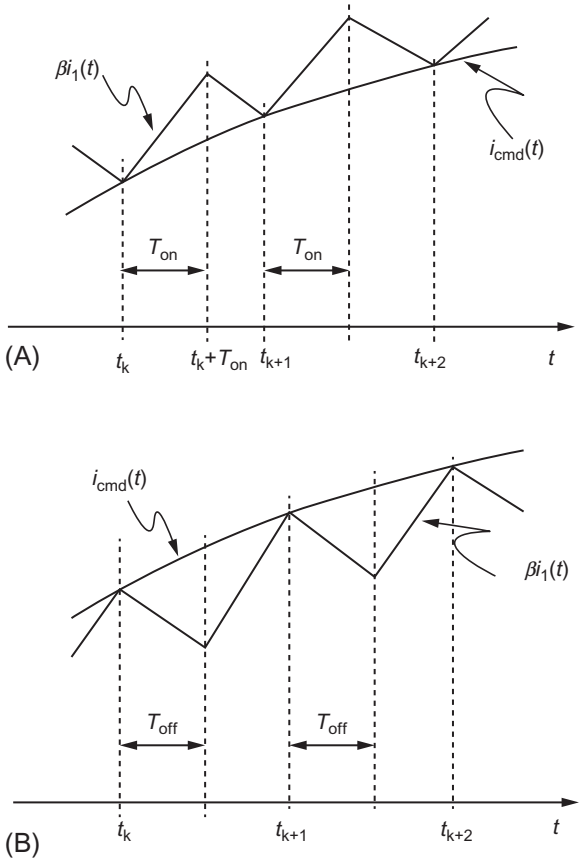


FIG. 16.28 Input current waveforms for variable frequency peak current control: (A) constant on-time control and (B) constant off-time control.

- At $t = t_k$ when $\beta i_1(t_k) = i_{cmd}(t_k)$, S is turned on.
- At $t = t_k + T_{on}$, S is turned off.

Constant off-time control: The input current waveform is shown in Fig. 16.28B. Assuming the offtime is T_{off}, the control rules are the following:

- At $t = t_k$ when $\beta i_1(t_k) = i_{cmd}(t_k)$, S is turned off.
- At $t = t_k + T_{off}$, S is turned on.

16.4.1.4 Constant Frequency Peak Current Control

Generally speaking, to make it easier to design the EMI filter and to reduce harmonics, constant switching frequency AC-DC PFC converter is preferred. Based on the block diagram shown in Fig. 16.29, with T_s is the switching period, the following control rules can be considered to realize a constant frequency peak current control (shown in Fig. 16.30B) [1]:

- At $t = nT_s$, S is turned on.
- At $t = t_n (t_n \in [(n-1)T_s, nT_s])$ when $\beta i_1(t_n) = i_{cmd}(t_n)$, S is turned off.

The logic circuit for the above control rules can be realized by using an R-S flip-flop with a constant frequency setting clock pulse (CP), as shown in Fig. 16.29. Unfortunately, this logic circuit will result in instability when the duty ratio exceeds 50%. This problem can be solved by subtracting a stabilizing ramp signal from the original command signal. Fig. 16.30A shows a complete block diagram for typical constant frequency peak current control strategy. The line current waveform is shown in Fig. 16.30B [1].

It should be noticed that in both variable frequency and constant frequency peak current control strategies, either the input current or the switch current could be controlled. Thus, it makes possible to apply these control methods to buck-type converters. There are several advantages of using peak current control [1]:

- The peak current can be sensed by current transformer, resulting in reduced transducer loss.
- The current-error compensator for average control method has been eliminated.

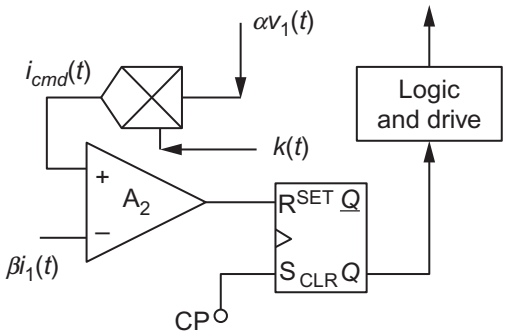


FIG. 16.29 Logic circuit for constant frequency peak current control.

- Low gain in the feedforward loop enhances the system stability.
- The instantaneous pulse-by-pulse current limit leads to increased reliability and response speed.

However, the three signals, line voltage, peak current, and output voltage signals, are still necessary to be sensed and multiplier is still needed in each of the peak current control method. Comparing with the ACM method, the input current ripple of these peak current control methods may be high when the line voltage is near the peak value. As a result, considerable line current distortion exists under high-line voltage and light low operation conditions [1].

16.4.1.5 Hysteresis Control

Unlike the constant on-time (COT) and the constant off-time control, in which only one current command is used to limit either the minimum input current or the maximum input current, the hysteresis control has two current commands, $i_{hcmd}(t)$ and $i_{lcmd}(t)$ ($i_{lcmd}(t) = \delta i_{hcmd}(t)$); $\delta$is the hysteresis band width which is supposed to be constant to limit both the minimum and the maximum of input current [81–84]. To achieve smaller ripple in the input current, we desire a narrow hysteresis band. However, with a reduced hysteresis band width a higher switching frequency is required. Therefore, the hysteresis bandwidth should be optimized based on circuit components such as switching devices and magnetic components. Moreover, the switching frequency varies with the change of line voltage, resulting in difficulty in the design of the EMI filter. The circuit diagram and input current waveform are given in Fig. 16.31A and B, respectively. When $\beta i_1(t) \geq i_{hcmd}(t)$, a negative pulse is generated by comparator A_1 to reset the R-S flip-flop. When $\beta i_1(t) \leq i_{lcmd}(t)$, a negative pulse is generated by comparator A_2 to set the R-S flip-flop. The control rules are the following:

- At $t = t_k$ when $\beta i_1(t_k) = i_{lcmd}(t_k)$, S is turned on.
- At $t = t_{k+1}$ when $\beta i_1(t_{k+1}) = i_{hcmd}(t_{k+1})$, S is turned off.

Like the above mentioned peak current control methods, the hysteresis control method has simpler implementation, enhanced system stability, and increased reliability and response speed. In addition, it has better control accuracy than that the peak current control methods have. However, this improvement is achieved on the penalty of wide range of variation in the switching frequency. It is also possible to improve the hysteresis control in a constant frequency operation [85,86], but usually, this will increase the complexity of the control circuit [1].

16.4.1.6 Charge Control

In order to make the average control method to be applicable for buck-derived topologies where the switch current instead of the inductor current needs to be controlled, an alternative method to realize ACM, namely, charge control was proposed in [87–89]. Since the total charge of the switch current per

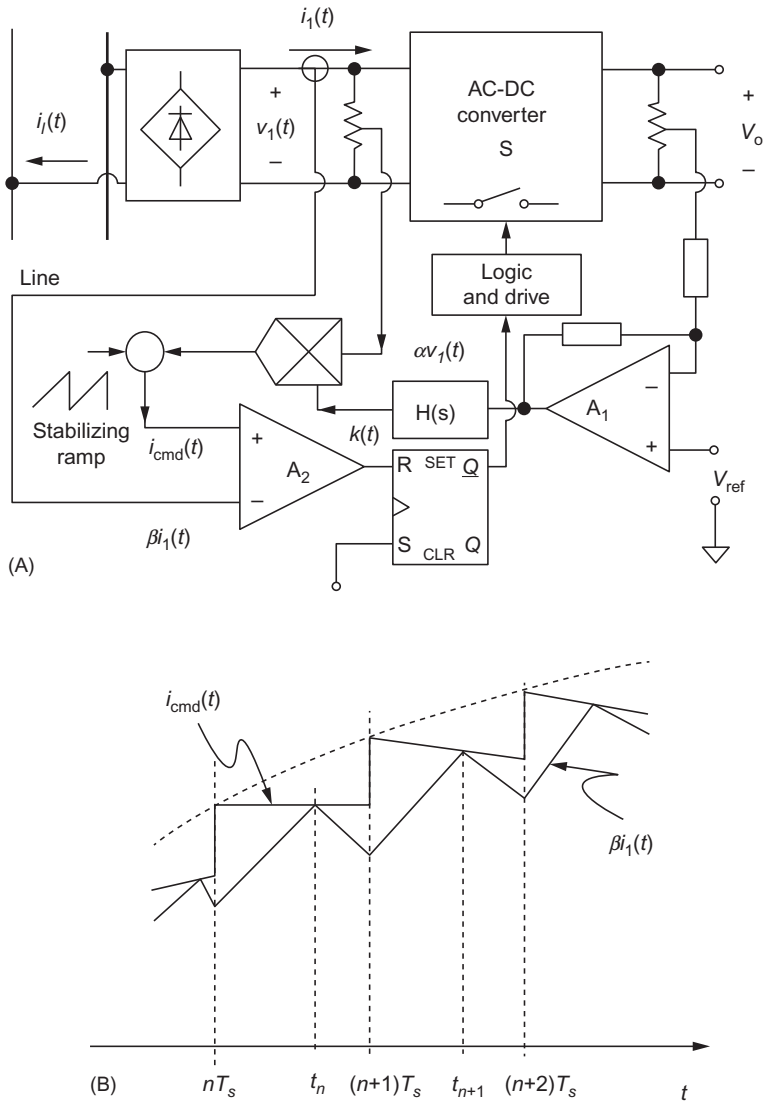


FIG. 16.30 (A) Constant frequency peak current control with stabilizing ramp compensation and (B) line current waveform for constant frequency peak current control.

switching cycle is proportional to the average value of the switch current, the average current can be detected by a capacitor-switch network. Fig. 16.32 shows a block diagram for charge control. The switch current is sensed by current transformer T_1 and charges the capacitor C_T to form average line current signal. As the switch current increases, the charge on capacitor C_T also increases. When the voltage reaches the control command v_c, the power switch turns off. At the same time, the switch S_d turns on to reset the capacitor. The next switching cycle begins with the power switch turning on and the switch S_d turning off by a CP [1].

The advantages of charge control are the following:

- Ability to control average switch current
- Better switching noise immunity than peak current control
- Good dynamic performance
- Elimination of turn-off failure in some converters (e.g., multiresonant converter) when the switch current reaches its maximum value

The disadvantages are the following:

- Synthesis of the reference v_c still requires sensing both input and output voltage and use of a multiplier.
- Subharmonic oscillation may exist.

16.4.1.7 Nonlinear-Carrier Control

To further simplify the control circuitry, nonlinear-carrier (NLC) control methods were introduced [90,91]. In CCM operation, since the input voltage is related to the output voltage through the conversion ratio, the input voltage information can be recovered by the sensed output voltage signal. Thus, the sensing of input voltage can be avoided, and therefore, the

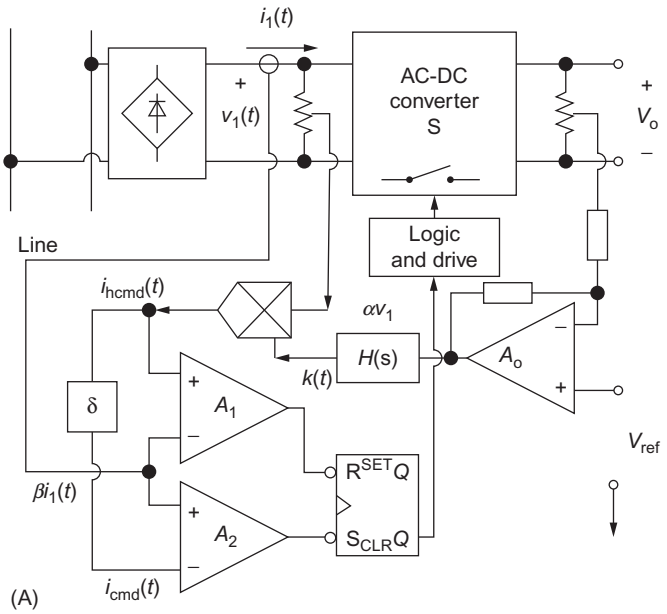


FIG. 16.31 Hysteresis control: (A) block diagram for hysteresis control and (B) line current waveform of hysteresis control.

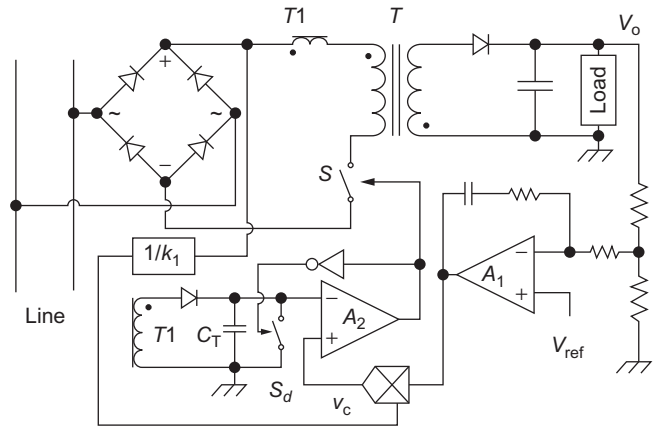


FIG. 16.32 Flyback PFC converter using charge control.

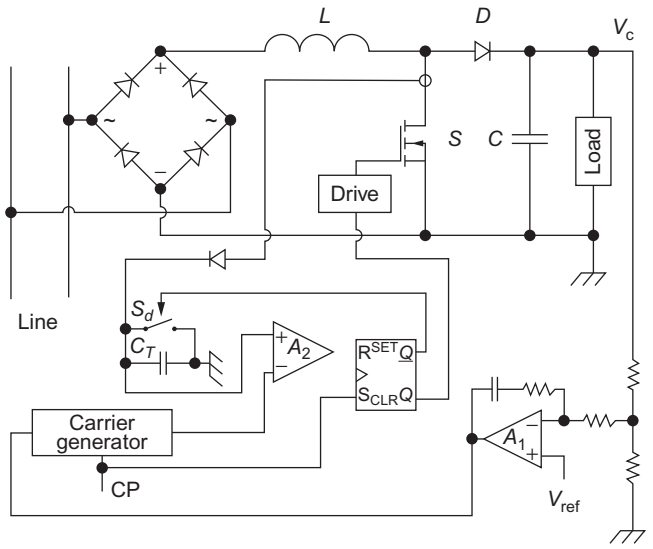


FIG. 16.33 Boost PFC converter using NLC control.

multiplier is not needed, resulting in significant simplification in the control circuitry. However, complicated NLC waveform generator and its designs are involved. Fig. 16.33 shows the block diagram of the NLC charge control first introduced in [90,1].

16.4.2 Voltage Mode Control

Generally, current mode control is preferred in current source driven converters, as the boost converter. To develop controllers for voltage source driven converter, like the buck converter and to improve dynamic response, voltage mode control (VMC) strategy was proposed [92,93]. Fig. 16.34 shows the input circuit of an AC-DC converter and its phasor diagram representation, where ϕ is the phase shift between the line current and the capacitor voltage. An *LC* network could be added to the input either before a switch-mode rectifier (SMR) or after a passive rectifier to perform such kind of control. In boost type converter, the inductor L_i is the input inductor. It can be seen from the phasor diagram that to keep the line current in phase with the line voltage, we can control either the capacitor voltage or the inductor voltage. If the capacitor voltage is chosen as controlled variable, the control strategy is known as delta modulation control [1].

16.4.2.1 Capacitor Voltage Control

Fig. 16.35 gives a SMR with PFC using capacitor voltage control [92]. The capacitor voltage $v_{c1}(t)$ is forced to track a sinusoidal command signal $v_{c1}{}^*(t)$ to indirectly adjust the line current $i_l(t)$ to be in phase with the line voltage $v_l(t)$. The command signal is the product of the line voltage signal with a phase shift of ϕ and the feedback error signal. The phase shift ϕ that has to be measured accurately is a function of the magnitudes of line voltage and line current; therefore, achieving the delta modulation control is not really simple. In addition, since ϕ is usually very small, a small change in capacitor voltage that may occur

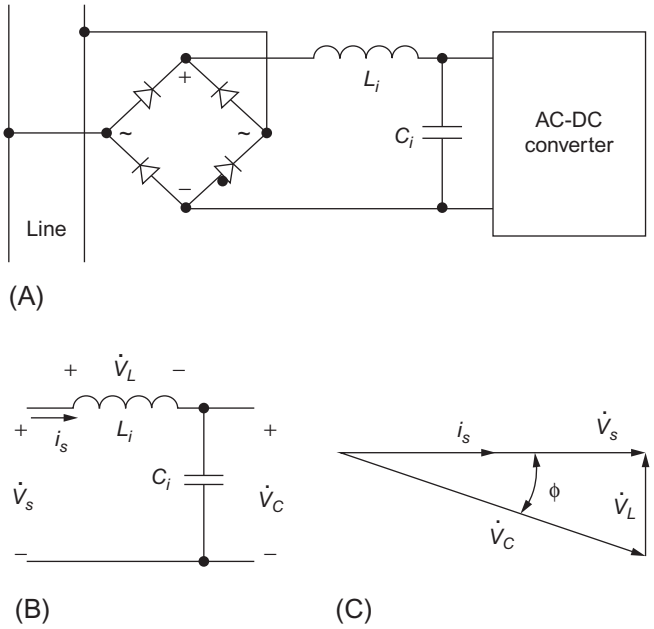


FIG. 16.34 Input circuit and phasor diagram for voltage control: (A) input circuit of voltage control ac-dc converter, (B) simplified input circuit, and (C) phasor diagram.

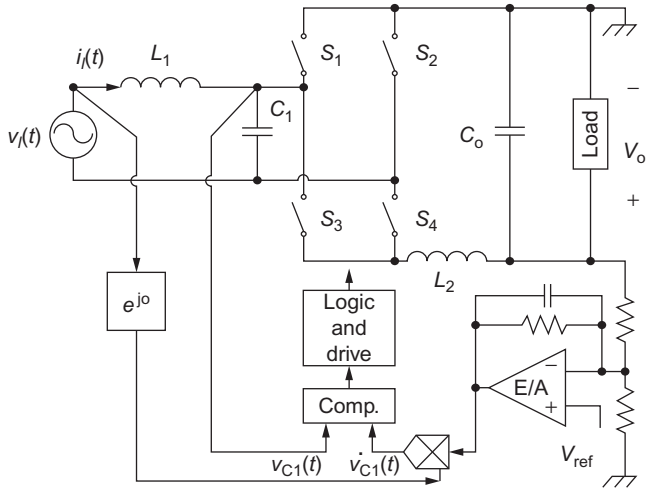


FIG. 16.35 SMR using capacitor voltage control.

due to small load change or to small output voltage reference change V_{ref} will cause a large change in the inductor voltage and hence in the line current. Thus, it makes the circuit very sensitive to parameter variations and perturbations [1].

16.4.2.2 Inductor Voltage Control

To overcome the above shortcomings, inductor voltage control (IVC) strategies were reported in [93]. Fig. 16.36 shows an SMR with PFC using IVC. As the phase difference between the line voltage and the inductor voltage is fixed at 90 degrees ideally, the control circuit is simpler in implementation than that of

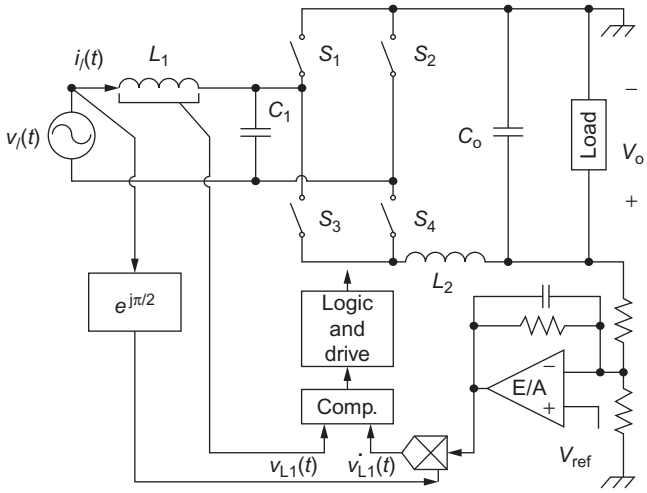


FIG. 16.36 SMR using inductor voltage control.

capacitor voltage control. As the inductor voltage is sensitive to the phase shift ϕ, but not sensitive to the change in magnitude of reference, the IVC method is more effective in keeping the line current in phase with the line voltage. However, in the implementations of both the two kinds of voltage control methods hysteresis technique is normally used. Therefore, unlike the previous current mode control, variable frequency problem is encountered in these control methods [1].

Generally speaking, by using CCM shaping technique, the input current can trace the wave shape of the line voltage well. Hence, the PF can be improved efficiently. However, this technique involves in the designing of complicated control circuits. Multiloop control strategy is needed to perform ICS and output regulation. In most CCM shaping techniques, current sensor and multiplier are required, which result in higher cost in practical applications. In some cases, variable frequency control is inevitable, resulting in additional difficulties in its closed-loop design. Table 16.1 gives a comparison among these control methods [1].

16.5 DCM Input Technique

The DCM can be considered as a special case of the CCM. It presents more than one structural change during one switching period. To get rid of the complicated control circuit invoked by CCM shaping technique and reduce the cost of the electronic interface, DCM input technique can be adopted in low-power to medium power level application.

In DCM, the inductor current of the core converter is no longer a valid state variable since its state in a given switching cycle is independent of the value in the previous switching cycle [94]. The peak of the inductor current is sampling the line voltage automatically, resulting in sinusoidal-like average input current (line current). This is why DCM input circuit is also called

TABLE 16.1 Comparison of CCM shaping techniques

	Average current	I^2 average current	VF peak current	CF peak current	Hysteresis	Charge	Nonlinear-carrier	Capacitor voltage	Inductor voltage
Input ripple	Low	Low	High	High	Low	Low	Low	Low	Low
Switching frequency	Constant	Constant and variable	Variable	Constant	Variable	Constant	Constant	Variable	Variable
Dynamic response	Slow	Improved transient response	Slow	Slow	Fast	Fast	Fast	Fast	Fast
Control signal sensed for inner loop	Input current and input voltage	Two input current and input voltage	Input (or switch) current and input voltage	Input (or switch) current and input voltage	Input current and input voltage	Input (or switch) current and input voltage	Input (or switch) current	Input voltage and capacitor voltage	Input voltage and inductor voltage
Inner loop E/A	Yes	Yes	No	No	Yes	No	No	No	No
Multiplier	Yes	No	Yes	Yes	Yes	Yes	No	Yes	Yes

"voltage follower" or "automatic controller" [1]. The benefit of using DCM input circuit for PFC is that no feedforward control loop is required, because with this approach, the internal current loop is completely eliminated, so that the switch is operated at COT and frequency. This is also the main advantage over a CCM PFC circuit, in which multiloop control strategy is essential. However, the input inductor operating in DCM cannot hold the excessive input energy because it must release all its stored energy before the end of each switching cycle. As a result, a bulky capacitor is used to balance the instantaneous power between the input and output. In addition, in DCM, the input current is normally a train of triangle pulses with nearly constant duty ratio. In this case, an input filter is necessary for smoothing the pulsating input current [1]. With the converter working in DCM, the DCM PWM control technique allows unity PF when used with converter topologies like flyback, Cuk, and Sepic. Instead, with the boost PFC, this technique causes some harmonic distortion in the line current [95].

16.5.1 PFC Capabilities of the Basic Converter Topologies in DCM

The DCM input circuit can be one of the basic DC-DC converter topologies. However, when they are applied to the rectified line voltage, they may draw different shapes of average line current. In order to examine the PFC capabilities of the basic converters, we first investigate their input characteristics. Because the input currents of these converters are discrete when they are operating in DCM, only averaged input currents are considered. Since switching frequency is much higher than the line frequency, let's assume the line voltage is constant in a switching cycle. In steady state operation, the output voltage is nearly constant, and the variation in duty ratio is slight. Therefore, constant duty ratio is considered in deriving the input characteristics [1]. To simplify the analysis of different topologies of converter working in DCM for achieving the main objective of current shaping, the following assumptions were made:

1. The converter is lossless.
2. The duty ratio of the converter is kept constant throughout the entire line cycle.
3. The switching frequency is much higher than the line frequency.
4. The leakage inductances of transformers are negligible.
5. Despite of slight changes in DC bus voltage, it is considered to be constant during each line cycle.

16.5.1.1 Buck Converter

The basic buck converter topology and its input current waveform when operating in DCM are shown in Fig. 16.37A and B, respectively. The instantaneous output current of the rectifier is presented as follows:

$$i_1(t) = \frac{|v_1(t)| - V_0}{L} t \tag{16.27}$$

It can be shown that the average output current of the rectifier in one switching cycle is given by

$$i_{1,\text{avg}}(t) = \frac{1}{2} \cdot D^2 T_s \frac{|v_1(t)| - V_0}{L} = \frac{D^2 T_s}{2L} (|v_1(t)| - V_0) \tag{16.28}$$

The average line current or the average input current of the rectifier during one switching cycle is given as follows:

$$\begin{cases} i_l(t) = \dfrac{D^2 T_s}{2L} (|v_1(t)| - V_0) & \text{if } v_1(t) \geq V_0 \\ i_l(t) = -\dfrac{D^2 T_s}{2L} (|v_1(t)| - V_0) & \text{if } v_1(t) \leq -V_0 \\ i_l(t) = 0 & \text{if } |v_1(t)| \geq V_0 \end{cases} \tag{16.29}$$

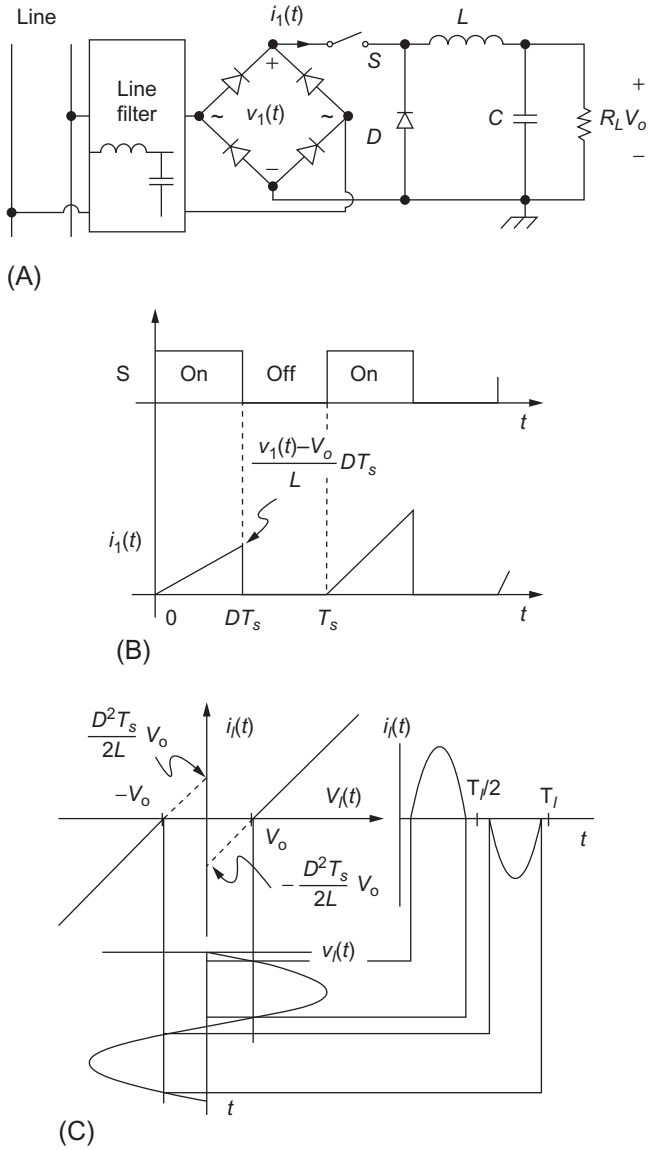


FIG. 16.37 Input *I-V* characteristic of basic buck converter operating in DCM: (A) buck converter, (B) input current, and (C) input *I-V* characteristic.

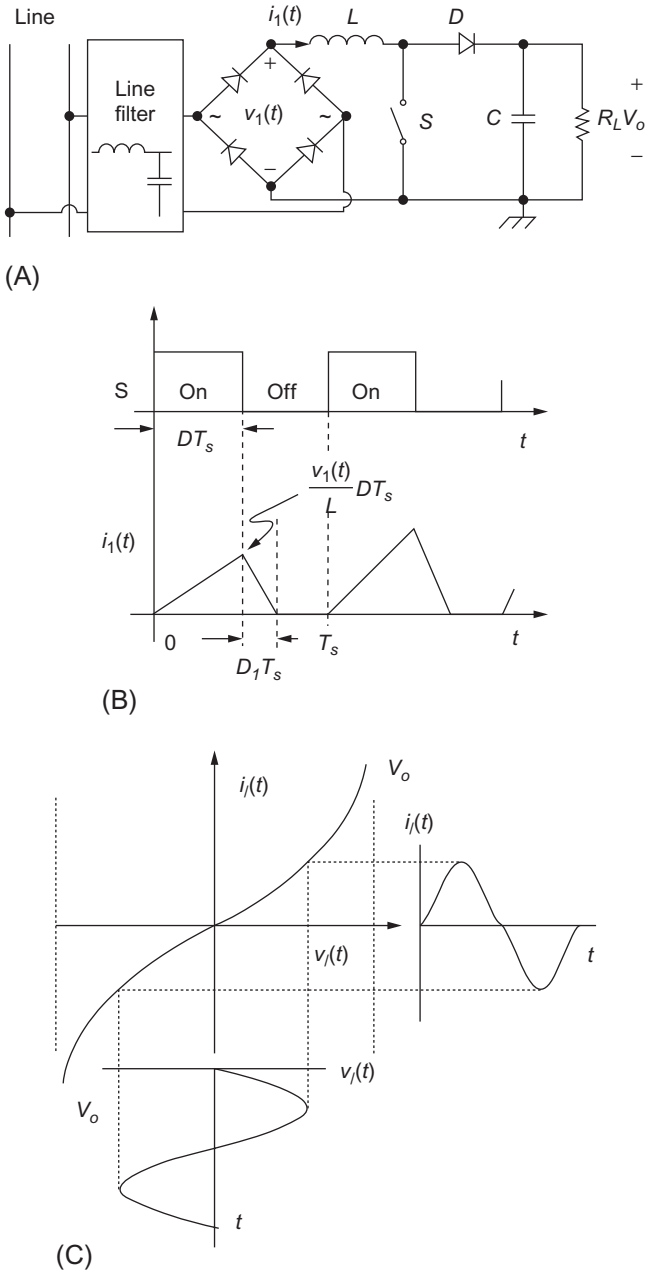


FIG. 16.38 Input *I-V* characteristic of basic boost converter operating in DCM: (A) boost converter, (B) input current, and (C) input *I-V* characteristic.

Where it is supposed that the input voltage waveform is sinusoidal and the drop voltage along the rectifier is neglected. Based on Eq. (16.27), Fig. 16.37C shows that the input voltage-input current *I-V* characteristic consists of two straight lines in quadrants I and III. These straight lines that are presenting the average instantaneous input current versus the input voltage do not go through the origin. It is obvious that the instantaneous average value of the input current is equal to zero within the interval $v_1 \in [-V_0 V_0]$. When $v_1(t) \geq 0 \& v_1(t) \geq V_0$, positive input current would occurs when $v_1(t) \leq 0 \& v_1(t) \leq -V_0$ and negative input current occurs. As a result, due to the zero regions of the input current as shown in Fig. 16.37C. The input current is distorted simply because the buck converter can work only under the condition when the input voltage is larger than the output voltage. Therefore, the basic buck converter cannot fulfill the requirement of a good candidate that can be used to achieve the DCM input PFC.

16.5.1.2 Boost Converter

The basic boost converter and its input current waveform are shown in Fig. 16.38A and B, respectively. This current can be presented by the following expression:

$$\begin{cases} i_1(t)=\dfrac{|v_1(t)|}{L}t & kT_s\le t\le kT_s+DT_s \\ i_1(t)=-\dfrac{V_0-|v_1(t)|}{L}(t-(D+D_1)T_s) & kT_s+DT_s\le t\le kT_s+(D+D_1)T_s \\ i_1(t)=0 & kT_s+(D+D_1)T_s\le t\le (k+1)T \end{cases} \tag{16.30}$$

The average instantaneous input current of the boost converter in one switching cycle is given as follows:

$$\begin{aligned} i_{1,\text{avg}}(t)&=\frac{1}{2}\cdot DT_s\frac{|v_1(t)|}{L}(D+D_1) \\ &=\frac{D^2T_s}{2L}\frac{|v_1(t)|V_0}{V_0-|v_1(t)|} \end{aligned} \tag{16.31}$$

where DT_s is the interval of time during which the inductor current increases from zero to the current peak and D_1T_s is the time during which the inductor current decreases from the current peak to zero.

The average line current or the average input current of the rectifier during one switching cycle is given as follows:

$$\begin{aligned} i_{l,\text{avg}}(t)&=\frac{D^2T_s}{2L}\frac{|v_1(t)|V_0}{V_0-|v_1(t)|}v_1(t)\ge 0 \\ i_{l,\text{avg}}(t)&=-\frac{D^2T_s}{2L}\frac{|v_1(t)|V_0}{V_0-|v_1(t)|}v_1(t)\le 0 \end{aligned} \tag{16.32}$$

By plotting Eq. (16.32), we obtain the input *I-V* characteristic curve as given in Fig. 16.35C. As we can see that as long as the output voltage is larger than the peak value of the line voltage in certain range, the relationship between $v_1(t)$ and $i_{1,\text{avg}}(t)$ is nearly linear. When the boost converter is connected to the line, it will draw almost sinusoidal average input current from the line, shown as in Fig. 16.38C [1].

Because of the above reasons, boost converter is comparably superior to most of the other converters when applied to do PFC. However, it should be noted that boost converter can operate properly only when the output voltage is higher than its input voltage. When low-voltage output is needed, a step-down DC-DC converter must be cascaded [1].

16.5.1.3 Buck-Boost Converter

Fig. 16.39A shows a basic buck-boost converter topology; its input current waveform is shown in Fig. 16.39B. This current can be presented by the following expression:

$$\begin{cases} i_1(t)=\dfrac{|v_1(t)|}{L}t & kT_s\le t\le kT_s+DT_s \\ i_1(t)=0 & kT_s+DT_s\le t\le (k+1)T_s \end{cases} \tag{16.33}$$

The averaged input current of this converter can be found according to Eq. (16.33) as follows:

$$i_{1,\text{avg}}(t)=\frac{D^2T_s}{2L}|v_1(t)| \tag{16.34}$$

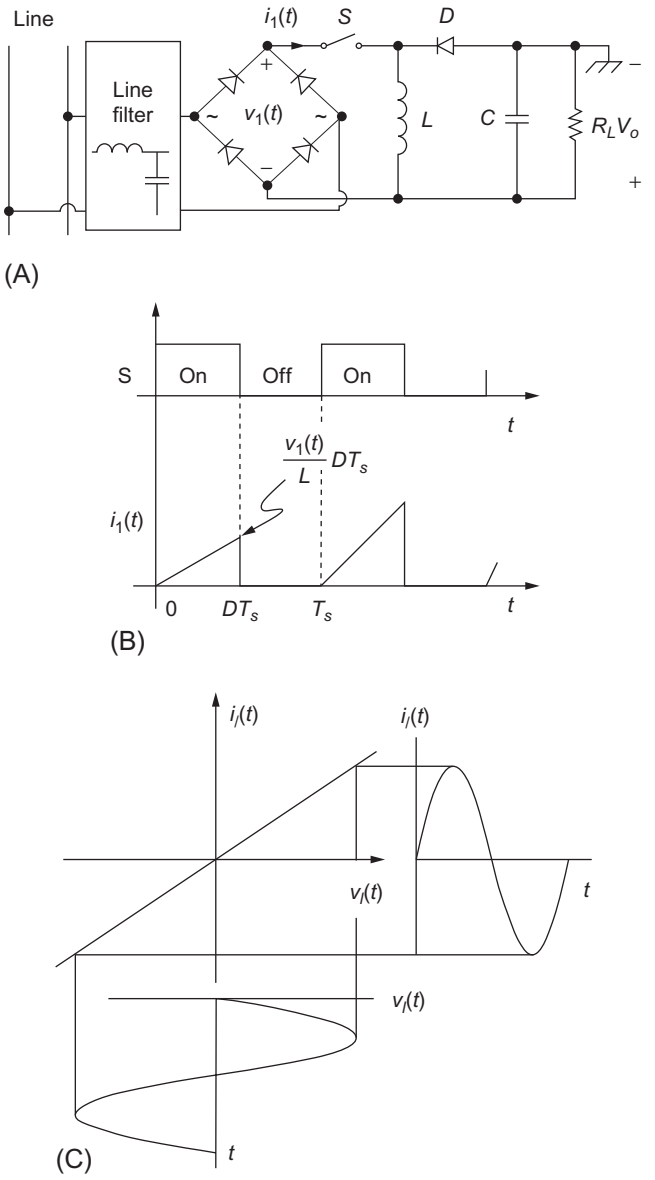


FIG. 16.39 Input *I-V* characteristic of basic buck-boost converter operating in DCM: (A) buck-boost converter, (B) input current, and (C) input *I-V* characteristic.

The average line current or the average input current of the rectifier during one switching cycle is given as follows:

$$i_{l,\text{avg}}(t)=\frac{D^2T_s}{2L}v_1(t) \tag{16.35}$$

Eq. (16.35) gives a perfect linear relationship between $i_{l,\text{avg}}(t)$ and $v_1(t)$, which proves that the buck-boost topology has an excellent automatic PFC property. It is obvious that the input current of this kind of converter is independent of the discharging behavior of the inductor. Its input *I-V* characteristics and input voltage and current waveforms are shown in Fig. 16.39C.

Furthermore, the main objective of the buck-boost converter is to ensure an output voltage that can be either higher or lower than the input voltage; in the same time and due to the continuous linear relationship between $i_{l,\text{avg}}(t)$ and $v_1(t)$ based on the DCM technique, this topology demonstrates strong availability to achieve a sine waveform of the input current and in phase with the input voltage that means a good PFC function.

Theoretically, buck-boost converter is a perfect candidate. Unfortunately, this topology has two limitations: (1) The polarity of its output voltage is reversed, that is, the input voltage and the output voltage cannot have the common ground, and (2) it needs floating drive for the power switch. The first limitation circumscribes this circuit into a very narrow scope of applications. As a result, it is not widely used [1].

16.5.1.4 Flyback Converter

Flyback converter is an isolated converter whose topology is presented in Fig. 16.40A; its input current waveform is shown in Fig. 16.40B, and it is presented by the following equation:

$$\begin{cases} i_1(t) = \dfrac{|v_1(t)|}{L_m} t & kT_s \le t \le kT_s + DT_s \\ i_1(t) = 0 & kT_s + DT_s \le t \le (k+1)T_s \end{cases} \tag{16.36}$$

It can be seen clearly that this current is similar to the buck-boost converter input current, where L_m is the magnetizing inductance of the output transformer. The averaged input current of this converter can be found according to Eq. (16.36) as follows:

$$i_{1,\text{avg}}(t) = \frac{D^2 T_s}{2L_m} |v_1(t)| \tag{16.37}$$

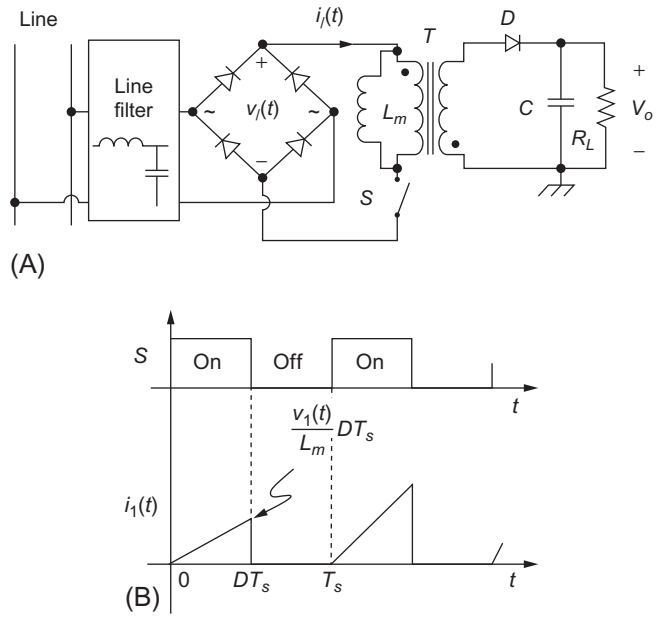


FIG. 16.40 Input *I-V* characteristic of basic flyback converter operating in DCM: (A) flyback converter and (B) input current.

The average line current or the average input current of the rectifier during one switching cycle is given as follows:

$$i_{l,\text{avg}}(t) = \frac{D^2 T_s}{2L_m} v_1(t) \tag{16.38}$$

Therefore, the flyback converter topology has the same input *I-V* characteristic as the buck-boost converter topology, and hence, it has the same input voltage and input current waveforms as shown in Fig. 16.40C.

Comparing with buck-boost converter, flyback converter has all the advantages of the buck-boost converter. What's more, input-output isolation can be provided by flyback converter. These advantages make flyback converter well suitable for PFC with DCM input technique. Comparing with boost converter, the flyback converter has better PFC, and the output voltage can be either higher or lower than the input voltage. However, due to the use of power transformer, the flyback converter has some drawbacks such as high d_i/d_t noise, lower efficiency, and lower density (larger size and heavier weight) [1].

16.5.1.5 Forward Converter

The forward converter topology is shown in Fig. 16.41. In order to avoid transformer saturation, it is well-known that forward converter needs the third winding to demagnetize (reset) the transformer.

The forward converter topology, when compared with the flyback topology, has the advantages of lower peak output current and less leakage energy-related problems; it is generally more energy efficient, and it is used for applications requiring little higher power output (in the range of 100–200 W). However, the circuit topology, especially the output filtering circuit, is not as simple as in the flyback converter, and when its basic

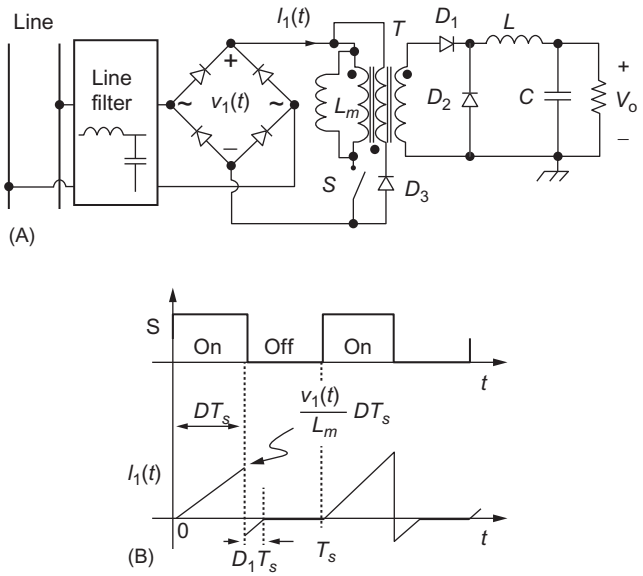


FIG. 16.41 (A) Forward converter and (B) input current waveform.

topology is connected to the rectified line voltage, the path of the demagnetizing current through the third winding is blocked by the rectifier bridge diodes during the turn-off period of the main switch *S*. Moreover, energy transfer to output ceases during the interval when the rectified input voltage $|v_1(t)|$ is lower than the reflected output voltage on the primary (i.e., $V_0 \cdot n_1/n_3$), resulting in distorted input current. Therefore, this basic topology cannot be used to achieve the PFC purpose unless a certain circuit modification is applied such as forward converter with a resistor-capacitor-diode (RCD) clamp circuit, the forward converter with an active clamp (FAC).

16.5.1.6 Cuk Converter and Sepic Converter

It can be shown that Cuk converter and Sepic converter given in Fig. 16.42A and B, respectively, have the same input *I-V* characteristic. Each of these converter topologies has two inductors, with one located at its input and the other at its output. Let's consider the case when the input inductor operates in DCM, while the output inductor operates in CCM. In this case, the capacitor C_1 can be designed with large value to balance the instantaneous input/output power, resulting in high PF in the input and low second-harmonic ripple in the output voltage. To investigate the input characteristic of these converters, let's take the Cuk converter as an example. One should note that the results from the Cuk converter are also suitable for Sepic converter [1].

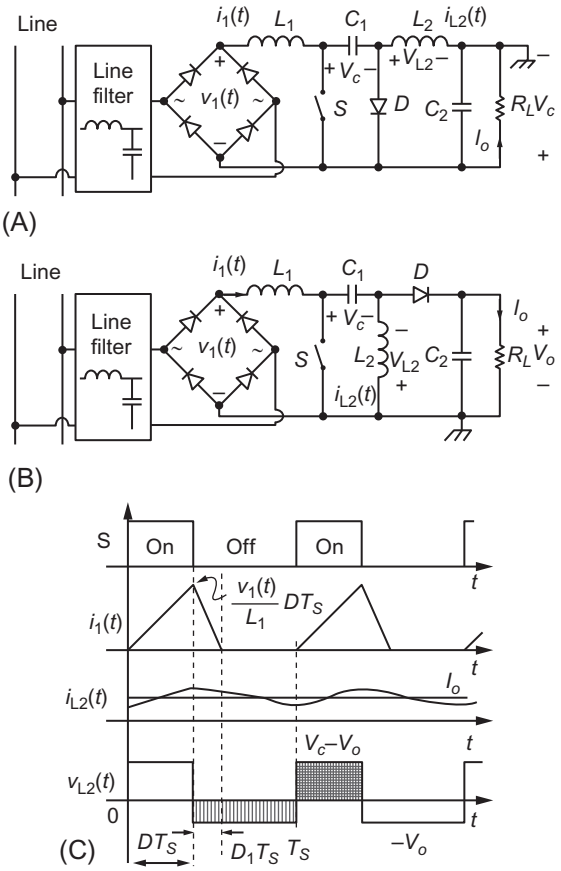


FIG. 16.42 Input *I-V* characteristic of basic Cuk converter and Sepic converter operating in DCM: (A) Cuk converter, (B) Sepic converter, and (C) typical waveforms of Cuk converter with input inductor operating in DCM.

For the Cuk converter shown in Fig. 16.42A, the waveforms for input inductor current (the same as the input current), output inductor current, and the voltage across the output inductor are depicted in Fig. 16.42C [1]. Assume that the capacitor C_1 is large enough to be considered as a voltage source V_c, in steady state, employing volt-second equilibrium principle on L_2, we obtain

$$V_C = \frac{1}{D} V_o \tag{16.39}$$

The input inductor current (the same as the input converter current) can be presented by the following expression:

$$\begin{cases} i_1(t) = \dfrac{|v_1(t)|}{L} t & kT_s \le t \le kT_s + DT_s \\ i_1(t) = -\dfrac{D|v_1(t)| - V_0}{DL}(t - (D+D_1)T_s) & kT_s + DT_s \le t \le kT_s + (D+D_1)T_s \\ i_1(t) = 0 & kT_s + (D+D_1)T_s \le t \le (k+1)T_s \end{cases} \tag{16.40}$$

The input inductor current reset time ratio D_1 is given by

$$D_1 = -\frac{D^2|v_1(t)|}{V_0 - D|v_1(t)|} \tag{16.41}$$

Therefore the averaged input current can be found as

$$\begin{aligned} i_{1,\text{avg}}(t) &= \frac{1}{2} \cdot DT_s \frac{|v_1(t)|}{L}(D+D_1) \\ &= \frac{D^2 T_s}{2L} \frac{|v_1(t)| V_0}{V_0 - D|v_1(t)|} \end{aligned} \tag{16.42}$$

It can be seen that Eq. (16.42) is very similar to Eq. (16.32) except that the denominator in the former equation is $(V_o - Dv_1(t))$ instead of $(V_o - v_1(t))$. This will lead to some improvement in that *I-V* characteristic in Cuk converter. Referring to the *I-V* characteristic shown in Fig. 16.38C, Cuk converter has a curve more close to a straight line. Such improvement, however, is achieved at the expense of using more circuit components. It can be proved that the same results can be obtained by the Sepic converter [1].

16.5.1.7 Zeta Converter

Fig. 16.43A gives a Zeta converter connected to the line. In DCM operation, the key waveforms are illustrated in Fig. 16.43B, where we presume the capacitor being equivalent to a voltage source V_c. As we can see that the converter input current waveform is exactly the same as that drawn by a buck-boost converter [1]. Thus, the instantaneous input current for

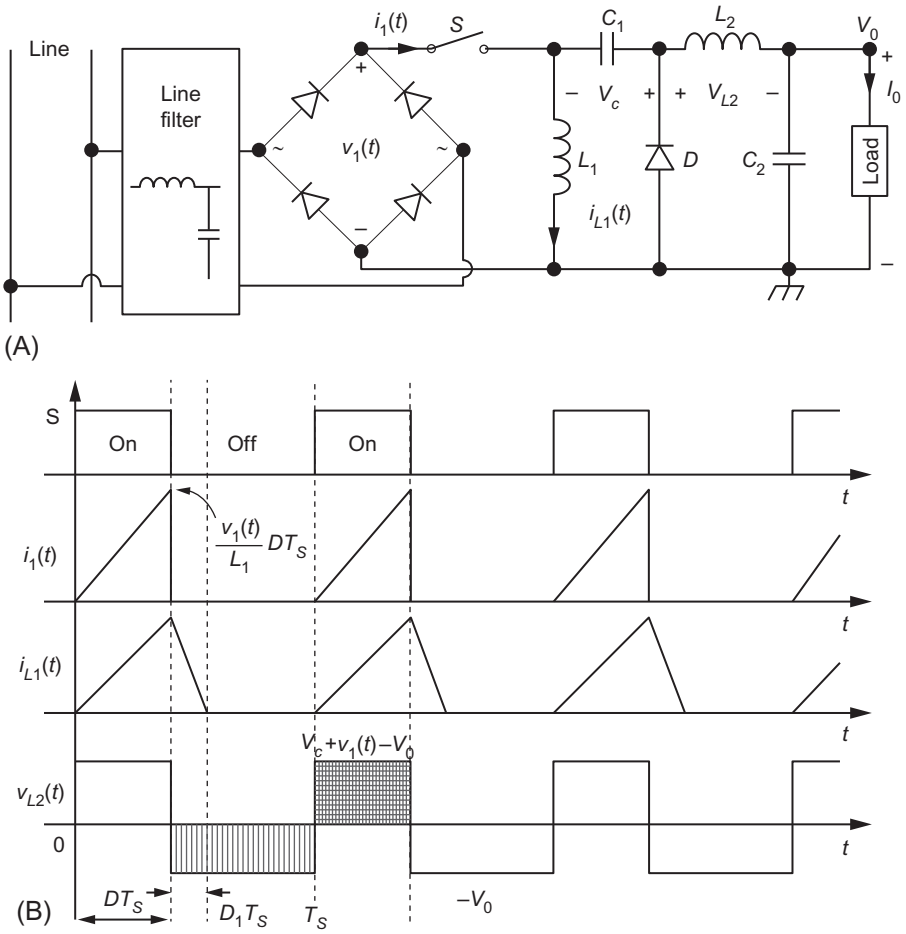


FIG. 16.43 Input *I-V* characteristic of basic Zeta converter operating in DCM: (A) Zeta converter and (B) typical waveforms of Zeta converter with input inductor operating in DCM.

the Zeta converter is identical to that for the buck-boost converter. It is expressed as follows:

$$\begin{cases} i_1(t) = \dfrac{|v_1(t)|}{L}t & kT_s \le t \le kT_s + DT_s \\ i_1(t) = 0 & kT_s + DT_s \le t \le (k+1)T_s \end{cases} \tag{16.43}$$

The averaged input current of this converter can be found according to Eq. (16.43) as follows:

$$i_{1,\text{avg}}(t) = \frac{D^2 T_s}{2L}|v_1(t)| \tag{16.44}$$

The average line current or the average input current of the rectifier during one switching cycle is given as follows:

$$i_{l,\text{avg}}(t) = \frac{D^2 T_s}{2L}v_1(t) \tag{16.45}$$

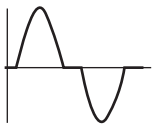
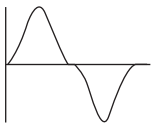
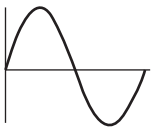
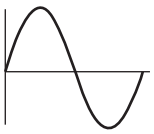
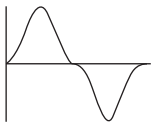
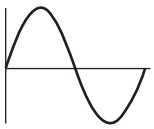
which is the same as the one given by Eq. (16.33). As a result, the Zeta converter has as good automatic PFC capability as the buck-boost converter. The improvement achieved here is the noninverted output voltage. However, like the buck converter, floating drive is required for the power switch [1].

Based on the above discussion, we may conclude that all the eight basic converters except forward converter have good inherent PFC capability and are available for DCM PFC usage. Among them, boost converter and flyback converter are especially suitable for single-stage PFC scheme because they have minimum component count and grounded switch drive, and their power switches are easy to be shared with the output DC-DC converter. Hence, these two converters are most preferable by the designers for PFC purpose. The other converters could also be used to perform certain function such as circuit protection and small output voltage ripple. The characteristics of the eight basic converter topologies are summarized in Table 16.2 [1].

16.5.1.8 Flyboost Converter

Unlike the aforementioned converter used for PFC applications, the flyboost converter was proposed in [96,97] to benefit simultaneously from the advantages of both flyback power transfer and boost power transfer. This proposed topology gains

TABLE 16.2 Comparison of basic converter topologies operating for DCM input technique

	Buck	Boost	Buck-boost	Flyback	Forward[a]	Cuk and Sepic	Zeta
Line current waveform					–		
Switch drive	Floating	Grounded	Floating	Grounded	Grounded	Grounded	Floating
Peak input current	High	Lower	High	High	—	Lower	High
Inrush and overload protection	Yes	No	Yes	Yes	—	Yes	Yes
Output voltage	$V_o < V_{l,m}$	$V_o > V_{l,m}$	Inverted	$V_o < V_{l,m}$ or $V_o > V_{l,m}$	—	$V_o < V_{l,m}$ or $V_o > V_{l,m}$; inverted for Cuk	$V_o < V_{l,m}$ or $V_o > V_{l,m}$
Power level	Low to medium	Low to medium	Low to medium	Low	—	Low to medium	Low to medium

[a]The standard forward converter is not recommended as a PF corrector since the rectifier at the input will block the demagnetizing current through the tertiary winding.

the features of the flyback and boost converter from point of view of power transfer process to achieve a unify PF and a very reduced input current harmonics. Indeed, it can be said that the difference of this topology from the basic topologies such as boost, SEPIC, buck-boost, Cuk, and buck is not so important; however, the operation principle is very different. It is obvious that there are only two operation modes for flyboost converter, the flyback mode and the boost mode. A derived flyboost converter topology has been used as shown in Fig. 16.44. It consists mainly of one switch, a flyboost transformer T_1, tow input transformer T_2, two capacitor, an output inductor, and six diodes [98,99]. This derived PFC topology has some advantages in comparison with other PFC topologies such as [96]

- one switch is used that means easy control implementation,
- high-performance capability for power transfer process,
- high PF and high efficiency,
- automatic clamping of the intermediate dc bus voltage within a desirable range,
- relatively low-voltage stress on power devices,
- capability to support input inrush and to ensure self-surge current protection,
- can be used in medium power level with low-cost.

16.5.2 AC-DC Power Supply with DCM Input Technique

In two-stage PFC power supply, the DCM converter is connected in front of the ac line to achieve high input PF and provide a roughly regulated dc bus voltage, as shown in Fig. 16.45. This stage is also known as "preregulator." The duty ratio of the preregulator should be maintained relatively stable so that high PF is ensured. To stabilize the dc bus voltage, a bank capacitor is

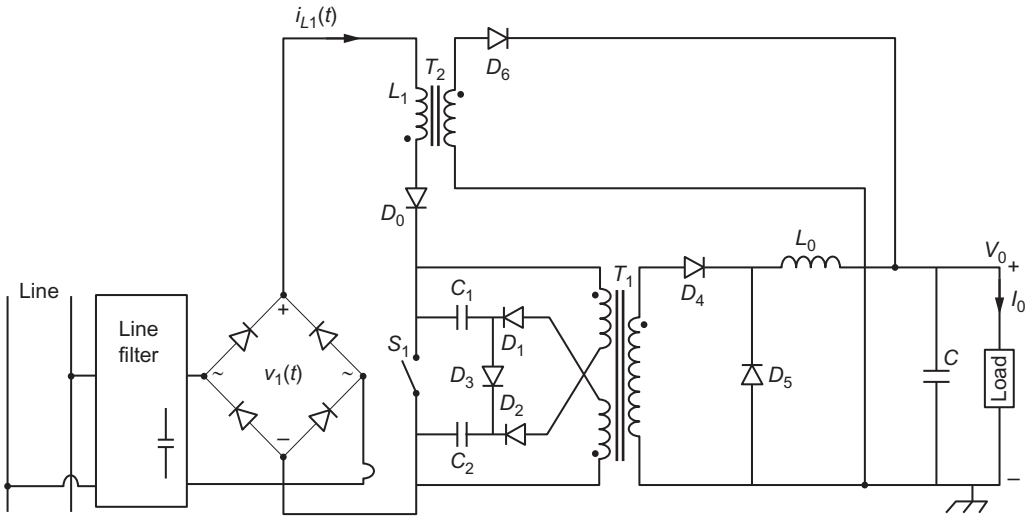


FIG. 16.44 The improved topology of the flyboost converter.

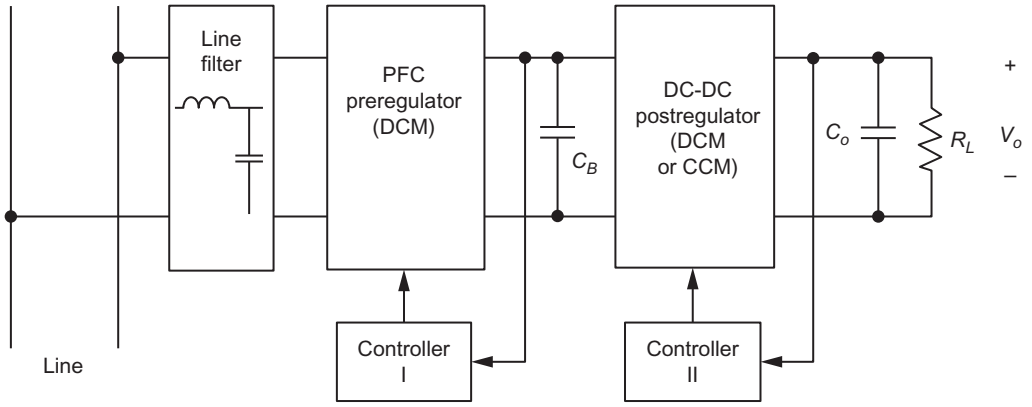


FIG. 16.45 DCM input preregulator in two-stage ac-dc power supply.

used at the output of the preregulator. The second stage, followed by the preregulator, is a DC-DC converter, called postregulator, with its output voltage being tightly controlled. This stage can operate either in DCM or in CCM. However, CCM is normally preferred to reduce the output voltage ripple [1].

DCM input technique has been widely used in one-stage PFC circuit configurations. Using a basic converter (usually boost or flyback converter) operating in DCM, combining it with another isolation converter can form a one-stage PFC circuit. A storage capacitor is generally required to hold the dc bus voltage in these combinations. Unlike the two-stage PFC circuit, in which the bus voltage is controlled, the single-stage PFC converter has only one feedback loop from the output. The input circuit and the output circuit must share the same control signal. In [100–102], a number of combinations have been studied. Figs. 16.46 and 16.47 show a few examples of successful combinations. Since the input circuit and the output circuit are in a single-stage, it is possible for them to share the same power switch. Thus it results in single-stage single-switch PFC (S_4-PFC) circuit, as shown in Fig. 16.47 [100,103,104,1].

The boost integrated with flyback rectifier/energy storage/dc-dc converter (BIFRED) and boost integrated with buck rectifier/energy storage/dc-dc converter (BIBRED) are two single-stage converters of the integrated high-quality rectifier-regulator (IHQRR) family that have been firstly presented by [103–106]. Both topologies are able to ensure an input current with a low harmonic content and, also, a regulated and isolated output voltage bus using only one switch. The two topologies of BIFRED and BIBRED are designed so that the input inductor and the output inductive element both operate in the DCM mode. It is obvious that BIFRED topology presents a strong similarity with the isolated version of the Sepic converter. Furthermore, the BIBRED topology resembles to the isolated version of the Cuk converter [107]. As it was explained, the two topologies of the BIFRED and BIBRED converters are composed of two integrated converters, where only one switch is used. The BIFRED converter is an integration of a discontinuous conduction mode (DCM) boost converter and a flyback converter. In the BIBRED, the corresponding parts are a DCM boost converter and a forward converter. Schematics of the BIFRED and BIBRED converters are shown in Fig. 16.47A and B, respectively.

Due to the simplicity and low-cost, DCM boost converter is most commonly used for unity PF operation. The main drawback of using boost converter is that it shows considerable distortion of the average line current owing to the slow discharging of the inductor after the switch is turned off [1].

The output DC-DC converter can operate either in DCM or in CCM if small output ripple is desired. If the output circuit operates in CCM, there exists a power unbalance in S^4-PFC converter when the load changes. Because the duty ratio is only sensitive to the output voltage in CCM operation, when the output power (output current) decreases, the duty ratio will keep unchanged. As both the input and the output circuit share the power switch, the input circuit will draw an unchanged power from the ac source. As a result, the input power is higher than the output power. The difference between the input power and the output power has to be stored in the storage capacitor, and hence, increase in the dc bus voltage occurs. With the dc bus voltage's rising, the duty ratio decreases. This process will be finished until a new power balance is built. As we can see, the new power balance is achieved at the penalty of increased voltage stress, resulting in high conduction losses in circuit components. Particularly, the high bus voltage causes difficulties in developing S^4-converter for universal input (input line voltage *rms* value from ac 90–260 *V*) application [1].

Recent research on solving this problem can be found in [108–116]. The circuit in [108] uses two bulk capacitors that share the dc bus voltage change, shown in Fig. 16.48A. As a result, lower voltage is present at each of the capacitor. Ref. [109] proposed a modified boost-forward PFC converter, in which a negative current feedback is introduced to the input circuit by the coupled windings of forward transformer, shown in Fig. 16.48B. In [110], a series resonant circuit called charge pump circuit is introduced into S^4-PFC circuit, shown in Fig. 16.48C. As the load decrease, the charge pump circuit can suppress the dc bus voltage automatically [1].

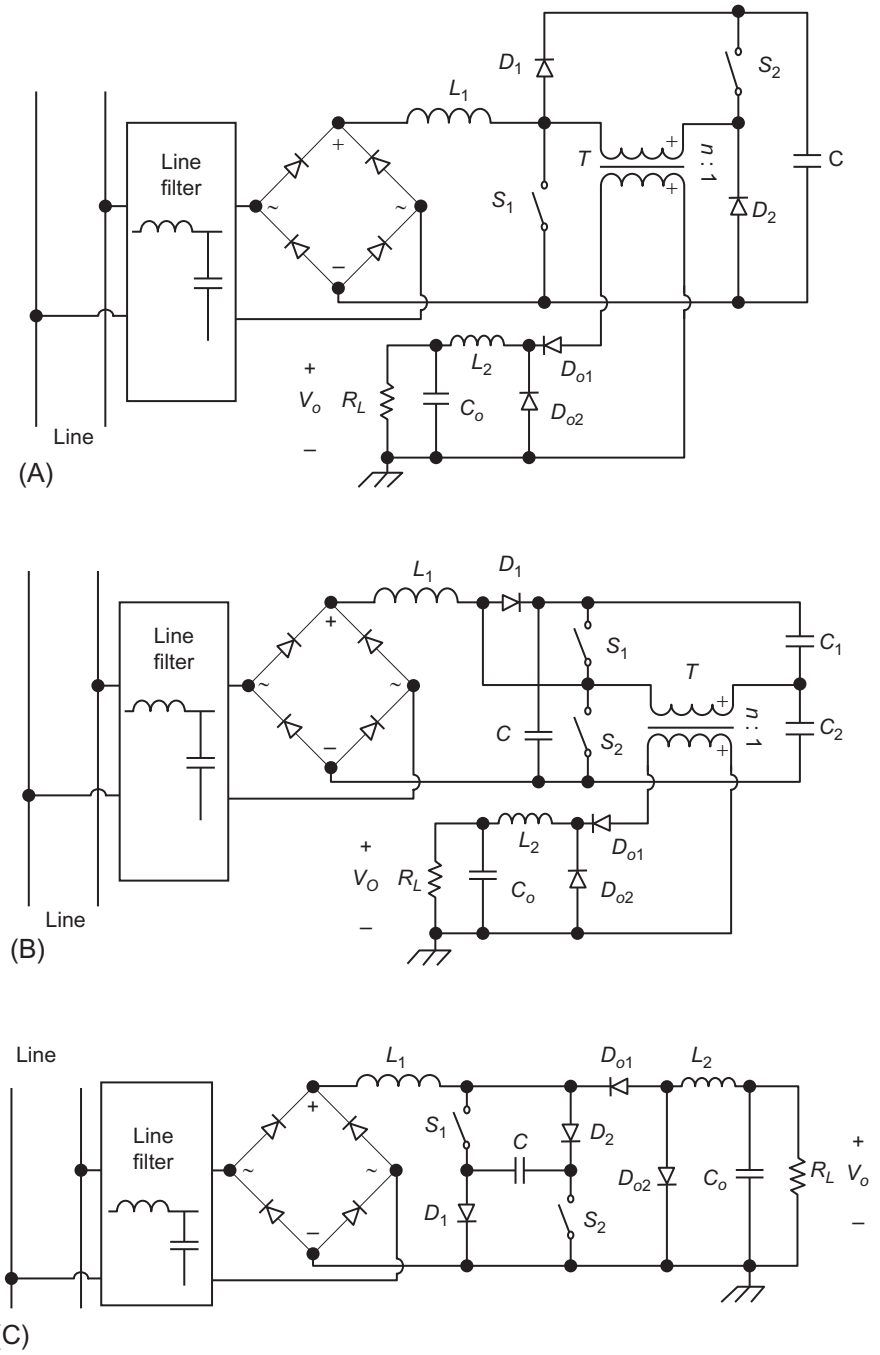


FIG. 16.46 Two-switch single-stage power factor corrector: (A) boost-forward converter, (B) boost-half-bridge converter, and (C) Sheppard-Taylor converter.

16.5.3 CRM Technique

In this control technique, the switch is turned on when the inductor current falls to zero (when it reaches the time axis), where the switch is kept on for a constant duration during the line cycle and the switch off duration is controlled by a given signal loop. It is clear that the converter operates at the boundary between the continuous and discontinuous current mode (CCM-DCM) [117,118]. It can be said that this type of control is a particular case of hysteretic control in which the lower current command is zero anywhere.

It was proved that the CRM technique has some interesting advantages when it is applied to the boost converter, where the line current is shaped to be sinusoid under COT control [117,119]. Unfortunately, the CRM technique when it is

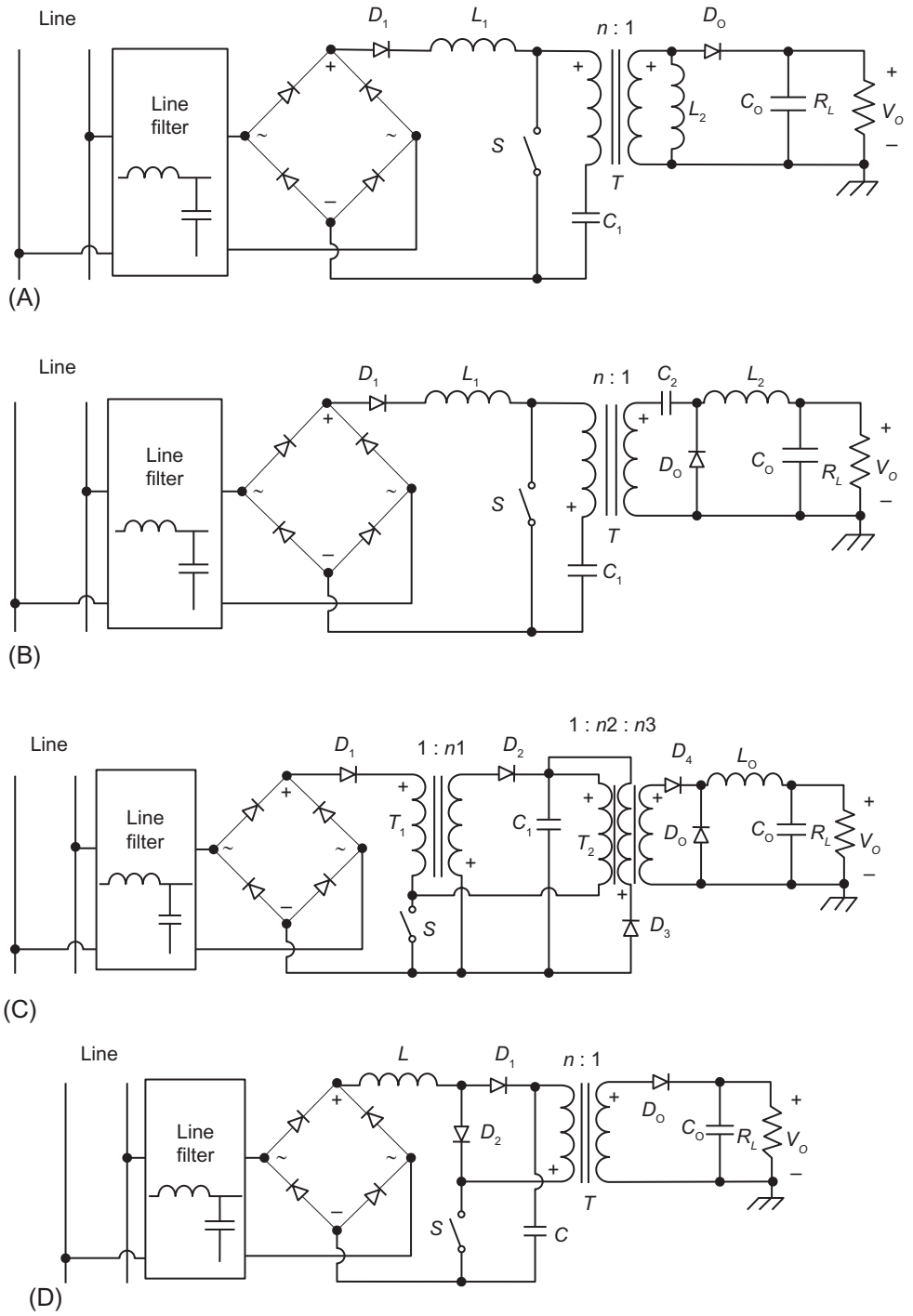


FIG. 16.47 Single-stage single-switch PFC circuit: (A) boost-flyback combination circuit (BIFRED), (B) boost-buck combination circuit (BIBRED), (C) flyback-forward combination, and (D) boost-flyback combination.

applied to the buck and flyback converters and their derived topologies such as buck-boost, Sepic, and Cuk under COT control leads to a somewhat distorted line current. Hence, the application of CRM technique to these kinds of converters will not allow to meet the PF and THD requirements within the known standards [117,119,120]. To overcome the drawbacks of the CRM control technique, variable on-time (VOT) control technique was proposed and applied to the buck PFC converter [121,122] to achieve high PF and low THD requirement given by the standards. In the same way, based on the input voltage,

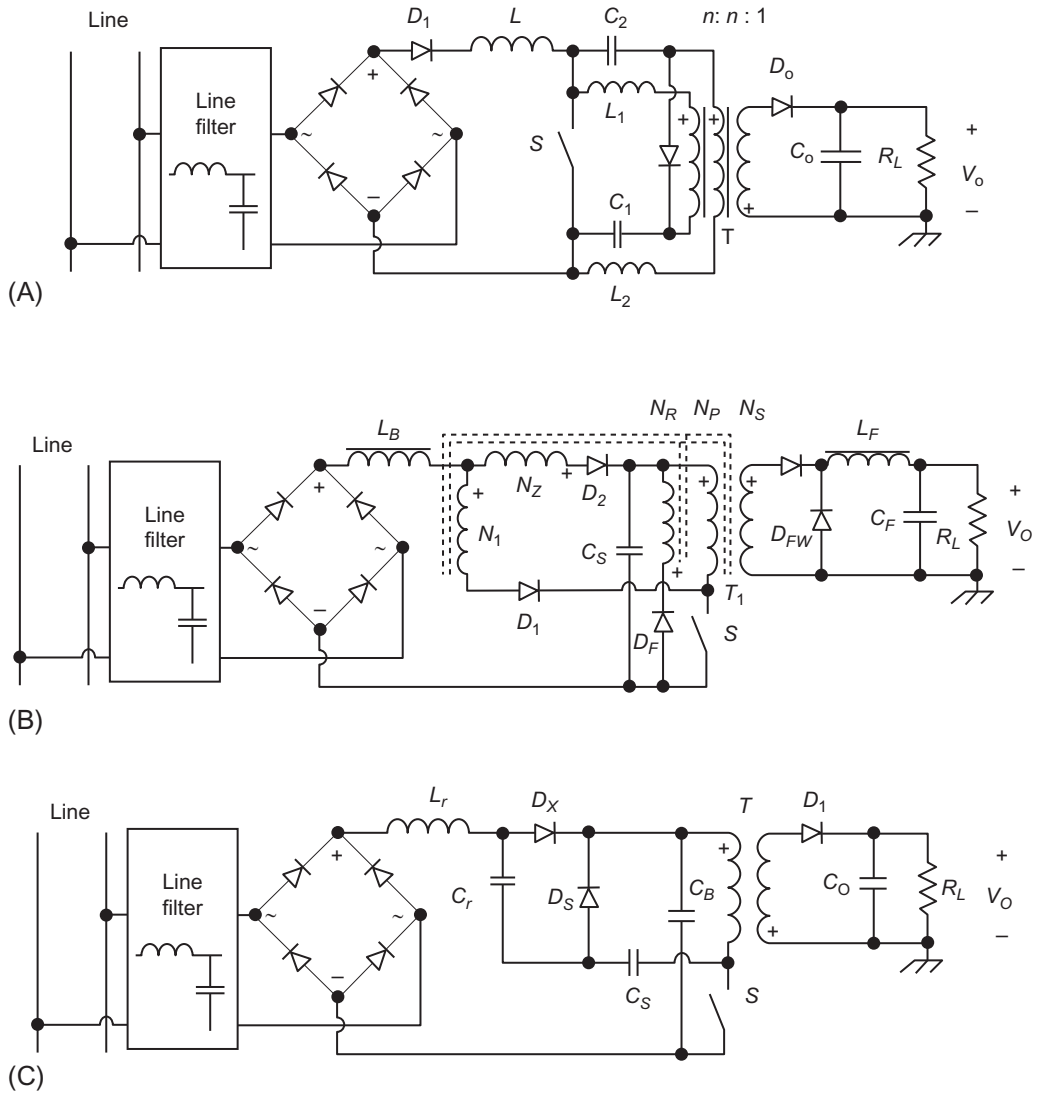


FIG. 16.48 Improved S^4-PFC converter: (A) boost-forward PFC circuit using two bulk capacitors, (B) boost-forward PFC circuit with reduced bus voltage, and (C) boost-flyback PFC circuit with charge pump circuit.

an improved CRM technique is applied on flyback PFC converter by modulating the turn-on time, However, as the output voltage is not used to modulate the on-time of the switch, when output voltage is varying under constant output current power supply, unity PF is very difficult to be ensured [123]. It is important to clarify that in this control technique, the inductor and switch peak currents are twice the ac system input current peak value. Therefore, the CRM technique is not suitable for high-power applications. However, the CRM technique is attractive in low-power applications such as the PFC for "electronic ballasts" where the following advantages can be achieved: (1) the switch can be easily oversized without increasing cost; (2) the switch operates under zero-current turn-on, avoiding turn-on losses and electromagnetic interference problems; and (3) the smaller sized inductor can be used to reduce the size and cost of the system.

16.5.4 Other PFC Techniques

Extensive research in PFC continues to yield countless new techniques [58,61,124–152]. The research topics are mainly focused on improvements of the PFC circuit performs such as fast performance, high efficiency, low-cost, small input current distortion, and output ripple. The classification of PFC techniques presented here can only cover those methods that are frequently documented in the open literature. There are still many PFC methods that do not fall into the specified categories. The following are some examples [1]:

- *Second-harmonic-injected method* [126]: In DCM input technique, even the converter operates at constant duty ratio, current distortion still exists. The basic idea of second-harmonic-injected method is compensating the duty ratio by injecting a certain amount of second-

harmonic into the duty ratio to modify the input *I-V* characteristic of the input converter. However, the output voltage may be affected by the modified duty ratio.

- *Cycle control technique* [127]: It is a new a method recently proposed for harmonics reduction in dc-dc converter that has the simplicity of voltage follower technique. In this technique, a periodic signal proportional to the rectified ac line voltage is used to modulate the duty-cycle of the power switch, where the main goal is to reduce the line current THD and to improve the PF; it offers the following advantages: (1) The generation of the injected signal is based on sensing the output voltage of the bridge rectifier that permits to have a simpler circuit without any additional circuit of phase detecting and phase synchronization, and (2) the modulation index can be used to obtain constant content of harmonics under a wide range of load variation, just with a simple PI controller, and (3) can have a good dynamic behavior under input voltage and load transients.
- *Interleaved method* [128]: An interleaved PFC circuit composed of several input converters in parallel. The peak input current of these converters follow the line voltage and are interleaved. A sinusoidal total line current is obtained by superimposing all the input current of the converters. The advantage of this method is that the converter input current can be easily smoothed by input EMI filter.
- *Waveform synthesis method* [129]: This method combines passive and active PFC techniques. Since the rectifier in the passive inductive-input PF corrector has a limited conduction angle, the input current is a single pulse around the peak of the line voltage, whereas the boost converter draws a nonzero current around the zero cross of the line voltage. By controlling the operation mode of the active switch (enable and disable the boost converter at certain line voltage), the waveforms of active and passive PFC circuits are tailored to extend the conduction angle of the rectifier. The resulting current waveform has a PF greater than 0.9 and a THD lower than 20%.
- *Digital PFC control technique* [130–152]: The digital control of PFC (DPFC) is expected to replace the analog PFC control, especially in medium- and high-power-level applications, due to its several advantages and to the great development in digital circuits. The main advantages of digital PFC control that push and motivate the application of the digital PFC control over other control techniques are mainly summarized in the following points [135]:
  a. Reduced sensitivity to circuits' parameter changes.
  b. Reduced of analog electronics components.
  c. An easy implementation of the controller.
  d. An easy adjustment of control parameters.
  e. An easy adaptation of the control against the changes of the measured or sensed variables.
  f. Digital controller is less expensive compared with the analog controller.
  g. Digital controller can be modified easily.

In this chapter, we are not focusing in digital PFC control; however, all the control techniques that have been presented in this chapter in DCM, CCM, and CRM modes can be furthermore extended to digital application for medium- and high-power-level applications (output power range between 200 and 2 kW) when high converter efficiency is desired. As an example, the following digital PFC control techniques have been already investigated:

1. Digital average current mode PFC control (DACM) [135–138]: In this PFC control, the instantaneous sensed variables of the rectified input voltage, the input/inductor current, and the output voltage are digitized. On the other side, a digital PWM (DPWM) is used for the output of the digital-current-loop compensator feeds, a DPWM that generates a discrete time gate driving waveform.
2. Predictive PFC control [139–141]: This control technique allows the computing of the next control value using the current sensed values based on the equations presenting the behavior of the concerned converter to fulfill the requirement of tracking the input reference current shape. The performance of this PFC control is depending on the used sampling frequency; therefore, under high sampling frequency, better result and performance are obtained.
3. Hybrid PFC control [135–146]: This control technique has several advantages that make it a very attractive technique. It is based on combining the digital and the analog techniques, where the analog technique is used for the current loop and the digital technique is used for the voltage loop. The HPFCC gains the merit of both techniques for obtaining improved performances for tracking the input current shape and the desired output voltage under ease and less cost of the hardware implementation, reduced control circuit, rapid dynamic response, and compacted topology.
4. Other digital PFC control techniques [135–152]: All the techniques mentioned in Sections 16.4 and 16.5 can be used under the digital PFC control technique and under the hybrid PFC technique, where in all case the main aim is that the technical advantages and economical advantages have to be respected during the design of the appropriated PFC control technique for the concerned converter topology and the level of the required power.

16.6 Summary

To reduce losses and decrease weight and size associated with converting ac power to dc power in linear power supply, SMPSs were introduced. The high nonlinearity of this kind of power

electronic systems that are connected to the power systems supply, handicaps itself by providing the utility power system with low PF and high THD. These unwanted harmonics are commonly corrected by incorporating PFC technique into the SMPS. This chapter gives a technical review of current research in high-frequency PFC, including the definition of PF and THD, configuration of PFC circuit, DCM input technique, CRM technique, and CCM shaping technique. The common issue of these techniques is to properly process the power flow so that the constant power dissipation at the output is reflected into ac power dissipation with two times the line frequency. Technically, PFC techniques encounter the following trade-offs:

(a) *Simplicity and accuracy*: Single-stage PFC circuit has simple topology and simple control circuit but has less control accuracy, while two-stage PFC circuit has the contrary performance.
(b) *Control simplicity and power-handling capability*: DCM input technique requires no input current control but has less power-handling capability, while CCM has multiloop control and has more power-handling capability;
(c) *Switching frequency and conversion efficiency*: To reduce weight and size of the PFC converter, higher switching frequency is desired. However, the associated switching losses result in decrease in conversion efficiency.
(d) *Frequency response and bandwidth*: To have good dynamic response, wider bandwidth is desired; however, to achieve high PF, bulk storage capacitor and output capacitor have to be used.

In the past decades, research in PFC techniques has led to the development of more efficient circuits and control strategies in order to optimize the design without compromising the above trade-offs. Moreover, since the growth in power electronics strongly relies on the development of semiconductor devices and the recent advent of higher rating power devices, it is believed that the switching-mode PF correctors will completely replace the existing passive reactive compensators in power system. In the distributed power system (DPS) where small size and high efficiency are of extreme importance, a new soft-switching technique has been used in designing PFC circuits. With the ever-increasing market demanding for ultrafast computer, the need for low output voltage (typically less than 1 *V*) with high output currents and high efficiency converters has never been greater. Research efforts in developing high-frequency high efficiency PFC circuits will continue to grow.

References

[1] I. Batarseh, H. Wei, Chapter One: Power factor correction circuits, Power Electronics Handbook, third ed., pp. 517–541.
[2] C.K. Duffey, R.P. Stratford, Update of harmonic Standard IEEE-519: IEEE recommended practices and requirements for harmonic control in electric power systems, IEEE Trans. Ind. Appl. 25 (6) (1989) 1025–1034.
[3] B.K. Bose, Power electronics—a technology review, Proc. IEEE 80 (1992) 1303–1334.
[4] H. Akagi, Trends in active power line conditioners, IEEE Trans. Power Electron. 9 (3) (1994) 263–268.
[5] W. McMurray, Power electronics in the 1990's, in: Proceedings of IEEE-IECON'90, 1990, pp. 839–843.
[6] A. McEachern, W.M. Grady, W.A. Moncrief, G.T. Heydt, M. McGranaghan, Revenue and harmonics: an evaluation of some proposed rate structures, IEEE Trans. Power Delivery 10 (1) (1995) 474–480.
[7] R. Redl, P. Tenti, J. Dan van Wyk, Power electronics' polluting effects, IEEE Spectr. 34 (5) (1997) 32–39.
[8] A. Kouzou, M.O. Mahmoudi, M.S. Boucherit, The space vector modulation PWM control methods applied on four leg inverters, in: Electric Machines and Drives, InTech, ISBN 978-953-307-548-8, 2011. Chapter 12.
[9] A. Kouzou, M.O. Mahmoudi, M.S. Boucherit, Evaluation of the Shunt Active Power Filter apparent power ratio using particle swarm optimization, Arch. Control Sci. 20 (1) (2010) 47–76.
[10] A. Kouzou, B.S. Khaldi, M.O. Mahmoudi, M.S. Boucherit, The effect of the zero sequence component on the evaluation of the series APF apparent power, Int. Rev. Electr. Eng. 4 (6) (2009) 1357–1366.
[11] A. Kouzou, B.S. Khaldi, M.O. Mahmoudi, M.S. Boucherit, The effect of the zero sequence component on the evaluation of the series APF apparent power, in: ICEEE 2008, The International Conference on Electrical Engineering, 2008.
[12] A. Kouzou, B.S. Khaldi, M.O. Mahmoudi, M.S. Boucherit, Apparent power evaluation of series active power filter with recent definitions, in: IEEE SSD'08, The Fifth International Multi-Conferences on Systems, Signals, and Devices, 2008.
[13] A. Kouzou, B.S. Khaldi, M.O. Mahmoudi, M.S. Boucherit, Shunt Active power filter apparent power for design process, in: SPEEDAM 2008 International Symposium on Power Electronics, Electrical Drives, 2008, pp. 1402–1408.
[14] A. Kouzou, B.S. Khaldi, M.O. Mahmoudi, M.S. Boucherit, Apparent power ratio of the shunt active power filter, in: EPE-PEMC 2008, The 13th International Power Electronics and Motion Control Conference, 2008, pp. 1987–1994.
[15] A. Kouzou, H. Abu Rub, M.O. Mahmoudi, M.S. Boucherit, R. Kennel, Four wire Shunt Active Power Filter based on four-leg inverter, in: International Aegean Conference on Electrical Machines and Power Electronics and Electromotion, Joint Conference (ACEMP), 2011, pp. 508–513.
[16] J.S. Lai, D. Hurst, T. Key, Switch-mode power supply power factor improvement via harmonic elimination methods, in: Conference Record of IEEE-APEC'91, 1991, pp. 415–422.
[17] IEEE, IEEE Guide for Harmonic Control and Reactive Compensation of Static Power Converters (IEEE Std. 519-1981), ANSI/IEEE, 1981.
[18] I.E.E.E. Inc, IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power systems (IEEE Std. 519-1992), ANSI/IEEE Inc., 1993.
[19] I. Batarseh, Power Electronic Circuits, John Wiley & Sons (in press).
[20] A.R. Prasad, P.D. Ziogas, S. Manias, A novel Passive wave-shaping method for single phase Diode Rectifiers, IEEE Trans. Ind. Electron. 37 (6) (1990) 521–530.

[21] S.B. Dewan, Optimum input and output filters for a single-phase rectifier power supply, IEEE Trans. Ind. Appl. IA-17 (3) (1981) 282–288.
[22] R.E. Tarter, Solid-State Power Conversion Handbook, John Wiley & Sons, 1993.
[23] P. Electronics Group, Input-current-Shaped Ac-to-Dc Converters: Final Report, NASA Lewis Research Center, California Institute of Technology, 1986.
[24] V. Vorperian, Simplified analysis of PWM converters using the model of the PWM switch: parts I and II, IEEE Trans. Aerosp. Electron. Syst. 26 (3) (1990) 490–505.
[25] K.I. Hwu, Y.T. Yau, L. Li-Ling, Powering LED using high-efficiency SR flyback converter, IEEE Trans. Ind. Electron. 47 (1) (2011) 376–386.
[26] J. Garcia, M.A. Dalla-Costa, A. Andre Luis Kirsten, D. Gacio, A. Calleja, A novel flyback-based input PFC stage for electronic ballasts in lighting applications, in: Proceedings of the IEEE Industry Applications Society Annual Meeting (IAS), October 2011, 2011, pp. 1–6.
[27] M. Hao, J. Yue, X. Ye, Design and analysis of single-stage power factor correction converter with a feedback winding, IEEE Trans. Power Electron. 25 (6) (2010) 1460–1470.
[28] Z. Jun, D.D.C. Lu, S. Ting, Flyback-based single-stage power-factor-correction scheme with time-multiplexing control, IEEE Trans. Ind. Electron. 57 (3) (2010) 1041–1049.
[29] H.J. Chiu, Y.K. Lo, H.C. Lee, et al., A single-stage soft-switching flyback converter for power-factor-correction applications, IEEE Trans. Ind. Electron. 57 (6) (2010) 2187–2190.
[30] H.S. Athab, D.D.C. Lu, K. Ramar, A single-switch AC/DC flyback converter using a CCM/DCM quasi-active power factor correction front-end, IEEE Trans. Ind. Electron. 59 (3) (2012) 1517–1526.
[31] J. Duarte, L.R. Lima, L. Oliveira, M. Mezaroba, L. Michels, C. Rech, Modeling and digital control of a single-stage step-up/down isolated PFC rectifier, IEEE Trans. Ind. Inf. 9 (2) (2013) 1017–1028.
[32] X. Xie, J. Li, K. Peng, C. Zhao, Q. Lu, Study on the single-stage forward-flyback PFC converter with QR control, IEEE Trans. Power Electron. 31 (1) (2016) 430–442.
[33] D. Gacio, J. Marcos Alonso, A.J. Calleja, J. García, M. Rico-Secades, A universal-input single-stage high-power-factor power supply for HB-LEDs based on integrated buck–flyback converter, IEEE Trans. Ind. Electron. 58 (2) (2011).
[34] M.A. Dalla Costa, J.M. Alonso, J.C. Miranda, D.G. Lamar, A single-stage high power factor electronic ballast based on integrated buck flyback converter to supply metal halide lamps, IEEE Trans. Ind. Electron. 55 (3) (2008) 1112–1122.
[35] H.F. Liuand, L.K. Chang, Flexible and low cost design for a flyback AC/DC converter with harmonic current correction, IEEE Trans. Power Electron. 20 (1) (2005) 17–24.
[36] J.Y. Leeand, M.J. Youn, A single-stage power factor correction converter with simple link voltage suppressing circuit (LVSC), IEEE Trans. Ind. Electron. 48 (3) (2001) 572–584.
[37] J.J. Lee, J.M. Kwon, E.H. Kim, W.Y. Choi, B.H. Kwon, Single-stage single-switch PFC flyback converter using a synchronous rectifier, IEEE Trans. Ind. Electron. 55 (3) (2008) 1352–1365.
[38] D.G. Lamar, M. Arias, A. Rodriguez, A. Fernandez, M. M. Hernando, J. Sebastian, Design-oriented analysis and performance evaluation of a low-cost high-brightness LED driver based on flyback power factor corrector, IEEE Trans. Ind. Electron. 60 (7) (2013) 2614–2626.
[39] K.-W. Siu, Y.-S. Lee, A novel high-efficiency flyback power-factor-correction circuit with regenerative clamping and soft switching, IEEE Trans. Circuits Syst. I, Fundam. Theory Appl. 47 (3) (2000) 350–356.
[40] S. Buso, G. Spiazzi, D. Tagliavia, Simplified control technique for high-power-factor flyback Cuk and Sepic rectifiers operating in CCM, IEEE Trans. Ind. Appl. 36 (5) (2000) 1413–1418.
[41] J. Zhang, H. Zeng, T. Jiang, A primary-side control scheme for high-power-factor LED driver with TRIAC dimming capability, IEEE Trans. Power Electron. 27 (11) (2012) 4619–4629.
[42] J.J. Zheng, A. Shteynberg, D. Zhou, J. McCreary, A novel multi-mode digital control approach for single-stage flyback power supplies with power factor correction and fast output voltage regulation, in: Proceedings of the IEEE APEC, March 2005, 2005, pp. 830–836.
[43] L. Yu-Kang, K. Tsu-Shou, L. Jing-Yuan, Analysis and design of an interleaved active-clamping forward converter, IEEE Trans. Ind. Electron. 54 (4) (2007) 2323–2332.
[44] W. Xinke, Y. Jianyou, Z. Junming, Q. Zhaoming, Variable on-time (VOT)-controlled critical conduction mode buck PFC converter for high-input AC/DC HB-LED lighting applications, IEEE Trans. Power Electron. 27 (11) (2012) 4530–4539.
[45] X. Xiaogao, Z. Chen, L. Qiang, L. Shirong, A novel integrated buck-flyback nonisolated PFC converter with high power factor, IEEE Trans. Ind. Electron. 60 (12) (2013) 5603–5612.
[46] H.E. Tacca, Power factor correction using merged flyback-forward converters, IEEE Trans. Power Electron. 15 (4) (2000) 585–594.
[47] V.N. Shet, A high power factor forward flyback converter with input current waveshaping, in: Proceedings of the IEEE Power Electronics, Drives and Energy Systems (PEDES), December 2006, 2006, pp. 1–6.
[48] C. Yoon, K. Moon-Hwan, H. Sang-Kyoo, K. Jeong-il, High efficiency and high power factor single-stage balanced forward-flyback converter, in: Proceedings of the IEEE IECON, November 2013, 2013, pp. 822–827.
[49] A. Tsu-Hua, L. Tsorng-Juu, C. Jiann-Fuh, Line ripple suppressed flyback-forward converters with power factor correction, in: IEEE Proceedings of the 4th Power Electronics and Drive Systems (PEDS), October 2001, 2001, pp. 152–156.
[50] K. Jung-Min, C. Woo-Young, K. Bong-Hwan, Single-switch quasi-resonant converter, IEEE Trans. Ind. Electron. 56 (4) (2009) 1158–1163.
[51] D. Vinnikov, I. Roasto, R. Strzelecki, M. Adamowicz, Two-stage quasi-Z-source network based step-up DC/DC converter, in: IEEE International Symposium on Industrial Electronics, 4–7 July 2010, 2010, pp. 1143–1148.
[52] D. Vinnikov, I. Roasto, T. Jalakas, An improved high-power DC/DC Converter for distributed power generation, in: 10th International Conference on Electrical Power Quality and Utilisation (EPQU 2009), 15–17 September 2009, 2009, pp. 1–6.
[53] C. Honnyong, F.Z. Peng, Y. Dongwook, Z-source resonant DC-DC converter for wide input voltage and load variation, in: 2010 International Power Electronics Conference (IPEC), 21-24 June 2010, 2010, pp. 995–1000.
[54] Q. Trong Nha, C.-Y. Lin, M. Mahmood Alamn, Y.-K. Lo, H.-J. Chiu, Implementation of a single-stage quasi Z-source AC-DC Power Factor Correction converter, in: International Conference on Anti-Counterfeiting, Security and Identification (ASID), 2012.

[55] Q. Trong Nha, H.-J. Chiu, Y.-K. Lo, P. Phu Hieu, M. Mahmood Alam, Isolated quasi Z-source bridgeless power factor correction with coupled inductor, in: The 1st International Future Energy Electronics Conference (IFEEC), 2013, 3–6 November 2013, 2013.
[56] M.O. Eissa, S.B. Leeb, G.C. Verghese, A.M. Stankovic, A fast analog controller for a unity-power-factor AC/DC converter, in: Conference Record of APEC'94, 1994, pp. 551–555.
[57] R. Liu, I. Batarseh, C.Q. Lee, Resonant power factor correction circuits with resonant capacitor-voltage and inductor-current-programmed controls, in: Conference Record of IEEE-APEC'93, 1993, pp. 675–680.
[58] K.W. Rustom, Steady state and dynamic analysis and optimization of single-stage-power factor correction converters, Department of Electrical Engineering and Computer Science in the College of Engineering and Computer Science at the University of Central Florida, Orlando, FL, 2007. PhD thesis.
[59] N. Vazquez, C. Hernandez, R. Cano, J. Antonio, E. Rodriguez, J. Arau, An efficient single-switch voltage regulator, in: Power Electronics Specialists Conference, vol. 2, 2002, pp. 811–816.
[60] C.K. Se, M.H.L. Chow, M.K.H. Cheung, A family of PFC voltage regulator configurations with reduced redundant power processing, IEEE Trans. Power Electron. 16 (2001) 794–802.
[61] J. Sebastian, P.J. Villegas, F. Nuno, O. Garcia, J. Arau, Improving dynamic response of power-factor preregulators by using two-input high-efficient postregulators, IEEE Trans. Power Electron. 12 (1997) 1007–1016.
[62] O. Garcia, J.A. Cobos, R. Prieto, P. Alou, J. Uceda, A new approach for single-stage AC/DC power factor correction converters with an improved energy processing, in: Power Electronics Specialists Conference, vol. 2, 1998.
[63] O. Garcia, J.A. Cobos, R. Prieto, P. Alou, J. Uceda, Simple AC/DC converters to meet IEC 1000-3-2, in: Applied Power Electronics Conference and Exposition, vol. 1, 2000, pp. 487–493.
[64] J.Y. Lee, Single-stage power factor correction converter with parallel power processing for wide line and load changes, Electron. Lett. 38 (2002) 421–423.
[65] S. Kim, P.N. Enjeti, A parallel-connected single phase power factor correction approach with improved efficiency, IEEE Trans. Power Electron. 19 (1) (2004) 87–93.
[66] Y. Jiang, F.C. Lee, Single-stage single-phase parallel power factor correction scheme, in: Conference Record IEEE-PESC'94, 1994, pp. 1145–1151.
[67] Y. Jiang, G.C. Hua, W. Tang, F.C. Lee, A novel single-phase power factor correction scheme, in: Proceedings of the IEEE Applied Power Electronics Conference, 1993, pp. 287–292.
[68] M. Mrozek, Power factor correction algorithm in AC-DC converter, Problemy Eksploatacj J. 2 (2013) 129–138.
[69] J. Baek, J. Shin, P. Jang, B. Cho, A critical conduction mode bridgeless flyback converter, in: 8th International Conference on Power Electronics—ECCE Asia May 30-June 3, 2011, The Shilla Jeju, Korea, 2011.
[70] L. Dixon, Average current mode control of switching power supplies, Product & Applications Handbook 1993–94, Unitrode Integrated Circuits Corporation, 1993. U140 pp. 9-457–9-470.
[71] L. Dixon, High power factor switching preregulator design optimization, in: Unitrode Power Supply Design Seminar, Sem-1000, 1994, pp. I3-1–I-12.
[72] J.P. Noon, D. Dalal, Practical design issues for PFC circuits, in: Conference Record of APEC'97, 1997, pp. 51–58.
[73] B. Mammano, Average current-mode control provides enhanced performance for a broad range of power topologies, in: PCIM'92-Power Conversion, September 1992, 1992, pp. 205–213.
[74] Y. Yan, F.C. Lee, P. Mattavelli, P.-H. Liu, I2 average current mode control for switching converters, in: IEEE Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual, 2013, pp. 229–236.
[75] S. He, R.M. Nelms, Digital I2 average current mode control for switch-mode power supplies, in: IEEE Applied Power Electronics Conference and Exposition (APEC), Charlotte, NC, USA, 2015, pp. 628–634.
[76] J.P. Gegner, C.Q. Lee, Linear peak current mode control: a simple active power factor correction control technique for continuous conduction mode, in: Conference Record of IEEE-PESC'96, 1996, pp. 196–202.
[77] R. Redl, B.P. Erisman, Reducing distortion in peak-current-controlled boost power-factor corrector, in: Conference Record of IEEE-APEC'94, 1994, pp. 576–583.
[78] C.A. Caneson, I. Barbi, Analysis and design of constant-frequency peak-current-controlled high-power-factor boost rectifier with slope compensation, in: Conference Record of IEEE-APEC'96, 1996, pp. 807–813.
[79] A.R. Prasad, P.D. Ziogas, S. Manias, A new active power factor correction method for single-phase buck-boost AC-DC converter, in: Conference Record of IEEE-APEC'92, 1992, pp. 814–820.
[80] A.V. Costa, C.H.G. Treviso, L.C. Freitas, A new ZCS-ZVS-PWM boost converter with unit power factor operation", in: Conference Record of IEEE-APEC'94, 1994, pp. 404–410.
[81] J. Mahdavi, M. Tabandeh, A.K. Shahriari, Comparison of conducted RFI emission from different unity power factor AC/DC converters, in: Conference Record of IEEE-PESC'96, 1996, pp. 1979–1985.
[82] J.C. Salmon, Techniques for minimizing the input current distortion of current-controlled single-phase boost rectifiers, IEEE Trans. Power Electron. 8 (4) (1993) 509–520.
[83] R. Srinivasan, R. Oruganti, A unity power factor converter using half-bridge boost topology, IEEE Trans. Power Electron. 13 (3) (1998) 487–500.
[84] I. Barbi, S.A. Oliveira da Silva, Sinusoidal line current rectification at unity power factor with boost quasi-resonant converters, in: Conference Record of APEC'90, 1990, pp. 553–562.
[85] M. Kazerani, P.D. Ziogas, G. Joos, A novel active current waveshaping technique for solid-state input power factor conditioners, IEEE Trans. Ind. Electron. 38 (1) (1991) 72–78.
[86] H.Y. Wu, C. Wang, K.W. Yao, J.F. Zhang, High power factor single-phase AC/DC converter with DC biased hysteresis control technique, in: Conference Record of IEEE-APEC'97, 1997, pp. 83–93.
[87] W. Tang, F.C. Lee, R. Ridley, I. Cohen, Charge control: modeling, analysis and design, in: Conference Record of IEEE-PESC'92, 1992, pp. 503–511.
[88] W. Tang, C.S. Leu, F.C. Lee, Charge control for zero-voltage-switching multiresonant converter, IEEE Trans. Power Electron. 11 (2) (1996) 270–274.
[89] R. Watson, G.C. Hua, F.C. Lee, Characterization of an active clamp flyback topology for power factor correction applications, in: Conference Record of IEEE-APEC'94, 1994, pp. 412–418.
[90] D. Maksimovic, Y. Jang, R. Erickson, 635–641, Nonlinear-carrier control for high power factor boost rectifiers, in: Conference Record of APEC'95, 1995, pp. 635–641.

[91] R. Zane, D. Maksimovic, Nonlinear-carrier control for high-power-factor rectifiers based on flyback, Cuk or sepic converters, in: Conference Record of APEC'96, 1996, pp. 814–820.
[92] H.Y. Wu, X.M. Yuan, J.F. Zhang, W.X. Lin, Single-phase unity power factor current-source rectifiction with buck-type input, in: Conference Record of IEEE-PESC'96, 1996, pp. 1149–1154.
[93] R. Oruganti, M. Palaniapan, Inductor voltage controlled variable power factor buck-type Ac-Dc converter, in: Conference Record of IEEE-PESC'96, 1996, pp. 230–237.
[94] S.M. Cuk, Modeling, Analysis, and Design of Switching Converters, Ph.D. dissertation, California Institute of Technology, 1977.
[95] A. Kulshreshtha, A.R. Saxena, A.K. Wadhwani, Average current control of DC-DC Cuk converters as power factor corrector, Int. J. Eng. Res. Appl. 5 (5(Part-1)) (2015) 56–61.
[96] S. Luo, W. Qiu, W. Wu, I. Batarseh, Flyboost power factor correction cell and a new family of single-stage AC/DC converters, IEEE Trans. Power Electron. 20 (1) (2005).
[97] S. Luo, W. Qiu, W. Wu, B. Issa, Flyboost power factor correction cell and its applications in single-tage ac/dc converters, in: Proceedings of the IEEE PESC'02 Conference, 2002, pp. 1375–1380.
[98] R. Redl, Power factor correction in single-phase switching-mode power supplies—an overview, Int. J. Electron. 77 (5) (1994) 555–582.
[99] H. Weiand, I. Bartarseh, et al., A single-switch ac/dc converter with power factor correction, IEEE Trans. Power Electron. 15 (3) (2000) 421–430.
[100] R. Redl, L. Balogh, N.O. Sokal, A new family of single-stage isolated power-factor correctors with fast regulation of the output voltage, in: Conference Record of IEEE-PESC'94, 1994, pp. 1137–1144.
[101] T.F. Wu, T.H. Yu, Y.C. Liu, Principle of synthesizing single-stage converters for off-line applications, in: Conference Record of IEEE-APEC'98, 1998, pp. 427–433.
[102] M. Berg, J.A. Ferreira, A family of low EMI, unity power factor correctors, in: Conference Record of IEEE-PECS'96, 1996, pp. 1120–1127.
[103] M. Madigan, R. Erickson, E. Ismail, Integrated high-quality rectifier-regulators, in: Conference Record of IEEE-PESC'92, 1992, pp. 1042–1051.
[104] P. Kornetzky, H. Wei, I. Batarseh, A novel one-stage power factor correction converter, in: Conference Record IEEE-APEC'97, 1997, pp. 251–258.
[105] Q. Li, F.C. Lee, Design consideration of the active-clamp forward converter with current mode control during large-signal transient, IEEE Trans. Power Electron. 18 (4) (2003) 958–965.
[106] M.T. Madigan, R.W. Erickson, E.H. Ismail, Integrated high-quality rectifier-regulators, IEEE Trans. Ind. Electron. 46 (4) (1999) 749–758.
[107] V. Tuomainen, Low-Power PFC and Forward Converters Methods to Improve Performances, The Department of Electrical and Communications Engineering, Helsinki University of Technology, Espoo, Finland, 2004 Dissertation for the degree of Doctor of Science.
[108] P. Kornetzky, H. Wei, G. Zhu, I. Bartarseh, A single-switch Ac/Dc converter with power factor correction, in: Conference. Record IEEE-PESC'97, 1997, pp. 527–535.
[109] L. Huber, M.M. Jovanovic, Single-stage, single-switch, isolated power supply technique with input-current shaping and fast output-voltage regulation for universal input-voltage-range applications, in: Conference Record IEEE-APEC'97, 1997, pp. 272–280.
[110] J. Qian, Q. Zhao, F.C. Lee, Single-stage single-switch power factor correction (S4-PFC) AC/DC converters with DC Bus voltage feedback for universal line applications, in: Conference Record of IEEE-APEC'98, 1998, pp. 223–229.
[111] J. Qian, F.C. Lee, A high efficient single stage single switch high power factor AC/DC converter with universal input, in: Conference Record IEEE-APEC'97, 1997, pp. 281–287.
[112] R. Redl, Reducing distortion in boost rectifiers with automatic control, in: Conference Record of IEEE-APEC'97, 1997, pp. 74–80.
[113] Y.S. Lee, K.W. Siu, Single-switch fast-response switching regulators with unity power factor, in: Conference Record of IEEE-APEC'96, 1996, pp. 791–796.
[114] M.M. Jovanovic, D.M.C. Tsang, F.C. Lee, Reduction of voltage stress in integrated high-quality rectifier-regulators by variable-frequency control, in: Conference Record of IEEE-APEC'94, 1994, pp. 569–575.
[115] Q. Li, F.C. Lee, M.M. Jovanovic, Large-signal transient analysis of forward converter with active-clamp reset, IEEE Trans. Power Electron. 17 (1) (2002) 15–24.
[116] J. Wang, W.G. Dunford, K. Mauch, A fixed frequency, fixed duty cycle boost converter with ripple free input inductor current for unity power factor operation, in: Conference Record of IEEE-PESC'96, 1996, pp. 1177–1183.
[117] J.-S. Lai, D. Chen, Design consideration for power factor correction boost converter operating at the boundary of continuous conduction mode and discontinuous conduction mode, in: Proceedings of the Applied Power Electronics Conference and Exposition, H. Discontinuous current PWM control, 1993, pp. 267–273.
[118] K. Georgakas, A. Safacas, Power factor correction and efficiency investigation of AC–DC converters using forced commutation techniques, in: ISIE Conference, Dubrovnik, June 20–23, 2005, 2005.
[119] T. Yan, J. Xu, F. Zhang, J. Sha, Z. Dong, Variable on-time controlled critical conduction mode flyback PFC converter, IEEE Trans. Ind. Electron. 61 (11) (2014) 6091–6099.
[120] C. Adragna, "Design equations of high-power-factor flyback converters based on the L6561," ST Application Note, 2003.
[121] A.J. Sabzali, E.H. Ismail, M.A. Al-Saffar, A.A. Fardoun, A new bridgeless PFC Sepic and Cuk rectifiers with low conduction and switching losses, in: Proceedings of the Power Electronics and Drive Systems, 2009, pp. 550–556.
[122] X. Wu, J. Yang, J. Zhang, Z. Qian, Variable on-time (VOT)-controlled critical conduction mode buck PFC converter for high-input AC/DC HB-LED lighting applications, IEEE Trans. Power Electron. 27 (11) (2012) 4530–4539.
[123] Y. Wang, Y. Zhang, Q. Mo, M. Chen, Z. Qian, An improved control strategy based on multiplier for CRM flyback PFC to reduce line current peak distortion, in: Proceedings of the IEEE Energy Conversion Congress and Exposition, September 2010, 2010, pp. 901–905.
[124] J. Sebastian, P. Villegas, F. Nuno, M.M. Hernando, Very efficient two-input DC-to-DC switching post-regulators, in: Conference Record IEEE-PESC'96, 1996, pp. 874–880.
[125] J. Hwang, A. Chee, Improving efficiency of a pre-/post-switching regulator (PFC/PWM) at light loads using green-mode function, in: Conference Record IEEE-APEC'98, 1998, pp. 669–675.
[126] D. Weng, S. Yuvarajan, Constant-switching frequency AC-DC second-harmonic-injected PWM, in: Conference Record IEEE-APEC'95, 1995, pp. 642–646.
[127] H.S. Athab, A duty cycle control technique for elimination of line current harmonics in single-stage DCM boost PFC circuit, in: TENCON 2008, International Technical Conference of IEEE Region 10, TENCON 2008, 19–21 Nov. 2008, 2008, pp. 19–21.
[128] A. Miwa, D.M. Otten, M.F. Schlecht, High efficiency power factor correction using interleaving techniques, in: Conference Record IEEE-APEC'92, 1992, pp. 557–568.

[129] M.S. Elmore, W.A. Peterson, S.D. Sherwood, A power factor enhancement circuit, in: Conference Record IEEE-APEC'91, 1991, pp. 407–414.
[130] J. Sebastian, P. Villegas, M.M. Hernando, S. Ollero, High quality flyback power factor correction based on a two-input buck postregulator, in: Conference Record IEEE-APEC'97, 1997, pp. 288–294.
[131] J. Rajagopalan, J.G. Cho, B.H. Cho, F.C. Lee, High performance control of single-phase power factor correction circuits using a discrete time domain control method, in: Conference Record IEEE-APEC'95, 1995, pp. 647–653.
[132] L.J. Borle, C.V. Nayar, Ramptime current control, in: Conference Record IEEE-APEC'96, 1996, pp. 828–834.
[133] S.Z. Dai, N.L. Lujara, B.T. Ooi, A unity power factor current-regulated SPWM rectifier with a notch feedback for stabilization and active filtering, IEEE Trans. Power Electron. 7 (2) (1992) 356–363.
[134] T. Ohnuki, O. Miyashita, T. Haneyoshi, E. Ohtsuji, High power factor PWM rectifiers with an analog pulsewidth prediction controller, IEEE Trans. Power Electron. 11 (3) (1996) 460–471.
[135] B.A. Mather, Digital Control Techniques for Single-Phase Power Factor Correction Rectifiers, Department of Electrical, Computer and Energy Engineering, Faculty of the Graduate School of the University of Colorado, Colorado, USA, 2010. PhD thesis.
[136] A. Prodic, J. Chen, D. Maksimovic, R.W. Erickson, Self-tuning digitally controlled low-harmonic rectifier having fast dynamic response, IEEE Trans. Power Electron. 18 (2003) 420–428.
[137] A. Prodic, D. Maksimovic, R.W. Erickson, Dead-zone digital controllers for improved dynamic response of low harmonic rectifiers, IEEE Trans. Power Electron. 21 (2006) 173–181.
[138] S. Buso, P. Mattavelli, L. Rossetto, G. Spiazzi, Simple digital control improving dynamic performance of power factor preregulators, IEEE Trans. Power Electron. 13 (1998) 814–823.
[139] W. Zhang, G. Feng, Y. Lui, B. Wu, A digital power factor correction (PFC) control strategy optimized for DSP, IEEE Trans. Power Electron. 19 (2004) 1474–1485.
[140] J. Chen, A. Prodic, R.W. Erickson, D. Maksimovic, Predictive digital current programmed control, IEEE Trans. Power Electron. 18 (2003) 411–419.
[141] P. Mattavelli, G. Spiazzi, P. Tenti, Predictive digital control of power factor preregulators with input voltage estimation using disturbance observers, IEEE Trans. Power Electron. 20 (2005) 140–147.
[142] A. de Castro, P. Zumel, O. Garcia, T. Riesgo, J. Uceda, Concurrent and simple digital controller of an AC/DC converter with a power factor correction based on an FPGA, in: IEEE Trans. Power Electron., 18 2003, pp. 334–343.
[143] C.P. Henze, N. Mohan, A digitally controlled AC to DC power conditioner that draws sinusoidal input current, in: Proceedings of the IEEE Power Electronics Specialist Conference, 1986, pp. 531–540.
[144] L.T. Jakobsen, N. Nielsen, C. Wolf, M.A.E. Anderson, Hybrid control method for a single phase PFC using low cost microcontroller, in: Proceedings of the Applied Power Electronics Conference, 2005, pp. 1710–1715.
[145] A.H. Mitwalli, S.B. Leeb, G.C. Verghese, V.J. Thottuvelil, An adaptive digital controller for a unity power factor converter, IEEE Trans. Power Electron. 11 (1996) 374–382.
[146] Y. Chen, D. He, R.M. Nelms, Control of a single-phase PFC preregulator using an 8-bit microcontroller, in: Proceedings of the Applied Power Electronics Conference, 2007, pp. 1454–1460.
[147] F.J. Azcondo, A. de Castro, V.M. Lopez, O. Garcia, Power factor correction without current sensor based on digital current rebuilding, IEEE Trans. Power Electron. 25 (2010) 1527–1536.
[148] S. Bibian, H. Jin, Digital control with improved performance for boost power factor correction circuits, in: Proceedings of the Applied Power Electronics Conference and Exposition vol. 1, 2001, pp. 67–73.
[149] P. Zumel, A. de Castro, O. Garcia, T. Riesgo, J. Uceda, A simple digital hardware to control a PFC converter, in: Proceedings of Industrial Electronics Society, 2001, pp. 943–948.
[150] H. Peng, D. Maksimovic, Digital current-mode controller for DC-DC converters, in: Proceedings of Applied Power Electronics Conference and Exposition, vol. 2, 2005, pp. 899–905.
[151] S. Kim, P.N. Enjeti, Control of multiple single-phase PFC modules with a single low-cost DSP, IEEE Trans. Ind. Appl. 39 (2003) 1379–1385.
[152] W. Stefanutti, P. Mattavelli, G. Spiazzi, P. Tenti, Digital control of single-phase power factor preregulators based on current and voltage sensing at switch terminals, IEEE Trans. Power Electron. 21 (2006) 1356–1363.

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17

Magnetic Circuit Design for Power Electronics

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17.1 Introduction

The evolution of power electronics since the middle of the 20th century has largely depended on the introduction of semiconductor devices. The invention of the SCR in the late 1950s led to the expansion of the field of motor drives both DC and AC. The coming of age of the power MOSFET in the 1970s presaged the era of efficient switch-mode power supplies. This was followed by the insulated gate bipolar transistor (IGBT) that opened up the possibility of inverter variable speed drives and their ever-expanding range of application by combining the gate drive of a MOSFET with the current and voltage capability of the bipolar junction transistor. The new millennium saw innovation in wide bandgap materials such as the silicon carbon (SiC) devices and gallium nitride (GaN). The devices based on these materials have enabled further developments in resonant power supplies.

All of these innovations and advances along with their associated circuit and topology enhancements have placed the role of magnetics center stage. Furthermore, each device in turn has facilitated an increase in the frequency of operation with the result that magnetic components in the MHz range for power electronics applications are now the norm.

The most basic transformer equation informs us that the size of the transformer is directly reduced in proportion to increasing frequency. The reality of losses in the transformer winding and in the core material places limits on the size reduction. More recent developments in the movement to high-frequency operation have introduced additional losses in the form of fringing around air gaps. Multiple strands in conductors in the form of litz wire to mitigate high-frequency skin and proximity effects have in themselves introduced new sources of losses.

The switch-mode power supply greatly improved the overall converter efficiency; size reduction followed from the high operating frequency (up to 500 kHz). Of course losses during the turn-on and turn-off processes increased with frequency, and the presence of parasitic inductance and capacitance limited the turn-on and turn-off times, placing further restrictions on the upper operating frequency of the magnetic components. The advent of soft switching with zero voltage switching (ZVS) or zero-current switching (ZCS) coped with the switching losses and led to another leap in frequencies (and consequent reduction in the size of the magnetics). This conceptually removed the barrier to high-frequency operation. More advantages followed: reduced electromagnetic interference (EMI)

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and smaller filter components. Evidently, all roads lead to high-frequency operation.

Recall that the transformer performs three basic functions in an electric circuit: to provide isolation, to reduce voltage stress in a switching device by adjusting the voltage, and to allow operation at high-frequency to reduce size. Major losses occur in the magnetic materials and improvements in the materials must parallel improvements in topologies and devices. The main magnetic materials encountered in power electronics will be described in Section 17.2, along with their characteristics. An understanding of the basic laws of electromagnetism is the essential starting point for magnetic design. The basic elements will be covered in Section 17.3. Transformer design for modern power electronics will be the subject of Section 17.4. The objective here is to establish a straightforward and robust set of equations to select the transformer core in applications ranging from switch-mode power supplies to resonant converters.

Selecting the core is just the starting point. Additional considerations are required for high-frequency effects including fringing around air gaps. The proper selection and use of litz wire where appropriate and mitigation techniques for winding losses such as interleaving will be treated in Section 17.5.

By their very nature, circuits in power electronics that usually involve switching elements give rise to nonsinusoidal waveforms of voltage and current. Traditional definitions of power factor and loss mechanisms based on sinusoidal waveforms must be revisited and modified to take the nonsinusoidal waveforms into account in the design of magnetic components.

17.2 Magnetic Materials and Characteristics

The main purpose of magnetic core materials in power electronics is to provide a low reluctance path to magnetic flux produced by current flowing in inductors and transformers. Traditionally, iron-based silicon-steel materials performed this role in mains frequency transformers, and they continue to do so in existing power systems, although tape wound amorphous core materials are now being considered. For application at higher frequencies typical of switching mode power supplies (SMPS), eddy current losses are excessive and cannot be controlled without significantly reducing the thickness of silicon-steel sheets. For operation at mains frequencies, typical silicon sheet thicknesses are in the range of 0.2–0.5 mm [1], and thinner forms are emerging to enable operation at frequencies up to several kHz [2].

Ferrite and powdered (distributed air gap) materials have been developed specifically for application in high-frequency power electronic circuits, where their material structures are designed to limit eddy current loss by restricting the magnetic particle size within an insulating binder. For both material types, manufacturers provide different material grades that are optimized for operation within different frequency ranges to support standard applications up to 500 kHz. More recently, amorphous and nanocrystalline materials have emerged as potential competitor materials, due to their higher saturation flux density and low loss characteristics at frequencies up to approximately 100 kHz [3]. Meanwhile, with the ongoing drive toward system integration in power-supply-in-package (PwrSiP) and power supply on chip (PwrSoC), the integration of magnetic materials within power supply packaging has driven developments in magnetic materials well into the MHz range. This includes electroplating and lamination of metal core layers within PCB's [4,5] and electroplating and sputtering of magnetic films onto silicon [6–8]. Nanoparticle-based materials are also being developed for use as discrete miniaturized cores in PwrSiP and PwrSoC at frequencies up to 30 MHz [9].

17.2.1 Magnetic Material Properties

Magnetic materials are highly nonlinear with many properties varying with magnetic field excitation level, operating frequency, and temperature, thereby complicating the design of magnetic components. For instance, the primary property of a magnetic material is its relative permeability, μ_r, which relates the magnetic flux density B, within the material to the magnetic field intensity H, according to

$$B = \mu_r \mu_0 H \tag{17.1}$$

where $\mu_o = 4\pi \times 10^{-7}$ H/m is the permeability of free space. However, the value of μ_r is dependent on the level of magnetic flux density B as shown in the B-H plot of a magnetic material in Fig. 17.1. Indeed, it is seen that magnetic materials exhibit hysteretic behavior, where the interdependence between B and H depends not only on their relative levels but also on the rate of change of B with H; that is, the magnetic flux density level corresponding to a given value of magnetic field intensity H_x as it increases is different to that found for the same value as

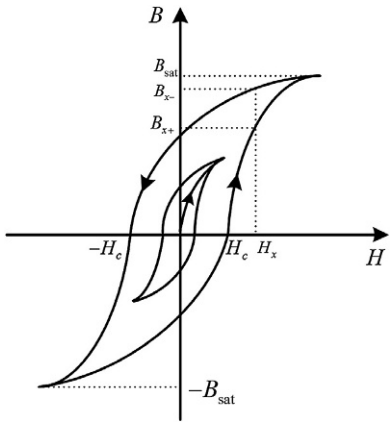


FIG. 17.1 B-H loops of a magnetic material.

it decreases. This is illustrated in Fig. 17.1, where B_{x+} is the magnetic flux density at H_x as it increases, while B_{x-} corresponds to H_x as it decreases over the given B-H loop. This difference is due to magnetic coercivity, H_c, which is the minimum value of magnetic field intensity for which the material responds to a varying magnetic flux density. Alternatively, it is the value of magnetic field intensity remaining within a material after the applied magnetic flux density reduces to zero. Ideally, for soft magnetic materials, such as those used in inductors and transformers, H_c should be as small as possible, while it should be as high as possible in permanent magnet materials in order to preserve magnetism.

Practically, in magnetic component design for power electronics, a linear relationship between B and H is assumed between their peak applied values (as shown in Fig. 17.1) to enable definition of relative permeability based on the amplitude of applied magnetic flux density:

$$\mu_r = \frac{1}{\mu_0}\frac{\hat{B}}{\hat{H}} \tag{17.2}$$

Examination of Fig. 17.1 shows that due to the hysteretic behavior, μ_r typically increases with increasing amplitude of magnetic flux density, so long as this amplitude is lower than the saturation flux density, B_{sat}. Beyond this value, there is no further increase in magnetic flux density with increasing magnetic field intensity, and therefore, magnetic saturation imposes a limit on the useful operating range of a magnetic material.

Similarly, under DC bias conditions, the relative permeability depends on both the DC and AC levels of magnetic flux density. As an aid to magnetic component design, the manufacturers of magnetic cores provide graphs to quantify the level of variation under typical application conditions levels. For example, ferrite materials can have relative permeability values that vary by up to 200% over a typical range of AC magnetic flux density.

In terms of operating frequency, relative permeability generally remains constant for frequencies up to the point where eddy current losses become dominant. For ferrite and powdered materials, this frequency is usually higher than the optimal one at which overall core losses can be tolerated, and therefore, variations in relative permeability are not significant. However, eddy current losses are more dominant in metal film cores, and therefore, variations the relative permeability with frequency may impact on designs based on metal film cores.

Loss in magnetic materials includes contributions from eddy current, hysteresis, and anomalous effects. Eddy current loss is conductive I^2R loss produced by circulating currents induced in response to AC flux linkage, flowing against the internal resistance of the core. In ferrite materials, it is limited by restricting the size of individual ferrite particles within an insulating binder, while in metal film layers, its effect is limited so long as the film thickness is maintained smaller than the material skin depth δ where

$$\delta = \frac{1}{\sqrt{\pi f \mu_r \mu_0 \sigma}} \tag{17.3}$$

f is the operating frequency and σ is the conductivity of the material.

Hysteresis loss is thought to be due to frictional effects between magnetic domains within the material structure as they rotate in response to AC magnetic fields. Hysteresis loss per unit volume may be estimated in terms of the area enclosed by the material BH loop under given AC and DC conditions:

$$P_{hys} = f\oint_B H dB \tag{17.4}$$

where the integral is performed over a complete cycle of the given magnetic flux density excitation levels.

Anomalous loss, also termed excess eddy current loss, is due to the presence of magnetic domains within magnetic material structures. The exact nature of this effect is not fully understood, but it is thought to be attributed to nonuniform magnetic flux density distributions produced within magnetic domains. However, a lack of understanding of the variation in magnetic domain sizes and orientations under field excitation further complicates its contribution [10]. Anomalous loss is most prominent in tape wound and metal film core materials where classical eddy current loss is controlled by maintaining film thicknesses lower than the material skin depth.

Practically, total core loss per unit volume, P_{fe}, may be estimated using the Steinmetz equation:

$$P_{fe} = K_c f^{\alpha} \hat{B}^{\beta} \tag{17.5}$$

for which manufacturers provide material parameters, K_c, α and β, that are based on measurements of loss characteristics performed over a range of sinusoidal magnetic flux density excitation levels and frequencies. Given that the loss parameters are based on measurements, the Steinmetz equation therefore accounts for the combined contributions of all loss effects.

In power electronics applications, voltage and current waveforms applied to magnetic components are more often rectangular than sinusoidal, and therefore, due to significant contributions of voltage/current harmonics, direct application of the Steinmetz equation does not produce accurate predictions of total core loss. Instead, the Steinmetz equation has been modified to account for nonsinusoidal waveforms, by recognizing the general dependence of core loss on both the magnetic flux density and the rate of change of magnetic flux density with respect to time in the generalized Steinmetz equation (GSE) [11]. In a further development, the effects of minor BH loop excursions are incorporated in the improved generalized Steinmetz equation (iGSE):

$$P_{fe} = \frac{1}{T}\int_0^T k_i \left|\frac{dB(t)}{dt}\right|^{\alpha} |\Delta B|^{\beta-\alpha} dt \tag{17.6}$$

where

$$k_i = \frac{K_c}{2^{\beta-1}\pi^{\alpha-1}\int_0^{2\pi} |\cos\theta|^{\alpha} d\theta} \tag{17.7}$$

and where ΔB is the peak-to-peak amplitude of magnetic flux density over each minor loop as it contributes during the excitation waveform [12]. A further modification to the Steinmetz equation has been proposed to account for the effects of magnetic relaxation effects during periods of zero applied voltage [13]. However, it should be remembered that the Steinmetz parameters themselves are based on experimental data and that they vary over different operating frequency ranges. Therefore, the accuracy of models based on these parameters relates directly to the original manufacturers' measurement accuracy. Practically, Eqs. (17.5) or Eqs. (17.6–17.7) are best applied to estimate initial values of core loss, with follow-up measurements recommended to confirm losses under applied operating conditions.

The temperature range and temperature stability of magnetic materials should be considered because standard ferrite and powdered material loss properties vary by up to 500% from room temperature to 140°C. Some ferrite grades are designed to have more stable loss properties with temperature variation, while others are optimized to have minimum loss at a standard operating temperature such as 140°C for automotive applications.

17.2.2 Comparison of Magnetic Material Types

The properties of magnetic core materials used in switched-mode power electronic applications are compared in Table 17.1, while power loss density values are compared in Fig. 17.2. The most commonly applied material type is ferrite, which consists of a combination of metal oxide particles that are pressed and sintered together to form one of several standard core shapes (E, C, toroid, planar E, I, etc.). Owing to the small particle size (of the order of μm), eddy currents are restricted so that ferrites are characterized by high resistivity

TABLE 17.1 Properties of magnetic core materials commonly used in power electronics

Materials	Ferrites	Nanocrystalline	Amorphous	Si iron	Ni-Fe (permalloy)	Powdered iron
Model	Ferroxcube 3F3	VIROPERM 500 F	METGLAS 2605	AK Oriented M-4	MAGNETICS PERMALLOY 80	MICROMETALS 35 μ
Permeability, μ_i	2000–4500	15,000	10,000–150,000	5000–10,000	20,000	3–550
B_{peak}, T	0.34–0.42	1.2	1.56	2.0	0.82	0.6–1.3
ρ, μΩm	2×10^6	1.15	1.3	0.51	0.57	10^6
Curie temp. T_c, °C	200	600	399	746	460	665
P_{loss}	210 mW/cm^3 at 0.1 T/200 kHz	588 mW/cm^3 at 0.3 T/100 kHz	72 mW/cm^3 at 0.2 T/25 kHz	2.295–30.6 mW/cm^3 at 1.5 T/50 Hz	192.28 mW/cm^3 at 0.2 T/5 kHz	126–315 mW/cm^3 at 0.1 T/10 kHz

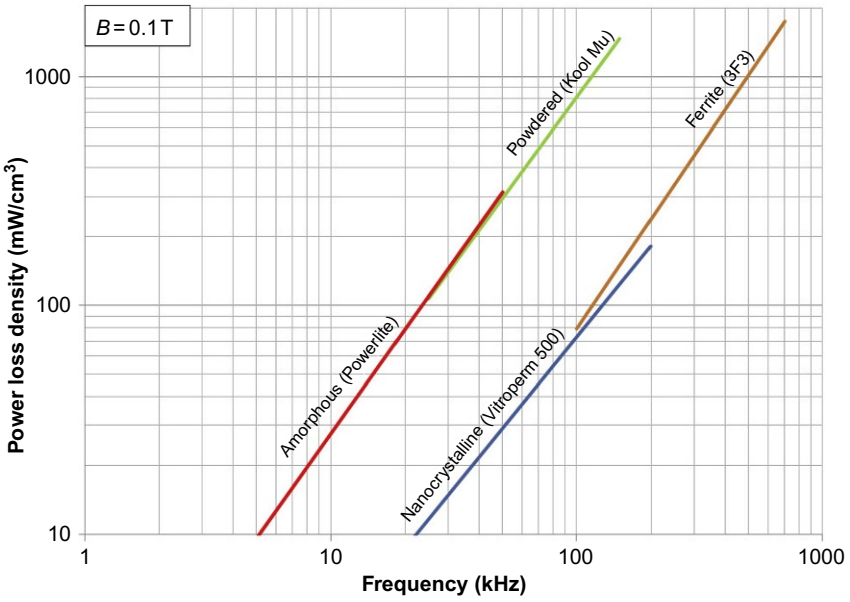


FIG. 17.2 Core loss density versus frequency for common magnetic materials.

and high relative permeability, with the properties of each ferrite grade depending on the relative concentration and particle size of constituent metal oxides. Typically, Mn-Zn ferrites are most widely applied in power electronics applications, with manufacturers providing a range of grades having loss properties suitable for operation at frequencies up to 2 MHz. On the other hand, Ni-Zn grades are more suited to signal level applications at frequencies in the 1–10 MHz range. The main limitation of ferrites is their low saturation flux density of 300–450 mT, which is at least half that of silicon-steel.

In inductor and transformer applications where the core is subjected to a DC bias field, magnetic powder materials provide a suitable alternative to ferrites. With ferrite, a lumped gap is generally needed to ensure that the material is not saturated under DC bias conditions. This results in a significantly reduced effective relative permeability and causes increased eddy current losses due to the interaction of fringing fields with windings placed in the vicinity of the gap (see Section 17.5.2). In powder materials, the gap is distributed throughout the bulk material, which consists of magnetic alloy grains bound together within an insulating material. Magnetic powder materials are therefore also known as distributed air gap material. They contribute little or no fringing field effects. Constituent magnetic alloys include various combinations of nickel, iron, silicon, aluminum, molybdenum, and boron. Relative permeability values are in the range of 10–550, which are comparable with the effective permeability of gapped ferrite cores, and saturation flux density can be as high as 1.6 T. While bulk core loss properties are not as competitive as ferrite (see Fig. 17.2), when the effects of eddy current losses in windings surrounding a discrete gap are accounted for, powder materials can provide an overall reduced loss design.

In the 1980s, the development of new rapid cooling methods for hot-spun melt magnetic tape materials led to the emergence of amorphous and nanocrystalline materials as competitors initially to silicon-steel and nickel-iron metal alloys in tape wound cores. With ongoing research, these material types have since been developed for application in common mode choke and other power electronic applications. Due to the similarity in their composition and manufacturing processes, both materials have similar structures and properties, much of which result from their nanoscale magnetic particle sizes (10–20 nm). They comprise various concentrations of iron, cobalt, and nickel, with silicon and boron included to ensure stabilization of the amorphous structure. After rapid cooling of the molten metal, a tape of amorphous material with a thickness of approximately 20 μm is produced. Nanocrystalline materials are amorphous tapes that have further heat treatment applied that provides them with superior loss and saturation properties. The materials are characterized by very high permeability values (100,000's), high saturation flux density (up to 1.7 T), and loss properties that are competitive to ferrites for power electronic applications in the range of 100–200 kHz. Research is continuing to develop these materials and core shapes for a wider range of applications.

17.2.3 Future Developments

Much of the latest research in magnetic materials is focused on the development of core materials suitable for operation in the multi-MHz range and on processes to integrate them into power electronics packaging, that is, within printed circuit boards (PCBs) or onto silicon. The main drivers are reduced size and improved response rate of low power applications, both of which are achieved by increased operating frequency. At a larger power scale, developments in SiC and GaN semiconductors are progressing to enable higher switching frequencies in high-voltage, smart grid, and renewable energy applications. This in turn will lead to developments in compatible core materials, where the high saturation flux density and competitive loss properties of amorphous and nanocrystalline materials make them the most suitable solutions.

17.3 Magnetic Circuits

Faraday's law and Ampere's law have built the relationship between the electric characteristics and magnetic characteristics and are key principles guiding the transformer and inductor design in power electronics. The typical analytic model for a magnetic circuit is the magnetic reluctance model that is based on a reluctance-resistance analogy.

17.3.1 Faraday's Magnetic Circuit Law

Faraday's law states that a time-varying magnetic flux $\phi(t)$ passing through the interior of a winding generates a voltage $v(t)$ in the winding. Fig. 17.3 illustrates time-varying flux $\phi(t)$ passing through the interior of a loop of wire and the voltage $v(t)$ induced in the closed loop enclosing the flux.

The loop cross-sectional area is expressed by A_c. According to Faraday's law, the flux induces a voltage $v(t)$ in the termination of the wire, given by

$$v(t) = \frac{d\phi(t)}{dt} \tag{17.8}$$

For a winding with N turns, the induced voltage can be expressed as

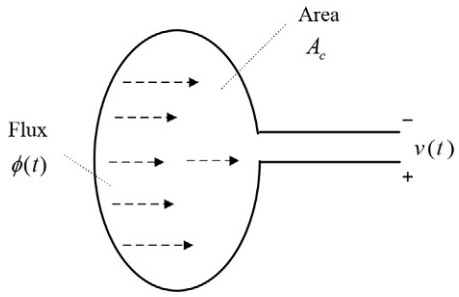


FIG. 17.3 Illustration of Faraday's law.

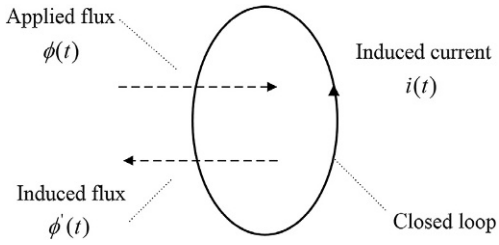


FIG. 17.4 Illustration of Lenz's law in a closed loop.

$$v(t) = N \cdot \frac{d\phi(t)}{dt} \tag{17.9}$$

The induced flux ϕ may link with each turn of the winding, so that the flux linkage is

$$\lambda = N \cdot \phi \tag{17.10}$$

For a uniform flux distribution, the expression (17.9) can be rewritten as

$$v(t) = N \cdot A_c \cdot \frac{dB(t)}{dt} \tag{17.11}$$

where $B(t)$ is magnetic flux density passing through the winding.

Lenz's law states that the current induced in the closed loop due to the changing flux tends to oppose the flux change. Fig. 17.4 shows an example of Lenz's law. The flux $\phi(t)$ induces current $i(t)$, which in turn generates flux $\phi'(t)$ that tends to oppose changes in $\phi(t)$.

The induced voltage opposes the creating flux by generating secondary currents called eddy currents. Lenz's law can well explain the eddy current effects in magnetic cores and in the winding conductors.

17.3.2 Ampere's Magnetic Circuit Law

Ampere's law states that a time-varying current $i(t)$ induces a time-varying magnetic field $H(t)$, as shown in Fig. 17.5. The net magnetomotive force (MMF) in the core is equal to the total currents passing though the interior of the magnetic core loop. The line integral of H around any closed contour is equal to the total current enclosed by that contour, and it may be stated in the integral form:

$$\oint_C H \cdot dl = i \tag{17.12}$$

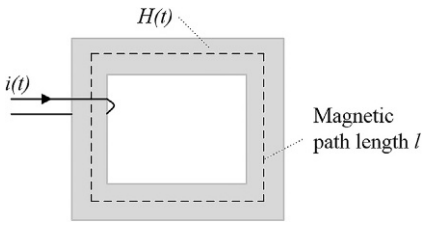


FIG. 17.5 Illustration of Ampere's law.

For the winding with N turns, Ampere's law is

$$\oint_C H \cdot dl = N \cdot i \tag{17.13}$$

The magnetic field intensity H leads to a resulting magnetic flux density B due to the B-H characteristics of core materials. The nonlinearity of the characteristics is neglected in this section, and therefore, the relation of the B-H characteristic is given by Eq. (17.1).

17.3.3 Reluctance and Inductance

When making an analogy between magnetic circuits and electric circuits, it is natural to regard the magnetomotive force (MMF) between the two terminations of the winding as analogous to the voltage and magnetic flux, ϕ, as analogous to the current. As shown in Fig. 17.6, the MMF, $F = N \cdot i$, is visualized as a force like quantity that pushes a magnetic flux, ϕ, around the magnetic circuit. Magnetic core reluctance, R, in a magnetic circuit is then the counterpart of resistance of an electric circuit. $\phi = F/R$, directly corresponding to Ohm's law. The reluctance opposes the magnetic flux flow, similarly to the way the resistance opposes the electric current flow. Therefore, magnetic circuits described by Eq. (17.14) can be solved in a similar manner as electric circuits described by Ohm's law.

$$F = H \cdot l = N \cdot i = \phi \cdot R \tag{17.14}$$

Fig. 17.6 illustrates a coil with N turns wound on a closed magnetic core of mean length l_c and cross-sectional area A_c. The reluctance of a basic magnetic circuit element is given by

$$R = \frac{l_c}{\mu_0 \cdot \mu_r \cdot A_c} (At/H) \tag{17.15}$$

The self-inductance L relates the flux linkage produced by a coil to the current in that coil:

$$L = \frac{\lambda}{i} = \frac{N \cdot \phi}{i} = \frac{N^2}{R} = \frac{\mu_0 \cdot \mu_r \cdot A_c \cdot N^2}{l_c} \tag{17.16}$$

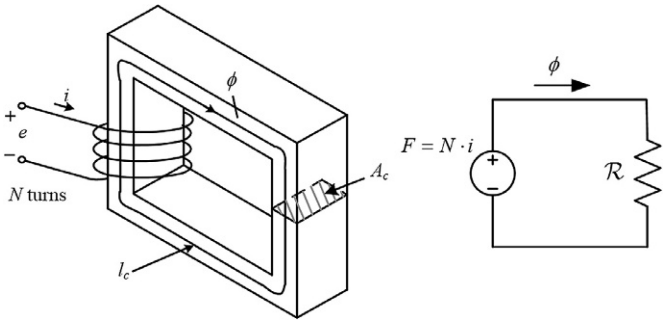


FIG. 17.6 Example of magnetic circuit and equivalent magnetic reluctance circuit.

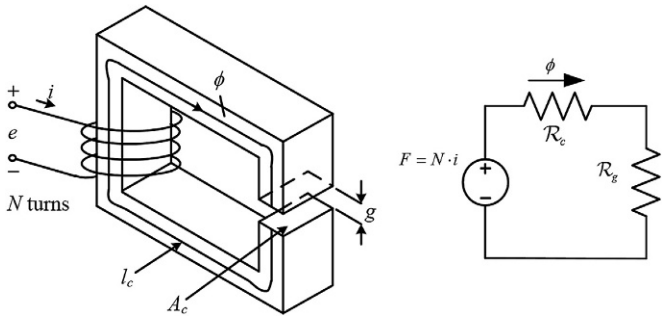


FIG. 17.7 Example of magnetic circuit for gapped inductor.

In fact, the *B-H* characteristic is a nonlinear function of the applied magnetic field intensity in ferromagnetic materials. In the magnetic core of Fig. 17.6, the flux density B is limited by the core material, and a small current with sufficient turns can easily drive the magnetic core material into saturation. To avoid the core saturation, an air gap is often introduced into the core as shown in Fig. 17.7, a larger current can pass through the winding without reaching saturation because of the increased reluctance. The analysis to follow also shows that the air gap gives rise to more energy storage.

In the structure of Fig. 17.7, there are two reluctances in series, so,

$$F = N \cdot i = \phi \cdot \left(R_c + R_g\right) \tag{17.17}$$

The individual reluctances are given by their respective physical properties of length and cross section; subscript c refers to the core and subscript g refers to the air gap. For the core reluctance,

$$R_c = \frac{l_c}{\mu_0 \cdot \mu_r \cdot A_c} \tag{17.18}$$

and for the air gap reluctance, $\mu_r = 1$,

$$R_g = \frac{g}{\mu_0 \cdot A_g} \tag{17.19}$$

where g is the length of the air gap. Since $\mu_r \gg \mu_0$, the reluctance of the core R_c can be ignored, $R_c \ll R_g$, invoking Eq. (17.17) yields

$$F = N \cdot i = \phi \cdot R_g \tag{17.20}$$

Therefore, the gapped inductance L is

$$L = \frac{N^2}{R_g} = \frac{\mu_0 \cdot A_g \cdot N^2}{g} \tag{17.21}$$

The air gap increases the total reluctance of the magnetic circuit and decreases the inductance.

17.4 Transformer Design

The basic transformer model is shown in Fig. 17.8.

This is a transformer with a turns ratio a:1. The winding resistance is R_1 and R_2 for the primary and secondary, respectively. X_{l1} and X_{l2} represent the leakage reactance in the primary windings and secondary windings, respectively. R_c represents the core loss and X_c represents the magnetizing inductance. For an ideal transformer, the permeability of the core material is considered infinite and the magnetizing current is negligible.

The voltage across the primary winding is [14]

$$E_1 = K_v f N_1 B_{\max} A_c \tag{17.22}$$

where f is the frequency, N_1 is the number of turns, $B_{\max}$ is the maximum flux density in the core, and A_c is the cross-sectional area of the core. These are shown in Fig. 17.9.

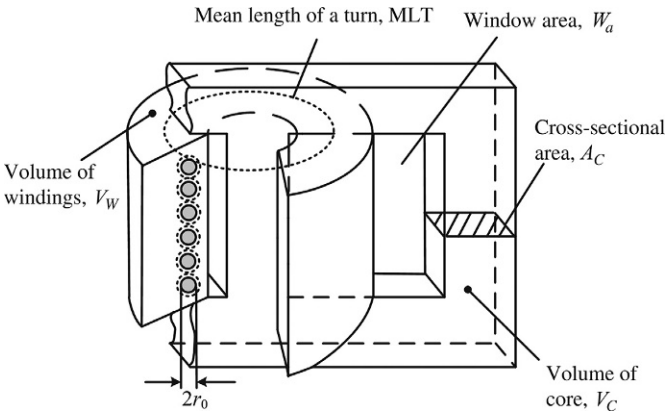


FIG. 17.9 Physical dimensions of a transformer.

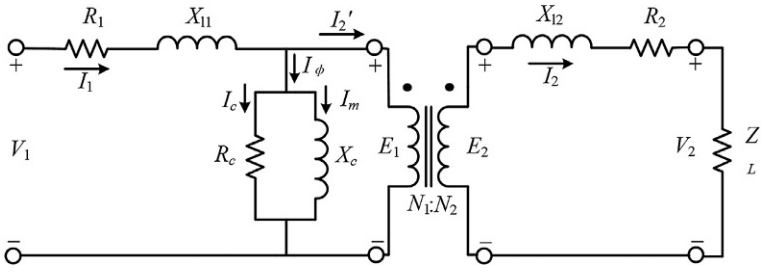


FIG. 17.8 The basic electric circuit of a practical transformer.

K_v depends on the shape of the voltage waveform. It has the value of 4.44 for sinusoidal waveforms and 4.0 for a square waveform. It may be calculated for any other waveform; the approach to calculate K_v will be outlined in an example later on.

The first step in developing the design methodology is to apply Eq. (17.22) to each of n windings and calculate the total VA rating of all the windings.

It may be shown that in a magnetic component with multiple windings, the optimum layout of the coils in terms of wire size is to maintain a constant current density J_o. Taking A_{wi} as the area of the conductor in winding i summing up the VA rating of each winding using Eq. (17.22) yields

$$\sum VA = K_v f N_i B_{\max} A_c J_o A_{wi} \tag{17.23}$$

Define the window utilization factor k_u as the rate of the window area W_a occupied by copper

$$k_u = \frac{\sum_{i=1}^{n} N_i A_{wi}}{W_a} \tag{17.24}$$

and Eq. (17.23) becomes

$$\sum VA = K_v f B_{\max} k_u J_o W_a A_c \tag{17.25}$$

The product $W_a \cdot A_c$ is the window area product A_p of the core. This result establishes the connection between the transformer rating and core size. The next step is the establishment of the winding loss and the core loss.

The copper loss in each winding is RI^2. At this point, we will take R to be the DC resistance and take the high-frequency skin and proximity effects into account later on. The mean length of a turn in the transformer winding is MLT and the total length of a coil i is $N_i \cdot$MLT. The copper loss is

$$P_{cu} = \sum_{i=1}^{n} \frac{\rho N_i MLT}{A_{wi}} (J_o A_{wi})^2 \tag{17.26}$$

Invoking the definition of the window utilization factor, Eq. (17.24) becomes

$$P_{\text{cu}} = \rho MLT\, W_a k_u J_o^2 \tag{17.27}$$

MLT $\cdot W_a$ is simply the volume of the windings, V_w.

Combining Eqs. (17.26) and (17.27) yields a new expression for the copper loss:

$$P_{cu} = \rho_w MLT\, W_a k_u \left[\frac{\sum VA}{K_v k_u W_a A_c}\right]^2 \frac{1}{f^2 {B_{\max}}^2} \tag{17.28}$$

The core loss under sinusoidal excitation is given by the celebrated Steinmetz formula Eq. (17.5):

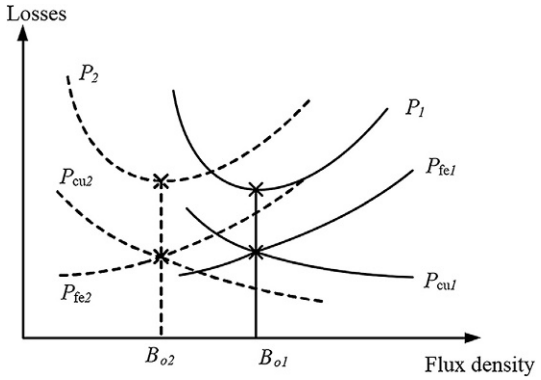


FIG. 17.10 Core and winding losses as a function of frequency and maximum flux density.

$$P_{\text{fe}} = V_c K_c f^{\alpha} \hat{B}^{\beta} \tag{17.29}$$

where K_c, α and β are constants supplied by the manufacturer. V_c is the volume of the core. Here, $\hat{B}$ is the amplitude of the sinusoidal flux density.

The total loss (at this point) is the sum of the two components given by Eqs. (17.28) and (17.29).

Evidently, the copper loss is inversely proportional to the product of frequency and maximum flux density Eq. (17.28), and the core loss is proportional to frequency and maximum flux density Eq. (17.29). These are illustrated in Fig. 17.10 for two different frequencies, $f_2 > f_1$.

The minimum value of the total losses occurs at

$$\frac{\partial P_{\text{total}}}{\partial \hat{B}} = 0 \tag{17.30}$$

and for a given frequency

$$P_{\text{fe}} = \frac{2}{\beta} P_{\text{cu}} \tag{17.31}$$

It follows that

$$P_{\text{total}} = P_{\text{cu}} + P_{\text{fe}} = \frac{\beta + 2}{\beta} P_{\text{cu}} \tag{17.32}$$

We can split the copper loss as follows:

$$P_{\text{cu}}^{1/12} P_{\text{cu}}^{7/12} = P_{\text{cu}}^{2/3} \tag{17.33}$$

Combining Eqs. (17.31) and (17.32) with Eq. (17.33) after some rearranging,

$$\frac{(\beta+2)^{2/3}}{2^{7/12}\beta^{1/12}} P_{\text{cu}}^{1/12} P_{\text{fe}}^{7/12} = P_{\text{total}}^{2/3} \tag{17.34}$$

As a first step, we assume the heat loss from the surface of the transformer is predominately by convection

$$P_{\text{total}} = hA_t\Delta T \tag{17.35}$$

where h is the coefficient of heat transfer by convection, A_t is the surface area of the transformer assembly and ΔT is the temperature rise in the transformer due to the losses. Taking this, Eqs. (17.28) and (17.29), and substituting them into Eq. (17.34) yields

$$\frac{(\beta+2)^{2/3}}{2^{7/12}\beta^{1/12}}\left[\rho MLT\,W_a k_u J_o^2\right]^{1/12}\left[V_c K_c f^{\alpha}\hat{B}^{\beta}\right]^{7/12} = \left[hA_t\Delta T\right]^{2/3} \tag{17.36}$$

At this point, we need dimensional analysis to simplify Eq. (17.36). The physical quantities, surface area A_t, the volume of the core V_c and the volume of the winding V_w are all related to the core window area product $A_p = W_a \cdot A_c$.

$$V_w = k_w A_p^{3/4} \tag{17.37}$$

$$V_c = k_c A_p^{3/4} \tag{17.38}$$

$$A_t = k_t A_p^{1/2} \tag{17.39}$$

The constants k_w, k_c, and k_t may be found from the dimensions of typical cores, and for the present purposes, $k_w = 10$, $k_c = 5.6$, and $k_t = 40$ would typify the cores used in modern power electronics.

Returning to Eq. (17.36), with these dimensionless constants

$$\frac{(\beta+2)^{2/3}}{2^{7/12}\beta^{1/12}}\left[\rho k_w k_u\right]^{1/12}\left[k_c K_c f^{\alpha}\hat{B}^{\beta}\right]^{7/12}\left[J_o A_p\right]^{1/6} = \left[hk_t\Delta T\right]^{2/3} \tag{17.40}$$

We need to return to Eq. (17.25) to find an expression for $J_o A_p$

$$\left[J_o A_p\right]^{1/6} = \left[\frac{\sum VA}{K_v f k_u B_{\max}}\right]^{1/6} \tag{17.41}$$

This result, substituted into Eq. (17.40), yields an expression for B_o and f at the optimum point in Fig. 17.10, that is, for minimum losses:

$$B_o^{7\beta-2} f_o^{7\alpha-2} = \frac{2^7\beta}{(\beta+2)^8}\frac{\left[hk_t\Delta T\right]^8}{\left[\rho k_w\right]\left[k_c K_c\right]^7}\left[\frac{{K_v}^2 k_u}{\sum VA^2}\right] \tag{17.42}$$

Note that $B_{\max}$ in Eq. (17.22) may include a DC component, but for the present purposes, we assume, it is the amplitude of the sinusoidal component, and we can adjust K_v if necessary.

The first and second terms on the right-hand side are fixed quantities. The third term is dependent on the circuit conditions and specifications. Normally, frequency is specified so this allows us to calculate the optimum value of maximum flux density in the core.

At this point, we need an expression for the current density in the windings. Taking Eq. (17.32) with Eqs. (17.27) and (19.35)

$$\rho MLT\,k_u W_a J_o^2 = \frac{\beta}{\beta+2}hA_t\Delta T \tag{17.43}$$

Adapting the dimensional analysis,

$$J_o = \sqrt{\frac{\beta}{\beta+2}\frac{hk_t}{\rho k_w}}\sqrt{\frac{\Delta T}{k_u}\frac{1}{{A_p}^{1/8}}} = K_\theta\sqrt{\frac{\beta}{\beta+2}}\sqrt{\frac{\Delta T}{k_u}\frac{1}{{A_p}^{1/8}}} \tag{17.44}$$

for $h = 10$ W/m^2°C, $k_w = 10$, $k_t = 40$, $\rho = 1.72\times10^{-8}$ Ω-m, and $K_\theta = 48.224\times10^3$.

Combining this expression for the current density with the optimum value of $f_o B_o$ given by Eq. (17.42) in Eq. (17.35) results in an expression for A_p that is found from the specifications of the circuit.

$$A_p = \left[\frac{\beta+2}{\beta}\frac{1}{k_u\Delta T}\right]^{4/7}\left[\frac{\sum \text{VA}}{K_v f_o B_o K_\theta}\right]^{8/7} \tag{17.45}$$

17.4.1 Design Example: Push-pull Converter

A 600 W push-pull converter operates at 80 kHz with a nominal DC input voltage of 325 V and the DC output voltage is 24 *V*. The allowable temperature rise is 50°C and the ambient temperature is 70°C. Using an EE ferrite core (N87 material), select the transformer core and calculate the copper loss in the windings and the core loss.

The push-pull converter and its associated waveforms are shown in Figs. 17.11 and 17.12.

The RMS value of the voltage waveform in the primary winding is

$$V_{\text{rms}} = \sqrt{D}V_s \tag{17.46}$$

Consider the time period 0-DT′:

$$V_s = N_p\frac{d\phi}{dt} = N_p A_c\frac{dB}{dt} = N_p A_c\frac{2B_{\max}}{DT'} = N_p A_c\frac{4B_{\max}}{DT} \tag{17.47}$$

Combining Eqs. (17.46) and (17.47),

$$V_{\text{rms}} = \frac{4}{\sqrt{D}}fN_p B_{\max}A_c = K_v f N_p B_{\max}A_c \tag{17.48}$$

So by the definition in Eq. (17.23),

$$K_v = \frac{4}{\sqrt{D}} \tag{17.49}$$

We also need the power factor of the input and output windings.

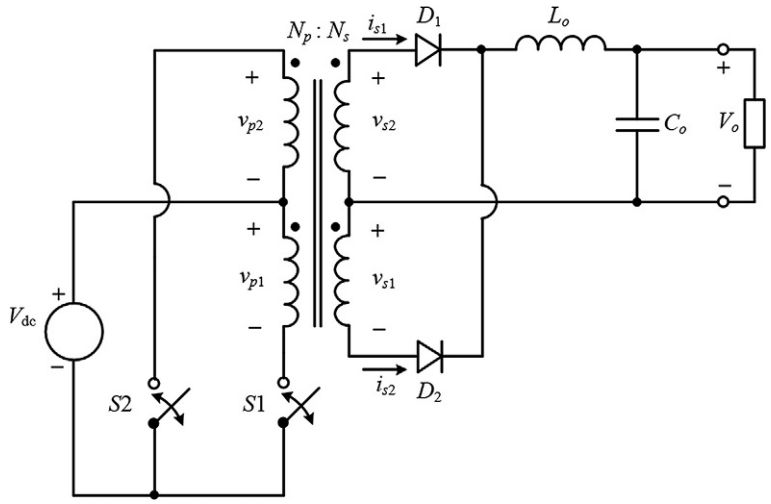


FIG. 17.11 Push-pull converter.

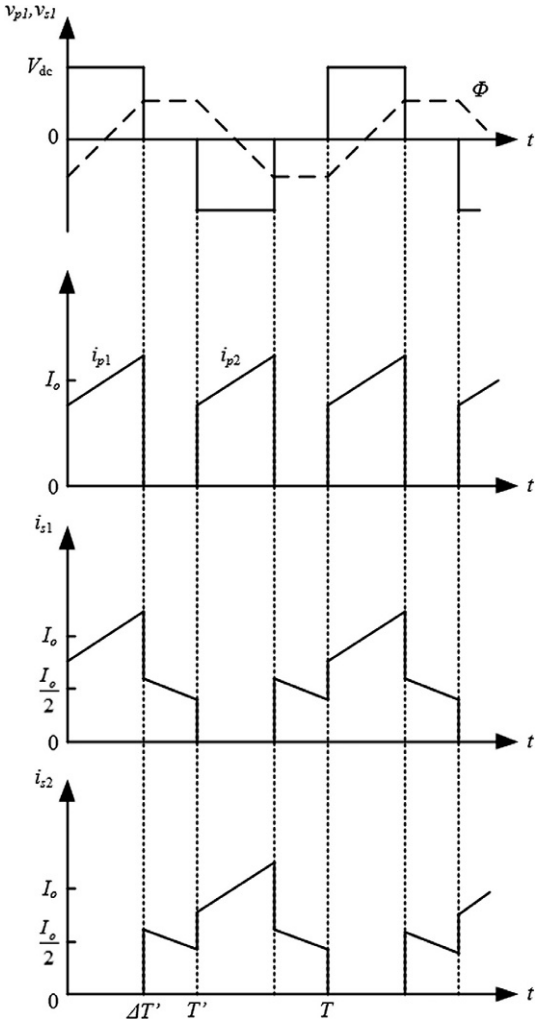


FIG. 17.12 Push-pull converter waveforms.

Input winding:

$$V_{p\text{rms}} = \sqrt{D}V_s$$
$$I_{p\text{rms}} = \sqrt{D/2}I_s \tag{17.50}$$

The average power delivered by each of the primary windings is

$$< p >= \int_0^{DT'} v(t)i(t)dt = \frac{1}{T}V_s I_s DT' = \frac{D}{2}V_s I_s \tag{17.51}$$

$$k_{pp} = \frac{< p >}{V_{p\text{rms}} I_{p\text{rms}}} = \frac{1}{\sqrt{2}} \tag{17.52}$$

The power factor of the secondary winding is found by the same approach and is given by

$$k_{ps} = \sqrt{\frac{D}{1+D}} \tag{17.53}$$

The switch stress parameter must be reduced by selecting a turns ratio of $a = 6$, and the duty cycle ratio is then

$$D = \frac{V_o}{V_s/a} = \frac{24}{325/6} = 0.443 \tag{17.54}$$

K_v from Eq. (17.49) is 6.0.

We can now establish the VA rating for all the windings, noting that each winding carries half of the load on average.

$$\sum \text{VA} = \left(\frac{1}{k_{pp}}\left(\frac{P_o}{2} + \frac{P_o}{2}\right) + \frac{1}{k_{ps}}\left(\frac{P_o}{2} + \frac{P_o}{2}\right)\right) = 1931\,\text{VA} \tag{17.55}$$

17.4.2 Step 1 Core Selection

EPCOS N87 Mn-Zn ferrite has constants $K_c = 16.9$, $\alpha = 1.25$, and $\beta = 2.35$. The saturation flux density is 0.4 T.

The first step is to find B_o from Eq. (17.42) with $f_o = 80$ kHz, $\Delta T = 50$, $K_v = 6.0$, $\sum VA = 1931$ VA, $k_u = 0.4$, $\beta = 2.35$, $h = 10$ W/m^2°C, $k_w = 10$, $k_c = 5.6$, and $k_t = 40$:

$$B_o = 0.038\ T$$

The window area product is given by Eq. (17.45) with $K_\theta = 48.224 \times 10^3$:

$$A_p = 9.647\,\text{cm}^4.$$

The EPCOS ETD 55/28/21 core meets the requirement with $A_P = 9.723$ cm^4.

The core has the following physical dimensions:

$W_a = 2.77$ cm^2, $A_c = 3.51$ cm^2, and MLT = 11.3 cm, and the volume of the core is $V_c = 43.5$ cm^3.

17.4.3 Step 2 Winding Selection

The number of turns in the primary winding is found from Eq. (17.47)

$$N_p = 30\,\text{turns}$$

With a 6:1 turns ratio, the secondary winding is 5 turns.

The current density in the windings is obtained from Eq. (17.44)

$$J_o = 2.982\,\text{A/mm}^2.$$

The primary current is a pulsed waveform with duty cycle $D/2$, so the RMS value is

$$I_{p,\text{rms}} = \sqrt{\frac{D}{2}}\frac{1}{a} I_o = 1.96\,\text{A} \tag{17.56}$$

and the conductor area is $A_w = I_{p,\text{rms}}/J_o = 0.658$ mm^2.

This corresponds to a 0.915 mm diameter wire. The skin depth at 80 kHz is 0.233 mm and therefore the diameter of the wire should be less than 0.5 mm to avoid skin depth losses (see Fig. 17.14). Four 0.45 mm diameter parallel wires will suffice with a combined DC resistance of 27.0 mΩ/m at 20°C.

The secondary current must take into account the conduction when both switches are open; it follows from Fig. 17.12

$$I_{s,\text{rms}} = \frac{I_o}{2}\sqrt{1+D} = \frac{25}{2}\sqrt{1+0.443} = 15.02\,A \tag{17.57}$$

and the conductor area is $A_w = I_{s,\text{rms}}/J_o = 5.035$ mm^2.

This is equivalent to a 2.5 mm diameter round conductor or a 0.2×24.5 mm copper foil. As the skin depth at 80 kHz is 0.233 mm, the round conductor is unsuitable, and the thickness of the foil should be less than 0.1 mm to avoid proximity effect losses (see Fig. 17.16). Two 0.1 mm foils in parallel will meet this requirement and with a combined DC resistance of 4.73 mΩ/m at 20°C.

17.4.4 Step 3 Losses

The total DC resistance of each primary winding at the maximum operating temperature is

$$R_p = N_p \times \text{MLT} \times (\Omega/m) \times [1 + \alpha_{20}(T_{\text{amb}} + \Delta T - 20°\text{C})] \tag{17.58}$$

With $T_{\text{amb}} = 70$°C, $R_p = 127.5$ mΩ, and the copper loss in each primary winding is

$$127.5 \times 10^{-3}(1.96)^2 = 0.49\,\text{W}.$$

The total DC resistance of each secondary winding at the maximum operating temperature is 3.723 mΩ, and the copper loss in each secondary winding is $2.792 \times 10^{-3}(15.02)^2 = 0.831$ W.

Later we will take the proximity effect into account in Section 17.5.

Then total copper loss is 2.642 W.

The core loss is found from the Steinmetz equation Eq. (17.29), $P_{\text{fe}} = 0.599$ W, so that the total loss is 3.241 W.

The thermal resistance of the core assembly, given by the manufacturer, is 10°C/W.

The maximum dissipation is then

$$P_D = \frac{\Delta T}{R_\theta} = \frac{50}{10} = 5.0\,\text{W} \tag{17.59}$$

The design meets this specification; however, there will be additional high-frequency proximity effect losses to include later.

17.5 High-Frequency Effects

A major effect of high-frequency inductors and transformers is ac loss in windings, which include skin and proximity effect losses. Both effects can be alleviated, to a greater or lesser extent with careful design. Winding layers can be optimized to minimize the proximity effect loss. Interleaving can further reduce the loss associated with proximity effects. Both skin effect and proximity effects may be mitigated by the use of litz wire. Design of inductors and transformers with litz wire conductors encompasses different challenges such as the modeling and calculation of ac resistance, the selection of the number and diameter of strands, and the optimal balance between the cross-sectional copper area and the stranding level. Fringing of the flux field around air gaps interacts with the adjoining conductors in a proximity type effect and introduces further losses. All of these effects will be discussed in this section.

Skin effect arises in a conductor due to the varying magnetic field generated by the AC current in the conductor itself. Eddy currents flow to counter the AC field, and the net effect is to reduce the current in the center of the conductor and to increase it at the outer edges, with the overall current remaining the same.

This is illustrated in Fig. 17.13 in a round conductor at three frequencies. At low frequency, the current is uniformly distributed over the conductor cross section. As the frequency increases, the current density increases toward the outside illustrated by the red band. At 1 MHz in the example shown, most of the current is in an annular ring at the outer radius of the conductor. Fig. 17.14 shows the factor Φ_{skin}, which represents the increase of the resistance due to the skin effect, per unit of length, with respect to the ratio of the conductor radius, r_s, to the skin depth. The skin depth is defined by Eq. (17.3).

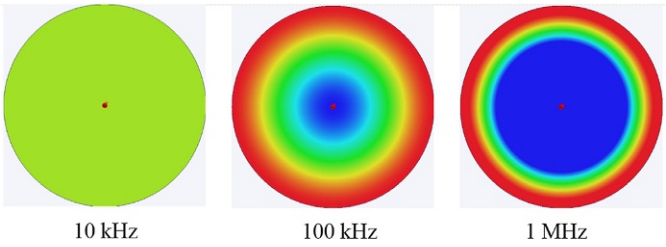


FIG. 17.13 Current distribution in a round conductor.

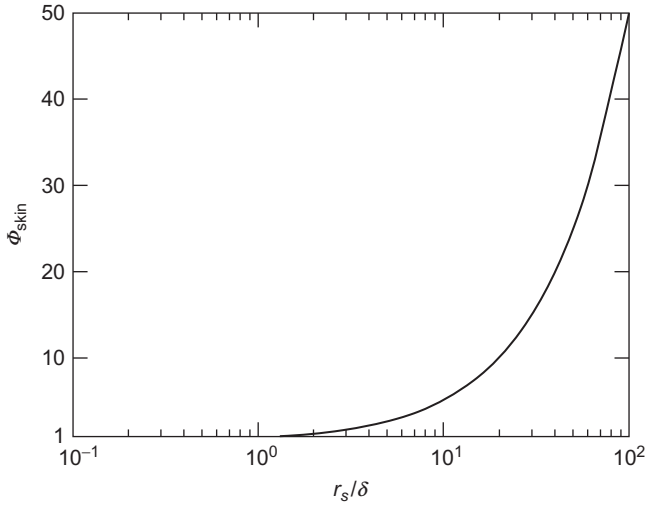


FIG. 17.14 Skin effect loss of a round conductor with respect to the ratio of the strand radius to the skin depth.

Both DC resistance and skin effect may be represented by a resistive element called conduction resistance. The conduction resistance per unit of length of a round strand of radius r_s, R_{cond}, is

$$R_{cond} = R_{dc}\Phi_{skin}(r_s/\delta) \tag{17.60}$$

where R_{dc} is the dc resistance of the conductor. For round conductors, the exact expression of Φ_{skin} is [15]

$$\Phi_{skin}(r_s/\delta) = \mathrm{Re}\left[\frac{(-1+j)(r_s/\delta)}{2}\frac{J_0((-1+j)(r_s/\delta))}{J_1((-1+j)(r_s/\delta))}\right] \tag{17.61}$$

where J_0 and J_1 are the Bessel functions of the first kind and order 0 and 1, respectively.

For practical designs, the ratio r_s/δ would be less than 2 to control the skin effect loss and a useful approximation is [14]

$$\Phi_{skin}(r_s/\delta) = 1 + \frac{(r_s/\delta)^4}{48 + 0.8(r_s/\delta)^4} \quad r_s/\delta < 2 \tag{17.62}$$

The proximity effect is more complicated and depends on the layout of the winding.

Consider the case illustrated in Fig. 17.15. It consists of a transformer with a solenoidal winding with two turns in the primary and three turns in the secondary. In an ideal transformer with infinite permeability in the core, the magnetic field between the turns can be found from Ampere's law. The eddy currents flow as illustrated to counter the magnetic fields on each side of the conducting layer. The red band shows the region with the high current density. Dowell's formula [16] was derived to deal with this case; the resistance due to proximity is

$$R_{prox} = R_{dc}\Phi_{prox}(\Delta) \tag{17.63}$$

$$\begin{aligned}\Phi_{prox}(\Delta) &= \mathrm{Re}\left(\Delta(1+j)\left[\coth(\Delta(1+j)) + \frac{2(p^2-1)}{3}\tanh\left(\frac{\Delta}{2}(1+j)\right)\right]\right)\\ &= \Delta\left[\frac{\sinh 2\Delta + \sin 2\Delta}{\cosh 2\Delta - \cos 2\Delta} + \frac{2(p^2-1)}{3}\frac{\sinh\Delta - \sin\Delta}{\cosh\Delta + \cos\Delta}\right]\end{aligned} \tag{17.64}$$

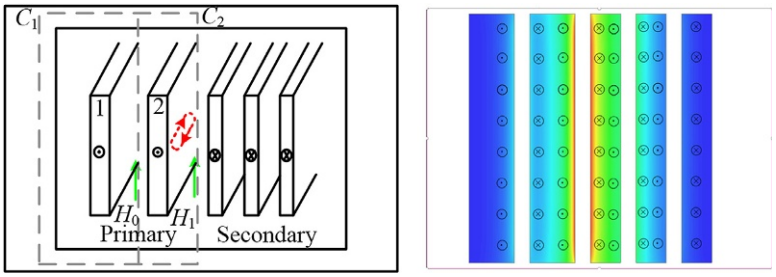


FIG. 17.15 Proximity effect in a transformer winding.

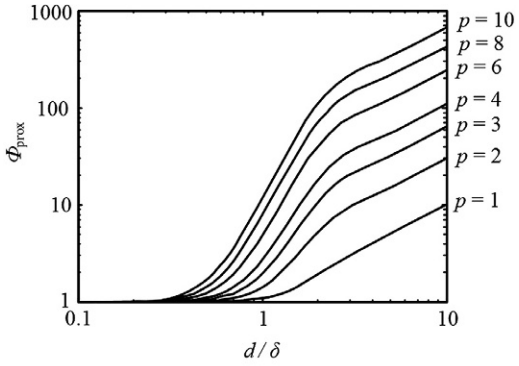


FIG. 17.16 Proximity effect factor in a transformer winding.

where p is the number of layers and Δ is the ratio d/δ, d being the thickness of the layer.

The nature of ϕ_{prox} is illustrated in Fig. 17.16.

As with the skin effect, as designers, we consider the region where $\Delta < 2$ and a useful approximation is

$$\phi_{prox}(\Delta) = 1 + \frac{5p^2 - 1}{45}\Delta^4 \tag{17.65}$$

This result is applicable to sinusoidal waveforms, but in power electronics, there are nonsinusoidal waveforms.

Consider the general case where a current waveform is represented by its Fourier series:

$$i(t) = I_{dc} + \sum_{n=1}^{\infty} \hat{I}_n \cos(n\omega t + \varphi_n) \tag{17.66}$$

where I_{dc} is the DC component and $\hat{I}_n$ is the amplitude of the n^{th} harmonic. The derivative is

$$\frac{di(t)}{dt} = -\omega \sum_{n=1}^{\infty} n\hat{I}_n \sin(n\omega t + \varphi_n) \tag{17.67}$$

The rms value of these expressions may be found from their Fourier coefficients:

$$I_{rms}^2 = I_{dc}^2 + \sum_{n=1}^{\infty} I_{n,rms}^2 \tag{17.68}$$

and

$$I'^2_{rms} = \omega^2 \sum_{n=1}^{\infty} n^2 I_{n,rms}^2 \tag{17.69}$$

where

$$I_{n,rms} = \frac{\hat{I}_n}{\sqrt{2}} \tag{17.70}$$

The proximity effect loss may be found by applying Dowell's formula to each frequency component. Using the approximation in Eq. (17.65), with the definition of skin depth in Eq. (17.3),

$$\phi_{prox}(\Delta_n) = 1 + \frac{5p^2 - 1}{45}\Delta_n^4 = 1 + \frac{5p^2 - 1}{45}n^2\Delta^4 \tag{17.71}$$

The effective resistance taking the harmonics into account is then

$$\begin{aligned} \frac{R_{eff}}{R_{dc}} &= \frac{I_{dc}^2 + \sum_{n=1}^{\infty} \phi_{prox}(\Delta_n) I_{n,rms}^2}{I_{rms}^2} \\ &= \frac{I_{dc}^2 + \sum_{n=1}^{\infty} I_{n,rms}^2 + \frac{5p^2 - 1}{45}\Delta^4 \sum_{n=1}^{\infty} n^2 I_{n,rms}^2}{I_{rms}^2} \end{aligned} \tag{17.72}$$

Simplifying with Eqs. (17.68) and (17.69),

$$\frac{R_{eff}}{R_{dc}} = 1 + \frac{5p^2 - 1}{45}\Delta^4 \left[\frac{I'_{rms}}{\omega I_{rms}}\right]^2 \tag{17.73}$$

Define R_δ as the DC resistance of a layer of thickness δ, rewriting Eq. (17.73)

$$R_{eff} = R_\delta \left\{ \frac{1}{\Delta} + \frac{5p^2 - 1}{45}\Delta^3 \left[\frac{I'_{rms}}{\omega I_{rms}}\right]^2 \right\} \tag{17.74}$$

Recall that Δ is defined at the fundamental frequency of the periodic waveform.

A typical graph of effective resistance versus layer thickness for a periodic waveform is shown in Fig. 17.17. For thin layers (less than a skin depth), the resistance is high and decreases as the thickness increases until the proximity effect kicks in and increases the effective resistance. There is an optimum thickness that minimizes the overall loss, and this may be found by taking the derivative of Eq. (17.74) w.r.t. Δ to yield

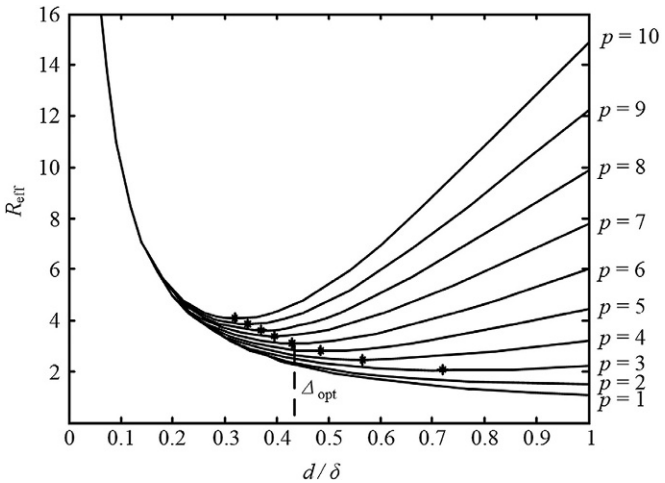


FIG. 17.17 Effective resistance as a function of layer thickness.

$$\Delta_{opt} = \sqrt[4]{\frac{15}{5p^2-1}}\sqrt{\frac{\omega I_{rms}}{I'_{rms}}} \tag{17.75}$$

and at this optimum value of the layer thickness, the effective resistance is

$$\frac{R_{eff}}{R_{dc}} = \frac{4}{3} \tag{17.76}$$

17.5.1 Example: Push-Pull Converter

In the push-pull converter design, we had a choice between the 2.5 mm diameter wire and the 24.5×0.2 mm foil in the secondary. We can approximate the current in the secondary to the pulsed waveform shown in Fig. 17.18 with a finite rise time, and it may be easily established that

$$\begin{aligned} I_{rms} &= I_o\sqrt{D'' - \frac{4t_r}{3T}} \\ I'_{rms} &= I_o\sqrt{\frac{2}{t_r T}} \end{aligned} \tag{17.77}$$

and

$$\Delta_{opt} = \sqrt[4]{\frac{15}{5p^2-1}}\sqrt[4]{\left[D - \frac{4t_r}{3T}\right]2\pi^2\frac{t_r}{T}} \tag{17.78}$$

For a rise time of $t_r/T = 2.5\%$, the optimum value of Δ is 0.459 and the optimum foil thickness at 80 kHz, with a skin depth of 0.233 mm, is 0.1 mm. This is the foil thickness we used in the example for the push-pull converter. The effective resistance is 4/3 times the DC resistance, so the total copper loss in the secondary windings is now $(4/3) \times 0.831 \times 2 = 2.216$ W, bringing the total losses to 3.795 W.

If we had selected the 2.5 mm diameter wire, the AC resistance factor from Eq. (17.62) is 3.0, and the total copper loss would be 3.738 W; coupled with the core loss, the total losses would have exceed the maximum dissipation of 5.0 W.

17.5.2 Fringing Effect

In order to limit the maximum flux density in the magnetic core of an inductor, the air gap is usually placed in the core, as shown in Fig. 17.11. Besides, the air gap is required even for the transformer applied in the LLC resonant converter to guarantee the proper magnetizing inductance. Basically, the reluctance of the air gap could be calculated based on the same cross-sectional area of the magnetic core and the actual gap length, as discussed in Section 17.3. According to the magnetic field distribution between two different materials, that is, ferrite and air, derived by the Maxwell equations, the magnetic flux line around the air gap bulges out as presented in Fig. 17.19, which is normally named the "fringing effect." Due to the variation in the magnetic field of the component, the inductance must be evaluated with the fringing field taken into account which means the calculated method given in Section 17.3 should be improved. The fringing field will increase the power loss of conductors near the air gap under AC conditions because the magnetic field around the conductor is not uniform. Consequently, the fringing effect is significant for the magnetic design.

The magnetic field around the air gap depends on the dimensions of the gap and the position in the core. Typically, finite element analysis (FEA) is the most accurate method to obtain the inductance. Fig. 17.20 shows the fringing flux for an inductor with an air gap in the outer leg of the core.

FEA simulation is resource and time-consuming. A simple and effective method to estimate the increase in inductance due to fringing is presented in Fig. 17.21. The cross section of the gap is a rectangular area with dimensions x by y.

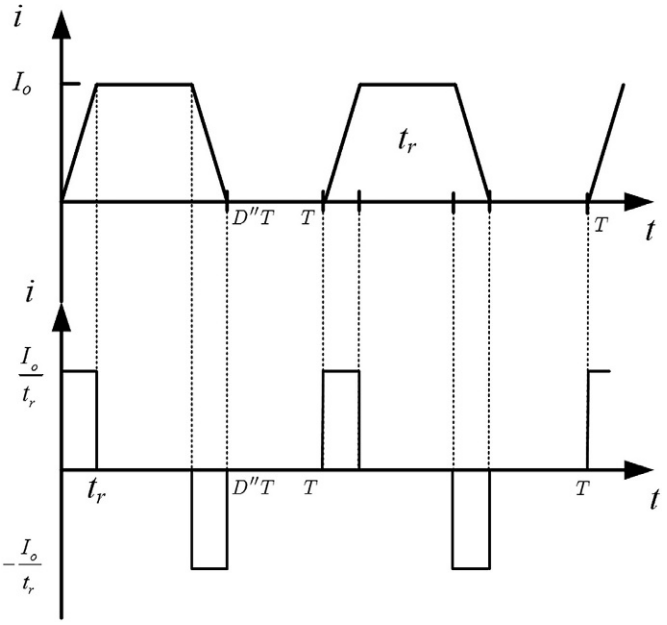


FIG. 17.18 Pulsed waveform for the push-pull converter.

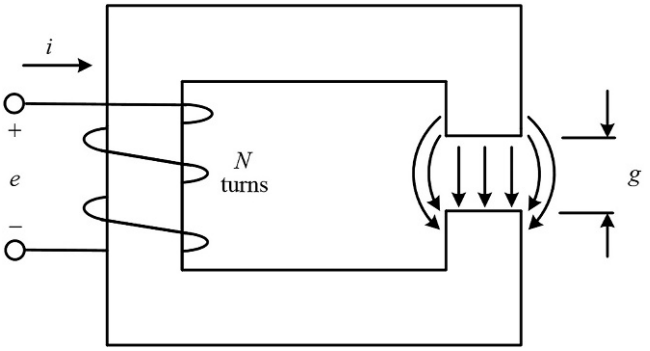


FIG. 17.19 Fringing effect around the air gap.

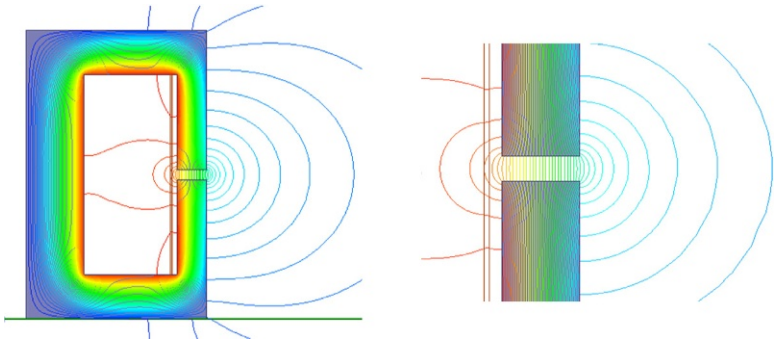


FIG. 17.20 Fringing flux simulated by finite element analysis.

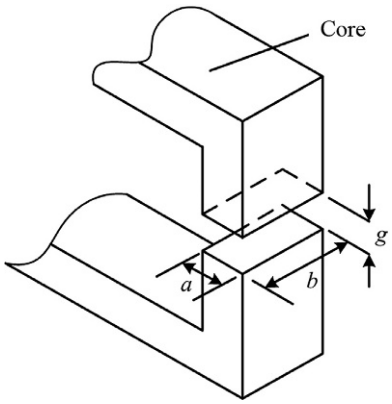


FIG. 17.21 Inductor with an air gap in the core.

Assuming the gap length is g, the equivalent cross-sectional area of the air gap can be set as $(x+g)$ by $(y+g)$ instead of x by y to calculate the inductance by the following equation:

$$L' = \frac{N^2}{R_c + R'_g} \asymp \frac{N^2}{R'_g} = L\frac{(x+g)(y+g)}{xy} \tag{17.79}$$

where R_c and R'_g are the reluctances of the core and the equivalent gap, N is the number of turns in the inductor and L is the inductance calculated by Eq. (17.16).

The gap length would be very small in practice. With the assumption that g is much smaller than x or y, Eq. (17.79) can be rewritten as

$$L' \asymp L\left(1 + \frac{x+y}{xy}g\right) \tag{17.80}$$

For a magnetic core with a square cross section, the inductance will be increased by the factor of $(1 + 2\,g/x)$. If the inductor has a circular core, the equivalent diameter of the air gap should be increased by g.

The fringing field will lead the nonuniform current density in the conductor near the air gap and result in extra loss in the winding. The winding loss due to the air gap is dependent on the operating frequency of the magnetic component. Fig. 17.22 shows the current density in the conductor near the gap for the same inductor at frequencies of 1 and

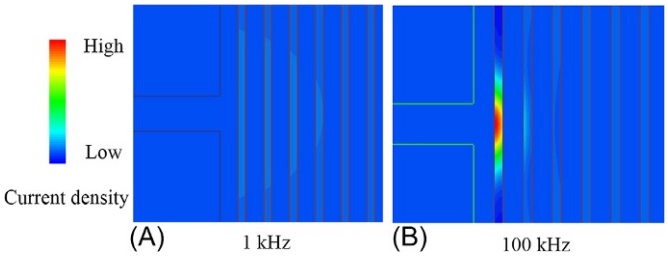


FIG. 17.22 Inductor with an air gap in the core.

100 kHz, respectively. It is obvious that the extra winding loss at high-frequency is significantly larger than it is at low frequency.

Due to the complex fringing field distribution around the gap, a simple and accurate analytic expression to evaluate the winding loss considering the fringing effect is not available. Several representative methods to calculate the fringing loss have been proposed [17–19]; all of these methods have substantial limitations. Simulation by finite element analysis is the most accurate method to evaluate the winding loss due to the air gap.

A number of proposals have emerged to reduce the fringing effect on the winding loss. The windings may be placed away from the air gap or may have a particular shape [20]. The recommended distance between the conductor and the air gap should be larger than twice the gap length. The other frequently implemented method to reduce the fringing loss is to apply a distributed gap in the core to replace the discrete large air gap [21].

17.5.3 High-Frequency Litz Wire

Litz wires consist of a number of fine strands that are twisted together, forming a compact bunch, and are externally connected in parallel. Insulated and enameled copper or aluminum strands are the most commonly used conductors. Multistranded cables are used in order to reduce the AC losses in thick conductors.

An easy process of manufacturing litz wires simply consists of twisting together a set of isolated strands. Other improved manufacturing methods can include some combination of braiding, twisting, or weaving processes. Ideally, strands should be equivalent in order to effectively share the currents and

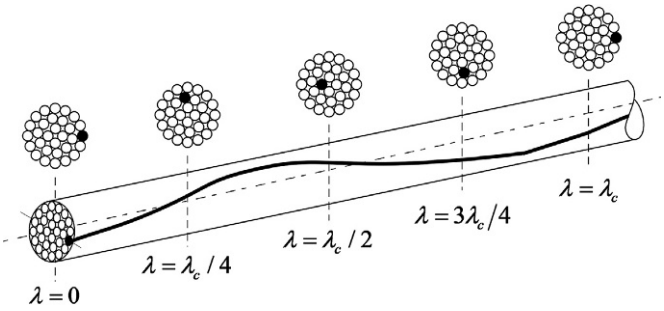


FIG. 17.23 Litz wire ideal structure of a multistranded conductor.

minimize the losses. However, equivalence of strands requires a carefully designed transposition pattern to guarantee that each strand occupies every place in the cross section for a periodic length of the cable λ_c, as it is schematically represented in Fig. 17.23. Achieving the ideal litz wire structure becomes complicated in conventional implementations, especially for cables with a high number of strands.

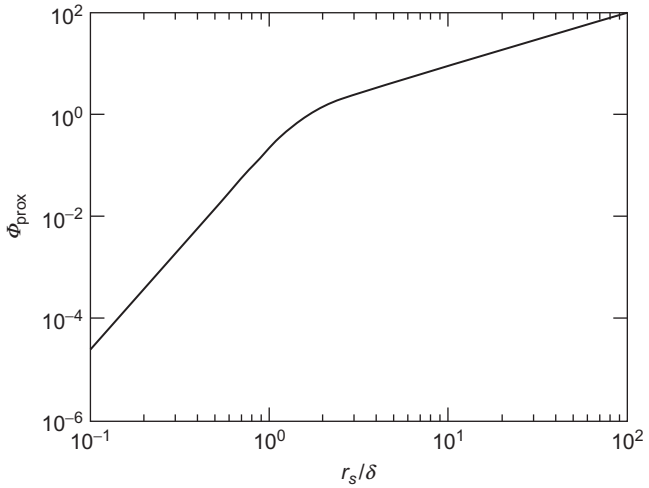


FIG. 17.24 Proximity losses of a round conductor with respect to the ratio of the strand radius to the skin depth.

Considering round conductors, skin and proximity effects are penalized when the ratio of radius to the skin depth is high. The nature of the skin effect was shown in Section 17.5, where the increase of the dc resistance with respect to geometry and frequency was characterized by means of the factor Φ_{skin}. On the other hand, considering the proximity effect, the factor Φ_{prox}, shown in Fig. 17.24, represents the induced losses on a round conductor per unit of length by an external alternating magnetic field (e.g., generated by nearby conductors), with respect to the ratio of the conductor radius to the skin depth. In both cases, the AC losses are strongly penalized when the ratio r_s/δ is higher than one, which points the convenience of using multistranded conductors.

Apart from the reduction of ac losses, litz wires present some disadvantages, including the high cost with respect to round wires. In general, litz wire winding requires more space than the equivalent round wire implementation because the fill factor is deteriorated.

Losses in multistranded wire correspond to the sum of the losses in its individual strands. These loses comprise DC resistance and skin and proximity effects. Skin and proximity effects may be further divided into strand-level and bundle-level effects [22], where the latter effects relate to unequal sharing of current in strands.

Bundle-level proximity effect loss can be controlled by simple twisting, that is, angular transposition. Bundle-level skin effect can be controlled by a complex transposition pattern that involves both radial and angular transposition of the strands. Radial transposition would involve each strand occupying all the other strand positions, whereas in angular transposition all the outside strands are transposed into other outside positions.

Simple twisting achieves angular transposition, but not radial transposition. In practice it is difficult to achieve radial transposition in a manufacturing environment. The skin effect at bundle-level is illustrated in Fig. 17.25 with simple twisting,

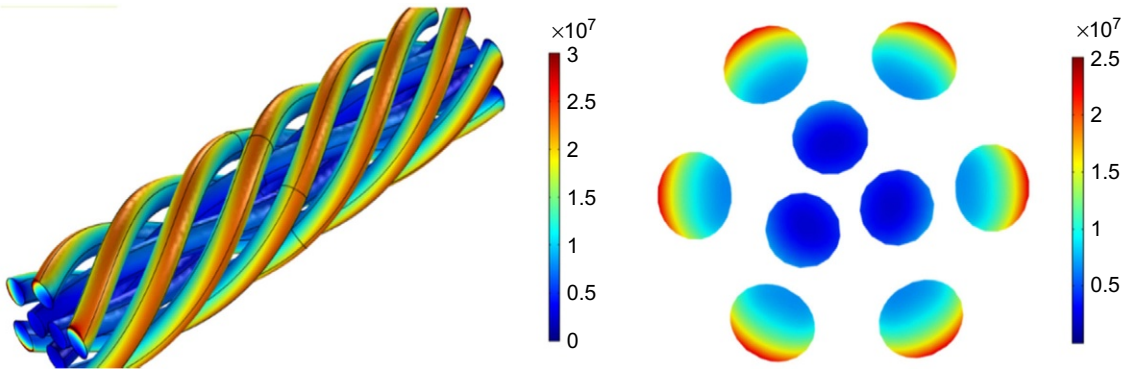


FIG. 17.25 Bundle-level skin effect in a twisted litz wire.

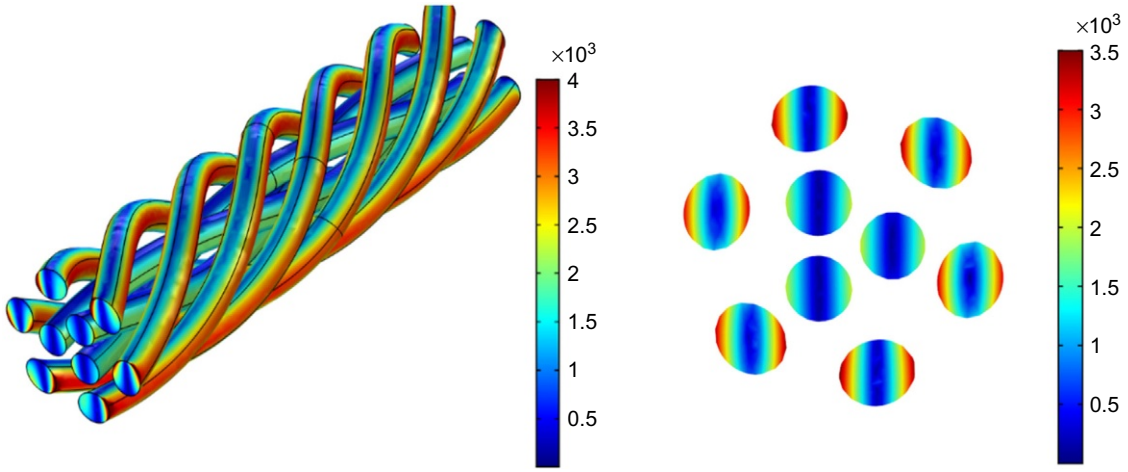


FIG. 17.26 Strand-level external proximity effect in a twisted litz wire.

where to a large extent the wire acts like a solid conductor from the point of view of skin effect.

Skin effect at the strand-level is covered in Section 17.5 where each strand must meet the requirements of individual wires as discussed, that is, $r_s/\delta_s < 1$. The proximity effect at strand-level has two components. The internal component takes into account the losses induced in a strand by the neighboring strands. The external component is generated by the other turns in a winding; this is analogous to the Dowell effect discussed in Section 17.5. The external proximity effect is illustrated in Fig. 17.26, where the Dowell effect is evident.

Several approaches to optimizing litz wire are available in the literature [23,24]; it is difficult to generalize, but as a rule of thumb, the strand diameter should be less than $\delta_s/4$.

Apart from the cost, winding volume restrictions should be taken into account when small strands are used because the copper utilization factor is deteriorated due to the isolation between strands. Values of the utilization factor k_u with respect to the radius of strand were measured and are shown in some references [14]. The fit to these values has the following expression:

$$k_u \asymp \frac{\pi}{4}\frac{\pi}{2\sqrt{3}}\left(\frac{r_s}{r_s + t_{\text{ins}}}\right)^2 \tag{17.81}$$

where t_{ins} is the thickness of the insulation. An image of these values and the fit are shown in Fig. 17.27. Needless to say, the final value of k_u will be even smaller when the insulation to satisfy international standards on electric isolation between the windings is included. The sizing formula for A_p in Eq. (17.45) shows that the reduced value of k_u will greatly influence the overall core size, for example, a 40% reduction in the window utilization factor due to litz wire will result in a 30% increase in core size.

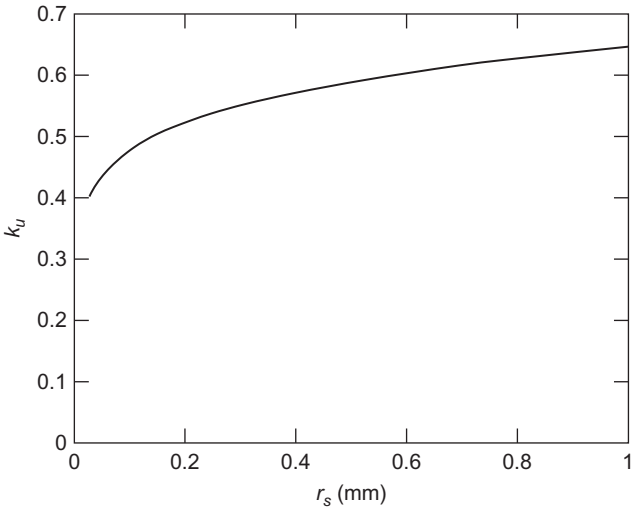


FIG. 17.27 Copper utilization factor in litz wire.

17.5.4 Interleaving

Another approach to reducing losses is to interleave the windings. Take the original transformer in Fig. 17.28; the losses dominate the primary and secondary windings at the interface between the two windings, where the magnetic field intensity is highest.

The plot of current density shows that the highest (red) values are at the interface of the primary and secondary winding; in the interleaved case, the maximum value of the magnetic field is reduced, and the current density is reduced accordingly.

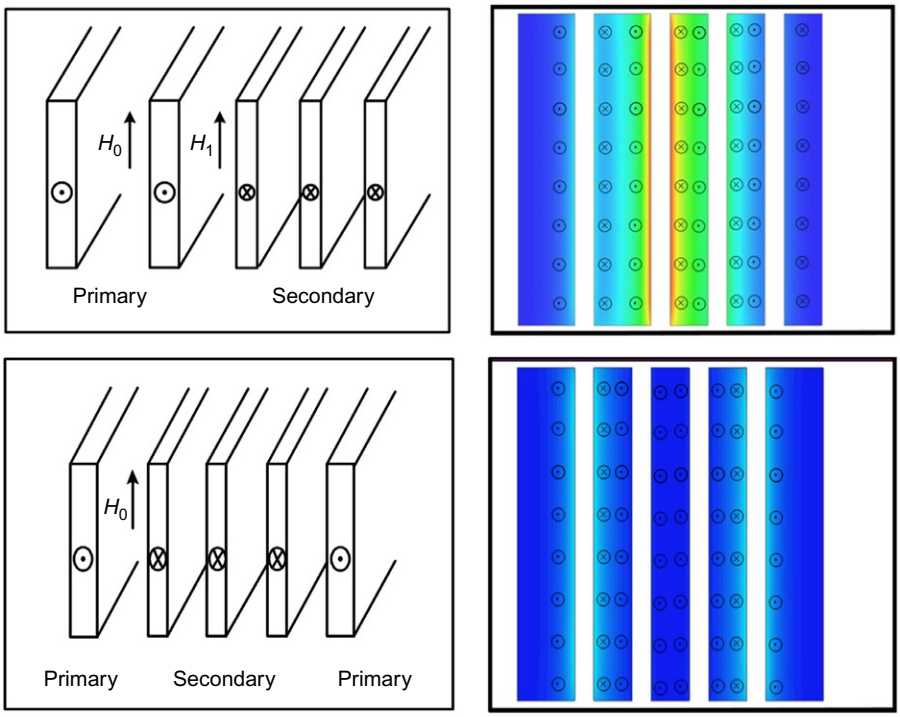


FIG. 17.28 Interleaved windings to reduce proximity effect losses.

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References

[1] T. Takamiya, K. Hanazawa, T. Suzuki, Recent Development of Grain-Oriented Electrical Steel in JFE Steel: JFE Technical Report, Available from: http://www.jfe-steel.co.jp/en/research/report.html, 2016. Accessed 23 February 2017.

[2] B.J. Lyons, J.G. Hayes, M.G. Egan, Experimental investigation of iron-based amorphous metal and 6.5% silicon steel for high-current inductors in low-medium frequency DC-DC converters, in: Proceedings of the Industry Applications Conference, 2007, IEEE 42nd IAS Annual Meeting, New Orleans, LA, 2007, pp. 1781–1786.

[3] G. Herzer, Modern soft magnets: amorphous and nanocrystalline materials, Acta Mater. 61 (3) (2013) 718–734.

[4] M. Ludwig, M. Duffy, T. ODonnell, P. McCloskey, S. OMathuna, Design study for ultra-flat PCB-integrated inductors for low-power conversion applications, IEEE Trans. Magn. 39 (5) (2003) 3193–3195.

[5] C. Marxgut, J. Muhlethaler, F. Krismer, J.W. Kolar, Multiobjective optimization of ultraflat magnetic components with PCB-integrated core, IEEE Trans. Power Electron. 28 (7) (2013) 3591–3602.

[6] N. Wang, R. Miftakhutdinov, S. Kulkarni, C. O'Mathuna, High efficiency on Si-integrated microtransformers for isolated power conversion applications, IEEE Trans. Power Electron. 30 (10) (2015) 5746–5754.

[7] J. Kim, M. Kim, F. Herrault, J. Park, M.G. Allen, Highly laminated soft magnetic electroplated CoNiFe thick films, IEEE Magn. Lett. 4 (2013).

[8] D. Yao, C.G. Levey, R. Tian, C.R. Sullivan, Microfabricated V-groove power inductors using multilayer Co–Zr–O thin films for very-high-frequency DC–DC converters, IEEE Trans. Power Electron. 28 (9) (2013) 4384–4394.

[9] D.V. Harburg, G.R. Khan, F. Herrault, J. Kim, C.G. Levey, C. R. Sullivan, On-chip RF power inductors with nanogranular magnetic cores using prism-assisted UV-LED lithography, in: Transducers & Eurosensors XXVII, 17th International Conference on Solid-State Sensors, Actuators and Microsystems, Barcelona, 2013, pp. 701–704.

[10] K. Overshott, The causes of the anomalous loss in amorphous ribbon materials, IEEE Trans. Magn. 17 (6) (1981) 2698–2700.

[11] J. Li, T. Abdallah, C.R. Sullivan, Improved calculation of core loss with nonsinusoidal waveforms, in: Industry Applications Conference, 2001. Thirty-Sixth IAS Annual Meeting. Conference Record of the 2001 IEEE, Chicago, IL, USA, 2001, pp. 2203–2210.

[12] K. Venkatachalam, C.R. Sullivan, T. Abdallah, H. Tacca, Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only Steinmetz parameters, in: Computers in Power Electronics, 2002. Proceedings. 2002 IEEE Workshop on, 2002, pp. 36–41.

[13] J. Muhlethaler, J. Biela, J.W. Kolar, A. Ecklebe, Improved core-loss calculation for magnetic components employed in power electronic systems, IEEE Trans. Power Electron. 27 (2) (2012) 964–973.

[14] W.G. Hurley, W.H. Wolfle, Transformers and Inductors for Power Electronics: Theory, Design and Applications, first ed., Wiley, Chichester, West Sussex, UK, 2013.
[15] C. Carretero, J. Acero, R. ALonso, TM-TE decomposition of power losses in multi-stranded litz-wires used in electronic devices, Prog. Electromagn. Res. 123 (2012) 83–103.
[16] P.L. Dowell, Effects of eddy currents in transformer windings, Proc. Inst. Electr. Eng. 113 (8) (1966) 1387–1394.
[17] P. Wallmeier, Improved analytical modeling of conductive losses in gapped high-frequency inductors, IEEE Trans. Ind. Appl. 37 (4) (2001) 1045–1054.
[18] W.A. Roshen, Fringing field formulas and winding loss due to an air gap, IEEE Trans. Magn. 43 (8) (2007) 3387–3394.
[19] A. Stadler, R. Huber, T. Stolzke, C. Gulden, Analytical calculation of copper losses in litz-wire windings of gapped inductors, IEEE Trans. Magn. 50 (2) (2014) 81–84.
[20] J.D. Pollock, C.R. Sullivan, Gapped-inductor foil windings with low AC and DC resistance, in: Proceedings of the IEEE Industry Applications Conference, 2004, p. 557.
[21] N.H. Kutkut, D.M. Divan, Optimal air-gap design in high-frequency foil windings, IEEE Trans. Power Electron. 13 (5) (1998) 942–949.
[22] A.W. Lotfi, F.C. Lee, A high frequency model for litz wire for switch-mode magnetics, in: Proceedings of the 1993 IEEE Industry Applications Society Annual Meeting, (IAS), vol. 2, 1993, pp. 1169–1175.
[23] C.R. Sullivan, Optimal choice for number of strands in a litz-wire transformer winding, IEEE Trans. Power Electron. 14 (1999) 283–291.
[24] I. Lope, J. Acero, C. Carretero, Analysis and optimization of the efficiency of induction heating applications with litz-wire planar and solenoidal coils, IEEE Trans. Power Electron. 31 (7) (2016) 5089–5101.

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Section III

General Applications

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18

Solid-State Pulsed Power Modulators and Capacitor Charging Applications

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18.1 Introduction

Pulsed power, PP, can be considered as the science and technology of accumulating electric energy over a relatively long period of time, followed by the subsequent energy release in very short pulses, a single one or a controlled repetitive sequence, thus increasing the instantaneous peak power. Supposing zero losses, the output energy E_o, delivered at power P_o during T_o, equals the accumulated energy E_i at a power P_i during T_i, bringing

$$E_i \approx E_o \Rightarrow P_i T_i \approx P_o T_o \Rightarrow \frac{P_o}{P_i} \approx \frac{T_i}{T_o} \tag{18.1}$$

An example is shown in Fig. 18.1, where a stored energy of 1 kJ can be discharged into a long pulse of 1 kW for 1 s or a short pulse of 1 GW for 1 μs, respectively, considering the ideal case of a lossless system.

PP is a technique primarily developed for radars, accelerators, and military applications but with great potential for civil applications [1]. In fact, there is a growing variety of environmental, biomedical, commercial, and industrial applications that use positive and/or negative high-voltage, HV, repetitive pulses, for enhancing the properties of a product or a technique [2]. These pulses may last from hundreds of picoseconds to tens of seconds, being released as a single shot or as a repetitive sequence up to several tens of thousands per second.

What makes PP so unique is the concept that extremely high peak powers can be delivered during short times without the demand for highly powerful energetic power sources, custom direct, dc, or alternating, ac, voltage systems being suited.

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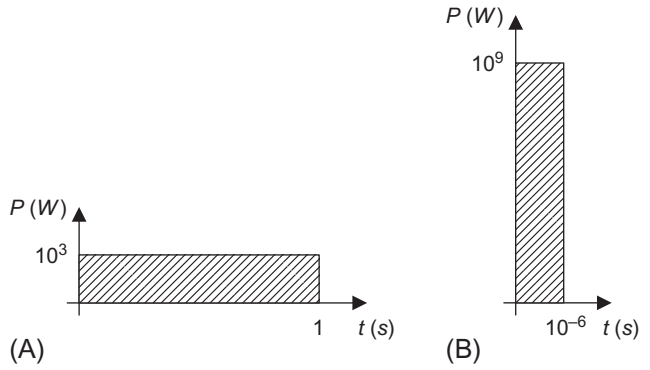


FIG. 18.1 Discharge of 1 kJ energy: (A) 1 kW during 1 s pulse and (B) 1 GW during 1 μs pulse.

In the past, the PP technology was dominated by vacuum or gas tubes (i.e., electronic valves) for switching the high-powers needed for military and large plant physical applications [3]. With the technological advent of power semiconductors in the 1970s and particularly modern power semiconductors in the 1990s, developing PP generators based on power semiconductors was possible. Still, they were lower power rated compared with electronic valve generators but largely rewarded by the higher energetic efficiency and flexibility together with compactness and cost-effectiveness [4].

Nowadays, the applications of PP are driving the need for technological advances in medical, environment, biological, energetic, and industrial applications, for example, in the reduction of pollution emissions from fossil fuels, in killing bacteria and organic pollutants, in melanoma cancer treatment, and in molding metals sheets [5–9].

This chapter provides basic concepts and advanced know-how on the generation of repetitive HV pulses using state-of-the-art power semiconductor technology. Apart from this introduction, in Section 18.2, power semiconductor devices used in solid-state-based high-voltage generators are reviewed together with the latest silicon carbide (SiC) insulated-gate bipolar transistor (IGBT) and metal-oxide-semiconductor field-effect (MOSFET) through the latest gallium nitride (GaN) power junction field-effect transistors (JFET). In Section 18.3, several types of PP applications are presented, and the type of load requirements they present to the high-voltage modulators is described. The most widespread semiconductor-based HV pulse modulator topologies are analyzed and discussed in terms of solid-state device operation in Section 18.4. In Section 18.5, capacitor charging applications are presented and described. The main conclusions about semiconductor use in high-voltage pulse generation are presented in Section 18.6 and the future trends on this technology.

18.2 Power Semiconductors for PP

The demand for high-voltage modulators to generate repetitive high-voltage pulses with optimized performance and characteristics, based in solid-state technology, is being fulfilled through the enhancement of the volt-ampere capabilities and switching speed of modern power semiconductors.

Still, using power semiconductors in PP is a matter of optimizing their use, going beyond the present semiconductor ratings and taking advantage of usually nonuseful phenomena or nonideal characteristics, such as controlled avalanche breakdown (for avalanche transistors), diode reverse recovery sharpness that can generate inductive high-voltage pulses, Zener capacitances, peak currents, and unusual very short pulse behavior.

In the next sections, the particular characteristics of power semiconductors enabling their use in PP applications will be summarized, from silicon (Si) high-voltage diodes, silicon-controlled rectifier thyristors (SCR), gate turn-off thyristor (GTO), gate-controlled thyristor (GCT), integrated gate-commutated thyristor (IGCT), injection enhanced gate transistor (IEGT), insulated-gate bipolar transistor (IGBT), and metal-oxide-semiconductor field-effect transistors (MOSFET) to the latest silicon carbide (SiC) IGBTs or gallium nitride (GaN) power junction field-effect transistors (JFET) (also termed enhancement-mode high-electron-mobility transistor (E-HEMT)). To overcome the still limited hold-off voltages of power semiconductors and their current ratings (Fig. 18.2), regarding the electronic valves, some techniques will be described, including series and parallel semiconductor arrangements, and the source switching of a JFET using a low-voltage MOSFET (cascode stacks).

Much attention is being devoted to power semiconductors based on silicon carbide (SiC) structures, which can switch voltages in the tens of kV range and currents nearing the kA barrier. The 4H-SiC MOSFET is being investigated for 12–15 kV, while SiC IGBTs are now in the 15 kV range (Fig. 18.2). Alternative semiconductor materials, such as gallium nitride (GaN), are being investigated to build GaN enhancement-mode JFETs called HEMTs (available 650 V, 60 A, and 25 mΩ). GaN JFETs are expected to be faster devices (100 MHz switching frequency and 10 ns switching time) than SiC or Si power semiconductors. The cascode switch is expected to attain 10 kV blocking voltages.

Superjunction (SJ) transistors are being researched to build bipolar power transistors; super trench MOSFETs (STM), vertical deep trench (resurf diffusion MOS-VTR-DMOS), SJ DMOS, UMOS, JFET, and JFET-derived structures are also being considered [4].

18.2.1 High-Voltage PIN Diodes (Step Recovery Diodes SRD)

Fig. 18.3A shows the simplified structure of a typical Si high-voltage high-power diode with forward bias carriers in Fig. 18.3A [10]. This type of diode has a heavily doped P^+ anode and N^+ substrate separated by a lightly doped N^- (or near intrinsic, I) epitaxial layer, called drift region [11]. The drift region, usually not found in low-power diodes, has to contain

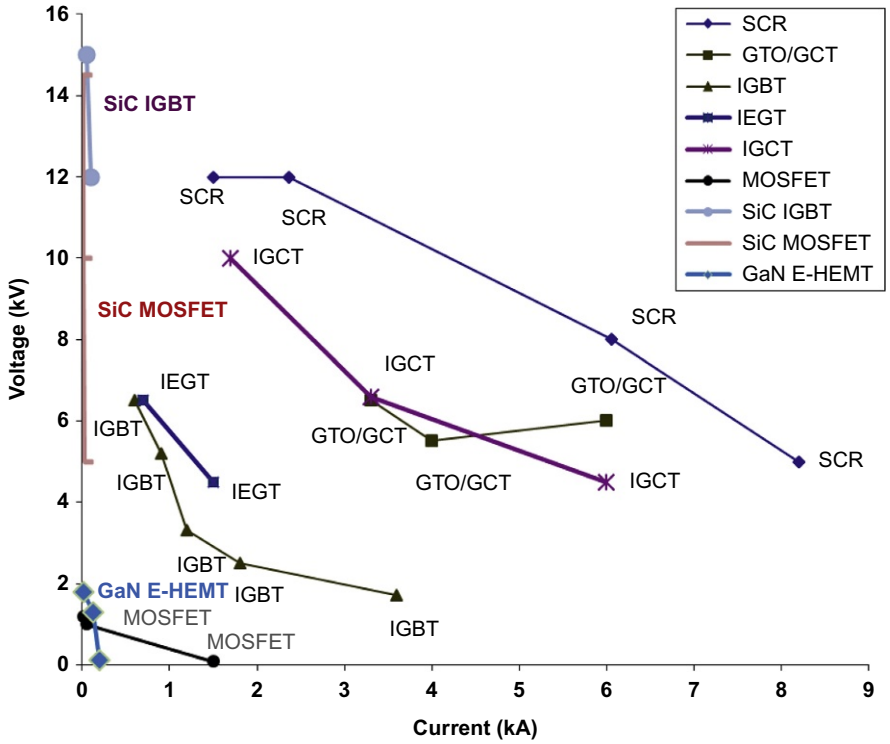


FIG. 18.2 Maximum volt-ampere capabilities of current Si (SCR, GTO/MCT, IGCT, IEGT, IGBT, and MOSDET), SiC (MOSFET and IGBT), and GaN (E-HEMT) high-power semiconductors.

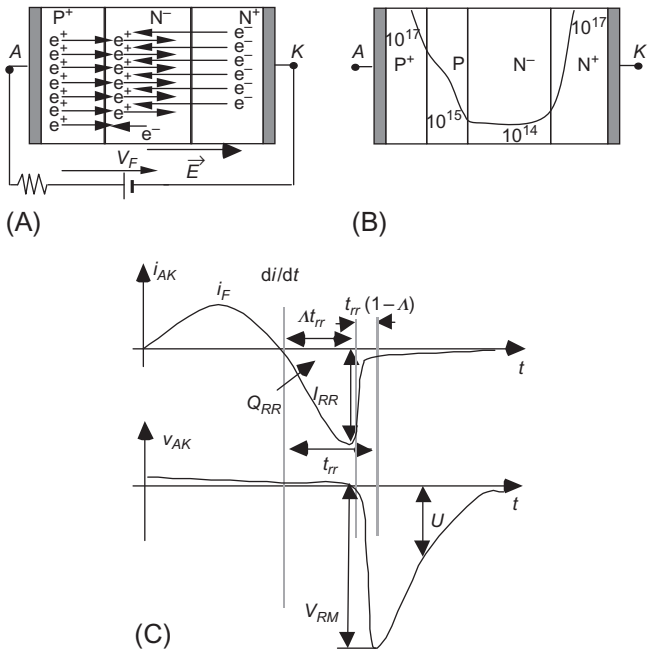


FIG. 18.3 (A) Forward-biased PIN diode, (B) $P^+PN^-N^+$ SOS diode structure and typical doping profile, and (C) SOS diode reverse-blocking behavior.

the thick depletion layer of the reverse-biased high-voltage PIN diode, establishing the diode reverse breakdown (or hold-off) voltage rating (punch-through diodes).

PIN diodes turn-on requires the depletion layer removal (forward voltage recovery, as the diode is reverse-biased prior to turn-on). Removal of the stored depletion charge needs a certain current and time. Forward conduction is dominated by high-level injection of holes (conductivity modulation) in the drift region, which becomes a virtual P region. The minority injected charge is positive if the diode is conducting, the forward current providing minority carriers at the rate they recombine. The *on*-state voltage is relatively high, the electric field extending through the drift region. This electric field is need to the transport of charge carriers from P to N region.

To turn-off the PIN diode, the stored excess carriers, mostly in the drift region, must be discharged before the diode reverse biases, the minority charge becoming negative (reverse recovery). Upon applying a reverse voltage U_R, the forward current will decrease (Fig. 18.3C) at a rate of

$$\frac{di_F}{dt} \approx \frac{I_{RR}}{t_{rr}} \tag{18.2}$$

becoming negative to swept the excess carriers out of the drift region and charge the depletion capacitance C_{eqoff}, which is relatively small due to the wide drift region. At constant reverse U_R voltage applied in inductive circuits (L_S inductor), the diode reverse current rate of rise, considered constant, is

$$\frac{di}{dt} \approx \frac{U_R}{L_S} \tag{18.3}$$

reaching the value I_{RR}

$$I_{RR} = t_{rr} \frac{U_R}{L_S} \tag{18.4}$$

at the reverse recovery time t_{rr}

$$t_{rr} = L_S \frac{I_{RR}}{U_R} \tag{18.5}$$

being the reverse recovery charge Q_{RR}

$$Q_{RR} = \frac{I_{RR} t_{rr}}{2} \tag{18.6}$$

In LC oscillating circuits (Fig. 18.4), the PIN diode may become reverse-biased by a negative fast-rising voltage with high peak value V_{RM}, which can be more than three times higher than the applied direct voltage U (Fig. 18.3C).

At high reverse voltages, the pulse energy must be limited to avoid the impact ionization current destroying the diode by avalanche breakdown and excessive power dissipation. Therefore, PIN diodes should be used with very short pulses, sharpening and increasing the voltage amplitude of the applied pulses.

Semiconductor opening switches (SOS), also known as step recovery diodes (SRD), charge diodes or snap diodes, are modified PIN high-voltage diodes using a $P^+PN^-N^+$ structure with gradually doped P layer (Fig. 18.3B) [12]. The diode injected minority carriers must not have the time to recombine and should not diffuse too far from the junction before they are withdrawn under reverse bias with a reverse current. The minority carrier lifetime of the SOS diode determines the pulse length. SOS diodes are thus optimized to exhibit relatively slow reverse recovery ($\Lambda t_{rr} \approx 50$–$100$ ns) but abrupt recovery (very fast reverse current decay) $(1-\Lambda)t_{rr} \approx 5$ ns (Fig. 18.3C).

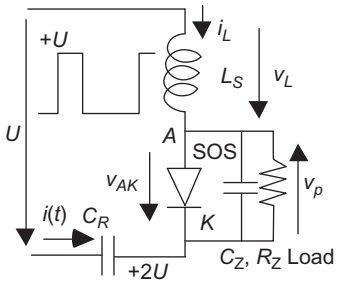


FIG. 18.4 SOS pulse generation using magnetic energy storage.

SOS diode characteristics depend not only on the pumping forward current (current density and very short time to avoid saturation) but also on the doping profile of the $P^+PN^-N^+$ structure and carrier lifetime. The reverse recovery of SOS diodes (e.g., their opening) should differ from PIN diodes, since current interruption ought to occur mostly in the narrower P-doped layer, not in the drift layer. The SOS diode can switch high-currents (kA) in nanosecond opening times, with automatic uniform distribution of reverse voltage (kV) in series-connected SOS diodes during current decay. Series stacks of up to one thousand SOSs can be deployed to obtain working voltages near the megavolt level, peak currents of several kA, peak power of GW, and average powers of tens of kilowatts.

In a simplified circuit for SOS operation (Fig. 18.4), it is supposed that a rectangular prepulse with amplitude U and pulse length T_U is generated and applied to the SOS in series with an inductor L_S to charge the capacitor C_R.

During the positive part of the prepulse, the forward pumping period, the SOS diode is forward-biased, and the inductor near-sinusoidal current rises to build up energy in the resonant $L_S C_R$ circuit and excess carriers in the diode.

Supposing the $L_S C_R$ with zero series resistor r_S ($r_S \to 0$), then this LC is underdamped ($\zeta < 1$), the inductor current being given as

$$\begin{aligned} i_L &= I_m e^{-\zeta \omega_R t} \sin\left(\omega_R \sqrt{1-\zeta^2}\ t + \phi\right) \\ \zeta &= \frac{r_S}{2Z_R} \approx 0;\ \ Z_R = \sqrt{\frac{L_S}{C_R}};\ \ \omega_R = \frac{1}{\sqrt{L_S C_R}} \end{aligned} \tag{18.7}$$

The I_m and ϕ values are obtained from the initial conditions $i_L(0) = 0, v_{CR}(0) \Rightarrow v_L(0) = U$. Therefore,

$$i_L = \frac{U}{Z_R \sqrt{1-\zeta^2}} e^{-\zeta \omega_R t} \sin\left(\omega_R \sqrt{1-\zeta^2}\ t\right) \tag{18.8}$$

where Z_R is the characteristic impedance

$$Z_R = \sqrt{L_S / C_R} \tag{18.9}$$

of the $L_S C_R$ resonant tank with oscillation frequency ω_R, set to allow charging during T_U:

$$\omega_R = \sqrt{L_S C_R}^{-1} = \frac{\pi}{T_U} \tag{18.10}$$

Charging must occur only during half the oscillation cycle; thus, $T_U = (2\pi/\omega_R)/2$.

Neglecting losses ($L_S C_R$ resonant tank damping factor nearly zero), parasitic effects and diode voltage drops, the diode forward current is obtained from

$$i_L = \frac{U}{Z_R} \sin(\omega_R\ t) \tag{18.11}$$

with peak value

$$I_F \approx U/Z_R \tag{18.12}$$

Since $r_S \approx 0$, the capacitor C_R voltage is

$$v_{CR} = \frac{1}{C_R}\int_0^t \frac{U}{Z_R}\sin(\omega_R\, t)dt + v_{CR}(0) = U(1-\cos(\omega_R\, t)) \tag{18.13}$$

At $t = T_U = \pi/\omega_R$, the C_R capacitor will charge to nearly

$$V_{CR} \approx 2U \tag{18.14}$$

Neglecting the recombination decay time constant, the diode forward stored charge is nearly

$$Q_F \approx \frac{2I_F}{\omega_R} \approx \frac{2U}{\omega_R Z_R} \approx 2U\,C_R \tag{18.15}$$

During the sinusoidal negative oscillation interval, the diode is still conducting, the prepulse voltage is nearly zero, and the inductor current goes negative. The SOS diode reverse recovery instant (opening) happens at nearly the C_R discharge peak current

$$I_{RR} \approx \frac{2U}{Z_R} \approx 2I_F \tag{18.16}$$

being the reverse recovery charge

$$Q_{RR} \approx \frac{I_{RR}}{\omega_R} \tag{18.17}$$

nearly equal to the forward injected charge. Thus, the reverse recovery current is nearly the double of the peak forward current $I_{RR} \approx 2U/Z_R \approx 2I_F$, being

$$Z_R = \frac{2U}{I_{RR}} \tag{18.18}$$

Supposing diode abrupt recovery and assuming energy conservation, the v_p pulse voltage is dependent on the load capacitor C_Z and resistor R_Z; for underdamped $L_S C_Z || R_Z$ parallel circuits, ($\xi < 1$) given as

$$\begin{aligned} v_p &= V_m e^{-\xi\omega_Z t}\sin\left(\omega_z\sqrt{1-\xi^2}\; t + \phi\right) \\ \xi &= \frac{Z_z}{2R_z};\;\; Z_z = \sqrt{\frac{L_S}{C_z}};\;\; \omega_z = \frac{1}{\sqrt{L_S C_z}} \end{aligned} \tag{18.19}$$

where the load R_Z is in parallel with Z_Z, being $Z_Z = \sqrt{L_S/C_Z}$ the characteristic impedance of the second-order $L_S C_Z || R_Z$ parallel circuit with damping factor $\xi \approx Z_Z/(2R_Z)$ and undamped resonant frequency $\omega_Z \approx \sqrt{L_S C_Z}^{-1}$, driven by the initial current I_{RR} of inductor L_S.

The V_m and ϕ values are obtained from the initial conditions $v_p(0) = 0$ and $i_{Ls}(0) = I_{RR}$. Therefore,

$$v_p = I_{RR}\frac{Z_z}{\sqrt{1-\xi^2}} e^{-\xi\omega_Z t}\sin\left(\omega_z\sqrt{1-\xi^2}\, t\right) \tag{18.20}$$

The maximum voltage $v_{pmax} = V_{RM}$ occurs at $t = t_{peak}$ and is

$$\begin{aligned} t_{peak} &= \frac{\tan^{-1}\left(\sqrt{1/\xi^2 - 1}\right)}{\omega_z\sqrt{1-\xi^2}} \\ V_{RM} = v_{pmax} &= I_{RR} Z_z\, e^{-\frac{\xi\tan^{-1}\left(\sqrt{1/\xi^2-1}\right)}{\sqrt{1-\xi^2}}} \end{aligned} \tag{18.21}$$

The V_{RM} equation above can be used to determine the needed I_{RR} and then, using Eq. (18.18), the Z_R value.

For near-optimum energy transfer to the load resistor R_Z, a damping value slightly lower than the critical value should be used, the v_p pulse being roughly sinusoidal. Pulse forming networks or lines can be used to almost square it [12].

From the above equations, assuming a damping factor $0.7 < \xi < 0.9$, the design SOS diode pulser follows the steps:

$$\begin{aligned} &(1)\;\; \xi \approx 0.8 \;\; (\text{small oscillations}) \Rightarrow Z_z = 2\xi R_z \\ &(2)\;\; Z_R = \frac{2UZ_z}{v_{Pmax}} e^{-\frac{\xi\tan^{-1}\left(\sqrt{1/\xi^2-1}\right)}{\sqrt{1-\xi^2}}} \\ &(3)\;\; \omega_R = \frac{\pi}{T_U} \\ &(4)\;\; C_R = \frac{1}{\omega_R Z_R} \\ &(5)\;\; L_S = \frac{Z_R}{\omega_R} \\ &(6)\;\; C_Z = \frac{L_S}{Z_Z^2} \end{aligned} \tag{18.22}$$

This design considers the SOS properties are suitable, assuming that SOS diode carrier lifetime is long enough to nearly conserve charge, abrupt reverse recovery and zero *on*-state voltages (regarding the U values). Often, C_Z should account for the intrinsic SOS diode capacitance or nonabrupt diode recovery.

A simplified design, valid nearly for $0.75 < \xi < 1$, leads to slightly higher V_{RM} pulse voltages. Consider

$$V_{RM} \approx I_{RR}(R_Z || Z_Z) \quad \text{for } C_R \gg C_Z \tag{18.23}$$

To obtain a near-critical damped load ($0.7 < \xi < 0.9$), it must be

$$1.4R_Z < Z_Z < 2R_Z \tag{18.24}$$

Then, from the required V_{RM} and I_{RR} the Z_R value, it is

$$Z_R \approx \frac{2U(R_Z || Z_Z)}{V_{RM}} \tag{18.25}$$

and

$$\omega_R = \frac{\pi}{T_U}$$

Then, the resonant tank has values

$$L_S \approx \frac{Z_R}{\omega_R} \tag{18.26}$$

and

$$C_R \approx \frac{1}{\omega_R Z_R} \tag{18.27}$$

From L_S and Z_Z, the load parallel capacitor C_Z, either added or stray capacitance or SOS C_{eqoff}, should be

$$C_Z \approx \frac{L_S}{Z_Z^2} \tag{18.28}$$

For a required V_{RM} in load resistor R_Z and capacitor C_Z, the SOS diode must withstand

- forward current I_F,
- pumping time T_U,
- V_{RM} reverse voltage,
- reverse recovery current I_{RR},
- reverse recovery charge Q_{RR}.

High peak voltages V_{RM} and comparatively low values of I_{RR} need very low values of the load (spurious) parallel capacitance C_Z, or higher values of I_{RR}.

Example 18.1 Determine the circuit parameters of Fig. 18.4 to obtain a 30 ns 1 MV pulse in resistor $R_Z = 1\,\text{k}\Omega$ (1 MW peak) paralleled with C_Z capacitor, from a prepulse having $U = 300$ kV and pulse length T_U.

Solution Supposing volts × second conservation at equal current, the prepulse length should be

$$T_U \approx 30 \times 10^{-9} \times 10^6 / \left(300 \times 10^3\right) \approx 100\text{ ns}$$

Then, from the above equations, it is obtained

$$\omega_R = \pi / T_U = \pi / \left(100 \times 10^{-9}\right) \approx 3.14 \times 10^7\text{ rad/s}$$

If it is assumed $\xi = 0.75$, then

$$Z_Z \approx 2\xi R_Z \approx 1.5\, R_Z \approx 1.5\,\text{k}\Omega$$

$$Z_R = \frac{2UZ_z}{v_{Pmax}} e^{-\frac{\xi \tan^{-1}\left(\sqrt{1/\xi^2 - 1}\right)}{\sqrt{1-\xi^2}}} \approx 396\,\Omega$$

$$L_S \approx Z_R / \omega_R \approx 360 / 3.14 \times 10^7 \approx 12.6\,\mu\text{H}$$

$$C_R \approx 1/(Z_R \omega_R) \approx 1/\left(360 \times 3.14 \times 10^7\right) \approx 81\,\text{pF}$$

and

$$C_Z \approx L_S / {Z_Z}^2 \approx 12.6 \times 10^{-6} / 396^2 \approx 5.6\,\text{pF}$$

This is a low value considering the SOS diode (or diode association) equivalent off-depletion capacitance C_{eqoff}, not to forget stray capacitances. The SOS diode must withstand

$$I_F \approx U / Z_R \approx 300 \times 10^3 / 396 \approx 758\,\text{A}$$

$$I_{RR} \approx 2 I_F \approx 1.52\,\text{kA}$$

$$v_{pmax} = I_{RR} Z_z\, e^{-\frac{\xi \tan^{-1}\left(\sqrt{1/\xi^2 - 1}\right)}{\sqrt{1-\xi^2}}} \approx V_{RM} \approx I_{RR}(R_Z \| Z_Z) \approx 1520 \times 600 \approx 10^6\,\text{V}$$

$$Q_{RR} \approx I_{RR} / \omega_R \approx 1520 / \left(3.14 \times 10^7\right) \approx 50\,\mu\text{C}$$

Excess carrier (holes) mean lifetime (reciprocal of recombination decay) should be higher than 1 μs and diode reverse recovery time should be

$$t_{rr} \approx \pi / (2\omega_R) \approx \pi \sqrt{L_S C_R} / 2 \approx 50\,\text{ns}$$

that is, nearly half of the forward pumping time.

Since the damped resonant frequency is

$$\omega_{Zd} = \omega_Z \sqrt{1 - \xi^2}$$

the pulse duration (settling time) is close to

$$T_p = \pi / \left(\omega_Z \sqrt{1 - \xi^2}\right) = \pi \sqrt{L_S C_Z} / \sqrt{1 - \xi^2} \approx 34\,\text{ns}$$

This is near the required 30 ns, as can be seen in Fig. 18.5. Designs for higher C_Z values require damping factors ξ toward 0.5, which increase SOS diode ratings (I_F, I_{RR}, and Q_{RR}) but would allow the doubling of C_Z capacitances.

This SOS pulse generator multiplies the incoming prepulse amplitude by a factor slightly higher than 3.

Given the present capabilities of SOS diodes (nearly 1 kA and 1 kV), this 1 MV pulse modulator would require

1. an array of some thousands of SOS diodes arranged in a series of few paralleled diodes;
2. oil isolation and cooling, complemented with water/air heat sinking;
3. special care to minimize parasitic inductances and capacitances.

Other SOS devices use unique diffusion techniques to achieve ultrafast switching times, such as the drift step

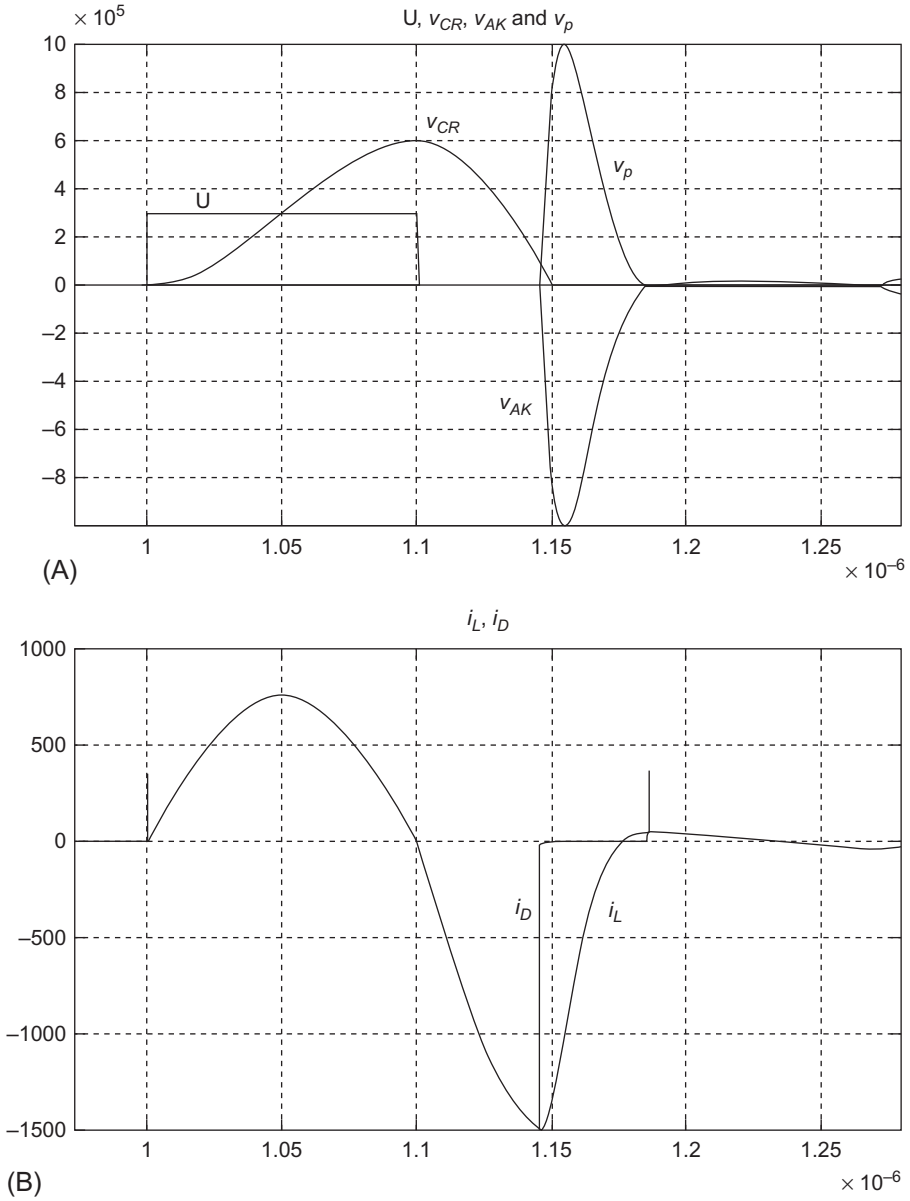


FIG. 18.5 SOS v_p pulse generated using magnetic energy storage. (A) Upper graph shows waveforms of U, v_{CR}, v_{AK}, and v_p in volts and (B) waveforms of i_D and i_L in amperes in the lower graph.

recovery device (DSRD), the inverse recovery diode (IRD), and the delayed ionization device (DID). Each device is capable of producing pulses ranging from 1 to 10 kV, with rise times between 100 ps and 1 ns.

The PIN diode-based silicon avalanche sharpener (SAS) is a sharpening device that shortens the pulse rise time. Usually, it works reverse-biased, a slow rise time and short reverse pulse being applied to the SAS in order to avalanche it. When avalanche breakdown of the SAS drift layer occurs, a very short rise time pulse is applied to the load. Avalanche breakdown does not destroy the SAS if the input pulse is short enough.

18.2.2 Metal-Oxide Semiconductor Technology Transistors

18.2.2.1 Metal-Oxide Semiconductor Field-Effect Transistors (MOSFET)

MOSFETs are very fast unipolar-carrier enhancement-mode semiconductor devices controlled by the electric field associated to the v_{GS} voltage applied at the gate-source terminals (Fig. 18.6A) [10–13]. Their speed is mostly due to the absence of carrier recombination since in N-type MOSFETs the carriers are almost only electrons. MOSFET semiconductor structure forms an $N^+N^-PN^+$ shorted base-emitter bipolar transistor

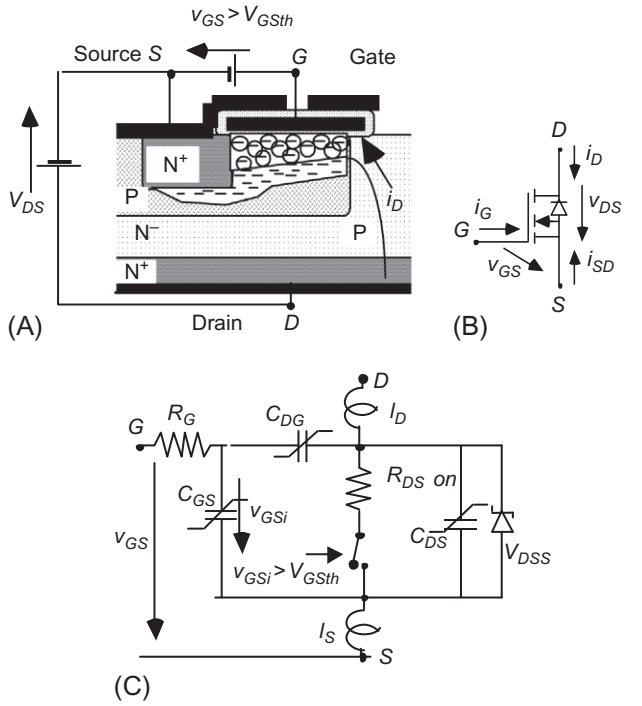


FIG. 18.6 (A) MOSFET structure showing the DS current path, (B) electronic symbol including intrinsic diode, and (C) MOSFET model with parasitic components.

(Fig. 18.6A), which is often referred as behaving as an intrinsic antiparallel PIN diode (Fig. 18.6B).

The MOSFET has the capabilities for high-speed switching in the nanosecond or subnanosecond range [14,15].

In PP applications, MOSFETs should behave as ideal switches, being conductive (switched ON) if v_{GS} exceeds the threshold value V_{GSth}, while maintaining

$$v_{GS} > V_{GSth} + V_{DSon} \tag{18.29}$$

The ON MOSFET behaves almost like a resistor R_{DSon}, with low value and positive temperature coefficient being the drop ON voltage

$$V_{DSon} \approx R_{DSon} I_D \tag{18.30}$$

The MOSFET stops conduction (opens) turning to the *off*-state if

$$v_{GS} < V_{GSth} (off - \text{state}, I_D \approx 0)$$

Usually, the gate driver enforces $v_{GS} < 0$ with $v_{DS} > 0$, to have noise immunity.

If $v_{DS} < 0$, then the intrinsic diode starts to conduct (on voltage $V_{DS} = -V_{PINon}$), which is seldom advantageous since the internal PIN diode usually is not optimized for low-voltage drop or high-speed switching.

In this case, it is better that the gate driver turns on the MOSFET channel in order to prevent the PIN diode conduction, if $-R_{DSon}\ I_D < V_{PINon}$.

The gate current after charging or discharging of gate stray capacitances is almost zero; therefore, the needed gate power is very low. In PP applications, fast switching is required; consequently, the circuit driving the v_{GS} voltage must be designed to charge/discharge the MOSFET parasitic nonlinear capacitances taking into account the effects of device terminal inductances (Fig. 18.6C). The switching speed of existing MOSFETs is limited mainly by packaging (lead inductances) and drain and gate and source resistances together with intrinsic capacitances.

The switching times can be in the order of some nanoseconds or lower and are affected by the driver R_G value.

Resistor R_G dampens the RLC series circuit that contains C_{GS}, C_{DG}, and gate and source stray inductances L_S. The gate resistor can be sized adopting a suitable value for the damping factor ζ of the RLC series circuit

$$\zeta = \frac{R_G}{2Z_G} \tag{18.31}$$

where

$$Z_G = \sqrt{L_S / C_G} \tag{18.32}$$

and C_G is the equivalent gate capacitor, being

$$R_G = 2\zeta \sqrt{L_S / C_G} \approx 1.4 \sqrt{L_S / C_G} \text{ for } \zeta = 0.7 \tag{18.33}$$

The equivalent gate capacitor C_G can be known from the manufacturer datasheets:

$$C_{GS} = C_{iss} - C_{rss} \tag{18.34}$$

$$C_{DG} = C_{rss} \tag{18.35}$$

$$C_{DS} = C_{oss} - C_{rss} \tag{18.36}$$

giving

$$C_G \approx C_{GS} + C_{DG} \frac{dv_{GD}}{dv_{GS}} \tag{18.37}$$

while the gate and source stray inductances L_S can be estimated considering typical per unit values.

For printed circuit boards (striplines) or typical parallel wires, inductance L_S is usually given nearly by 10 nH/cm times the current path total length in centimeters (typical TO220-packaged MOSFETs exhibit source terminal inductances of $l_S \approx 5$ nH).

For twisted wire pairs, coaxial cables, or other low inductance connections, that value can be estimated as low as 3 nH/cm. The inductor estimation (and C_G nonlinear capacitor

calculation) does not need to be very precise since they only affect R_G by their square root values.

Example 18.2 Calculate the gate resistor for a MOSFET with $C_{GS} \approx 800$ pF and $C_{DG} \approx 40$ pF, operating at a drain voltage of 800 V, driven by $v_{GS} = 15$ V through a printed circuit stripline of 5 cm total length.

Solution For the given stripline length, it is obtained

$$L_S \approx 10\,\text{nH/cm} \times 5\,\text{cm} \approx 50\,\text{nH}$$

The gate equivalent capacitance is

$$C_G \approx C_{GS} + C_{DG}(dv_{GD}/dv_{GS}) \approx 10^{-12} \times (800 + 40 \times (800/15)) \approx 2.9\,\text{nF}$$

Therefore, the gate resistor is

$$R_G \approx 1.4\sqrt{L_S/C_G} \approx 5.8\,\Omega$$

As C_{GS} and C_{DG} are nonlinear-voltage-dependent capacitances, using $R_G \ll Z_G$ can establish gate-source overvoltages two to three times the applied v_{GS} voltage, which can disrupt the gate insulation oxide if they exceed the breakdown voltage V_{GSS}, destroying the MOSFET.

To minimize the R_G value, for faster gate capacitor charging and switching, it is essential to strongly reduce the stray inductances (if $L_S \to 0$, then $R_G \to 0$).

Fast driving using avalanche transistors

Fast MOSFET drivers require low stray inductances and often must be based on avalanche transistors [12] (switching bipolar transistors optimized to operate near their collector emitter breakdown voltage V_B but at limited current) or resonant circuits [13]. The avalanche transistors rapidly charge the capacitors C_{GS} and C_{DG}, by transferring capacitor charge from a capacitor reservoir C_a to C_{GS} and C_{DG} (Fig. 18.7A).

Supposing charge continuity, the MOSFET gate voltage should be

$$V_{GS} \approx \frac{V_B C_a}{(C_a + C_G)} \tag{18.38}$$

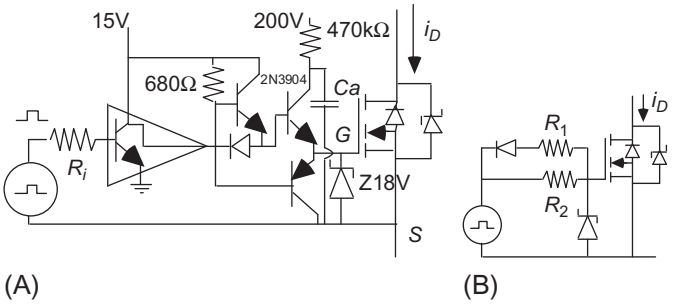


FIG. 18.7 (A) Avalanche transistor MOSFET driver and (B) tailoring switching speed using two resistors.

The Zener diode Z18V helps protect the gate oxide against disruption, but the Zener junction capacitance, if significant, should be added to the C_G value above.

MOSFET switching behavior includes crossing the saturation zone (MOSFET active zone) where

$$i_D \approx K_M(v_{GS} - V_{GSth})^2$$

being K_M a MOSFET structural parameter dependent on width and length of the device channel and electron mobility [16]. The crossing path may imply higher switching losses when switching PP capacitive loads.

Switch-on t_{on} and switch-off t_{off} times can be tailored using different resistive gate current paths to turn-on (R_2) and to turn-off ($R_1||R_2$) (Fig. 18.7B), limiting the charging current and the drain voltage rise or fall rates, at the expense of increased switching losses.

Considering the on and off switching times (t_{on} and t_{off}), the dissipated switching power at the switching frequency f_S in inductive loads is

$$P_S = \left[\left(t_{on} + t_{off}\right) V_{DS} I_D + C_{DS} V_{DS}^2\right] \frac{fs}{2} \tag{18.39}$$

while in resistive loads, it can be quite smaller:

$$P_S = \left[\left(t_{on} + t_{off}\right) V_{DS} I_D + 3 C_{DS} V_{DS}^2\right] \frac{fs}{6} \tag{18.40}$$

PP applications often need semiconductor *switch protection to limit load short-circuit current*. Since in MOSFETs $V_{DSon} \approx R_{DSon} I_D$ and R_{DSon} is fairly constant, then short-circuit protection circuits can be based on the measured V_{DSon} voltage (Fig. 18.8A) [10]. Sensed by diode D_{b3}, this voltage if low enough maintains the C_z voltage low preventing D_z to avalanche and maintaining Q_{t2} off. However, if V_{DSon} rises then D_{b3} turns off, C_z voltage rises and D_z avalanches turning Q_{t2} into saturation that shorts the v_{GS} voltage and turns off the MOSFET. Capacitor C_z acts as a memory, creating a delay that enables the MOSFET turn-on. Fig. 18.8B and C shows alternatives in which the rate of the v_{GS} decay is slowed to lower the rate of rise of the v_{DS} preventing this voltage to exceed the MOSFET hold-off (avalanche) voltage V_{DSS}. Fig. 18.8B shows a capacitive method in which $C_g \gg C_G$, while in Fig. 18.8C, the low-power P MOSFET M_p, in series with the main MOSFET gate, is turned off, putting the high-valued resistor R_{g2} in the turn-off path to limit the v_{GS} decay and v_{DS} rate of rise.

The maximum turn-off overvoltage can also be limited either by using MOSFET parallel connected Zeners (or voltage clamping metal oxide varistors (MOV)) or alternatively by using an avalanche diode (with avalanche voltage higher than the supply voltage but somewhat lower than maximum semiconductor voltage rating) in series with a blocking diode connected to the gate-drain terminals (Fig. 18.9).

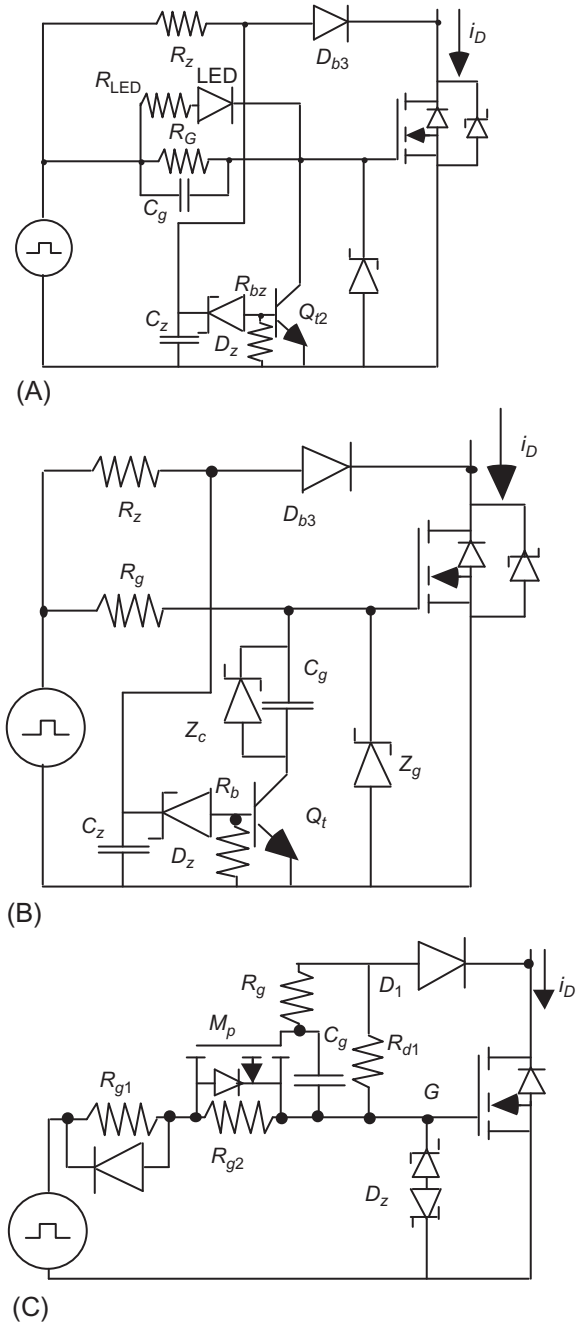


FIG. 18.8 (A) Active protection against load short-circuits, (B) active protection including capacitive v_{DS} rate limiter, and (C) active protection including resistive v_{DS} rate limiter.

18.2.2.2 Insulated-Gate Bipolar Transistors (IGBT)

IGBTs are MOS technology-based semiconductor devices with reduced *on*-state voltage drop, obtained by adding an extra P^+ semiconductor layer in the drain side (punch-through IGBT) or by substituting the N^+ by a P^+ layer (nonpunch-through (NPT) or reverse-blocking IGBT (RB-IGBT)) [10,11,13]. The P^+ layer injects holes in the drift layer reducing voltage drop

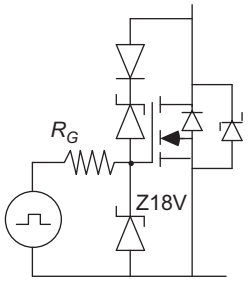


FIG. 18.9 MOSFET overvoltage protection circuit.

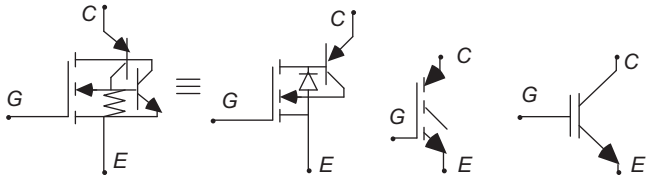


FIG. 18.10 IGBT equivalent circuit and common symbols.

by conductivity modulation. The resulting device can be viewed as a low gain high-voltage PNP bipolar transistor driven by a power MOSFET (Fig. 18.10). Then, gate drivers for IGBTs are similar to those of MOSFETs.

IGBTs can turn-on almost as fast as MOSFETs, using

$$v_{GE} > V_{GEth} \Rightarrow \text{IGBT } on - \text{state} \tag{18.41}$$

The *on*-state saturation voltage V_{CEon}

$$V_{CEon} = V_{CEsat} + r_{CEon} I_{CE} \approx V_{CEsat@I_{CE}} \tag{18.42}$$

where $V_{CEsat@I_{CE}}$ is the *on*-state voltage at current I_{CE} and depends on the I_{GE} value and increases rapidly for $V_{GE} < 12$ V, the device risks working into the active zone for lower V_{GE} values.

Due to the injected minority recombination into the base, however, IGBTs are relatively slow turn-off devices and exhibit tail currents. Switching losses are higher than in MOSFETs.

However, Si IGBTs can withstand much higher hold-off voltages (up to 6.5 kV) and currents (up to 3 kA) than Si MOSFETs that are limited to nearly 1.2 kV, 100 A peak current. At 6 kV voltages and 3 kA currents, IGBTs *on*-state losses are significant, degrading efficiency and causing heat removal problems, yet they are being used in very high-voltage systems [17–20].

Most considerations about the MOSFET drive and protections are still valid for IGBTs. In particular, in shoot-through situations, the IGBT device can be protected by detecting desaturation voltage and then shutting down the IGBT using gate drive circuits similar to those in Fig. 18.8.

18.2.2.3 Injection Enhanced Gate Transistors (IEGT)

IEGTs are IGBT-like structures with deep trench gates and wider cell widths. Hole concentration in the P layer under the gate electrode is enhanced due to hole accumulation,

similar to the conductivity modulation of a PIN diode, lowering the *on*-state voltage and increasing the efficiency specially in high-voltage devices. The enhanced carrier distribution under the gate electrode leads to higher conductivity of the N-base region in the trench-gate IGBT structure, as the gate region extends into the N-base region below the P-base layer. This phenomenon has been called the injection enhancement effect in deep trench-gate IGBT structures and enables higher device voltage rating. As this phenomenon of carrier enhancement under the gate electrode occurs in all IGBT structures, including the planar-gate structures, the IEGT device is a kind of IGBT and can be viewed as such, although their particular physical structure enables them to withstand higher voltages and currents than planar IGBTs structures. The same is valid for similar proposed structures such as the carrier-stored trench-gate bipolar transistor (CSTBT-IGBT).

18.2.3 Thyristors and Turn-Off Thyristor Devices

High-voltage high-power *thyristors*, also termed silicon-controlled rectifiers (SCR), are PNIPN structures (Fig. 18.11A) that can be gated-on by injecting a relatively small gate current into the device gate terminal. In PP applications, thyristors can be used in capacitor discharging circuits, since they can be easily turned on by a small gate current [10,11,13]. Thyristor turn-off behavior is not gate-controlled, being similar to the PIN diode and of little use in PP.

Thyristors can block voltages near 12 kV (the silicon limit is near 15 kV) and can conduct currents up to 8 kA.

Modern thyristor structures like the light-activated silicon-controlled rectifier (LASCR) or the light-triggered thyristor (LTT) are optically triggered (Fig. 18.11B) using an optical fiber and can be valuable in high-voltage applications to enable reducing stray capacitances.

Gate turn-off thyristors (GTO and sometimes called gate-controlled thyristors (GCT)) are distributed gate thyristor structures, roughly equivalent to an NPN-PNP bipolar transistor association [10,11,13]. As such, they have turn-on and turn-off gate capability, present low forward drop voltage, and maintain the PNIPN structure, which enable blocking voltages up to 6 kV and forward currents up to 6 kA.

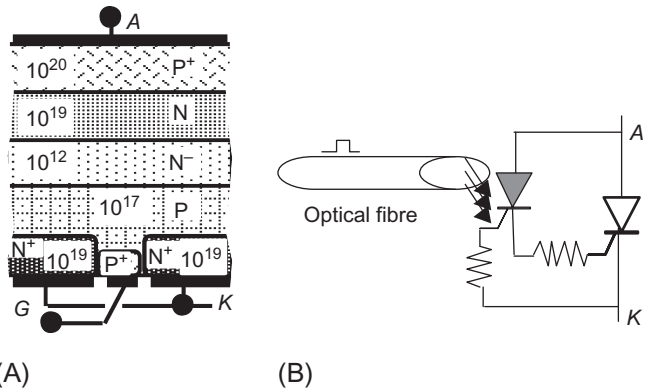


FIG. 18.11 (A) High-voltage thyristor structure and (B) LTT operating principle.

The GTO, although turn-off controlled, is much slower than MOSFET or IGBTs, since it is a bipolar carrier device, and it needs high turn-off gate currents, only slightly lower than their anode currents, meaning their turn-off current gain is low (between 2 and 10). Therefore, the GTO use in pulse power is usually limited to the generation of relatively long prepulses to be applied, through transformers, in sharpening devices such as the SOS diode. Symmetrical GTO structures are even slower than asymmetrical GTOs, although they can block both forward and reverse voltages (symmetrical gate-controlled thyristor (SGCT)).

The GTO turn-on peak and back-porch gate currents are also significantly higher than in thyristors, since the PNP transistor must have low enough current gain to preserve the turn-off capability. Therefore, GTO gate drivers usually need roughly 100 times more power than the gate power needed by a MOSFET or IGBT.

Second breakdown of GTO bipolar junctions (transistors) and the distributed gate structure mean that the GTO needs turn-off (dv_{AK}/dt) and usually turn-on snubbers (di_{AK}/dt) (Fig. 18.12). Considering an $R_V L_V C_V$ series circuit with $\xi = 1$,

$$C_V \approx \frac{I_{AK}}{(dv_{AK}/dt)} \tag{18.43}$$

$$L_V \approx \frac{V_{AK}}{(di_{AK}/dt)} \tag{18.44}$$

$$R_V \approx 2\sqrt{L_V/C_V} \tag{18.45}$$

which dissipates relatively high-power, thus requiring the use of low GTO switching frequencies. GTO thyristors also exhibit current tail at turn-off.

The above drawbacks bound the application of GTO like semiconductor devices to high-voltage and high-current applications, where the low *on*-state voltage is mandatory for high efficiency, but the switching speed, gate drive power, and reliability are not at concern.

The GTO device is difficult to protect against short-circuit currents due to its long storage time, long turn-off delay, and comparatively low turn-off current capability.

Some GTO-derived devices, such as the *integrated gate-commutated thyristor* (IGCT) and sometimes the GCT,

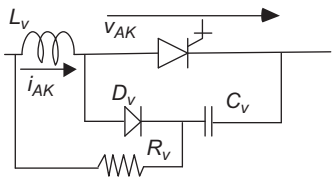


FIG. 18.12 Typical GTO combined di_{AK}/dt and dv_{AK}/dt snubbers.

incorporate distributed gate drives in close association with the GTO, being a single device, thus improving reliability [19]. This approach tries to circumvent the gate wiring inductances and enables accurate control of the turn-on speed. It is useful for series association of IGCTs, including overvoltage and short-circuit protections, together with redundancy. Still, the gate power is significant, and the IGCT needs a turn-on snubber.

Some GTO devices integrating MOSFET-based distributed gate turn-off drivers, with very low gate stray inductances, are sometimes called *MOS turn-off thyristors* (MTO) [13] (Fig. 18.13A). They have the potential to block up to 9 kV and can be faster than the GTO itself, although they need hybrid gate drives to turn-on.

If low-voltage high-current MOSFETs are connected in series with the GTO cathodes (cascode connection) and are used to turn-on and off the GTO, then the whole device is usually called the *emitter turn-off thyristor* (ETO) Fig. 18.13B [13], which has higher switching speed, higher reliability, and easier gate drive than the GTO itself. The ETO *on*-state voltage can be lower than in a comparable IGBT and even lower than in IGCT/GTOs. Thus, emitter switched GTOs can present efficiencies and switching speeds higher than comparable high-voltage IGBTs or IGCTs at 4.5 kV and 4 kA, although at higher costs than IGBTs but lower than IGCTs or even GTOs. Like IGCTs, ETOs include a GTO and need a turn-on snubber but can be fully optical fiber controlled (stray and electromagnetic interference reduction). The ETO drivers can easily generate the needed gate power (self-gate-drive power) and include minimum on/off time generation needed by the GTO, voltage, current and temperature sensors, and easy overcurrent protection (MOS turn-off).

The *MOS-controlled thyristors* (MCT) [13] are silicon fully integrated devices that try to improve GTOs, using integrated both turn-on and turn-off MOS devices, Fig. 18.13D. They can have lower *on*-state losses than IGBTs, current densities higher than IGBTs, working temperatures up to 200°C and block forward voltages of few kV. Switching speed is higher than in the GTO or even in the higher voltage IGBTs. The MCT promises to withstand much higher values of dv_{AK}/dt and di_{AK}/dt than GTOs, needing almost no snubbers and benefiting of simple MOSFET like gate drivers. As MOSFETs, MCTs can easily be connected in series or parallel associations to increase their voltage or current ratings.

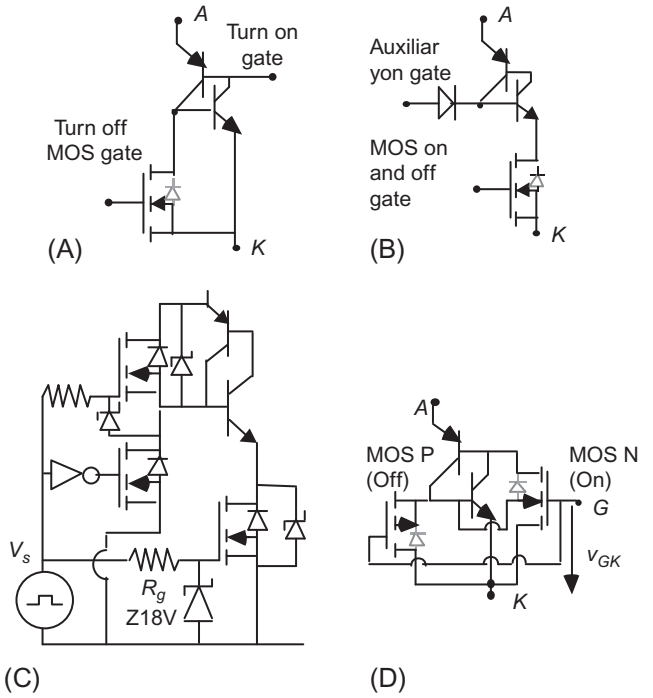


FIG. 18.13 Functional equivalent models of (A) MTO, (B) ETO, (C) conceptual ETO driver, and (D) MCT.

18.2.4 Power JFETs and Derived Devices

Power junction field-effect transistors (JFET) (Fig. 18.14), also termed static induction transistors (SIT), are short-channel depletion-type junction field-effect devices operating in the prepunch-through zone [13]. Their operation depends on the flow of majority carriers (electrons) only (unipolar device), and they have very low stray capacitances. Therefore, SITs have low switching losses and the potential to switch at very high frequencies, even higher than MOSFETs, up to the THz band.

The SIT is normally on a device (with $v_{GS}=0$, it is in the *on*-state) that turns off by applying negative gate-source voltages $v_{GS}<0$, up to several tens of volts. The v_{GS} negative voltage reverse biases the PN gate-source junction, pinching off the conducting epidrain and interrupting the flow of majority carriers.

Unlike SCRs, GTOs, MOSFETs, or IGBTs, the SIT normally on property enables its used in high-speed pulse generation circuits similar to those of SOS diodes, the main difference being the controlled turn-off with a negative gate voltage $v_{GS}\approx -v_{DS}/\upsilon$, where υ is the SIT blocking gain:

$$\upsilon \approx \frac{\Delta v_{DS}}{\Delta v_{GS}}$$

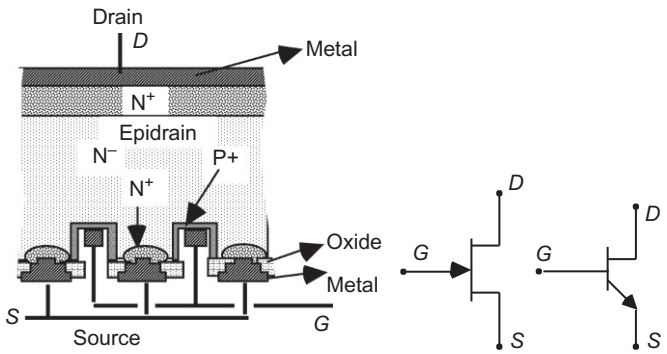


FIG. 18.14 Power JFET structure and possible symbols.

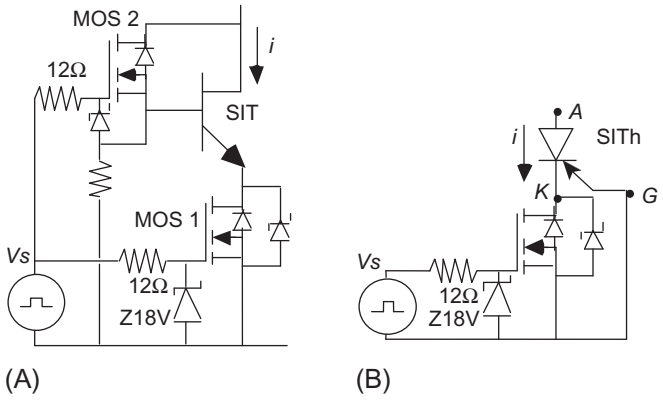


FIG. 18.15 (A) JFET cascode using two MOSFETs. MOS2 can be used to operate the SIT in the bipolar mode and (B) SITh cascode.

The normally on property of the SIT can increase its gate drive circuit complexity. A power JFET usually requires larger power and gate voltages compared with a similar MOSFET. These two SIT drawbacks can be advantageously solved using a cascode connection (Fig. 18.15A) in which a JFET is source-switched by a low-voltage high-current MOSFET.

The SIT device presents positive temperature coefficient, enabling easy paralleling like the MOSFET, and is a unipolar voltage-controlled device enabling relatively easy series connection. The SIT does not need turn-on or turn-off snubbers; simple RC clamping circuits (Fig. 18.16) are enough for stray inductance overvoltage protection.

The SIT can be operated in the bipolar mode (called bipolar mode SIT, BSIT, or BMSIT), if they are designed to allow positive gate currents to inject holes in the drain channel. The *on*-state of the BSIT is almost like that of a bipolar carrier device, increasing the turn-off time, but current density is much higher and useful phenomena for PP might occur [10,11,13].

A SIT-derived structure, which is being used in PP, is the static induction thyristor (SITh) also called field-controlled thyristor (FCTh) or field-controlled diode (FCD). It includes (Fig. 18.17) a P^+ layer (instead of the SIT drain N^+ layer) to obtain a PN junction (hence the name pinched diode). Present SITh devices block 4 kV and can switch peak currents in the kA range, presenting long lifetimes.

The SITh behaves like a diode if $v_{GK}=0$ (gate-cathode short). This diode can be turned off with almost no reverse recovery, making v_{GK} negative. However, the depletion capacitance gate current to turn-off can be as high as half of the anode current, making the SITh gate driver difficult to design and operate. An alternative to ease the gate driver is to use a cascode connection (Fig. 18.15B).

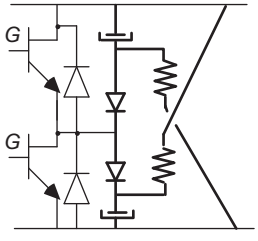


FIG. 18.16 SIT voltage clamper.

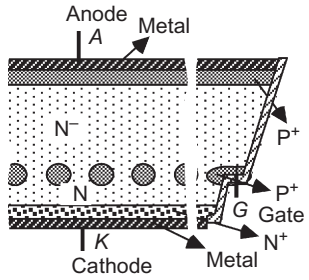


FIG. 18.17 Typical SITh (GTO-SIT) structure.

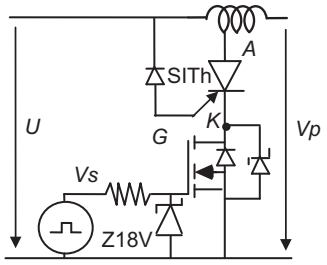


FIG. 18.18 SITh cascode pulse generation using magnetic energy storage.

The SITh is being used for pulse generation as an opening switch in inductive circuits (Fig. 18.18), much like the SOS diode (the SITh behaves as a controlled diode), and holds the pulse voltage *Vp* during the output phase. The gate current needed to extract carriers out of the device, to cause depletion and the off-state, is obtained by switching off the inductive current (with the cascode SITh) in a step-up autotransformer. The switching off induces the fast-rising negative v_{GK} voltages necessary to extract SITh carriers and to apply the load pulse. Speed switching in this case can be enhanced by positive feedback, the fast gate current decay creating a depleted SITh that helps in turning off the current.

18.2.5 Semiconductor Series Stacks and Generalized Cascodes, Semiconductor Parallel Stacks

18.2.5.1 Semiconductor Series Stacks

For applications where the needed working voltage is higher than the available semiconductor ratings, one possible solution is to series connect several power devices. Steady-state and transient balance or sharing of the voltage between series semiconductor devices is very important, since most power semiconductor devices do not hold voltages above their rating and their reverse currents, and reverse recovered charges differ

from device to device even within the same type and maker; the semiconductor with the least reverse leakage current will hold higher voltages.

Example 18.3 Consider a string of two series diodes, and suppose the total voltage $U=10$ kV, the two diodes both with nominal repetitive reverse voltage $V_{RRM}=6$ kV but reverse leakage currents of $I_{Rmax}=40$ mA and $I_{Rmin}=10$ mA. Calculate the diode reverse voltages.

Solution We can determine (Fig. 18.19)

$$R_{eqoffmin}=V_{RRM}/I_{Rmax}=150\,\text{k}\Omega$$

and

$$R_{eqoffmax}=V_{RRM}/I_{Rmin}=600\,\text{k}\Omega$$

Therefore, the diode with $R_{eqoffmin}$ would have the voltage

$$V_{Reqoffmin}=10\times10^3\times150/(150+600)=2\,\text{kV}$$

while the $R_{eqoffmax}$ diode

$$V_{Reqoffmax}=10\times10^3\times600/(150+600)=8\,\text{kV}$$

that exceeds the diode maximum rating. This diode would operate near its avalanche voltage ($\approx$6 kV) that could be destructive.

From the above, $V_{Reqoffmax}$ could be evaluated as

$$V_{Reqoffmax}=\frac{U\,I_{Rmin}}{[I_{Rmax}+(n-1)I_{Rmin}]}. \tag{18.46}$$

Steady-state balancing can be achieved using high-value parallel resistors R_h, so that the parallel of R_h with $R_{eqoffmin}$ or $R_{eqoffmax}$ should give a resistance able to maintain the semiconductor reverse voltage within acceptable limits.

Considering n-series-connected power semiconductors and one of them with

$$I_{Rmin}=0\left(R_{eqoffmax}\approx\infty\right)$$

while the remaining $n-1$ has the typical value R_{eqoff}, the total value R_T of the string of resistors is (Fig. 18.20)

$$R_T=R_h+(n-1)\left(R_h\|R_{eqoff}\right) \tag{18.47}$$

The maximum voltage occurs in the diode with $R_{eqoffmax}\approx\infty$ being

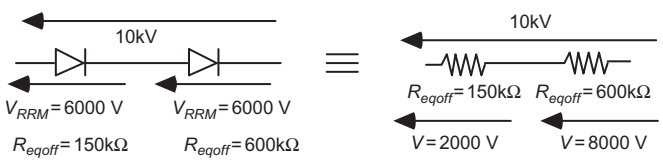


FIG. 18.19 Series connection of power semiconductors.

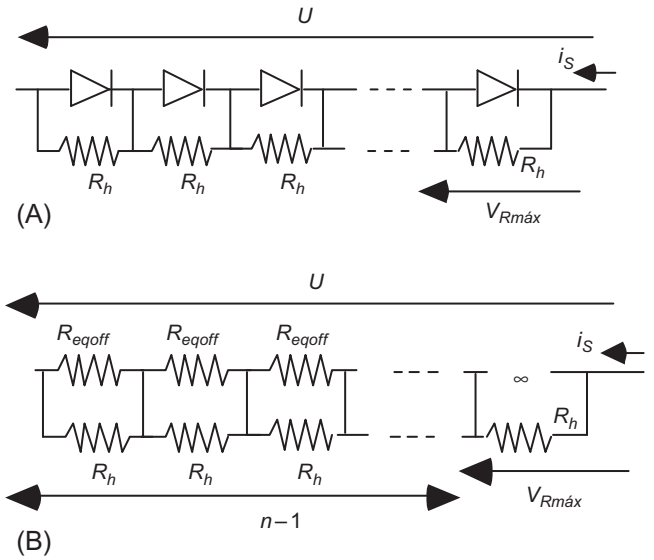


FIG. 18.20 (A) Steady-state balancing of a series connection of power semiconductors and (B) equivalent model.

$$V_{Rmax}=\frac{U\,R_h}{R_T} \tag{18.48}$$

This value should observe a safety margin:

$$U/n<V_{Rmax}<\kappa V_{RRM} \tag{18.49}$$

where $\kappa<1$, giving

$$n>\frac{U}{V_{Rmax}}\Rightarrow n>\frac{U}{\kappa V_{RRM}} \tag{18.50}$$

and

$$R_h=R_{eqoff}\frac{n\kappa V_{RRM}-U}{U-\kappa V_{RRM}} \tag{18.51}$$

Note that

$$U>\kappa V_{RRM}\ \text{and}\ n\kappa V_{RRM}>U \tag{18.52}$$

The R_h resistors should be as high as possible to minimize their dissipated power. The maximum R_h value can be obtained considering the I_{Rmin} and I_{Rmax} semiconductor currents (instead of $I_{Rmin}=0$) to obtain

$$R_h<\frac{(n\kappa V_{RRM}-U)}{(n-1)(I_{Rmax}-I_{Rmin})} \tag{18.53}$$

An alternative to the use of the dissipative resistors is to anti-parallel avalanche or Zener diodes or metal MOV with each series device.

To help share the voltage during transients, R_SC_S parallel snubbers must be also included (Fig. 18.21). If they are designed

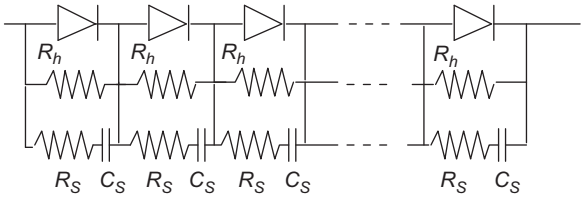


FIG. 18.21 Dynamic and steady-state balancing of series-connected power semiconductors.

just to balance the reverse recovered charge Q_{RR}, then the capacitor value can be given by

$$C_{Smin} \approx \frac{\Delta Q_{RR}}{\Delta U} \tag{18.54}$$

being ΔU the allowed voltage mismatch and ΔQ_{RR} the Q_{RR} variation among devices.

Resistor R_S limits the discharge current when the power semiconductor turns on.

To operate the $R_S C_S$ as a parallel snubber, then the circuit associated stray inductance L_S should be estimated or measured. Then, assuming energy conservation, a rough estimation of the C_S value is

$$C_S \approx \frac{L_S {I_{RR}}^2}{n(\kappa V_{RRM})^2} \tag{18.55}$$

Resistor R_S should define the damping factor ξ of the equivalent RLC series circuit, being

$$R_S = 2\xi\sqrt{L_S/(nC_S)} \tag{18.56}$$

For controlled turn-on and turn-off devices, the $R_S C_S$ parallel snubber can be improved using an extra diode ($R_V C_V D_V$ in Fig. 18.12, with $L_V = L_S$). To obtain near-balanced turn-on t_r and turn-off t_f times for each series semiconductor, with direct current I_{AK}, hold-off voltage κV_{DRM}, and pulse on minimum peak time T_{pmin}, L_S should have the value

$$L_S \approx \frac{\kappa V_{RRM} t_r}{I_{AK}} \tag{18.57}$$

and

$$C_V \approx \frac{I_{AK} t_f}{\kappa V_{DRM}} \tag{18.58}$$

being

$$R_V \approx 2T_{pmin} \cdot \frac{\xi\sqrt{1-\xi^2}}{\pi C_V} \tag{18.59}$$

18.2.5.2 Generalized Cascodes

To use a series stack of controlled turn-off semiconductors such as MOSFETs, SITs, or even IGBTs, the generalized cascode association (Fig. 18.22) is a valuable alternative to the simple series connection [10,14,15]. The simple series association of turn-off devices usually needs optical fiber isolated gate drivers using transformer isolated current source power inverters with series connection through closed-loop high-voltage cables, to assure the insulation between the voltage levels.

The cascode association is faster than other associations when unipolar-carrier semiconductors such as MOSFETs or SITs are used. For MOSFET devices (Fig. 18.22B), the capacitor C must hold the charge to turn the MOSFET on, being

$$C_a \approx \frac{V_{GS} C_G}{(V_{Dsoff} - V_{GS})} \tag{18.60}$$

Zener diodes should be used to protect the gate-source oxide. In Fig. 18.22B, the charge holding gate capacitors are placed in a configuration where the m capacitor C_m should have the value

$$C_m \approx C_a(n - m + 1) \tag{18.61}$$

being n the total number of MOSFETs and $m > 1$ [15].

For stacking IGBTs, care must be taken when designing the drivers of the totem pole IGBTs [21,22]. The positive voltage of each driver can be obtained from the capacitor of the below $R_S C_S$ snubber through a blocking diode connecting the resistor R_S to a turn-off MOSFET driving the IGBT [21,22]. The C_S capacitor should hold the charge to turn-on the IGBT.

When dealing with Cascodes, it is mandatory to minimize the source (or emitter) inductances as they can badly affect the charging rate of the gate capacitances. Bare chips (bare dice) and surface mount design should be used, instead of packaged MOSFETs, IGBTs, or SITs.

18.2.5.3 Parallel Stacks

Parallel associations of power devices can be used when the available semiconductors do not present the needed current ratings.

For positive temperature coefficient devices such as MOSFETs, SITs, and most of their derived structures, the devices can be just connected in parallel, taking care of symmetry to minimize stray inductances and capacitances and to balance junction temperatures. Individual gate drivers and protection circuits (except if stray effects are not a concern) should also be used. This is not valid for the MOSFET intrinsic diode, which must be disabled using channel conduction or extra external diodes.

For negative temperature coefficient devices such as diodes, thyristors, bipolar transistors, GTO, and other bipolar devices, several methods could be used:

(a) To select devices with very small relative parameter variations (matched devices) and to balance their junction temperatures by using a single heat sink and symmetrical disposition.
(b) To use current sharing transformers or coupled inductors (Fig. 18.23).

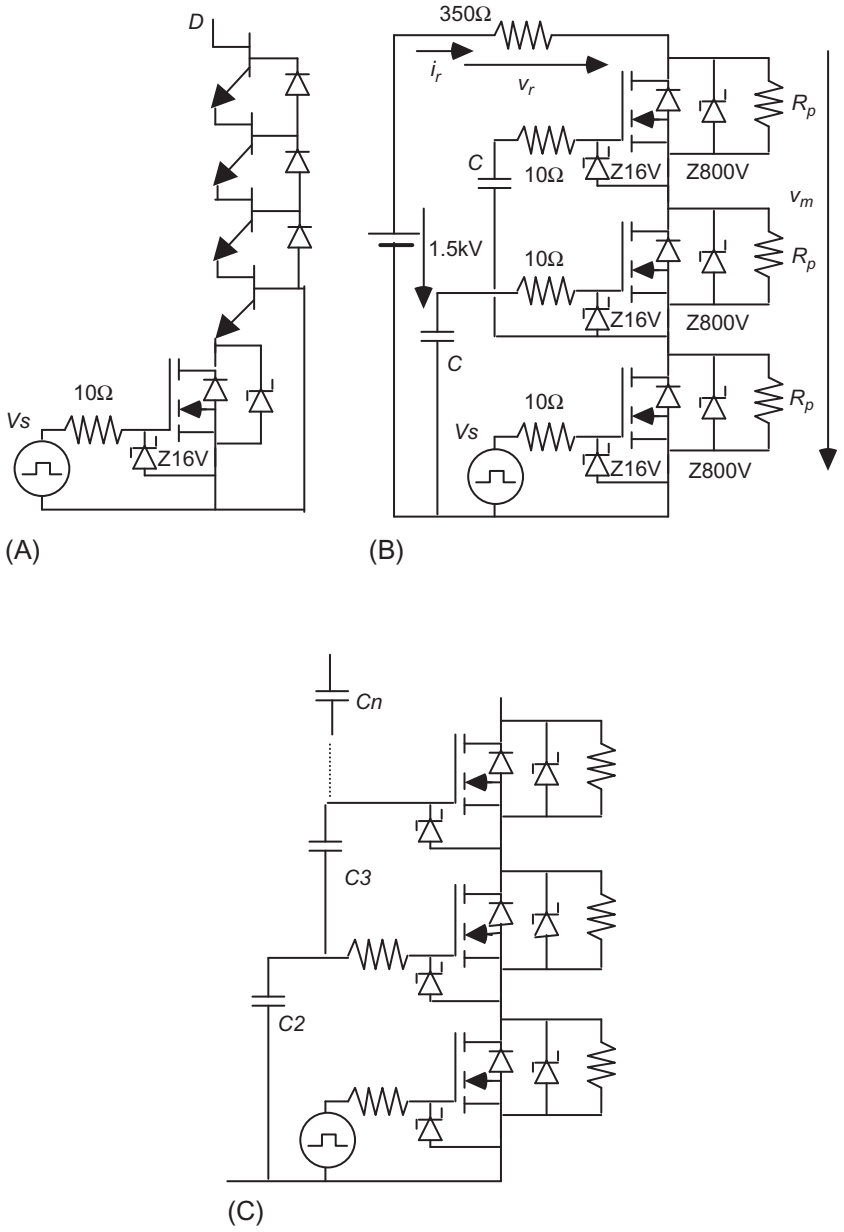


FIG. 18.22 Generalized cascade associations: (A) using SIT devices, (B) using only MOSFETs, and (C) using alternative connection of gate capacitor.

(c) To use current feedback control techniques [23] if the paralleled devices have turn-off capability.

(d) To use small resistors in series with each power semiconductor device (Fig. 18.24), calculated upon the maximum, minimum, and typical device parameters. It is possible to show that a rough estimate for the series resistor R_E is

$$R_E \approx \frac{(V_{1max} - V_{2min})}{(I_2 - I_1)} \tag{18.62}$$

where V_{1max} is the device family maximum on voltage at the minimum allowed current I_1 and V_{2min} is the device type minimum on voltage at the maximum allowed current I_2 ($I_2 > I_1$) [10].

One of the previous approaches has to be selected upon the PP application to minimize costs and maximize performance.

18.2.6 Wide Band Gap Power Semiconductor Devices

Silicon carbide (SiC) and gallium nitride (GaN) are new semiconductor materials with wider bandgaps than silicon (nearly three times higher) resulting in a higher critical electric field

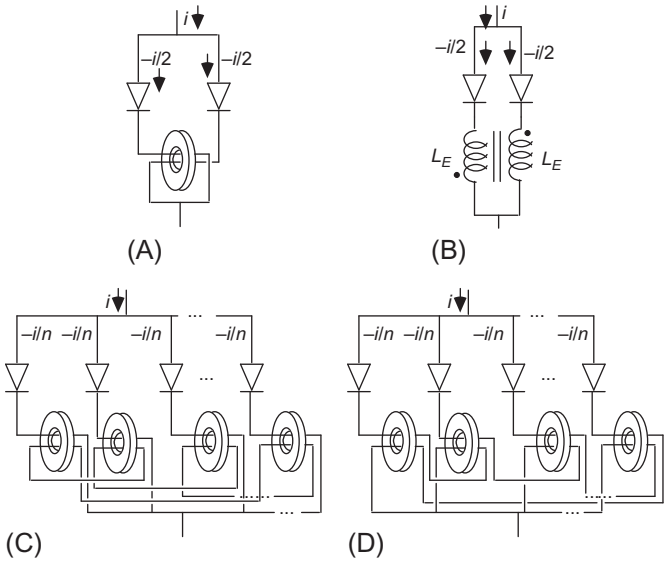


FIG. 18.23 Using transformers or coupled inductors for paralleling power devices: (A) two diodes, (B) modeling the parallel connection of two diodes, and (C and D) alternatives to n-paralleled power semiconductors.

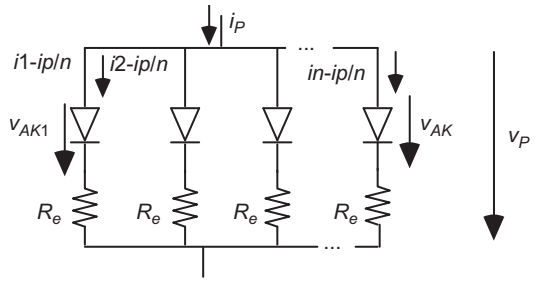


FIG. 18.24 Parallel connection of power semiconductors using current sharing resistors.

and lower *on*-state resistance. In particular, the structure 4H-SiC presents high thermal conductivity (three times higher than Si), high electric field breakdown strength (10 times higher than Si), high maximum current density, very low thermal expansion coefficient, and higher electron saturation velocity. These properties allow higher switching frequency (ns switching time) and 10 times lower switching losses in power applications. Therefore, SiC is a much more promising semiconductor material than Si to build high-powered devices.

SiC allows a very low drift region resistance, enabling *on*-state current densities near 100 A/cm^2 at 25°C with forward voltage drops at 3–4 V in SiC Schottky diodes and power MOSFETs rated at several kV. SiC devices would need approximately 20 times less area than corresponding Si devices, and could operate at higher temperatures and higher breakdown voltages than conventional Si devices.

Schottky barrier diodes use a suitable metal-semiconductor junction. Being unipolar-carrier devices show almost no minority recombination. SiC Schottky diodes have extremely low reverse recovery time, negligible switching losses, and 20 times lower reverse recovery charge than Si while needing a ringing correcting RC snubber, as the reverse-biased diode has a capacitive behavior, causing ringing with stray inductances. Since minority carrier injection is not present in SiC Schottky diodes and SiC transistors, they are expected to have fast switching characteristics, low switching losses, and high reliability.

To profit from the advantageous performance of high-voltage SiC devices, a gate driver design tailored for each particular device is required to provide fast switching for the SiC devices while preventing ringing. Some form of current sensing and limitation is absolutely needed and dv/dt limitation using dedicated gate drivers, RC parallel tuning, and protection Zeners. Gate voltages of nearly 20 V are usually needed for *on*-state, together with a suitable gate ON resistor to limit switching dv/dt and di/dt and the turn-on current spike due to charge/discharge of the freewheeling Schottky barrier diode equivalent capacitance. A too small gate ON resistor can increase switching times and switching energy losses relatively to the optimum values, which are roughly 10 times lower than in the Si technology.

To turn off the SiC device, a negative voltage near −5 V should be applied through a gate OFF resistor, usually much smaller than the gate ON resistance.

High-voltage SiC devices feature *on*-state equivalent resistances with a positive thermal coefficient θ_r ($\theta_r \approx 0.001\ \Omega/°C$). Their *on*-state resistance R_{ON} increases with junction temperature T_j, $T_j \in$ (25 and 175°C):

$$R_{ON} = R_{ON0} + \theta_r T_j \tag{18.63}$$

The SiC threshold voltage V_T (18.64) shows a negative thermal coefficient θ_v ($\theta_v \approx -0.0015$ V/°C) similar to the Si coefficient (−2 mV/°C). However the SiC *on*-state voltage increases with T_j (18.65) for I_{ON} currents bigger than a few amps, as long as $\theta_r I_{ON} + \theta_v > 0$:

$$V_T = V_{T0} + \theta_v T_j \tag{18.64}$$

$$V_{ON} = V_T + R_{ON} I_{ON} = V_{T0} + R_{ON0} I_{ON} + T_j(\theta_r I_{ON} + \theta_v) \tag{18.65}$$

This behavior is advantageous when needing to parallel SiC devices, since they will share the total current. However, for single devices, thermal runaway can occur when high-current is applied. A gate driver able to cope with this phenomenon may be advisable, and the heat sink should be designed to minimize temperature T_j for the required average and root mean square values of I_{ON}. The thermal runaway can further be mitigated by using SiC devices with extra P^+ implantations in the device structure.

GaN enhancement-mode JFETs (E-HEMTs) are very fast unipolar-carrier devices controlled by the electric field associated to the v_{GS} voltage applied at the gate-source terminals.

These normally *off*-state GaN E-HEMTs are conductive with $v_{GS} \approx 6$ V, while they are blocking with $v_{GS} = 0$ V if $v_{DS} > 0$. However, if $v_{DS} < 0$ with $v_{GS} = 0$ V, then device conducts in the reverse direction with zero reverse recovery charge. Negative gate bias $v_{GS} < 0$ V could be used for noise immunity in the *off*-state but increases reverse conduction losses, since the gate-drain voltage must exceed the gate threshold voltage. The gate turn-on resistor has values between 12 and 30 Ω for optimal performance, while the gate turn-off resistor should be 10 times smaller to almost cancel Miller voltage effects (Fig. 18.7B). It is claimed E-HEMTs have 1% switching losses of the corresponding Si transistor.

GaN E-HEMTs have a positive temperature coefficient *on*-state resistance that is useful to balance the current when paralleling several devices. However, given the fast switching speed, to minimize oscillations and to enable balanced dynamic current sharing, the driver circuit layout should be carefully designed to ensure circuit symmetry and to equalize the loop length of the gate drive striplines (using a star connection to all paralleled devices and adding an extra 10% gate resistor to each device).

Superjunction (SJ) transistors are being researched to build high-voltage bipolar power transistors with very short switching times and high base current gain. They present a low *on*-state voltage drop (less than 1 V) at current densities near 100 A/cm^2, due to very low minority injected carries, the device acting nearly as a majority carrier device.

18.3 Load Types and Requirements

PP applications present some of the most demanding loads to the modulators in terms of pulse requirements, as, normally, almost rectangular pulses are needed to many applications in capacitive and inductive loads.

Nowadays, when evaluating a PP modulator topology, it is important to consider, in addition to cost, size, simplicity of operation, and efficiency, the flexibility for different operating conditions into various load conditions (i.e., resistive, capacitive, and inductive).

In fact, the growing variety of environmental, biological, medical, and industrial applications using positive or negative high-voltage repetitive pulses, for enhancing the characteristics of a product or method, impose various load conditions to the modulator circuits [24].

For example, applications with plasmas or gases present normally capacitive behavior, like plasma implantation or air processing for pollution control [25,26]. Applications that use coils present an inductive behavior, like electromagnetic forming, or whenever a high-voltage transformer is associated to the modulator to further increase the output voltage [27,28]. In addition, food processing, water treatment present resistive behavior.

Pulse feeders distributed capacitance and inductance might be important to be considered in PP loads, often needing some sort of resistive compensation added to the PP load.

18.3.1 Resistive (*R*) Loads

Pure resistive-type loads are not common in PP applications, being the processing of liquids one of the exceptions, in applications such as liquid food sterilization, wastewater decontamination, and biomedical materials. However, resistive loads are used frequently as a load reference for testing and comparison the pulse voltage waveform between different types of modulators.

The problem is to find a resistor that can handle the generated power, the voltage level and, at the same time, without presenting inductive behavior. Although there are expensive commercially available types for HV and kW operation, alternatively, it is possible to fabricate, much cheaper, water resistors for any power and voltage needed.

A water resistor is essentially an insulator tube filed with an aqueous electrolytic solution and a metal electrode in each extremity, capable of dissipating the average power and holding the high-voltage from the modulator. Typically, it is made up of dilute solution of copper sulfate ($CuSO_4$) in deionized water (a good electric insulator), which does not degrade the copper electrodes. The higher the $CuSO_4$ concentration, the lower the resistance being the total resistance proportional to the length of the tube [29].

The energy dissipated in the water produces a change in its temperature Δt, which can be determined by knowing the specific heat of water, C_p,

$$\Delta t = \frac{Q}{mC_p} \tag{18.66}$$

where Q is the change in thermal energy and m is the mass of the water resistance tube.

Nevertheless, the use of water resistances brings some limitations. First, with the temperature increase, air bubbles are formed that change the resistance value. Second, the $CuSO_4$ molecule breakdown linked with electrolysis phenomenon has undesirable results: (i) With gas release that increases the pressure inside the tube, a gas release aperture is advisable in the tube edges to prevent the increase of the pressure inside the tube, and (ii) the metallic copper decomposition in the cathode (i.e., copper transport from the anode to the cathode) changes the test conditions. With time, the performance of a water resistance may change in consequence of these effects.

Example 18.4 Consider an HV pulse modulator that produces a 20 kV/10 A pulse during 10 μs with 100 Hz repetition rate. Calculate the temperature increment of $l = 1$ m tube (made from insulating material) with an internal diameter of $d = 2.5$ cm when used as a load to the modulator during 60 s.

Solution The energy per pulse is

$$E_p = V_p I_p t_{on} = 20 \times 10^3 \times 10 \times 10^{-5} = 2\,\text{J}$$

The energy in 60 s is

$$E_{60} = 60 f E_p = 60 \times 100 \times 2 = 12\,\text{kJ}$$

The volume of water inside of the tube is

$$V_W = \pi r^2 l = \pi \times 0.0125^2 = 0.491 \times 10^{-3}\,\text{m}^3 = 491\,\text{g}$$

Then, considering that 1 Cal = 4.2 J, results in

$$\Delta t = \frac{Q}{mC_p} = \frac{12{,}000}{491 \times 4.2} = 5.8\,^\circ\text{C}$$

Hence, for an initial water temperature at 25ºC, after 60 s, the temperature will increase to 30.8°C.

18.3.2 Capacitive (*C*) and *RC* Loads

Pulse power applications associated with plasma and gas processing, and occasionally liquids, present typically capacitive behavior to the PP modulators. In fact, some of the most challenging operating conditions are related with the operation with plasmas.

A typical example is plasma-based ion implantation (PBII), where a target is immersed in a plasma, produced in a confined volume, and almost rectangular negative HV pulses are applied to it. This results into a high-current peak at the beginning of the pulse, rapidly decreasing to a much smaller value. The initial transient current that charges the main system capacitances can be several orders of magnitude greater than the stationary current at the pulse end, when the load imposes almost open-circuit impedance, presenting an additional challenge to the modulator. The above load dynamic characteristics can be represented in an RC electric equivalent circuit as in Fig. 18.25 [30,31].

For plasma loads such as PBII, considering plasma characteristics and typical wanted results, the modulator requirements can be sought: (a) The voltage pulse waveform must be independent of the load impedance, (b) the pulse rise time must be in the order of the μs and small compared with the pulse width, (c) the pulse duty-cycle must be a few percent, (d) the pulse width and frequency should allow some load variation, (e) there must be a current limit in case of short-circuit, and (f) in order to be practical, the power supply cannot be too complex and bulky while including all the necessary protection systems for personnel and equipments.

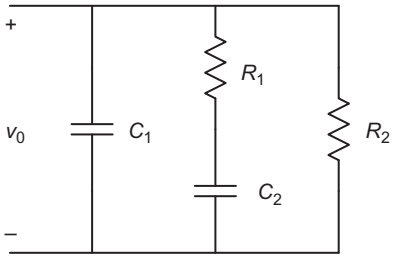


FIG. 18.25 Simplified electric equivalent circuit of a PBII load.

In capacitive-type loads, it is extremely important, also, that the modulator topology has the capability to short-circuit the load after the HV pulse, quickly discharging all the load and parasitic capacitances to zero; otherwise, the load stays charged to almost full pulse voltage. Occasionally, this type of load must be compensated by adding parallel resistors.

18.3.3 Inductive (*L*) and *LR* Loads

Inductive-type loads are present when a pulse transformer is used to further increase the voltage level of a modulator or when voltage pulses are applied to inductive loads such as coils. An example of the last is electromagnetic metal forming application, EMF, where HV resonant topologies apply kA current pulses, during hundreds of μs, into very low inductance systems [8].

For inductive operation, the modulator must clamp the load with an opposite polarity voltage after each HV pulse, during enough time to guarantee a zero average load voltage. In general, this is not accomplished with turn-off capability semiconductor switches but rather with freewheeling diodes. Also, the topology either can be dissipative or can send the energy stored in the magnetic circuit back to the power supply, increasing the efficiency of the modulator.

18.4 Solid-State PP Topologies

The use of innovative techniques, supported on dc-dc isolated converter topologies, brought from solid-state power electronics, taking advantage of all the capabilities of such devices, circumventing their limitations, is playing an important role to the expansion of pulse power technology to a wide range of new applications, needing compact, small size and efficient pulse modulators, spreading to almost every industrial and commercial fields, from food sterilization, biomedical applications and pollution control to surface engineering [31–37].

Nevertheless, each PP application represents a different challenge for the PP technology and the load requirements normally imposes limits to the use of each type of power converter topology. One important characteristic associated with many pulse power applications is the low duty ratio, *D*, pulse operation (i.e., usually lower than 5% [1,2]), where the pulse width is much shorter than the pulse period, which reduces significantly the modulator average power and also the dissipated power into the load, as

$$P_{av} = V_p I_p D \tag{18.67}$$

where V_p and I_p are, respectively, the pulse voltage and current amplitude, supposing a rectangular pulse with $D = t_{on}/T$ duty ratio.

In order to take the most of each topology and also to be able to extend these concepts to other topologies that have potential for high-voltage pulsed generation, it is important to understand the concepts and to know the advantages and limitations when using each topology.

In this section, several topologies capable of generating high-voltage pulses based on relatively low-voltage semiconductors devices are analyzed. The study begins with the most common configurations for pulse generation that switch the HV voltage directly into the load, using stacks of series semiconductors.

The dc-dc isolated converter topologies, forward, flyback, full-bridge, and half-bridge, which can be modified to produce high-voltage rectangular repetitive pulses, with techniques that enable the use of relatively low semiconductor devices, are presented next. Here, the use of a step-up transformer provides galvanic isolation and further increases the output voltage pulse amplitude, although the transformer presents limitations to its use. In order to overcome various technical hitches in assembling a unique high-voltage circuit, stacked associations of lower voltage topologies are also discussed with and without the use of output transformers. Finally, the mature Marx generator pulse power topology is discussed with the intensive use of semiconductors. This concept is also proposed for distributing the voltage in series stacks of semiconductors.

It is important to define some of the pulse parameters mentioned in the following sections, as shown in Fig. 18.26 for the practical shape of unipolar voltage pulses.

Considering Fig. 18.26, the voltage pulse can be characterized by several parameters:

- Rise time, t_r: period of time from 0.1 to 0.9V, where V is the plateau amplitude of the pulse
- Overshoot, ΔV_s: voltage excursion, after the rise time, above the pulse plateau V
- Width, Δt: pulse duration in the 0.5 V region
- Undershoot, ΔV_d: voltage excursion, after the fall time, below minimum voltage, 0 V
- Droop, ΔV: in relation to the plateau amplitude V, $\Delta V = V - V_f$
- Fall time, t_f: period of time from 0.9 to 0.1V_f, where V_f is the final pulse voltage, different from V because of ΔV
- Tail: voltage descend during pulse fall

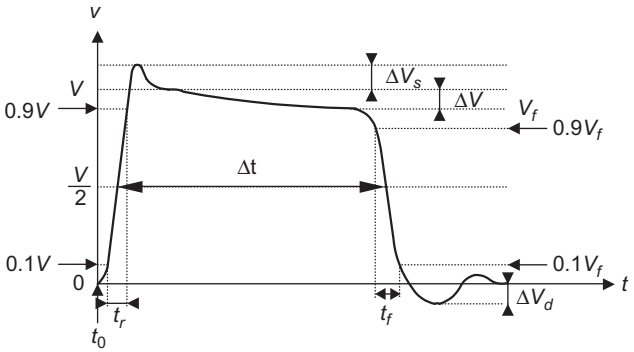


FIG. 18.26 Voltage pulse wave practical shape.

18.4.1 Direct Switching

The most straightforward technique for high-voltage pulse generation consists in switching directly the voltage from a dc capacitor bank charged with high-voltage into the load, using a floating or a grounded switch, as shown in Figs. 18.27 and 18.29, respectively.

18.4.1.1 Floating Switch

Consider the circuit in Fig. 18.27 where the HV power supply, PS, V_{dc} charges an energy storage capacitor bank C_{dc}. The PS internal resistance added by the switch and wiring ohmic resistances is represented by R_{dc} that limits the maximum charging current. Sometimes, a series inductor L_{aux} is also added, which acts as a current limiter and causes some boost of the capacitor voltage during the charging period.

The voltage is modulated into the load by the series floating switch Sp, which operates with duty ratio D. The switch-*on* and *off* control applies the full bank voltage to the load with the pulse width and frequency being controlled by the gate trigger. Supposing C_{dc} charged with V_{dc}, when S_m is *on*, during t_{on}, the C_{dc} capacitor applies a voltage V_{dc} into the load. During this period the inductance L_{aux} limits the discharge of the Power Supply to the load.

If the load has capacitive behavior, an auxiliary circuit must be added to discharge the load capacitance to zero after the voltage pulse. For low duty ratio operation or low-power operation, a permanent parallel resistor R_{a1} can be connected to the load, which must hold off the applied voltage. The R_{a1} value depends on its average power dissipation

$$P_{R_{a1}} = \frac{V_{dc}^2}{R_{a1}} D \tag{18.68}$$

and the required load voltage fall time.

As an alternative, for high duty ratio operation or high-power operation, it is preferable to use an auxiliary series switch S_a with R_{a2} to short the load after the pulse. In this case, the value of R_{a2} can be significantly reduced.

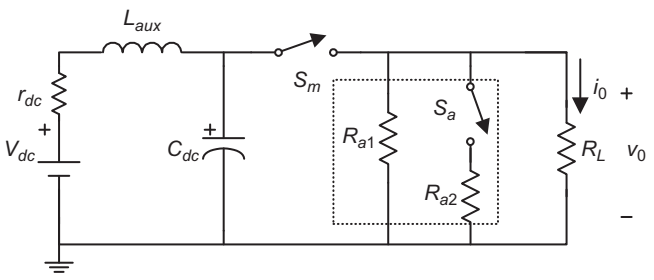


FIG. 18.27 Direct modulator simplified circuit with floating switch.

The main advantages of Fig. 18.27 topology are associated with the generation of voltage pulses with low rise time, low-voltage droop, and also the flexibility to change the frequency and duty ratio operation. However, the pulse characteristics are limited by the energy stored in the capacitor bank and on the performance and power dissipated in the switches and also on the rate of charge of C_{dc}.

The energy initially stored in the C_{dc} capacitor is

$$E_{C_{dci}} = \frac{C_{dc} V_{dc}^2}{2} \tag{18.69}$$

if the S *off* time, $T - t_{on}$, is enough for the PS V_{dc} to charge C_{dc}. Following and during t_{on}, the energy delivered to the load is

$$E_0 = \frac{V_{dc}^2}{R_L} t_{on} \tag{18.70}$$

For PP applications, only a small fraction of the stored energy should be transferred to the output during the pulse mode; otherwise, the pulse voltage has a typical RC discharge waveform, shown Fig. 18.28, and not an almost rectangular shape, as shown in Fig. 18.26.

For a resistive load, the pulse voltage decay V_{dcf} can be calculated as

$$V_{dcf} = V_{dci} e^{-\frac{t}{R_L C_{dc}}} \tag{18.71}$$

Considering a resistive load R_L, the capacitance of the C_{dc} capacitor (Fig. 18.27 circuit) can be determined according to energy delivered to the load. For the required pulse voltage droop ΔV_0,

$$\Delta v_0 = \frac{V_{C_{dcf}}}{V_{C_{dci}}} \tag{18.72}$$

where $V_{C_{dcf}}$ is the capacitor voltage at the end-of-pulse, t_{on}, and $V_{C_{dci}}$ is the capacitors voltage immediately before the pulse. Considering Eq. (18.70), the difference between Eqs. (18.68), (18.69) is the energy stored in the C_{dc} capacitor at end-of-pulse mode, $E_{C_{dcf}}$:

$$E_{C_{dci}} - E_0 = E_{C_{dcf}} \tag{18.73}$$

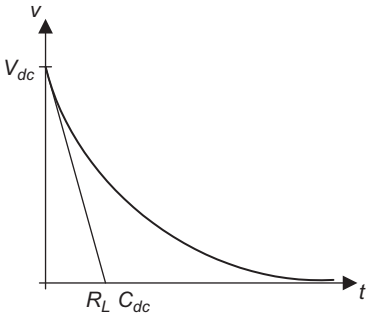


FIG. 18.28 Typical RC discharge waveform.

where Eq. (18.71) for this case results in

$$\frac{C_{dc} V_{dc}^2}{2} - \frac{V_{dc}^2}{R_L} t_{on} = \frac{C_{dc} (\Delta v_0 V_{dc})^2}{2} \tag{18.74}$$

considering that $V_{C_{dci}} = V_{dc}$. Equating (18.72), the capacitor value should satisfy the condition

$$C_{dc} \geq \frac{2 t_{on}}{R_L (1 - \Delta v_0{}^2)} \tag{18.75}$$

Considering Eqs. (18.68) through (18.73), it is mandatory to store in C_{dc} an energy greater than five times the pulse energy in order to have an output voltage droop better than 10%, but if a 1% voltage droop is expected, a 50 times storage energy is required, which may impose limits to the design of the modulator.

In addition, the V_{dc} power supply must be able to recharge the C_{dc} capacitor with an energy equal to the delivered pulse energy, E_0, plus losses, during the charging, $T - t_{on}$, and pulse, t_{on}, periods

$$P_{V_{dc}} = \frac{E_0}{T - t_{on}} + P_{loss} \tag{18.76}$$

During the initial charging of the capacitor C_{dc}, the PS takes a longer time in order to limit the power dissipation in the R_{dc} resistor.

The main disadvantages associated with the circuit in Fig. 18.27 are the S_m switch floating trigger terminals, resulting in a trigger signal that must be transmitted with galvanic isolation. Also, switch S_m must hold the total V_{dc} voltage during the *off* period, $T - t_{on}$, and conduct the load current during the *on* period.

Example 18.5 Consider the HV pulse modulator of Fig. 18.27 where $V_{dc} = 20$ kV. Calculate the value of the capacitor C_{dc} for applying 50 μs and 1600 Hz into an $R_L = 1$ kΩ load and the minimum power of the power supply, V_{dc}, considering 20% losses during the charging and pulse modes.

Solution Considering the capacitor C_{dc} initially charged with V_{dc} and a voltage droop of 5%, then Eq. (18.72),

$$\Delta v_0 = \frac{V_{C_{dcf}}}{V_{C_{dci}}} = \frac{19{,}000}{20{,}000} = 0.95$$

which results Eq. (18.75)

$$C_{dc} \geq \frac{2 t_{on}}{R_L (1 - \Delta v_0{}^2)} = \frac{2 \times 50 \times 10^{-6}}{1000 (1 - 0.95^2)} = 1.025\,\mu\text{F}$$

Choosing a 1.2 μF, then, the energy stored in C_{dc} initially is

$$E_{C_{dci}} = \frac{C_{dc} V_{dc}^2}{2} = \frac{1.2 \times 10^{-6} \times 20{,}000^2}{2} = 240\,\text{J}$$

The energy delivered to the pulse is

$$E_0 = \frac{V_{dc}^2}{R_L} t_{on} = \frac{20{,}000^2}{1000} \times 50 \times 10^{-6} = 20\text{J}$$

This means that after the pulse, the energy stored in the C_{dc} capacitor is 220 J, corresponding to a final pulse voltage of 19.149 V that is 4.2% voltage droop.

Finally, the PS V_{dc} must recharge the 20 J and 4 J (i.e., 10% losses) in $T - t_{on} = 625$ μs, and then,

$$P_{V_{dc}} = \frac{E_0}{T - t_{on}} + P_{loss} = \frac{20 + 4}{625 \times 10^{-6}} = 38.4\text{kW}$$

18.4.1.2 Ground Switch

It is possible to connect the switch S_m referenced to ground and the C_{dc} capacitor floating as shown in Fig. 18.29. Considering this circuit, when S_p is *off*, the C_{dc} capacitor is charged through the load. Supposing C_{dc} charged with V_{dc}, when S_m turns on the positive terminal of C_{dc} is grounded and a voltage of V_{dc} is applied into the load.

The main advantage of Fig. 18.29 configuration in relation to Fig. 18.27 is that S_m is grounded, which makes easier the triggering process. However, in the Fig. 18.29 circuit, during the pulse period t_{on}, the V_{dc} power supply is shorted, increasing dramatically the power dissipation in R_{dc}, which is a significant disadvantage that limits the operation to very low duty ratios.

If inductive-type loads are to be connected in both circuits, it is mandatory to use a freewheeling diode in parallel with the load to reset it after the pulse and, also, to maintain the magnetic energy continuity.

18.4.1.3 Series Stacks of Semiconductors

Considering the dozens of kV range pulse amplitude in the majority of PP applications and the limited maximum reverse voltage of semiconductor switches, such as power BJT, MOSFET, IGBT, GTO, and IGCT, it is necessary to connect many semiconductors in series to assemble the S_m and S_a switches in Figs. 18.27 and 18.29, as shown in Fig. 18.30 [38–43].

As seen, sharing resistors for steady-state and *RCD* snubber circuits for transient voltage balance are needed for *on-off* controlled semiconductors. In addition, it is complex to synchronously trigger many devices in series, placed at different floating high-voltage potentials.

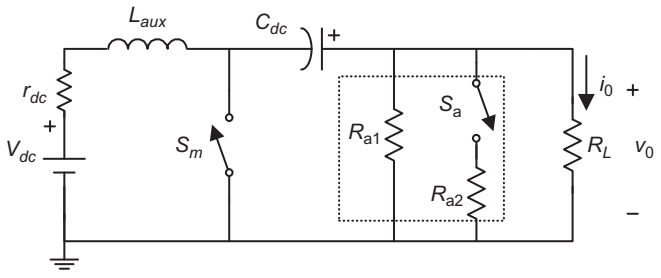


FIG. 18.29 Direct modulator simplified circuit with grounded switches.

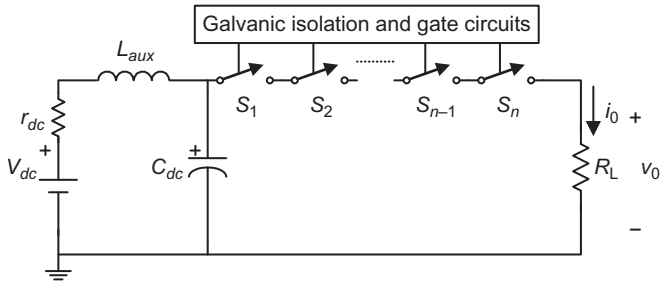


FIG. 18.30 Series-stacked semiconductor topology for high-voltage pulse generation.

Gate-control delay techniques or generalized cascades are used to force the synchronized operation of semiconductors with mismatched switching *on*/*off* characteristics [44].

Nevertheless, in order to prevent shutdown of a series-stacked semiconductor switch due to a defect arising in one semiconductor, redundant switches are, usually, included in the series, about 20% more, such that the surviving semiconductors share the voltage and the failed semiconductor is still able to carry the load current. This is true since the power switches used are built to short-circuit when failing [45].

In order to decrease the voltage hold-off stress on the semiconductors, it is possible to add a high-voltage step-up pulse transformer in the output, further increasing the output voltage to the desired amplitude. However, several issues must be taking into consideration before designing the circuit [44–47]:

1. The parasitic elements (i.e., distributed capacitance and leakage inductance) normally associated with the assembling of the transformer impose limitations to the output pulse waveform, degrading the pulse rise time and voltage plateau.
2. The transformer core volt-second product limits the transformer flexibility to accommodate different operating conditions, such as duty ratio and frequency.
3. After the pulse, it is mandatory to reset the transformer core magnetic flux back to the initial status before the next pulse, which imposes an auxiliary circuit.

Some of the topologies used in power electronics, designed for dc-dc isolated converters, can be specially modified for pulse generation, where the addition of the transformer gives the galvanic insulation and contributes to the reduction of the hold-off voltage in the semiconductors as described in the following sections.

18.4.2 dc-dc Isolated Converters

The use of classic high-voltage modulator topologies, such as the ones described in the last section, substituting the hard-tube

switches by stacked semiconductors is frequently not the best solution for high-voltage pulse generation when using semiconductors, due to the still high-voltage limitations of the devices and their sensibility to overvoltage and overcurrents.

Alternatively, it is advantageous to take into account the topologies that were originally designed for power semiconductors such as the dc-dc isolated converters. The literature refers the use of full-bridge, half-bridge, forward, and flyback converters in hard-switching and resonant topologies for applications such as rapid capacitor high-voltage charging, food processing, X-ray, plasma processing, and air and water pollution control [33–37].

The use of a transformer for galvanic isolation in the forward converter, derived from the buck dc-dc converter; the flyback converter, derived from the buck-boost dc-dc converter; and the bridge topologies can significantly reduce the voltage stress on the semiconductors. In this section, the focus is placed on the particular characteristics that enable high-voltage pulse generation, using relatively low-voltage semiconductor devices.

As the objective is to generate high-voltage pulses at the output, several changes must be introduced in the typical topologies and operating conditions of these circuits. The most obvious is the elimination of the output LC filter, used to keep the output voltage nearly constant.

In the following analysis, it is considered that the semiconductor switches have ideal switching behavior, instantaneous commutation times, zero voltage drop, and zero leakage current.

18.4.2.1 Forward Topology

The simplified forward-type circuit used to generate negative unipolar high-voltage pulses into a load is shown in Fig. 18.31 and the theoretical key waveforms in Fig. 18.32. For positive unipolar pulses, the ground should be placed on the opposite

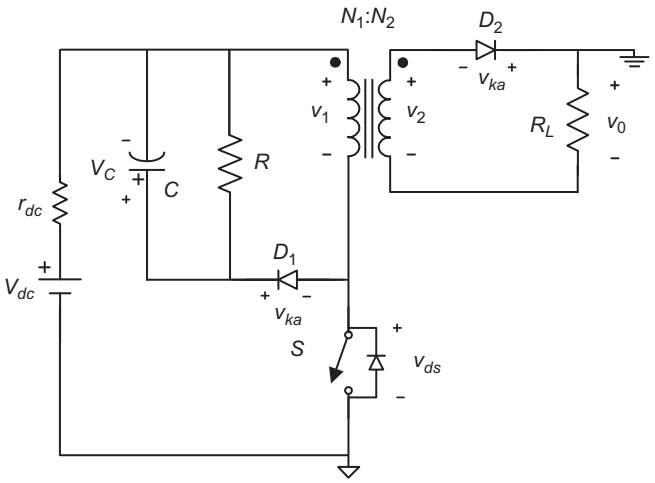


FIG. 18.31 Simplified layout of the pulsed power forward-type circuit used to generate negative high-voltage pulses to a load.

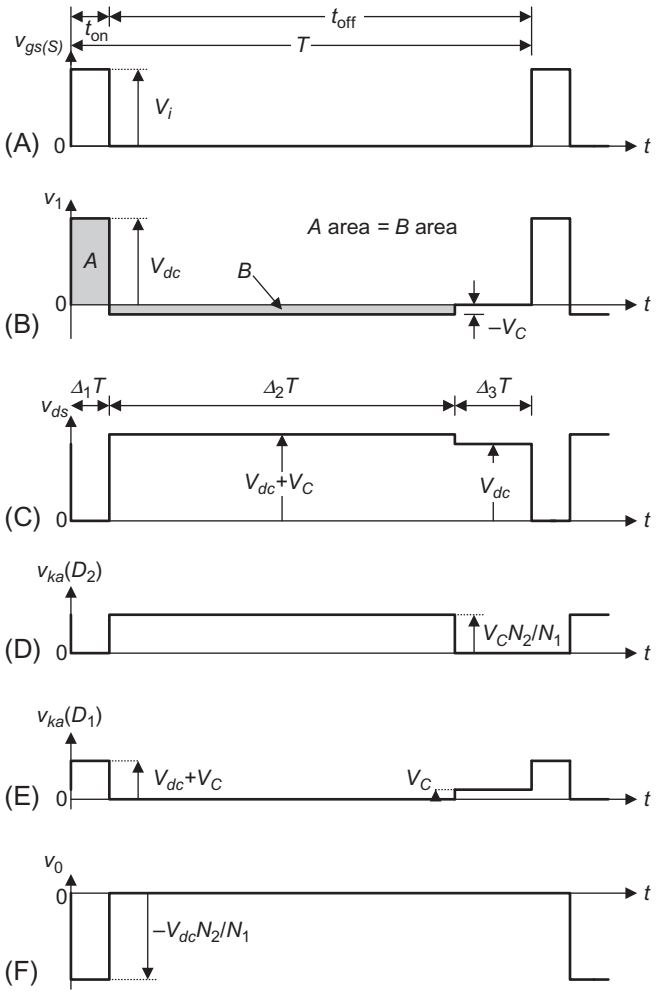


FIG. 18.32 Theoretical key waveforms for the circuit in Fig. 18.31, for a resistive load: (A) switch trigger signal v_{gs}, (B) primary winding voltage v_1, (C) switch voltage v_s, (D) D_2 reverse voltage, (E) D_1 reverse voltage, and (F) load voltage v_0.

secondary transformer terminal. The auxiliary RCD voltage clamp circuit connected to the transformer primary winding is used to reset the transformer using the lowest constant voltage. Considering that the RCD clamp capacitance C_s is sufficiently large, the voltage V_C across it can be assumed constant [48,49].

For pulse generation, the circuit operation can be explained considering only three operating modes [33,50]. In the first mode, the pulse mode, when the main switch S is turned *on* during $\Delta_1 T = DT = t_{on}$, where $\Delta_1 T = D$ and T are, respectively, the S duty ratio and operating period, the energy is transferred from the transformer primary winding circuit to the output. As the voltage applied to the transformer primary winding N_1 is V_{dc}, the secondary winding N_2 diode D_2 is *on*; thus, the voltage applied to the load is

$$v_0 = \frac{N_2}{N_1} V_{dc} \tag{18.77}$$

where N_2/N_1 is the transformer turn ratio, N. In addition, the RCD diode D_1 is *off*, with a reverse voltage of

$$v_{ka(D1)} = V_{dc} + V_C \tag{18.78}$$

For a resistive load R_L, the pulse amplitude is given by

$$i_0 = \frac{\frac{N_2}{N_1}V_{dc}}{R_L} \tag{18.79}$$

In the second mode, the reset mode, when the main switch S turns *off*, the RCD diode D_1 goes *on* and the voltage applied to transformer primary winding is $-V_C$, which resets the transformer core. During this time, $\Delta_2 T$, the secondary diode D_2 is *off*, holding off a reverse voltage of

$$v_{ka(D_2)} = \frac{N_2}{N_1}V_C \tag{18.80}$$

which results to a zero load voltage. From Eq. (18.80), the lower the V_C voltage and the transformer turns ratio N, the lower is the voltage hold-off by diode D_2. In addition, the switch S must hold off a voltage

$$v_s = V_{dc} + V_C \tag{18.81}$$

where V_C must be as low as possible to decrease this voltage.

Finally, in the third mode, the safety mode, following the transformer reset period, during $\Delta_3 T$, still with S *off*, the voltage applied to S is

$$v_s = V_{dc} \tag{18.82}$$

and the voltage applied to the transformer is zero. It is important to have $\Delta_3 T > 0$ in order to guarantee a safety operating margin for the transformer core reset. For practical operation, values between 20% and 30% should be sufficient. This is done be increasing the V_C clamp voltage above the calculated value.

The operation of the Fig. 18.31 circuit for high-voltage pulse generation imposes several conditions:

1. The use of a step-up transformer in order to decrease the voltage on the devices connected on the primary side
2. A minimum reset voltage V_C to guarantee the complete transformer core reset during the S off period, $\Delta_3 T > 0$, reducing at the same time the hold-off voltage of D_2 Eq. (18.80) and of S Eq. (18.81)

Considering the last, it is important to understand the relation between the reset voltage V_C with the operating conditions, such as the duty ratio D.

The reset voltage V_C can be calculated by equating the integral of the primary winding voltage, v_1, over one time period to zero

$$\begin{aligned}\frac{1}{T}\int_0^T v_1 dt = 0 \Leftrightarrow \frac{1}{T}\left[\int_0^{\Delta_1 T} V_{dc} dt\right. \\ \left. + \int_{\Delta_1 T}^{\Delta_1 T + \Delta_2 T} (-V_C) dt + \int_{\Delta_1 T + \Delta_2 T}^{T} 0 dt\right] = 0 \\ \Leftrightarrow V_C = V_{dc}\frac{D}{\Delta_2} = V_{dc}\frac{t_{on}}{\Delta_2 T}\end{aligned} \tag{18.83}$$

where $\Delta_2 T = \tau$ is the transformer core reset period.

For the boundary condition $\Delta_3 T = 0$ (i.e., $\Delta_1 T + \Delta_2 T = T$ and $\Delta_2 = D$), then, Eq. (18.83) becomes

$$V_c = \frac{D}{1-D}V_{dc} \tag{18.84}$$

substituting Eq. (18.84) in Eq. (18.80) the v_{ka} in diode D_2 is:

$$V_{ka(D_2)} = \frac{N_2}{N_1}V_C = \frac{N_2}{N_1}V_{dc}\frac{D}{\Delta_2} \tag{18.85}$$

Considering Eqs. (18.83), (18.85), introducing the load voltage module $|V_0|$, the ratio of τ/t_{off}, the reset time and the time when switch S is *off* it is received:

$$\frac{V_{ka(D_2)}}{|V_0|} = \frac{t_{on}}{\Delta_2 T} = \frac{t_{on}}{\Delta_2 T\frac{t_{off}}{t_{off}}} = \frac{t_{on}}{\frac{\Delta_2 T}{t_{off}}(T - t_{on})} = \frac{DT}{\frac{\Delta_2 T}{t_{off}}(T - t_{on})} \tag{18.86}$$

by simplifying becomes

$$\frac{V_{ka}}{|V_0|} = \left(\frac{D}{\frac{\tau}{t_{off}}(1-D)}\right) \tag{18.87}$$

which can be represented graphically by Fig. 18.33, where

$$\frac{\tau}{t_{off}} = \frac{\Delta_2 T}{(\Delta_2 + \Delta_3)T} = \frac{\Delta_2}{\Delta_2 + \Delta_3} \tag{18.88}$$

with $\Delta_1 + \Delta_2 + \Delta_3 = 1$ and $\Delta_1 = D$

The graphics in Fig. 18.33 shows the maximum load voltage hold-off by diode D_2 as a function of S duty ratio, D, and the transformer reset factor, τ/t_{off}.

Various conditions can be presented for high-voltage pulse generation by forward converters using low-voltage solid-state devices:

1. If the switching duty ratio is only a few percent and the resetting time extends to almost all the main switch-*off* time (i.e., $\Delta_2 T + \Delta_3 T$), diode D_2 holds off a small fraction of the output voltage.

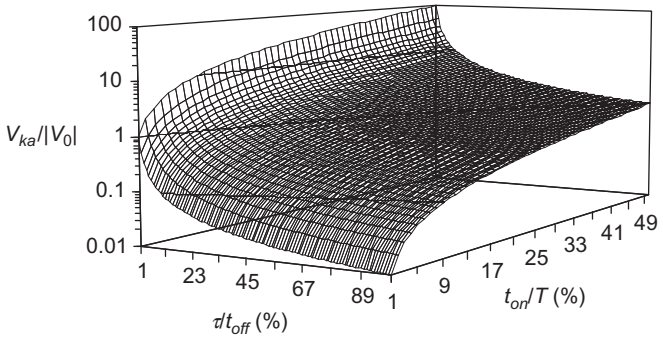


FIG. 18.33 Graphic representation of the reverse voltage of diode D_2 as a function of the reset time and duty ratio of the forward topology (Fig. 18.31).

2. If a step-up transformer is used, $N \gg 1$, this topology enables, also, the use of low hold-off voltage semiconductors in the primary transformer side, when compared with the output load voltage.

For safety reasons in order to ensure that the transformer core is fully reset, the transformer resetting time must end before the *off*-state of the *S* switch ends, $\Delta_3 T > 0$.

The short duty cycles required for generation HV pulses with low-voltage semiconductors are not a shortcoming, as most PP applications require short pulse widths and large recovery times.

Much care should be put in the design and assembling of the transformer as this element must sustain the HV between its terminals. In addition, this topology requires the polarity of the primary winding of the transformer to be identical to that of the secondary winding, and so, the energy of the load is obtained during the *on*-state of the switching device. Therefore, it behaves like a true transformer, wherein energy storage is undesirable, associated with the leakage inductance. However, the forward converter transformers have the poorest utilization and efficiency ratios, because neither the core nor the windings are used during the lengthy core reset interval.

Due to the low main switch *S* duty-cycle operation and transformer behavior, the RCD clamp voltage is designed for a low current, typically, a few % of the main circuit current.

The RCD clamp can be considered a buck-boost converter in discontinuous mode of operation, and designed so that, under any load conditions, during the *S* switch-*off* period the transformer core is fully reset [49].

For resetting the transformer core, other solutions can be implementing, such as a third auxiliary winding, but the fact that this transformer is for HV pulse generation limits in terms of parasitic, assembling complexity and safety.

EXAMPLE 18.6 Suppose the generation of −5 kV amplitude pulses with 5 μs and $f = 10$ kHz ($D = 5\%$) from the circuit in Fig. 18.31. The circuit is supplied from a mains transformer at $V_{dc} = 500$ V, and an $N = 10$ pulse transformer is used. Calculate the semiconductor switches *S*, D_1, and D_2 hold-off voltage.

SOLUTION Consider first boundary condition Eq. (18.84), and then,

$$V_C = \frac{D}{1-D} V_{dc} = \frac{0.05}{1-0.05} 500 = 26.3\,\text{V}$$

The semiconductors hold off 526.3 V for the *S* switch and diode D_1 and 263 V for diode D_2, respectively, 10.5% and 5.26% of the output voltage.

Consider now a reset factor of $\tau/t_{off} \approx 65\%$, and then, $\Delta_1 = 5\%$, $\Delta_2 \approx 62.5\%$, and $\Delta_3 \approx 32.5\%$. From (18.83),

$$V_C = V_{dc} \frac{t_{on}}{\Delta_2 T} = 40\,\text{V}$$

resulting in 540 V for the *S* switch and diode D_1 and 400 V for diode D_2, respectively, 10.8% and 8% of the output voltage.

Hence, for generating 5 kV pulse, 800 V semiconductors could be used, considering a 100% safety factor.

18.4.2.2 Flyback Topology

The simplified flyback-type circuit used to generate negative high-voltage pulses into a load is shown in Fig. 18.34, for positive pulses the ground should be placed on the opposite terminal.

The circuit in Fig. 18.34 is similar to the circuit in Fig. 18.31, but the polarity of the diode D_2 on the secondary winding is reversed. However, this simple change imposes completely different circuit behavior [48].

Considering the circuit in Fig. 18.34 and the theoretical key waveforms of Fig. 18.35, for boundary conditions, when the main switch *S* turns *on*, the energy is stored in the transformer

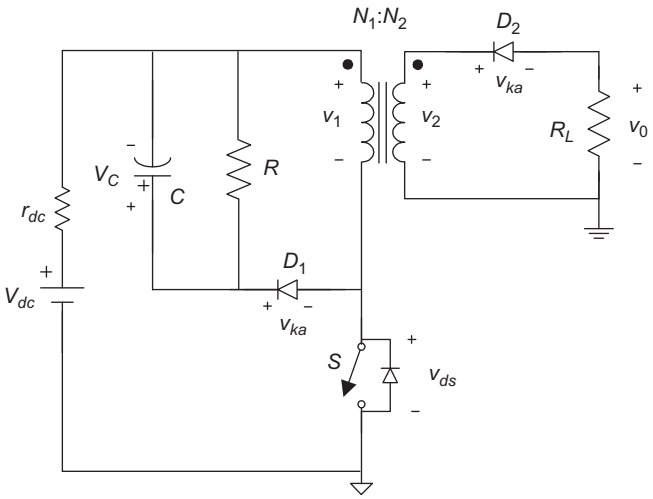


FIG. 18.34 Simplified layout of the pulsed power flyback-type circuit used to generate negative high-voltage pulses to a load.

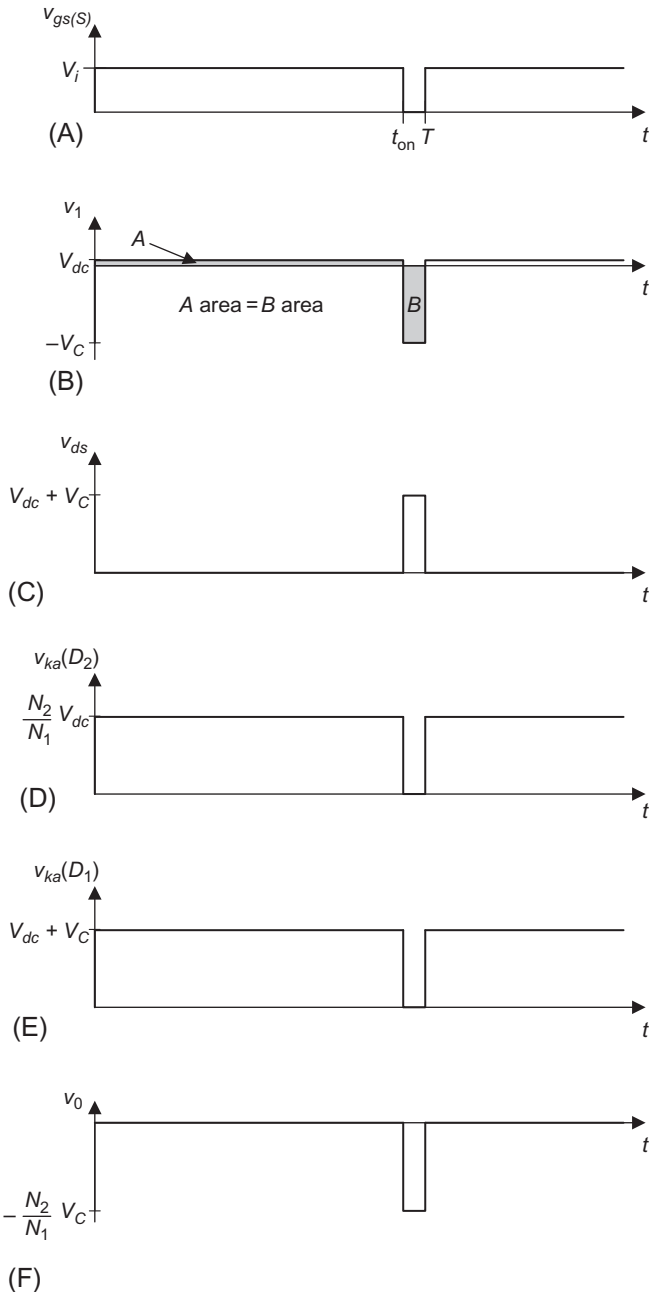


FIG. 18.35 Theoretical key waveforms for the circuit in Fig. 18.34, for a resistive load: (A) switch trigger signal v_{gs}, (B) primary winding voltage v_1, (C) Switch voltage v_s, (D) D_2 reverse voltage, (E) D_1 reverse voltage, and (F) load voltage v_0.

as magnetic flux, the transformer must act as a coil storing energy. The voltage applied to the transformer primary winding is V_{dc}, the RCD diode D_1 and the secondary winding diode D_2 are *off*, thus the voltage applied to the load is zero. The secondary diode D_2 reverse voltage is

$$v_{ka(D_2)} = \frac{N_2}{N_1} V_{dc} \tag{18.89}$$

and the RCD diode D_1 reverse voltage is

$$v_{ka(D_1)} = V_{dc} + V_C \tag{18.90}$$

When the main switch S is turned *off*, the energy stored in the transformer is transferred to the output. The voltage applied to the transformer primary winding is $-V_C$, and the RCD diode D_1 and the secondary winding diode D_2 are *on*, and voltage applied to the load is, approximately,

$$v_0 = -\frac{N_2}{N_1} V_C \tag{18.91}$$

The hold off voltage of the main switch S is

$$v_{ds} = V_{dc} + V_C \tag{18.92}$$

The RCD clamp voltage has two purposes: (i) reduce the voltage spike that occurs due to the resonance between the transformer leakage inductance and the switch S output capacitance, in the *off*-state and (ii) establish the pulse voltage during the same period of time.

Considering the transformer primary winding voltage waveform given in Fig. 18.35 the clamp voltage, V_C, can be approximately derived by equating the integral of the primary winding voltage, V_1, over one time period to zero

$$V_C = \frac{D}{1-D} V_{dc} \tag{18.93}$$

similar to the V_C voltage in the buck-boost topology Eq. (18.84).

Regarding high-voltage pulse generation [50], if the switching duty ratio is near 100%, D_2 blocks only a small fraction of the output voltage. Additionally, if the RCD diode D_1 is *on* during the S switch-*off* time, meaning the flyback circuit runs in continuous mode, the output voltage pulse is well defined by the RCD capacitors voltage V_C. Moreover, with a step-up transformer ($N \gg 1$), this topology also enables relatively low-voltage semiconductor devices in the primary side.

For efficiency reasons, the flyback circuit parameters should be calculated in order that the circuit works at the boundary between the continuous and noncontinuous state. This is done by assuring that the RCD diode D_1 turns *off* at the same instant the switch S turning *on*. The RCD clamp voltage is sized by the main circuit current due to the high duty ratio operation of switch S and the coil-like transformer behavior.

The flyback transformer design is more complex than the forward transformer, as the energy is supplied to the load during the *off*-state of the S switch, meaning that the transformer must be designed to store energy during the *on*-state of the S switch, behaving as a coupled inductor.

The S switch current interruption requirements and the coupled inductor design can be much more challenging in the flyback topology at power levels of interest and represent

a limitation of this topology. This is normally the realm of much higher current devices such as the IGBT and GTO or the use of parallel semiconductors.

Nevertheless, the flyback circuit is much more fault tolerant to a short-circuit in the load or load faults since the switch S is in the *off*-state during the output pulse and will not see the fault current as would the forward converter topology.

Comparing the forward with flyback topologies for HV pulse generation for the same output voltage pulse amplitude, using the same turn ratio transformer, the forward circuits need a high-amplitude dc PS voltage V_{dc}, but the RCD voltage is lower, and the switch S duty ratio is low. Also, in the flyback topology, the voltage pulse width is not as well defined as in the forward, because it is generated by the RCD circuit.

The two topologies have problems in dealing with capacitive loads, because the dynamic variations in the load impedance mismatch the output of the transformer. The solution requires the use of a permanent dummy load, but this increases the power dissipation. Another possibility is the use of a switch dummy load, which will put a semiconductor device in the high-voltage region.

Example 18.7 Suppose the generation of −5 kV amplitude pulses with 5 μs and $f = 10$ kHz ($D = 95\%$) from the circuit in Fig. 18.34. The circuit is supplied at $V_{dc} = 25$ V, and an $N = 10$ pulse transformer is used. Calculate the semiconductor switches S, D_1, and D_2 hold-off voltage.

Solution Consider Eq. (18.93), and then,

$$V_C = \frac{D}{1-D} V_{dc} = \frac{0.95}{1-0.95} 26.3 = 500\,\text{V}$$

The semiconductors hold off 526.3 V for the S switch and diode D_1 and 263 V for diode D_2, respectively, 10.5% and 5.26% of the output voltage.

Hence, for generating 5 kV pulse, 800 V semiconductors could be used, considering a 100% safety factor.

18.4.2.3 Bridge Topologies

The forward and flyback topologies are suitable for the generation of unipolar HV pulses. If bipolar pulses are needed, bridge configurations should be used, like the full- and half-bridge topologies with or without a step-up transformer [33,34,36,37].

Considering a half-bridge topology, Fig. 18.36A shows the configuration for obtaining positive pulses, where the switch S_1 applies the pulse to the load and switch S_2 is capable of applying a zero voltage to the load, which can be important if the load is capacitive, as shown in Fig. 18.36B, otherwise the load will stay charged. If antiparallel diodes are connected to the switches, pulses can be applied to inductive loads, where the S_2 antiparallel diode reset the load after the pulse. For negative pulses, the circuit is presented in Fig. 18.37A; similar operating behavior applies now for opposite polarity, as shown in Fig. 18.37B.

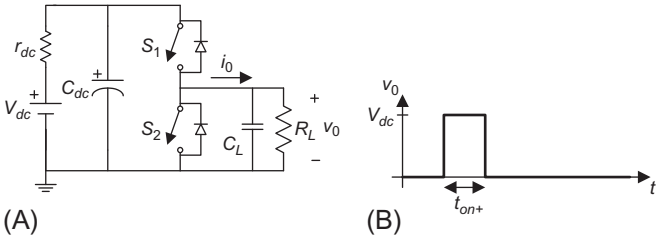


FIG. 18.36 Half-bridge topology for generating positive HV pulses: (A) simplified circuit and (B) output voltage, V_0, for a capacitive load, $C_L||R_L$.

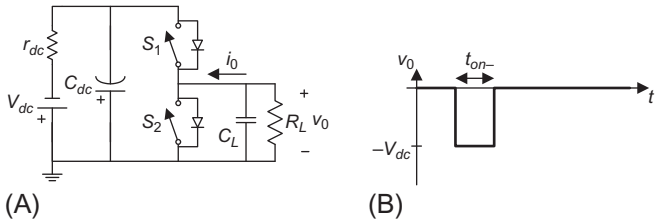


FIG. 18.37 Half-bridge topology for generating negative HV pulses: (A) simplified circuit and (B) output voltage, V_0, for a capacitive load, $C_L||R_L$.

The main limitation of this topology is the hold-off voltage of the semiconductors, which must block the same voltage as the dc HV power supply V_{dc}. If a transformer is connected in parallel with switch S_2, its antiparallel diode can reset the transformer core after the pulse, but this is limited to low duty ratio operation due to the low reset voltage impose by the diode.

If positive and negative pulse (i.e., bipolar) need to be generated using a half-bridge topology, then two power supplies are required, as shown in Fig. 18.38. In this case, each switch S_i must hold off the sum of the two power supplies voltages, that is, $2V_{dc}$. However, for capacitive-type loads, it is not possible to discharge the load capacitance after the pulse, as shown in Fig. 18.38B, since both S_1 and S_2 must be off.

In order to decrease the switches' voltage hold-off, it is common to use instead the full-bridge topology, shown in Fig. 18.39A, which also uses one less power supply. Each switch hold-off voltage is only V_{dc}. The use of more switches also increases the capability to deal with different load conditions, as shown in Fig. 18.39B. In fact, with the full-bridge topology

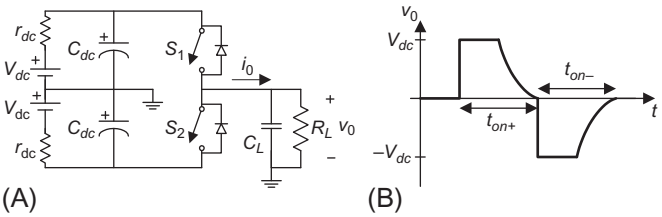


FIG. 18.38 Half-bridge topology for generating positive and/or negative HV pulses: (A) simplified circuit and (B) output voltage, V_0, for a capacitive load, $C_L||R_L$.

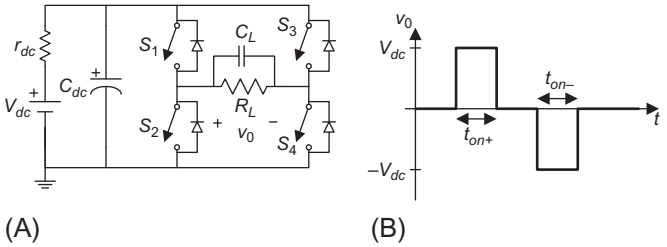


FIG. 18.39 Full-bridge topology for generating positive and/or negative HV pulses: (A) simplified circuit and (B) output voltage, V_0, for a capacitive load, $C_L||R_L$.

positive and/or negative pulses can be applied to any type of load. Nevertheless, depending on the flux of energy not all the controlled turn-off switches are always required.

These topologies are used in applications such as rapid high-voltage capacitor charging, food processing or air pollution control, where bipolar pulses enhance the process [27–31].

It is also possible to connect a transformer at the output terminals to increase the output voltage amplitude and to lower the hold-off voltage in the semiconductors switches if high-voltage pulses are to be generated, with the limitations already described. In order to limit the switches losses, it is common to use auxiliary inductors and capacitors in series or parallel configurations to couple the H-bridge to the HV transformer and also to guarantee a zero average voltage applied to the primary winding.

18.4.3 Cascaded Topology

The assembling of a single modulator circuit with very HV can be a very complex task and result in a number of problems:

- Transformer assembled with very high turn ratio and voltage output
- Many semiconductors stacked in series
- The presence of HV in small distributed volume and safety distances
- Coupling parasitic capacitances and inductances between devices

In order to avoid these problems, it is possible to cascade single modulators circuits where the output voltage is the sum of the individual outputs. However, care is needed in the connection of each circuit as voltage sharing between them is essential.

18.4.3.1 Modulators Without Output Transformers

In the topology shown in Fig. 18.40, there is no transformer between the energy storing capacitors and the load; the system is composed of basic pulse generator cells, made by a capacitor C_i and a switch S_i, stacked in series. The challenge in this type of generator is the uniform distribution of the voltage between each cell due to the floating nature of each cells and the high dv/dt with respect to the ground occurring during the rise

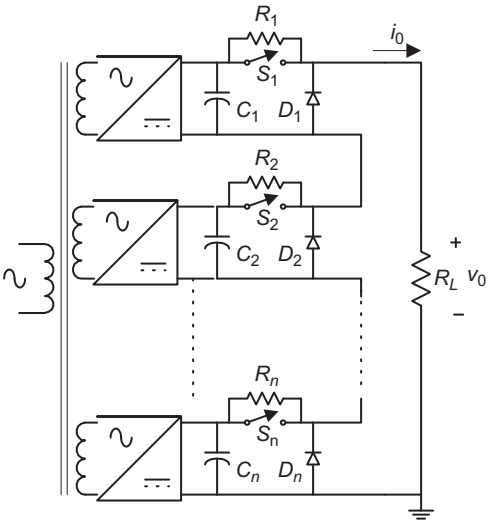


FIG. 18.40 Series-stacked modulator topology.

and falling time of the pulse. For this reason, great care must be taken in order to limit capacitance between each cell and the ground [18].

For proper operation, the capacitors in each cell of Fig. 18.40 circuit need to be charged using a galvanically isolated power supply. One of the possible methods includes the use of floating transformer secondary windings connected to an ac-dc converter, as shown in Fig. 18.40, using full-bridge converters operating as unity power factor rectifiers.

During the pulse period, the voltages of the individual cells are added up; hence, the output voltage is

$$v_0 = v_1 + v_2 + \cdots + v_n \tag{18.94}$$

and the current through all the switches is almost the same.

The freewheeling diode D_i in the output of each cell enables the switch of each cell *on* and *off* independently of other cells, which makes the system capable of adjusting the output voltage. This technique protects also the switches during the *on-off* commutation transient for any mismatch in the voltage distribution, where the R_i resistors help on equalizing the voltage in the S_i switches during *off*-state (see Section 18.2.5).

18.4.3.2 Modulators With Output Transformers

The construction of a single high-voltage pulse transformer, needing a high enough turns ratio ($N \gg 1$) to increase the output voltage, is complex due to the transformer nonideal behavior leading to significant parasitic effects as the output voltage rises. To solve this problem, it is possible to stack series several pulse transformers with lower turns ratio, in order to have only a fraction of the total voltage in each one [28,34,51]. With a careful design, the leakage inductance and distributed capacitances of the equivalent circuit are reduced as compared with one single equivalent transformer, leading

to a better rise time performance [52]. Another alternative is to use auxiliary windings in the transformer to couple leakage fluxes [47,53].

The most common ways to associate pulse transformers are shown in Fig. 18.41 [54]. The autotransformer-type cascade layout is shown in Fig. 18.41A, with three transformers, each one holding one-third of the output voltage v_0:

$$v_0 = v_1 + v_2 + v_3 \tag{18.95}$$

In this topology, power is supplied to T_{p2} and T_{p3} from the previous transformers. Transformer T_{p1} and T_{p2} have three secondary terminals, two of them to feed the primary of the next transformer, and the third to step-up the voltage of the next transformer. This configuration decreases significantly the distributed capacitive between windings.

The major advantage of the cascade association, of Fig. 18.41A, is that the isolation voltage between windings of each transformer is the same and equal to $v_0/3$. However:

- Considering transformers with equal turn ratio N and primary voltage, v_{in}, as each transformer is fed by the previous one, each transformer has a different power. Considering Fig. 18.41A, if the load power is P, neglecting the losses, in the first transformer, the input cascade power is P. The following transformer withstands $2P/3$, and the third transformer withstands $P/3$, being the total installed transformer power $2P$.
- Due to the inclusion of an extra terminal in the high-voltage side with different current ratings, the transformer assembling is complex.

Alternatively, Fig. 18.41B presents three transformers with the secondary windings in series, each one designed for one-third of the output voltage v_0. In the primary side, windings are in parallel, supplied by v_{in}, and referenced to ground. Hence, the isolation voltage between windings of each transformer is different.

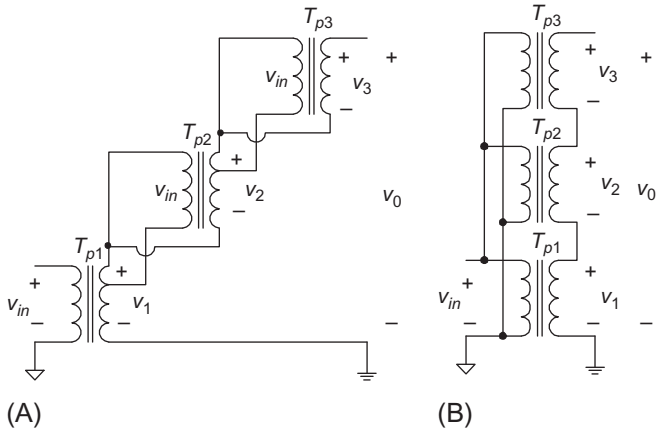


FIG. 18.41 Simplified transformers association: (A) cascade and (B) secondary windings in series.

Considering Fig. 18.41B, while the secondary winding potential in transformer T_{p2} and T_{p3} is, respectively, increased by $v_0/3$ and $2v_0/3$ through the secondary winding of transformer T_{p1} and T_{p2}, in the primary windings, the reference potential stays constant. As a result, each transformer holds a different voltage between windings, depending on the series position of each transformer, which increases toward higher potentials. Thus, transformer galvanic isolation between windings must be designed to $v_0/3$ for T_{p1}, $2v_0/3$ for T_{p2}, and v_0 for T_{p3}.

The above drawback sets serious difficulties for pulse applications of the Fig. 18.41B circuit. Since the pulse transformers placed at higher potentials hold higher voltages, the isolation distance should be increased. Consequently, the pulse waveform is distorted due to the increase of the parasitic leakage inductance with the isolation distance.

To overcome this problem, it is possible to feed the primary windings of the pulse transformers with galvanic isolated power supplies. This can be achieved with the introduction of isolation transformers, in order to keep the secondary windings of the pulse transformers in series but with the same isolation voltage between windings. This solution has the immediate advantage that all the pulse transformers are similarly built, with the same minimum isolation distance, which helps to reduce the output pulse rise time. Two configurations can be considered (Fig. 18.42):

- Independent isolation transformers (Fig. 18.42A)
- Cascade connected isolation transformers (Fig. 18.42B)

For both circuits in Fig. 18.42, the secondary windings of the pulsed transformer are series-connected, delivering each one (T_{p1}, T_{p2}, and T_{p3}) $v_0/3$ of the total output voltage v_0. In the circuit of Fig. 18.42A, the primary windings of T_{p1}, T_{p2}, and T_{p3} are fed, respectively, by the secondary windings of the isolation transformers T_{i1}, T_{i2}, and T_{i3}, these ones being fed by the input voltage v_{in}. In this way, the pulse transformers T_{p1}, T_{p2}, and T_{p3} can be assembled with the same structure and characteristics, for the same isolation voltage of $v_0/3$. The voltage increase due to the secondary winding series connection of T_{p2} and T_{p3} is sustained by the isolation transformer T_{i2} and T_{i3}. Then, for the worst running condition (considering a high capacitance between primary and secondary of the pulse transformers), the galvanic isolation of T_{i2} and T_{i3} must be predicted to hold, respectively, $v_0/3$ and $2v_0/3$. The isolation transformer T_{i1} is not necessary.

In the circuit of Fig. 18.42B, the primary windings of T_{p1}, T_{p2}, and T_{p3} are fed, respectively, by the secondary windings of T_{i1}, T_{i2}, and T_{i3}, with primary windings fed successively by the secondary windings of the previous transformer (i.e., T_{i3} fed by T_{i2}, which is fed by T_{i1}, which is fed by v_{in}). In this way, the pulse transformers T_{p1}, T_{p2}, and T_{p3} can be assembled with the same structure and characteristics, for the same isolation voltage of $v_0/3$. The voltage increase due to the secondary winding series connection of T_{p2} and T_{p3} is held by the isolation transformer T_{i2} and T_{i3}. The isolation transformer T_{i1} is not needed.

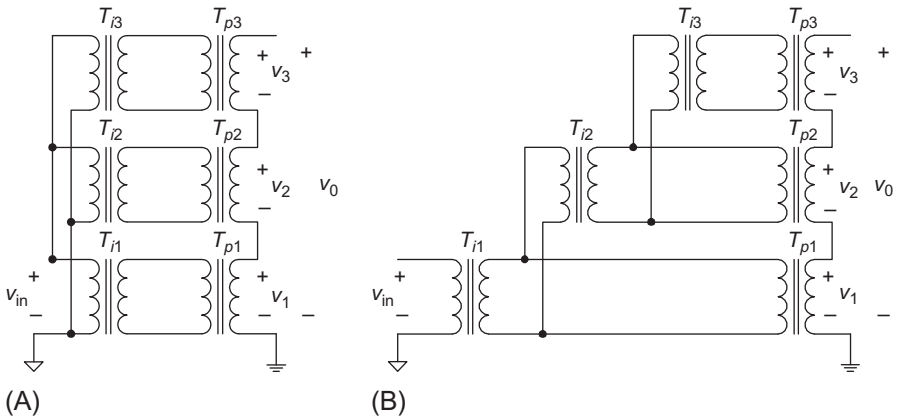


FIG. 18.42 Simplified layout of series-connected secondary winding transformers fed by (A) independent isolation transformers and (B) cascade isolation transformers.

Taking into account the two circuits of Fig. 18.42:

- In Fig. 18.42A, considering a load power P and neglecting the losses in the transformers, each one is assembled for a power of $P/3$ (i.e., the power installed in all the transformers is $2P$). However, in Fig. 18.42B, the pulse transformers are assembled with a power of $P/3$, but the isolation transformers have successive powers of P, $2P/3$, and $P/3$. The total power installed in all the transformers is $3P$.
- In Fig. 18.42B, all the transformers have the same isolation voltage, while in Fig. 18.42A, the isolation voltage in isolation transformers is different.

Considering only the pulse transformers, the two topologies, in Fig. 18.42, are equivalent. Hence, the choice between the two should be based on the characteristics preferred for the isolation transformers and the features desired for the pulse generator.

Regarding the last, it is considered a great advantage for the high-voltage pulse generator to be of modular construction, built upon several equal modules, where each one could occupy any position in the generator.

Example 18.8 Consider the generation of −15 kV pulse from a series stack of three −5 kV forward HV pulse generators based on the topology shown in Fig. 18.31, with the operating conditions of Example 18.6. Select the stack method to implement and draw the complete assembly, taking into consideration a modular perspective. Specify, also, the energy supply to the three stages, the selection of semiconductors and their triggering.

Solution The modular high-voltage generator construction is based on three main principles:

- Distribute the total voltage of a high-voltage circuit by holding the potential of several points in the circuit relatively to ground.
- Distribute the total voltage for several transformers connected in series.
- Use isolation transformers to feed the primary of the series-connected transformers, as shown in Fig. 18.42A.

The proposed circuit layout is shown in Fig. 18.43. If positive pulses are desired, it is only necessary to invert the polarity of the secondary diodes D_{ri}, where $i \in \{1, 2, \ldots, n\}$. Power is supplied to the three modules via isolation transformers (1:1), T_{ii}, which must hold off a maximum voltage of 1 kV between primary and secondary. These transformers are assembled with primary windings in parallel, connected to a dc-ac high-frequency inverter to reduce the size and increase the efficiency of the system. In addition, each secondary winding is connected to an ac-dc rectifier that produces the necessary v_{dci} voltage to the forward converters.

Considering the −5 kV voltage at each individual forward pulse generator with the operating condition of Example 18.3, then, 800 V semiconductors can be used. Hence, MOSFETs can be select for switches S_i.

Considering the three modules, in Fig. 18.43, with switch S_i *on*, diodes D_{ri} are conducting, and the voltage applied to the load is

$$v_0 = -(v_{01} + v_{02} + v_{03}) = -3 \times 5000 = -15\text{kV}$$

considering three equal modules, $v_{01} = v_{02} = v_{03} = v_{0i}$. During this time, the voltage reference at the secondary terminal with a dot point of each pulse transformer is raised:

$$v_{ref\ Tp1} = 0\text{V}$$

$$v_{ref\ Tp2} = (2-1)v_{0i} = -5\text{kV}$$

$$v_{ref\ Tp3} = (3-1)v_{0i} = 2 \times 5000 = -10\text{kV}$$

During the off time of switches S_i, the voltage applied to the load goes to zero, diodes D_{ri} in each module hold off only

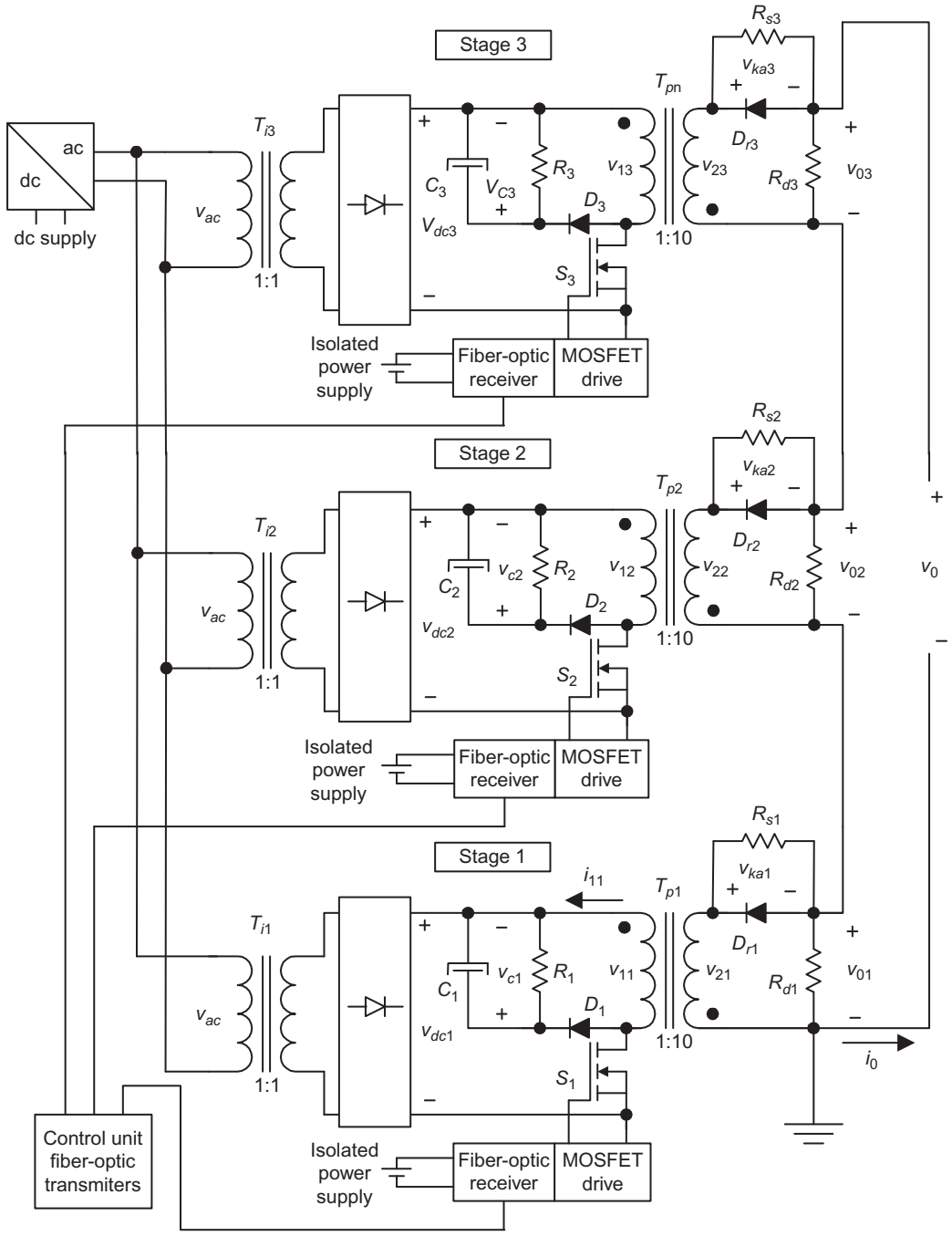


FIG. 18.43 Modular pulsed generator simplified layout for −15 kV output pulses.

the reset voltage of their respective pulse transformer. Voltage sharing resistors, R_{si}, are used to equally distribute the reset voltages of each module through diodes D_{ri}. In order to hold the high-voltage potential in each module relative to ground, high-valued R_{di} resistances can also be used.

Regarding the triggering of the MOSFETs in each stage, dc isolated power supplies are used in each stage to supply the necessary energy to the trigger drives that receives the signals by optical fiber from the ground control circuit.

18.4.4 Solid-State Marx Generators

The use of voltage multiplication techniques for generating HV repetitive pulses is not limited to the use of transformers. More complex methods can be used without the limitation of transformers. The most common is the Marx generator concept [55].

The Marx generator concept is presented in the circuit of Fig. 18.44, which comprises a number of modular stages

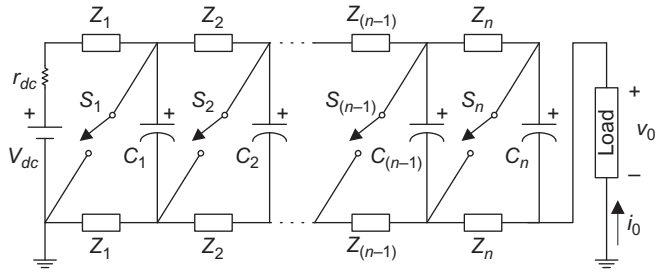


FIG. 18.44 Marx generator topology for producing repetitive negative high-voltage pulses into a load.

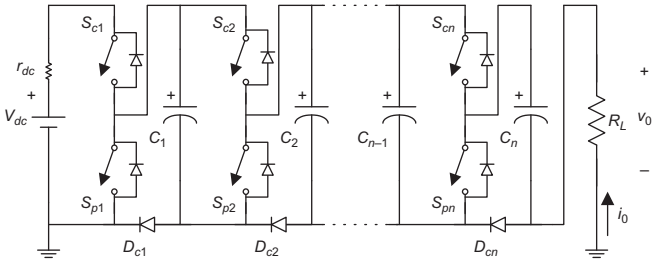


FIG. 18.45 Circuit for applying HV negative repetitive pulses into resistive load.

constituted by an energy storage capacitor C_i, two impedances Z_i (resistive and/or inductive) for charging and limiting the self-short-circuit capacitor paths and a switch S_i, for $i \in \{1, 2, \ldots, n\}$. During the charging period, a relatively low-voltage dc power supply V_{dc} charges the C_i capacitors in parallel through impedances Z_i.

When switches S_i are turned *on*, the C_i capacitors are connected in series and apply a voltage into the load, equal to

$$v_0 = -nV_{dc} \tag{18.96}$$

depending that the capacitors are charged to the power supply full voltage, V_{dc}. During this time, the bottom impedances Z_i limit the self-short-circuit path of the C_i capacitors.

The circuit in Fig. 18.44 is assembled in such a way that there is voltage modularity, meaning that each stage holds the power supply voltage V_{dc}. However, due to this parallel process, the first stages carry the total charging current, which sets different power requirements for the devices in each stage.

This concept has been used intensively through the years, with spark gaps used as switch S_i for very high-voltages and powers, but the spark gap only turns *off* when the current goes to zero. Recent technological upgrades with the addition of solid-state switches and the replacement of most of the passive elements increased the lifetime of the modulator and allowed higher pulse repetition rates, meaning an improved performance [22,56–58].

18.4.4.1 Generation of Negative Pulses

During the last years, various semiconductor-based Marx and SM topologies have been described, with analogous characteristics in order to reduce the losses and increase the performance of the circuit for different types of applications and loads [22,56–58].

Fig. 18.45 shows a typical SM topology, with n stages able to deliver negative high-voltage repetitive pulses into a load R_L; the theoretical key waveforms are shown in Fig. 18.46. Each stage of the SM consists of an energy storing capacitor C_i, a diode D_{ci}, and two switches S_{ci} and S_{pi}, with antiparallel diodes, where the subscript $i \in \{1, 2, \ldots, n-1, n, n+1\}$. The S_i switches can be implemented with BJTs, GTOs, IGCTs, IGBTs, MOSFETS, or other *on-off* devices. The inclusion of

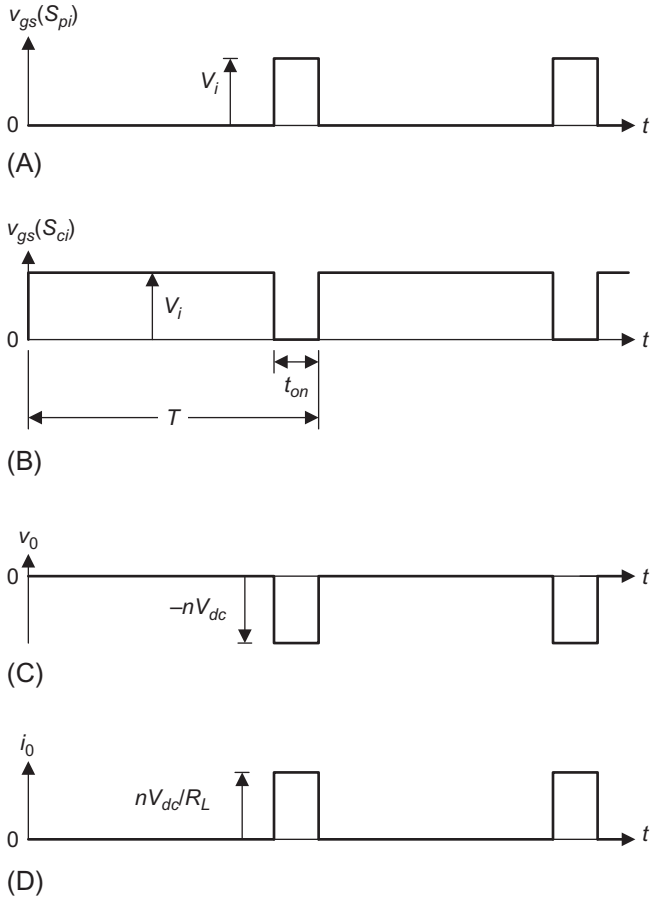


FIG. 18.46 Theoretical waveform for the operation of the circuit in Fig. 18.45: (A) trigger signal of switches S_{pi}, $v_{gs(Spi)}$; (B) trigger signal of switches S_{ci}, $v_{gs(Sci)}$; (C) output voltage, v_0; and (D) output current, i_0.

S_{c1} guarantees that during the pulse period, the dc charging power supply V_{dc} is not short-circuited, preventing high-current-load pulses through the power supply.

Considering resistive load, R_L, the operation of the Fig. 18.45 modulator can be understood considering two operating modes, for a switch duty ratio $D = t_{on}/T$. In the first one, switches S_{ci} and S_{pi} are, respectively, turned *on* and turned *off*. During the charging period, $(T - t_{on})$, capacitors C_i are

charged from the dc charging power supply, V_{dc}, with current limited by the internal resistance of the semiconductors, the wires, and the dc charging power supply internal resistance (or externally added) R_{dc}, resulting in a small time constant that enables kHz operation. The *on*-state of D_{ci} ensures that during this period, the voltage, V_0, applied to the load is, approximately, zero.

In the second operating mode, switches S_{ci} and S_{pi} are, respectively, turned *off* and turned *on*. During the pulse mode, t_{on}, capacitors C_i are connected in series and their voltage applied to the load. The load voltage v_0 is proportional to the charging power supply:

$$v_0 = -knV_{dc} \tag{18.97}$$

where n is the number of stages and $k<1$ characterizes the nonideal behavior of the passive and active elements in the circuit and operating conditions.

The D_{ci} diodes guarantee, also, that the S_{pi} switches only block a maximum voltage of V_{dc}, even in fault condition, such as the lack of synchronization. Considering Fig. 18.45, for example, if switch T_{pn} is *off* during pulse mode, D_{cn} conducts and short-circuits the last stage, imposing an output voltage of

$$v_0 = -k(n-1)V_{dc} \tag{18.98}$$

The operation of Fig. 18.45 circuit can be represented by its equivalent model during both operating modes, considering ideal switches and $C_i = C$. During the charging mode, the C_i capacitors are in parallel, and the circuit can be model as shown in Fig. 18.47A, where nC is the equivalent capacitance, seen by the power supply, charged with V_{dc}. In addition, during pulse mode, the C_i capacitors are in series, where C/n is the equivalent capacitance, seen by the load, charged with nV_{dc}, as shown in Fig. 18.47B.

The energy stored in the C_i capacitors, during $T-t_{on}$, is

$$E_{C_i} = \frac{n}{2}CV_{dc}^2 \tag{18.99}$$

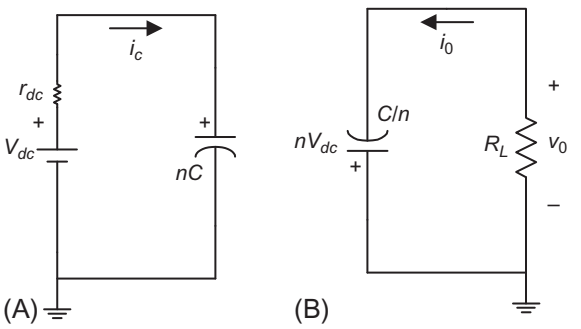


FIG. 18.47 Equivalent circuit of Fig. 18.45: (A) the charging mode and (B) the pulse mode, for negative output pulses.

and the energy delivered to the load, during t_{on}, is

$$E_0 = n^2\frac{V_{dc}^2}{R_L}t_{on} \tag{18.100}$$

For pulse power applications, only a small fraction of the stored energy should be transferred to the output during the pulse mode, otherwise the pulse voltage has a typical RC discharge waveform, not an almost rectangular shape. Considering a resistive load R_L, the capacitance of the C_i capacitors in Fig. 18.45 circuit can be determined according to energy delivered to the load. For the required pulse voltage droop,

$$\Delta v_0 = \frac{V_{C_f}}{V_{C_i}} \tag{18.101}$$

where V_{C_f} is the capacitor voltage at the end-of-pulse mode, t_{on}, and V_{C_i} is the capacitors voltage immediately before pulse mode. Considering Eq. (18.101), the difference between Eqs. (18.99) and (18.100) is the energy stored in the C_i capacitors at end-of-pulse mode, E_{C_f}:

$$E_{C_i} - E_0 = E_{C_f} \tag{18.102}$$

where Eq. (18.102) for this case results in

$$\frac{n}{2}CV_{dc}^2 - n^2\frac{V_{dc}^2}{R_L}t_{on} = \frac{n}{2}C(\Delta v_0 V_{dc})^2 \tag{18.103}$$

Assuming that $V_{C_i} = V_{dc}$, equating (18.103), the capacitor value should satisfy the condition

$$C \geq \frac{2nt_{on}}{R_L(1-\Delta v_0^2)} \tag{18.104}$$

Considering Eqs. (18.99) through (18.104), it is mandatory to have storage energy greater than five times the pulse energy in order to have an output voltage droop better than 10%, but if a 1% voltage droop is expected, a 50 times storage energy is required, which impose limits to the design of the modulator.

The power dissipation in the switches and the capacitors charging time impose a high-voltage pulse frequency limitation. Therefore, this circuit operates better with low duty ratio, D, pulses as required in most PP applications.

In addition, the V_{dc} power supply must be able to charge the C_i capacitors with an energy equal to the delivered pulse energy, E_0, plus losses during the charging time, $T-t_{on}$:

$$P_{V_{dc}} = \frac{E_0}{T-t_{on}} - P_{loss} \tag{18.105}$$

where the P_{loss} term represents the power dissipated in the circuit wiring and switches.

This determines the maximum power rating for the V_{dc} power supply that imposes the maximum operating frequency, pulse duty ratio, and load power to the modulator.

To build and operate the circuit of Fig. 18.45, some design consideration must be considered. First, during start-up, when the energy storing capacitors are completely discharged, the charging voltage V_{dc} must be slowly increased in order to limit the charging current on the switches S_{ci} and D_{ci}, which is critical in the first stages due to the parallel charging topology of the capacitors.

Actually, in the parallel charging method, the semiconductor modules current loading is not equal. For instance, in the Fig. 18.45 circuit, switch S_{c1} conducts current required to capacitors C_1, C_2…, C_{n-1}, C_n, switch S_{c2} conducts charging current for C_2, C_3…, C_{n-1}, C_n, and so forth. Thus, in practical implementation, modules with successive decreasing current ratings can be used, the benefits of standardization being somewhat compromised.

Also, the S_{ci} and S_{pi} switches conduct different current values, respectively, the discharge and pulse current. Hence, instead of switches needing to block unequal voltages, they are required to conduct unequal currents.

Consequently, when choosing semiconductors to implement the *S* switches, it is fundamental that the semiconductor current rating must be selected to guarantee that the devices work always in the saturation region inside the forward safe operating area. If not, during the first instants of the *on*-state (when the current is high) the semiconductors can operate in the active region where the voltage drop and losses are higher, which might destroy the devices.

The switches triggering is another important concern in these circuits. There are two drive signals, $v_{gs(Spi)}$ and $v_{gs(Sci)}$, respectively, to S_{pi} and S_{ci}, which should be triggered synchronously. Since all the semiconductor switches are at different high-voltage potentials, gate drive circuits with galvanic isolation are required (the use of optical fibers is mandatory to transmit the gate signals and to reduce stray capacitances to ground and neighbor cells), together with isolated power supplies to further process the transmitted gate signal and supply power to the gate drivers.

Several authors have come up with solutions to supply power to semiconductor triggering drivers for high-voltage applications. The most common include isolation transformers [59], but diode strings are also described [57].

The circuit in Fig. 18.45 enables the use of typical half-bridge semiconductor structures currently integrated in modular packages, which is advantageous to assemble the circuit and trigger the semiconductors, since it allows bootstrap operation [10].

However, the circuit topology shown in Fig. 18.45 is not suitable for dealing with capacitive loads. In fact, if a capacitive-type load is connected to the circuit output, the load stays charged after the HV pulse with a negative voltage until the charging mode of the energy storing capacitors. However, during the charging period, the load is not shorted by the D_{ci}, except if the energy stored in the load is very low and the charging current of capacitors C_i is sufficient to turn-on diodes D_{ci}.

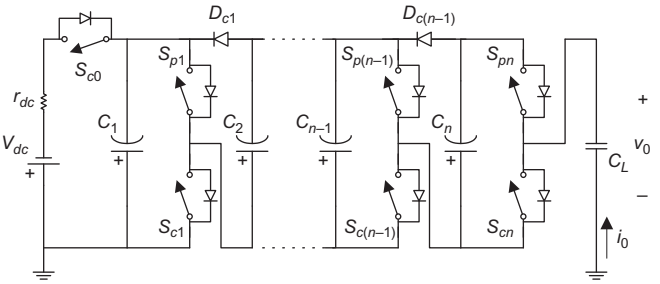


FIG. 18.48 Circuit for applying HV negative repetitive pulses into a capacitive load, with a negative dc power supply, V_{dc}.

In order to guarantee the discharge of the load capacitances after the negative HV pulse, it is necessary to change the Fig. 18.45 circuit topology for the one shown in Fig. 18.48, which also produces negative HV pulses into the load.

Considering the circuit in Fig. 18.48, as the V_{dc} power supply is negative, it is necessary to change the topology in comparison with Fig. 18.45 in order to maintain a similar operating behavior. The two main differences are the addition of an extra switch, S_{c0}, which guarantees that during the pulse period, the dc charging power supply V_{dc} does not participate in the pulse mode, t_{on}. The most important regards the fact that during the charging period, $T-t_{on}$, the S_{ci} switches short-circuit the load discharging any capacitance, as the one shown in Fig. 18.48.

Considering now the application of negative HV pulses into inductive loads, the circuit in Fig. 18.45 requires an additional half-bridge switching structure that connects to the load, as shown in Fig. 18.49.

As shown in Fig. 18.50, the operation of the circuit in Fig. 18.49 in comparison with circuit of Fig. 18.45, has some changes, which includes one additional time period for enabling the reset of the inductive load by the freewheeling diodes, T_{ab}, besides the charging, T_c, and pulse modes, t_{on}, in order to impose a zero average voltage to the load.

During the charging period, the *on*-state of D_{ci} and the $S_{p(n+1)}$ antiparallel diode ensures that the output voltage, V_0, applied to the load is approximately zero.

After the HV negative pulse, t_{on}, the S_{ci} and S_{pi} switches are turned *off*, but in order to conserve energy, the inductive load current, i_0, must have an alternative path. This path is set by

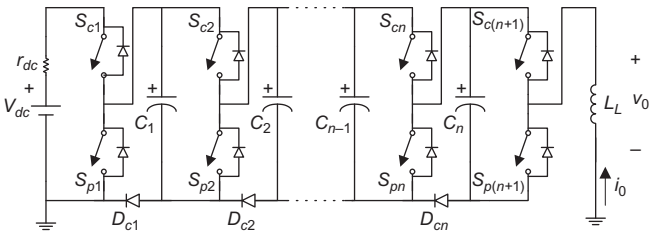


FIG. 18.49 Circuit for applying HV negative repetitive pulses into an inductive load.

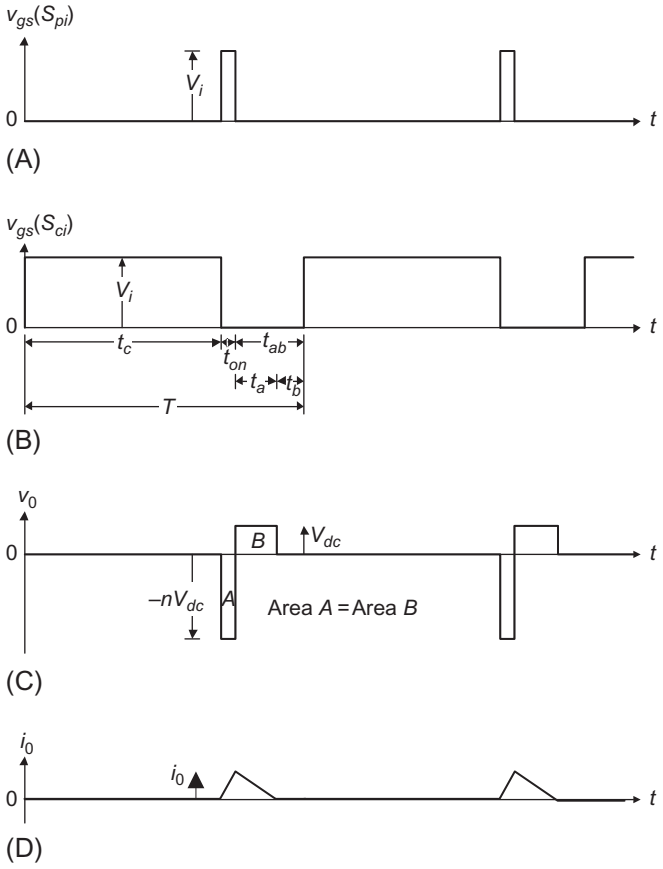


FIG. 18.50 Theoretical waveform for the operation of the circuit in Fig. 18.49: (A) trigger signal of switches S_{pi}, $v_{gs(Spi)}$; (B) trigger signal of switches S_{ci}, $v_{gs(Sci)}$; (C) output voltage, v_0; and (D) output current, I_0.

freewheeling diodes (S_{ci} antiparallel diodes and D_{ci} diodes) and the capacitor with the lowest voltage, which is charged. Normally, C_n has the lowest voltage; thus, the current path is through the $S_{c(n+1)}$ antiparallel diode D_B, capacitor C_n, and diodes $D_{c1}-D_{cn}$. During this time, T_a, the voltage applied to the load is, about, V_{dc} (voltage in capacitor C_n), resetting the inductive load. Capacitor C_n is charged until its voltage is equal to the capacitor C_{n-1} voltage, after which, if there is still energy in the load, the current path changes to capacitor C_{n-1}. As the maximum clamping voltage is V_{dc}, the higher the number of stages the longer the resetting time.

In this way, most of the load magnetic energy is sent back to energy storing capacitors C_i, after which the load current i_0 goes to zero, and it can be imposed again the charging mode of operation. It is important to have a safety time t_b in order to guarantee the completely reset of the load. Due to this load energy recovery method, the power supply energy needed to charge the capacitors after each pulse is lower, and the yield of this modulator can be higher.

Example 18.9 A negative solid-state Marx generator needs to be assembled for delivering −9 kV and 25 μs pulses into a 900 Ω resistive load, with less than 20% voltage droop. Considering the existing equipment, there are two alternatives: (1) $V_{dc}=1.5$ kV, $n=6$, and $C_i=1$ μF and (2) $V_{dc}=1$ kV, $n=9$, and $C_i=1$ μF. Determine which is the best alternative.

Solution Considering the capacitance of 1 μF in each stage, then, the pulse voltage droop can be determined by Eq. (18.104). Hence, for the first alternative,

$$C=\frac{2nt_{on}}{R_L(1-\Delta v_0{}^2)}\Leftrightarrow 10^{-6}=\frac{2\times 6\times 25\times 10^{-6}}{900(1-\Delta v_0{}^2)}\Leftrightarrow \Delta v_0=0.816$$

and for the second alternative,

$$C=\frac{2nt_{on}}{R_L(1-\Delta v_0{}^2)}\Leftrightarrow 10^{-6}=\frac{2\times 9\times 25\times 10^{-6}}{900(1-\Delta v_0{}^2)}\Leftrightarrow \Delta v_0=0.707$$

which gives, respectively, 18.35% and 29.23% voltage droop, meaning that after the pulse the capacitors stay charged with about Eq. (18.101), respectively, 1224.7 and 707.1 V. Hence, only the first alternative keeps the pulse voltage droop below 20%. In this case, the energy stored in the capacitors is Eq. (18.99) 6.75 J, three times bigger than the energy delivered to the load during each pulse Eq. (18.100) 2.25 J.

18.4.4.2 Generation of Positive Pulses

The solid-state Marx modulators for generating positive HV pulses, with different load conditions, have equivalent properties as the ones for negative pulses, shown in the last section, besides the necessary modifications to enable the change in the output polarity. Thus, Fig. 18.51 shows the basic topology of the SM, with n stages, able to deliver positive high-voltage repetitive pulses into resistive and capacitive loads, R_LC_L.

During the pulse mode, t_{on}, the switches S_{ci} and S_{pi} are, respectively, turned *off* and turned *on*. Capacitors C_i are connected in series and their voltage applied to the load. The load voltage v_0 is proportional to the charging power supply:

$$v_0=knV_{dc} \tag{18.106}$$

where n is the number of stages and $k<1$ characterizes the nonideal behavior of the passive and active elements in the

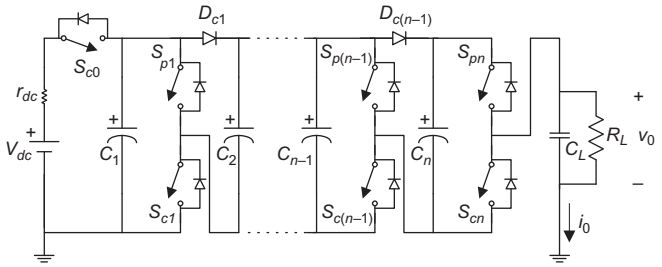


FIG. 18.51 Circuit for applying HV positive repetitive pulses into resistive and capacitive loads.

circuit and operating conditions. Also, in this topology, for example, if S_{pn} is *off* during pulse mode, the antiparallel S_{cn} diode conducts and short-circuits the last stage, imposing an output voltage of

$$v_0 = k(n-1)U_{dc} \tag{18.107}$$

Actually, the Fig. 18.51 circuit is equivalent to Fig. 18.45 circuit, whereas in this case with a positive V_{dc} power supply, it can produce positive HV pulses for both resistive and capacitive loads. The capacitive load can be driven, given that during the charging mode of capacitors C_i, the load is short-circuited by the S_{ci} switches, stray inductances limiting the discharge rate.

Considering now the application of positive HV pulses into inductive loads, the circuit in Fig. 18.51 requires an additional switch S_{p0} and diode D_0 at the input, as shown in Fig. 18.52.

The circuit operation requires, also, an additional time period for resetting the inductive load by the added freewheeling diodes, t_{ab}, in addition to the charging, t_c, and pulse modes, t_{on}, in order to impose a zero average voltage to the load.

Considering an inductive load, after the HV positive pulse, the S_{ci} and S_{pi} switches are *off*, and the path for the inductive current i_0 is set by the capacitor C_n, which usually has the lowest voltage, the S_{ci} antiparallel diode and diode D_B. During this time, the voltage applied to the load is approximately $-V_{dc}$ (the voltage in capacitor C_n), resetting the inductive load. After the load current i_0 goes to zero, the charging mode of operation can be imposed.

18.4.5 Solid-State Marx-Based High-Voltage Switches

The solid-state Marx generator concept described in the last section can be used for distributing the voltage in series-stacked semiconductors. Further, the Marx generator circuit can be used as a series switch, maintaining some intrinsic properties, which are desirable for the use with relatively low-voltage semiconductors, such as equal voltage distribution between stages and the fact the semiconductors in each stage hold off only the stage voltage capacitor.

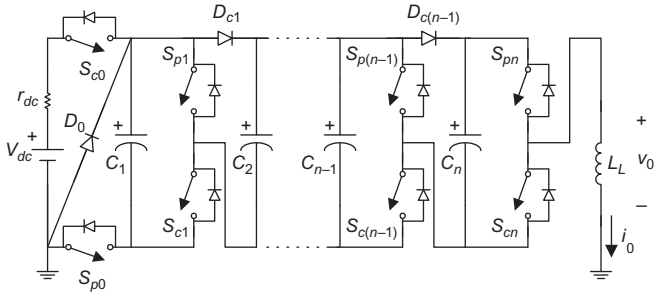


FIG. 18.52 Circuit for applying HV positive repetitive pulses into an inductive load.

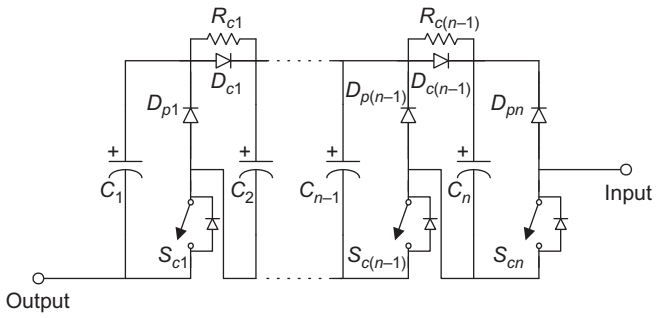


FIG. 18.53 Series switch for positive voltages based on the Marx concept.

The Marx series switch, based on the solid-state Marx of Fig. 18.51, for positive voltages, is shown in Fig. 18.53 not to apply voltage but to hold it between its terminals. Therefore, the input power supply V_{dc} is removed, and the S_{pi} switches are replaced by diodes D_{pi}. Also, resistors R_{ci} are connected in parallel with the D_{ci} diodes in order to balance the voltage in the capacitors C_i.

Consider the common HV pulse power topology of Fig. 18.54, where switches S_1 and S_2 commutate alternately. A HV power supply, V_{dc}, charges an energy storage capacitor C_{dc}, with current limited by resistor R_{dc}. The switch S_1 applies the capacitor C_{dc} voltage v_c to the capacitive load $C_L||R_L$, during the pulse period, t_{on}. Subsequently, switch S_2 discharges the load and other circuit parasitic capacitances to zero.

Taking into account the proposed operating scheme, each switch S_i, where $i \in \{1, 2\}$, holds a maximum voltage equal to the power supply voltage amplitude, V_{dc}, considering that the capacitor C_{dc} is charged with the voltage V_{dc}. When S_1 is conducting, S_2 holds off the voltage V_{dc}, and when S_2 is conducting, S_1 holds off the voltage V_{dc}. Hence, if the voltage V_{dc} is greater than a couple of kV, a solid-state switch comprising series-stacked semiconductors is mandatory for implementing switches S_1 and S_2.

The switching frequency of S_1 and S_2 and the pulse *on* time depend on the energy stored in the C_{dc} capacitor, on the load consumption, and on the power dissipated in the switches during commutation.

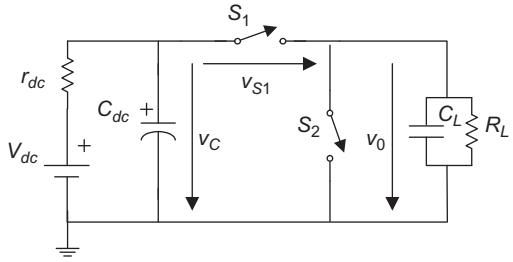


FIG. 18.54 Proposed pulsed power HV topology for describing the operation of the series switch (buck type) of Fig. 18.53.

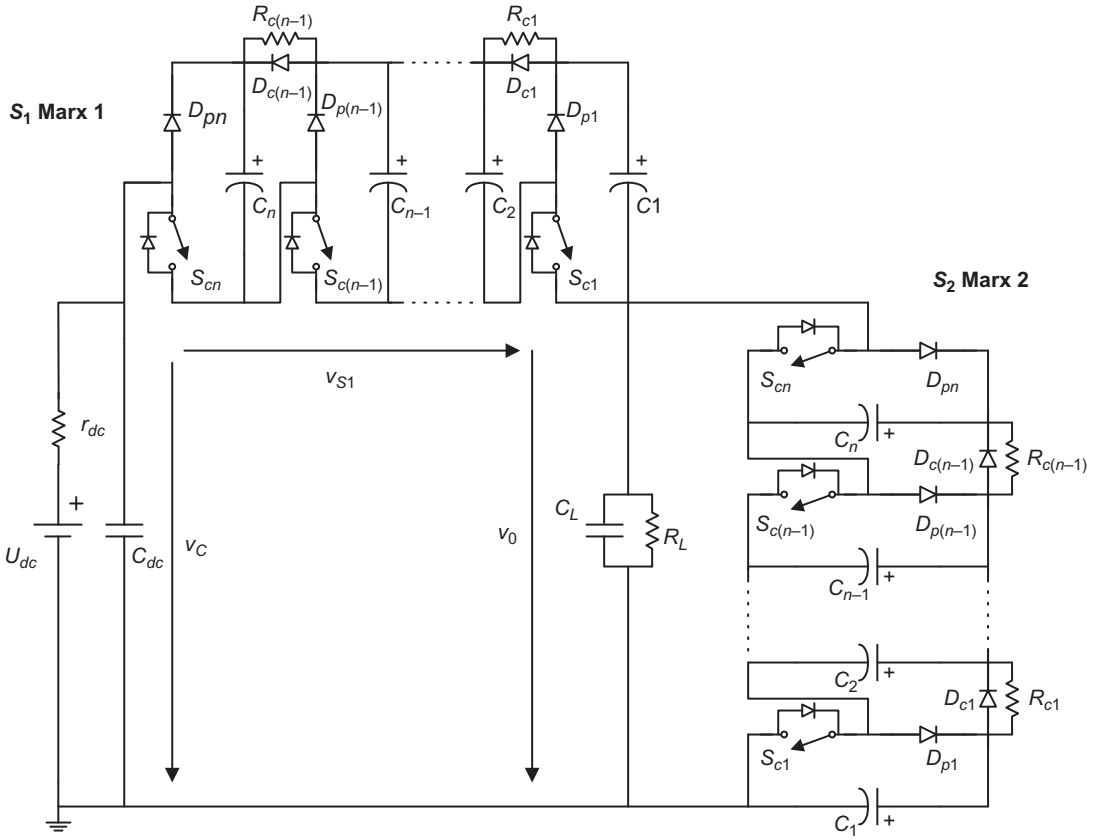


FIG. 18.55 Proposed pulsed power topology for testing the new series switches.

The proposed PP topology in Fig. 18.54 implemented with the series switch of Fig. 18.53 as series switch S_1 (Marx 1) and S_2 (Marx 2) is shown in Fig. 18.55.

The operation of Fig. 18.55 circuit can be understood considering the concept presented in Fig. 18.53 and the voltage waveforms presented in Fig. 18.57. For the first operating mode, during time t_{on}, the S_{ci} switches in Marx 1 are *on*, the C_i capacitors in Marx 1 are in parallel, and the S_{ci} switches in Marx 2 are *off*, as shown in Fig. 18.56A. The capacitor C_{dc} voltage, v_c, is applied into the load, v_0, and the C_i capacitors in Marx 2 are stacked in series, through the D_{pi} diodes, distributing the voltage across the S_{ci} switches, in parallel with the load.

Subsequently, in the second operating mode, during time $T-t_{on}$, the S_{ci} switches in Marx 1 are *off* and the S_{ci} switches in Marx 2 are *on*, and the load is discharged to zero, as shown in Fig. 18.56B. The v_c voltage appears between the Marx 1 terminals as shown in Fig. 18.57D, where this voltage is sustained by the C_i capacitors in series through the D_{pi} diodes, distributing the voltage across the S_{ci} switches.

Unlike in a typical Marx generator, the C_i capacitors in both Marx 1 and Marx 2 of Fig. 18.55 can suffer from voltage imbalance problems due to the fact that the C_i capacitors are charged in series: (i) in Marx 1 during period $T-t_{on}$ when the load is short-circuited and the voltage v_C appears between the Marx 1 terminals, $v_{S1,}$ and (ii) in Marx 2 during period t_{on} when the voltage is applied to the load and the voltage V_C appears between the Marx 2 terminals.

Two main causes contribute to this voltage imbalance: (i) The C_i capacitance values are not equal, and (ii) the C_i capacitors placed near the V_{dc} power supply are charged with a higher voltage due to the voltage droop in the semiconductors in each stage. Considering the last, the D_{ci} diodes do not conduct, and R_{ci} are used in parallel to uniformly distribute the voltage between the C_i capacitors during (i) t_{on} in the Marx 1 switch and (ii) $T-t_{on}$ in Marx 2 switch. Alternatively, extra switches can be placed in antiparallel with diodes D_{ci}.

18.4.6 Solid-State Marx-Based Bipolar Generators

The Marx generator concept was extended in Ref. [60] to allow the generation of positive and/or negative pulses. This bipolar Marx generator is shown in Fig. 18.58, based in n modules with four controlled semiconductors T_{fi}, T_{ei}, T_{ai}, T_{bi}, ($i \in \{1,2,\ldots,n\}$), two diodes D_{hi}, D_{gi}, and energy storage capacitor C_i.

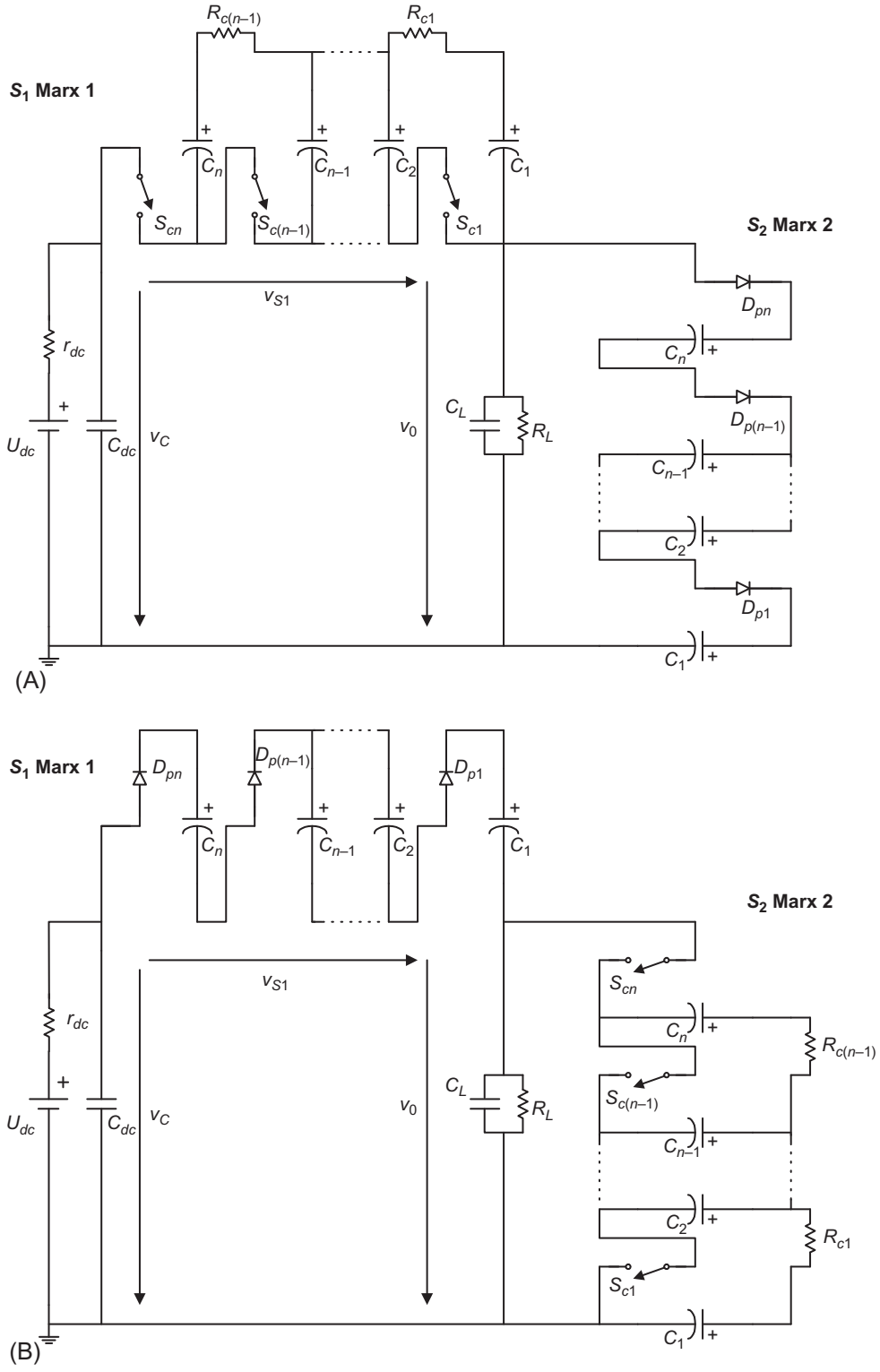


FIG. 18.56 Operating modes for the Fig. 18.55 circuit: (A) voltage applied to the load and (B) load discharge.

During the charging period, the dc power supply V_{dc} charges the C_i capacitors in parallel from the power supply and C_0 capacitor by turning ON switches T_{dc}, D_{dc}, T_{fi}, and T_{ei}, through diodes D_{hi} and D_{gi} (Fig. 18.59). The *on*-state of T_{ei} and D_{gi} switches, during this period, may guarantee a near-zero value to the load voltage, V_0, provided the charging current is bigger than the load current.

To obtain positive pulses, only switches T_{fi} and T_{ai} are driven *on* (Fig. 18.60). For negative pulses, only switches T_{bi} and T_{ei} are driven *on* (Fig. 18.61).

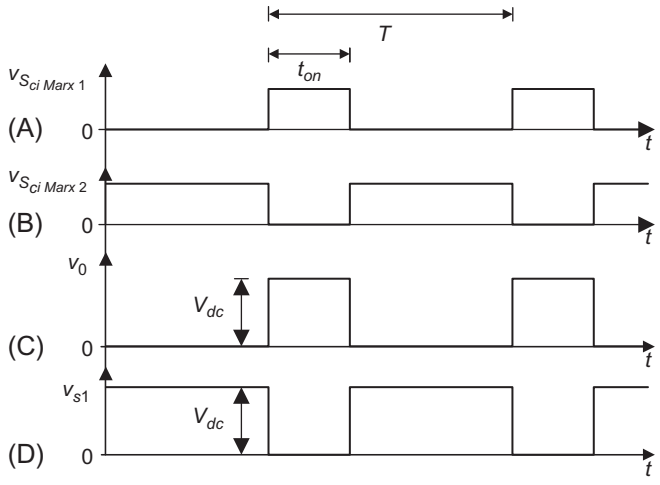


FIG. 18.57 Theoretical waveforms for Fig. 18.55 circuit operation: (A) Marx 1 S_{ci} drive signal, (B) Marx 2 S_{ci} drive signal, (C) load voltage v_0, and (D) Marx 1 voltage V_{s1}.

18.4.7 Solid-State Marx-Based Multilevel Bipolar Generators

Some of the previous presented Marx modulators may be used to generate staircase like voltage waveforms with multiple voltage levels, which can be useful to reduce electromagnetic interference since the rate of change of the pulse voltage is reduced regarding the two level voltage pulse.

The solid-state Marx-based high-voltage switch of Fig. 18.55 can be enhanced by adding an antiparallel transistor to diodes D_{pi}, to obtain one of the $2(n-1)$ modules of the multilevel bipolar generator in Fig. 18.62A, able to output n voltage levels [61]. The extra transistor and the $D_{k\text{-}1,k}$ module interconnecting diode enable a better control of the charge/discharge of the storage capacitors C_k, since they can be connected in series with the capacitors in other modules to charge/discharge, or in parallel with some other capacitors to balance their voltages Fig. 18.62B, provided diode $D_{k\text{-}1,k}$ is forward-biased [61].

The C_k capacitors are charged in series (being $U_{Ck} \approx U_{dc}/(n-1)$).

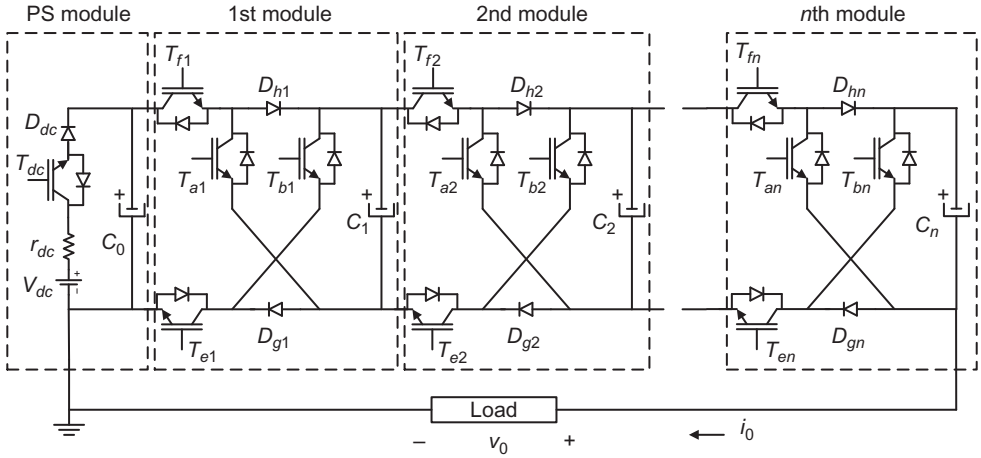


FIG. 18.58 Solid-state Marx-type bipolar generator topology, with n modules of four switches, enabling unipolar or bipolar pulse generation [60].

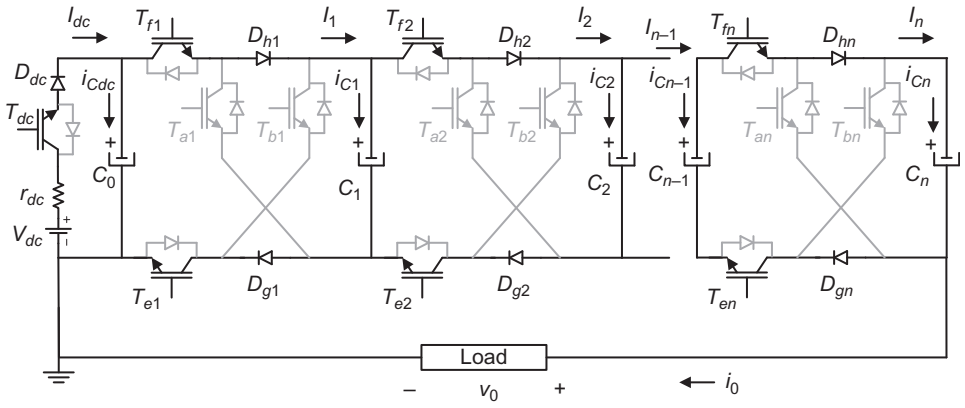


FIG. 18.59 Charging mode in the solid-state Marx-type bipolar generator [60].

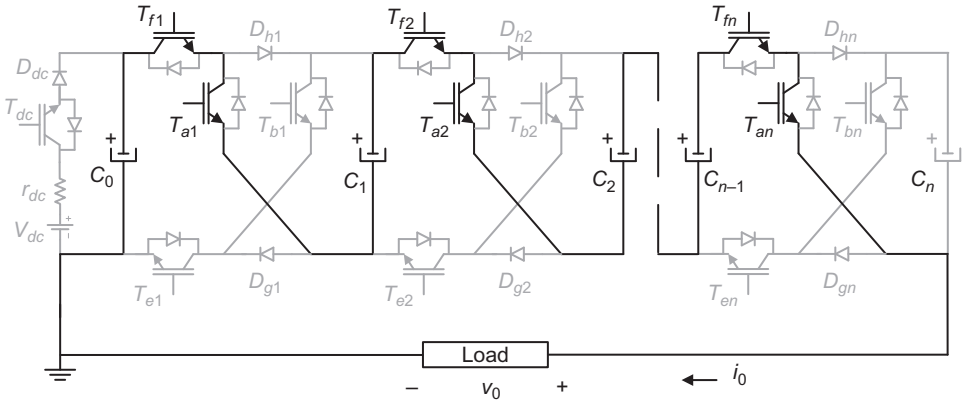


FIG. 18.60 Positive pulse operation in the solid-state Marx-type bipolar generator [60].

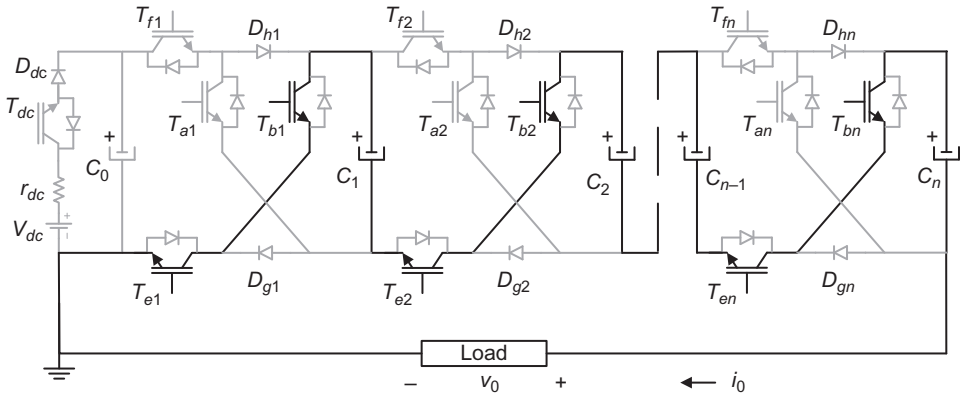


FIG. 18.61 Negative pulse generation in the solid-state Marx-type bipolar topology [60].

Considering a boolean switching function γ_k, the voltage U_k of each module is written as

$$U_k = \gamma_k U_{Ck}, \text{ being } \gamma_k = \begin{cases} 0 \text{ if } S_k, S_{k-1,k} \text{ are ON } \wedge \ S_{ka} \text{ is OFF} \\ 1 \text{ if } S_k, S_{k-1,k} \text{ are OFF } \wedge \ S_{ka} \text{ is ON} \end{cases} \tag{18.108}$$

Neglecting parasitic voltage drops, the load pulse voltage U_{Load} is

$$U_{Load} = U_{CA} - \sum_{k=1}^{n-1} \gamma_k U_{Ck} = -U_{CB} + \sum_{k=n}^{2(n-1)} \gamma_k U_{Ck} \tag{18.109}$$

Supposing $U_{CA} = U_{CB} = U_{dc}/2$, summing and subtracting the two previous equations, it can be obtained:

$$\begin{aligned} U_{Load} &= \frac{1}{2}\left(\sum_{k=n}^{2(n-1)} \gamma_k U_{Ck} - \sum_{k=1}^{n-1} \gamma_k U_{Ck} \right) \\ U_{dc} &= \sum_{k=n}^{2(n-1)} \gamma_k U_{Ck} + \sum_{k=1}^{n-1} \gamma_k U_{Ck} = \sum_{k=1}^{2(n-1)} \gamma_k U_{Ck} \end{aligned} \tag{18.110}$$

To obtain the maximum output voltage $U_{Loadmax} = U_{dc}/2$, it must be $\sum_{k=1}^{n-1} \gamma_k U_{Ck} = 0$, which from the second equation of (18.110) means $\sum_{k=n}^{2(n-1)} \gamma_k U_{Ck} = U_{dc}$. Supposing balanced capacitor voltages, then, each capacitor voltage is $U_{Ck} = U_{dc}/(n-1)$. To generate the minimum voltage, $U_{Loadmin} = -U_{dc}/2$, and then, $\sum_{k=n}^{2(n-1)} \gamma_k U_{Ck} = 0$, being $U_{dc} = \sum_{k=1}^{n-1} \gamma_k U_{Ck}$. These relationships show that each generator half arm must hold off the high-voltage U_{dc}. From $U_{dc} = \sum_{k=1}^{n-1} \gamma_k \frac{U_{dc}}{n-1} \Rightarrow \sum_{k=1}^{n-1} \gamma_k = n-1$, which must be used to define the γ_k values needed for each level n. This means that half of the total $2(n-1)$ modules must have $\gamma_k = 1$, while the remaining half must have $\gamma_k = 0$. The γ_k values can create redundant states that must be used to balance the C_k capacitor voltages [61].

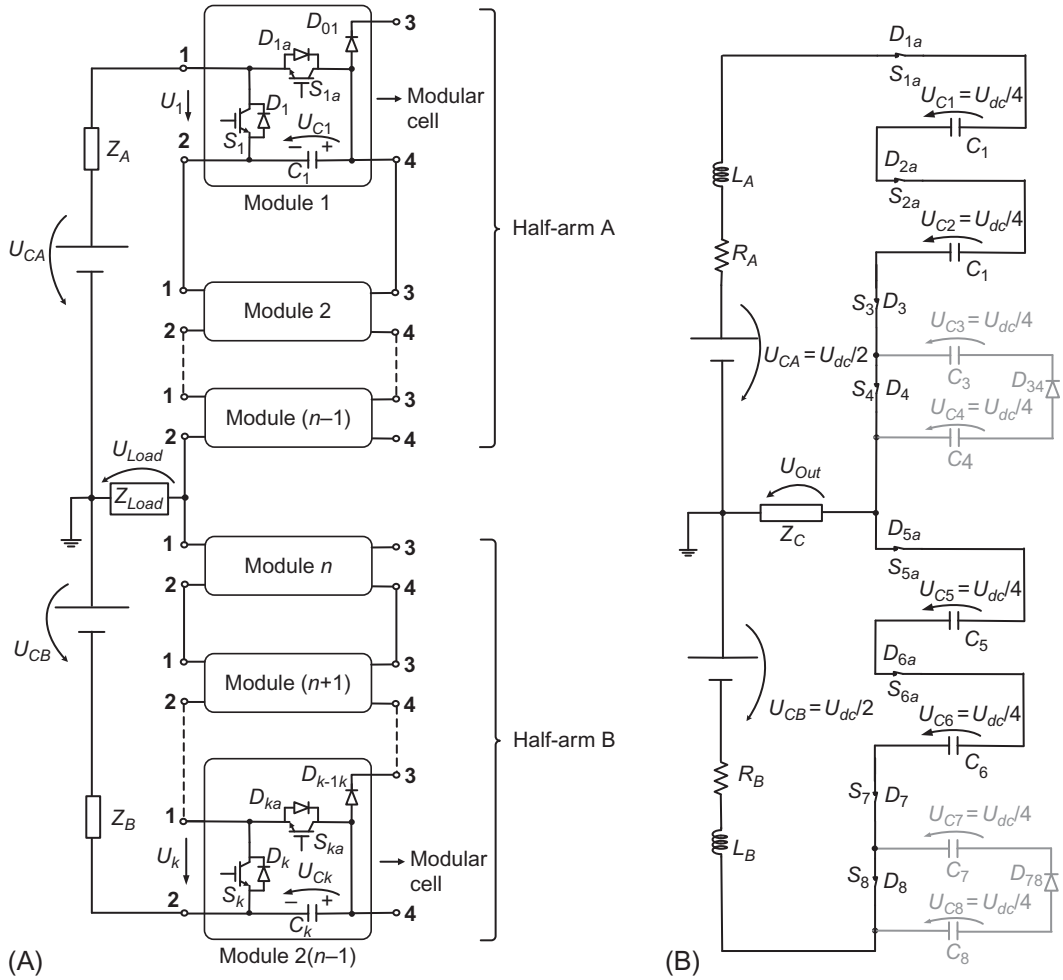


FIG. 18.62 (A) Solid-state Marx-based multilevel bipolar generator with n levels using $2(n-1)$ modules and (B) five-level generator with level 0 V, $U_{Out}=0$ V, showing one possibility of series and parallel connection of energy storage capacitors.

Fig. 18.63 shows the simulated output voltage of a seven levels (500 V each) 12 modules bipolar generator, including the zero voltage level.

18.5 Power Electronics in Capacitor Charging Applications

18.5.1 Introduction

Conventional dc power supplies operate at a given dc output voltage into a constant or near-constant load. However, pulse loads such as lasers, flashlamps, rail guns, and radar require short but intense bursts of energy. Typically, this energy is stored in a capacitor and then released into the load. The rate at which the capacitor is charged and discharged is called the repetition rate, T, and may vary from 0.01 Hz for large capacitor banks to a few kHz for certain lasers. Recharging the capacitor voltage to a specified voltage is tasked to a capacitor charging power supply (CCPS). The role of power electronics devices, topologies, and charging strategies for capacitor charging applications is presented in this chapter.

Fig. 18.64 shows the voltage across the energy storage capacitor connected to the output of a CCPS. This figure shows that the CCPS has three modes of operation. The first mode is the charging mode in which the capacitor is charged from an initial voltage of zero to a specified final voltage. The duration of the charging mode is determined by the capacitance of the energy storage capacitor and the rate at which the CCPS delivers energy. The next mode of operation is the refresh mode, which can be considered a "standby mode," where the stored energy is simply maintained. When the output voltage drops below a predetermined value, the CCPS should turn-on and deliver the energy necessary to compensate for capacitor leakage. Since energy is lost during the refresh mode, the duration of the refresh mode should be as brief as possible. Issues that lead to nonzero refresh times include safety margins for worst-case charging and discharging mode times and SOA requirements

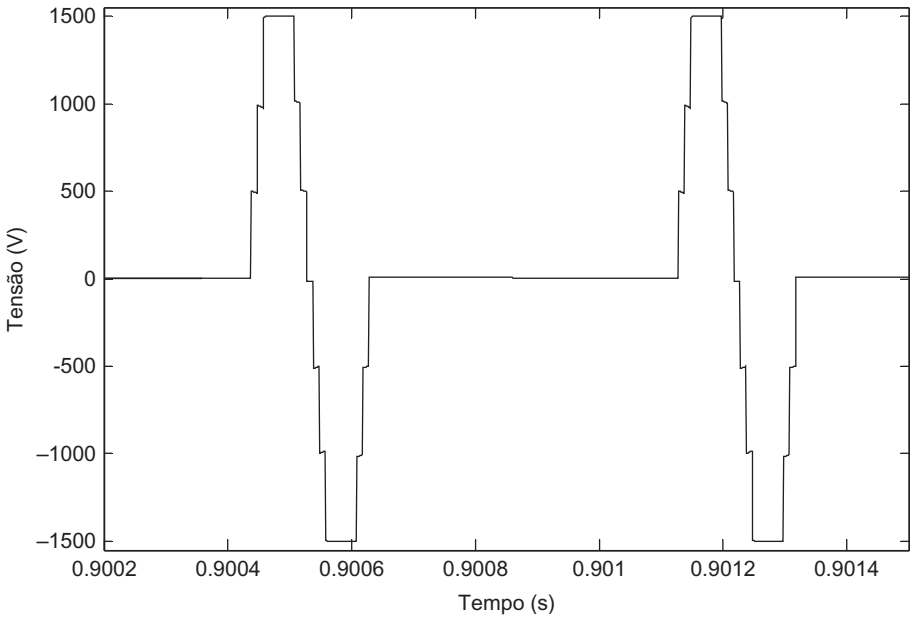


FIG. 18.63 Seven-level bipolar pulse obtained using the Marx-based multilevel bipolar generator (500 V/div and 200 μs/div).

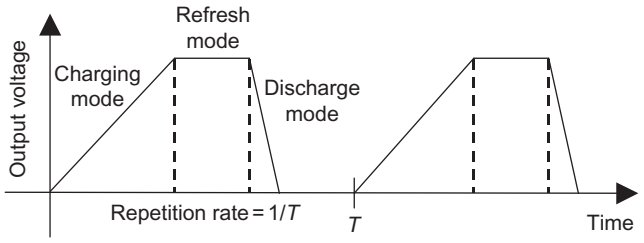


FIG. 18.64 Three modes of operation of a capacitor charging power supply.

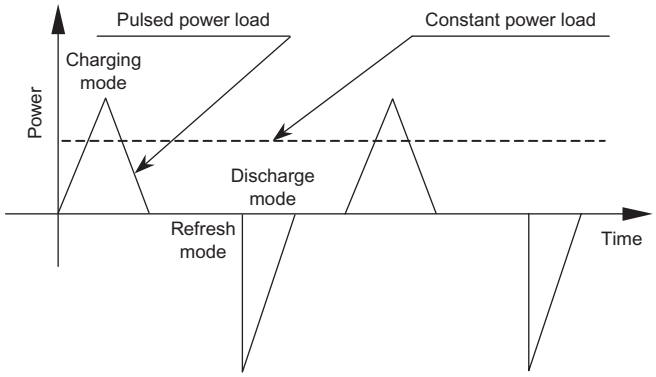


FIG. 18.65 Power requirements for pulsed power and constant power loads.

of switching devices. The final mode of operation is the discharge mode in which the load is actively discharging the capacitor. The CCPS does not supply any energy to the load in this mode. The amount of time the CCPS remains in this mode is determined by how quickly the load can discharge the capacitor.

The instantaneous output power for a CCPS varies over a wide range in comparison to a conventional dc power supply that supplies a near-constant power to its load. This is shown in Fig. 18.65; the output power for the PP load is drawn as linear for illustration purposes only. The charging mode is characterized by high peak power. At the beginning of this mode, the output power is zero (i.e., there is no voltage present but current is flowing). Thus, the load capacitor is equivalent to a short-circuit. In addition, at the end of the charging mode, the output power is again zero (i.e., there is an output voltage present but no current is flowing). Now, the load capacitor is equivalent to an open-circuit. The refresh mode is typically a low-power mode because the current required to compensate for capacitor leakage is small. The CCPS does not supply any power during the discharge mode when the energy storage capacitor is being discharged by the pulsed load.

The average output power for a CCPS depends on the discharge mode energy and the repetition rate of the load. It is maximum when the energy storage capacitor is discharged at the end of the charging mode (large voltage and current), which corresponds to operation without a refresh mode. Because the CCPS power is not constant, the rating of a CCPS is often given in kJ/s instead of kW. The kJ/s rating can be written as

$$\text{kJ/s} = \frac{W_{LOAD}}{T}$$

where W_{LOAD} is the energy delivered to the load per charging cycle and T is the repetition rate. In the optimum case with no refresh and instantaneous discharge, the kJ/s rating is limited to

how fast a particular capacitor can be charged by its specified voltage.

18.5.2 High-Voltage dc Power Supply With Charging Resistor

In this technique, the energy storage capacitor is charged by a high-voltage dc power supply through a charging resistor as shown in Fig. 18.66. The charging mode ends when the capacitor voltage equals the output voltage of the power supply. The capacitor is continually refreshed by the power supply. During the discharge mode, the charging resistor isolates the power supply from the pulse load. The advantages of this technique are its simplicity, reliability, and low cost.

The major disadvantage of this technique is its poor efficiency. In the charging mode, the energy dissipated in the charging resistor is equal to the energy stored in the capacitor in the ideal case; therefore, the maximum efficiency is 50%. As a result, this technique is utilized only in applications where the charge rate is low, that is, 200 J/s. Another disadvantage of this technique is related to the charging time, which is determined by the RC time constant. Some laser applications require that the output voltage be within 0.1% of a target voltage. For this technique, more than five time constants are required for the capacitor voltage to meet this voltage specification.

18.5.3 Resonance-Charging

The basic resonance-charging technique is shown in Fig. 18.67. An ac input voltage is stepped up with a transformer, rectified, and filtered with capacitor C_2 to produce a high dc voltage V_0. In this circuit, C_2 is much greater than C_1. Thyristor T_1 is gated and current flows through the inductor and diode D_1 is transferring energy from C_2 to C_1. The voltage $v(t)$ and current $i(t)$ are described by the following equations assuming that $C_2 \gg C_1$. The charge time, t_c, for this circuit can be calculated by finding the time at which the current, described by Eq. (18.112), reaches zero and is given below. The voltage $v(t)$ has a value of $2\,V_0$ at the end of the charging mode:

$$v(t) = V_0(1 - \cos\omega_0 t) \tag{18.111}$$

$$i(t) = V_0\sqrt{\frac{C_1}{L}}\sin\omega_0 t \tag{18.112}$$

$$\omega_0 = \frac{1}{\sqrt{LC_1}} \tag{18.113}$$

$$t_c = \pi\sqrt{LC_1} = \frac{\pi}{\omega_0} \tag{18.114}$$

Even though this technique is simple and efficient, it is not without its limitations. A high-voltage capacitor with a large capacitance value is needed for C_2, which increases the cost. A single thyristor is shown in Fig. 18.67. Multiple thyristors connected in series or a thyratron may be required depending on the voltage level. The repetition rate of the pulse load should be such that C_1 is fully charged and $i(t)$ has reached zero before the load discharges to prevent latch up of T_1. It is not possible for this circuit to operate in the refresh mode because of the switch characteristics; therefore, $v(t)$ will drift due to capacitor leakage. The charge time is a function of the circuit parameters and will drift as they change with temperature or due to aging.

Because all of the energy stored in C_1 is transmitted from C_2 in a single pulse, it can be difficult to achieve precise voltage regulation with the resonance-charging technique. However, regulation can be improved with the addition of a dequeing circuit as shown in Fig. 18.68. The voltage $v(t)$ is monitored with a sensing network. Before $v(t)$ reaches the desired level, thyristor T_2 is fired, which terminates the charging mode. The remaining energy stored in the inductor is dissipated in R. The addition of the dequeing circuit reduces the circuit efficiency and increases the circuit complexity and cost but still does not enable a refresh mode to compensate for capacitor leakage.

Boost charging, a variation on the resonance-charging technique, is shown in Fig. 18.69 [62]. An extra switch is added to

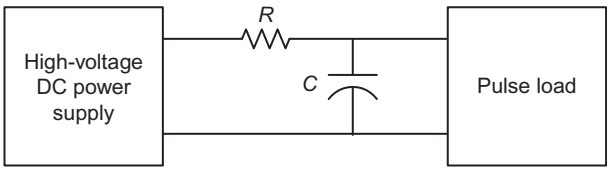


FIG. 18.66 High-voltage dc power supply and charging resistor.

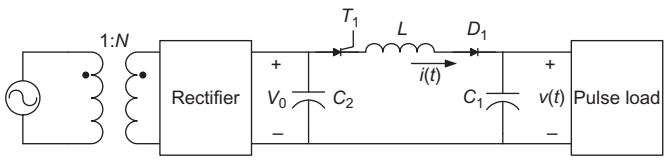


FIG. 18.67 Resonance-charging.

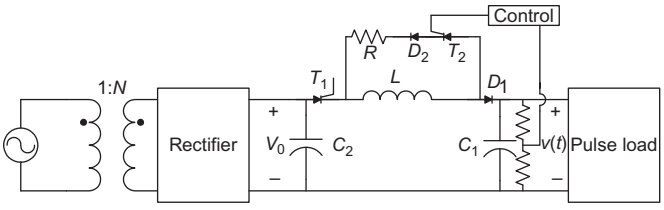


FIG. 18.68 Resonance-charging with dequeing.

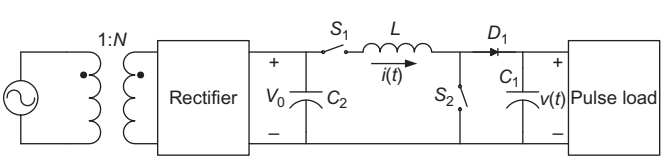


FIG. 18.69 Boost charging.

the circuit of Fig. 18.67, allowing energy to be stored in both C_2 and L. This can be modeled as an increase in the voltage gain of the CCPS. With switches S_1 and S_2 closed, the current $i(t)$ is given by

$$i(t) = \frac{V_0}{L}t \tag{18.115}$$

When $t = t_{on}$, S_2 is opened, and the current is now described by

$$i(t) = I_0 \cos\omega_0 t + V_0\sqrt{\frac{C_1}{L}}\sin\omega_0 t \tag{18.116}$$

where

$$I_0 = \frac{V_0}{L}t_{on} \tag{18.117}$$

is the inductor current initial value at t_{on}. The voltage $v(t)$ is then

$$v(t) = I_0\sqrt{\frac{L}{C_1}}\sin\omega_0 t + V_0(1 - \cos\omega_0 t) \tag{18.118}$$

The time required for the current to reach zero and for the voltage $v(t)$ to reach its peak value can be calculated from

$$\tan(\omega_0 t_c) = -\frac{I_0\sqrt{\frac{L}{C_1}}}{V_0} = -\omega_0 t_{on} \tag{18.119}$$

This is also the charge time, t_c, or the length of the charging mode. Note from Eq. (18.119) that the charge time depends on t_{on}, which is the on-time of switch S_2. In addition, the peak capacitor voltage is a function of t_{on}. The peak capacitor voltage is limited to $2V_0$ without S_2; voltage gains as high as 20 are possible with the addition of S_2 [62].

The switching elements in Figs. 18.67 and 18.68 are realized with thyristors. Simple switches are shown for the boost charging technique in Fig. 18.69. Switch S_1 could be implemented with a thyristor. The boost capability provided by switch S_2 is best realized with a gate-controlled semiconductor device such as a GTO or an IGBT.

18.5.4 Switching Converters

The poor efficiency when charging a capacitor through a resistor from a high-voltage power supply limits its application to low charging rates. In the resonance-charging concepts, the energy is transferred to the load capacitor in a single pulse, and it is not possible to compensate for capacitor leakage. Energy storage capacitors may be charged utilizing the same power electronic technology that has been applied in switching converters for constant power loads. Instead of charging the energy storage capacitor with a single pulse, switching converters can charge the capacitor with a series of pulses or pulse train. The peak current is reduced when charging with a series of pulses, thus improving the efficiency of the charging process. In addition, soft-switching techniques may be used in the switching converter to increase the efficiency. The regulation of the output voltage is also improved with the pulse train because the energy is passed to the energy storage capacitor as small packets. Common control techniques such as pulse width modulation can be used to control the size of the energy packet. This capability to control the size of the energy packet permits the CCPS to operate in the refresh mode and compensate for capacitor leakage. As a result, the CCPS may operate over a broad range of load repetition rates and still maintain tight output voltage regulation during refresh mode. During the refresh mode, energy lost due to capacitor leakage may be replaced in a burst fashion [63] or in a continuous fashion similar to trickle charging a battery [64].

In the switching converter, semiconductor switches may be operated on the lower side of the transformer permitting the use of MOSFETs or IGBTs in the CCPS. Because the CCPS begins the charging mode with a short-circuit across its output, the switching converter must be capable of operating under this severe load condition. This may require the implementation of a current limiting scheme in the converter control circuit.

One switching converter as shown in Fig. 18.70 consists of a resonant converter. Note that the MOSFETs and resonant components L_r and C_r are connected on the low-voltage side of the transformer. Only the rectifier diodes and energy storage capacitor must have high-voltage ratings. When the output rectifier is conducting, the energy storage capacitor C_1 is connected in series with the resonant capacitor C_r. For a transformer turn ratio of $1/N$, reflecting C_1 through the transformer yields a capacitance of N^2C_1. Since N is typically large, this reflected capacitance is much larger than C_r, thus the resonant frequency, which is defined in Eq. (18.120), is not affected by C_1. For high-voltage, high-frequency operation, the leakage inductance of the transformer may be utilized as L_r. Thus, the resonant frequency can be expressed as

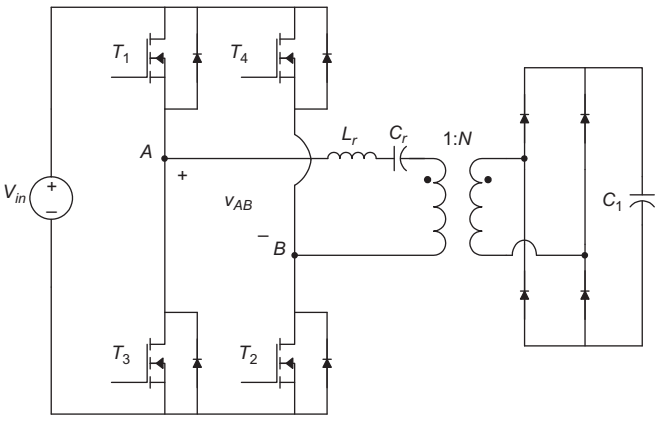


FIG. 18.70 Series resonant converter.

$$\omega_r = \frac{1}{\sqrt{L_r((NC_rC_1)/(C_r + NC_1))}} \tag{18.120}$$

One characteristic of this converter, which makes it attractive for capacitor charging, is the ability to operate under the short-circuit conditions present at the beginning of the charging mode. The voltage across C_1 is zero at the beginning of this mode. The current in the switches is limited by the input voltage and impedance Z_0 as is defined in Eq. (18.121).

$$Z_0 = \sqrt{\frac{L_r}{C_r}} \tag{18.121}$$

Another method for current limiting is to vary the ratio of f_s, the switching frequency of the MOSFETs, and the resonant frequency, f_r, which is $\omega_r/2\pi$. This effectively controls the flow of energy from the source to C_1. The ratio f_s/f_r may be set to a low value at the beginning of the charging mode and increased toward unity as the voltage across C_1 increases. This limits the current when the voltage across C_1 is low and allows increased energy transfer as the voltage approaches the target voltage. The disadvantage of this approach is that variable frequency operation complicates device and component selection and degrades EMI/EMC performance of the CCPS.

The flyback converter, shown in Fig. 18.71, also may be utilized for capacitor charging applications [65,66]. When the MOSFET is turned on, current increases in the primary winding, storing energy in the magnetic field. When it reaches a specified level, the MOSFET is turned off and the energy is transferred from the magnetic field to C_1. This energy transfer is terminated when the MOSFET is turned on again.

In cases where precise output regulation is not required and the packet energy is low, the diode in Fig. 18.71 can be replaced with a Zener diode with a Zener voltage of

$$V_Z = nV_{in} + V_{O,nom}$$

where $V_{O,nom}$ is the nominal value of V_O [67]. Once $V_{O,nom}$ is reached, the next energy packet will force the diode into a brief

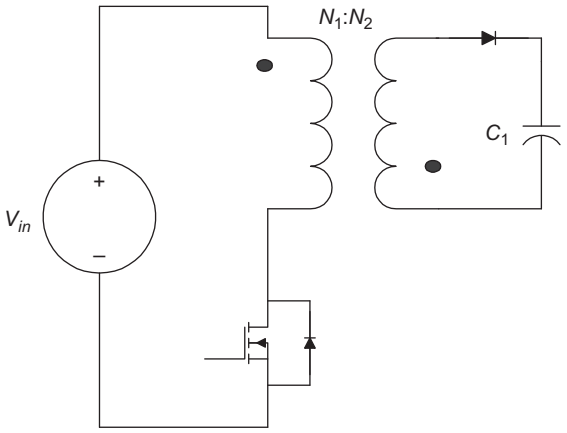


FIG. 18.71 Flyback converter.

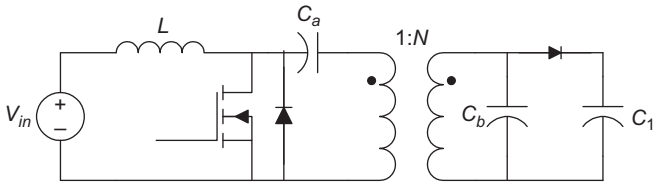


FIG. 18.72 Ward converter.

period of breakdown with the excess energy partially recycled to the input circuit. If the packet energy is small enough, the breakdown is not destructive and V_O is limited to

$$V_O = V_{O,nom} + V_{O,\Omega}$$

where $V_{O,\Omega}$ is the small excess voltage caused by the last energy packet.

Sokal and Redl [68] have investigated different control schemes for charging capacitors using the flyback converter. Their recommendation is to charge C_1 with current pulses that are nearly flat-topped. This strategy results in higher average current for a given peak current. The capacitor is charged faster because the charge delivered to it during a pulse is directly proportional to the average current. This desired pulse shape is achieved by turning on the MOSFET to terminate the transfer of energy to C_1 soon after the MOSFET is turned off, which increases the switching frequency. When the primary current rises to a preset minimum level, the MOSFET is again turned off. This switching strategy is essentially hysteretic current mode control, in which the switch current is limited between two preset bounds.

Another converter for capacitor charging applications is the Ward converter [69–71] shown in Fig. 18.72. When the MOSFET is turned on, energy is stored in the inductor, and capacitor C_a transfers energy into the energy storage capacitor C_1 and capacitor C_b. The energy stored in the inductor is transferred to C_a when the MOSFET is turned off. The leakage inductance of the transformer and C_a resonate producing a sinusoidal current that flows in the primary winding of the transformer and the MOSFET. When the primary current reaches zero and starts negative, the diode turns on, which allows the MOSFET to be turned off efficiently at zero-current.

In some converter operating conditions, the voltage across C_a is very small because most of the energy has been transferred from C_a to C_1. The energy stored in C_a may be too small to ensure zero-current turnoff of the MOSFET. In this case, the energy stored in C_b helps to ensure that the amplitude of the current is large enough for zero-current turnoff of this device.

18.6 Conclusions and Future Trends

This chapter reviewed some of the most typical semiconductors and topologies used for generating repetitive unipolar and bipolar high-voltage pulses based on semiconductor devices

for various load conditions. These topologies have in common the techniques for limiting the high-voltage stress onto the power semiconductor switches, still relatively low-voltage devices, considering the tens of kV needed for pulse power applications. High-voltage techniques spread from the series (and parallel) stacks of semiconductors switches to generalized cascodes, passing through the modified dc-dc isolated converters for pulse generation and their cascade association, to the Marx-type solid-state generators topologies and Marx-derived bipolar generators.

With semiconductor-based generators, pulse power applications have expanded into many new fields such as material modification, environment protection, and biological and medical developments. The presented topologies can bring a completely new extent of capability in repetition rate, efficiency, lifetime, compactness, and portability.

In addition to the methods to generate high-voltage pulse, the performances of the semiconductor switches determine the performance of the pulse power generators. In this way, power semiconductor devices have made significant progress in both power capability and operation speed. Various semiconductor switching units have become commercially available and have been used in various pulse power applications. The most typical devices such as SOS diodes, GTOs, IGBTs MOSFETs, SIThs, and the emerging devices based on SiC or GaN technology, such as SiC MOSFETs, JFETs, cascode JFETs, IGBTs, and GaN E-HEMTs, were described. As the performance of SiC devices continues to improve, it is expected they will replace the existing switching Si devices in high-voltage applications, reducing the number of needed stages.

State-of-the-art HV pulse generators must use several stages to obtain the desired final high-voltage pulse: the first stage can use SCRs and start at 1–2 kV, and then, intermediate full-bridge resonant stage using IGBTs or full-bridge associations can boost this voltage to 4–10 kV, which is applied to HV high-frequency or pulse transformers to obtain 50–100 kV in the secondary. Diode polyphase rectifiers in the transformer secondary windings or saturated pulse transformers can boost the voltage roughly to 300 kV. If needed, a final stage using a SOS or SAS diode can boost the voltage up to 1 MV. Alternatively, other solutions such as solid-state Marx generators are being used, each Marx module operating at 2–10 kV (using SiC semiconductors or series stacks if needed). The required number of Marx modules should be minimized and arranged in shielded groups, the groups being connected to obtain the full HV generator. Droop voltage control and balancing may be necessary to design a practical HV pulse generator. Power generators based in existing power electronics converters are also used to charge capacitors for high-voltage pulse generators.

The future of solid-state pulse power is linked to the capability of making semiconductor-based high-voltage generators with better characteristics in compactness, weight, cost, efficiency, modularity, and portability, very important to deal with future applications near the consumer.

Acknowledgments

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References

[1] M. Kristiansen, Pulsed power applications, in: Proceedings of IEEE International Pulsed Power Conference, 1993, pp. 6–10.
[2] S. Levy, et al., Commercial applications for modulators and pulse power technology, in: Proceedings of IEEE Power Modulator Symposium, 1992, pp. 8–14.
[3] E. Schamiloglu, Scanning the technology, Proc. IEEE 92 (7) (2004) 1014–1020.
[4] W. Jiang, et al., Compact solid-state switched pulsed power and its applications, Proc. IEEE 92 (7) (2004) 1180–1196.
[5] H. Akiyama, S. Sakai, T. Sakugawa, T. Namihira, Environmental applications of repetitive pulsed power, IEEE Trans. Dielectr. Electr. Insul. 14 (4) (2007) 825–833.
[6] K.H. Schoenbach, et al., Ultrashort electrical pulses open a new gateway into biological cells, Proc. IEEE 92 (7) (2004) 1122–1137.
[7] J. Raso-Pueyo, V. Heinz, Pulsed Electric Fields Technology for the Food Industry—Fundamentals and Applications, first ed., Springer-Verlag, USA, 2006.
[8] G.S. Daehn, ASM Handbook, Volume 14B, Metalworking: Sheet Forming, ASM International, Novelty, OH, USA, 2006. ISBN: 978-0-87170-710-9.
[9] E.L. Neau, Environmental and industrial applications of pulsed power systems, IEEE Trans. Plasma Sci. 22 (1) (1994) 2–10.
[10] J. Fernando Silva, Electrónica Industrial: Semicondutores e Conversores de Potência, série Manuais Universitários, Fundação Calouste Gulbenkian, Lisboa, ISBN 978-972-31-1499-7, 2013. 740 pp.
[11] N. Mohan, T. Undeland, W. Robbins, Power Electronics: Converters, Applications, and Design, third ed., John Wiley, New York, 2002.
[12] J. Mankowski, M. Kristiansen, A review of short pulse generator technology, IEEE Trans. Plasma Sci. 2 (1) (2000) 102–108.
[13] M.H. Rashid (Ed.), Power Electronics Handbook, second ed., Academic Press, Elsevier, USA, 2007. 1172 pp., ISBN 13:978-0-12-088479-7, ISBN 10:0-12-088479-8.
[14] R.J. Baker, B.P. Johnson, Applying the Marx bank circuit configuration to power MOSFETS, Electron. Lett. 29 (1) (1993) 56–57.
[15] R.J. Baker, S.T. Ward, Designing nanosecond high voltage pulse generators using power MOSFETs, Electron. Lett. 30 (20) (1994) 1634–1635.
[16] B. Jayant Baliga, Modern Power Devices, Wiley-Interscience, USA, 1987.
[17] C. Burkhart, et al., ILC Marx modulator development program status, in: Presented in Linear Accelerator Conference, 29 Victoria, British Columbia, Canada, September 2008, 2008.
[18] E.G. Cook, Review of solid-state modulators, in: Presented at the XX International Linac Conference, Monterey, CA, 21–25 August 2000, 2000.
[19] A. Welleman, J. Waldmeyer, E. Ramezani, Solid state switches for pulse power modulators, in: Proceedings of Linear Particle Accelerator, 2002, pp. 707–709.

[20] G. Leyh, Prototype development progress toward a 500 kV solid state Marx modulator, in: Proceedings of IEEE Power Electronics Specialists Conference, 2004, pp. 831–834.
[21] J. Kim, B. Min, S. Shenderey, G. Rim, High voltage marx generator implementation using IGBT stacks, IEEE Trans. Dielectr. Electr. Insul. 14 (4) (2007) 931–936.
[22] Y. Wu, K. Liu, J. Qiu, X. Liu, H. Xiao, Repetitive and high voltage Marx generator using solid-state devices, IEEE Trans. Dielectr. Electr. Insul. 14 (4) (2007) 937–940.
[23] J.F. Silva, S.F. Pinto, Advanced control of switching power converters, in: H. Rashid (Ed.), Power Electronics Handbook, third ed., Butterworth Heinemann, Elsevier, Chennai, 2011, pp. 1037–1114.
[24] M.A. Kempkes, J.A. Casey, M.P.J. Gaudreau, T.A. Hawkey, I. S. Roth, Solid-state modulators for commercial pulsed power systems, in: Proceedings of IEEE International Power Modulator Symposium, and High-Voltage Work, 2002, pp. 689–693.
[25] J. Pelletier, A. Anders, Plasma-based ion implantation and deposition: a review of physics, technology and applications, IEEE Trans. Plasma Sci. 33 (6) (2005) 1944–1959.
[26] E.H.W.M. Smulders, B.E.J.M. Van Heesch, S.S.V.B. Van Paasen, Pulsed power corona discharges for air pollution control, IEEE Trans. Plasma Sci. 26 (5) (1998) 1476–1484.
[27] A. Meriched, M. Féliachi, H. Mohellebi, Electromagnetic forming of thin metal sheets, IEEE Trans. Magn. 36 (4) (2000) 1808–1811.
[28] L.M. Redondo, J. Fernando Silva, E. Margato, Analysis of a modular generator for high-voltage, high-frequency pulsed applications, using low voltage semiconductors (<1 kV) and series connected step-up (1: 10) transformers, Rev. Sci. Instrum. 78 (3) (2007).
[29] Jim Lux's web site, High-voltage, high voltage resistors, water resistance, 2003. http://home.earthlink.net/~jimlux/hv/rwater.htm. (Accessed 23 February 2017).
[30] J. Brutscher, A 100 kV 10A high voltage pulse generator for plasma immersion ion implantation, Rev. Sci. Instrum. 67 (7) (1996) 2621–2625.
[31] A. Anders, D.M. Goebel, Pulse technology, Handbook of Plasma Immersion Ion Implantation & Deposition, first ed., John Wiley & Sons, USA, 2000 (Chapter 8).
[32] C. Wang, Q.H. Zhang, EMI and its elimination in an integrated high voltage (12 kV) pulse generator, in: Proceedings of IEEE Industrial Electronics Society, 2000, pp. 1044–1049.
[33] L.M. Redondo, E. Margato, J. Fernando Silva, A new method to build a high-voltage pulse supply using only semiconductor switches for plasma-immersion ion implantation, Surf. Coat. Technol. 136 (2001) 51–54.
[34] X. Tian, X. Wang, B. Tang, P.K. Chu, P.K. Ko, Y.C. Cheng, Special modulator for high frequency, low-voltage plasma immersion ion implantation, Rev. Sci. Instrum. 70 (3) (1999) 1824–1828.
[35] L.M. Redondo, J.F. Silva, P. Tavares, E. Margato, All Silicon Marx-bank topology for high-voltage, high-frequency rectangular pulses, in: 2005 IEEE 36th Power Electronics Specialists Conference, 2005, pp. 1170–1174.
[36] F. Wang, A. Kuthi, C. Jiang, Q. Zhou, M. Gundersen, Flyback resonant charger for high repetition rate pseudospark pulse generator, in: Proceedings of Power Modulator Conference Symposium, 2004, pp. 85–88.
[37] M. Giesselman, T. Heeren, Rapid capacitor charger, in: Proceedings of Power Modulator Conference Symposium, 2002, pp. 146–149.
[38] R. Petr, D. Reilly, J. Freshman, N. Orozco, D. Pham, L. Ngo, J. Mangano, Solid-state pulsed power for driving a high-power dense plasma focus x-ray source, Rev. Sci. Instrum. 71 (3) (2000) 1360–1362.
[39] W. Jiang, et al., Development of repetitive pulsed power generators using power semiconductor devices, in: Proceedings of International Symposium on Power Semiconductor Devices and ICs, 2005, pp. 1167–1172.
[40] M.P.J. Gaudreau, T. Hawkey, J. Petry, M. Kempkes, A solid state pulsed power system for food processing, in: Proceedings of Pulsed Power Plasma Science, vol. 2, 2001, pp. 1174–1177.
[41] A. Welleman, W. Fleischmann, W. Kaesler, Solid state on-off switches using IGCT technology, in: Proceedings of Pulsed Power Conference, 2007, pp. 1025–1028.
[42] W. Jiang, Fast high voltage switching using stacked MOSFETs, IEEE Trans. Dielectr. Electr. Insul. 14 (4) (2007) 947–950.
[43] J. Kim, B. Min, S. Shenderey, G.-H. Rim, High voltage pulsed power supply using IGBT stacks, IEEE Trans. Dielectr. Electr. Insul. 14 (4) (2007) 921–926.
[44] B.W. Williams, Power electronics, in: B.W. Williams (Ed.), Series and Parallel Device Operation, Protection, and Interference, Palgrave Macmillan, USA, 2005 (Chapter 10).
[45] S. Gunturi, J. Assal, D. Schneider, S. Eicher, Innovative metal system for IGBT press pack modules, in: Proceedings of International Symposium on Power Semiconductor Devices and ICs, 2003, pp. 110–113.
[46] D.M. Goebel, Pulse technology, in: A. Anders (Ed.), Handbook of Plasma Immersion Ion Implantation & Deposition, first ed., John Wiley & Sons, USA, 2000 (Chapter 8).
[47] L.M. Redondo, J.F. Silva, E. Margato, Pulse shape improvement in core-type high-voltage pulse transformers with auxiliary windings, IEEE Trans. Magn. 43 (5) (2007) 1973–1982.
[48] M.H. Rashid, Power Electronics: Circuits, Devices and Applications, Prentice Hall, USA, 2003.
[49] C.S. Leu, G. Hua, F.C. Lee, C. Zhou, Analysis and design of a R-C-D clamp Forward converter, in: Proceedings of High Frequency Power Conversion Conference, 1992, pp. 198–208.
[50] L.M. Redondo, J. Fernando Silva, Flyback versus Forward switching power supply topologies for unipolar pulsed power applications, IEEE Trans. Plasma Sci. 37 (1) (2009) 171–178.
[51] J. Klein, M. Padberg, A modular low-cost, high-voltage pulse generator that is highly effective in terms of pulse energy and repetition frequency, Meas. Sci. Technol. 6 (5) (1995) 550–555.
[52] W. Smith, Transient Electronics—Pulsed Circuit Technology, Wiley, USA, 2002.
[53] L.M. Redondo, E. Margato, J.F. Silva, Rise time reduction in high-voltage pulse transformers using auxiliary windings, IEEE Trans. Power Electron. 17 (2) (2002) 196–206.
[54] Kostenko, L. Piotrovski, Electrical Machines, Rev ed., Central Books, Moscow, 1980.
[55] W.L. Willis, Pulse-voltage circuits, in: R.E. Dollinger, W.J. Sarjeant (Eds.), High Power Electronics, first ed., Tab Books, PA, USA, 1989 (Chapter 3).
[56] K. Gregory, P. Stevenson, R. Burke, Four-stage Marx generator using thyristors, Rev. Sci. Instrum. 69 (11) (1998) 3996–3997.
[57] R.L. Cassel, An all solid state pulsed Marx type modulator for Magnetrons and Klystrons, in: Proceedings of IEEE International Power Modular Conference, 2004, pp. 836–838.

[58] L.M. Redondo, J. Fernando Silva, Repetitive high-voltage solid-state Marx modulator design for various load conditions, IEEE Trans. Plasma Sci. 37 (8) (2009) 1632–1637.
[59] W.D. Keith, D. Pringle, P. Rice, P.V. Birke, Distributed magnetic coupling synchronizes a stacked 25-kV MOSFET switch, IEEE Trans. Power Electron. 15 (1) (2000) 58–61.
[60] H. Canacsinh, L.M. Redondo, J.F. Silva, Marx-type solid-state bipolar modulator topologies: performance comparison, IEEE Trans. Plasma Sci. 40 (10) (2012) 2603–2610.
[61] L. Rocha, J.F. Silva, L. Redondo, Seven levels unipolar/bipolar pulsed power generator, IEEE Trans. Plasma Sci. 44 (10) (2016) 2060–2064.
[62] P.K. Bhadani, Capacitor-charging power supply for laser pulsers using a boost circuit, Rev. Sci. Instrum. 60 (4) (1989) 605–607.
[63] A.C. Lippincott, R.M. Nelms, A capacitor-charging power supply using a series-resonant topology, constant on-time/variable frequency control, and zero current switching, IEEE Trans. Ind. Electron. 38 (6) (1991) 438–447.
[64] B.E. Strickland, M. Garbi, F. Cathell, S. Eckhouse, M. Nelms, 2 kJ/sec 25-kV high-frequency capacitor-charging power supply using MOSFET switches, in: Proceedings of 1990 Nineteenth Power Modulator Symposium, 1990, pp. 531–534.
[65] R.L. Newsom, W.C. Dillard, R.M. Nelms, Digital power-factor correction for a capacitor-charging power supply, IEEE Trans. Ind. Electron. 49 (5) (2002) 1146–1153.
[66] F.P. Dawson, S.B. Dewan, A subresonant flyback converter for capacitor charging, in: Proceedings of Second Annual IEEE Applied Power Electronics Conference, March 1987, 1987, pp. 274–283.
[67] W.C. Dillard, R.M. Nelms, A digitally-controlled, low-cost driver for piezoceramic flight control surfaces in small unmanned air- craft and munitions, in: Seventeenth Annual Applied Power Electronics Conference Exposition, APEC '02, 2002, pp. 1154–1160.
[68] N.O. Sokal, R. Redl, Control algorithms and circuit designs for optimally flyback-charging an energy-storage capacitor (e.g. for flash lamp or defibrillator), IEEE Trans. Power Electron. 12 (5) (1997) 885–894.
[69] M.A.V. Ward, DC to DC converter current pump, U.S. Patent Number 4,868,730, September 1989.
[70] G.C. Chryssis, High-Frequency Switching Power Supplies: Theory and Design, McGraw-Hill Publishing, New York, 1989.
[71] R.M. Nelms, J.E. Schatz, A capacitor charging power supply utilizing a ward converter, IEEE Trans. Ind. Electron. 39 (5) (1992) 421–428.

Further Reading

[1] H.W. Lord, Pulse transformers, IEEE Trans. Magn. 7 (1) (1971) 17–28.
[2] P.M. Ranon, Compact pulsed transformer power conditioning system for generating high voltage, high energy, rapid rise time pulses, IEEE Trans. Magn. 25 (1) (1989) 480–484.

19

Uninterruptible Power Supplies

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19.1 Introduction

Power distortions such as power interruptions, voltage sags and swells, voltage spikes, and voltage harmonics can cause severe impacts on sensitive loads in the electric systems. Uninterruptible power supply (UPS) systems are used to provide uninterrupted, reliable, and high-quality power for these sensitive loads. Applications of UPS systems include medical facilities, life-supporting systems, data storage and computer systems, emergency equipment, telecommunications, industrial processing, and online management systems [1–3]. The UPS systems are especially required in places where power outages and fluctuations occur frequently. A UPS provides a backup power circuitry to supply vital systems when a power outage occurs. In situations where short-time power fluctuations or disturbed voltage occur, a UPS provides constant power to keep the important loads running. During extended power failures, a UPS provides backup power to keep the systems running long enough so that they can be gracefully powered down.

Most of the UPS systems also suppress line transients and harmonic disturbances. Generally, an ideal UPS should be able to simultaneously deliver uninterrupted power and provide the necessary power conditioning for the particular power application. Therefore, an ideal UPS should have the following features: regulated sinusoidal output voltage with low total harmonic distortion (THD) independent from the changes in the input voltage or in the load, online operation that means zero transition time from normal to backup mode and vice versa, low THD sinusoidal input current and unity power factor, high reliability, high efficiency, low EMI and acoustic noise, electric isolation, low maintenance, low cost, weight, and size. Obviously, there is not a single configuration that can provide all of these features. Different configurations of UPS systems emphasize on some of the features mentioned above. Classifications of UPS systems are described in Section 19.2.

19.2 Classifications

19.2.1 Standby UPS

This configuration of UPS system is also known as "off-line UPS" or "line-preferred UPS" [4,5]. Fig. 19.1 shows the configuration of a typical standby UPS system. It consists of an AC/DC converter, a battery bank, a DC/AC inverter, and a static switch. A passive low-pass filter may also be used at the output of the UPS or inverter to remove the switching frequency from the output voltage. The static switch is on during the normal mode of operation. Therefore, load is supplied from the AC line directly without any power conditioning. At the same time, the AC/DC rectifier charges the battery set. This converter is rated at a much lower power rating than the power demand of the load. When a power outage occurs or the primary power is out of a given preset tolerance, the static switch is opened and the DC/AC inverter provides power to the load from the battery set for the duration of the preset backup time or till the AC line is back again. This inverter is rated at 100% of the load power demand. It is connected in parallel to the load

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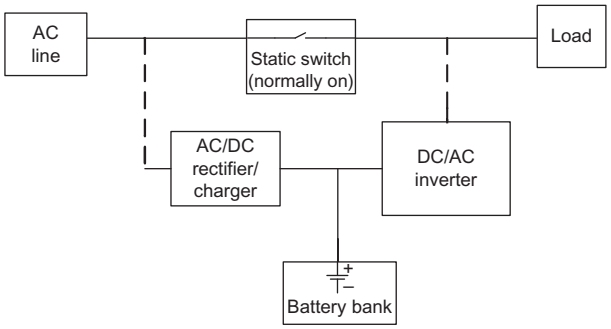


FIG. 19.1 Configuration of a typical standby UPS system.

and stays standby during the normal mode of operation. The transition time from the AC line to DC/AC inverter is usually about one-quarter of the line cycle, which is enough for most of the applications such as personal computers. The main advantages of this topology are simple design, low cost, and small size. On the other hand, the lack of real isolation of the load from the AC line, no output voltage regulation, long switching time, poor performance with nonlinear loads, and no line conditioning are the main disadvantages of this configuration.

Different configurations of AC/DC rectifiers such as linear or switching may be used in this system. To reduce the cost, a simple diode-bridge rectifier with a capacitor at the front end is used. A full-bridge or half-bridge full controlled converter is also used to charge the battery bank. Two typical topologies for a single-phase UPS system are shown in Fig. 19.2. The full controlled topologies can provide power factor correction (PFC) to meet the corresponding standards. To optimize the charging process, the charging cycle is divided into "constant current" and "constant voltage" modes. In the constant current mode, the converter injects a constant current into the battery till the battery is charged up to about 95% of its capacity. After this mode, the constant voltage mode starts that applies a constant voltage on the battery. In this mode, the input current of the battery declines exponentially until it is fully charged.

The purpose of the DC/AC inverter is to provide high-quality AC power to the load when the static switch is opened. A full- or half-bridge topology is used for this inverter. Fig. 19.3 shows two simple single-phase topologies for the DC/AC inverter.

In some topologies of standby UPS systems, an isolating transformer is used at the output stage of the UPS. This topology is called ferroresonant standby UPS system. The transformer also acts as a low-pass filter that cancels out switching frequency from the output voltage of the DC/AC inverter. On the other hand, the transformer stores electromagnetic energy in the core and acts as a buffer when a power

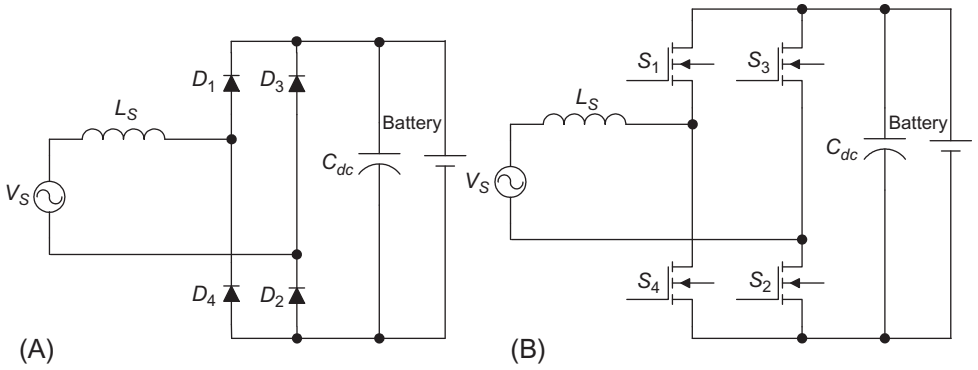


FIG. 19.2 Two simple topologies of AC/DC rectifier: (A) full-bridge diode rectifier and (B) full-bridge full controlled topology.

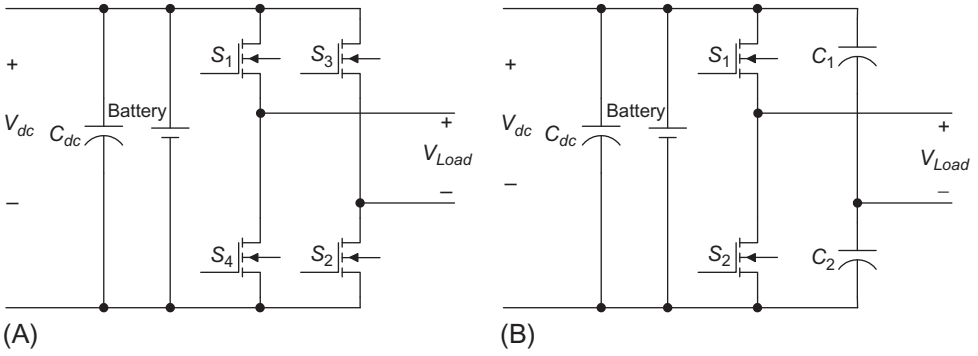


FIG. 19.3 Two simple single-phase topologies for the DC/AC inverter: (A) full bridge and (B) half bridge.

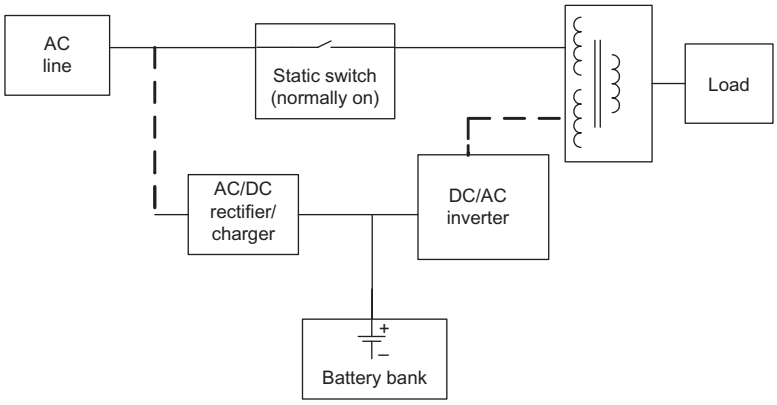


FIG. 19.4 Typical configuration of ferroresonant standby UPS system.

outage occurs. For a short time, the transformer provides power to the load and protects sensitive equipment from being affected during the transfer time from the input AC to the UPS. Fig. 19.4 shows the configuration of a ferroresonant standby UPS system. Since the transformer is bulky and expensive, this configuration is more appropriate for high-power applications.

19.2.2 On-Line UPS System

Similar to standby UPS systems, online UPS systems also consist of a rectifier/charger, a battery set, an inverter, and a static switch (bypass). Other names for this configuration are "true UPS," "inverter-preferred UPS," and "double-conversion UPS" [6,7]. Fig. 19.5 shows the block diagram of a typical online UPS. The rectifier/charger continuously supplies power to the DC bus. The power rating of this converter must be designed appropriately to supply power to the load and charge the battery bank at the same time. The batteries are rated in order to supply full power to the load during the backup time. The duration of this time varies in different applications. The inverter is rated at 100% of the load power since it must supply the load during the normal mode of operation and during the backup time. It is connected in series with the load; hence, there is no transfer time associated with the transition from normal mode to stored energy mode. This is the main advantage of online UPS systems. The static switch provides redundancy of the power source in the case of UPS malfunction or overloading. The AC line and load voltages must be in phase in order to use the static switch. This can be achieved easily by a phase-locked loop control. During the normal mode of operation, the power to the load is continuously supplied via the rectifier/charger and inverter. In fact, a double conversion from AC to DC and then from DC to AC takes place. This configuration of the UPS allows good power conditioning. The AC/DC converter charges the battery set and also supplies power to the load via the inverter. Therefore, it has the highest power rating in this topology, thereby increasing the cost. When the AC input voltage is outside the preset tolerance, the inverter and battery maintain continuity of power to the load. The duration of this mode is the duration of preset UPS backup time or till the AC line returns within the preset tolerance.

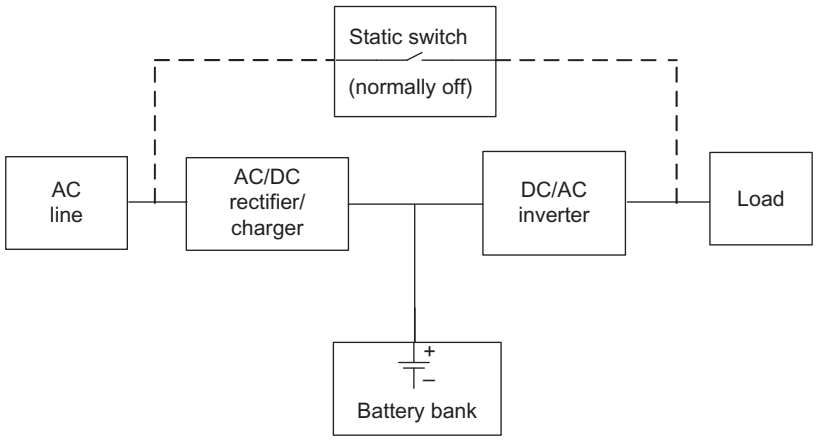


FIG. 19.5 Block diagram of an online UPS system.

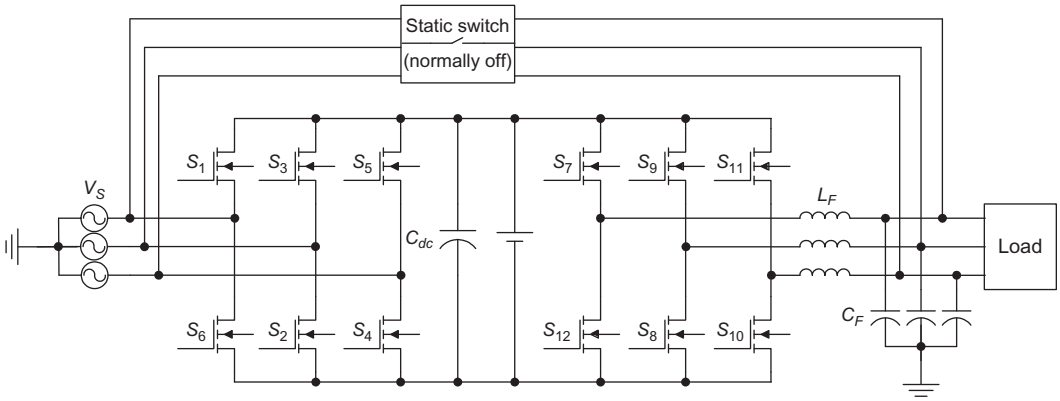


FIG. 19.6 Configuration of a three-phase online UPS system.

The main advantages of online UPS are very wide tolerance to the input voltage variation and very precise regulations of output voltage. In addition, there is no transfer time during the transition from normal to stored energy modes. It is also possible to regulate or change the output frequency [8]. The main disadvantages of this topology are low-power factor, high THD at the input, and low efficiency. The input current is distorted by the rectifier unless an extra PFC circuit is added; but, this adds to the cost of the UPS system [9].

As mentioned for the standby UPS system, different topologies are employed for the AC/DC rectifier and DC/AC inverter. Unlike standby UPS system, in this system, these converters provide power to the load continuously. Therefore, more care should be given to the quality of the input current and output voltage and the efficiency of the system. Fig. 19.6 shows the configuration of a three-phase online UPS system. The proper switching method such as pulse-width modulation (PWM) is employed for the AC/DC rectifier to minimize the input current harmonics and provide regulated DC bus voltage. A low-pass filter at the output of the system removes the switching frequency from the output voltage.

19.2.3 Line-Interactive UPS

Line-interactive UPS systems consist of a static switch, a series inductor, a bidirectional converter, and a battery bank. An optional passive filter can be added at the output of the bidirectional converter or at the input side of the load. A line-interactive UPS can operate either as an online UPS or as an off-line UPS. For an off-line line-interactive UPS, the series inductor is not required. However, most of the line-interactive UPS systems operate online in order to either improve the power factor of the load or regulate the output voltage for the load. When the AC line is within the preset tolerance, it feeds the load directly. The AC/DC converter is connected in parallel with the load and charges the battery. This converter may also be used to improve the power factor of the system and compensate the load current harmonics [10,11]. Typical configuration of a line-interactive UPS is shown in Fig. 19.7.

When a power outage occurs or input voltage falls outside the preset tolerance, the system goes to bypass mode. In this mode, the bidirectional converter operates as a DC/AC inverter and supplies power to the load from the battery set. The static switch disconnects the AC line in order to prevent back-feed from the inverter. The main advantages of the line-interactive UPS systems are simple design and, as a result, high reliability and lower cost compared with the online UPS systems. They also have good harmonic suppression for the input current. Since this is a single-stage conversion topology, the efficiency is higher than online UPS system. The main disadvantage is the lack of effective isolation of the load from the AC line. Employing a transformer in the output can eliminate this; but, it will add to the cost, size, and weight of the UPS system. Furthermore, the output voltage conditioning is not good because the inverter is not connected in series with the load. In addition, since the AC line supplies the load directly during the normal mode of operation, there is no possibility for regulation of the output frequency.

19.2.4 Universal UPS

This type of UPS is also called “series parallel” or “delta conversion.” Its topology is derived from unified power quality conditioner topology and combines the advantages of both online and line-interactive UPS systems [12,13]. It can achieve unity power factor, precise regulation of the output voltage, and high efficiency simultaneously. Its configuration is shown in Fig. 19.8. It consists of two bidirectional converters connected to a common battery set, a static switch, and a series transformer. The series bidirectional converter is rated at about 20% of the output power of the UPS system, and it is connected via a transformer in series with the AC line. The second bidirectional converter is the usual inverter for a line-interactive UPS connected in parallel to the load and rated at 100% of the output power.

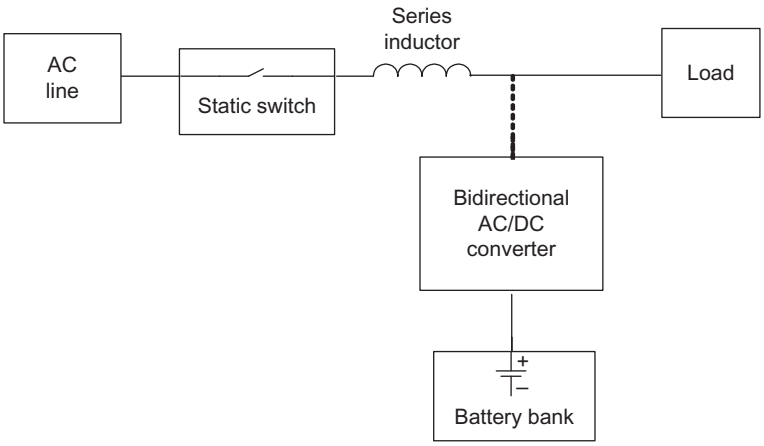


FIG. 19.7 A typical configuration of a line-interactive UPS system.

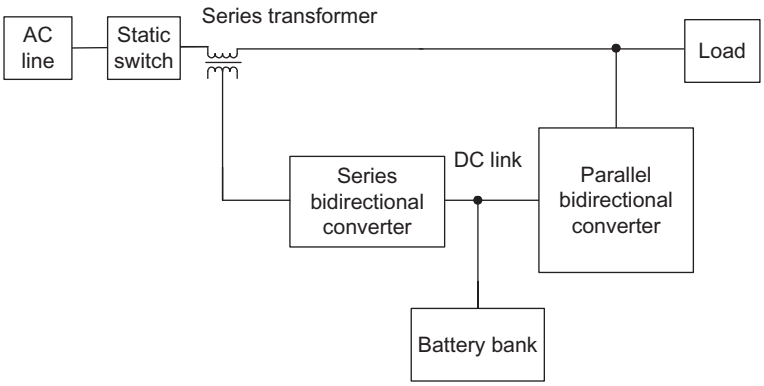


FIG. 19.8 Block diagram of a universal UPS system.

When the input voltage is in the acceptable range, the system is in the bypass mode. In this mode, parallel converter deals with current-based distortions. It mitigates load current harmonics and improves input power factor. At the same time, it charges the battery pack. Series converter deals with voltage-based distortions. It cancels input voltage harmonics and compensates voltage sags and swells. Most of the power is supplied directly from the AC line to the load. Only a small percentage of the input power is absorbed by parallel converter. This power is used to compensate the differences between input and reference voltages and to charge the battery pack. On the other hand, when the input voltage shuts down, the static switch separates the source and the load, and the system goes to backup mode. In this situation, the parallel inverter acts as a DC/AC inverter and supplies power to the load. Since a large portion of the power flows without any conversion from the AC line to the load, the efficiency is higher than that of an online UPS system. Having eliminated the main drawback of double-conversion UPS systems, the universal UPS topology appears to be a strong competitor of online UPS systems in many applications. Fig. 19.9 shows the topology of a three-phase universal UPS system.

19.2.5 Rotary UPS

Rotary UPS systems use the stored kinetic energy in the electric machines to provide power to the load when a power outage occurs. There are different configurations for rotary UPS systems. The simplest topology consists of an AC motor and an AC generator, which are mechanically coupled. A flywheel is also used on the shaft of the machines to store more kinetic energy in the system. In normal operation, the input AC line provides power to the AC motor, and this AC motor drives the AC generator. The configuration of this system is shown in Fig. 19.10A. In backup mode, the kinetic energy stored in the motor, flywheel, and generator is converted to electric power and supplies the load. This simple topology is designed to provide short-time backup power to the load (typically less than 2 s) in case of power interruption. In another configuration of rotary UPS system that is shown in Fig. 19.10B, an AC

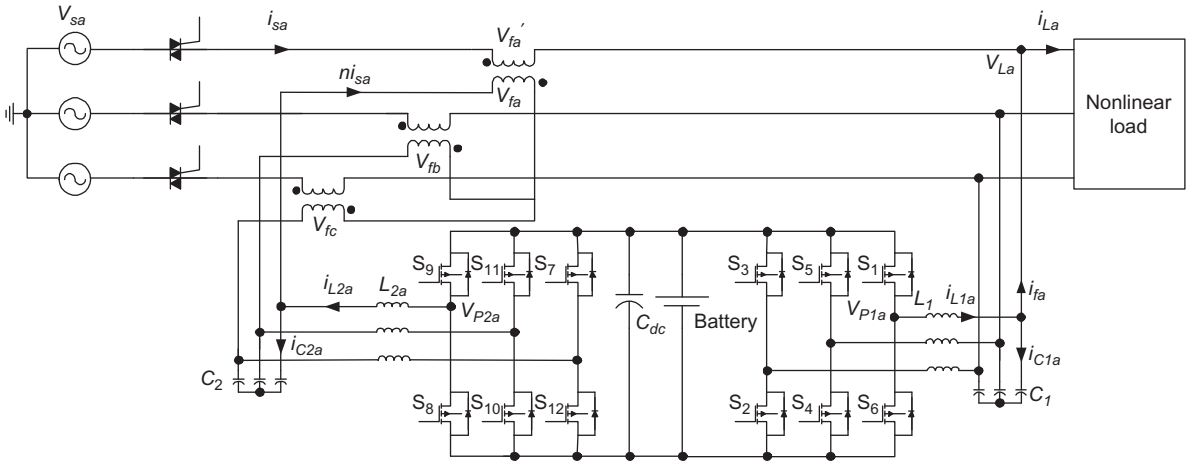


FIG. 19.9 A universal UPS topology based on two three-leg bidirectional converters.

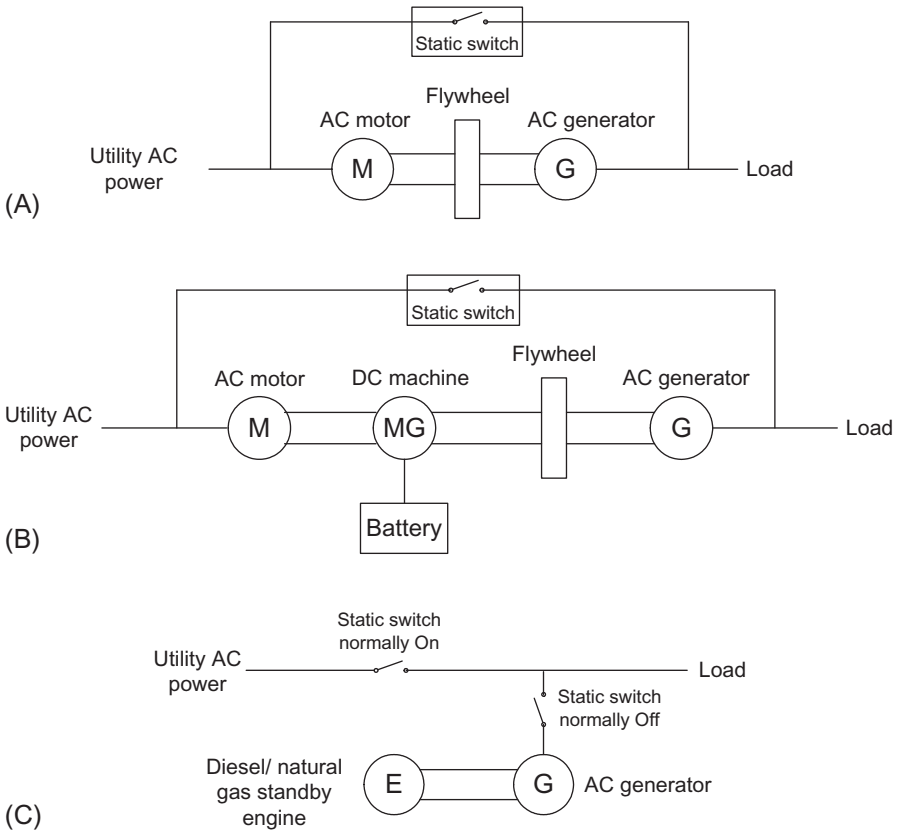


FIG. 19.10 Different configuration of rotary UPS systems: (A) motor-generator set, (B) rotary UPS with battery backup, and (C) rotary UPS with standby diesel/natural gas engine.

motor, a DC machine, an AC generator, and a battery bank are used. During the normal mode of operation, the AC line supplies the AC motor, which drives the DC machine. The DC machine drives the AC generator, which supplies the load. During the backup mode of operation, the battery bank supplies the DC machine, which, in turn, drives the AC generator and the AC generator supplies the load. This system can provide long-time backup power to the load depending on the capacity of the battery set. These two rotary UPS systems are much more reliable than the static UPS systems and provide complete electric isolation between the load and input AC line. Yet, they require more maintenance and have much bigger size and weight.

Therefore, they are usually used for high-power applications [14,15]. The configuration of a standby rotary UPS system is shown in Fig. 19.10C. This system does not provide electric isolation between the load and input AC. There is also a transition delay for switching from main AC to backup AC generator. However, it can provide power to the load as long as needed.

19.2.6 Hybrid Static/Rotary UPS

Hybrid static/rotary UPS systems combine the main features of both static and rotary UPS systems. They have low output impedance, high reliability, excellent frequency stability, and low maintenance requirements [16]. Typical configurations of hybrid static/rotary UPS are depicted in Fig. 19.11. They are usually used in high-power applications. In the system shown in Fig. 19.11A, during normal operation, the input AC power feeds the AC motor. The power is provided to the load from the AC generator, which is driven by the AC motor. In case of low input power quality or power interruption, the bidirectional AC/DC converter acts as an inverter and feeds the AC motor from battery pack. Configuration of a hybrid UPS system with power conditioning at the input is shown in Fig. 19.11B. Fig. 19.11C shows the configuration of a more complicated hybrid UPS system. This system has three operation modes. In normal operation, the load is directly supplied by the main AC input, and the AC motor is rotated at no-load. In the case of short power interruption, main breaker and generator breaker are opened and the inverter breaker is closed. The DC/AC inverter provides power to the load from the

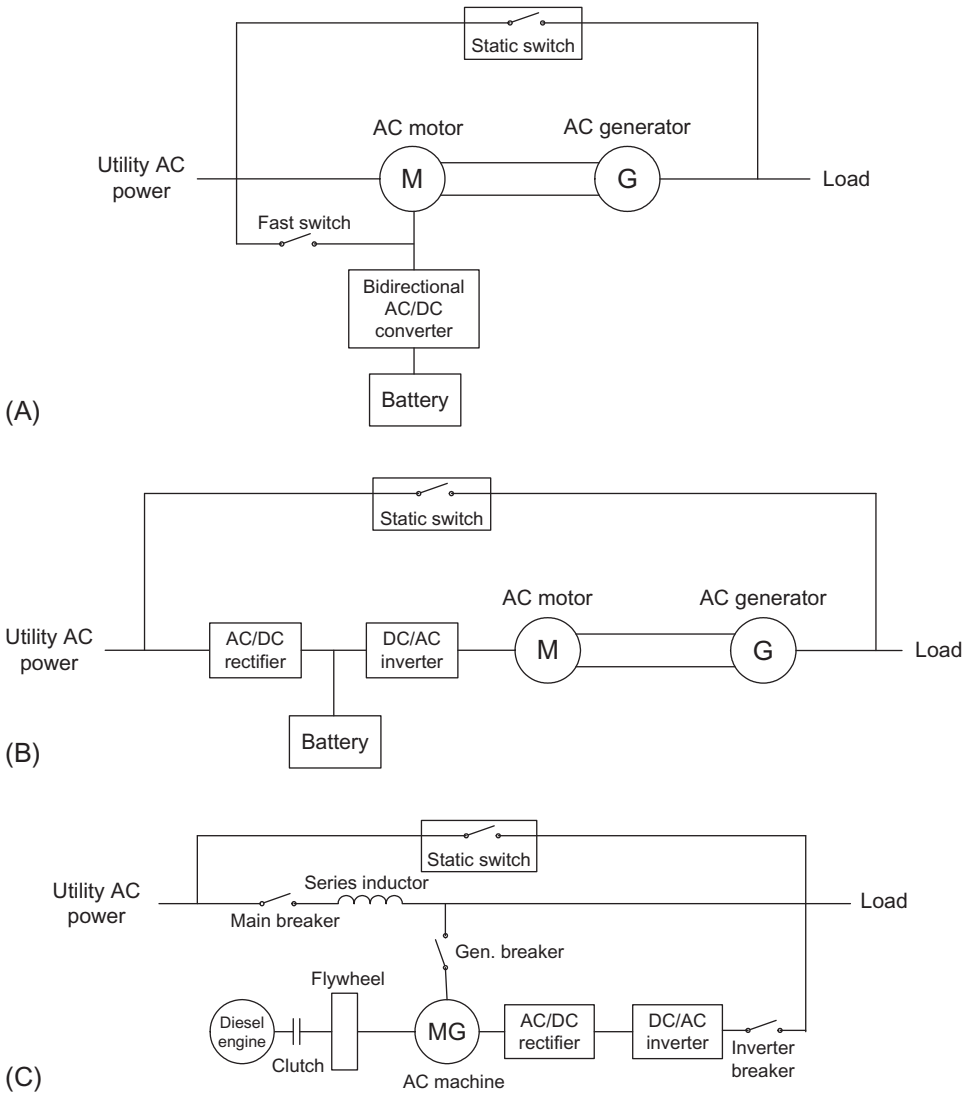


FIG. 19.11 Three configurations of hybrid rotary-static UPS systems: (A) motor-generator set with battery backup, (B) motor-generator set with power conditioning at input side, and (C) batteryless hybrid UPS system.

kinetic energy stored in the AC machine. If power is not restored in the short term, the diesel engine is turned on, which provides power to the load through the AC generator. In this mode, the main breaker and inverter breaker remain open. One of the advantages of this topology is operation without a battery set to minimize cost, space, and required maintenance. The second advantage is avoiding double power conversion in long-term power interruption.

19.2.7 DC UPS

All the aforementioned UPS configurations systems, including static, rotary, and hybrid UPS systems, are AC-based UPS systems as most UPS systems currently are available in the industry. In these systems, the AC main source directly or through several power conversions is connected to the load, and the power exchanged between different parts of the system has an AC format, except for the battery. The DC UPS system is based on the DC concept where the power flow in the system has DC characteristics, or in other words, the system shares power through a DC bus that connects all main parts, including source, loads, and energy storage, while in AC system, this link is an AC bus. The DC UPS system has several advantages with respect to the online three-phase UPS that is extensively used in industry, such as lower size, cost, and weight due to replacing the three-phase dual converter in the online UPS system with a single-stage single-phase DC/DC converter, and thus, higher efficiency is expected.

Fig. 19.12 illustrates the block diagram of the DC line-interactive UPS system. This UPS shares a DC bus between the attached sources and loads. The DC link is also integrated with a battery pack through a DC/DC bidirectional power converter. The DC UPS consists of an AC/DC rectifier, a DC/DC bidirectional converter, and the battery pack. This UPS configuration is designed for pulse loads where frequent high-power pulses with short-time duration, that is, less than 10 s, are required. The DC/DC converter regulates the DC link voltage and controls the charging and discharging processes of the battery pack. The AC/DC rectifier operates in such a way to provide unity power factor. The rectifier is designed to supply the load average power plus the battery charging power while the DC/DC converter rated for the load peak power.

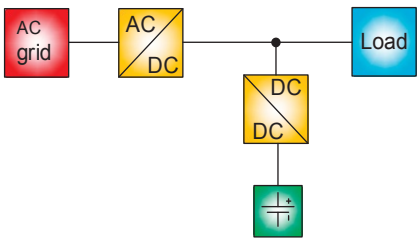


FIG. 19.12 Block diagram of the proposed DC line-interactive UPS system.

The DC UPS system will also provide load leveling feature for the main AC/DC rectifier that has not been offered by conventional AC UPS systems. It applies load power smoothing to reduce the rating of the incoming AC line and consequently reduce the installation cost and time.

The DC UPS, as shown in Fig. 19.12, is integrated with safe and high-power-density battery, which links to the DC link through a bidirectional DC/DC converter. In case of utility power disruptions, the proposed system provides power from the battery to directly energize the DC section and ensure continue and reliable operation.

The DC UPS system operates in four different modes, which are defined based on the load profile, battery pack status, and connection of the main AC source. These modes include high-rate discharging mode, a so-called load leveling mode, the standby mode, online mode, and UPS or islanded mode. The first mode is the high-rate discharging mode in which the load requires a pulsed peak power provided by the battery though DC/DC converter, following by a rest time in which battery is charged from the grid power. The third mode begins when the battery is fully charged during second mode. Finally, the fourth mode is when the AC main source is not available and the entire power provided by the battery pack.

19.2.8 Comparison of UPS Configurations

Table 19.1 provides the comparison between the characteristics of different types of UPS systems.

19.3 Performance Evaluation

There are four criteria for evaluating the performance of a UPS system: quality of output voltage, input PFC and current harmonic cancellation, transition time, and efficiency.

The quality of output voltage is the most important factor. The output voltage of an AC UPS system should be sinusoidal with low THD in different loading conditions even with nonlinear loads. The control system should have small transient responses to provide appropriate line conditioning in different loading profiles. Typically, rotary UPS systems, which employ an AC generator at the load side, have better output voltage quality than static UPS systems. In these systems, there is no converter switching frequency present at the output voltage. Among the static UPS systems, online UPS configuration provides better output voltage quality. In this system, output voltage is provided by a DC/AC inverter regardless of input voltage quality. Usually, a PWM method is used to regulate the output voltage. This kind of UPS should be designed to have minimum switching frequency at the output and provide pure sinusoidal voltage at different loading conditions. Followed by online UPS system are universal and line-interactive configurations. In universal topology, during normal mode of operation,

TABLE 19.1 Performance comparison of different configurations of UPS systems

Parameter	Online	Line interactive	Off-line	Universal	Rotary	Hybrid	DC
Surge protection	Excellent	Good	Good	Good	Excellent	Excellent	Good
Transition time	Excellent	Good	Poor	Good	Excellent	Excellent	Good
Line conditioning	Poor	Good	Poor	Excellent	Good	Good	Good
Backup duration	Depends on battery	Depends on battery	Depends on battery	Depends on battery	Typically 0.1–0.5 s	Depends on battery	Depends on battery
Efficiency	Low around 80%	High up to 95%	High	High up to 95%	High typically above 85%	High typically around 95%	High up to 95%
Input/output isolation	Poor	Poor	Poor	Poor	Perfect	Perfect	Good
Load leveling	No	No	No	No	No	No	Excellent
Cost	High	Medium-high	Low	High	Very high	Very high	Low-medium

the series converter provides voltage conditioning and regulates output voltage. In the backup mode, the parallel converter provides the load with sinusoidal voltage. In the line-interactive topology, during normal operation mode, input voltage directly supplies the load and no voltage conditioning is provided. In the backup mode, the DC/AC inverter provides the load with sinusoidal voltage.

The second criterion is transition time from normal mode of operation to stored energy mode. Online rotary, DC, and static UPS systems have superior performance in this regard. The output voltage is always provided by the output generator or output converter, and there is no transition time between operation modes of the systems. However, some of the rotary and hybrid configurations shown in Figs. 19.10 and 19.11 can only provide power to the load for a limited time. This time is determined by the amount of kinetic energy stored in the mechanical system. The transfer time in universal and line-interactive topologies depends on the time necessary for converting the power flow from the battery bank through the inverter to the load. Improved performance is achieved by choosing the DC bus capacitor voltage at the battery side to be slightly higher than the floating voltage of the batteries. Therefore, when the AC line fails, it is not necessary to sense the failure because the DC bus voltage will immediately fall under the floating voltage of the batteries and the power flow will naturally turn to the load. For off-line UPS systems, the transfer time is the longest. It depends upon the speed of sensing the failure of the AC line and starting the inverter.

The next important factor is the input power factor and the ability of the system to provide conditioning for load power. Universal UPS system has better performance followed by line-interactive and online UPS in this regard. During normal mode of operation, the parallel converter acts as an active filter and compensates reactive current and current harmonics generated by the load. In the line-interactive system, the bidirectional AC/DC converter performs this task. In an online UPS system, an additional system must be added to improve PFC and mitigate current harmonics.

The last criterion for performance evaluation is efficiency. To emphasize this factor, it should be noted that losses in UPS systems represent about 5%–12% of all the energy consumed in data centers. Efficiency in rotary and hybrid configurations depends on the topology of the system, but typically, for low-power application due to mechanical loss in the motor and generator, the efficiency is not very high. Among the static UPS systems, online UPS system has the poorest efficiency due to double conversion. Line-interactive and universal topologies provide higher efficiencies since most of the power directly flows from the input AC to the load during normal operation. The DC UPS has efficiency close to the line-interactive UPS type and higher than online UPS due to lower number of power conversion stages between source and load.

19.4 Applications

The UPS systems have wide applications in a variety of industries. Their common applications range from small power rating for personal computer systems to medium power rating for medical facilities, life-supporting systems, data storage, and emergency equipment and high power rating for telecommunications, industrial processing, and online management systems. Different considerations should be taken into account for these applications. For emergency systems and lighting, the UPS should support the system for at least 90 min. Except for emergency systems, the UPS is designed to provide backup power to sensitive loads for 15–20 min. After this time, if the power is not restored, the system will be gracefully shut down. If a longer backup period is considered, a larger battery with higher cost and space is required. For process equipment and high-power applications, some UPS systems are designed to provide enough time for the secondary power sources such as diesel generators to start up.

For industrial applications, it should be noted that UPS systems add to the complexity of the electric system. They also add installation and ongoing maintenance costs. They may

also add nonlinearity to the system, decrease the efficiency, and deteriorate the input PFC mechanism. The power rating of the UPS should be appropriately selected considering the existing load and future extensions. For many applications, input voltage surges and spikes cause more damage than power outages. For these systems, another device instead of UPS can be utilized. Load characteristics should also be considered in UPS selection. For motor loads, the inrush current, which is sometimes 2.5 times of the rated current, should be considered. A good UPS for the motor loads is the one with higher transient overloads. For nonlinear loads such as switching power supplies, the input current is not sinusoidal. Therefore, the instantaneous current is higher than the RMS current. This high instantaneous current should be considered in UPS selection.

For a power distribution network, two different approaches are taken to support sensitive loads. In a distributed approach, which is more suitable for highly proliferated loads such as medical equipment, data processing, and telecommunications, many separate UPS units operate in parallel to supply critical loads. UPS units are placed flexibly in the system to form a critical load network. A typical online distributed UPS system is shown in Fig. 19.13. High flexibility and redundancy are the main advantages of distributed systems. Individual load increase can be supported by adding more UPS systems. Consideration for future extension can also be delayed until the loads are added. On the other side, this method has some disadvantages. The load sharing between different UPS units is a difficult task. Complicated digital control methods and communication between units are required to perform optimal load sharing. The second disadvantage is that the monitoring of the whole system is difficult and requires specially trained staff.

The other method to support distributed loads is to use a large UPS unit to supply all the critical loads in a centralized approach. This approach is more desirable for industrial and utility applications. The advantage of this method is easier maintenance and troubleshooting. The disadvantages on the other side are the lack of redundancy and high installation cost. In addition, consideration for system expansion should be taken into account when the original UPS unit is selected.

19.5 Control Techniques

The main task of the control system in an UPS unit is to minimize the output voltage THD in different loading profiles. In addition, it should provide the proper mechanism to recharge the battery set and maintain high input power factor and low total input current harmonic distortion. Other factors considered for a good control technique are nearly zero steady-state inverter output voltage error, good voltage regulation, robustness, fast transient response, and protection of the inverter against overload under linear/nonlinear loads.

The most common switching technique is sinusoidal PWM. This method can be utilized for both single-phase and three-phase systems. The advantage of this method is low output voltage harmonic and robustness. This strategy uses a single feedback loop to provide well-regulated output voltage with low THD. The feedback control can be continuous or discontinuous. Analog techniques are used in continuous approach. The sinusoidal PWM (SPWM) can be of natural sampling type, average type, or instantaneous type [17,18].

In natural sampling type, the peak value of the output voltage is detected and compared with a reference voltage in order to obtain the error, which is used to control the reference to the modulator. The average approach is basically the same; but, the sensed voltage is converted to an average value and, after that, is compared with a reference signal. These approaches control only the amplitude of the output voltage and are good only at high frequencies. In an instantaneous voltage feedback SPWM control, the output voltage is continuously compared with the reference signal improving the dynamic performance of the UPS inverter.

A typical block diagram of a three-phase DC/AC inverter for UPS systems and SPWM switching control technique is shown in Fig. 19.14. The disadvantage of this method is lack of flexibility for nonlinear loads. Other programmed PWM techniques such as selective harmonic elimination, minimum THD, minimum loss, minimum current ripple, and reduced acoustic noise may be used for the inverter.

Better performance even with nonlinear and step-changing loads can be achieved by multiple control loop strategies [19].

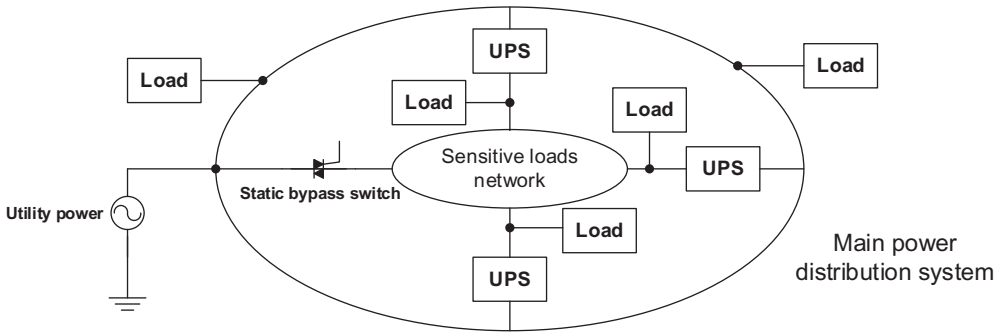


FIG. 19.13 Typical configuration of a distributed UPS network.

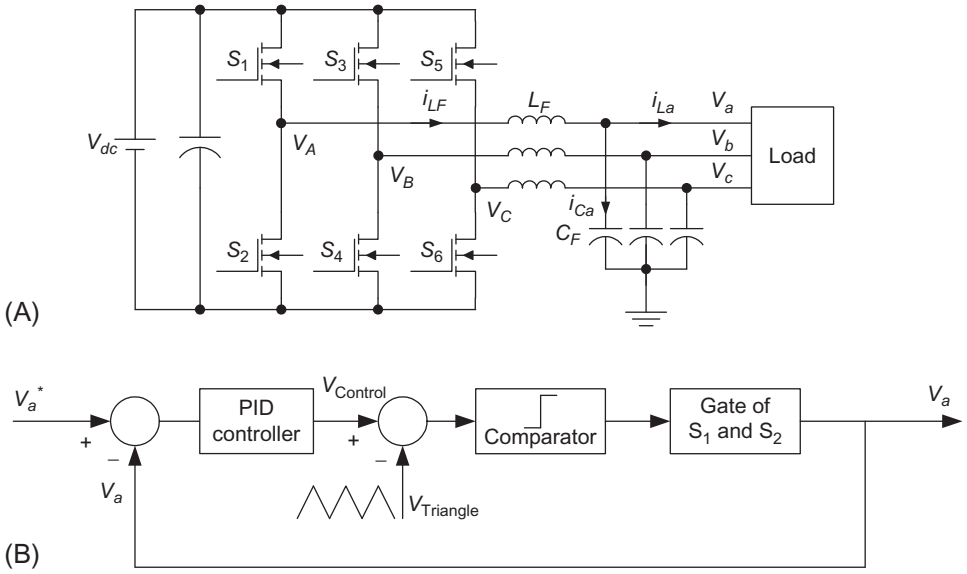


FIG. 19.14 (A) Configuration of a three-phase DC/AC inverter for UPS systems and (B) simple voltage controller using PWM technique.

As shown in Fig. 19.15, there are two-control loops: an outer and an inner. The outer control loop uses the output voltage as a feedback signal, which is compared with a reference signal. The error is compensated by a PI integrator to achieve stable output voltage under steady-state operation. This error is also used as a reference signal for the inner current regulator loop, which uses the inductor or the capacitor output filter current as the feedback signal. The minor current loop ensures fast dynamic responses enabling good performance with nonlinear or step-changing loads. The basic current regulators employed as minor current loop are hysteresis regulators, sinusoidal PWM regulator, and predictive regulators. In a typical hysteresis regulator, the reference signal is compared with the feedback signal. The sign and predetermined amplitude of the error determine the output of the modulator. The duration between two successive levels is determined by the slope of the reference signal. The output voltage tracks the reference signal within the upper and lower boundary levels. This hysteresis control has fast transient response; but, the switching frequency varies widely [20].

In SPWM control technique, the output voltage feedback is compared with a sine reference signal, and the error voltage is compensated by a PI regulator to produce the current reference. The current through the inductor or the capacitor is sensed and compared with the reference signal. After being compensated by a PI regulator, the error signal is compared with a triangular waveform to generate SPWM signal for switching control. The SPWM current control has a constant switching frequency and also provides fast dynamic responses. In predictive current control method, the switching instants are determined by suitable error boundaries. When the current vector touches the boundary line, the next switching state vector is determined by prediction and optimization in order to minimize the error. Predictive current control requires a good knowledge of the load parameters. All these current regulators are typically used as an inner loop to regulate the current in the filter inductor. The current reference for the current regulator is obtained by summing together the error in an outer voltage loop with the actual load current to yield the rated output voltage.

With the increase of speed and reliability of digital processors and a decrease in their cost, digital processors have been facing an enormous growth of popularity in

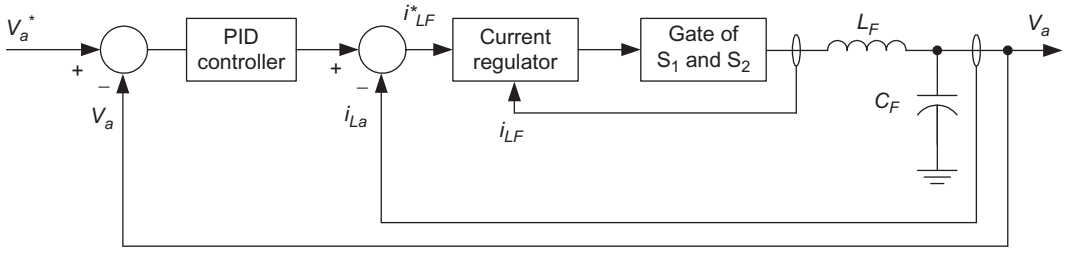


FIG. 19.15 Typical current and voltage control loops for UPS inverter.

control applications in the past few years. Many digital and discrete control techniques such as deadbeat control [21], dissipativity-based control [22], sliding-mode control [23], space vector-based control [24], and multiple-feedback loop [25] have been developed using digital signal processors.

In this section, fundamental analysis of a deadbeat control method is explained for the three-phase UPS configuration shown in Fig. 19.14A. The state-space equations of one phase of this system in the continuous time domain are as follows:

$$C_F\frac{dV_a}{dt}=i_{LF}-i_{La} \tag{19.1}$$

$$L_F\frac{di_{LF}}{dt}=V_A-V_a \tag{19.2}$$

Considering V_a and i_{LF} as state variables, the state-space equation of the system is as follows:

$$\begin{bmatrix}V_a\\ i_{LF}\end{bmatrix}^{\bullet}=\begin{bmatrix}0 & 1/C_F\\ -1/L_F & 0\end{bmatrix}\begin{bmatrix}V_a\\ i_{LF}\end{bmatrix}+\begin{bmatrix}0\\ 1/L_F\end{bmatrix}V_A+\begin{bmatrix}-1/C_F\\ 0\end{bmatrix}i_{La} \tag{19.3}$$

These continuous time-domain state-space equations are converted to the discontinuous time domain with a sampling period of T_s [26]:

$$\begin{aligned}\begin{bmatrix}V_a(k+1)\\ i_{LF}(k+1)\end{bmatrix}=&\begin{bmatrix}\cos\omega_0T_s & \dfrac{\sin\omega_0T_s}{\omega_0C_F}\\ -\dfrac{\sin\omega_0T_s}{\omega_0L_F} & \cos\omega_0T_s\end{bmatrix}\begin{bmatrix}V_a(k)\\ i_{LF}(k)\end{bmatrix}\\&+\begin{bmatrix}1-\cos\omega_0T_s\\ \dfrac{1}{\omega_{02}L_F}\sin\omega_0T_s\end{bmatrix}V_A(k)\\&+\begin{bmatrix}-\dfrac{1}{\omega_0C_F}\sin\omega_0T_s\\ 1-\cos\omega_0T_s\end{bmatrix}i_{La}(k)\end{aligned} \tag{19.4}$$

where ω_0 is the angular resonance frequency of L_F and C_F. The sampling frequency of the system is always considered much higher than the resonance frequency of L_F and C_F. With this assumption, Eq. (19.4) is simplified to Eq. (19.5). This conversion is valid for almost $f_s\geq 20f_0$:

$$\begin{aligned}\begin{bmatrix}V_a(k+1)\\ i_{LF}(k+1)\end{bmatrix}=&\begin{bmatrix}1 & T_s/C_F\\ -T_s/L_F & 1\end{bmatrix}\begin{bmatrix}V_a(k)\\ i_{LF}(k)\end{bmatrix}\\&+\begin{bmatrix}0\\ T_s/L_F\end{bmatrix}V_A(k)+\begin{bmatrix}-T_s/C_F\\ 0\end{bmatrix}i_{La}(k)\end{aligned} \tag{19.5}$$

The current equation according to Eq. (19.5) is given by

$$i_{LF}(k+1)=i_{LF}(k)+\frac{T_s}{L_F}[V_A(k)-V_a(k)] \tag{19.6}$$

Alternatively, this equation can be achieved by converting Eq. (19.2) from a differential equation to a difference equation. The same suggestion of $f_s\geq 20f_0$ has to be made for this conversion as well. If V_a and i^*_{LF} are considered constant over the next switching period, the output voltage of the inverter, which corrects the error of i_{LF} after two sampling periods, is described by

$$V_A(k+1)=V_a(k+1)+\frac{L_F}{T_s}\left[i^*_{LF}(k+1)-i_{LF}(k+1)\right] \tag{19.7}$$

A linear estimation of $V_a(k+1)$ can be achieved from previous values:

$$V_a(k+1)=V_a(k)+[V_a(k)-V_a(k-1)]=2V_a(k)-V_a(k-1) \tag{19.8}$$

By substituting Eqs. (19.8) and (19.10) in Eq. (19.9) and updating reference current for i_{LF} in every two sampling periods, the deadbeat digital control for series converter is described by

$$V_A(k+1)=\frac{L_F}{T_s}\left[i^*_{LF}(k)-i_{LF}(k)\right]-V_A(k)+3V_a(k)-V_a(k-1) \tag{19.9}$$

Eq. (19.9) ensures that the current error between i_{LF} and i^*_{LF} at time $k+2$ goes to zero with a delay of two sampling periods. Avoiding interaction between voltage and current control loops, load voltage, V_a, is sampled at half of the current sampling frequency. The voltage equation according to Eq. (19.5) is as follows:

$$V_a(k+1)=V_a(k)+\frac{T_s}{C_F}i_{CF}(k) \tag{19.10}$$

$$\begin{aligned}V_a(k+2)&=V_a(k+1)+\frac{T_s}{C_F}i_{CF}(k+1)\\&=V_a(k)+\frac{T_s}{C_F}i_{CF}(k)+\frac{T_s}{C_F}i_{CF}(k+1)\end{aligned} \tag{19.11}$$

As current control is suggested to be deadbeat with a delay of two sampling periods, capacitor current at time k and $(k+1)$ are given by

$$i_{CF}(k)=i^*_{CF}(k-2),i_{CF}(k+1)=i^*_{CF}(k-1) \tag{19.12}$$

Substituting Eq. (19.12) in Eq. (19.11) and updating the reference current at each of the two sampling periods, $V_a(k+2)$ is given by

$$V_a(k+2)=V_a(k)+\frac{2T_s}{C_F}i^*_{CF}(k-2) \tag{19.13}$$

The current of i^*_{CF} at time k that corrects the voltage error of V_a at time $k+4$ is as follows:

$$i^*_{CF}(k)=\frac{C_F}{2T_s}\left[V^*_a(k)-V_a(k)\right]-i^*_{CF}(k-2) \tag{19.14}$$

A block diagram of the implementation of voltage and current control of the inverter is shown in Fig. 19.16. Block diagram of the current and voltage controller for the inverter is also shown in Fig. 19.17. Voltage regulator is a pure deadbeat controller

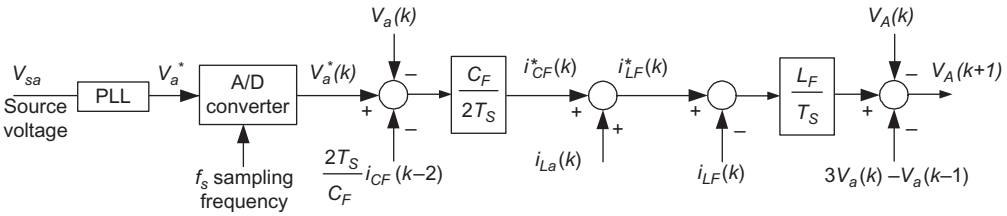


FIG. 19.16 Implementation of the current and voltage control for the inverter shown in Fig. 19.13A.

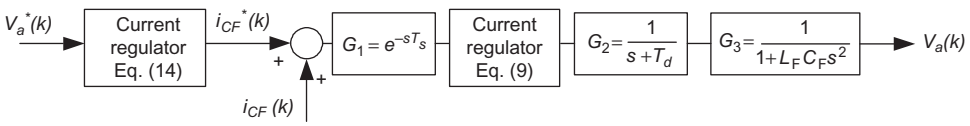


FIG. 19.17 Block diagram of the current and voltage controller for the inverter shown in Fig. 19.13A.

with a delay of two sampling periods including the consumed time for calculation. G_1 is the time delay needed for calculations and analog-to-digital conversions. G_2 is the time delay caused by the PWM inverter, and G_3 is the transfer function of the low-pass filter. Current regulator is also considered as a pure delay. The output voltage of the inverter follows its reference with four sampling periods of delay. In practice, the dynamics of the current regulator is not a pure delay and shows some deviation from the deadbeat controller.

Fig. 19.18 shows the schematic of the DC UPS. The system consists of two main converters, an AC/DC converter that manages power flow from grid to the DC bus and a DC/DC converter that regulates the DC bus voltage and also manages battery charging/discharging process. The goal for the grid-tied AC/DC rectifier is to deliver constant power to the DC link. In order to satisfy the goal, the rectifier operates on current mode and is controlled by the direct power control (DPC) method [27]. In the direct power control scheme, the direct and quadrature components of the grid currents are used to control active and reactive power independently. Fig. 19.19 illustrates the block diagrams of the AC/DC converter and the control technique.

A two-control loop method is used to manage the DC/DC converter. The controller consists of two main loops, an inner current loop and an outer voltage loop to monitor battery current while regulating the DC link voltage. Fig. 19.20 depicts the block diagram of the two-loop control technique. G_{vd} is the transfer functions of DC link voltage versus duty ratio of the DC/DC converter, and G_{id} is the transfer function of battery current versus duty ratio of the converter. G_{ci} and G_{vi} are the compensations, which need to be designed appropriately. There are several ways to design the compensators, such as desired pole/zero placement, step response, or frequency response. The frequency response characteristics are desired phase margin and crossover frequency (w_{wc}). It is desired for the system to have a crossover frequency 5–10 times lower than switching frequency and a phase margin of equal or greater than 40 degrees to have enough marginal stability.

19.6 Energy Storage Devices

In this section, three dominant main energy storage devices for the existing and future UPS systems are described. These energy storage devices are battery, flywheel, and fuel cell.

19.6.1 Battery

Battery is the energy storage component of current static UPS systems. It determines the capacity and run time of the UPS. For small units, it is the size of battery that determines the size of the UPS. Different types of batteries are used in UPS systems, but the most commonly used types are lead-acid, nickel-cadmium, and lithium-ion batteries. The lead-acid batteries used in this application are the same as the ones used in the cars. However, there is one small difference. Car batteries generate electricity by the reaction of sulfuric acid on lead plates that are drowned under the liquid. These types of battery cells are not suitable for UPS applications because there is a chance of acid spillage from them. In addition, during the charging process, they release hydrogen that is explosive and dangerous in a closed environment. Lead-acid batteries used in UPS systems are a special kind called sealed or valve-regulated. The nickel-cadmium batteries are another popular type of batteries used in UPS systems. They usually provide higher energy and power density compared with lead-acid batteries. The nominal voltage of nickel-cadmium cells is 1.2 V, which is smaller than 1.5 V of lead-acid batteries. However, the cell voltage variation throughout different charge levels is less than lead-acid batteries. These batteries also have less series resistance and can provide higher surge currents.

Lithium-ion batteries have much higher energy density. This kind of battery can be molded into different shapes. They have a nominal voltage of 4.2 V. These batteries have higher power and energy densities compared with lead-acid batteries. A long life cycle without memory effect, together with high columbic efficiency and low self-discharge characteristics, makes this type of battery the preferred energy storage choice for a wide variety of applications including UPS systems.

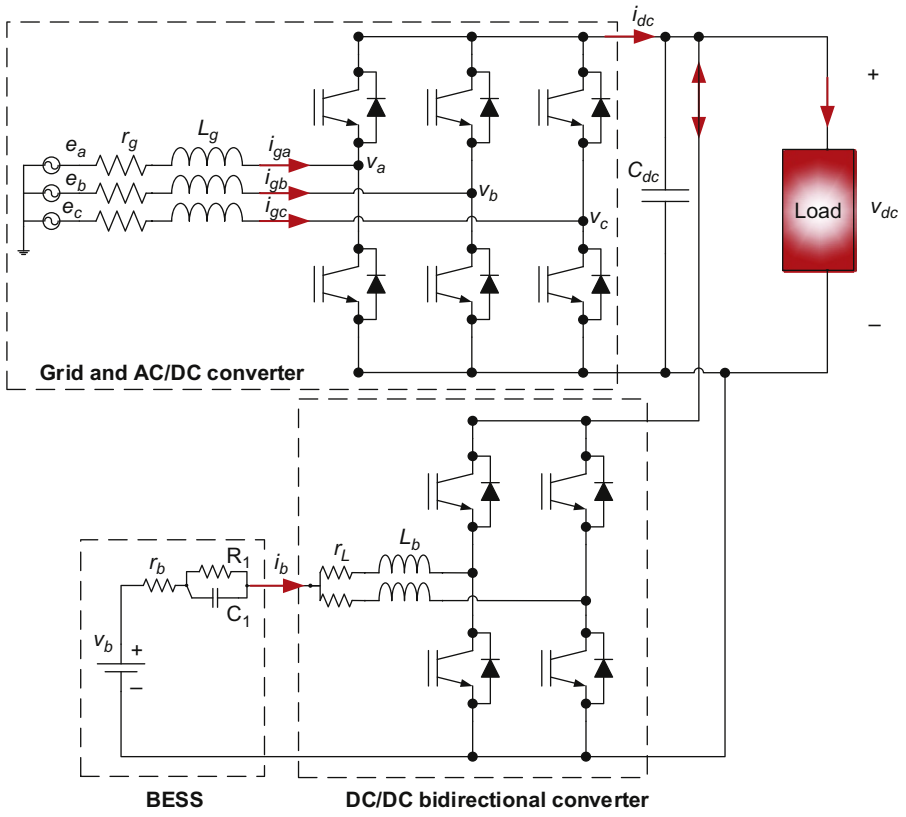


FIG. 19.18 Schematic of the DC UPS system.

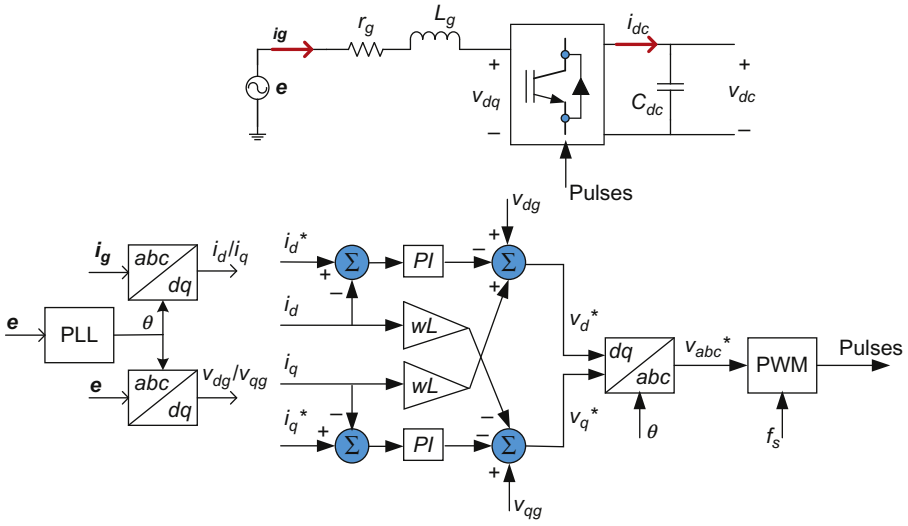


FIG. 19.19 Block diagram of the grid-tied AC/DC rectifier and controller scheme. Direct power control method is used to control the rectifier.

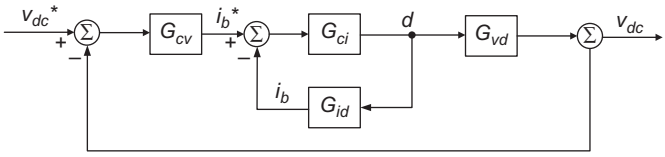


FIG. 19.20 Block diagram of the two-control loop method used to manage the DC/DC converter in the DC UPS.

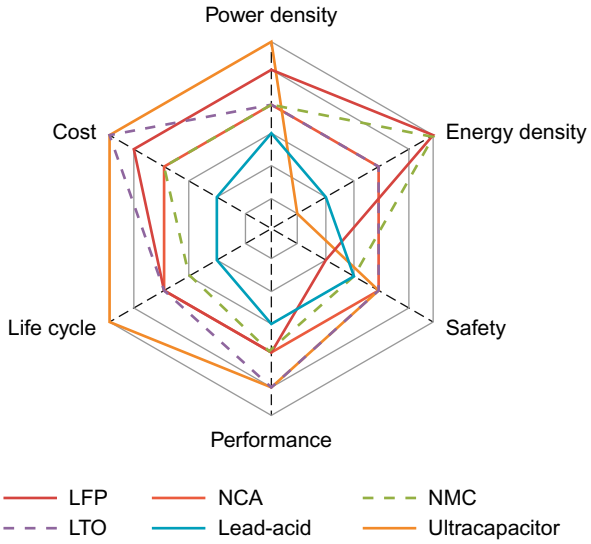


FIG. 19.21 Comparison of different Li-ion batteries, lead-acid, and ultracapacitor.

The electrode material greatly influences the battery specifications in terms of power and energy density, voltage characteristics, lifetime, and safety. A typical cathode, that is, the positive active electrode, is made of a lithium metal oxide and common materials such as cobalt ($LiCoO_2$ or LCO) and manganese ($LiMn_2O_4$ or LMO). Combined chemistries including nickel-cobalt-aluminum (NCA), nickel-manganese-cobalt (NMC), and iron phosphate (LFP) are also employed for the cathode. Graphite and lithium titanate ($Li_4Ti_5O_{12}$ or LTO) are the typical choices for the anode, that is, the negative active electrode [28]. Fig. 19.21 compares different Li-ion batteries with lead-acid and ultracapacitor.

19.6.2 Flywheel

Flywheel is simply a mechanical mass that is placed on the shaft of a motor-generator set and stores mechanical energy in the form of kinetic energy. When the electric power is required, this kinetic energy is converted to electricity by the generator coupled with the flywheel. Flywheels are the oldest type of energy storage devices. The advantages of flywheel energy storage systems are high efficiency, high energy and power density, and long life. On the other hand, flywheels are more expensive and require more space than batteries and fuel cells. There are also some safety concerns about flywheels rotating at high speeds.

19.6.3 Fuel Cell

Due to high efficiency and low emissions, fuel cell systems have been gaining popularity in recent years. A fuel cell uses hydrogen as fuel and produces electricity, heat, and water from the reaction between hydrogen and oxygen. Each cell consists of an electrolyte and two electrodes as anode and cathode. Fig. 19.22 shows the configuration of a typical fuel cell system. There are different kinds of fuel cell system depending on the types of electrolyte and hydrogen sources. Some fuel cell systems have an onboard fuel reformer and generate hydrogen from natural gas, methanol, and other hydrocarbons. Recent technology development in this field has made fuel cells a more reliable and cost-effective alternative for batteries. Fuel cells currently have a variety of applications in automotive, electric utility, and portable power industries. Table 19.2 provides a comparison between the most popular types of fuel cells.

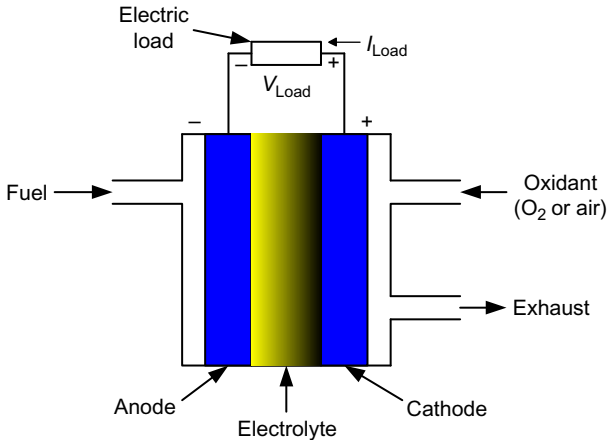


FIG. 19.22 Configuration of a typical fuel cell system.

TABLE 19.2 A comparison between the different types of fuel cell system

Fuel cell type	Applications	Advantages	Disadvantages
Proton exchange membrane (PEM)	• Electric utility • Portable power • Automotive	• Solid electrolyte reduces corrosion and management problems • Low temperature • Quick start-up	• Expensive catalysts • High sensitivity to fuel impurities
Alkaline (AFC)	• Military • Space	• High performance	• Expensive removal of CO_2 from fuel and air streams required
Phosphoric acid (PAFC)	• Electric utility • Automotive	• Up to 85% efficiency in cogeneration of electricity and heat • Can use impure H_2 as fuel	• Expensive catalysts • Low power • Large size/weight
Molten carbonate (MCFC)	• Electric utility	• High efficiency • Fuel flexibility • Can use a variety of catalysts	• High temperature enhances corrosion and breakdown of cell components
Solid oxide fuel cell (SOFC)	• Electric utility	• High efficiency • Fuel flexibility • Can use a variety of catalysts • Solid electrolyte reduces corrosion and management problems • Low temperature • Quick start-up	• High temperature enhances the breakdown of cell components
Direct alcohol fuel cell (DAFC)	• Automotive • Portable power	• Compactness • High energy density	• Lower efficiency • Alcohol passing between electrodes without reacting

References

[1] S. Karve, Three of a kind, IEE Rev. 46 (2) (2000) 27–31.

[2] R.H. Carle, UPS applications: mill perspective, IEEE Ind. Appl. Mag. 1 (6) (1995) 12–17.

[3] R. Krishnan, S. Srinivasan, Topologies for uninterruptible power supplies, in: Proc. IEEE International Symposium on Industrial Electronics, Hungary, 1993, pp. 122–127.

[4] F. Kamran, T.G. Habetler, A novel on-line UPS with universal filtering capabilities, IEEE Trans. Power Electron. 13 (2) (1998) 366–371.

[5] J.H. Choi, J.M. Kwon, J.H. Jung, B.H. Kwon, High-performance online UPS using three-leg-type converter, IEEE Trans. Ind. Electron. 52 (3) (2005) 889–897.

[6] H. Pinheiro, P.K. Jain, G. Joos, A comparison of UPS for powering hybrid fiber/coaxial networks, IEEE Trans. Power Electron. 17 (3) (2002) 389–397.

[7] I. Youichi, I. Satoru, T. Isao, H. Hitoshi, New power conversion technique to obtain high performance and high efficiency for single-phase UPS, in: Proc. 36th IEEE Industry Applications Conference, vol. 4, 2001, pp. 2383–2388.

[8] H. Gueldner, H. Wolf, N. Blacha, Single phase UPS inverter with variable output voltage and digital state feedback control, in: Proc. IEEE International Symposium on Industrial Electronics, vol. 2, 2001, pp. 1089–1094.

[9] J. Lee, Y. Chang, F. Liu, A new UPS topology employing a PFC boost rectifier cascaded high-frequency tri-port converter, IEEE Trans. Ind. Electron. 46 (4) (1999) 803–813.

[10] F. Kamran, T.G. Habetler, A novel on-line UPS with universal filtering capabilities, IEEE Trans. Power Electron. 13 (3) (1998) 410–418.

[11] B. Kwon, J. Choi, T. Kim, Improved single-phase line-interactive UPS, IEEE Trans. Ind. Electron. 48 (4) (2001) 804–811.

[12] A. Nasiri, S. Bekiarov, A. Emadi, Reduced parts three-phase series-parallel UPS system with active filter capabilities, in: Proc. IEEE 38th Industry Applications Conference, vol. 2, 2003, pp. 963–969.

[13] S. da Silva, P.F. Donoso-Garcia, P.C. Cortizo, P.F. Seixas, A three-phase line-interactive UPS system implementation with series-parallel active power-line conditioning capabilities, IEEE Trans. Ind. Appl. 38 (6) (2002) 1581–1590.

[14] A. Kuskoand, S. Fairfax, Survey of rotary uninterruptible power supplies, in: Proc. 18th International Telecommunications Energy Conference, 1996, pp. 416–419.

[15] A. Windhorn, A hybrid static/rotary UPS system, IEEE Trans. Ind. Appl. 28 (3) (1992) 541–545.

[16] W.W. Hung, G.W.A. McDowell, Hybrid UPS for standby power systems, Power Eng. J. 4 (6) (1990) 281–291.

[17] S.R. Bowes, Advanced regular-sampled PWM control techniques for drives and static power converters, IEEE Trans. Ind. Electron. 42 (4) (1995) 367–373.

[18] C. Rech, H.A. Grundling, J.R. Pinheiro, Comparison of discrete control techniques for UPS applications, in: Proc. IEEE Industry Applications Conference, 2000, pp. 2531–2537.

[19] J. Chen, C. Chu, Combination voltage-controlled and current-controlled PWM inverters for UPS parallel operation, IEEE Trans. Power Electron. 10 (5) (1995) 547–558.

[20] P. Mattavelli, W. Stefanutti, Fully digital hysteresis modulation with switching time prediction, in: Proc. 19th Applied Power Electronics Conference and Exposition, 2004, pp. 493–499.

[21] P. Mattavelli, An improved deadbeat control for UPS using disturbance observers, IEEE Trans. Ind. Electron. 52 (1) (2005) 206–212.

[22] G.E. Valderrama, A.M. Stankovic, P. Mattavelli, Dissipativity-based adaptive and robust control of UPS in unbalanced operation, IEEE Trans. Power Electron. 18 (4) (2003) 1056–1062.

[23] T. Tai, J. Chen, UPS inverter design using discrete-time sliding-mode control scheme, IEEE Trans. Ind. Electron. 49 (1) (2002) 67–75.
[24] U. Burup, P.N. Enjeti, F. Blaabjerg, A new space-vector-based control method for UPS systems powering nonlinear and unbalanced loads, IEEE Trans. Ind. Appl. 37 (6) (2001) 1864–1870.
[25] N.M. Abdel-Rahim, J.E. Quaicoe, Analysis and design of a multiple feedback loop control strategy for single-phase voltage-source UPS inverters, IEEE Trans. Power Electron. 11 (4) (1996) 532–541.
[26] A. Nasiri, A. Emadi, Digital control of a three-phase series-parallel uninterruptible power supply/active filter system, in: Proc. IEEE 35th Annual Power Electronics Specialists Conference, 2004, pp. 4115–4120.
[27] R. Teodorescu, M. Liserre, P. Rodríguez, Grid Converters for Photovoltaic and Wind Power Systems, John Wiley & Sons, Ltd. ISBN: 978-0-470-05751-3, 2011.
[28] S.A. Hamidi, Dan M. Ionel, Adel Nasiri, Modeling and management of batteries and ultracapacitors for renewable energy support in electric power systems—an overview, J. Electr. Power Compon. Syst. 43 (12) (2015) 1434–1452.

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20

Power Supplies

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20.1 Introduction

Power supplies are used in most electric equipment. Their applications cut across a wide spectrum of product types, ranging from consumer appliances to industrial utilities, from milliwatts to megawatts, and from handheld tools to satellite communications.

By definition, a power supply is a device that converts the output from an ac power line to a steady dc output or multiple outputs. The ac voltage is first rectified to provide a pulsating dc and then filtered to produce a smooth voltage. Finally, the voltage is regulated to produce a constant output level despite variations in the ac line voltage or circuit loading. Fig. 20.1 illustrates the process of rectification, filtering, and regulation in a dc power supply. The transformer, rectifier, and filtering circuits are discussed in other chapters. In this chapter, we will concentrate on the operation and characteristics of the regulator stage of a dc power supply.

In general, the regulator stage of a dc power supply consists of a feedback circuit, a stable reference voltage, and a control circuit to drive a pass element (a solid-state device such as transistor and MOSFET). The regulation is done by sensing variations appearing at the output of the dc power supply. A control signal is produced to drive the pass element to cancel any variation. As a result, the output of the dc power supply is maintained essentially constant. In a transistor regulator, the pass element is a transistor, which can be operated in its active region or as a switch, to regulate the output voltage. When the transistor operates at any point in its active region, the regulator is referred to as a *linear voltage regulator*. When the transistor operates only at cutoff and at saturation, the circuit is referred to as a *switching regulator*.

Linear voltage regulators can be further classified as either series or shunt types. In a series regulator, the pass transistor is connected in series with the load as shown in Fig. 20.2. Regulation is achieved by sensing a portion of the output voltage through the voltage divider network R_1 and R_2 and comparing this voltage with the reference voltage V_{REF} to produce a resulting error signal that is used to control the conduction of the pass transistor. This way, the voltage drop across the pass transistor is varied and the output voltage delivered to the load circuit is essentially maintained constant.

In the shunt regulator shown in Fig. 20.3, the pass transistor is connected in parallel with the load, and a voltage-dropping resistor R_3 is connected in series with the load. Regulation is achieved by controlling the current conduction of the pass transistor such that the current through R_3 remains essentially constant. This way, the current through the pass transistor is varied, and the voltage across the load remains constant.

As opposed to linear voltage regulators, switching regulators employ solid-state devices, which operate as switches: either completely *on* or completely *off*, to perform power conversion. Because the switching devices are not required to operate in their active regions, switching regulators enjoy a much lower

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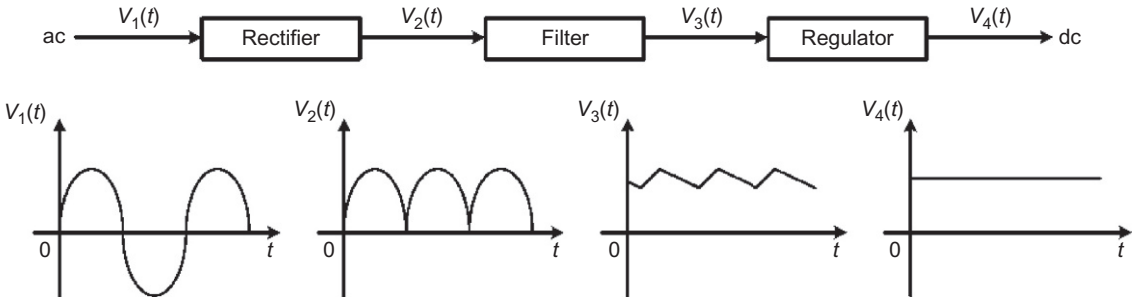


FIG. 20.1 Block diagram of a dc power supply.

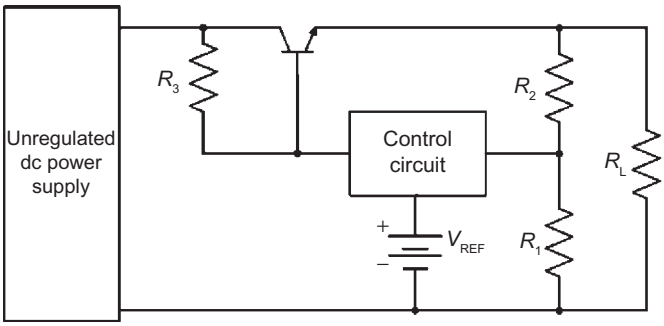


FIG. 20.2 A linear series voltage regulator.

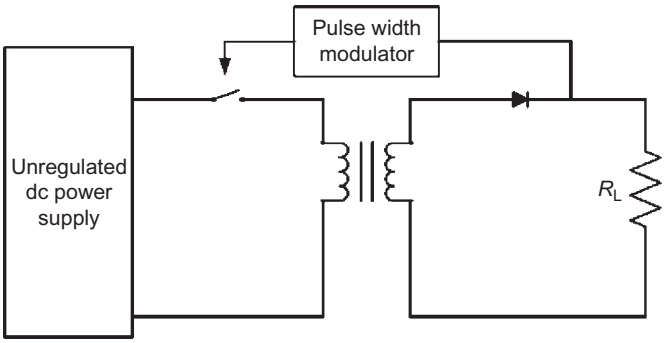


FIG. 20.4 A simplified form of a switching regulator.

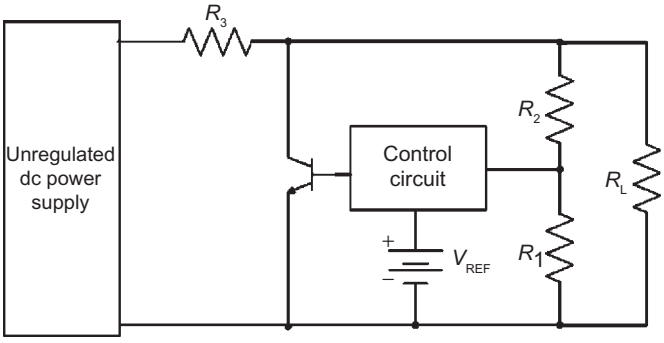


FIG. 20.3 A linear shunt voltage regulator.

power loss than those of linear voltage regulators. Fig. 20.4 shows a switching regulator in a simplified form. The high-frequency switch converts the unregulated dc voltage from one level to another dc level at an adjustable duty cycle. The output of the dc supply is regulated by means of a feedback control that employs a pulse-width modulator (PWM) controller, where the control voltage is used to adjust the duty cycle of the switch.

Both linear and switching regulators are capable of performing the same function of converting an unregulated input into a regulated output. However, these two types of regulators have significant differences in properties and performances. In designing power supplies, the choice of using certain type of regulator in a particular design is significantly based on the cost and performance of the regulator itself. In order to use the more appropriate regulator type in the design, it is necessary to understand the requirements of the application and select the type of regulator that best satisfies those requirements. Advantages and disadvantages of linear regulators, as compared with switching regulators, are given below:

1. Linear regulators exhibit efficiency of 20%–60%, whereas switching regulators have a much higher efficiency, typically 70%–95%.
2. Linear regulators can only be used as a step-down regulator, whereas switching regulators can be used in both step-up and step-down operations.
3. Linear regulators require a mains frequency transformer for off-the-line operation. Therefore, they are heavy and bulky. On the other hand, switching regulators use high-frequency transformers and can therefore be small in size.
4. Linear regulators generate little or no electric noise at their outputs, whereas switching regulators may produce considerable noise if they are not properly designed.
5. Linear regulators are more suitable for applications of less than 20 W, whereas switching regulators are more suitable for large-power applications.

In this chapter, we will examine the circuit operation, characteristics, and applications of linear and switching regulators. In Section **20.2**, we will look at the basic circuits and properties of linear series voltage regulators. Some current-limiting techniques will be explained. In Section **20.3**, linear shunt regulators will be covered. The important characteristics and uses of linear integrated circuit (IC) regulators will be discussed in Section **20.4**. Finally, the operation and characteristics of switching regulators will be discussed in Section **20.5**. Important design guidelines for switching regulators will also be given in this section.

20.2 Linear Series Voltage Regulator

A zener diode regulator can maintain a fairly constant voltage across a load resistor. It can be used to improve the voltage regulation and reduce the ripple in a power supply. However, the regulation is poor, and the efficiency is low because of the nonzero resistance in the zener diode. To improve the regulation and efficiency of the regulator, we have to limit the zener current to a smaller value. This can be accomplished by using an amplifier in series with the load as shown in Fig. 20.5. The effect of this amplifier is to limit the variation of the current I_D through the zener diode D_z. This circuit is known as a linear series voltage regulator because the transistor is in series with the load.

Because of the current-amplifying property of the transistor, I_D is reduced by a factor of $(\beta+1)$, where β is the dc current gain of the transistor. Hence, there is a small voltage drop across the diode resistance, and the zener diode approximates an ideal voltage source. The output voltage V_o of the regulator is

$$V_o = V_z + V_{BE} \tag{20.1}$$

where V_z is the zener voltage and V_{BE} is the base-to-emitter voltage of the transistor. The change in output voltage is

$$\begin{aligned}\Delta V_o &= \Delta V_z + \Delta V_{BE} \\ &= \Delta I_D r_d + \Delta I_L r_e\end{aligned} \tag{20.2}$$

where r_d is the dynamic resistance of the zener diode and r_e is the output resistance of the transistor. Assume that V_i and V_z are constant. With $\Delta I_D \approx \Delta I_L/(\beta+1)$, the change in output voltage is then

$$\Delta V_o \approx \Delta I_L r_e \tag{20.3}$$

If V_i is not constant, then the current I will change with the input voltage. In calculating the change in output voltage, this current change must be absorbed by the zener diode.

In designing linear series voltage regulators, it is imperative that the series transistor must work within the rated safe operation area (SOA) and be protected from excess heat dissipation because of current overload. The emitter-to-collector voltage V_{CE} of Q_1 is given by

$$V_{CE} = V_i - V_o \tag{20.4}$$

Thus, with specified output voltage, the maximum allowable V_{CE} for a given Q_1 is determined by the maximum input voltage to the regulator. The power dissipated by Q_1 can be approximated by

$$P_{Q_1} \approx (V_i - V_o) I_L \tag{20.5}$$

Consequently, the maximum allowable power dissipated in Q_1 is determined by the combination of the input voltage V_i and the load current I_L of the regulator. For a low output voltage and a high loading current regulator, the power dissipated in the series transistor is about 50% of the power delivered to the output.

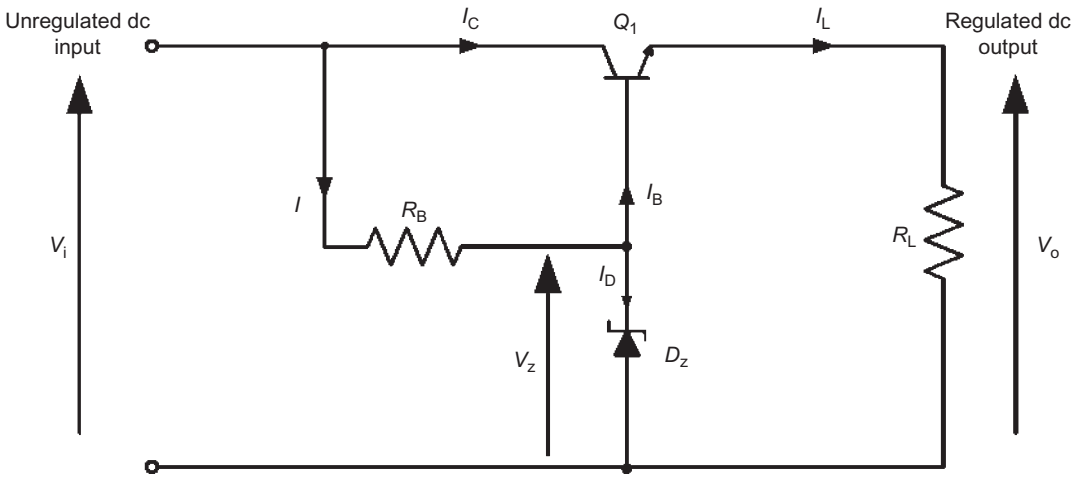


FIG. 20.5 Basic circuit of a linear series regulator.

In many high-current high-voltage regulator circuits, it is necessary to use a Darlington-connected transistor pair so that the voltage, current, and power ratings of the series element are not exceeded. The method is shown in Fig. 20.6. An additional desirable feature of this circuit is that the reference diode dissipation can be reduced greatly. The maximum base current I_{B1} is then $I_L/(\beta_1+1)(\beta_2+1)$, where β_1 and β_2 are the dc current gain of Q_1 and Q_2, respectively. This current is usually of the order of less than 1 mA. Consequently, a low-power reference diode can be used.

20.2.1 Regulating Control

The series regulators shown in Figs. 20.5 and 20.6 do not have feedback loop. Although they provide satisfactory performance for many applications, their output resistances and ripples cannot be reduced. Fig. 20.7 shows an improved form of the series regulator, in which negative feedback is employed to improve the performance. In this circuit, transistors Q_3 and Q_4 form a single-ended differential amplifier, and the gain of this amplifier is established by R_6. Here, D_z is a stable zener diode reference, biased by R_4. For higher accuracy, D_z can be replaced by an IC reference such as REF series from Burr-Brown. Resistors R_1 and R_2 form a voltage divider for output voltage sensing. Finally, transistors Q_1 and Q_2 form a Darlington pair output stage. The operation of the regulator can be explained as follows. When Q_1 and Q_2 are on, the output voltage increases, and hence, the voltage V_A at the base of Q_3 also increases. During this time, Q_3 is off and Q_4 is on. When V_A reaches a level that is equal to the reference voltage V_{REF} at the base of Q_4, the

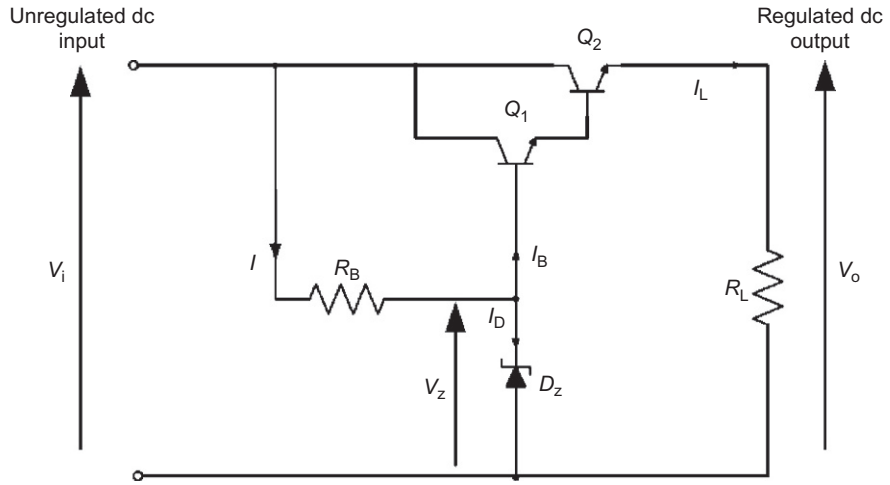


FIG. 20.6 A linear series regulator with Darlington-connected amplifier.

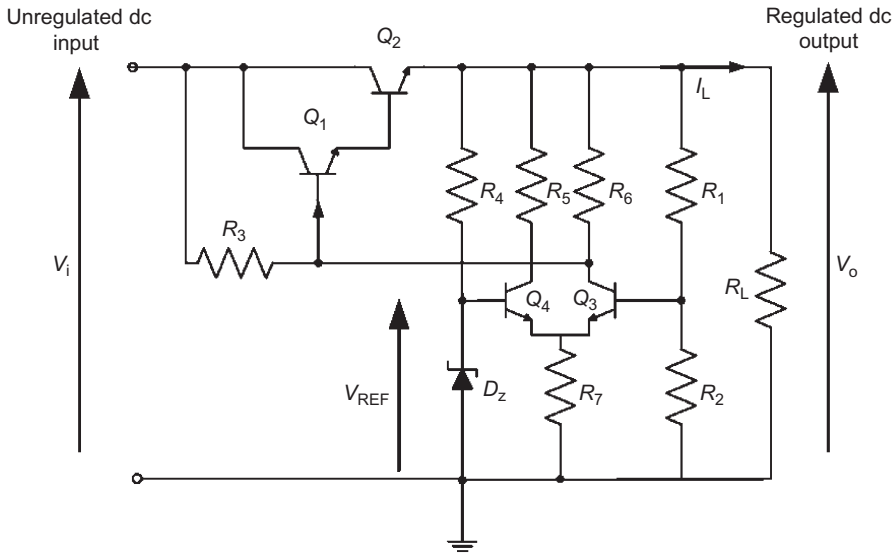


FIG. 20.7 An improved form of discrete component series regulator.

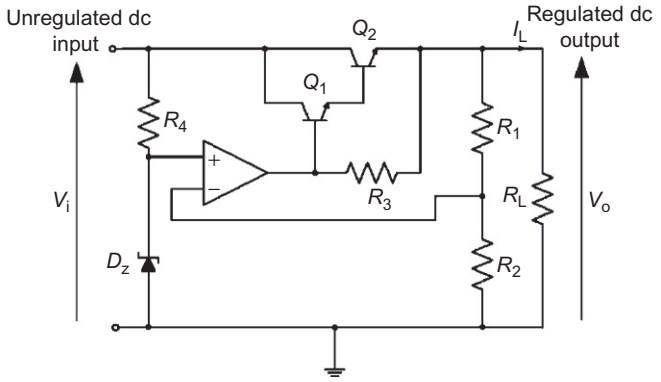


FIG. 20.8 An improved form of op-amp series regulator.

base-emitter junction of Q_3 becomes forward-biased. Some Q_1 base current will divert into the collector of Q_3. If the output voltage V_o starts to rise above V_{REF}, Q_3 conduction increases to further decrease the conduction of Q_1 and Q_2, which will in turn maintain output voltage regulation. Fig. 20.8 shows another improved series regulator that uses an operational amplifier to control the conduction of the pass transistor.

One of the problems in the design of linear series voltage regulators is the high-power dissipation in the pass transistors. If an excess load current is drawn, the pass transistor can be quickly damaged or destroyed. In fact, under short-circuit conditions, the voltage across Q_2 in Fig. 20.7 will be the input voltage V_i, and the current through Q_2 will be greater than the rated full-load output current. This current will cause Q_1 to exceed its rated SOA unless the current is reduced. In the next section, some current-limiting techniques will be presented to overcome this problem.

20.2.2 Current Limiting and Overload Protection

In some series voltage regulators, overloading causes permanent damage to the pass transistors. The pass transistors must be kept from excessive power dissipation under current overloads or short-circuit conditions. A current-limiting mechanism must be used to keep the current through the transistors at a safe value as determined by the power rating of the transistors. The mechanism must be able to respond quickly to protect the transistor and yet permit the regulator to return to normal operation as soon as the overload condition is removed. One of the current-limiting techniques to prevent current overload, called the constant current-limiting method, is shown in Fig. 20.9A. Current limiting is achieved by the combined action of the components shown inside the dashed line. The voltage developed across the current-limit resistor R_3 and the base-to-emitter voltage of current-limit transistor Q_3 is proportional to the circuit output current I_L. During current overload, I_L reaches a predetermined maximum value that is set by the value of R_3 to cause Q_3 to conduct. As Q_3 starts to conduct, Q_3 shunts a portion of the Q_1 base current. This action, in turn, decreases and limits I_L to a maximum value $I_{L(max)}$. Since the base-to-emitter voltage V_{BE} of Q_3 cannot exceed above 0.7 V, the voltage across R_3 is held at this value and $I_{L(max)}$ is limited to

$$I_{L(max)} = \frac{0.7\text{V}}{R_3} \tag{20.6}$$

Consequently, the value of the short-circuit current is selected by adjusting the value of R_3. The voltage-current characteristic of this circuit is shown in Fig. 20.9B.

In many high-current regulators, foldback current limiting is always used to protect against excessive current. This technique is similar to the constant current-limiting method, except that as the output voltage is reduced as a result of load impedance moving toward zero, the load current is also reduced. Therefore, a series voltage regulator that includes a foldback current-limiting circuit has the voltage-current characteristic shown in Fig. 20.10. The basic idea of foldback current limiting, with reference to Fig. 20.11, can be explained as follows. The foldback current-limiting circuit (in dashed outline) is similar to the constant current-limiting circuit, with the exception of resistors R_5 and R_6. At low output current, the current-limit transistor Q_3 is cutoff.

A voltage proportional to the output current I_L is developed across the current-limit resistor R_3. This voltage is applied to the base of Q_3 through the divider network R_5 and R_6. At the point of transition into current limit, any further increase in I_L will increase the voltage across R_3 and hence across R_5, and Q_3 will progressively be turned on. As Q_1 conducts, it shunts a portion of the Q_1 base current. This action, in turn, causes the output voltage to fall. As the output voltage falls, the voltage across R_6 decreases and the current in R_6 also decreases, and more current is shunted into the base of Q_3. Hence, the current required in R_3 to maintain the conduction state of Q_3 is also decreased. Consequently, as the load resistance is reduced, the output voltage and current fall, and the current-limit point decreases toward a minimum when the output voltage is short-circuited. In summary, any regulator using foldback current limiting can have peak load current up to $I_{L(max)}$. But when the output becomes shorted, the current drops to a lower value to prevent overheating of the series transistors.

20.3 Linear Shunt Voltage Regulator

The second type of linear voltage regulator is the shunt regulator. In the basic circuit shown in Fig. 20.12, the pass transistor Q_1 is connected in parallel with the load. A voltage-dropping resistor R_3 is in series with this parallel network. The operation of the circuit is similar to that of the series regulator, except that regulation is achieved by controlling the current through Q_1. The operation of the circuit can be explained as follows. When the output voltage tries to increase because of a change in load

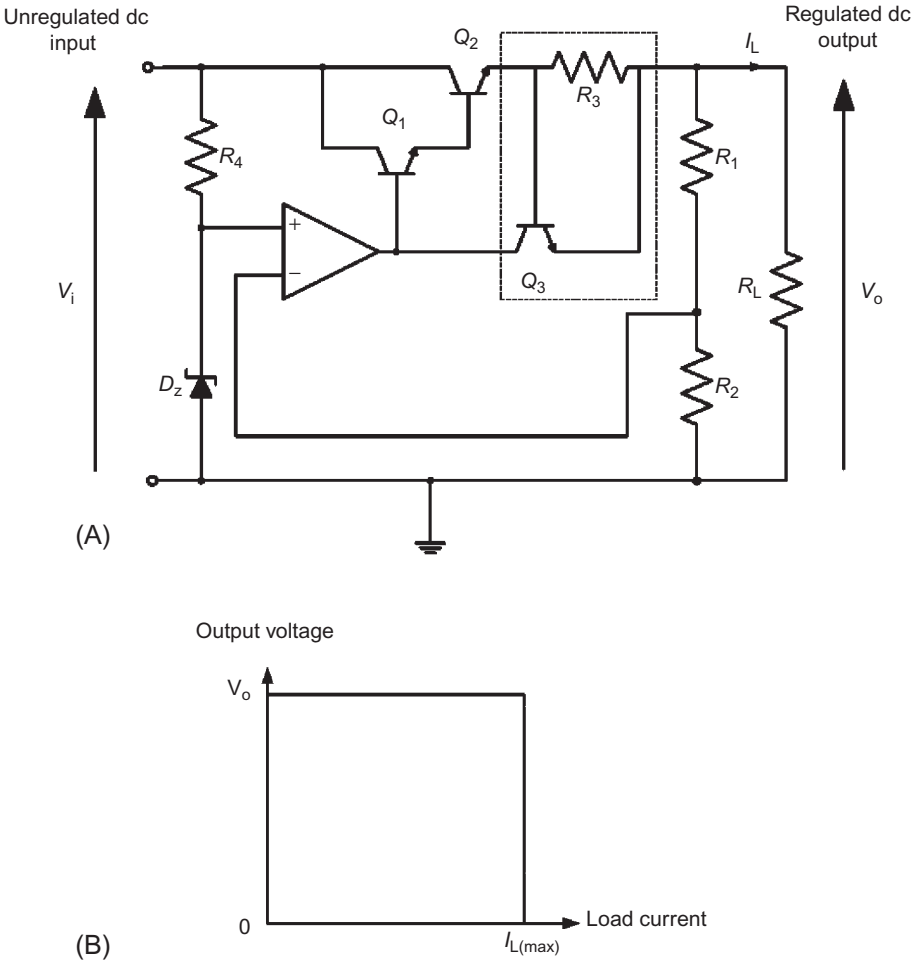


FIG. 20.9 Series regulator with constant current limiting: (A) circuit and (B) voltage-current characteristic.

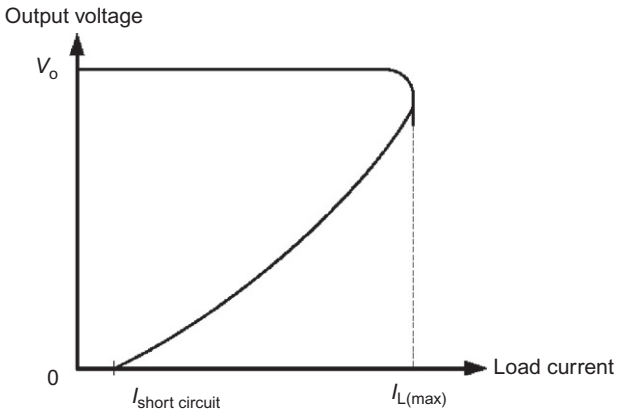


FIG. 20.10 Voltage-current characteristic of foldback current limit.

resistance, the voltage at the noninverting terminal of the operational amplifier also increases. This voltage is compared with a reference voltage, and the resulting difference voltage causes Q_1 conduction to increase. With constant V_i and V_o, I_L will decrease, and V_o will remain constant. The opposite action occurs when V_o tries to decrease. The voltage appearing at the base of Q_1 causes its conduction to decrease. This action offsets the attempted decrease in V_o and maintains it at an almost constant level.

Analytically, the current flowing in R_3 is

$$I_{R3} = I_{Q1} + I_L \tag{20.7}$$

and

$$I_{R3} = \frac{V_i - V_o}{R_3} \tag{20.8}$$

With I_L and V_o constant, a change in V_i will cause a change in I_{Q_1}:

$$\Delta I_{Q1} = \frac{\Delta V_i}{R_3} \tag{20.9}$$

With V_i and V_o constant,

$$\Delta I_{Q1} = -\Delta I_L \tag{20.10}$$

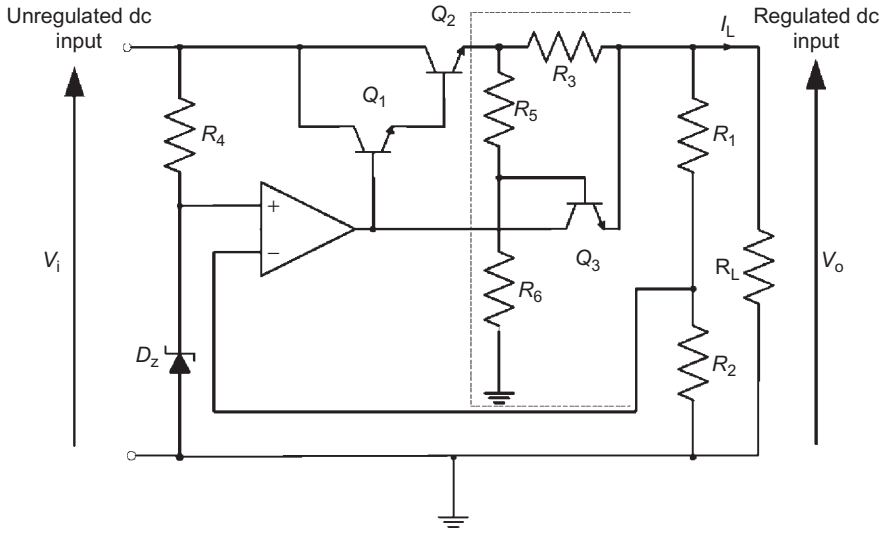


FIG. 20.11 Series regulator with foldback current limiting.

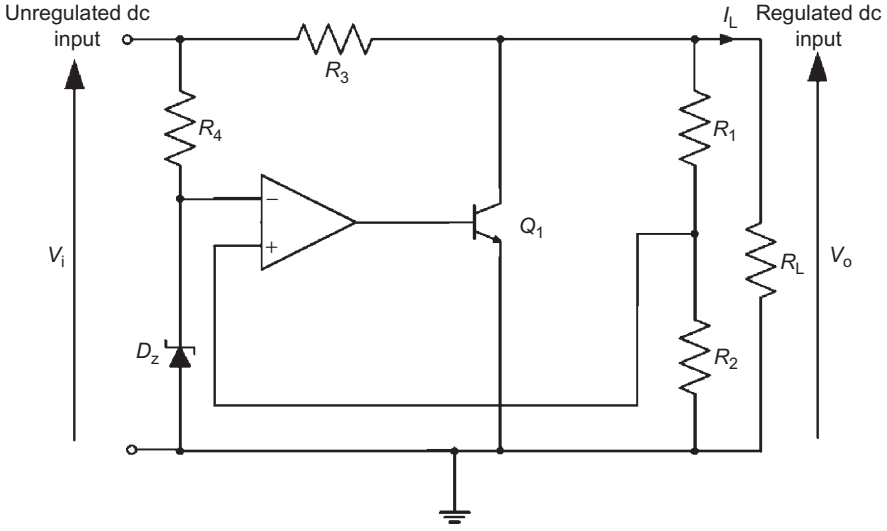


FIG. 20.12 Basic circuit of a linear shunt regulator.

Eq. (20.10) shows that if I_{Q1} increases, I_L decreases and vice versa. Although shunt regulators are not as efficient as series regulators for most applications, they have the advantage of greater simplicity. This topology offers inherently short-circuit protection. If the output is shorted, the load current is limited by the series resistor R_3 and is given by

$$I_{L(max)} = \frac{V_i}{R_3} \tag{20.11}$$

The power dissipated by Q_1 can be approximated by

$$\begin{aligned} P_{Q1} &\approx V_o I_C \\ &= V_o(I_{R3} - I_L) \end{aligned} \tag{20.12}$$

For a low value of I_L, the power dissipated in Q_1 is large, and the efficiency of the regulator may drop to 10% under this condition.

To improve the power handling of the shunt transistor, one or more transistors connected in the common-emitter configuration in parallel with the load can be employed, as shown in Fig. 20.13.

20.4 Integrated Circuit Voltage Regulators

The linear series and shunt voltage regulators presented in the previous sections have been developed by various solid-state

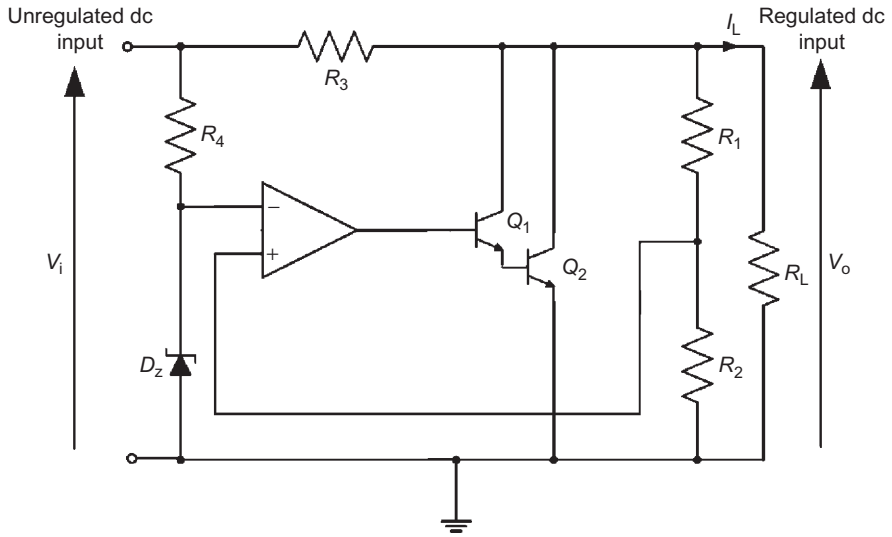


FIG. 20.13 Linear shunt regulator with two transistors as shunt element.

device manufacturers and are available in integrated circuit (IC) form. Like discrete voltage regulators, linear IC voltage regulators maintain an output voltage at a constant value despite variations in load and input voltage.

In general, linear IC voltage regulators are three-terminal devices that provide regulation of a fixed positive voltage, a fixed negative voltage, or an adjustable set voltage. The basic connection of a three-terminal IC voltage regulator to a load is shown in Fig. 20.14. The IC regulator has an unregulated input voltage V_i applied to the input terminals, a regulated voltage V_o at the output, and a ground connected to the third terminal. Depending on the selected IC regulator, the circuit can be operated with load currents ranging from milliamperes to tens of amperes and output power from milliwatts to tens of watts. Note that the internal construction of IC voltage regulators may be somewhat more complex and different from that previously described for discrete voltage regulator circuits. However, the external operation is much the same. In this section, some typical linear IC regulators are presented, and their applications are also given.

20.4.1 Fixed Positive and Negative Linear Voltage Regulators

The 78XX series of regulators provide fixed regulated voltages from 5 to 24 V. The last two digits of the IC part number denote the output voltage of the device. For example, a 7824 IC regulator produces a +24 V regulated voltage at the output. The standard configuration of a 78XX fixed positive voltage regulator is shown in Fig. 20.15. The input capacitor C_1 acts as a line filter to prevent unwanted variations in the input line, and the output capacitor C_2 is used to filter the high-frequency noise that may appear at the output. In order to ensure proper operation, the input voltage of the regulator must be at least 2 V above the output voltage. Table 20.1 shows the minimum and maximum input voltages of the 78XX series fixed positive voltage regulator.

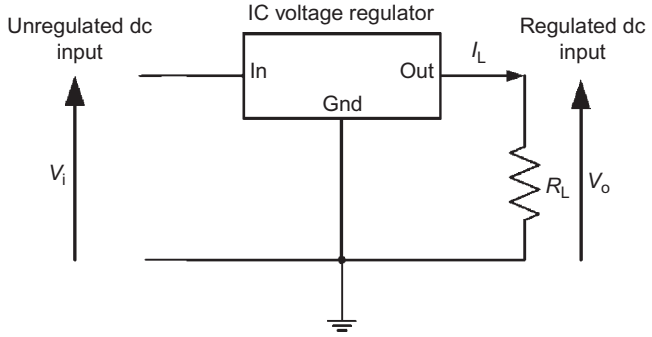


FIG. 20.14 Basic connection of a three-terminal IC voltage regulator.

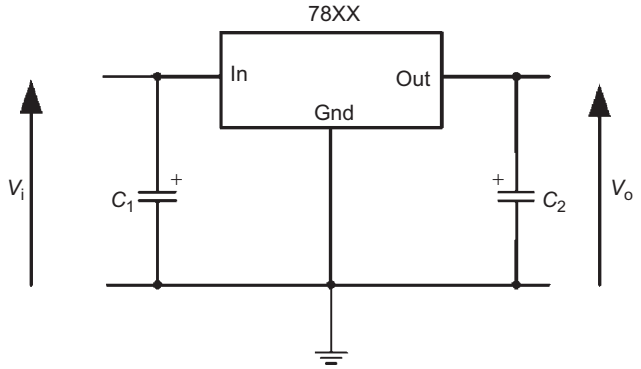


FIG. 20.15 The 78XX series fixed positive voltage regulator.

TABLE 20.1 Minimum and maximum input voltages for 78XX series regulators

Type number	Output voltage V_o (V)	Minimum V_i (V)	Maximum V_i (V)
7805	+5	7	20
7806	+6	8	21
7808	+8	10.5	25
7809	+9	11.5	25
7812	+12	14.5	27
7815	+15	17.5	30
7818	+18	21	33
7824	+24	27	38

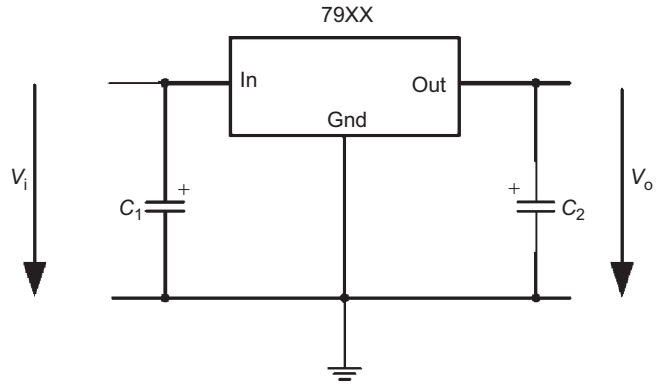


FIG. 20.16 The 79XX series fixed negative voltage regulator.

TABLE 20.2 Minimum and maximum input voltages for 79XX series regulators

Type number	Output voltage V_o (V)	Minimum V_i (V)	Maximum V_i (V)
7805	−5	−7	−20
7806	−6	−8	−21
7808	−8	−10.5	−25
7809	−9	−11.5	−25
7812	−12	−14.5	−27
7815	−15	−17.5	−30
7818	−18	−21	−33
7824	−24	−27	−38

The 79XX series voltage regulator is identical to the 78XX series except that it provides negative regulated voltages instead of positive ones. Fig. 20.16 shows the standard configuration of a 79XX series voltage regulator. A list of 79XX series regulators is provided in Table 20.2. The regulation of the circuit can be maintained as long as the output voltage is at least 2–3 V greater than the input voltage.

20.4.2 Adjustable Positive and Negative Linear Voltage Regulators

The IC voltage regulators are also available in circuit configurations that allow the user to set the output voltage to a desired

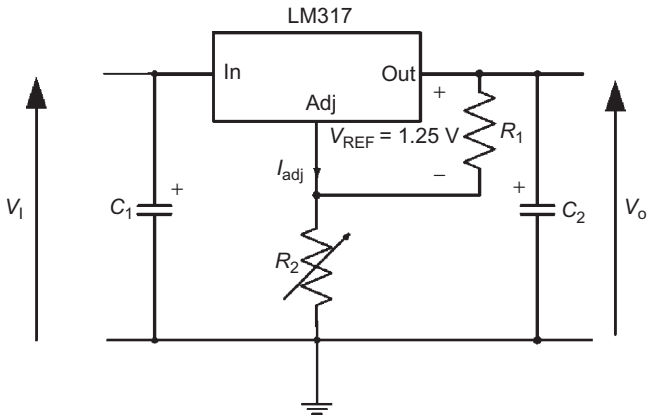


FIG. 20.17 The LM317 adjustable positive voltage regulator.

regulated value. The LM317 adjustable positive voltage regulator, for example, is capable of supplying an output current of more than 1.5 A over an output voltage range of 1.2–37 V. Fig. 20.17 shows how the output voltage of an LM317 can be adjusted by using two external resistors R_1 and R_2. The capacitors C_1 and C_2 have the same function as those in the fixed linear voltage regulator.

As indicated in Fig. 20.17, the LM317 has a constant 1.25 V reference voltage, V_{REF}, across the output and the adjustment terminals. This constant reference voltage produces a constant current through R_1 regardless of the value of R_2. The output voltage V_o is given by

$$V_o = V_{REF}\left(1 + \frac{R_2}{R_1}\right) + I_{adj}R_2 \tag{20.13}$$

where I_{adj} is a constant current into the adjustment terminal and has a value of approximately 50 μA for the LM317. As can be seen from Eq. (20.13), with fixed R_1, V_o can be adjusted by varying R_2.

The LM337 adjustable voltage regulator is similar to the LM317 except that it provides negative regulated voltages instead of positive ones. Fig. 20.18 shows the standard configuration of an LM337 voltage regulator. The output voltage can

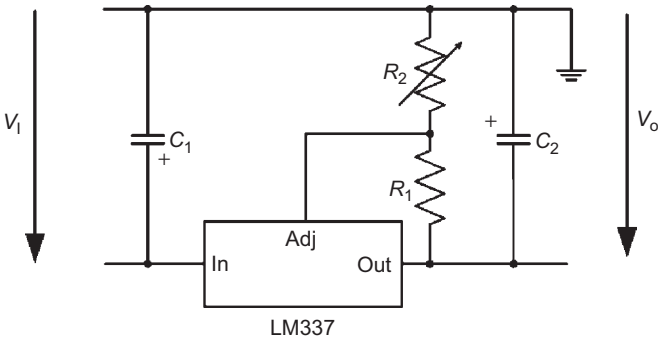


FIG. 20.18 The LM337 adjustable negative voltage regulator.

be adjusted from −1.2 to −37 V, depending on the external resistors R_1 and R_2.

20.4.3 Applications of Linear IC Voltage Regulators

Most IC regulators are limited to an output current of 2.5 A. If the output current of an IC regulator exceeds its maximum allowable limit, its internal pass transistor will dissipate an amount of energy more than it can tolerate. As a result, the regulator will be shutdown.

For applications that require more than the maximum allowable current limit of a regulator, an external pass transistor can be used to increase the output current. Fig. 20.19 illustrates such a configuration. This circuit has the capability of producing higher current to the load but still preserving the thermal shutdown and short-circuit protection of the IC regulator.

A constant current-limiting scheme, as discussed in Section 20.2.2, is implemented by using the transistor Q_2 and the resistor R_2 to protect the external pass transistor Q_1 from excessive current under current-overload or short-circuit conditions. The value of the external current-sensing resistor R_1 determines the value of current at which Q_1 begins to conduct. As long as the current is less than the value set by R_1, the transistor Q_1 is off, and the regulator operates normally as shown in Fig. 20.15. But when the load current I_L starts to increase, the voltage across R_1 also increases. This turns on the external transistor Q_1 and conducts the excess current. The value of R_1 is determined by

$$R_1 = \frac{0.7\text{V}}{I_{\max}} \tag{20.14}$$

where $I_{\max}$ is the maximum current that the voltage regulator can handle internally.

20.5 Switching Regulators

The linear series and shunt regulators have control transistors that are operating in their linear active regions. Regulation is achieved by varying the conduction of the transistors to maintain the output voltage at a desirable level. The switching regulator is different in that the control transistor operates as a switch, either in cutoff or saturation region. Regulation is achieved by adjusting the on-time of the control transistor. In this mode of operation, the control transistor does not dissipate as much power as that in the linear types. Therefore, switching voltage regulators have a much higher efficiency and can provide greater load currents at low voltage than linear regulators.

Unlike their linear counterparts, switching regulators can be implemented by many different topologies such as forward and flyback. In order to select an appropriate topology for an application, it is necessary to understand the merits and drawbacks of each topology and the requirements of the application. Basically, most topologies can work for various applications. Therefore, we have to determine from the factors such as cost, performances, and application that make one topology more desirable than the others. However, no matter which topology we decide to use, the basic building blocks of an off-the-line switching power supply are the same, as depicted in Fig. 20.1.

In this section, some popular switching regulator topologies, namely, flyback, forward, half-bridge, and full-bridge topologies, are presented. Their basic operation is described, and the critical waveforms are shown and explained. The merits, drawbacks, and application areas of each topology are discussed. Finally, the control circuitry and PWM of the regulators will also be discussed.

20.5.1 Single-Ended Isolated Flyback Regulators

An isolated flyback regulator consists of four main circuit elements: a power switch, a rectifier diode, a transformer, and a filter capacitor. The power switch, which can be either a power transistor or a MOSFET, is used to control the flow of energy in the circuit. A transformer is placed between the input source and the power switch to provide dc isolation between the input and the output circuits. In addition to being an energy storage element, the transformer also performs a stepping up or down function for the regulator. The rectifier diode and filter

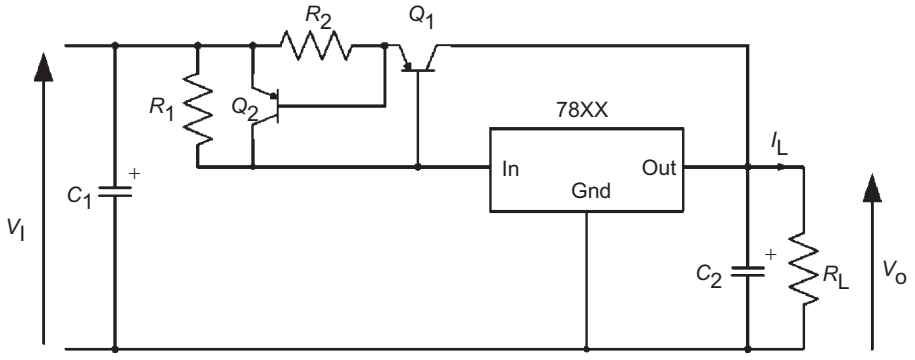


FIG. 20.19 A 78XX series regulator with an external pass transistor.

capacitor form an energy transfer mechanism to supply energy to maintain the output voltage of the supply. Note that there are two distinct operating modes for flyback regulators: *continuous* and *discontinuous*. However, both modes have an identical circuit. It is only the transformer magnetizing current that determines the operating mode of the regulator. Fig. 20.20A shows a simplified isolated flyback regulator. The associated steady-state waveforms, resulting from a discontinuous-mode operation, are shown in Fig. 20.20B. As shown in the figure, the voltage regulation of the regulator is achieved by a control circuit, which controls the conduction period or duty cycle of the switch, to keep the output voltage at a constant level. For clarity, the schematics and operation of the control circuit will be discussed in a separate section.

20.5.1.1 Discontinuous-Mode Flyback Regulators

Under steady-state conditions, the operation of the regulator can be explained as follows. When the power switch Q_1 is on, the primary current I_p starts to build up and stores energy in the primary winding. Because of the opposite polarity arrangement between the input and output windings of the transformer, the rectifier diode D_R is reverse-biased. In this period of time, there is no energy transferred from the input to the load R_L. The output voltage is supported by the load current I_L, which is supplied from the output filter capacitor C_F. When Q_1 is turned off, the polarity of the windings reverses as a result of the fact that I_p cannot change instantaneously. This causes D_R to turn on. Now, D_R is conducting, charging the output capacitor C_F, and delivering current to R_L. This charging action ends at the point where all the magnetic energy stored in the secondary winding during the first half cycle is emptied. At this point, D_R will cease to conduct and R_L absorbs energy just from C_F until Q_1 is switched on again.

During the Q_1 on-time, the voltage across the primary winding of the transformer is V_i. The current in the primary winding I_p increases linearly and is given by

$$I_p = \frac{V_i t_{on}}{L_p} \tag{20.15}$$

where L_p is the primary magnetizing inductance. At the end of the on-time, the primary current reaches a value equal to $I_{p(pk)}$ and is given by

$$I_{p(pk)} = \frac{V_i D T}{L_p} \tag{20.16}$$

where D is the duty cycle and T is the switching period. Now, when Q_1 turns off, the magnetizing current in the transformer forces the reversal of polarities on the windings. At the instant of turnoff, the amplitude of the secondary current $I_{s(pk)}$ is

$$I_{s(pk)} = \left(\frac{N_p}{N_s}\right) I_{p(pk)} \tag{20.17}$$

This current decreases linearly at the rate of

$$\frac{dI_s}{dt} = \frac{V_o}{L_s} \tag{20.18}$$

where L_s is the secondary magnetizing inductance.

In the discontinuous-mode operation, $I_{s(pk)}$ will decrease linearly to zero before the start of the next cycle. Since the energy transfer from the source to the output takes place only in the first half cycle, the power drawn from V_i is then

$$P_{in} = \frac{L_p I_p^2}{2T} \tag{20.19}$$

Substituting Eq. (20.15) into Eq. (20.19), we have

$$P_{in} = \frac{(V_i t_{on})^2}{2TL_p} \tag{20.20}$$

The output power P_o may be written as

$$\begin{aligned} P_o &= \eta P_{in} \\ &= \frac{\eta (V_i t_{on})^2}{2TL_p} = \frac{V_o^2}{R_L} \end{aligned} \tag{20.21}$$

where η is the efficiency of the regulator. Then, from Eq. (20.21), the output voltage V_o is related to the input voltage V_i by

$$V_o = V_i D \sqrt{\frac{\eta R_L T}{2L_p}} \tag{20.22}$$

Since the collector voltage V_{Q1} of Q_1 is maximum when V_i is maximum, the maximum collector voltage $V_{Q1(max)}$, as shown in Fig. 20.20B, is given by

$$V_{Q1(max)} = V_{i(max)} + \left(\frac{N_p}{N_s}\right) V_o \tag{20.23}$$

The primary peak current $I_{p(pk)}$ can be found in terms of P_o by combining Eq. (20.16) and Eq. (20.21) and then eliminating L_p as

$$\begin{aligned} I_{p(pk)} &= \frac{2V_o^2}{\eta V_i D R_L} \\ &= \frac{2P_o}{\eta V_i D} \end{aligned} \tag{20.24}$$

The maximum collector current $I_{C(max)}$ of the power switch Q_1 at turn on is

$$\begin{aligned} I_{C(max)} &= I_{p(pk)} \\ &= \frac{2P_o}{\eta V_i D} \end{aligned} \tag{20.25}$$

As can be seen from Eq. (20.21), V_o will be maintained constant by keeping the product $V_i t_{on}$ constant. Since maximum

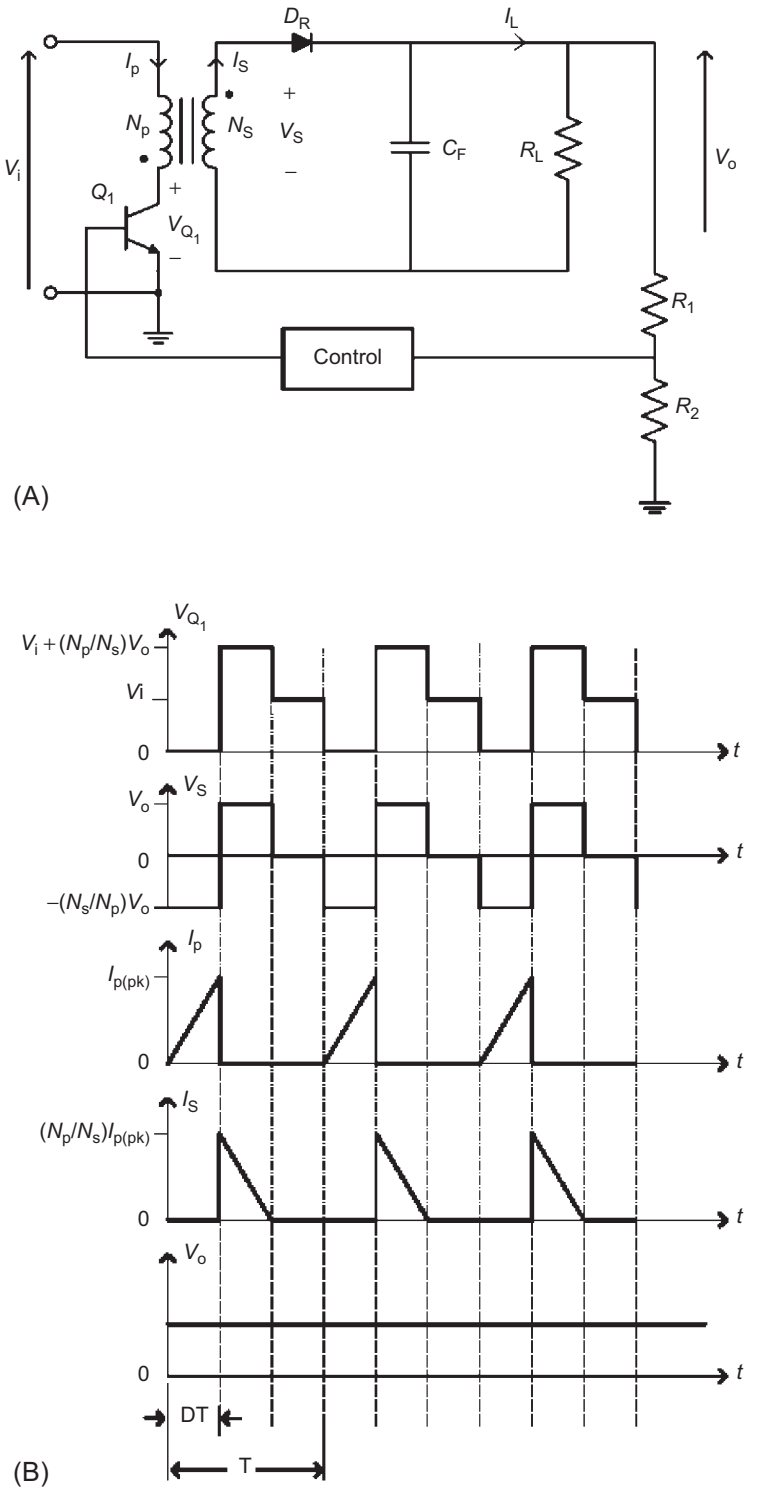


FIG. 20.20 A simplified isolated flyback regulator: (A) circuit and (B) the associated waveforms.

on-time $t_{on(max)}$ occurs at minimum supply voltage $V_{i(min)}$, the maximum allowable duty cycle for the discontinuous mode can be found from Eq. (20.22) as

$$D_{max} = \frac{V_o}{V_{i(min)}}\sqrt{\frac{2L_p}{\eta R_L T}} \tag{20.26}$$

and V_o at D_{max} is then

$$V_o = V_{i(min)} D_{max}\sqrt{\frac{\eta R_L T}{2L_p}} \tag{20.27}$$

20.5.1.2 Continuous-Mode Flyback Regulators

In the continuous-mode operation, the power switch is turned on before all the magnetic energy stored in the secondary winding empties itself. The primary and secondary current waveforms have a characteristic appearance as shown in Fig. 20.21. This mode produces a higher-power capability without increasing the peak currents. During the on-time, the primary current I_p rises linearly from its initial value $I_p(0)$ and is given by

$$I_p = I_p(0) + \frac{V_i t_{on}}{L_p} \tag{20.28}$$

At the end of the on-time, the primary current reaches a value equal to $I_{p(pk)}$ and is given by

$$I_{p(pk)} = I_p(0) + \frac{V_i DT}{L_p} \tag{20.29}$$

In general, $I_p(0) \gg V_i DT/L_p$; thus, Eq. (20.29) can be written as

$$I_{p(pk)} \approx I_p(0) \tag{20.30}$$

The secondary current I_s at the instant of turn off is given by

$$\begin{aligned} I_{s(pk)} &= \left(\frac{N_p}{N_s}\right) I_{p(pk)} \\ &= \left(\frac{N_p}{N_s}\right)\left(I_p(0) + \frac{V_i DT}{L_p}\right) \\ &\approx \left(\frac{N_p}{N_s}\right) I_p(0) \end{aligned} \tag{20.31}$$

This current decreases linearly at the rate of

$$\frac{dI_s}{dt} = \frac{V_o}{L_s} \tag{20.32}$$

The output power P_o is equal to V_o times the time average of the secondary current pulses and is given by

$$\begin{aligned} P_o &= V_o I_s \frac{T - t_{on}}{T} \\ &\approx V_o I_{s(pk)} \frac{T - t_{on}}{T} \end{aligned} \tag{20.33}$$

or

$$I_{s(pk)} = \frac{P_o}{V_o(1 - t_{on}/T)} \tag{20.34}$$

For an efficiency of η, the input power P_{in} is

$$\begin{aligned} P_{in} &= \frac{P_o}{\eta} \\ &= V_i I_p \frac{t_{on}}{T} \\ &\approx V_i I_{p(pk)} \frac{t_{on}}{T} \end{aligned} \tag{20.35}$$

or

$$I_{p(pk)} = \frac{P_o}{\eta V_i (t_{on}/T)} \tag{20.36}$$

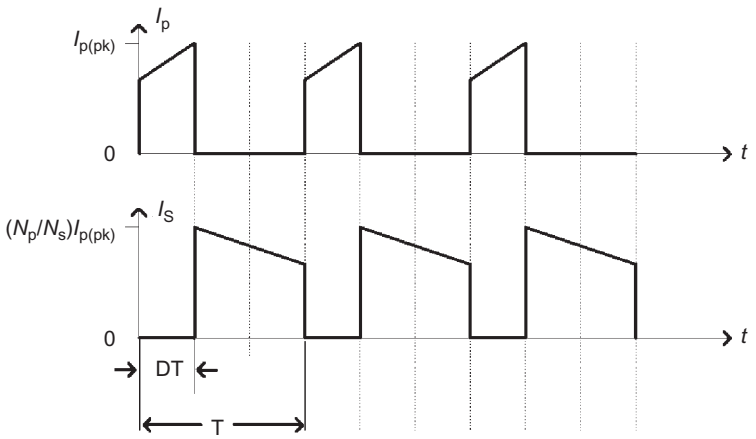


FIG. 20.21 The primary and secondary winding currents of a flyback regulator operated in the continuous mode.

Combining Eqs. (20.31), (20.34), and (20.36) and solving for V_o, we have

$$V_o = \left(\frac{N_s}{N_p}\right)\frac{\eta V_i D}{1-D} \tag{20.37}$$

The output voltage at D_{max} is then

$$V_o = \left(\frac{N_s}{N_p}\right)\frac{\eta V_{i(min)} D_{max}}{1-D_{max}} \tag{20.38}$$

The maximum collector current $I_{C(max)}$ for the continuous mode is then given by

$$\begin{aligned} I_{C(max)} &= I_{p(pk)} \\ &= \frac{P_o}{\eta V_i D_{max}} \end{aligned} \tag{20.39}$$

The maximum collector voltage of Q_1 is the same as that in the discontinuous mode and is given by

$$V_{Q1(max)} = V_{i(max)} + \left(\frac{N_p}{N_s}\right)V_o \tag{20.40}$$

The maximum allowable duty cycle for the continuous mode can be found from Eq. (20.38) and is given by

$$D_{max} = \frac{1}{1+\left(\frac{N_s}{N_p}\right)\frac{\eta V_{i(min)}}{V_o}} \tag{20.41}$$

At the transition from the discontinuous mode to continuous mode (or from continuous mode to discontinuous mode), the relationships in Eqs. (20.27) and (20.38) must hold. Thus, equating these two equations, we have

$$V_{i(min)} D_{max}\sqrt{\frac{\eta R_L T}{2L_p}} = \frac{N_s}{N_p}\frac{D_{max}}{1-D_{max}}\eta V_{i(min)} \tag{20.42}$$

Solving this equation for L_p to give the critical inductance $L_{p(limit)}$, at which the transition occurs, we have

$$\begin{aligned} L_{p(limit)} &= \frac{1}{2\eta}TR_L\left[(1-D_{max})\frac{N_p}{N_s}\right]^2 \\ &= \frac{1}{2\eta}T\frac{V_o^2}{P_o}\left[(1-D_{max})\frac{N_p}{N_s}\right]^2 \end{aligned} \tag{20.43}$$

Replacing V_o with Eq. (20.38) and solving for $L_{p(limit)}$, we have

$$L_{p(limit)} = \frac{1}{2}\eta T\frac{D_{max}^2 V_{i(min)}^2}{P_o} \tag{20.44}$$

Then, for a given D_{max}, input, and output quantities, the inductance value $L_{p(limit)}$ in Eq. (20.44) determines the mode of operation for the regulator. If $L_p < L_{p(limit)}$, then the circuit is operated in the discontinuous mode. Otherwise, if $L_P > L_{p(limit)}$, the circuit is operated in the continuous mode.

In designing flyback regulators, regardless of their operating modes, the power switch must be able to handle the peak collector voltage at turnoff and the peak collector currents at turnon as shown in Eqs. (20.23), (20.25), (20.39), and (20.40). The flyback transformer, because of its unidirectional use of the *B-H* curve, has to be designed so that it will not be driven into saturation. To avoid saturation, the transformer needs a relatively large core with an air gap in it.

Although the continuous and discontinuous modes have an identical circuit, their operating properties differ significantly. As opposed to the discontinuous mode, the continuous mode can provide higher-power capability without increasing the peak current $I_{p(pk)}$. It means that, for the same output power, the peak currents in the discontinuous mode are much higher than those operated in the continuous mode. As a result, a higher current rating and, therefore, a more expensive power transistor are needed. Moreover, the higher secondary peak currents in the discontinuous mode will have a larger transient spike at the instant of turnoff. However, despite all these problems, the discontinuous mode is still much more widely used than its continuous-mode counterpart. There are two main reasons. First, the inherently smaller magnetizing inductance gives the discontinuous mode a quicker response and a lower transient output voltage spike to sudden changes in load current or input voltage. Second, the continuous mode has a right-half-plane zero in its transfer function, which makes the feedback control circuit more difficult to design.

The flyback configuration is mostly used in applications with output power below 100 W. It is widely used for high output voltages at relatively low power. The essential attractions of this configuration are its simplicity and low cost. Since no output filter inductor is required for the secondary, there is a significant saving in cost and space, especially for multiple output power supplies. Since there is no output filter inductor, the flyback exhibits high ripple currents in the transformer and at the output. Thus, for higher-power applications, the flyback becomes an unsuitable choice. In practice, a small *LC* filter is added after the filter capacitor C_F in order to suppress high-frequency switching noise spikes.

As mentioned previously, the collector voltage of the power transistor must be able to sustain a voltage as defined in Eq. (20.23). In cases where the voltage is too high for the transistor to handle, the double-ended flyback regulator shown in Fig. 20.22 may be used. The regulator uses two transistors that are switched on or off simultaneously. The diodes D_{R1} and D_{R2} are used to restrict the maximum collector voltage to V_i. Therefore, the transistors with a lower voltage rating can be used in the circuit.

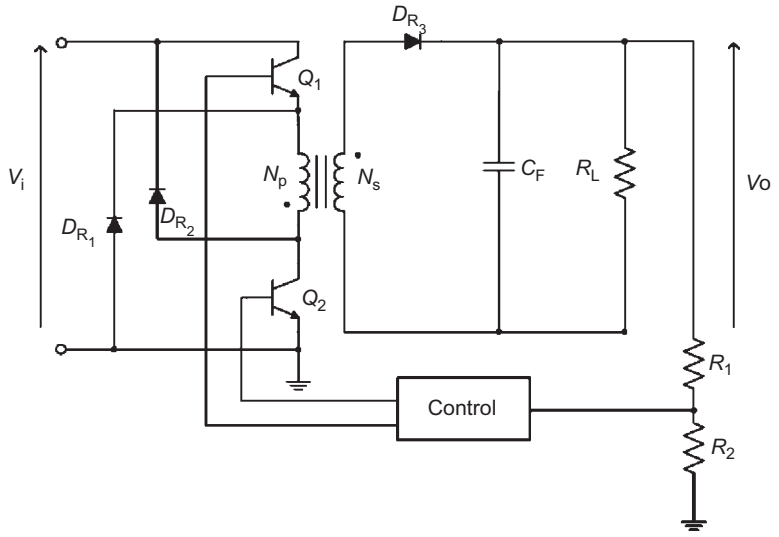


FIG. 20.22 A double-ended flyback regulator.

20.5.2 Single-Ended Isolated Forward Regulators

Although the general appearance of an isolated forward regulator resembles that of its flyback counterpart, their operations are different. The key difference is that the dot on the secondary winding of the transformer is so arranged that the output diode is forward-biased when the voltage across the primary is positive, that is, when the transistor is *on*. Energy is thus not stored in the primary inductance as it was for the flyback. The transformer acts strictly as a transformer. An inductive energy storage element is required at the output for proper and efficient energy transfer.

Unlike the flyback, the forward regulator is very suitable for working in the continuous mode. In the discontinuous mode, the forward regulator is more difficult to control because of a double pole at the output filter. Thus, it is not as much used as the continuous mode. In view of it, only the continuous mode will be discussed here.

Fig. 20.23 shows a simplified isolated forward regulator and the associated steady-state waveforms for the continuous-mode operation. Again, for clarity, the details of the control circuit are omitted from the figure. Under steady-state condition, the operation of the regulator can be explained as follows. When the power switch Q_1 turns on, the primary current I_p starts to build up and stores energy in the primary winding. Because of the same polarity arrangement of the primary and secondary windings, this energy is forward transferred to the secondary and onto the L_1C_F filter and the load R_L through the rectifier diode D_{R2}, which is forward-biased. When Q_1 turns off, the polarity of the transformer winding voltage reverses. This causes D_{R2} to turn off and D_{R1} and D_{R3} to turn on. Now, D_{R3} is conducting and delivering energy to R_L through the inductor L_1. During this period, the diode D_{R2} and the tertiary winding provide a path for the magnetizing current returning to the input.

When the transistor Q_1 is turned on, the voltage across the primary winding is V_i. The secondary winding current is reflected into the primary, and the reaction current I_p, as shown in Fig. 20.24, is given by

$$I_p = \frac{N_s}{N_p} I_s \tag{20.45}$$

The magnetizing current in the primary has a magnitude of I_{mag} and is given by

$$I_{mag} = \frac{V_i t_{on}}{L_p} \tag{20.46}$$

The total primary current I_p' is then

$$\begin{aligned} I_p' &= I_p + I_{mag} \\ &= \frac{N_s}{N_p} I_s + \frac{V_i t_{on}}{L_p} \end{aligned} \tag{20.47}$$

The voltage developed across the secondary winding V_s is

$$V_s = \frac{N_s}{N_p} V_i \tag{20.48}$$

Neglecting diode voltage drops and losses, the voltage across the output inductor is $V_s - V_o$. The current in L_1 increases linearly at the rate of

$$I_{L1} = \frac{(V_s - V_o) t_{on}}{L_1} \tag{20.49}$$

At the end of the on-time, the total primary current reaches a peak value equal to $I'_{p(pk)}$ and is given by

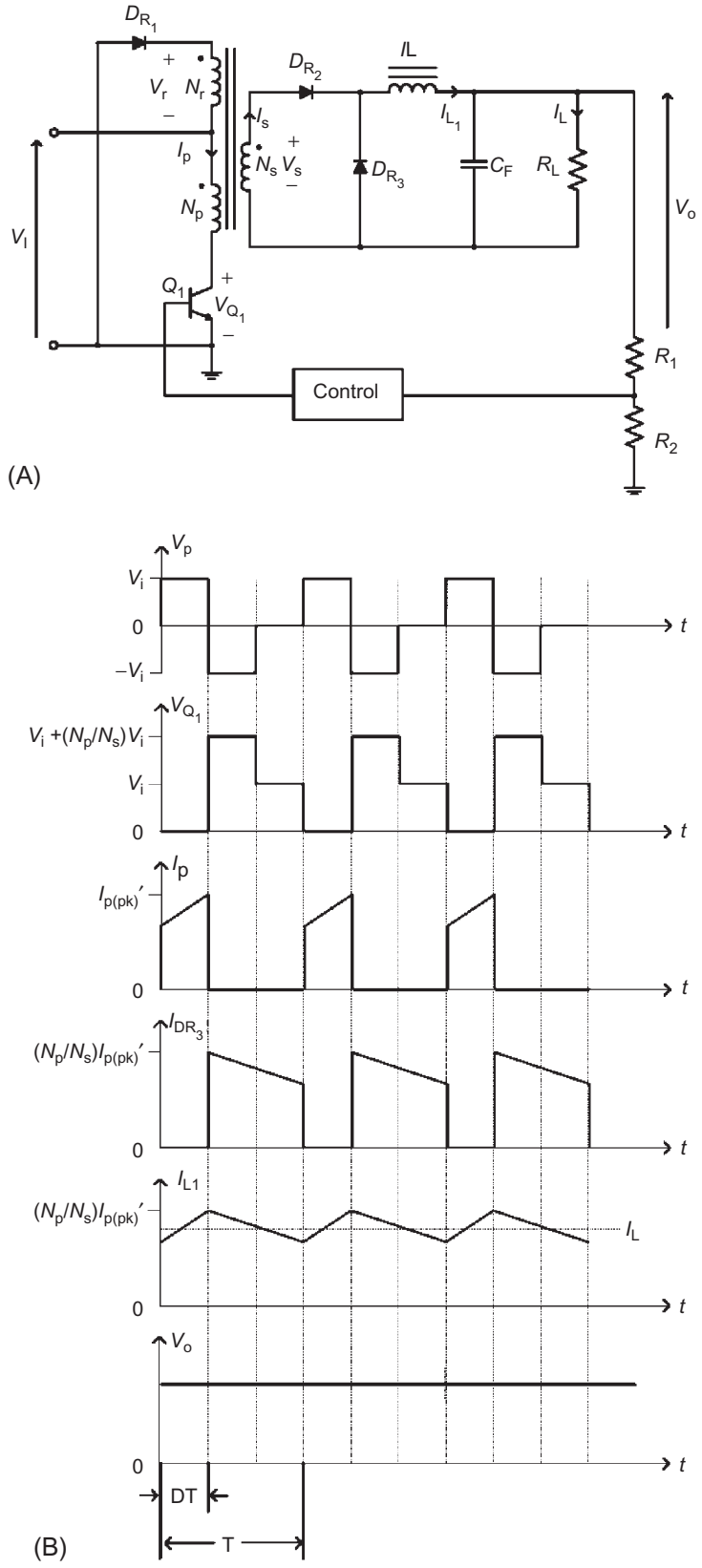


FIG. 20.23 A simplified isolated forward regulator: (A) circuit and (B) the associated waveforms.

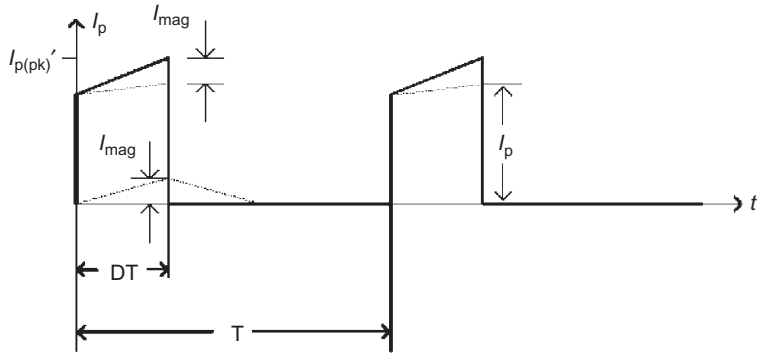


FIG. 20.24 The current components in the primary winding.

$$I'_{p(pk)} = I'_p(0) + \frac{V_i DT}{L_p} \tag{20.50}$$

The output inductor current I_{L1} is

$$I_{L1(pk)} = I_{L1}(0) + \frac{(V_s - V_o)DT}{L_1} \tag{20.51}$$

At the instant of turn-on, the amplitude of the secondary current has a value of $I_{s(pk)}$ and is given by

$$\begin{aligned} I_{s(pk)} &= \left(\frac{N_p}{N_s}\right) I'_{p(pk)} \\ &= \left(\frac{N_p}{N_s}\right)\left[I'_p(0) + \frac{V_i DT}{L_p}\right] \end{aligned} \tag{20.52}$$

During the off-time, the current I_{L1} in the output inductor is equal to the current I_{DR3} in the rectifier diode D_{R3}, and both decrease linearly at the rate of

$$\begin{aligned} \frac{dI_{L1}}{dt} &= \frac{dI_{DR3}}{dt} \\ &= \frac{V_o}{L_1} \end{aligned} \tag{20.53}$$

The output voltage V_o can be found from the time integral of the secondary winding voltage over a time equal to DT of the switch Q_1. Thus, we have

$$\begin{aligned} V_o &= \frac{1}{T}\int_0^{DT} \frac{N_s}{N_p} V_i dt \\ &= \frac{N_s}{N_p} V_i D \end{aligned} \tag{20.54}$$

The maximum collector current $I_{C(max)}$ at turn-on is equal to $I'_{p(pk)}$ and is given by

$$\begin{aligned} I_{C(max)} &= I'_{p(pk)} \\ &= \left(\frac{N_s}{N_p}\right)\left[I'_p(0) + \frac{V_i DT}{L_p}\right] \end{aligned} \tag{20.55}$$

The maximum collector voltage $V_{Q_1(max)}$ at turnoff is equal to the maximum input voltage $V_{i(max)}$ plus the maximum voltage $V_{r(max)}$ across the tertiary winding and is given by

$$\begin{aligned} V_{Q_1(max)} &= V_{i(max)} + V_{r(max)} \\ &= V_{i(max)}\left(1 + \frac{N_p}{N_r}\right) \end{aligned} \tag{20.56}$$

The maximum duty cycle for the forward regulator operated in the continuous mode can be determined by equating the time integral of the input voltage when Q_1 is on and the clamping voltage V_r when Q_1 is off.

$$\int_0^{DT} V_i dt = \int_{DT}^{T} V_r dt \tag{20.57}$$

that leads to

$$V_i DT = V_r(1 - D)T \tag{20.58}$$

Grouping the D terms in Eq. (20.58) and replacing V_r/V_i with N_r/N_p, we have

$$D_{max} = \frac{1}{1 + N_r/N_p} \tag{20.59}$$

Thus, the maximum duty cycle depends on the turn ratio between the demagnetizing winding and the primary one.

In designing forward regulators, the duty cycle must be kept below the maximum duty cycle D_{max} to avoid saturating the transformer. It should also be noted that the transformer magnetizing current must be reset to zero at the end of each cycle. Failure to do so will drive the transformer into saturation, which can cause damage to the transistor. There are many ways of implementing the resetting function. In the circuit shown in Fig. 20.23A, a tertiary winding is added to the transformer so that the magnetizing current will return to the input source V_i when the transistor turns off. The primary current always starts at the same value under the steady-state condition.

Unlike flyback regulators, forward regulators require a minimum load at the output. Otherwise, excess output voltage will be produced. One commonly used method to avoid this situation is to attach a small load resistance at the output terminals. Of course, with such an arrangement, a certain amount of power will be lost in the resistor.

Because forward regulators do not store energy in their transformers, for the same output power level, the transformer can be made smaller than for the flyback type. The output current is reasonably constant owing to the action of the output inductor and the flywheel diode; as a result, the output filter capacitor can be made smaller, and its ripple current rating can be much lower than that required for the flybacks.

The forward regulator is widely used with output power below 200 W, though it can be easily constructed with a much higher output power. The limitation comes from the capability of the power transistor to handle the voltage and current stresses if the output power were to increase. In this case, a configuration with more than one transistor can be used to share the burden. Fig. 20.25 shows a double-ended forward regulator. Like the double-ended flyback counterpart, the circuit uses two transistors that are switched on and off simultaneously. The diodes are used to restrict the maximum collector voltage to V_i. Therefore, the transistors with low voltage rating can be used in the circuit.

20.5.3 Half-Bridge Regulators

The half-bridge regulator is another form of an isolated forward regulator. When the voltage on the power transistor in the single-ended forward regulator becomes too high, the half-bridge regulator is used to reduce the stress on the transistor. In a half-bridge regulator, the voltage stress imposed on the power transistors is subject to only the input voltage and is only half of that in a forward regulator. Thus, the output power of a half bridge is double to that of a forward regulator for the same semiconductor devices and magnetic core.

Fig. 20.26 shows the basic configuration of a half-bridge regulator and the associated steady-state waveforms. As seen in Fig. 20.26A, the half-bridge regulator can be viewed as two back-to-back forward regulators, fed by the same input voltage, each delivering power to the load at each alternate half cycle. The capacitors C_1 and C_2 are placed between the input and ground terminals. As such, the voltage across the primary winding is always half the input voltage. The power switches Q_1 and Q_2 are switched on and off alternatively to produce a square-wave ac at the input of the transformer. This square wave is either stepped down or up by the isolation transformer and then rectified by the diodes D_{R1} and D_{R2}. Subsequently, the rectified voltage is filtered to produce the output voltage V_o.

Under steady-state condition, the operation of the regulator can be explained as follows. When Q_1 is on and Q_2 off, D_{R1} conducts and D_{R2} is reverse-biased. The primary voltage V_p is $V_i/2$. The primary current I_p starts to build up and stores energy in the primary winding. This energy is forward transferred to the secondary and onto the L_1C filter and the load R_L, through the rectifier diode D_{R1}. During the time interval Δ, when both Q_1 and Q_2 are off, D_{R1} and D_{R2} are forced to conduct to carry the magnetizing current that resulted in the interval during which Q_1 is turned on. The inductor current I_{L1} in this interval is equal to the sum of the currents in D_{R1} and D_{R2}. This interval terminates at half of the switching period T, when Q_2 is turned on. When Q_2 is on and Q_1 off, D_{R1} is reverse-biased and D_{R2} conducts. The primary voltage V_p is now $-V_i/2$. The circuit operates in a likewise manner as during the first half cycle.

With Q_1 on, the voltage across the secondary winding is

$$V_{s1} = \frac{N_{s1}}{N_p}\left(\frac{V_i}{2}\right) \tag{20.60}$$

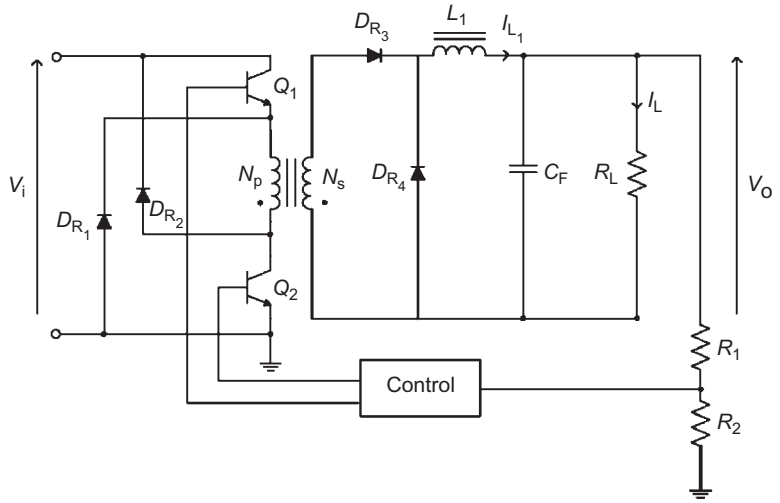


FIG. 20.25 Double-ended forward regulator.

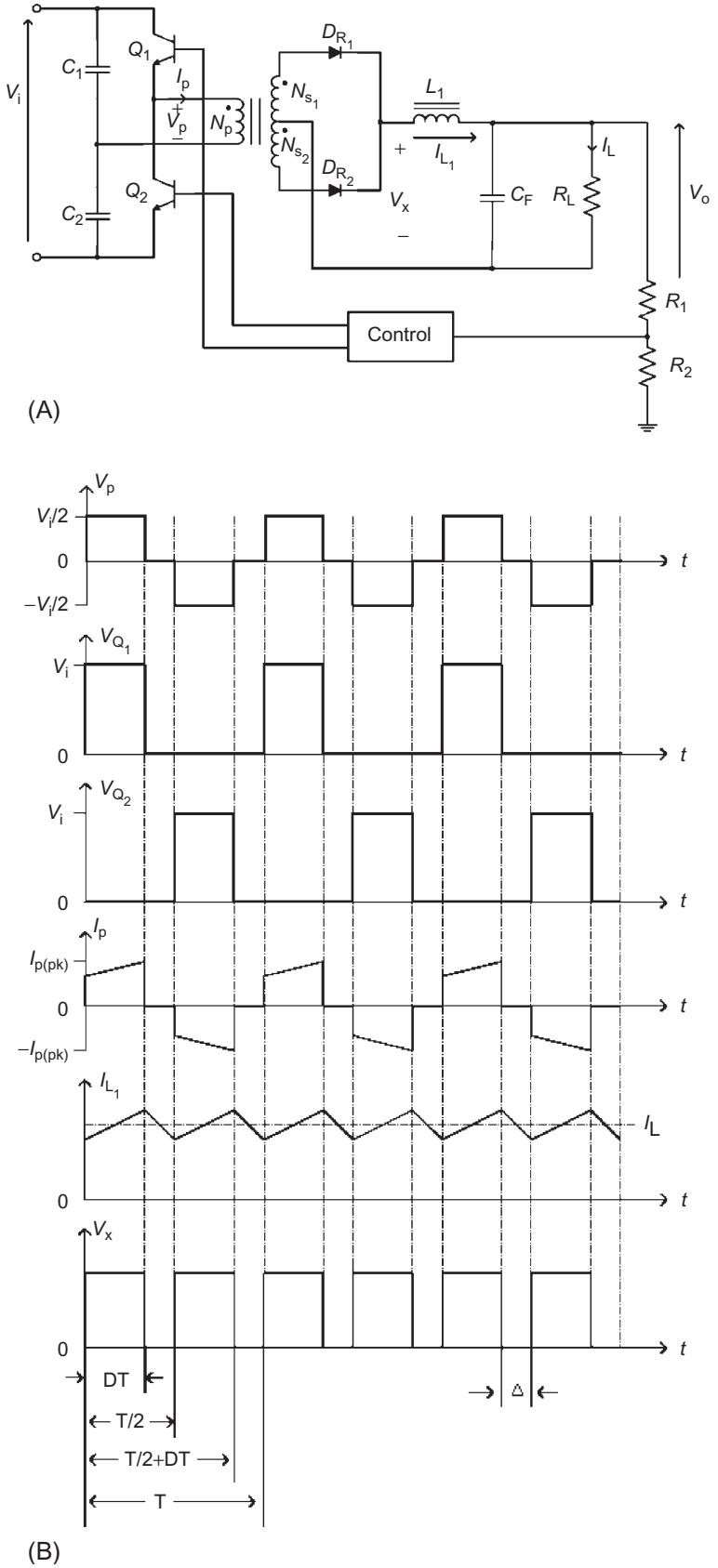


FIG. 20.26 A simplified half-bridge regulator: (A) circuit and (B) the associated waveforms.

Neglecting diode voltage drops and losses, the voltage across the output inductor is then given by

$$V_{L1} = \frac{N_{s1}}{N_p}\left(\frac{V_i}{2}\right) - V_o \tag{20.61}$$

In this interval, the inductor current I_{L1} increases linearly at the rate of

$$\begin{aligned}\frac{dI_{L1}}{dt} &= \frac{V_{L1}}{L_1} \\ &= \frac{1}{L_1}\left[\frac{N_{s1}}{N_p}\left(\frac{V_i}{2}\right) - V_o\right]\end{aligned} \tag{20.62}$$

At the end of Q_1 on-time, I_{L1} reaches a value that is given by

$$I_{L1(pk)} = I_{L1}(0) + \frac{1}{L_1}\left[\frac{N_{s1}}{N_p}\left(\frac{V_i}{2}\right) - V_o\right]DT \tag{20.63}$$

During the interval Δ, I_{L1} is equal to the sum of the rectifier diode currents. Assuming the two secondary windings are identical, I_{L1} is given by

$$I_{L1} = 2I_{DR1} = 2I_{DR2} \tag{20.64}$$

This current decreases linearly at the rate of

$$\frac{dI_{L1}}{dt} = \frac{V_o}{L_1} \tag{20.65}$$

The next half cycle repeats with Q_2 on and for the interval Δ.

The output voltage can be found from the time integral of the inductor voltage over a time equal to T. Thus, we have

$$V_o = 2 \times \frac{1}{T}\left[\int_0^{DT}\left(\frac{N_{s1}}{N_p}\left(\frac{V_i}{2}\right) - V_o\right)dt + \int_{T/2}^{T/2+DT} - V_o dt\right] \tag{20.66}$$

Note that the multiplier of 2 appears in Eq. (20.66) because of the two alternate half cycles. Solving Eq. (20.66) for V_o, we have

$$V_o = \frac{N_{s1}}{N_p}V_i D \tag{20.67}$$

The output power P_o is given by

$$\begin{aligned}P_o &= V_o I_L \\ &= \eta P_{in} \\ &= \eta\frac{V_i I_{p(avg)} D}{2}\end{aligned} \tag{20.68}$$

or

$$I_{p(avg)} = \frac{2P_o}{\eta V_i D} \tag{20.69}$$

where $I_{p(avg)}$ has the value of the primary current at the center of the rising or falling ramp. Assuming the reaction current I_p' reflected from the secondary is much greater than the magnetizing current, then the maximum collector currents for Q_1 and Q_2 are given by

$$\begin{aligned}I_{C(max)} &= I_{p(avg)} \\ &= \frac{2P_o}{\eta V_i D_{max}}\end{aligned} \tag{20.70}$$

As mentioned, the maximum collector voltages for Q_1 and Q_2 at turnoff are given by

$$V_{C(max)} = V_{i(max)} \tag{20.71}$$

In designing half-bridge regulators, the maximum duty cycle can never be greater than 50%. When both the transistors are switched on simultaneously, the input voltage is short-circuited to ground. The series capacitors C_1 and C_2 provide a dc bias to balance the volt-second integrals of the two switching intervals. Hence, any mismatch in devices would not easily saturate the core. However, if such a situation arises, a small coupling capacitor can be inserted in series with the primary winding. A dc bias voltage proportional to the volt-second imbalance is developed across the coupling capacitor. This balances the volt-second integrals of the two switching intervals.

One problem in using half-bridge regulators is related to the design of the drivers for the power switches. Specifically, the emitter of Q_1 is not at ground level, but is at a high ac level. The driver must therefore be referenced to this ac level. Typically, transformer-coupled drivers are used to drive both switches, thus solving the grounding problem and allowing the controller to be isolated from the drivers.

The half-bridge regulator is widely used for medium-power applications. Because of its core-balancing feature, the half bridge becomes the predominant choice for output power ranging from 200 to 400 W. Since the half bridge is more complex, for application below 200 W, the flyback or forward regulator is considered to be a better choice and more cost-effective. Above 400 W, the primary and switch currents of the half bridge become very high. Thus, it becomes unsuitable.

20.5.4 Full-Bridge Regulators

The full-bridge regulator is yet another form of isolated forward regulator. Its performance is improved over that of the half-bridge regulator because of the reduced peak collector current. The two series capacitors that appeared in half-bridge circuits are now replaced by another pair of transistors of the same type. In each switching interval, two of the switches are turned on and off simultaneously such that the full input voltage appears at the primary winding. The primary and the switch currents are only half that of the half bridge for the same power level. Thus, the maximum output power of this topology is twice that of the half bridge.

Fig. 20.27 shows the basic configuration of a full-bridge regulator and the associated steady-state waveforms. Four power switches are required in the circuit. The power switches Q_1 and Q_4 turn on and off simultaneously in one of the half cycles. Q_2 and Q_3 also turn on and off simultaneously in the other half cycle but with opposite phase as Q_1 and Q_4. This produces a square-wave ac with a value of $\pm V_i$ at the primary winding of the transformer. Like the half bridge, this voltage is stepped down, rectified, and then filtered to produce a dc output voltage. The capacitor C_1 is used to balance the volt-second integrals of the two switching intervals and prevent the transformer from being driven into saturation.

Under steady-state conditions, the operation of the full bridge is similar to that of the half bridge. When Q_1 and Q_4 turn on, the voltage across the secondary winding is

$$V_{s1} = \frac{N_{s1}}{N_p} V_i \tag{20.72}$$

Neglecting diode voltage drops and losses, the voltage across the output inductor is then given by

$$V_{L1} = \frac{N_{s1}}{N_p} V_i - V_o \tag{20.73}$$

In this interval, the inductor current I_{L1} increases linearly at the rate of

$$\begin{aligned} \frac{dI_{L1}}{dt} &= \frac{V_{L1}}{L_1} \\ &= \frac{1}{L_1}\left[\frac{N_{s1}}{N_p} V_i - V_o\right] \end{aligned} \tag{20.74}$$

At the end of Q_1 and Q_4 on-time, I_{L1} reaches a value that is given by

$$I_{L1(pk)} = I_{L1}(0) + \frac{1}{L_1}\left[\frac{N_{s1}}{N_p} V_i - V_o\right] DT \tag{20.75}$$

During the interval Δ, I_{L1} decreases linearly at the rate of

$$\frac{dI_{L1}}{dt} = \frac{V_o}{L_1} \tag{20.76}$$

The next half cycle repeats with Q_2 and Q_3 on, and the circuit operates in a similar manner as in the first half cycle.

Again, as in the half bridge, the output voltage can be found from the time integral of the inductor voltage over a time equal to T. Thus, we have

$$V_o = 2 \times \frac{1}{T}\left[\int_0^{DT}\left(\frac{N_{s1}}{N_p} V_i - V_o\right) dt + \int_{T/2}^{T/2+DT} -V_o dt\right] \tag{20.77}$$

Solving Eq. (20.77) for V_o, we have

$$V_o = \frac{N_{s1}}{N_p} 2 V_i D \tag{20.78}$$

The output power P_o is given by

$$\begin{aligned} P_o &= \eta P_{in} \\ &= \eta V_i I_{p(avg)} D \end{aligned} \tag{20.79}$$

or

$$I_{p(avg)} = \frac{P_o}{\eta V_i D} \tag{20.80}$$

where $I_{p(avg)}$ has the same definition as in the half-bridge case.

Comparing Eq. (20.80) with Eq. (20.69), we see that the output power of a full bridge is twice that of a half bridge with same input voltage and current. The maximum collector currents for Q_1, Q_2, Q_3, and Q_4 are given by

$$\begin{aligned} I_{C(max)} &= I_{p(avg)} \\ &= \frac{P_o}{\eta V_i D_{max}} \end{aligned} \tag{20.81}$$

Comparing Eq. (20.81) with Eq. (20.70), for the same output power, the maximum collector current is only half that of the half bridge.

As mentioned, the maximum collector voltage for Q_1 and Q_2 at turnoff is given by

$$V_{C(max)} = V_{i(max)} \tag{20.82}$$

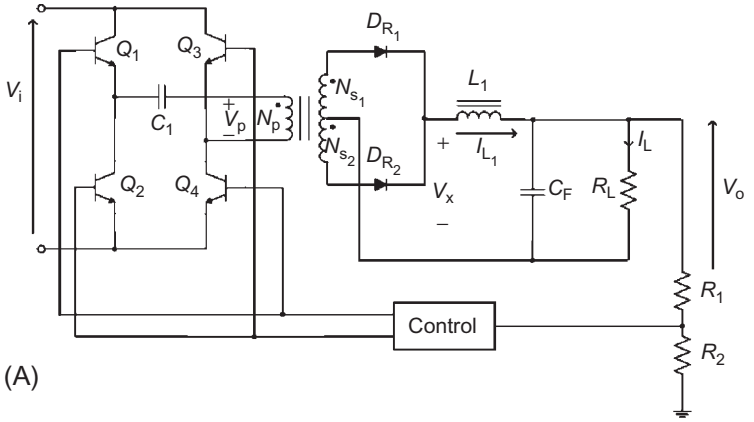
The design of the full bridge is similar to that of the half bridge. The only difference is the use of four power switches instead of two in the full bridge. Therefore, additional drivers are required by adding two more secondary windings in the pulse transformer of the driving circuit.

For high-power applications ranging from several hundred to thousand kilowatts, the full-bridge regulator is an inevitable choice. It has the most efficient use of magnetic core and semiconductor switches. The full bridge is complex and therefore expensive to build and is only justified for high-power applications, typically over 500 W.

20.5.5 Control Circuits and Pulse-Width Modulation

In previous subsections, we presented several popular voltage regulators that may be used in a switching mode power supply. This section discusses the control circuits that regulate the output voltage of a switching regulator by constantly adjusting the conduction period t_{on} or duty cycle d of the power switch. Such adjustment is called *pulse-width modulation* (PWM).

The duty cycle is defined as the fraction of the period during which the switch is on, that is,



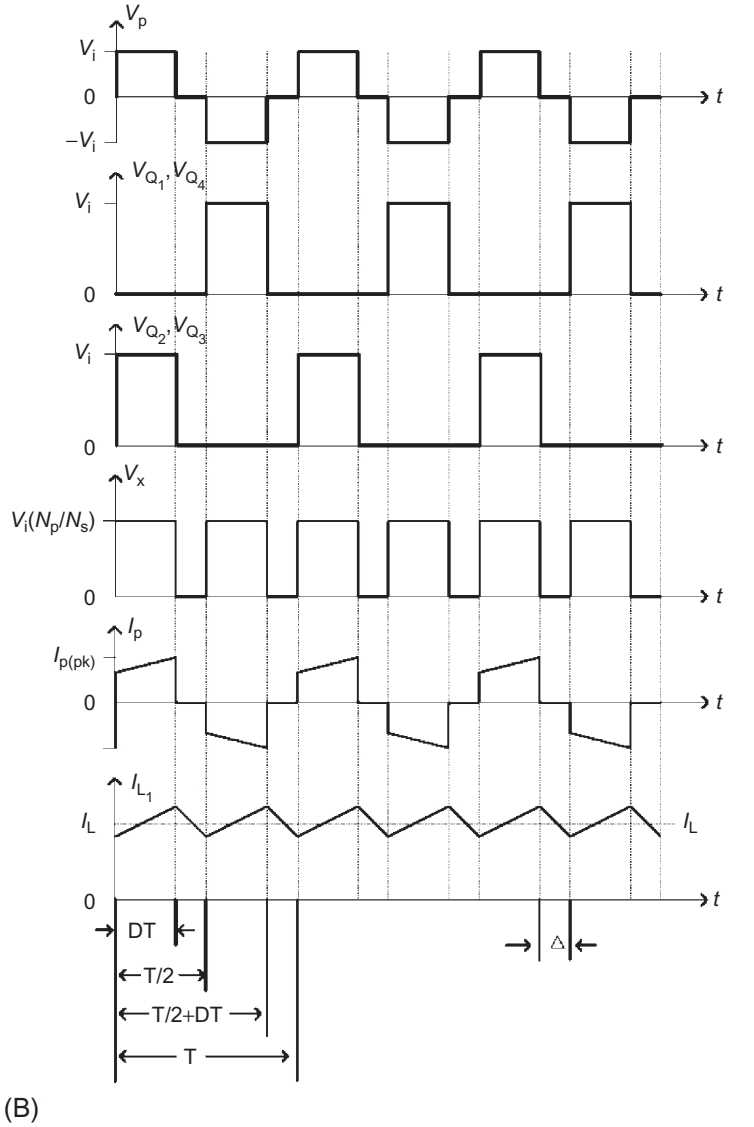


FIG. 20.27 A simplified full-bridge regulator: (A) circuit and (B) the associated waveforms.

$$d = \frac{t_{on}}{T} = \frac{t_{on}}{t_{on} + t_{off}} \tag{20.83}$$

where T is the switching period, that is, $t_{off} = T - t_{on}$. By adjusting either t_{on} or t_{off} or both, d can be modulated. Thus, PWM controlled regulators can operate at variable frequency and fixed frequency.

Among all types of PWM controllers, the fixed-frequency controller is by far the most popular choice. There are two main reasons for their popularity. First, low-cost fixed-frequency PWM IC controllers have been developed by various solid-state device manufacturers, and most of these IC controllers have all the features that are needed to build a PWM switching power supply using a minimum number of components. Second, because of their fixed-frequency nature, fixed-frequency controllers do not have the problem of unpredictable noise spectrum associated with variable frequency controllers. This makes EMI control much easier.

There are two types of fixed-frequency PWM controllers, namely, *the voltage-mode controller* and the *current-mode controller*. In its simplified form, a voltage-mode controller consists of four main functional components: an adjustable clock for setting the switching frequency, an output voltage error amplifier for detecting deviation of the output from the nominal value, a ramp generator for providing a sawtooth signal that is synchronized to the clock, and a comparator that compares the output error signal with the sawtooth signal. The output of the comparator is the signal that drives the controlled switch. Fig. 20.28 shows a simplified PWM voltage-mode controlled forward regulator operating at fixed frequency and its associated driving signal waveform. As shown, the duration of the on-time t_{on} is determined by the time between the reset of the ramp generator and the intersection of the error voltage with the positive-going ramp signal.

The error voltage v_e is given by

$$v_e = \left(1 + \frac{Z_2}{Z_1}\right) V_{REF} - \frac{Z_2}{Z_1} v_2 \tag{20.84}$$

From Eq. (20.84), the small-signal term can be separated from the dc operating point by

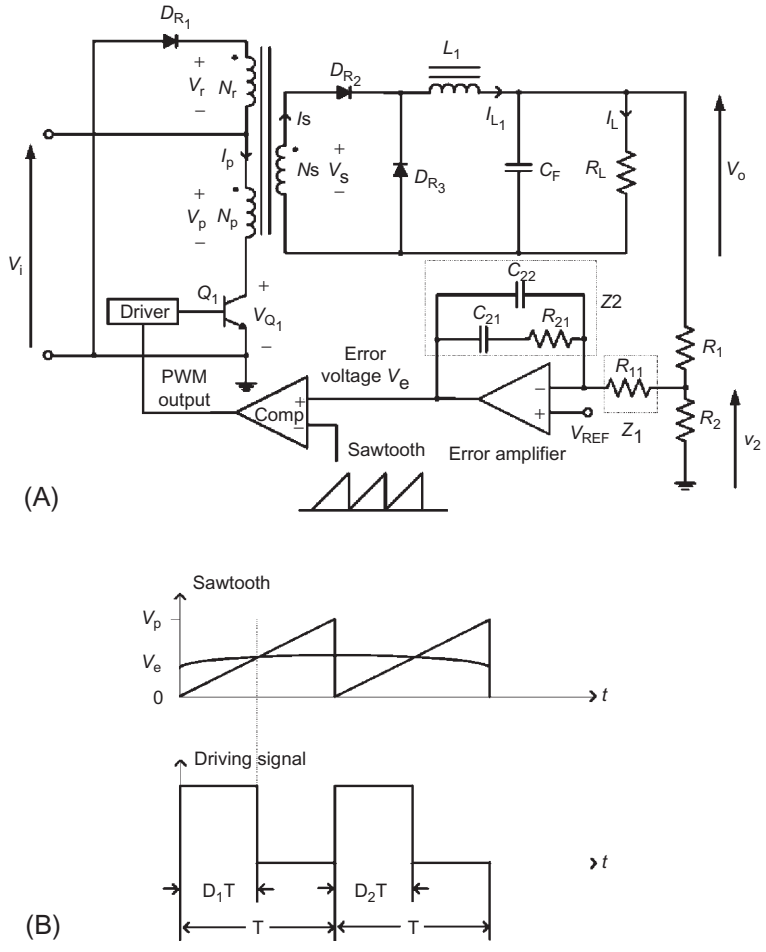


FIG. 20.28 A simplified voltage-mode controlled forward regulator: (A) circuit and (B) the associated driving signal waveform.

$$\Delta v_e = -\frac{Z_2}{Z_1}\Delta v_2 \tag{20.85}$$

$$V_e = \left(1 + \frac{Z_2}{Z_1}\right) V_{REF} - \frac{Z_2}{Z_1} V_2 \tag{20.86}$$

The dc operating point is given by

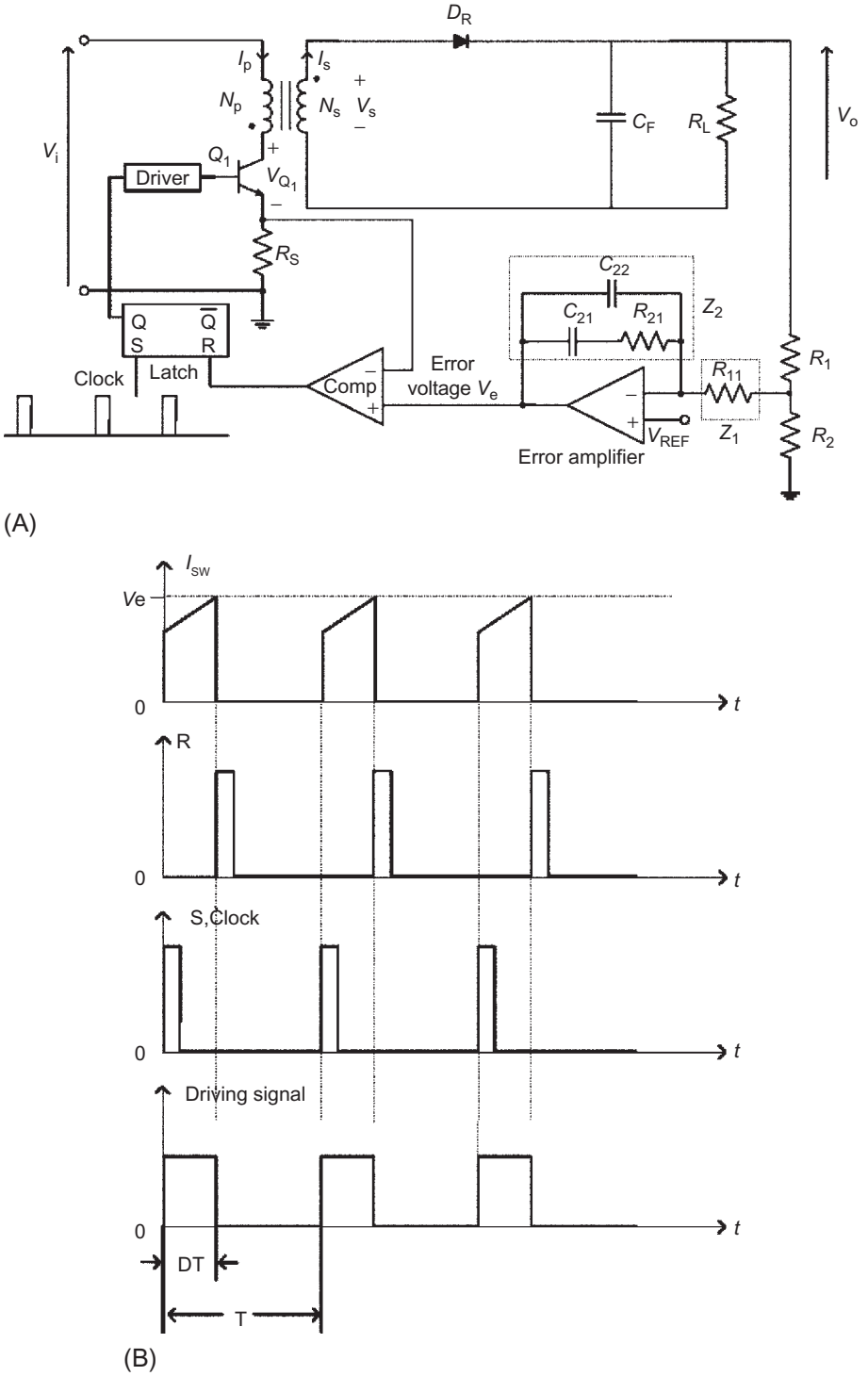


FIG. 20.29 A simplified peak current-mode controlled flyback regulator: (A) circuit and (B) the associated waveforms.

Inspecting the waveform of the sawtooth and the error voltage shows that the duty cycle is related to the error voltage by

$$d = \frac{v_e}{V_p} \tag{20.87}$$

where V_p is the peak voltage of the sawtooth.

Hence, the small-signal duty cycle is related to the small-signal error voltage by

$$\Delta d = \frac{\Delta v_e}{V_p} \tag{20.88}$$

The operation of the fixed-frequency voltage-mode controller can be explained as follows. When the output is lower than the nominal dc value, a high error voltage is produced. This means that Δv_e is positive. Hence, Δd is positive. The duty cycle is increased to cause a subsequent increase in output voltage. The feedback dynamics (stability and transient response) is determined by the operational amplifier circuit that consists of Z_1 and Z_2. Some of the popular voltage-mode control ICs are SG1524/25/26/27, TL494/5, and MC34060/63.

The current-mode control makes use of the current information in a regulator to achieve output voltage regulation. In its simplest form, current-mode control consists of an inner loop that samples the inductance current value and turns the switches off as soon as the current reaches a certain value set by the outer voltage loop. In this way, the current-mode control achieves faster response than the voltage mode. There are two types of fixed-frequency PWM current-mode control, namely, the *peak current-mode control* and the *average current-mode control*.

In the peak current-mode control, no sawtooth generator is needed. In fact, the inductance current waveform is itself a sawtooth. The voltage analog of the current may be provided by a small resistance or by a current transformer. Also, in practice, the switch current is used since only the positive-going portion of the inductance current waveform is required. Fig. 20.29 shows a peak current-mode controlled flyback regulator.

In Fig. 20.29, the regulator operates at fixed frequency. Turn-on is synchronized with the clock pulse, and turnoff is determined by the instant at which the input current equals the error voltage V_e.

Because of its inherent peak current-limiting capability, the peak current-mode control can enhance reliability of power switches. The dynamic performance is improved because of the use of the additional current information. One main disadvantage of the peak current-mode control is that it is extremely susceptible to noise, since the current ramp is usually small compared with the reference signal. A second disadvantage is its inherent instability property at duty cycle exceeding 50%, which results in subharmonic oscillation. Typically, a compensating ramp is required at the comparator input to eliminate this instability. The third disadvantage is that it has a nonideal loop response because of the use of the peak, instead of the average current sensing.

Fig. 20.30 shows an average current-mode controlled flyback regulator. In the circuit, a PWM modulator (instead of a clocked SR latch in the peak current-mode control) is employed to compare the current error with an externally generated sawtooth signal to formulate the desired control signal. The main advantages of this method over the peak current control are that it has excellent noise immunity property, it is stable at duty cycle exceeding 50%, and it provides good tracking of average current. However, since there are three compensation networks (Z_1, Z_2, and Z_3), the analysis and optimal design of these networks are nontrivial. This is a major obstacle for adopting the average current-mode control.

It should be noted that current-mode control is particularly effective for the flyback and boost-type regulators that have an inherent right-half-plane zero. Current-mode control effectively reduces the system to first order by forcing the inductor current to be related to the output voltage, thus achieving faster

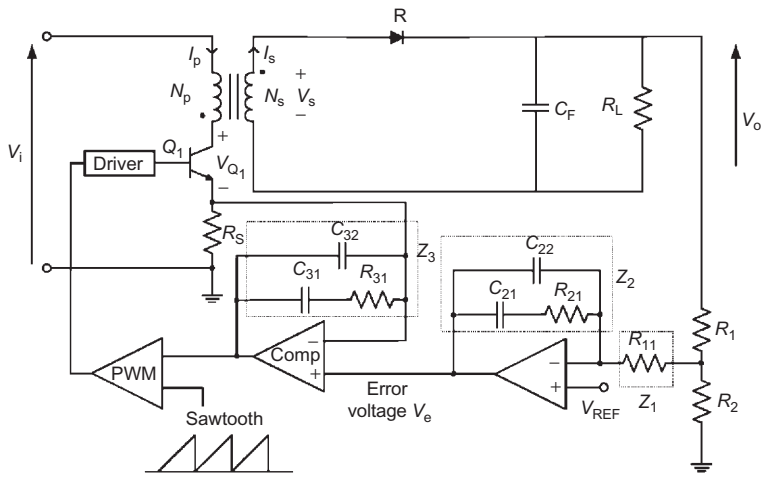


FIG. 20.30 A simplified average current-mode controlled flyback regulator: (A) circuit and (B) the associated waveforms.

response. In the case of the buck-type regulator, current-mode control presents no significant advantage because the current information can be derived from the output voltage, and hence, faster response can still be achieved with a proper feedback network. Some of the popular current-mode control ICs are UC3840/2, UC3825, MC34129, and MC34065.

Further Reading

[1] A.I. Pressman, Switching Power Supply Design, second ed., McGraw-Hill, New York, 1999.
[2] M. Brown, Practical Switching Power Supply Design, second ed., McGraw-Hill, New York, 1999.
[3] P.T. Krein, Elements of Power Electronics, first ed., Oxford University Press, Cambridge, 1998.
[4] J.G. Kassakian, M.R. Schlecht, G.C. Verghese, Principles of Power Electronics, first ed., Addison-Wesley, Reading, MA, 1991.
[5] G. Chryssis, High-Frequency Switching Power Supplies, first ed., McGraw-Hill, New York, 1984.
[6] M.H. Rashid, Power Electronics—Circuits, Devices, and Applications, second ed., Prentice-Hall, Upper Saddle River, NJ, 1993.
[7] T.L. Floyd, D. Buchla, Fundamentals of Analog Circuits, first ed., Prentice-Hall, Upper Saddle River, NJ, 1999.

21

Electronic Ballasts

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21.1 Introduction

Electronic ballasts, also called solid-state ballasts, are those power electronic converters used to supply discharge lamps. The modern age of electronic ballasts began with the introduction of power bipolar transistors with low storage time, allowing to supply fluorescent lamps at frequencies of several kilohertz and increasing lamp luminous efficacy by operating at these high frequencies. Later, electronic ballasts became very popular with the development of low-cost power MOSFETs, with unique features that make them very attractive to implement solid-state ballasts. The main benefits of electronic ballasts are the increase in the lamp and ballast overall efficiency, increase in lamp life, reduction of ballast size and weight, and improvement in lighting quality. This chapter attempts to give a general overview about the more important topics related to this type of power converters.

21.1.1 Basic Notions

Discharge lamps generate electromagnetic radiation by means of an electric current passing through a gas or metal vapor. This radiation is discrete, as opposed to the continuous radiation emitted by an incandescent filament. Fig. 21.1 shows the electromagnetic spectrum of an electric discharge, which consists of a number of separate spectral lines.

As can be seen in Fig. 21.1, only the electromagnetic radiation emitted within the visible region (380–780 nm) of the radiant energy spectrum is useful to provide lighting. The total power in watts emitted by an electric discharge can be obtained by integrating the spectral energy distribution. However, this is not a suitable parameter to measure the amount of light emitted by a discharge lamp.

The human eye presents different responses to the different types of electromagnetic waves within the visible range. As illustrated in Fig. 21.2, there exist two response curves. First, the photopic curve, also called $V(\lambda)$, is the characteristic used to represent the human eye under normal illuminating level conditions or daylight vision. Second, the scotopic curve $V'(\lambda)$ is the response of the human eye for situations with low illuminating levels, also known as nocturnal vision. The reason for this different behavior is physiological. The human eye consists of two types of photoreceptors: rods and cones. Rods are much more sensitive at low lighting levels than cones, but they are not sensitive to the different light colors. On the other hand, cones are responsible for normal color vision at higher lighting levels. Normally, only the photopic function is considered in lighting design and used to calibrate photometers [1,2].

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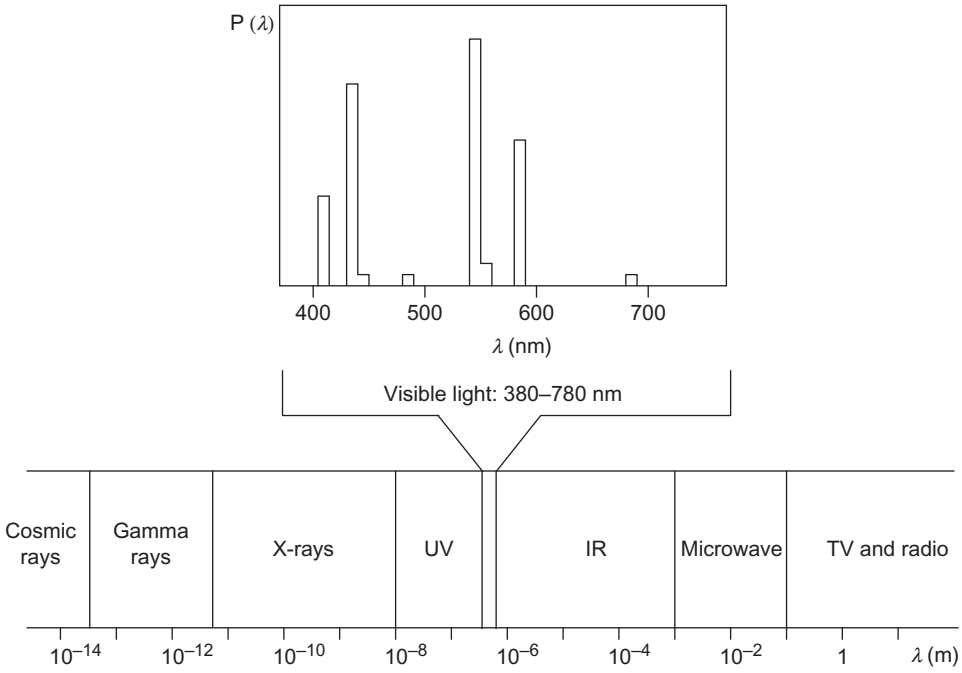


FIG. 21.1 Spectral energy distribution of an arc discharge and radiant energy spectrum.

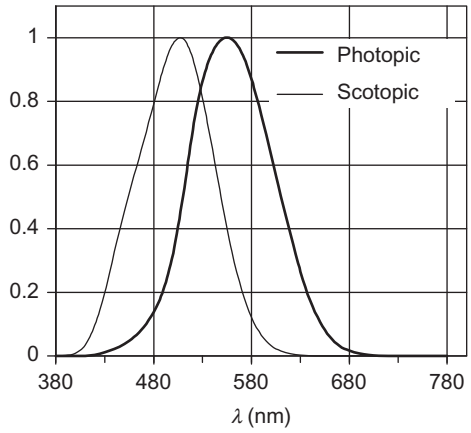


FIG. 21.2 Spectral luminous efficiency functions for standard photopic and scotopic observers.

Since the human eye responds in different ways to the different wavelengths or colors, the output power of a lamp, measured in watts, is no longer applicable to represent the amount of light generated. Thus, a new unit is used to incorporate the human eye response, which is called *lumen*. The total light output of a lamp is then measured in lumens, and it is known as luminous flux of the lamp, which is obtained by integrating the radiant power as follows:

$$\Phi = K_{\mathrm{m}} \int_{380\mathrm{nm}}^{780\mathrm{nm}} P(\lambda) V(\lambda) d\lambda \qquad (21.1)$$

where K_{m} represents the maximal spectral luminous efficacy, which is equal to 683 lm/W (at $\lambda = 555$ nm) for photopic vision and 1700 lm/W (at $\lambda = 507$ nm) for scotopic vision. The standard photopic and scotopic functions were defined by the International Commission on Illumination (CIE) in 1924 and 1951, respectively.

The measurement of the total luminous flux of the lamp is very useful to know whether the lamp is working properly. This can be measured by means of an integrating sphere and using the substitution method. The integrating sphere, also known as Ulbricht photometer, is internally coated with a perfectly diffusing material. Thus, the integral of the sphere is performed in Eq. (21.1), and the illuminance on the internal surface is proportional to the total luminous flux. A photometer with a $V(\lambda)$ filter is placed so that the internal illuminance can be measured, and a baffle is located to avoid direct illumination of the photometer probe by the lamp. The measurement is made in two steps, one with the lamp under test in place and the other with a standard lamp of known total luminous flux. From the two measurements, the total luminous flux of the lamp under test is deduced by linear relationship. Fig. 21.3 illustrates an integrating sphere photometer.

An important parameter related to the supply of discharge lamps is the *luminous efficacy*. Luminous efficacy is defined as the rate of the lamp total luminous flux to the total electric power consumed by the lamp, usually expressed in lumens per watt. The luminous efficacy of a discharge lamp can be increased by proper designing of the electronic ballast, which finally results in energy saving.

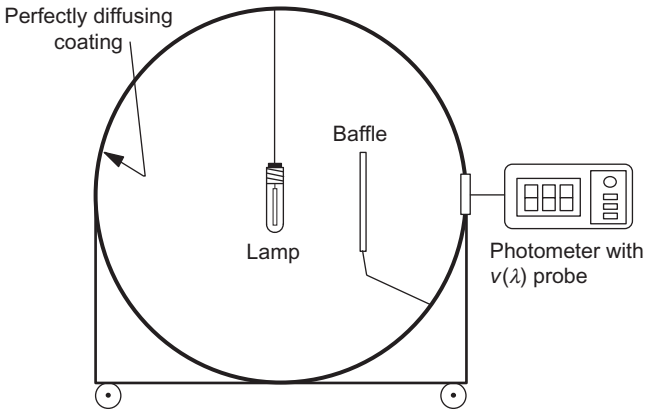


FIG. 21.3 Integrating sphere used for measurement of the lamp total luminous flux.

21.1.2 Discharge Lamps

Basically, discharge lamps consist of a discharge tube inside, which the electric energy is transformed into electromagnetic radiation. The discharge tube is made of a transparent or translucent material with two sealed-in electrodes placed at both ends, as shown in Fig. 21.4. The discharge tube is filled with an inert gas and a metal vapor. The electrodes generate free electrons, which are accelerated by the electric field existing in the discharge. These accelerated electrons collide with the gas atoms, resulting in both elastic and inelastic collisions depending on the electron kinetic energy. The basic processes inside the discharge tube are illustrated in Fig. 21.4. They are as follows [3]:

1. *Heat generation*. When the kinetic energy of the electron is low, an elastic collision takes place, and only a small part of the electron energy is transferred to the gas atom. The result of this type of collisions is an increase in the gas temperature. In this case, the electric energy is consumed to produce heat dissipation. However, this is also an important process because the discharge has to be set in its optimum operating temperature.
2. *Gas atom excitation*. Some electrons can have a high kinetic energy so that the energy transferred in the collision is used to send an electron of the gas atom to a higher orbit. This state is unstable, and the electron tends to recover its original level, emitting the absorbed energy in the form of electromagnetic radiation. This radiation is used to directly generate visible light, or in other case, ultraviolet radiation is first generated and then transformed into visible radiation by means of a phosphor coating existing in the inside wall of the discharge tube.
3. *Gas atom ionization*. In some cases, electrons have gained such high kinetic energy that during the collision with the gas atom, an electron belonging to the gas atom is freed, resulting in a positively charged ion and a free electron. This freed electron can play the same roles as those generated by the electrodes. This process is especially important during both discharge ignition and normal running because ionized atoms and electrons are necessary to maintain the electric current through the lamp.

The number of free electrons in the discharge can increase rapidly due to continuing ionization, producing an unlimited current and finally a short circuit. This is illustrated in Fig. 21.5, which shows how the voltage-current characteristics of a gas discharge exhibit a negative differential resistance. Therefore, in order to limit the discharge current, the use of an auxiliary supply circuit is mandatory. This circuit is called *ballast*.

Focusing on discharge lamps, the complete stabilization process consists of two main phases:

1. *Breakdown phase*. Most of the gases are very good insulators, and an electric discharge is only possible if a sufficient concentration of charged particles is present. Normally, a high voltage is used to provide electricity carriers and to initiate the discharge. The minimum voltage applied to initiate the discharge is called *starting voltage*. The starting voltage mainly depends on the type of gas, gas pressure, and distance between electrodes. Fig. 21.6A represents the starting voltage as a function of the gas pressure multiplied by electrode distance, for different gases. These functions are known as Paschen curves.

Usually, auxiliary inert gases are used to decrease the starting voltage. Particularly, there exist some special

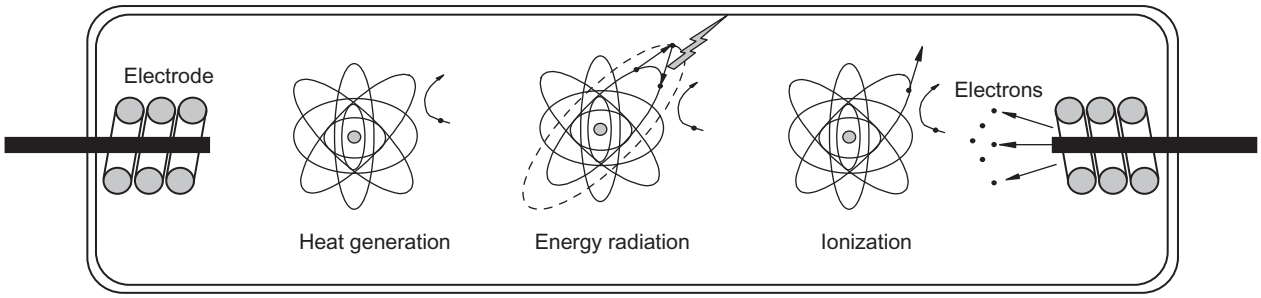


FIG. 21.4 Basic processes inside the discharge tube.

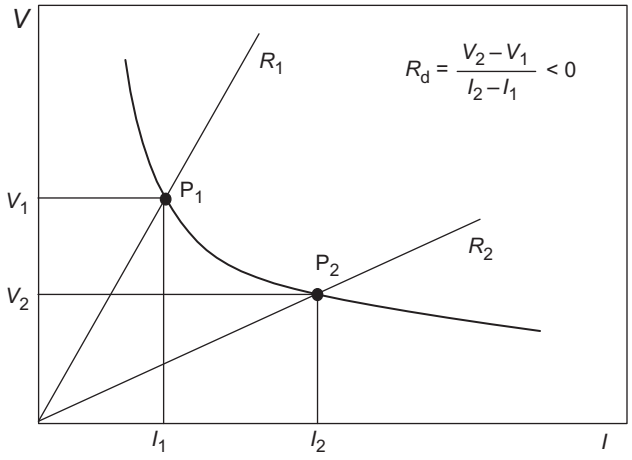


FIG. 21.5 Voltage-current characteristics of a gas discharge.

inert gas mixtures presenting a very low starting voltage, which are called *Penning mixtures*. These Penning mixtures are very often used as initial starting gas. Fig. 21.6A shows a typical Penning mixture constituted by neon with 0.1% of argon.

2. *Warm-up phase*. Once the lamp is ignited, the collisions between free electrons and atoms generate heat, and discharge temperature increases until reaching the normal operation conditions. During this phase, the heat is used to evaporate the metal atoms existing in the discharge tube, and the emitted electromagnetic radiation has the characteristics of a metal vapor discharge instead of an inert gas discharge. From the electric point of view, the discharge warm-up phase shows initially low discharge voltage and high discharge current. As long as more and more metal atoms are evaporated, the discharge voltage increases, and the discharge current decreases. Finally, an equilibrium is reached at steady-state operation with the normal values of voltage and current. The time constant of the warm-up phase strongly depends on the lamp type. It varies from seconds for fluorescent lamps to minutes for high-intensity discharge lamps. Fig. 21.6B illustrates some discharge waveforms during the warm-up phase.

The basic elements used in lamps to generate radiation in the visible part of the spectrum are sodium and mercury. The former generates radiation directly within the visible part of the spectrum; the latter generates radiation mainly in the ultraviolet region, but this radiation can be easily transformed to visible radiation by means of a phosphor coating on the internal wall of the discharge tube. Besides the element used, a very important parameter related to the efficiency and richness of the emitted radiation is the discharge pressure. For the sodium and mercury elements, there exist two pressure values around which the luminous efficacy of the discharge is higher. The first is obtained at quite low pressures, about 1 Pa, and the second at higher pressures around 10^5 Pa (1 at). This is the reason why there exist two main types of discharge lamps:

1. *Low-pressure discharge lamps*. This type of lamps operates with pressures around 1 Pa, and they feature low current density inside the discharge and low power/unit of discharge length. Therefore, these lamps present normally a quite large discharge volume with low power rating. Most representative examples are low-pressure mercury lamps, also known as fluorescent lamps and low-pressure sodium lamps.
2. *High-pressure discharge lamps*. The operating pressure in this type of lamps is around 10^5 Pa and higher, in order to achieve a considerable increase in the luminous efficacy of the discharge. These lamps present a high current density in the discharge and a high power/discharge length ratio, thus showing much smaller discharge tubes.

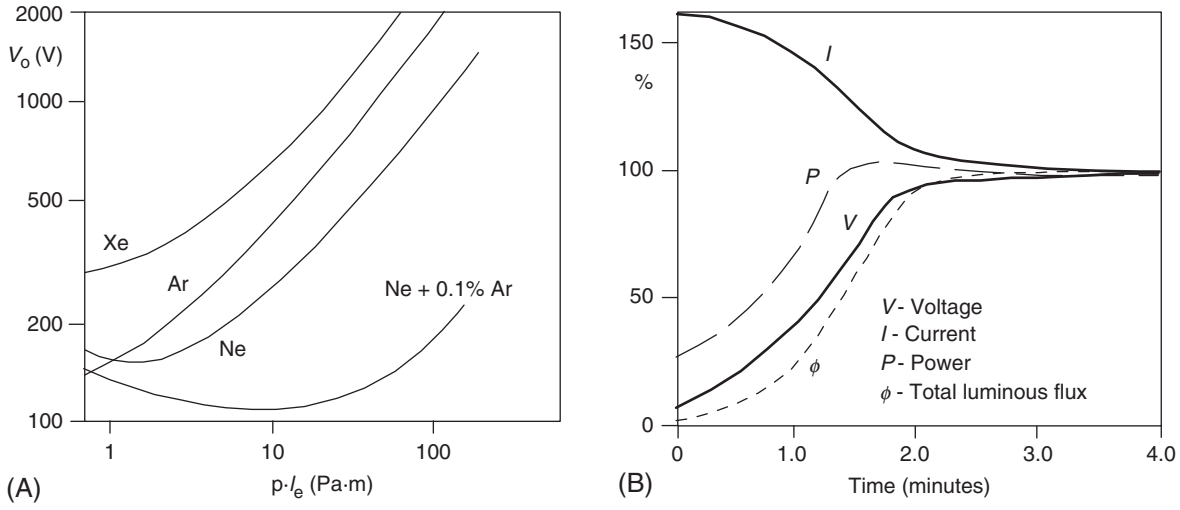


FIG. 21.6 (A) Paschen curves for different inert gases and (B) stabilization curve of a discharge lamp.

Examples of these lamps are high-pressure sodium lamps, high-pressure mercury lamps, and metal halide lamps.

Finally, to characterize the light produced by a discharge lamp, it is necessary to know two important concepts: the correlated color temperature (CCT) and the color rendering index (CRI).

The CCT is defined as the temperature of the blackbody radiator whose perceived color most closely resembles that of the discharge lamp. The color of an incandescent body changes from deep red to orange, yellow, and finally white as its temperature rises. Thus, a cool-white fluorescent lamp has a CCT around 3500 K, and it is perceived as a white source of light, whereas a high-pressure sodium lamp presents a CCT of about 2000 K, and it appears as yellow.

The CRI of a light source is the effect that the source has on the color appearance of the objects under it, when compared with their appearance under a reference source of equal CCT. The measurement gives a value lower than 100, and the higher the CRI, the better the color rendition. For example, daylight and incandescent lamps have a CRI equal to 100.

To conclude this introduction on the discharge lamps, some comments regarding the most important types of discharge lamps will be given. Table 21.1 provides some additional data on the different discharge lamps for comparison.

1. *Fluorescent lamps*. These lamps belong to the category of low-pressure mercury vapor discharge lamps. The discharge generates two main lines at 185 and 253.7 nm and other weak lines in the visible range of the spectrum. A fluorescent powder on the inside wall of the discharge tube converts the ultraviolet radiation into visible radiation, resulting in a broadband spectral distribution and good color rendition. In these lamps, the optimum mercury vapor pressure (which gives the maximum luminous efficacy) is 0.8 Pa. For the tube diameters normally used, this pressure is reached at a wall temperature of about 40°C, not much higher than typical ambient temperature. The heat generated inside the discharge is sufficient to attain the required operating temperature without using an outer bulb. However, this structure causes a great variation of the lamp lumen output with the temperature, which is one important drawback of the fluorescent lamps. One solution to this problem is the addition of amalgams to stabilize the light output. This is specially used in compact fluorescent lamps.
2. *Low-pressure sodium lamps*. These lamps are the most efficient source of light. The reason is the almost monochromatic radiation that they generate, with two main lines at 589 and 589.6 nm, very close to the maximum human eye sensitivity. Therefore, color rendition of these lamps is very poor; however, contrasts are seen more clearly under this light. This is the reason for using these lamps in situations where the recognition of objects and contours is essential for safety, such as motorway bridges, tunnels, and intersections. The optimum pressure for the low-pressure sodium discharge is about 0.4 Pa, which is attained in normal discharge tubes at a temperature of 260°C. An outer bulb is normally used to reach and maintain this temperature.
3. *High-pressure mercury vapor lamps*. The increase in the pressure of the mercury vapor produces a radiation richer in spectral lines; some of them are in the visible part of the spectrum (405, 436, 546, and 577/579 nm). This leads to an increase in the luminous efficacy, reaching values of 40–60 lm/W at pressures 10^5–10^7 Pa (1–100 at). These lamps operate with unsaturated mercury vapor, which means that all the mercury in the discharge tube has evaporated and the number of mercury atoms/unit volume remains constant. Thus, the operation of this type of lamps is more independent of the temperature than most other discharge lamps. One drawback of these lamps is the lack of spectral lines in the long wavelengths (reds) of the spectrum, thus showing low CRI. An increase of the color rendition can be obtained by adding metal halide compounds into the discharge tube, in order to generate radiation all over the visible spectrum. These lamps are known as *metal halide lamps*.
4. *High-pressure sodium lamps*. This is a very popular source of light due to its high luminous efficacy and long life. The increase in the sodium vapor pressure produces a very widening spectrum, with good color rendition compared with the low-pressure sodium lamps. This also leads to a lower luminous efficacy, but it is still higher than the other high-intensity discharge lamps. Some of these lamps also incorporate mercury in the form of

TABLE 21.1 Comparison of different discharge lamps

Lamp	Wattage (W)	Luminous efficacy (lm/W^{-1})	Life (h)	CCT (K)	CRI
Fluorescent	4–100	62	20,000	4200	62
Compact fluorescent	7–30	60–80	10,000	2700–5000	82
Low-pressure sodium	50–150	110–180	15,000	1800	<0
Mercury vapor	50–1000	40–70	24,000	4000–6000	15–50
Metal halide	40–15,000	80–125	10,000	4000	65
HPS	35–1000	65–140	24,000	2000	22
HPS (amalgam)	35–1000	45–85	10,000	2200	65

sodium amalgam to increase the field strength of the discharge, thus decreasing the discharge current. A lower lamp current and a higher lamp voltage allow to reduce the size and cost of the ballast. However, the addition of sodium amalgam strongly reduces the life of the lamp.

21.1.3 Electromagnetic Ballasts

Electromagnetic ballasts are commonly used to stabilize the lamp at the required operating point by limiting the discharge current. The operating point of the lamp is given by the intersection of both lamp and ballast characteristics, as shown in Fig. 21.7. The ballast line is the characteristic that shows the variation of the lamp power versus lamp voltage for a constant line voltage, and it can be measured during the warm-up phase of the lamp. The lamp line is the characteristic that gives the variation of the lamp power as a function of the lamp voltage for different line voltages, and it can be measured by varying the line voltage. Some lamps, such as high-pressure sodium lamps, exhibit a great variation of lamp voltage with changes in the lamp wattage. Because of this characteristic, trapezoids have been established that define maximum and minimum permissible lamp wattage versus lamp voltage for purposes of ballast design, as shown in Fig. 21.7.

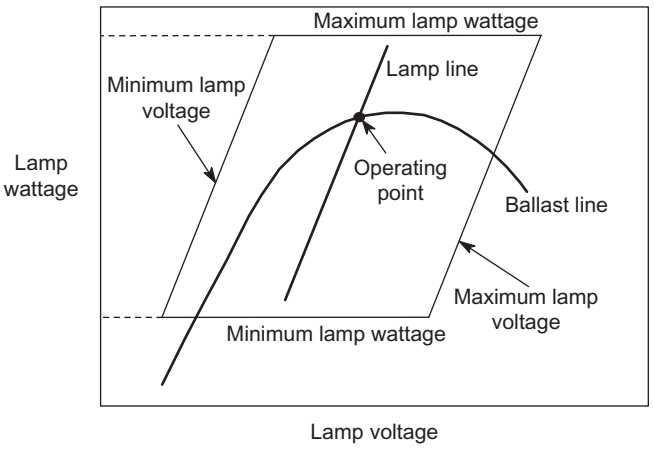


FIG. 21.7 Lamp and ballast characteristics.

Fig. 21.8 shows a basic electromagnetic ballast used to supply low- and high-pressure lamps at line frequencies (50–60 Hz). Fig. 21.8A illustrates the typical circuit used to supply fluorescent lamps with preheating electrodes, which basically uses a series inductor to limit the current through the discharge. Initially, the glow switch is closed, and the short circuit current flows through the circuit, heating the electrodes. A fraction of a second later, the glow switch is opened, and the energy stored in the ballast inductor causes a voltage spike between the lamp electrodes (about 800 V), which finally produces the discharge breakdown. Once ignited, the lamp voltage is lower than the line voltage, and the glow switch remains open during the normal lamp operation. Typical glow switches are based on two bimetal strips inside a small tube filled with an inert gas. An external capacitor of about 10 nF is used to enhance the glow-switch operation and also to reduce radio interference during lamp starting. Finally, in this type of inductive ballasts, a capacitor placed across the line input is mandatory to achieve a reasonable value of the input power factor.

Starting voltages of high-pressure discharge lamps are normally higher than low-pressure discharge lamps and can range from 2500 V for a lamp at room temperature to 30–40 kV to reignite a hot lamp. Thus, the simple ignition system based on the glow switch is no longer applicable for these lamps. Fig. 21.8B and C shows two typical arrangements to supply

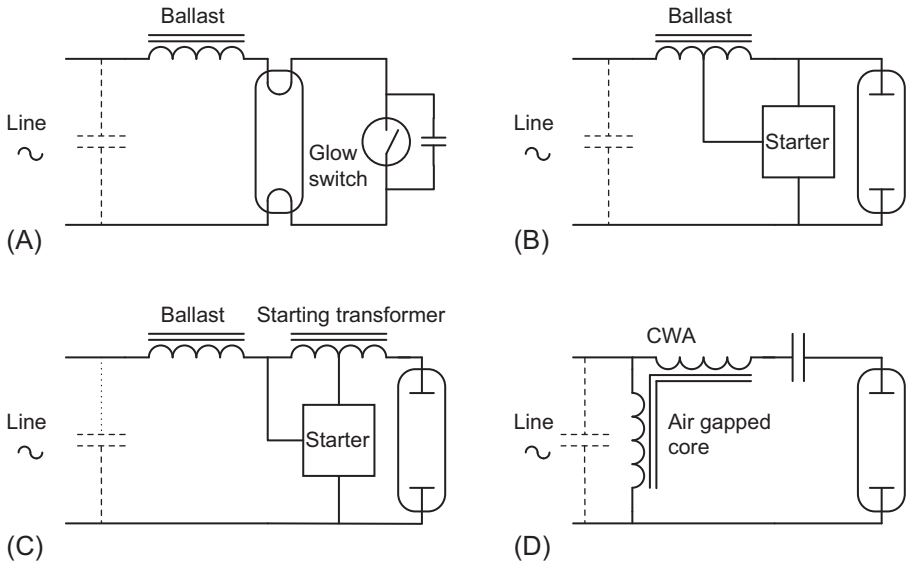


FIG. 21.8 Typical electromagnetic ballast used to supply discharge lamps at low frequency.

high-intensity discharge lamps. A series inductor is also used to limit the lamp current at steady-state operation, but autotransformers are used to attain higher voltage spikes for lamp ignition. For higher line voltages and short distances between starter and lamp, the inductor ballast can be used as an ignition transformer as shown in Fig. 21.8B. In other cases, a separate igniting transformer is needed to provide higher voltage spikes and to avoid the effect of parasitic capacitance of connection cables (Fig. 21.8C).

The inductive ballast provides low-lamp-power regulation against line voltage variation, and therefore, it is only recommended in those installations with low voltage fluctuations. When a good lamp power regulation is necessary, the circuit shown in Fig. 21.8D is normally used. This circuit is commonly named as constant wattage autotransformer (CWA) and incorporates a capacitor in series with the lamp to limit the discharge current. Compared with the normal inductive ballast, the CWA also exhibits higher input power factor, lower line extinguishing voltage, and lower line starting currents.

The main advantage of electromagnetic ballasts is their simplicity, which in turn provides low cost and high reliability. However, since they operate at line frequencies, typically 50–60 Hz, they also feature high size and weight. Other important drawbacks of electromagnetic ballasts are as follows:

- Low efficiency especially for those ballasts featuring good lamp-power regulation against line voltage variation.
- Low reliability for ignition and reignition. If the voltage spike is not well located within the line period, the ignition of the lamp can fail.
- Difficult to control the lamp luminous flux (dimming).
- Lamp operating point changes due to lamp aging process, thus reducing lamp life.
- Low input power factor and high harmonic distortion. Large capacitors are needed across the line input to increase power factor.
- Overcurrent risk due to ballast saturation caused by rectifying effect of some discharge lamps, especially at the end of their life.
- *Flickering* and *stroboscopic effect* due to low frequency supply. The energy radiated by the lamp is a function of the instantaneous input power. Therefore, when supplied from an ac line, an instantaneous variation of the light output occurs, which is called *flicker*. For a line frequency of 60 Hz, the resulting light frequency is 120 Hz. This variation is too fast for the human eye, but when rapidly moving objects are viewed under these lamps, the objects seem to move slowly or even halted. This is called *stroboscopic effect*, and it can be very dangerous in industrial environments. A flicker index is defined with values from 0 to 1.0 [4]. The higher the flicker index the higher is the possibilities of noticeable stroboscopic effect.
- Unsuitable for dc applications (emergency lighting, automobile lighting, etc.).

21.2 High Frequency Supply of Discharge Lamps

21.2.1 General Block Diagram of Electronic Ballasts

Fig. 21.9 shows the general block diagram of a typical electronic ballast. The main stages are the following:

- *EMI filter*. This filter is mandatory for commercial electronic ballast. Usually, it consists of two coupled inductors and a capacitor. The input filter is used to attenuate the electromagnetic interference (EMI) generated by the high-frequency stages of the ballasts. It also protects the ballast against possible line transients.
- *AC-DC converter*. This stage is used to generate a dc voltage level from the ac line. Normally, a full-bridge diode rectifier followed by a filter capacitor is used. However, this simple rectifier provides low input power factor and poor voltage regulation. In order to obtain a higher power factor and a regulated bus voltage, active converters can be used as expounded later in this chapter.

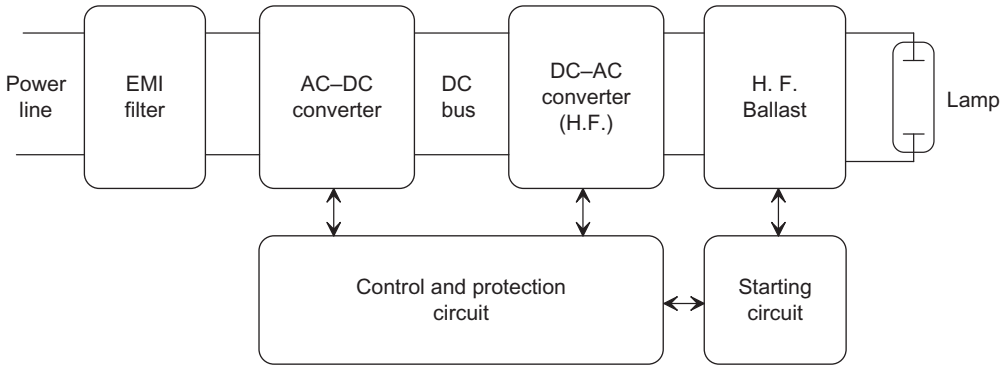


FIG. 21.9 Block diagram of a typical electronic ballast.

- *DC-AC inverter and high-frequency ballast*. These stages are used to supply the lamp at high frequency. The inverter generates a high-frequency waveform, and the ballast is used to limit the current through the discharge. Both inductors and capacitors can be used to perform this function, with the advantage of low size and weight, because they operate at high frequencies.
- *Starting circuit*. In most electronic ballast, especially those for low-pressure discharge lamps, the high-frequency ballast is used to both ignite the lamp and limit the lamp current at steady state. Therefore, no extra starting circuit is necessary. However, when supplying high-pressure discharge lamps, the starting voltages are quite higher, and separate ignition circuits are needed, especially if hot reignition is pursued.
- *Control and protection circuit*. This stage includes the main oscillator, error amplifiers to regulate lamp current or power, output overvoltage protection, timers to control the ignition times, overcurrent protection, and lamp failure protection. It can vary from very simple circuits, those used in self-oscillating ballasts, to very complicated ones, which sometimes include a microprocessor-based control circuit.

There are several important topics when designing electronic ballasts:

- *Operating frequency*. The operating frequency should be high in order to take benefit of the lower size and weight of the reactive elements used to stabilize the discharge. Usually, the operating frequency should be higher than 20 kHz to avoid audible frequencies, which can produce annoying noises. On the other hand, a higher frequency produces higher switching losses, and the practical limit of the switching frequency is about 100 kHz when using MOSFET switches. It is also important to avoid frequencies in the range of 30–40 kHz because these frequencies are normally used in IR remote controls and could generate some kind of interference.
- *Lamp current waveform*. In order to attain the maximum lamp life, it is important to drive the lamp with symmetrical alternating currents, thus making use of both the lamp electrodes alternately. Also, an important parameter is the *lamp current crest factor* (CF), which is the ratio of the peak value to the rms value of the lamp current. In case of electronic ballasts, the ratio of the peak value of the low-frequency-modulated envelope to the rms value should be used. The higher the CF, the lower the lamp life. The ideal situation is to supply the lamp with a pure sinusoidal waveform. Usually, a CF lower than 1.7 is recommended to avoid early aging of the lamp [5].
- *Lamp starting procedure*. This is a very important issue when developing commercially available electronic ballasts. The reason is that the life of the lamp greatly depends on how well the lamp starting is performed, especially for hot-cathode fluorescent lamps. During the starting process, electrodes must be warmed up to the emission temperature, about 800°C, and no high voltage should be applied until their temperature is sufficiently high, thus avoiding sputtering damage. Once the electrodes reach the emission temperature, the starting voltage can be applied to ignite the lamp. For lamps with cold cathodes, the starting voltage must be applied rapidly to prevent harmful glow discharge and cathode sputtering. In any case, starting voltage must be limited to the minimum value to ignite the lamp, since higher voltages could provide undesirable starting conditions that would reduce the life of the lamp.
- *Dimming*. This is an important feature, which allows the ballast to control lamp power and thereby lighting output. Usually, the switching frequency is used in solid-state ballasts as a control parameter to provide dimming capability. Variations in frequency affect the high-frequency ballast impedance and allow to change the discharge current. For example, if an inductor is used as high-frequency ballast, a frequency increase yields an increase in the ballast impedance, thus decreasing lamp current. Dimming should be carried out smoothly, avoiding abrupt changes in lamp power when passing from one level to another. In an eventual power cutoff, the lamp should be restarted at maximum lighting level and then slowly reduced to the required output level.
- *Acoustic resonance*. The HID lamps exhibit an unstable operation when they are supplied at high frequency. At certain operating frequencies, the arc fluctuates and becomes unstable, which can be observed as a high flicker due to important changes in the lamp power and thus in the lighting output. This can be explained by the dependence of the damping of acoustic waves on the plasma composition and pressure. More information about this topic can be found in [6]. The avoidance of acoustic resonance is mandatory to implement commercial electronic ballasts. This can be performed by selecting the operating frequency in a range free of acoustic resonances, typically below 1 kHz and over 100 kHz. Other methods are frequency modulation, square-wave operation, and sine-wave superposed with the third harmonic frequency [7,8].

21.2.2 Classification of Electronic Ballast Topologies

Typical topologies used to supply discharge lamps at high frequency can be classified into two main groups: nonresonant ballasts and resonant ballasts.

21.2.2.1 Nonresonant Ballasts

These topologies are usually obtained by removing the output diode of dc-to-dc converters, in order to supply alternating

current to the lamp. Current mode control is normally employed to limit the discharge lamp current. The lamp is supplied with a square current waveform, which can exhibit a dc level in some cases. A small capacitor is used to initially ignite the lamp, but its effect at steady-state operation can be neglected.

Examples of nonresonant electronic ballasts are shown in Fig. 21.10. Fig. 21.10A and b illustrates a boost-based and a flyback-based ballast, respectively. Other topologies, which can supply symmetrical alternating current through the lamp, are shown in Fig. 21.10C (symmetrical boost) and Fig. 21.10D (push-pull).

These topologies present several drawbacks such as high-voltage spikes across the switch, which necessitates the use of high-voltage transistors, and high switching losses due to hard switching, which gives low efficiency especially for high powers. Besides, since the ideal situation is the lamp being supplied with a sine wave, these circuits produce an early aging of the lamp. To conclude, typical applications of these topologies are portable and emergency equipments, in which lamp power is low and the number of ignitions during its life is not very high. Some applications of these circuits can be found in [9–12].

21.2.2.2 Resonant Ballasts

These ballasts use a resonant tank circuit to supply the lamp. The resonant tank filters the high-order harmonics, thus obtaining a sine current waveform through the lamp. Resonant ballasts can be classified into two categories:

Current-Fed resonant ballasts

These ballasts are supplied with a dc current source, usually obtained by means of a choke inductor in series with the input dc voltage source. The dc current is transformed into an alternating square current waveform by switching power transistors. Typical topologies of this type of ballasts are shown in Fig. 21.11.

The topology shown in Fig. 21.11A corresponds to a class E inverter. Inductor Le is used to obtain a dc input current with low current ripple. This current supplies the resonant tank through the power switch formed by Q1-D1. The resonant tank used in this topology can vary from one ballast to another; the circuit shown in Fig. 21.11A is the one, which is normally used. The main advantage of this topology is that zero voltage switching (ZVS) can be attained in the power switch, thus reducing the switching losses and making the operation at very high frequencies, which can reach several megahertz. This allows to drastically reduce the size and weight of the ballast. However, the adjustment of the circuit parameters to obtain the optimum operation results is quite difficult, especially for mass production. Another important drawback is the high voltage stress across the switch, which can reach values of three times the dc input voltage. For these reasons, the main applications of this circuit are battery-supplied ballasts with low input voltage and low lamp power, as those used in emergency lighting and portable equipment. Typical power range of this ballast varies from 5 to 30 W. Applications of this circuit can be found in [13,14].

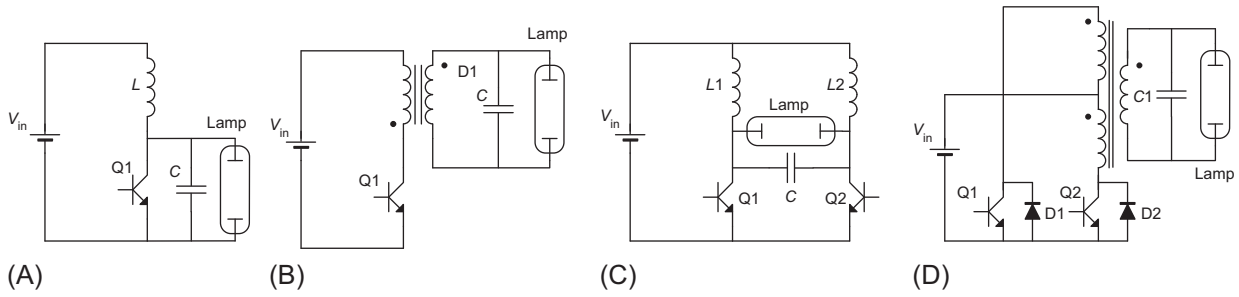


FIG. 21.10 Nonresonant electronic ballasts.

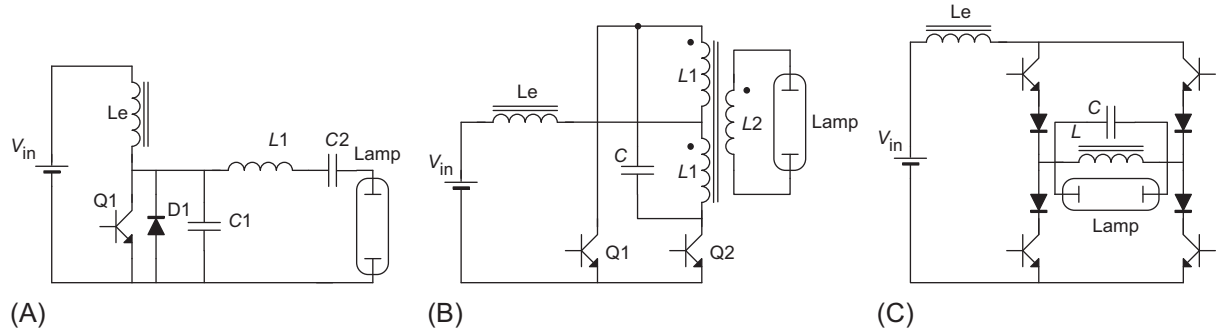


FIG. 21.11 Three typical current-fed resonant inverters: (A) class E inverter, (B) current-fed push-pull inverter, and (C) current-fed full-bridge resonant inverter.

Another typical topology in this group is the current-fed push-pull inverter shown in Fig. 21.11B. In this circuit, a dc input current is obtained by means of choke inductor Le. Transistors are operated with a 50% duty cycle, thus providing a current square wave, which supplies the current-fed parallel resonant circuit formed by the mutual inductance of the transformer and capacitor *C*. This circuit has the advantage of being relatively easy to implement in a self-oscillating configuration, avoiding the use of extra control circuits and thereby reducing the cost. Also, ZVS can be obtained in the power switches. However, the switches also present a high voltage stress, about three times the dc input voltage, which makes this topology unsuitable for power line applications. This circuit is also normally used in battery-operated applications in a self-oscillating arrangement. The typical power range is 4–100 W. Applications based on this circuit can be found in [15,16].

Finally, Fig. 21.11C shows a current-fed full-bridge resonant inverter, which can be used for higher power rating. Also, this circuit allows to control the output power at constant frequency by switching the devices of the same leg simultaneously, generating a quasi-square current wave through the resonant tank [17].

Voltage-fed resonant ballasts

At present, electronic ballast manufacturers mostly use voltage-fed resonant ballasts, especially for applications supplied from the ac mains. The circuit is fed from a dc voltage source, normally obtained by line voltage rectifying. A square-wave voltage waveform is then obtained by switching the transistors with a 50% duty cycle and is used to feed a series resonant circuit. This resonant tank filters the high-order harmonics and supplies the lamp with a sine current waveform. One advantage of the voltage-fed series resonant circuit is that the starting voltage can be easily obtained without using extra ignition capacitors by operating close to resonant tank frequency. Fig. 21.12 shows electric diagrams of typical voltage-fed resonant ballasts.

The voltage-fed version of the push-pull inverter is illustrated in Fig. 21.12A. This inverter includes a transformer, which can be used to step up or down the input voltage in order to obtain an adequate rms value of the output square-wave voltage. This not only provides higher design flexibility but also increases the cost. One disadvantage is that the voltage across transistors is twice the input voltage, which can be quite high for line applications. Therefore, this inverter is normally used for low-voltage applications. Another important drawback of this voltage-fed inverter is that any asymmetry in the two primary windings (different number of turns) or in the switching times of power transistors would provide an undesirable dc level in the transformer magnetic flux, which in turn could saturate the core or decrease the efficiency due to the circulation of dc currents.

Fig. 21.12B and C illustrates two possible arrangements for the voltage-fed half-bridge resonant inverter. The former is normally referred as asymmetrical half bridge, and it uses one of the resonant tank capacitors (*C*1 in the figure) to block the dc voltage level of the square wave generated by the bridge. This means that capacitor *C*1 will exhibit a dc level equal to half the dc input voltage superimposed to its normal alternating

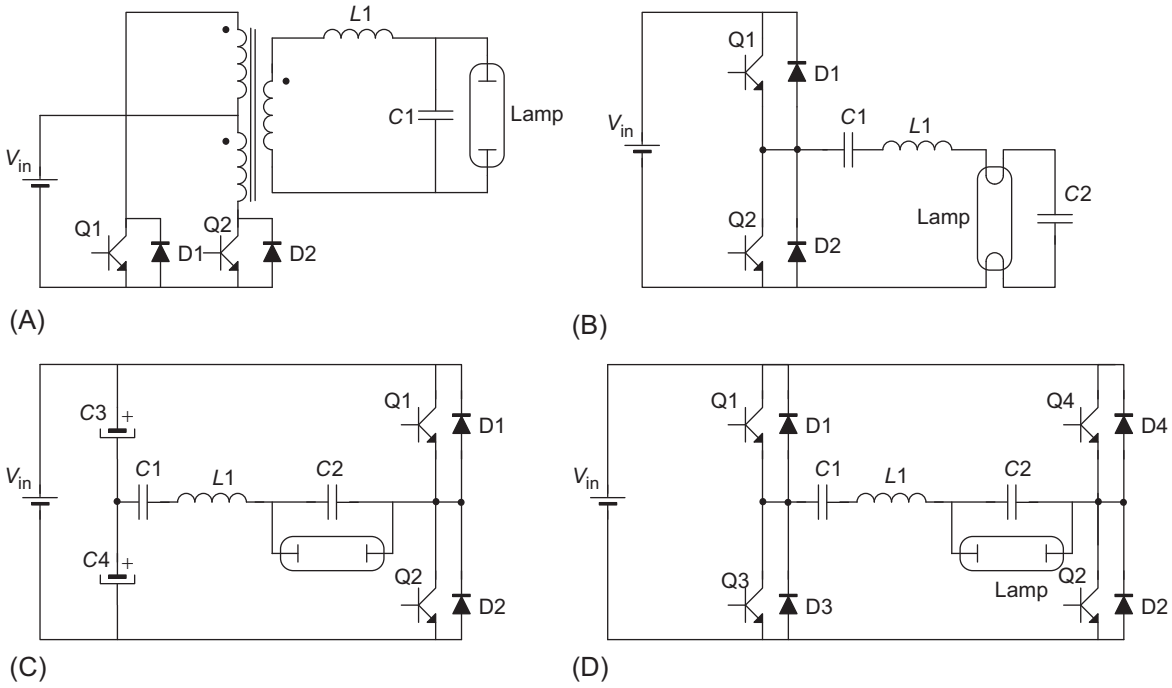


FIG. 21.12 Typical voltage-fed resonant inverters: (A) push-pull, (B)–(C) half-bridge, and (D) full-bridge.

voltage. A transformer can also be used in this inverter to step up or down the input voltage to the required level for each application. In this case, the use of the series capacitor $C1$ prevents any dc current from circulating through the primary winding, thus avoiding transformer saturation. This topology is widely used by ballast manufacturers to supply fluorescent lamps, especially in the self-oscillating version, which allows to drastically reduce the cost. When supplying hot-cathode fluorescent lamps, the parallel capacitor $C2$ is normally placed across two electrodes, as shown in Fig. 21.12B, in order to provide a preheating current for the electrodes and achieve soft ignition. Fig. 21.12C shows another version of the half-bridge topology, using two bulk capacitors to provide a floating voltage level equal to half the input voltage. In this case, capacitor $C1$ is no longer used to block a dc voltage, thus showing lower voltage stress.

Finally, for the high power range (>200 W), the full-bridge topology shown in Fig. 21.12D is normally used. The transistors of each half bridge are operated with a 50% duty cycle, and their switching signals are phase-shifted by 180 degrees. Thus, when switches Q1 and Q2 are activated, direct voltage V_{in} is applied to the resonant tank; when switches Q3 and Q4 are activated, the reverse voltage $-V_{in}$ is obtained across the resonant circuit. One of the advantages of this circuit is that the switching signals of the two branches can be phase-shifted by angles between 0 and 180 degrees, thus controlling the rms voltage applied to the resonant tank ranging from 0 to V_{in}. This provides an additional parameter to control the output power at constant frequency, which is useful to implement dimming ballast.

21.3 Discharge Lamp Modeling

The low frequency of the mains is not an adequate power source for supplying discharge lamps. At these low frequencies, electrons and ionized atoms have enough time to recombine at each current reversal. For this reason, the discharge must be reignited twice within each line period. Fig. 21.13A illustrates the current and voltage waveforms and the I–V characteristics of a 150 W HPS lamp operated with an inductive ballast at 50 Hz. As can be seen, the reignition voltage spike is nearly 50% higher than the normal discharge voltage, which is constant during the rest of the half cycle.

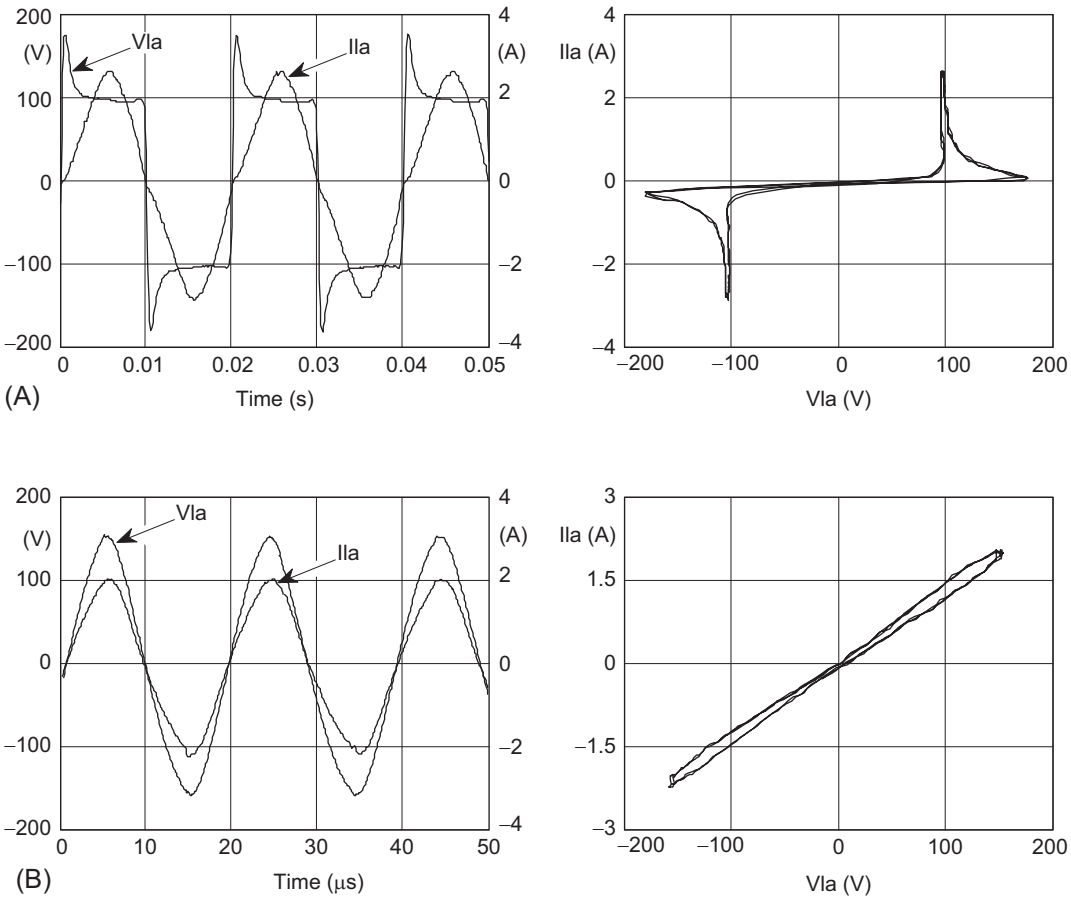


FIG. 21.13 150 W HPS lamp waveforms and I–V characteristics at (A) 50 Hz and (B) 50 kHz.

When lamps are operated at higher frequencies (above 5 kHz), electrons and ions do not have enough time to recombine. Therefore, charge carrier density is sufficiently high at each current reversal, and no extra power is needed to reignite the lamp. The result is an increase in the luminous flux compared with that at low frequencies, which is especially high for fluorescent lamps (10%–15%).

Fig. 21.13B shows the lamp waveforms and *I–V* characteristics for the same 150 W HPS lamp when supplied at 50 kHz. It also shows how the reignition voltage spikes disappear, and the lamp behavior is nearly resistive.

Fig. 21.14 illustrates how the voltage waveforms change in a fluorescent lamp when increasing the supply frequency. As can be seen, at a frequency of 1 kHz, the voltage is already nearly sinusoidal, and the lamp exhibits a resistive property.

Therefore, a resistor can be used to model the lamp at high frequencies for ballast design purposes. However, most lamp manufacturers provide only lamp data for operating at low frequencies, where the lamp acts as a square-wave voltage source. Table 21.2 shows the low-frequency electric data of different discharge lamps provided by the manufacturer and the measured values at high frequency for the same lamps. As can be seen, a power factor close to unity is obtained at high frequency.

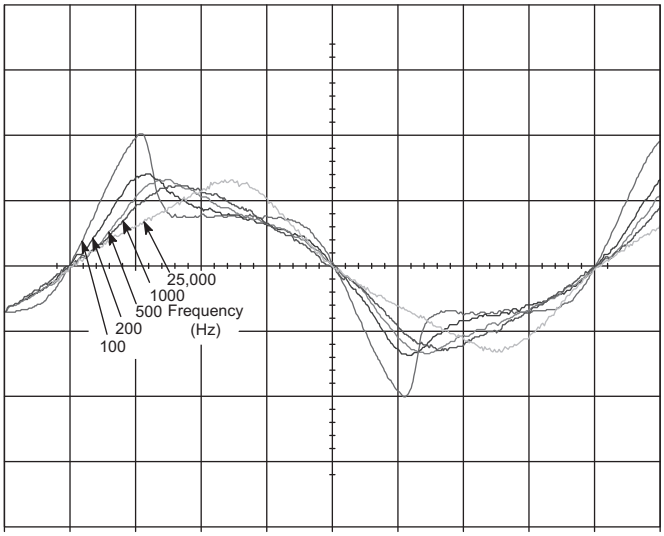


FIG. 21.14 Voltage waveforms for a 36 W linear fluorescent lamp supplied through a resistive ballast at nominal power and different operating frequencies. Vertical scale, 100 V/DIV.

The equivalent lamp resistance at high frequencies can be easily estimated from the low-frequency data. Lamp power at any operating frequency can be expressed as follows:

$$P_{LA} = V_{LA}\ I_{LA}\ FP_{LA} \tag{21.2}$$

where V_{LA} and I_{LA} are the rms values of lamp voltage and current and FP_{LA} is the lamp power factor.

At line frequencies, the lamp power factor is low (typically 0.8), due to the high distortion in the lamp voltage waveform. However, at high frequencies, the lamp power factor reaches nearly 1.0. Then, lamp voltage and current at high frequency ($V_{LA,hf}$ and $I_{LA,hf}$) can be estimated from the following equation:

$$I_{LA,hf}\, V_{LA,hf} = P_{LA} \tag{21.3}$$

where P_{LA} is the nominal lamp power provided by the manufacturer.

As can be seen in Table 21.2, fluorescent lamps tend to maintain nearly the same rms current at low and high frequency, whereas high-pressure discharge lamps tend to maintain nearly the same rms voltage. Based on these assumptions, the equivalent lamp resistance at high frequency estimated from the low frequency values is shown in Table 21.3.

Low-pressure sodium lamps maintain neither voltage nor current constant at high frequency, and they also exhibit an equivalent resistance quite dependent on the frequency. Therefore, their equivalent resistance can only be obtained by laboratory testing.

Note that the values given in Table 21.3 are only an approximation to the real value, which should be obtained by

TABLE 21.3 Estimated electric data of discharge lamps at high frequency

Lamp	$V_{LA,hf}$	$I_{LA,hf}$	$R_{LA,hf}$
Fluorescent lamps	$P_{LA}/I_{LA,lf}$	$I_{LA,lf}$	$P_{LA}/I^2_{LA,lf}$
High-pressure lamps	$V_{LA,lf}$	$P_{LA}/V_{LA,lf}$	$V^2_{LA,lf}/P_{LA}$

TABLE 21.2 Electric data of different discharge lamps

	Manufacturer at 50 Hz				Measured at H. F.			
Lamp[a]	V (V_{rms})	I (A_{rms})	P (W)	PF	V (V_{rms})	I (A_{rms})	P (W)	PF
Fluorescent (TLD-36 W)	103	0.44	36	0.79	83.2	0.46	36	0.94
Compact fluorescent (PLC-26 W)	105	0.31	26	0.80	82	0.32	26	0.99
Low-pressure sodium (SOX-55 W)	109	0.59	55	0.86	75	0.76	56	0.98
Mercury vapor (HPLN-125 W)	125	1.15	125	0.87	132	0.92	120	0.99
Metal halide (MHN-TD-150 W)	90	1.80	150	0.93	92	1.63	146	0.97
High-pressure sodium (SON-T-150 W)	100	1.80	150	0.83	105	1.42	148	0.99

[a]Lamps aged for 100 h.

measurement at the laboratory. This can be used as the first starting point in the design of the electronic ballast, but final adjustments should be made at the laboratory.

Another important issue is that the lamp equivalent resistance is strongly dependent on power delivered to the lamp, which is especially important for designing electronic ballasts with dimming feature. The characteristic lamp resistance versus lamp power is different for each discharge lamp type and must be obtained by laboratory testing. One of the best possibilities to fit the lamp resistance versus power characteristic is the hyperbolic approximation. For example, Mader and Horn propose in [18] the following simple approximation:

$$R_{LA}(P_{LA}) = \frac{V_0^2}{P_{LA} + P_0} \tag{21.4}$$

where R_{LA} is the equivalent lamp resistance, P_{LA} is the average lamp power, and V_0 and P_0 are two parameters that depend on each lamp. This characteristic has been plotted in Fig. 21.15 for a particular lamp with $V_0 = 100$ V and $P_0 = 1$ W.

This model can be implemented very easily in circuit simulation programs, such as SPICE-based programs. Fig. 21.16 shows the electric circuit and the description used to model the characteristic of lamp in a SPICE-based simulation program. The voltage-controlled voltage source EL is used to model the resistive property of the lamp. The voltage source Vs is used to measure the lamp current, so that the instantaneous and average lamp current can be calculated; for this reason, its voltage value is equal to zero. GP is a voltage-controlled current source used to calculate the instantaneous lamp power, which is then filtered by RP and CP in order to obtain the averaged lamp power. Finally, the hyperbolic relationship between the lamp resistance and power is implemented by means of the voltage-controlled voltage source EK. The time constant $\tau = RP \cdot CP$ is related to the ionization constant of the discharge.

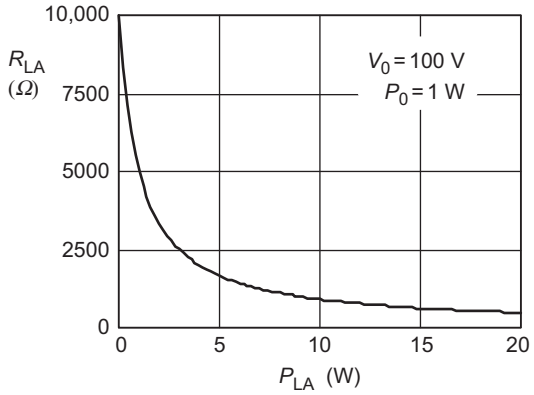


FIG. 21.15 Lamp resistance versus lamp power characteristic.

Fig. 21.17 illustrates some simulation results at low frequency when the lamp is supplied from a sinusoidal voltage source and stabilized with an inductive ballast.

The Mader-Horn model can also be used at high frequencies, which makes the lamp resistive. The equivalent lamp resistance at high frequency will also exhibit a hyperbolic variation with the averaged lamp power and with a time constant given by τ. This model is then useful to simulate an electronic ballast with dimming feature.

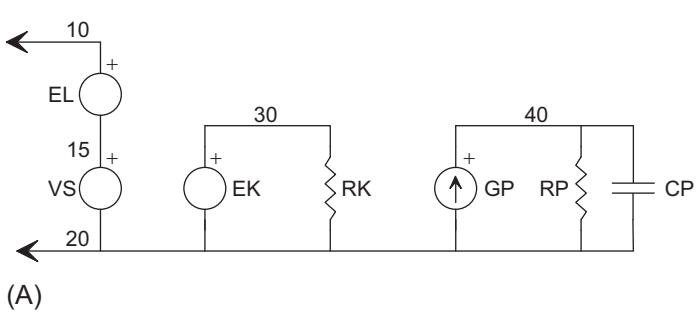
Discharge lamp modeling has become an important subject, since its results are very useful to optimize the electronic ballast performance. Some improvements on the Mader-Horn model and other interesting models can be found in the literature [18–20].

21.4 Resonant Inverters for Electronic Ballasts

Most modern domestic and industrial electronic ballasts use resonant inverters to supply discharge lamps. They can be implemented in two basic ways: current-fed resonant inverters and voltage-fed resonant inverters.

21.4.1 Current-Fed Resonant Inverters

One of the most popular topologies belonging to this category is the current-fed push-pull resonant inverter, previously shown in Fig. 21.11. For this reason, this inverter will be studied here to illustrate the operation of the current-fed resonant ballasts.




```
.subckt lamp 10 20
+ params: Vo=100 Po=1 Tau=0.3 m
EL 10 15 Value={V(30,20)*I(VS)}
VS 15 20 0
EK 30 20 Value={Vo*Vo/(V(40,20)+Po)}
RK 30 20 1
GP 20 40 Value={V(10,20)*I(VS)}
RP 40 20 1
CP 40 20 {Tau}
.ends
```

(B)

FIG. 21.16 (A) Mader-Horn linear model for discharge lamps and (B) SPICE description of the model.

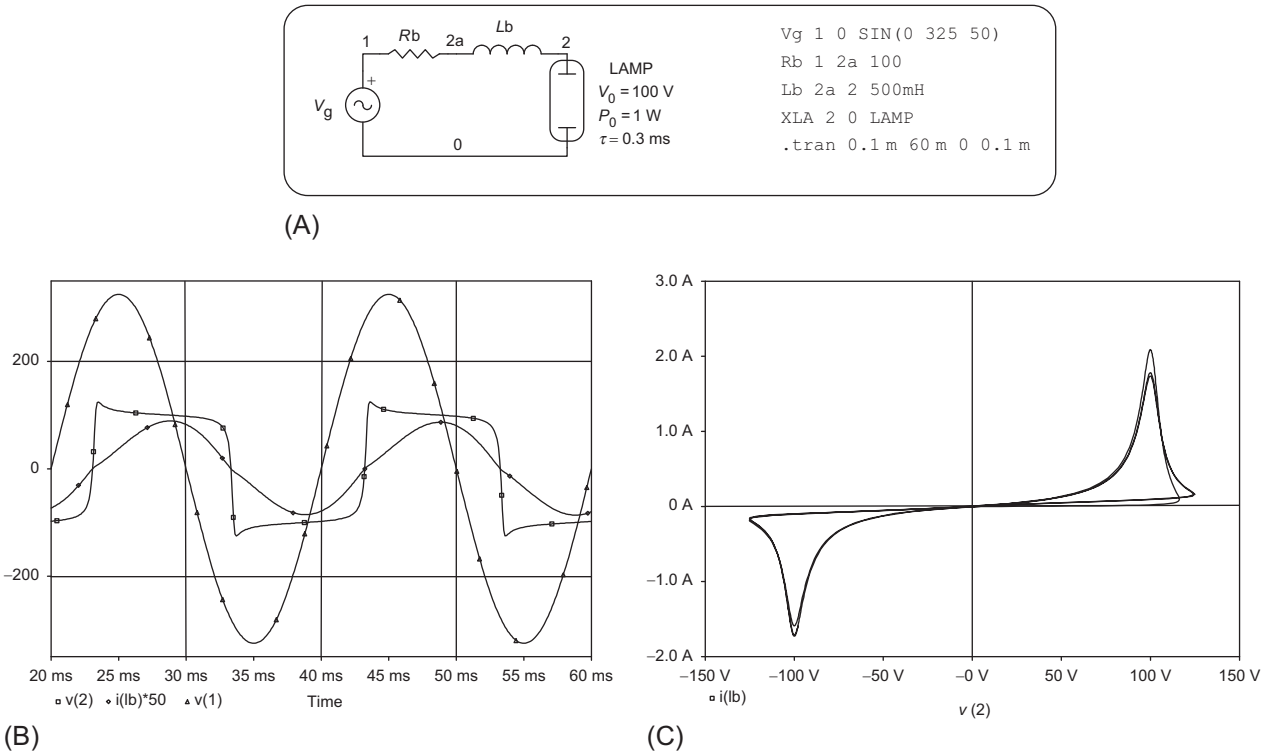


FIG. 21.17 (A) Example of simulation with an inductive ballast at low frequency, (B) operating waveforms, and (C) lamp *I*–*V* characteristics.

The current-fed push-pull inverter uses an input choke to obtain a dc input current with low current ripple. This current is alternatively conducted by the switches so that a parallel resonant tank can be supplied with a current square wave. Fig. 21.18 shows the equivalent circuit and the operating waveforms of a current-fed parallel resonant inverter.

The input current can be expressed as a Fourier series in the following way:

$$i_s(t) = \sum_{n=1,3,5} \ldots I_{S,n} \sin n\omega t = \sum_{n=1,3,5} \ldots \frac{4I_S}{n\pi} \sin n\omega t \qquad (21.5)$$

$I_{S,n}$ being the peak value of each current harmonic and I_S the DC input current of the inverter. The output voltage for each current harmonic is obtained by multiplying the input current $I_{S,n}$ by the equivalent parallel impedance $Z_{E,n}$, which is given below:

$$V_{0,n} = I_{S,n} Z_{E,n} = I_{S,n} \frac{1}{1/R + jn\omega C - j(1/n\omega L)} \qquad (21.6)$$

Usually, normalized values are employed in order to provide more general results. Then, the output voltage can be expressed as follows:

$$V_{0,n} = I_{S,n} Z_B \frac{1}{1/Q + jn\Omega - j(1/n\Omega)} \qquad (21.7)$$

where Z_B is the base impedance of the resonant tank, Q is the normalized load, Ω is the normalized frequency, and ω_0 is the natural frequency of the resonant circuit, given by

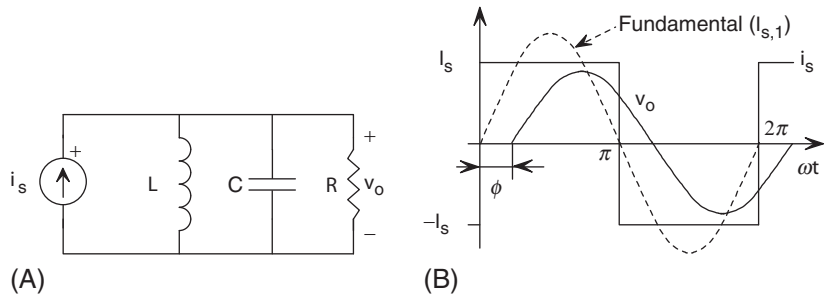


FIG. 21.18 (A) Equivalent circuit of a current-fed parallel resonant inverter and (B) operating waveforms.

$$Z_B = \sqrt{L/C}\ Q = R/Z_B\ \Omega = \omega/\omega_0 = \omega\sqrt{LC}\ \ \omega_0 = 1/\sqrt{LC} \tag{21.8}$$

From Eq. (21.7), the peak output voltage $V_{0,n}$ and phase angle φ_n can be obtained for each harmonic as follows:

$$V_{0,n} = I_{S,n}Z_B \frac{1}{\sqrt{1/Q^2 + (n\Omega - 1/n\Omega)^2}} \tag{21.9}$$

$$\varphi_n = -\tan^{-1}Q(n\Omega - 1/n\Omega) \tag{21.10}$$

The total harmonic distortion (THD) of the output voltage can be calculated as follows:

$$\text{THD}(\%) = \frac{\sqrt{\sum_{n=3,57} V_{0,n}^2}}{V_{0,1}} \cdot 100 \tag{21.11}$$

Based on these equations, the analysis and design of the current-fed resonant inverter can be performed. Normally, the circuit operates close to the natural frequency ω_0, and the effect of the high frequency harmonics can be neglected. To probe this, Fig. 21.19A obtained by plotting Eq. (21.11) illustrates the THD of the output voltage as a function of the normalized load and frequency. As can be seen, for values of Q higher than 1 and for operation close to the natural frequency ($\Omega = 1$), the THD is low, which means that the output voltage is nearly a sinusoidal waveform. However, for low values of Q, the output voltage tends to be a square waveform, and the THD tends to the value of about 48%, corresponding to the THD of a square waveform. Fig. 21.19B illustrates the normalized output voltage for the fundamental component.

As stated previously, when used as lamp ballast, the current-fed parallel resonant inverter operates at the natural frequency of the resonant tank to both ignite the lamp and limit the current at normal running. Neglecting the effect of high-order harmonics, the rms output voltage is given by the fundamental component and can be obtained using $\Omega = 1$ in Eq. (21.9) as follows:

$$V_{0(\text{rms})} \asymp V_{0,1(\text{rms})} = I_{S,1(\text{rms})}Z_B Q = \frac{4I_S R}{\pi\sqrt{2}} \tag{21.12}$$

In a current-fed resonant inverter, the dc input current I_S is supplied from a dc voltage source V_{in} with a series choke, as stated previously. Then, the dc input current can be obtained, assuming 100% efficiency, by equaling input and output power as follows:

$$P_{in} = V_{in}I_S = \frac{V_{0(\text{rms})}^2}{R} \tag{21.13}$$

And then,

$$I_S = \frac{V_{0(\text{rms})}^2}{V_{in}R} \tag{21.14}$$

Using Eq. (21.14) in Eq. (21.12) and solving for the output voltage,

$$V_{0(\text{rms})} = \frac{\pi\sqrt{2}}{4}V_{in} = 1.1\ V_{in} \tag{21.15}$$

As can be seen, when operating at the natural frequency, the rms output voltage is independent of the resonant tank load. The peak output voltage is equal to $\pi V_{in}/2$. This value is directly related to the peak voltage stress in the switches. For a full-bridge topology, as shown in Fig. 21.11C, this value is equal to the switch voltage stress. However, for the current-fed push-pull inverter, the voltage stress is twice this value, which is πV_{in}, due to the presence of the transformer. This gives a very high voltage stress for the switches in this topology, which is the reason why the current-fed push-pull is mainly used to implement low-input-voltage ballasts.

On the other hand, lamp starting voltage can vary from 5 to 10 times the lamp voltage in normal discharge mode. This

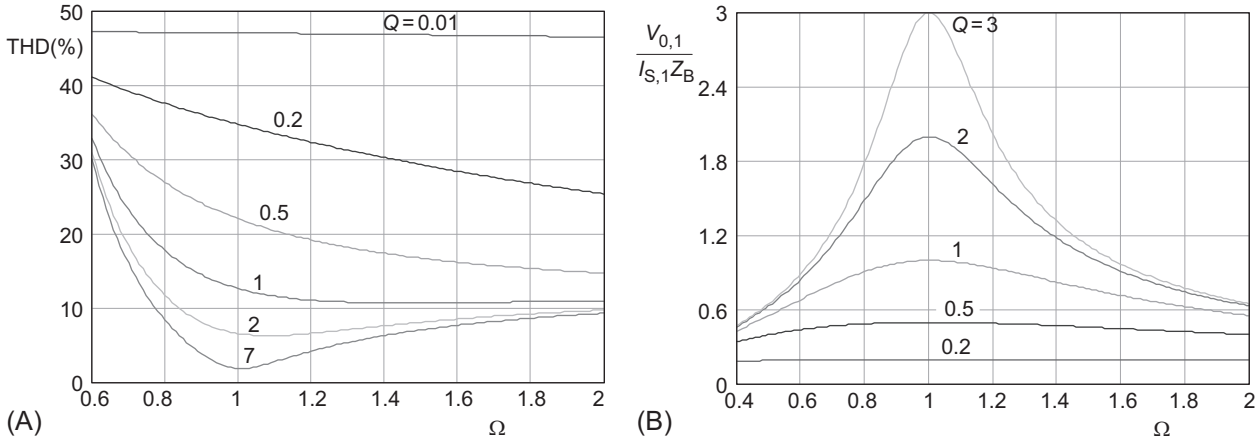


FIG. 21.19 Characteristics of the current-fed parallel resonant inverter: (a) THD and (b) fundamental output voltage.

makes the use of the current-fed parallel resonant inverter at constant frequency to both ignite the lamp and supply it at steady state difficult, since the output voltage is independent of the resonant tank load.

One solution to this problem is to ignite the lamp at the resonant tank natural frequency and then change the frequency to decrease the output voltage and output current to the normal running values of the lamp. This solution makes the use of extra circuitry to control the frequency necessary, normally in closed loop to avoid lamp instabilities, which increase the ballast cost.

Another solution, very often used in low-cost ballasts, is to design the parallel resonant tank to ignite the lamp and limit the lamp current in discharge mode by using an additional reactive element in series with the lamp. Normally, a capacitor is used to limit the lamp current in order to minimize the cost of the ballast. This solution is used in combination with the self-oscillating technique, which assures the operation at a constant frequency equal to the natural frequency of the resonant tank. Fig. 21.20A illustrates this circuit. Normally, the effect of the series capacitor is neglected, and the resonant tank is assumed to act as a sinusoidal voltage source during both ignition and normal operation, as shown in Fig. 21.20B. The high lamp starting voltage is obtained by means of a step-up transformer, which is the reason why typically a push-pull topology is used. If V_{in} is the dc input voltage and V_{ig} is the lamp ignition voltage, then the necessary transformer turn ratio is given by the following expression:

$$\frac{N_2}{N_1} = \frac{V_{ig}}{\pi V_{in}/2} \tag{21.16}$$

The rms lamp current in discharge mode can be approximated as follows:

$$I_{LA} = \frac{1.1\ (N_2/N_1)V_{in}}{\sqrt{R^2 + (1/2\pi f C_S)^2}} \tag{21.17}$$

where R is the equivalent resistance of the lamp. From Eq. (21.17), the necessary value of the series capacitor C_S, used to limit the lamp current to the nominal value I_{LA}, can be easily obtained.

Finally, Fig. 21.21A and B illustrates a typical ballast based on a current-fed resonant inverter and its equivalent circuit, respectively.

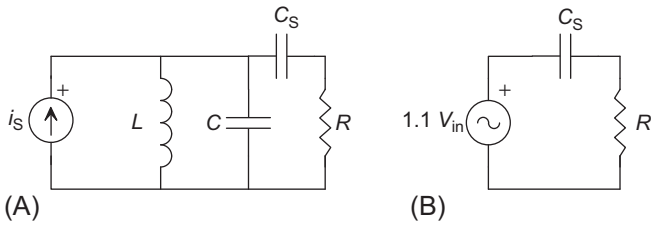


FIG. 21.20 (A) Typical parallel resonant circuit used to supply discharge lamps and (B) equivalent circuit.

21.4.2 Voltage-Fed Resonant Inverters

Some voltage-fed resonant inverters used to supply discharge lamps were previously shown in Fig. 21.12. Basically, they use two or more switches to generate a square voltage waveform. The different topologies are mainly given by the type of resonant tank used to filter this voltage waveform. There are three typical resonant tanks; their equivalent circuits are shown in Fig. 21.22. These circuits are the series-loaded resonant tank (Fig. 21.22A), the parallel-loaded resonant tank (Fig. 21.22B), and the series-parallel-loaded resonant tank (Fig. 21.22C). The typical operating waveforms are shown in Fig. 21.22D.

Similar to the current-fed resonant inverter, the input voltage can be expressed as a Fourier series in the following way:

$$v_s(t) = \sum_{n=1,3,5\ldots} V_{S,n} \sin\ n\omega t = \sum_{n=1,3,5\ldots} \frac{4V_S}{n\pi} \sin\ n\omega t \tag{21.18}$$

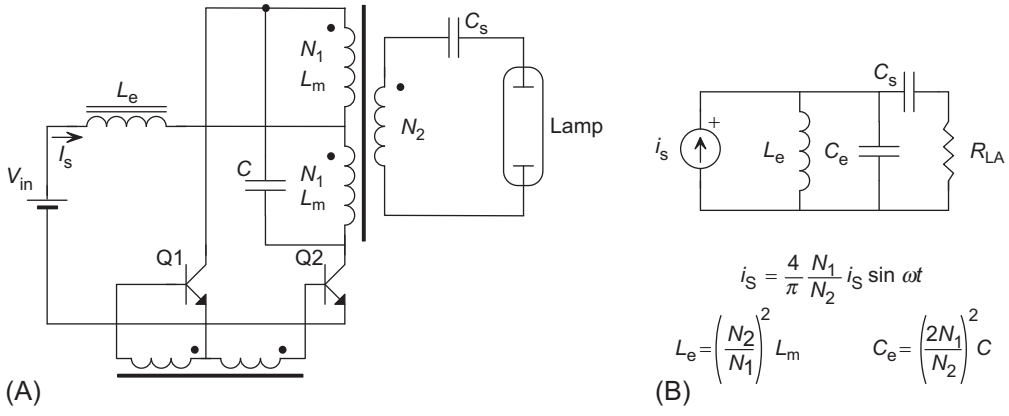


FIG. 21.21 (A) Self-oscillating current-fed push-pull electronic ballast and (B) equivalent circuit.

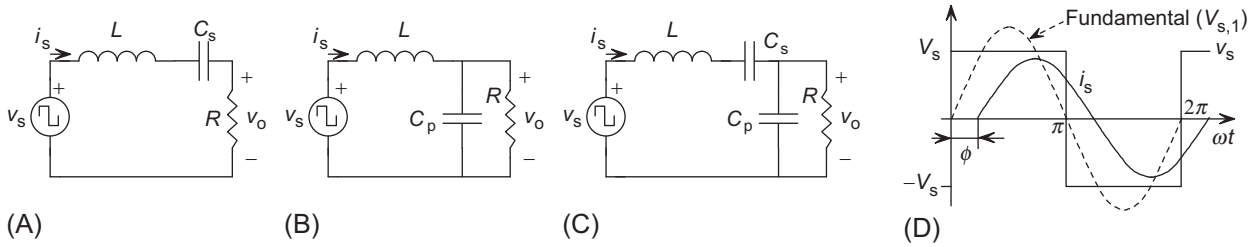


FIG. 21.22 (A–C) Equivalent circuits of voltage-fed resonant inverters and (D) typical operating waveforms.

$V_{S,n}$ being the peak value of each voltage harmonic and V_S the dc input voltage of the inverter. The same methodology as that used to analyze the current-fed resonant inverter will be used here to study the property of the three basic voltage-fed resonant inverters.

21.4.2.1 Series-Loaded Resonant Circuit

The output voltage corresponding to the n-order harmonic is easily obtained as follows:

$$V_{0,n} = V_{S,n} \frac{1}{\sqrt{1 + \frac{1}{Q_S^2}\left(n\Omega - \frac{1}{n\Omega}\right)^2}} \tag{21.19}$$

where Q_S and Ω are the normalized load and switching frequency given by the following expressions:

$$Q_S = R/Z_B = R(L/C_S)^{-1/2} \quad \Omega = \omega/\omega_0 = \omega\sqrt{LC_S} \tag{21.20}$$

Fig. 21.23A shows the THD of the series-loaded circuit, and Fig. 21.23B shows the fundamental output voltage, which is normally considered for design purposes.

In this circuit, the input and output currents are equal and can be calculated by dividing the output voltage by the load impedance. This current is also circulating through the inverter switches and therefore represents an important parameter for the design. Another important parameter is the phase angle of the input current, which defines the type of commutations in the inverter switches. For the fundamental harmonic, the phase angle of the current circulating through the resonant tank can be calculated as follows:

$$\varphi = -\tan^{-1}\frac{\Omega - 1/\Omega}{Q_S} \tag{21.21}$$

At the natural frequency (ω_0), the input voltage and current will be in phase, which means that there is no reactive energy handled by the circuit and all the input energy is transferred to the load at steady-state operation. For frequencies higher than ω_0, the current is lagged, and some reactive energy will be handled. In this case, the inverter switches will present ZVS [21]. For frequencies lower than ω_0, the current is in advance, and also some reactive energy will be handled. In this case, the inverter switches will present zero current switching (ZCS).

As can be seen in Fig. 21.23A, the THD is lower for the lower values of the normalized load and for frequencies close to the natural frequency of the resonant tank. For the higher values of Q_S, the THD tends to the value corresponding to a square wave. The output voltage is always lower than the input voltage, and for frequencies around the natural frequency, the circuit acts as a voltage source, especially for the high values of Q_S. This

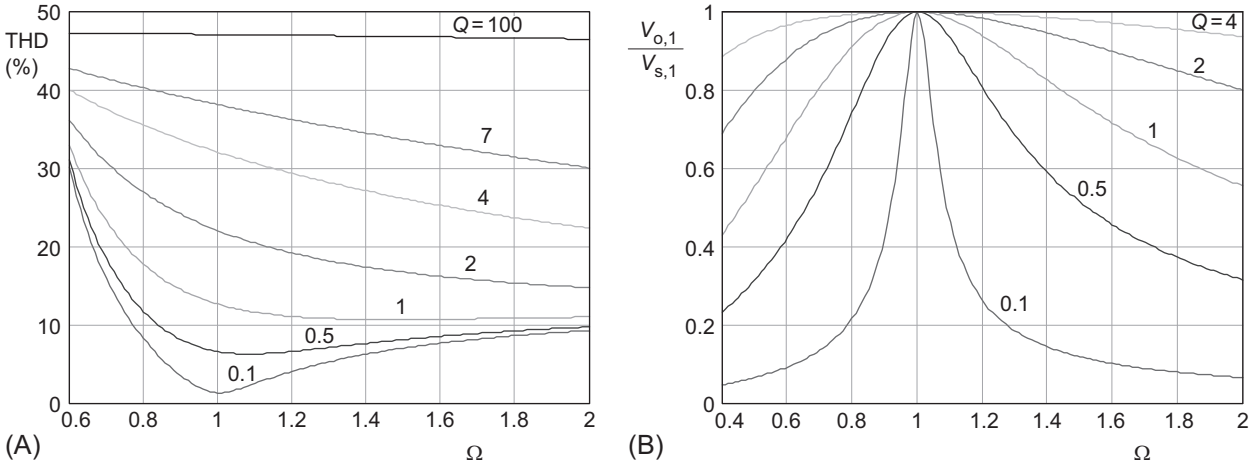


FIG. 21.23 Characteristics of series-loaded resonant inverter: (A) THD and (B) fundamental output voltage.

means that the lamp cannot be ignited and supplied in discharge mode, maintaining a constant switching frequency. This property is similar to that encountered for the current-fed resonant inverter. The use of step-up transformers is mandatory to achieve lamp ignition, especially for the low input voltages. In order to maintain the operating frequency constant, a series element will be necessary to limit the lamp current at normal discharge operation. A capacitor can also be used as expounded in the previous section. In summary, this circuit is mainly used in high input voltage and low-current applications, and it is not very frequently used to implement electronic ballasts.

21.4.2.2 Parallel-Loaded Resonant Circuit

In this circuit, the output voltage corresponding to the n-order harmonic is given by the following expression:

$$V_{0,n} = V_{S,n} \frac{1}{\sqrt{\dfrac{n^2\Omega^2}{Q_P^2} + \left(n^2\Omega^2 - 1\right)^2}} \tag{21.22}$$

where

$$Q_P = R/Z_B = R(L/C_P)^{-1/2} \quad \Omega = \omega/\omega_0 = \omega\sqrt{LC_P} \tag{21.23}$$

The THD and fundamental output voltage are shown in Fig. 21.24. This circuit has characteristics very much useful to implement electronic ballasts than the series-loaded resonant circuit. First, the THD of the output voltage around the natural frequency is in general quite lower than that of the series circuit. For the lower values of Q_P, the THD tends to a value of 12%, which corresponds to the THD of a triangular wave. As a result, the lamp voltage and current waveforms will be very similar to a sine wave, which is an adequate waveform to supply the lamp. Second, the frequency response of the output voltage (Fig. 21.24B) makes it possible to both ignite the lamp and limit the lamp current at steady state, maintaining a constant operating frequency. During ignition, the lamp shows a very high impedance, thus giving a high value of Q_P. Under these conditions, the parallel circuit can generate a very high output voltage, provided that the operating frequency is close to the natural frequency. Once the lamp is ignited, the normalized load Q_P decreases, and the circuit can limit the lamp current without changing the operating frequency. In fact, the parallel circuit operating close to the natural frequency acts as a current source for the load, as will be shown later. This is adequate to supply discharge lamps because it assures a good discharge stability, avoiding the lamp being easily extinguished by transitory power fluctuations.

The maximum value of the voltage gain shown in Fig. 21.24 can be calculated to be equal to $Q_P/\sqrt{1-1/4Q_P^2}$, and it appears at a frequency $\Omega_m = \sqrt{1-1/2Q_P^2}$. This means that a maximum is only present if Q_P is greater than $1/\sqrt{2} \asymp 0.71$. For the higher values of Q_P, the maximum gain can be approximated to Q_P, and the frequency of maximum gain can be approximated to the natural frequency ω_0.

The input current of the parallel resonant circuit is another important parameter to calculate the current handled by the inverter switches. Since the operating frequency is normally around resonance, only the fundamental component is considered. The value of this fundamental current and its phase angle can be obtained as follows:

$$I_{S,1} = \frac{V_{S,1}}{Z_B}\sqrt{\frac{1+Q_P^2\Omega^2}{\Omega^2 + Q_P^2\left(\Omega^2 - 1^2\right)}} \tag{21.24}$$

$$\varphi = \tan^{-1}\frac{-1}{\Omega Q_P} - \tan^{-1} Q_P\left(\Omega - \frac{1}{\Omega}\right) \tag{21.25}$$

The condition for the input voltage being in phase with the input current can be obtained by equaling Eq. (21.25) to zero.

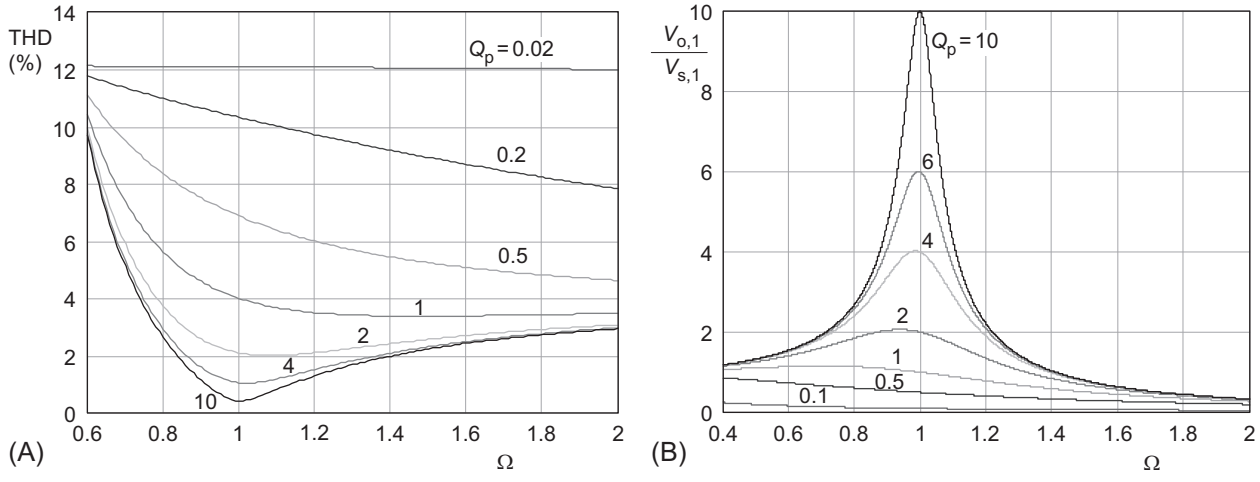


FIG. 21.24 Characteristics of parallel-loaded resonant inverter: (A) THD and (B) fundamental output voltage.

This gives a value of the normalized frequency, which is $\Omega_{\varphi=0}=\sqrt{1-1/Q_P^2}$. For a frequency greater than that value, the input current will lag the input voltage, and the inverter switches will present ZVS. For frequencies lower than that value, the current will be in advance, and zero current switching is obtained. The output voltage gain at that frequency is equal to Q_P.

Finally, it is very interesting to study the characteristic of this circuit for frequencies close to the natural frequency ω_0 ($\Omega=1$), since this is the normal region selected to operate for ballast applications. At this frequency, the output voltage gain is equal to Q_P, and then, the output current will be $V_{S,1}/Z_B$. This means that when operated at the natural frequency, the parallel circuit acts as a current source, whose value only depends on the input voltage. At the natural frequency, the input current is equal to $V_{S,1}\sqrt{1+Q_P^2}/Z_B$, and the phase angle is equal to $\tan^{-1}(-1/Q_P)$. The circuit is always inductive, with ZVS, and the phase angle decreases when Q_P increases, which means that less reactive energy is handled by the circuit.

21.4.2.3 Series-Parallel-Loaded Resonant Circuit

This circuit is also very widely used to implement electronic ballasts. The fundamental output voltage is given by the following expression:

$$V_{0,1}=V_{S,1}\frac{1}{\sqrt{\frac{1}{Q_{SP}^2}\left(\Omega-\frac{1-\alpha}{\Omega}\right)^2+\frac{1}{\alpha^2}\left(\Omega^2-1\right)^2}} \tag{21.26}$$

where

$$Q_{SP}=R/Z_B=R(L/C_E)^{-1/2}\qquad \Omega=\omega/\omega_o=\omega\sqrt{LC_E}$$
$$\alpha=C_E/C_P=1-C_E/C_S \tag{21.27}$$

and $C_E=C_SC_P/(C_S+C_P)$ is the series equivalent of the two capacitors present in this resonant circuit.

The fundamental input current and its phase angle are the following:

$$I_{S,1}=\frac{V_{S,1}}{Z_B}\left[\frac{1+\left(\Omega^2Q_{SP}^2/\alpha^2\right)}{\left(\Omega-(1-\alpha/\Omega)\right)^2+\left(Q_{SP}^2/\alpha^2\right)\left(\Omega^2-1\right)^2}\right]^{1/2} \tag{21.28}$$

$$\varphi=\begin{cases}\tan^{-1}\dfrac{-\alpha}{Q_{SP}\Omega}-\tan^{-1}\left(\dfrac{Q_{SP}}{\alpha}\dfrac{\Omega^2-1}{\Omega-((1-\alpha)/\Omega)}\right)+180^\circ \\ \quad \text{if}\quad \Omega<\Omega_C=\sqrt{1-\alpha} \\ \tan^{-1}\dfrac{-\alpha}{Q_{SP}\Omega}-\tan^{-1}\left(\dfrac{Q_{SP}}{\alpha}\dfrac{\Omega^2-1}{\Omega-((1-\alpha)/\Omega)}\right) \\ \quad \text{if}\quad \Omega\geq\Omega_C=\sqrt{1-\alpha}\end{cases} \tag{21.29}$$

Fig. 21.25 shows the characteristics corresponding to the THD of the output voltage and the fundamental output voltage for $\alpha=0.5$. As can be seen, the THD is also very low around the natural frequency, especially for the higher values of the normalized load Q_{SP}. Regarding the output voltage, this circuit acts as a parallel circuit around the natural frequency ω_0, with a maximum gain voltage of about Q_{SP}/α. Around the natural frequency of the series circuit given by L and C_S, $\omega_{0S}=\omega_0\sqrt{1-\alpha}$, the circuit acts as a series-loaded circuit with a maximum voltage gain equal to unity.

The series-parallel circuit can also be used to both ignite and supply the lamp at constant frequency, since it also acts as a current source at the natural frequency. Besides, this circuit allows to limit the ignition voltage by means of the factor α, thus avoiding sputtering damage of lamp electrodes. Also, the series capacitor can be used to block any dc component of the inverter square output voltage, as that existing in the asymmetrical half bridge. In summary, the series-parallel circuit combines the best features of the series-loaded and the

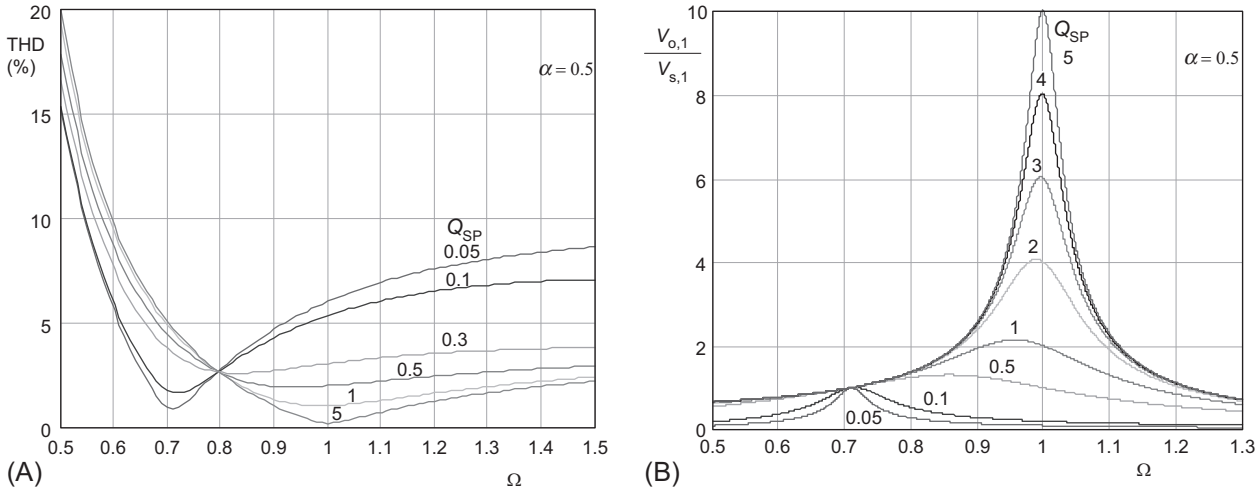


FIG. 21.25 Characteristics of series-parallel-loaded resonant inverter: (A) THD and (B) fundamental output voltage.

parallel-loaded; this is the reason why it is used widely to implement electronic ballasts.

When operated at frequency ω_0, the output voltage gain is equal to Q_{SP}/α, and then, the circuit acts as a current source equal to $V_{S,1}/\alpha Z_B$, which is independent of the load. As stated previously, this current source behavior is adequate to supply discharge lamps because it allows the lamp current to be limited all the time. The input current phase angle at this frequency is equal to $\tan^{-1}(-\alpha/Q_{SP})$, and the input current always lags the input voltage, thus showing ZVS operation.

Finally, the condition to have input current in phase with the input voltage can be obtained by equaling Eq. (21.27) to zero. This gives the following value:

$$Q_{SP,\varphi=0} = \frac{\alpha}{\Omega}\sqrt{\frac{\Omega^2-(1-\alpha)}{(1-\Omega^2)}} \tag{21.30}$$

Eq. (21.30) defines the borderline between the ZVS and the ZCS modes. The output voltage gain in this borderline can be obtained by using Eq. (21.30) in Eq. (21.26), and it is equal to $\alpha/\sqrt{\alpha(1-\Omega^2)}$.

21.4.3 Design Issues

The design methodology of a resonant inverter for discharge lamp supply can be very different depending on the lamp type and characteristics, inverter topology, design goals, etc. Some guidelines, especially focused for supplying fluorescent lamps with voltage-fed resonant inverters, are presented in this section to illustrate the basic design methodology.

A typical starting process for a hot-cathode fluorescent lamp is shown in Fig. 21.26. Initially, lamp electrodes are heated up to the emission temperature. During this phase, the inverter should assure a voltage applied to the lamp not high enough to produce sputtering damage in lamp electrodes, thus avoiding premature aging of the lamp. Once electrodes reach the emission temperature, the lamp can be ignited by applying the necessary starting voltage. Following this procedure, a soft starting is achieved, and a long lamp life is assured.

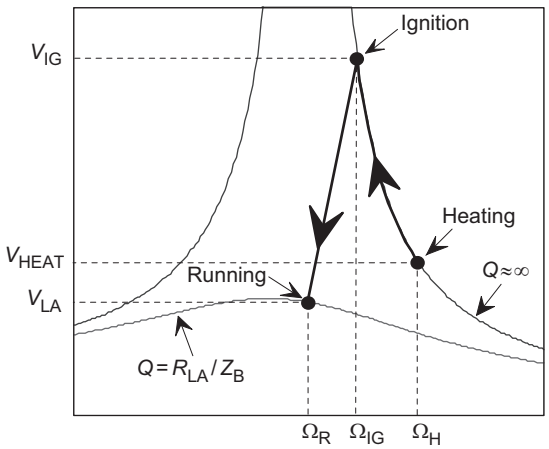


FIG. 21.26 Typical starting process of discharge lamps.

The best method to perform this soft starting is to control the inverter switching frequency, so that the lamp voltage and current are always under control. During the heating process, the operating frequency is adjusted to a value above the natural frequency of the resonant tank. In this way, the heating current can be adjusted to the necessary value, maintaining a lamp voltage quite lower than the starting voltage. Since normally MOSFET or bipolar transistors are used, the operation over the natural frequency is preferable because they provide ZVS, and the slow parasitic diodes existing in these transistors can be used. After a short period of time, the switching frequency is reduced until the starting voltage is obtained, and then, the lamp is ignited. Normally, the final operating point at steady-state operation is adjusted to be at a switching frequency equal to the natural frequency, so that a very stable operation for the lamp is assured.

Fig. 21.27A shows a fluorescent lamp supplied using a series-parallel-loaded resonant tank. The input data for the design are normally the fundamental input voltage V_S, the switching frequency in normal discharge operation (running) f_S, the lamp voltage and current at high frequency V_{LA} and I_{LA}, the electrode heating current I_H, the maximum lamp voltage during heating process V_H, and the lamp starting voltage V_{IG}.

The equivalent circuit during the heating and ignition phase is shown in Fig. 21.27B. The current circulating in this circuit is the electrode heating current, which can be calculated by using $Q_{SP}=\infty$ in Eq. (21.24):

$$I_H = \frac{V_S/Z_B}{\Omega - 1/\Omega} \tag{21.31}$$

where the electrode resistance has been neglected for simplicity. For a given heating current I_H, the necessary switching frequency is obtained from Eq. (21.31) as follows:

$$\Omega_H = \frac{V_S}{2Z_B I_H} + \sqrt{1+\left(\frac{V_S}{2Z_B I_H}\right)^2} \tag{21.32}$$

Regarding the heating voltage, it can be calculated from Eq. (21.26) using $Q_{SP}=\infty$, and the following value is obtained:

$$V_H = \frac{\alpha V_S}{\Omega_H^2 - 1} \tag{21.33}$$

The frequency at which the starting voltage is achieved can also be obtained using $Q_{SP}=\infty$ in Eq. (21.26), giving the following value:

$$\Omega_{IG} = \sqrt{1+\alpha\frac{V_S}{V_{IG}}} \tag{21.34}$$

Once the lamp is ignited, the new operation circuit is shown in Fig. 21.27C. Normally, the switching frequency is selected to be

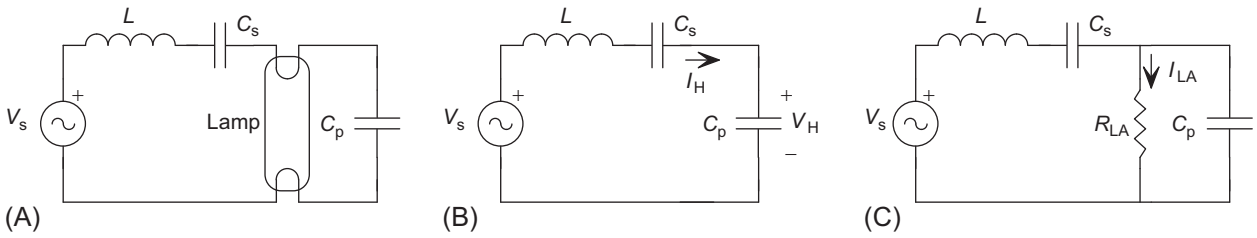


FIG. 21.27 (A) Fluorescent lamp supplied with a series-parallel circuit, (B) equivalent circuit during heating and ignition, and (C) equivalent circuit during normal discharge mode.

very close to the natural frequency, and the circuit characteristics can be obtained by using $\Omega = 1$. Thus, as stated previously, the circuit acts as a current source of the following value:

$$I_{LA} = \frac{V_S}{\alpha Z_B} \tag{21.35}$$

From this equation, the impedance Z_B needed to provide a lamp current equal to I_{LA} is easily obtained:

$$Z_B = \frac{V_S}{\alpha I_{LA}} \tag{21.36}$$

Using Eqs. (21.31)–(21.36), the design procedure can be performed as follows:

Step 1 Steady-state operation. Choose a value for the factor α; normally, a value of 0.8–0.9 will be adequate for most applications. From Eq. (21.36), calculate the value of Z_B for the resonant tank. Since the natural frequency is equal to the switching frequency, the reactive elements of the resonant tank can be calculated as follows:

$$L = \frac{Z_B}{2\pi f_S} \quad C_P = \frac{1}{2\pi f_S \alpha Z_B} \quad C_S = \frac{1}{2\pi f_S (1-\alpha) Z_B} \tag{21.37}$$

Step 2 Heating phase. From Eq. (21.32), calculate the switching frequency for a given heating current I_H. Then, calculate the value of the heating voltage V_H from Eq. (21.33).

Step 3 Check if the heating voltage is lower than the maximum value allowed to avoid electrode sputtering. If the voltage is too high, choose a lower value of α and repeat steps 1 and 2. Also, the maximum heating frequency can be limited to avoid excessive frequency variation. The lower the α, the lower is the frequency variation from heating to ignition, since the output voltage characteristics are narrower for the lower values of α.

The described procedure to achieve lamp soft ignition requires the use of a voltage-controlled oscillator to control the switching frequency. This can increase the cost of the ballast. A similar soft ignition can be achieved using the resonant circuit shown in Fig. 21.28. This circuit is very often used in self-oscillating ballasts, where the switches are driven from the resonant current using a current transformer [22].

In the circuit shown in Fig. 21.28, the PTC is initially cold, and capacitor C_{P1} is practically short-circuited by the PTC.

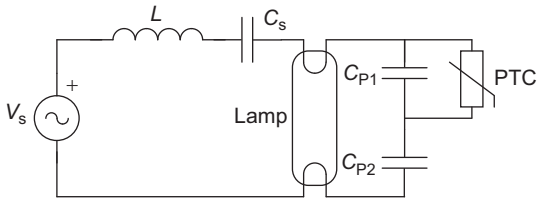


FIG. 21.28 Resonant circuit using a PTC resistor.

The resonant tank under these conditions is formed by L-C_S-C_{P2}, which can be designed to heat the lamp electrodes with a heating voltage low enough to avoid lamp cold ignition. Since the PTC is also heated by the circulating current, after a certain period of time, it reaches the threshold temperature and trips. At this moment, the new resonant tank is formed by L, C_S, and the series equivalent of C_{P1} and C_{P2}. This circuit can be designed to generate the necessary ignition voltage and to supply the lamp in normal discharge mode. Once the lamp is ignited, the PTC maintains its high impedance since the dominant parallel capacitor in this phase is C_{P1} (usually $C_{P1} \ll C_{P2}$).

21.5 High-Power Factor Electronic Ballasts

As commented in a previous section, when electronic ballasts are supplied from the ac line, an ac-dc stage is necessary to provide the dc input voltage of the resonant inverter (see Fig. 21.9). Since the introduction of harmonic regulations, as IEC 1000-3-2, the use of a full-bridge diode rectifier followed by a filter capacitor is no longer applicable for this stage due to the high harmonic content of the input current. Therefore, the use of an ac-dc stage showing a high input power factor (PF) and a low total harmonic distortion (THD) of the input current is mandatory. The inclusion of this stage can significantly increase the cost of the complete ballast, and therefore, the search for low-cost high-power-factor electronic ballasts is presently an important field of research.

Fig. 21.29A shows a first possibility to increase the input power factor of the ballast by removing the filter capacitor across the diode rectifier. However, since there are no low-frequency storage elements inside the resonant inverter, the

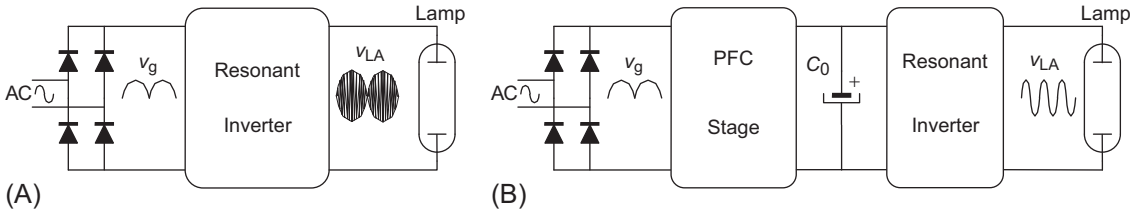


FIG. 21.29 High-power-factor ballasts.

output power instantaneously follows the input power, thus producing an annoying light flicker. Besides, the resulting lamp current crest factor is very high, which considerably decreases lamp life.

In order to avoid flicker and increase lamp current crest factor, continuous power must be delivered to the lamp. This can only be accomplished by using a PFC stage with a low-frequency storage element. This solution is shown in Fig. 21.29B, where capacitor C_0 is used as energy storage element. The main drawback of this solution is that the input power is handled by the two stages, which reduces the efficiency of the complete electronic ballast.

21.5.1 Harmonic Limiting Standards

The standards IEC 1000-3-2 and EN 61000-3-2 [23] are the most popular regulations regarding the harmonic pollution produced by electronic equipment connected to the mains. These standards are a new version of the previous IEC 555-2 regulation, and they are applicable to the equipment with less than 16 A/phase and supplied from low voltage lines of 220/380 V, 230/400 V, and 240/415 V at 50 or 60 Hz. Limits for equipment supplied from voltages lower than 220 V have not yet been established.

This regulation divides the electric equipment in several classes from class A to class D. Class C is especially for lighting equipment, including dimming devices; the harmonic limits for this class are shown in Table 21.4. As shown in Table 21.4, this regulation establishes a maximum amplitude for each input harmonic as a percentage of the fundamental harmonic component. The harmonic content established in Table 21.4 is quite restrictive, which means that the input current wave must be quite similar to a pure sine wave. For example, for a typical input power factor equal to 0.9, the THD calculated from Table 21.1 is only 32%.

TABLE 21.4 IEC 1000-3-2. Harmonic limits for class C equipment

Harmonic order n	Maximum permissible harmonic current expressed as a percentage of the input current at the fundamental frequency (%)
2	2
3	30λ[a]
5	10
7	7
9	5
$11 \leq n \leq 39$ (odd harmonics only)	3

[a] λ is the circuit power factor.

21.5.2 Passive Solutions

A first possibility to increase the ballast power factor and to decrease the harmonic content of the input current is the use of passive solutions. Fig. 21.30 shows two typical passive solutions, which can be used to improve the input power factor of electronic ballasts.

Fig. 21.30A shows the most common passive solution based on a filter inductor L. Using a large inductance L, a square input current can be obtained, with an input power factor of 0.9 and a THD of about 48%. However, a square input waveform does not satisfy the IEC 1000-3-2 requirements, and then, it is not a suitable solution. The addition of capacitor C across the ac terminals can increase the power factor up to 0.95, but still, the standard requirements are difficult to fulfill.

A simple variation of this circuit is shown in Fig. 21.30B, where a parallel circuit tuned to the third harmonic of the line frequency is used to improve the shape of the line current. The input power factor obtained with this circuit can be close to unity.

A third possible solution, known as valley-fill circuit, is shown in Fig. 21.31A. The typical filter capacitor following the diode rectifier is split into two different capacitors that are alternately charged using three extra diodes. The addition of a small series resistor improves the power factor by about two points, maintaining a low cost for the circuit. An inductor in place of the resistor can also be used to improve the power factor but with a higher cost penalty. Fig. 21.31B shows the output voltage and input current of the valley-fill circuit. The main disadvantage of this circuit is the high ripple of the output voltage, which produces lamp power and luminous flux fluctuation and high lamp current crest factor.

Passive solutions are reliable, rugged, and cheap. However, the size and weight of these solutions are high, and their design to fulfill the IEC 1000-3-2 requirements is usually difficult. Therefore, they are normally applied in the lower power range.

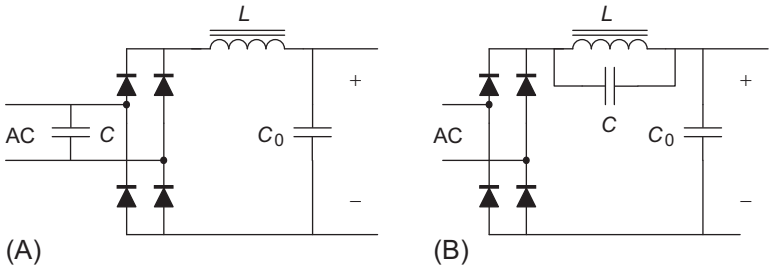


FIG. 21.30 Passive circuits to improve input power factor: (A) LC filter and (B) tuned LC filter.

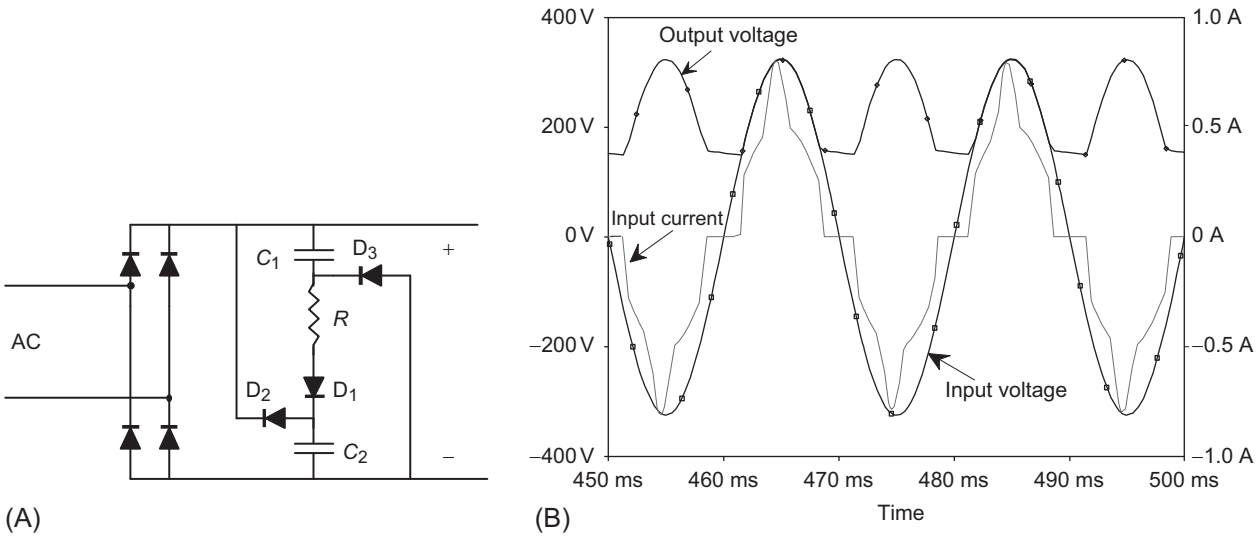


FIG. 21.31 Valley-fill circuit: (A) electric diagram and (B) waveforms.

21.5.3 Active Solutions

Active circuits are the most popular solutions to implement high-power-factor electronic ballasts. They use controlled switches to correct the input power factor and in some cases to include galvanic isolation via high-frequency transformers. Active circuits normally used in electronic ballasts operate at a switching frequency well above the line frequency and over the audible range.

Some typical active circuits used in electronic ballasts are shown in Fig. 21.32. Buck-boost and flyback converters shown in Fig. 21.32A and B, respectively, can be operated in discontinuous conduction mode (DCM) with constant frequency and constant duty cycle in order to obtain an input power factor close to unity [24].

Fig. 21.32C shows the boost converter, which is one of the most popular active circuits used to correct the input power factor of electronic ballasts [25–27]. If the boost converter is operated in DCM, an input power factor close to unity is obtained, provided that the output voltage is about twice the peak input voltage [25]. The main disadvantage of DCM operation, when compared with the CCM mode, is the high distortion of the input current (due to the discontinuous high-frequency current) and the higher current and voltage stresses

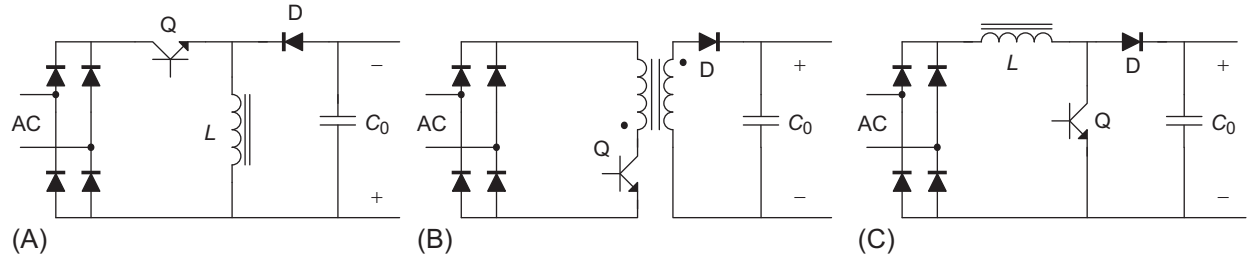


FIG. 21.32 Power factor correction circuits for ballasts: (A) buck-boost, (B) flyback, and (C) boost.

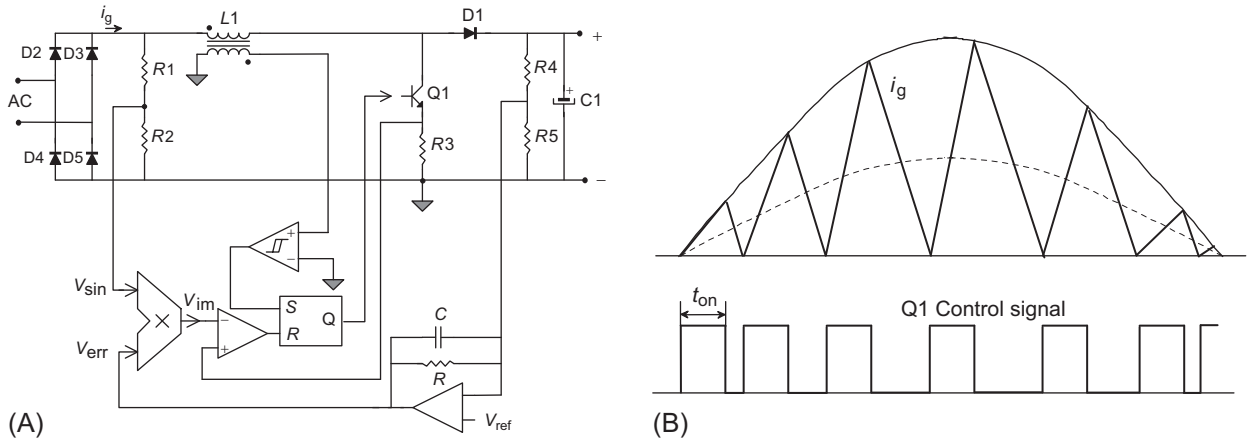


FIG. 21.33 (A) Boost power factor corrector with borderline control and (B) input current waveform.

in the switches. Therefore, the DCM operation is only used for the lower power range.

For the medium power range, the operation of the boost converter at the DCM-CCM borderline is preferred. In this solution, the on time of the controlled switch is maintained constant within the whole line period, and the switching frequency is adjusted to allow the input current to reach zero at the end of the switching period. The typical control circuit used and the input current waveform are shown in Fig. 21.33A and B, respectively. The inductor current is sensed using a resistor in series with the switch, and the peak inductor current is programmed to follow a sine wave using a multiplier. A comparator is employed to detect the zero crossing of the inductor current in order to activate the switch. Most IC manufacturers provide a commercial version of this circuit to be used for electronic ballast applications.

The boost circuit operating with borderline control provides a continuous input current, which is easier to filter. Besides, it presents low switch turn-on losses and low recovery losses in the output diode. The main disadvantages are the variable switching frequency and the high output voltage, which must be higher than the peak line voltage.

For the higher power range, the boost converter can be operated in continuous conduction mode (CCM) to correct the input power factor. The input current in this scheme is continuous with very low distortion and easy to filter. The current stress in the switch is also lower, which means that more power can be handled maintaining a good efficiency. The normal efficiency obtained with a boost circuit operating either in the DCM-CCM borderline or in CCM can be as high as 95%.

21.6 Applications

Electronic ballasts are widely used in lighting applications, such as portable lighting, emergency lighting, automotive applications, home lighting, and industrial lighting. They provide low volume and size, making it possible to reduce the luminaire size as well, which is a very interesting new trend in lighting design.

21.6.1 Portable Lighting

In this application, a battery is used as power source, and then, a low input voltage is available to supply the lamp. Examples are hand lanterns and backlightings for laptop computers. Typical input voltages in these applications range from 1.5 to 48 V. Therefore, a step-up converter is necessary to supply the discharge lamp, and then, electronic ballasts are the only suitable solution. Since the converter is supplied from a battery, the efficiency of the ballast should be as high as possible in order to optimize the use of the battery energy, thus increasing the operation time of the portable lighting. Typical topologies used are the class E inverter and the push-pull resonant inverter, obtaining efficiencies up to 95%.

21.6.2 Emergency Lighting

Emergency lightings are used to provide a minimum lighting level in case of a main supply cutoff. Batteries are employed to store energy from the mains and to supply the lamp in case of a main supply failure. A typical block diagram is shown in Fig. 21.34. An ac-dc converter is used as a battery charger to store energy during normal line operation. A control circuit continuously measures the line voltage and activates the inverter in case of a main supply failure. Normally, a minimum operating time of 1 h is required for the system in emergency state. Thus, the use of highly efficient electronic ballasts is mandatory to reduce the battery size and cost. Typical topologies used include class E inverters, push-pull resonant inverters, and half-bridge resonant inverters. Fluorescent lamps are mainly used in emergency ballasts, but high-intensity discharge lamps, such as metal halide lamps or high-pressure sodium lamps, are also used in some special applications.

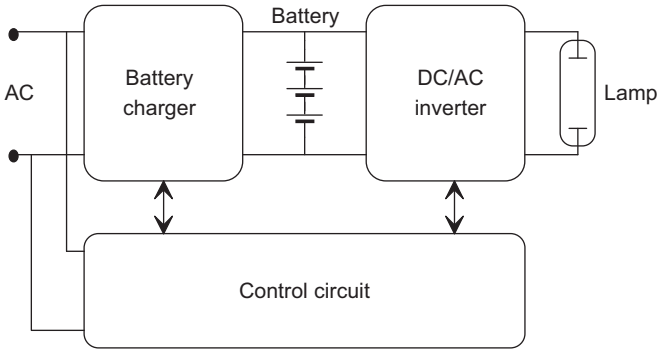


FIG. 21.34 Block diagram of an emergency lighting.

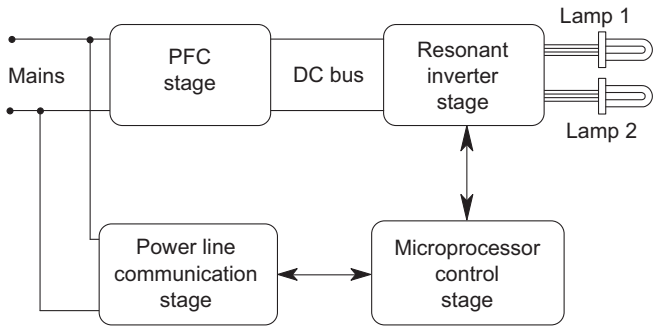


FIG. 21.35 Block diagram of a microprocessor-based lighting.

21.6.3 Automotive Lighting

Electronic ballasts are used in automotive applications such as automobiles, buses, trains, and aircrafts. Normally, a low-voltage dc bus is available to supply the lamps. These applications are similar to portable and emergency lightings previously commented. In modern aircrafts, a 120/208 V, 400 Hz, three-phase electric system is also available and can be employed for lighting. Fluorescent lamps are typically used for automotive indoor lighting, whereas high-intensity discharge lamps are preferred in the exterior lighting, for example, in automobile headlights.

21.6.4 Home and Industrial Lighting

Electronic ballasts, especially for fluorescent lamps, are also very often used in home and industrial applications. The higher efficiency of fluorescent lamps supplied at high frequency provides an interesting energy saving when compared with incandescent lamps. A typical application is the use of compact fluorescent lamps with the electronic ballast inside the lamp base, which can directly substitute an incandescent lamp reducing the energy consumption four or five times. A self-oscillating half-bridge inverter is typically used in these energy saving lamps, since it allows to reduce the size and cost. The power of these lamps is normally below 25 W.

Other applications for higher power include more developed ballasts based on a power factor correction stage followed by a resonant inverter. Hot-cathode fluorescent lamps are mostly used in these electronic ballasts. Also, with the development of modern HID lamps such as metal halide lamps and very-high-pressure sodium lamps (both showing very good color rendition), the use of HID lamps is being more and more frequent in home, commercial, and industrial lighting.

21.6.5 Microprocessor-Based Lighting

The use of microprocessors in combination with electronic ballasts is very interesting from the point of view of energy saving [28–30]. The inclusion of microprocessor circuits allows to incorporate control strategies for dimming, such as scheduling, task tuning, and daylighting [31]. Using these strategies, the achieved energy saving can be as high as 35%–40%. Another advantage of using microprocessors is the possibility of detecting lamp failure or bad operation, thus increasing the reliability and decreasing the maintenance cost of the installation. Most advanced electronic ballasts can include a communication stage to send and receive information regarding the state of the lighting to or from a central control unit. In some cases, communications can be performed via power line, thus reducing the installation costs. Fig. 21.35 shows the block diagram of a microprocessor-based electronic ballast.

References

[1] G. Wyszecki, W.S. Stiles, Color Science: Concepts and Methods, Quantitative Data and Formulae, John Wiley & Sons, Second Edition, 1982.
[2] J.A. Borton, K.A. Daley, A comparison of light sources for the petrochemical industry, IEEE Ind. Appl. Mag. (1997) 54–62.
[3] Chr. Meyer, H. Nienhuis, Discharge Lamps. Philips Technical Library, 1988.
[4] Illuminating Engineering Society of North America, IES Lighting Handbook, 1984 Reference Volume, IESNA, New York, 1984.
[5] W.R. Alling, Important design parameters for solid-state ballasts, IEEE Trans. Ind. Appl. 25 (2) (1989) 203–207.
[6] J. De Groot, J. Van Vliet, The High-Pressure Sodium Lamp, Philips Technical Library, Macmillan Education, 1986.
[7] Y. Koshimura, N. Aoike, O. Nomura, Stable high frequency operation of high intensity discharge lamps and their ballast design, in: Proc. CIE 20th Session'83, 1983. E36/1–E36/2.
[8] L. Laskai, P.N. Enjeti, I.J. Pitel, White-noise modulation of high-frequency high-intensity discharge lamp ballasts, IEEE Trans. Ind. Appl. 34 (3) (1998) 597–605.
[9] A.S. Simoes, M.M. Silva, A.V. Anunciada, A boost-type converter for DC-supply of fluorescent lamps, IEEE Trans. Ind. Electron. 41 (2) (1994) 251–255.
[10] D.M. Vasiljevic, The design of a battery-operated fluorescent lamp, IEEE Trans. Ind. Electron. 36 (4) (1989) 499–503.
[11] M. Hernando, C. Blanco, J.M. Alonso, M. Rico, Fluorescent lamps supplied with dc current and controlled in current mode,

in: Proceedings of European Power Electronics Conference (EPE), Firenze, 1991, pp. 1/499–1/503.
[12] E.L. Corominas, J.M. Alonso, A.J. Calleja, J. Ribas, M. Rico, Analysis of tapped-inductor inverters as low-power fluorescent lamp ballast supplied from a very low input voltage, in: PESC Conference Record, 1999, pp. 1103–1108.
[13] J.L. Duarte, J. Wijntjens, J. Rozenboom, Getting more from fluorescent lamps through resonant converters, in: Proceedings of IECON, San Diego, 1992.
[14] M. Ponce, J. Arau, J.M. Alonso, M. Rico-Secades, Electronic ballast based on class E amplifier with a capacitive inverter and dimming for photovoltaic applications, in: Proceedings of APEC, 1998, pp. 1156–1162.
[15] M. Gulko, S. Ben-Yaakov, Current-sourcing push-pull parallel-resonance inverter (CS-PPRI): theory and application as a discharge lamp driver, IEEE Trans. Ind. Electron. 41 (3) (1994) 285–291.
[16] M.-S. Lin, W.-J. Ho, F.-Y. Shih, D.-Y. Chen, Y.-P. Wu, A cold-cathode fluorescent lamp driver circuit with synchronous primary-side dimming control, IEEE Trans. Ind. Electron. 45 (2) (1998) 249–255.
[17] M.H. Rashid, Power Electronics. Circuits, Devices, and Applications, second ed., Prentice Hall, New Jersey, 1993.
[18] U. Mader, P. Horn, A dynamic model for the electrical characteristics of fluorescent lamps, in: IEEE Industry Applications Society Meeting Conference, 1992, pp. 1928–1934. Records.
[19] M. Sun, B.L. Hesterman, Pspice high-frequency dynamic fluorescent lamp model, IEEE Trans. Power Electron. 13 (2) (1998) 261–272.
[20] K.J. Tseng, Y. Wang, D.M. Vilathgamuwa, An experimentally verified hybrid Cassie-Mayr electric arc model for power electronics simulations, IEEE Trans. Power Electron. 12 (3) (1997) 429–436.
[21] J.M. Alonso, C. Blanco, E. López, A.J. Calleja, M. Rico, Analysis, design and optimization of the LCC resonant inverter as a high-intensity discharge lamp ballast, IEEE Trans. Power Electron. 13 (3) (1998) 573–585.
[22] Electronics Ballasts for Fluorescent Lamps Using BUL770/791 Transistors. Application Report, Texas Instruments, 1992.
[23] IEC 1000-3-2 (1995-03) standards on electromagnetic compatibility (EMC), Part 3, Section 2: Limits for harmonic current emissions. International Electrotechnical Commission, Switzerland: Geneva, April 1995.
[24] J.M. Alonso, A.J. Calleja, E. López, J. Ribas, M. Rico, A novel single-stage constant-wattage high-power-factor electronic ballast, IEEE Trans. Ind. Electron. 46 (6) (1999) 1148–1158.
[25] K.-H. Liu, Y.-L. Lin, Current waveform distortion in power factor correction circuits employing discontinuous-mode boost converters, in: Power Electronics Specialists Conference proceedings, 1989, pp. 825–829.
[26] J.S. Lai, D. Chen, Design consideration for power factor correction boost converter operating at the boundary of continuous conduction mode and discontinuous conduction mode, in: Applied Power Electronics Conference Proceedings, 1993, pp. 267–273.
[27] C. Blanco, J.M. Alonso, E. López, A.J. Calleja, M. Rico, A single-stage fluorescent lamp ballast with high power factor, in: IEEE APEC'96 proceedings, 1996, pp. 616–621.
[28] W.R. Alling, The integration of microcomputers and controllable output ballasts—a new dimension in lighting control, IEEE Trans. Ind. Appl. (1984) 1198–1205.
[29] J.M. Alonso, J. Díaz, C. Blanco, M. Rico, A microcontroller-based emergency ballast for fluorescent lamps, IEEE Trans. Ind. Electron. 44 (2) (1997) 207–216.
[30] J.M. Alonso, J. Ribas, A.J. Calleja, E. López, M. Rico, An intelligent neuron-chip-based fluorescent lamp ballast for indoor applications, in: Conference Proceedings of the IEEE Industry Applications Society Annual Meeting (IAS'97), New Orleans, Louisiana, 1997, pp. 2388–2394.
[31] Illuminating Engineering Society of North America, IES Lighting Handbook, 1984 Application Volume, IESNA, New York, 1987.

22

Wireless Power Transfer

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22.1 Introduction

Wireless power transfer (WPT), in its general term, has been around us for decades in applications such as telemetry, satellite communications, and radio frequency identification (RFID) tags. Most of these applications transfer low amounts of power, in the range of microwatts to milliwatts, for data transfer. For higher-power applications, from few watts to several kilowatts, over moderate distances, the WPT has recently been the focus of the industrial developments. The most common method of high power WPT is through inductive coupling that was invented by Nikola Tesla more than a century ago. The recent developments in semiconductor industry for high frequency and high-power applications have paved the path for high-power inductive WPT improvements. Inductive WPT offers several benefits over the wired connection and is applied in numerous applications such as wearable electronics, health care, and automotive industry. This chapter starts by reviewing various methods of WPT, followed by the design and analysis of inductive WPT. The overall inductive WPT is studied step by step and component by component; therefore, it is recommended to refer to the references for detailed analysis and information.

22.2 Methods of Wireless Power Transfer

There are different methods to wirelessly transfer power between a source and a receiver. Each method has its own characteristics that are useful for certain applications. Here, the most common methods of wireless power transfer are briefly discussed.

Radio frequency waves. Radio frequency (RF) is the most common way of transmitting data as the waves can propagate through vacuum (Fig. 22.1A). RF waves can also be used to transmit power such as in microwave oven and in RF heater and welding machines. The operating principle of RF transmitting and receiving antennas is based on the interaction of electric and magnetic inductions determined by the full set of Maxwell's equations [1].

Optical link. Optical links use the light—in the ultraviolet, visible, and infrared regions of electromagnetic frequency spectrum—to transfer energy between source and receiver over long distances (Fig. 22.1B). The light-emitting source can be sun or power laser diodes for high power delivery and LED for data transmission [2]. The receiver unit is a light-sensitive device such as photovoltaic converter, solar cell, or photodiode. The optical link can be free space, air, fiber optics (it can be considered a wireless link due to the

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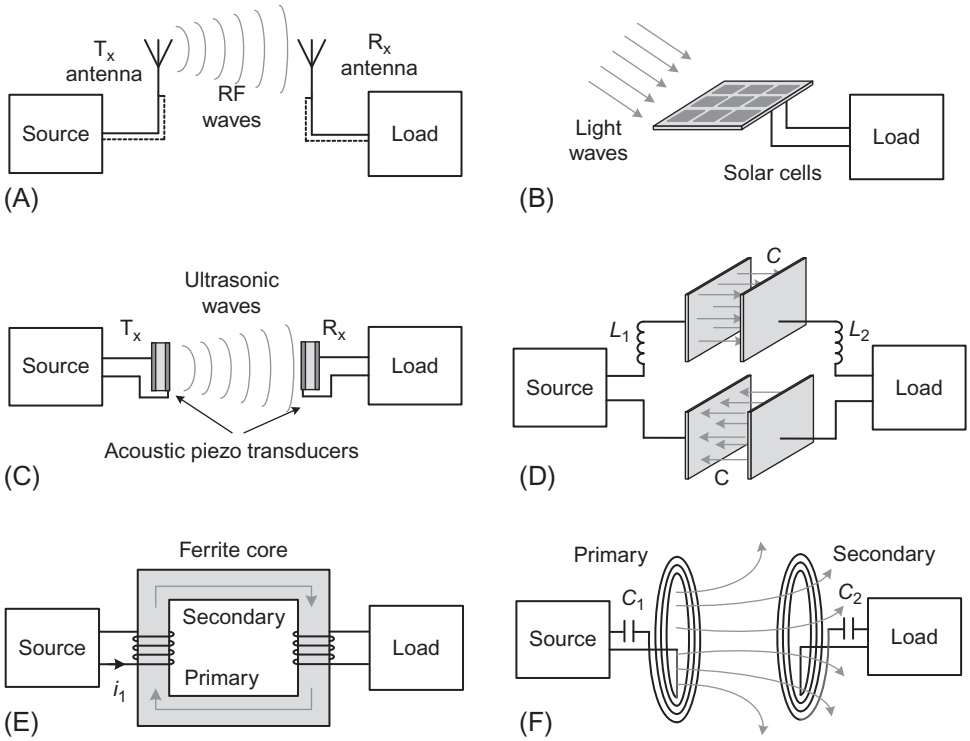


FIG. 22.1 Several methods of wireless power transfer. (A) WPT in radio-frequency waves, (B) solar radiation in optical WPT, (C) WPT using ultrasonic waves, (D) capacitive power transfer, (E) tightly coupled inductive power transfer, and (F) loosely coupled resonant inductive power transfer.

absence of conductive materials), etc. Although the optical links have been mostly used for data transmission, higher power in the form of solar and laser can also be transmitted [3]. One application is laser power transfer through optical fiber that has the advantage of electric isolation between the source and receiver.

Ultrasound. Ultrasonic waves propagate in a physical medium such as air, water, metal pipe, human tissue, etc., by exchanging in between kinetic and potential energies inside the medium (Fig. 22.1C). The ultrasound frequency is above the hearing limit of humans, about 20 kHz, and goes up to several megahertz. The ultrasound power delivery has been mostly applied in low power data transmission, nondestructive testing, remote sensing, and navigation systems [4]; however, higher power transfer for biomedical implants and consumer electronics has gained notable attention recently [5]. The ultrasound wave can be converted to electricity and vice versa, using piezoelectric crystal [6]. One of the advantages of ultrasound power delivery is the ability to travel long distances (depending on the attenuation in the link medium) and through the nontraditional curved power paths. In addition, the low propagation speed of ultrasound wave leads to a more achievable design of directional transceivers compared with RF waves.

Capacitive power transfer. Capacitive power transfer (CPT) uses time-varying electric field between capacitor electrodes to transfer power wirelessly (Fig. 22.1D). The coupling capacitance and the transferred power are limited to the available area and the minimum distance between the electrodes. The CPT has mostly been applied to low power and data transmission systems such as in biomedical implants, bioinstruments, integrated circuits, and the isolated power supply due to galvanic isolation of the source and receiver. The CPT can be implemented in different circuit topologies such as resonance to achieve higher power transfer with increased efficiency [7].

Inductive power transfer. Inductive power transfer (IPT) uses time-varying magnetic field between mutually coupled coils to transfer power wirelessly. As the amount of transferred power depends on the mutual coupling between the coils, IPT systems are divided into two categories, namely loosely and tightly coupled systems. In the tightly coupled systems, the coupling factor (coupling coefficient) is close to unity; therefore, the transferred power efficiency is quite high. A well-known application for tightly coupled systems is a power transformer (Fig. 22.1E). In loosely or weakly coupled systems, the coupling factor is quite low; depending on the application, it can range between 0.01 and 0.5. The main reasons for the low coupling coefficient are the large distance between the coupled coils compared with the coil sizes and/or the absence of high permeable magnetic path connecting them. The low coupling coefficient reduces the power transfer efficiency; therefore, the receiving coil needs to be resonated to increase the efficiency. This chapter is mainly focused on loosely coupled inductive WPT systems (Fig. 22.1F).

22.3 Inductive WPT System Applications

Inductive WPT systems are increasingly getting popular in applications where (a) the flexibility of relative movement between source and load is an advantage, (b) there is limited space for energy storage elements in the load, (c) there is limited access to the load side, and (d) cordless connection improves safety. Some applications that use inductive WPT include the following:

Consumer electronics. As the power density and usage of consumer electronic devices such as notebook, smartphone, and wearables keep increasing, the wireless power connection to the device is a significant advantage. The WPT in consumer electronics is a fast pace industry, and with several standards already in place, the time from product development to the market is short compared with health care and automotive sectors.

Health care. As medical therapies are getting more dependent on implantable electronics, WPT becomes a promising technology in health-care devices [8]. One such application is ventricular assist device (VAD) that circulates the blood inside the body as a pump. The use of inductive WPT eliminates the wire connection between the power source (outside the body) and the VAD (inside the body) [9], which is beneficial to the patient in many aspects.

Another benefit of WPT in electronic implants is the possible reduction or elimination of energy storage element in the implant. This leads to smaller size and lighter weight electronics that brings comfort to the patient. It also reduces the costs and risks associated with the replacement of the energy storage device inside the body. One such application is in retinal implants with the WPT device powering a chip implanted in the eye that (partially) restores vision to the patients with specific retinal diseases.

Electric vehicles. Wireless inductive charging for electric vehicles (EVs) is a step forward toward the mainstream adaptation of EVs as the main transportation systems. The EVs can get the wireless power while in motion (dynamic charging) [10] or in parked position (stationary charging). The dynamic charging can be applied by implementing numerous transmitter coils along the driving path, all connected to each other in parallel and fed by a single source [11]. This is currently most applicable for EVs with predetermined driving path such as electric busses. In the stationary charging, the EV gets the wireless power by having the receiver and transmitter coils aligned and stationary. Since a slight misalignment of the coils would drop the efficiency, specific coil arrangements or multiple coils can be used to make the WPT more tolerant to misalignment [12].

22.4 Resonant Inductive WPT System Design

22.4.1 System Components

Fig. 22.2 shows an inductive WPT system block diagram. The power source feeding the WPT system typically consists of AC-DC-AC (rectification-inversion) stages. The transmitter coil can be compensated to increase the overall system efficiency and reduce the volt-ampere rating of power source. However, this compensation (assuming loss-less) does not affect the magnetic link efficiency, η_{link}, defined from power source output up to the receiver rectification.

The power is transmitted from the source coil (transmitter) to the load coil (receiver) using Faraday's law of induction. Having the two mutually coupled coils, the higher the coupling coefficient between them, the higher the power transfer efficiency. The transmitter and receiver coils can be made up of various components. Magnetic core can be used to shape the flux path, increase the inductance, and enhance the coupling. Metallic shields can be used to reduce the high frequency magnetic fields around the system and reduce the electromagnetic interference (EMI). However, there will be eddy current losses inside the coil conductor and the metallic shield in addition to the magnetic core losses, which bring up the significance of efficient coil design in WPT systems. The high quality factor and highly coupled coils will be discussed in more details later in the chapter.

The wireless power is delivered to the load through the receiver coil, reactive compensation, and electronic rectification for DC loads. The link efficiency depends on the receiver coil compensation and the value of load resistance. The

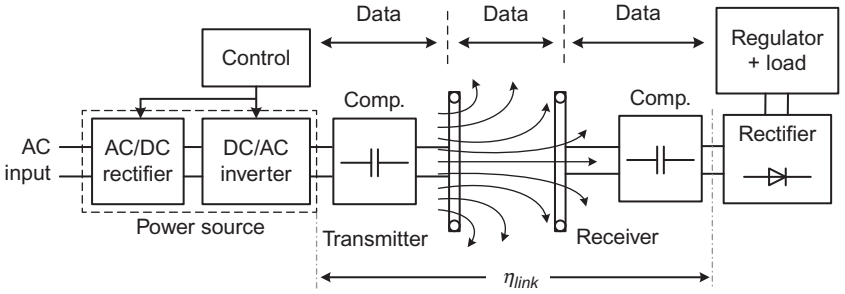


FIG. 22.2 Block diagram of a two-coil inductive WPT system.

feedback control electronic sensors are used in order to operate the WPT system reliably and efficiently.

22.4.2 Operating Field Region

The electromagnetic power transfer is based on Maxwell's equations. For a coil used in WPT system, the governing Maxwell's equations would have exact or simplified formats depending on the coil material, operating frequency, and the power transfer distance, leading the system to operate in one of the three near, Fresnel, or far-field regions [1] (Fig. 22.3). In the near-field region, the reactive energy storage is dominant, and there is negligible radiative power transfer. The transition from near-field in to far-field is through the Fresnel region where the reactive energy storage is still dominant but the coil has radiation patterns. At distances far from the coil, the system operation is in the far-field region where the coil has radiation patterns and the power is transmitted through radiation resistance, for example, RF WPT. In the far-field region, the coil electromagnetic fields are based on the exact set of Maxwell's equations.

For coils (antennas) much smaller than the electromagnetic wavelength λ, the transition happens from the near-field in to far-field, and the Frensel region may not exist. This boundary is typically defined at the distance $\lambda/2\pi$ from the coil. In the inductive WPT systems focused in this chapter, the frequency and the distance between the transmitter and receiver coils are small enough (up to several megahertz in frequency and from several millimeters to few meters in distance) for the system to remain in the near-field region.

22.4.3 Efficiency Equations

There are different methods for the analysis of inductive WPT systems depending on the complexity of the system and accuracy of the analysis. The most accurate method is mesh theory that uses the resistance, inductance, and capacitance matrices to solve for the voltage and current in the system: $\left(R + j\omega L + {}^{1}/_{j\omega C}\right) I = V$. This method is beneficial for systems with multiple coils (including transmitter, receiver, or repeaters), as the inductance matrix contains the self and mutual inductances for all the coils. The mutual capacitance (capacitive coupling) between the coils is neglected in inductive WPT systems, and the capacitance matrix is a diagonal matrix with compensating capacitors as the diagonal elements of that matrix.

The other method is based on the impedance reflection and is useful for simple WPT systems such as a two-coil system (can be modified to single transmitter/receiver system with repeaters/resonators in between). The advantage of this method is the ability to derive closed-form formulas for different variables such as voltage gain, input/output impedances, and link/system efficiencies. The focus of this section is on a typical two-coil inductive WPT system. Fig. 22.4 shows the equivalent circuit of the two-coil WPT system. The power dissipations inside the remote electronics, rectifier, regulator, and the load are included in the equivalent AC load R_L.

In the WPT system, the amount of impedance seen by the power source inverter is a key parameter that directly contributes to the inverter, link, and system efficiencies, along with voltage gain and maximum wireless power transfer. In order to find this impedance, all the impedances in the secondary side need to be reflected to the primary side. In a two mutually coupled coils with mutual inductance of M, the reflected impedance to the primary side is ${}^{(\omega M)^2}/_{Z_2}$ in which Z_2 is the total impedance in the secondary coil, $Z_2 = R_2 + R_L + Z_{L_2} + Z_{C_2}$. When the secondary side is resonant at $\omega = \omega_0$ (Z_2 is real), the reflective impedance to the primary side is pure resistive and is defined by

$$R_{ref1,2} = k^2 R_1 Q_1 \frac{Q_2 Q_L}{Q_2 + Q_L} \tag{22.1}$$

In the Eq. (22.1), k is the coupling coefficient between the primary and secondary coils, and R_1 and Q_1 are the primary coil resistance and quality factor, respectively. And Q_L is the secondary coil load quality factor that is defined by

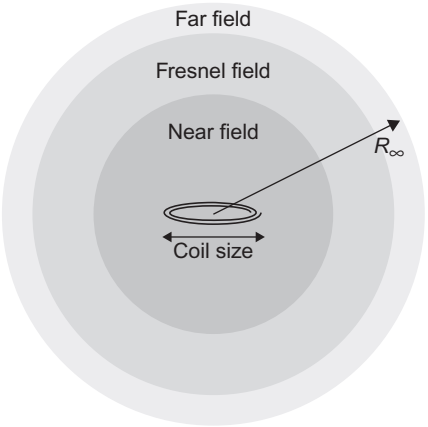


FIG. 22.3 The classification of electromagnetic field regions, inductive WPT systems are in the near-field region.

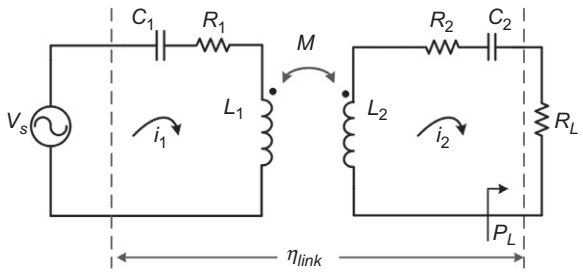


FIG. 22.4 A two-coil inductive WPT system equivalent circuit.

$Q_L = {}^{\omega_0 L_2}/_{R_L}$. Using the reflected impedance approach, the link efficiency is then defined by

$$\eta_{link} = \frac{R_{ref1,2}}{R_1 + R_{ref1,2}} \times \frac{R_L}{R_2 + R_L} \tag{22.2}$$

Eq. (22.2) is valid for both resonant and nonresonant secondary coils. In order to increase the link efficiency, the transmitter side efficiency that is the first term in Eq. (22.2) needs to be maximized by increasing the reflected resistance. As the reflected resistance is limited by the low coupling factor in weakly coupled inductive systems, resonating the secondary tank helps increasing the reflected resistance. This is the main reason to resonate the secondary side to increase the link efficiency.

There are three common optimization objectives for inductive WPT system design [13]. First, increasing the link efficiency that is the objective used in this chapter. Second, desensitizing the link gain versus coupling factor k variations. For example, in a bell-shaped link gain versus k, the maximum gain that corresponds to $k_{critical}$ has the least sensitivity to k variations. The disadvantage of this method is that the theoretical limit for the link efficiency is reduced. Third, stagger tuning that is the combination of the first two objectives to have higher limits for link efficiency while the link gain is not very sensitive to coupling factor changes.

The two-coil inductive WPT system, in its basic configuration, can have six different compensation topologies depending on the type of resonance in the primary and secondary coils (Fig. 22.5). The secondary coil is assumed to be resonated at $\omega = \omega_0$ in series or parallel. The series-resonant secondary has current output type and is suitable for small values of R_L. The parallel-resonant secondary, in the other hand, has voltage output type and is suitable for large loads. The advantage of parallel-resonant secondary is that the coil parasitic capacitance can be included in the compensating capacitor in parallel. The disadvantage of parallel resonance is that resonant frequency depends on the value of R_L.

The primary coil can be resonated (series or parallel) or nonresonated as it does not affect the link efficiency η_{link}. The series-resonant primary requires high-current and low-voltage output from the switched-mode power supply FETs, while the parallel resonant requires high-voltage and low-current output. High values of current increase the FET driver losses, and high voltages increase the FET capacitive losses. A combination of series- and parallel-resonant primary coil can be implemented to operate the system at high efficiencies[13]. Fig. 22.5 shows the different primary and secondary compensation topologies. In all these topologies, the system operating frequency is at $f = f_0$. The power supply output may not be pure sinusoidal; however, the power is transferred to the secondary only at fundamental frequency f_0. The other harmonics do not contribute to power transfer, but they increase the losses in the primary side.

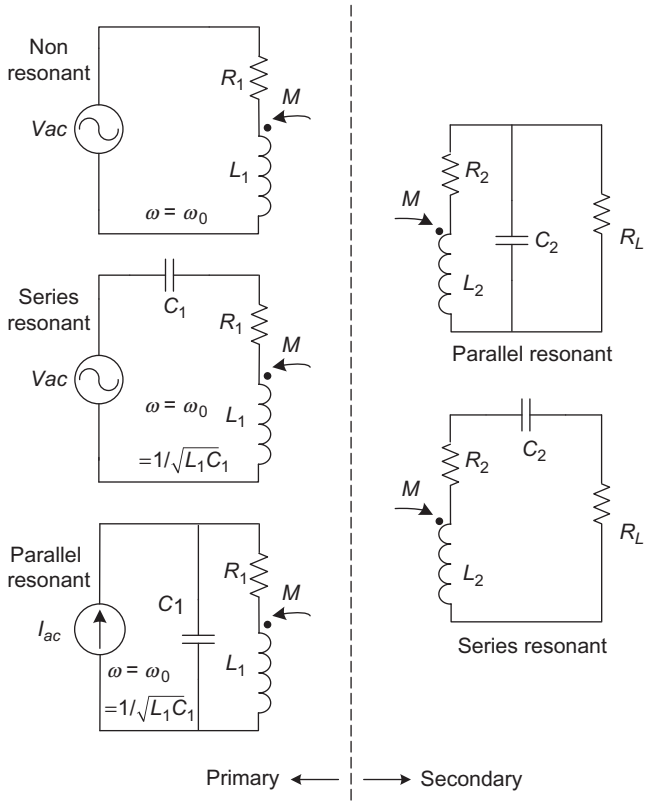


FIG. 22.5 Six different compensation topologies for primary and secondary sides of inductive WPT system.

Table 22.1 shows a summary of the key system parameters for a two-coil WPT system including the resonance frequency, reflected impedance to the primary side, load quality and dissipation factors, and link efficiency. Not to mention that the above-mentioned parameters do not depend on the primary coil compensation topology. In addition, the maximum link efficiency has the same equation for both the series- and parallel-resonant secondary coil.

It is observed from the Table 22.1 that the link efficiency η_{link} is a function of load factor α and $k^2Q_1Q_2$; and, $\eta_{link-max}$ is only a function of $k^2Q_1Q_2$. Fig. 22.6 shows the link efficiency of a two-coil inductive WPT system with a resonant (series or parallel) secondary side. For a fixed $k^2Q_1Q_2$, there is a load factor α that maximizes the link efficiency. The maximum link efficiency increases by increasing $k^2Q_1Q_2$, meaning that in inductive WPT systems, increasing not only the coupling factor but also the coil quality factors boost the efficiency.

In inductive WPT systems, the coupling factor is typically small, that is, in the range of 0.01–0.5. The low coupling factor leads to small values of impedance being reflected to the primary side. This brings the power supply close to unloaded operation mode at which its dissipation dominates the total power dissipated in the primary coil and transferred to the secondary side. Therefore, in loosely coupled systems, it is essential to optimize for the whole system efficiency by including the

TABLE 22.1 Inductive WPT system parameters for series- and parallel-resonant secondary

Secondary compensation	Series resonant	Parallel resonant
Resonance frequency	$\omega_0 = \frac{1}{\sqrt{L_2 C_2}}$	$\omega_0 = \sqrt{\frac{1}{L_2 C_2} - \frac{1}{R_L^2 C_2^2}}$
Load quality (Q)/dissipation (D) factors	$Q_L = \frac{\omega_0 L_2}{R_L} = \frac{1}{\omega_0 C_2 R_L}$	$D_L = \omega_0 R_L C_2$
Reflected resistance to primary	$R_{ref} = k^2 R_1 Q_1 \frac{Q_2 Q_L}{Q_2 + Q_L}$	$R_{ref} = k^2 R_1 Q_1 \frac{Q_2 D_L}{Q_2 + D_L}$
Reflected reactance to primary	$X_{ref} = 0$	$X_{ref} = 0$
Load factor	$\alpha = \frac{Q_L}{Q_2}$	$\alpha = \frac{D_L}{Q_2}$
Link efficiency	$\eta_{link} = \frac{k^2 Q_1 Q_2}{\left(1 + k^2 Q_1 Q_2 \frac{\alpha}{\alpha+1}\right)} \frac{\alpha}{(\alpha+1)^2}$	$\eta_{link} = \frac{k^2 Q_1 Q_2}{\left(1 + k^2 Q_1 Q_2 \frac{\alpha}{\alpha+1}\right)} \frac{\alpha}{(\alpha+1)^2}$
Maximum link efficiency	$\eta_{link-max} = \frac{k^2 Q_1 Q_2}{\left(1 + \sqrt{1 + k^2 Q_1 Q_2}\right)^2}$	$\eta_{link-max} = \frac{k^2 Q_1 Q_2}{\left(1 + \sqrt{1 + k^2 Q_1 Q_2}\right)^2}$

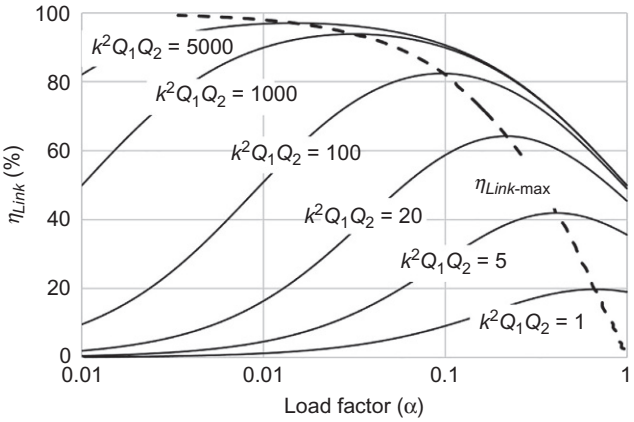


FIG. 22.6 The link efficiency of a two-coil WPT system versus load factor α and $k^2Q_1Q_2$.

power supply, magnetic link, and also secondary side remote electronics.

22.5 WPT Systems With Multiple Coils

In WPT systems, there can be multiple coils in the transmitter, receiver, or in between them that help extend the use of WPT to practical applications. Here, the most common types of multiple-coil inductive WPT systems are reviewed, discussing their applications, (dis)advantages, and challenges.

22.5.1 Single Transmitter and Receiver With Multiple Coils in Between

The single transmitter and receiver WPT structure can include one, two, or more repeaters (resonators) in between. There are different applications that implement such structures. One application is to transmit power to large distances using repeaters along the path or even transmit power along a curved path. The other application is to have the repeater tightly coupled to either the transmitter or the receiver [14] (three-coil WPT, Fig. 22.7A), similarly, two repeaters in a four-coil WPT [15] (Fig. 22.7B). There are two main reasons for such configurations: (a) to have more degrees of freedom to maximize the efficiency and desensitize the link gain versus coupling factor without scarifying one objective for the other as was discussed earlier in the chapter and (b) to have the highly coupled transmitter-repeater or repeater-receiver coils act as practical and efficient impedance matching elements in both the source and load sides.

22.5.2 Multiple Transmitters and Single Receiver

The applications that implement multiple transmitter coils and a single receiver are mainly classified into two areas, one is dynamic WPT and the other is misalignment tolerant systems. The dynamic WPT systems transfer the power wirelessly while the receiver is in motion. A known example is EV dynamic charging in which multiple transmitter coils are placed along

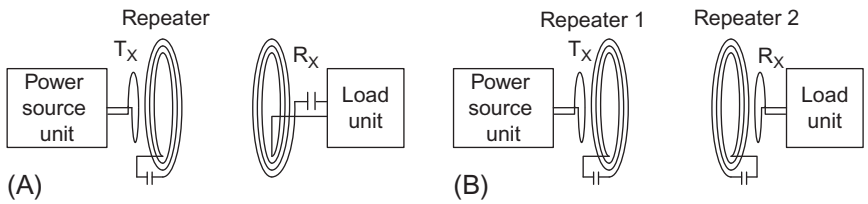


FIG. 22.7 Three-coil and four-coil WPT structures. (A) Three-coil WPT and (B) four-coil WPT.

the driving path and the receiver coil is placed in the moving vehicle. The challenge of such systems is to efficiently power the transmitter coils. A simple method is to have a power supply for each transmitter, and the power is transferred to the receiver by sensing it when it is aligned to it. The drawback of this method is the use of numerous power supplies. The other method is to have a long transmitter pad along the vehicle driving path. The disadvantage of this method is that only a portion of the coil transmits power while all of it is dissipating power. A way to solve these problems is to have multiple transmitters coils connected in parallel to one power supply. The current flows in a coil that is aligned with the receiver coil using reflected impedance while there is no current flowing in the other transmitter coils [11] (Fig. 22.8).

The other application with multiple transmitter coils is to have a misalignment tolerant system. As the coupling (and so the efficiency) of a two mutually coupled coils drops sharply by a slight misalignment between them, implementing multiple transmitter coils can increase this tolerance [12]. Multiple transmitter coils can also be used to provide a uniform magnetic field across a surface area giving the receiver the freedom of movement over that area [16].

22.5.3 Single Transmitter and Multiple Receivers

In some WPT applications, multiple receivers need to get the power simultaneously from a single transmitter pad (Fig. 22.9). The amount of power transferred to each receiver is linearly related to the resistance it reflects to the transmitter. In such systems, the first challenge is that the change of power transfer to one receiver could affect the amount of power transfer to other receivers. To avoid this, constant-current-flow topologies such as LCL in the transmitter coil are required.

With the transmitter coil having a constant current, power sharing to the receivers can be implemented using dynamic (active) tuning in each receiver side. The dynamic tuning can be implemented using L-C network [17], standard boost [18], or tristate boost [19]. In the L-C network method, a discrete matrix of L and C components is actively switched to control the reflected impedance to the transmitter side. The standard boost method controls the active power transfer to the receiver by changing the reflected resistance to the transmitter coil. Similarly, the tristate boost controls the active power flow, but also, the reactive power flow to the receiver can be controlled in case of detuning. The tristate boost has an extra degree of freedom compared with standard boost by shorting the inductive energy in boost (freewheeling).

One of the challenges in multiple-receiver WPT systems is the magnetic cross coupling between the receivers when they are in close proximity to each other (Fig. 22.9). The cross coupling would change the expected power transfer to the receivers and impose system performance issues. One method to reduce the cross coupling is to use multiresonant WPT system in which each receiver is resonant at one of the transmitter carrier frequencies [20].

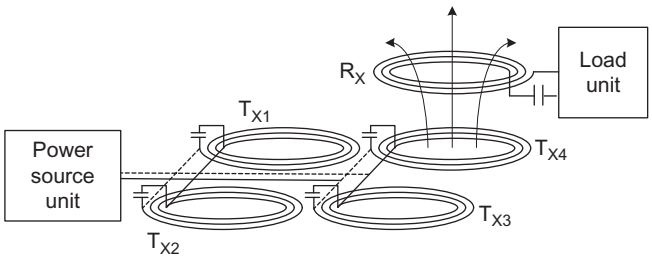


FIG. 22.8 A dynamic WPT structure with parallel-connected transmitter coils.

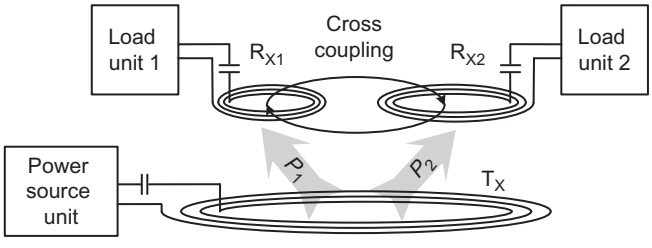


FIG. 22.9 Single transmitter coil WPT with multiple receivers.

22.6 A Glance Into WPT Power Source Converter

In weakly coupled inductive powering applications, the design of transmitter coil power converter is directly linked to magnetic link design and therefore needs to be part of the whole WPT system optimization. The main reason is due to the weak coupling, as the amount of reflected resistance to the transmitter coil is quite small, the converter operates close to freewheeling. And large amount of current is needed to flow in the coil to generate the required magnetic field and power.

The choice of transmitter coil power converter depends on the WPT application, power level, and operating frequency. For example, in EVs, the amount of power required to wirelessly charge the battery can range from 3.3 kW up to several tens of kilowatts, with frequency ranges from 20 kHz up to few hundreds of kilohertz. For such power and frequency levels, highly efficient AC-AC power converters such as full-bridge AC-DC rectifier and DC-AC inverter can be used to drive the transmitter coil. These power converters have been well stablished in the past few decades in terms of efficiency, reliability, and cost.

An important benefit of inductive WPT is in applications with small size and medium to high power requirements. As the magnetic link size reduces, the reflected resistance to the transmitter coil gets reduced as well. To compensate for this reduction, the operating frequency needs to increase to keep

the power level up. For example, in electronic devices such as phones, wearables, and laptops, the power rating can range from 1 W up to about few hundred watts. For inductive WPT in the megahertz frequency region, the operating frequency is typically bound to industrial, scientific, and medical (ISM) band of 6.78, 13.56 MHz, and so on. The power converter design in the megahertz region is critical as the dynamic losses increase in the FETs. There are several typically used DC-AC power inverters in the megahertz frequency range such as classes A, B, AB, C, D (ZCS and ZVS), and E. In this section, the focus is on switched-mode class-D and class-E power inverters as they deliver highest efficiencies of all the classes [21,22].

22.6.1 Class-D Inverter

Class-D inverter has a voltage output characteristic that is good to feed series-resonant transmitter coil. The resonance is not a critical requirement for class-D inverter although it increases the current for a fixed voltage. And the inverter can power resistive, inductive, and capacitive loads [23]. Fig. 22.10 shows the schematic of the class-D inverter with ideal waveforms. At resonance, the impedance seen by the inverter is the transmitter coil resistance R_1, in addition to the reflected resistance from the receiver side R_{ref}. In weakly coupled WPT systems, the R_{ref} is very small and can bring the inverter to the freewheeling operation. At this condition, the static conduction losses in the FETs dominate both the power dissipated in the transmitter and transferred to the receiver ($R_{on} > R_1 + R_{ref}$).

The class-D output voltage is square wave and fixed, independent of the load or coupling variations. Only the fundamental harmonic of current (at receiver coil resonance ω_0) contributes to the wireless power transfer, and the other harmonics (although small as are blocked by the resonance) cause dissipation in the transmitter coil. For moderately large transmitter coil loaded quality factor ($Q_{1L} = \dfrac{\omega_0 L_1}{R_1 + R_{ref}} > 20$), the coil current would be close to sinusoidal, operating at its series resonance frequency that is also ω_0.

One of the challenges of class-D inverter in the megahertz frequency range is the switch output capacitive losses during S_2 turn-on. A solution is to have the inverter output current lag the output voltage so it can self-commute to zero value during S_2 turn-on (ZVS). To do so, one method is to have the impedance seen by the inverter to be slightly inductive by operating above the transmitter coil resonance frequency ($\omega L_1 - \dfrac{1}{\omega C_1} = \omega L_{eff} > 0$) (Fig. 22.11). Note that the receiver coil is resonant at the operating frequency. Another way to provide lagging output current while not shifting the frequency from the transmitter coil resonance frequency is to add an inductive element L_{sh} in parallel to the inverter output [24] (Fig. 22.12). The L_{sh} provides the negative current required for the V_{sw} to self-commute to zero during S_2 turn-on (ZVS).

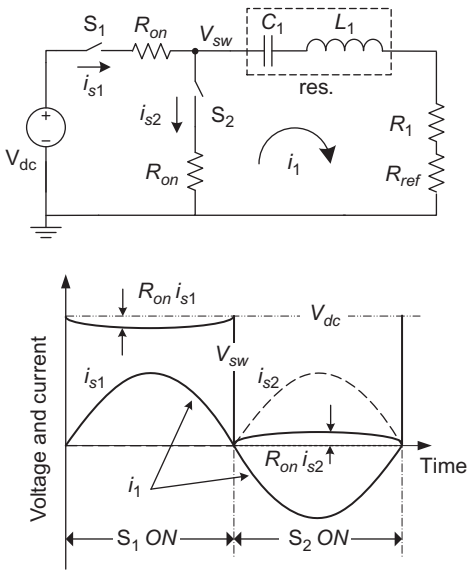


FIG. 22.10 Class-D inverter with ideal waveforms.

22.6.2 Class-E Inverter

The series-resonant transmitter coil (as for class-D) requires high amount of current that increases FET gate driver losses. The parallel-resonant coil, in the other hand, reduces the current rating of the switches by circulating it through the resonant tank. However, it produces high voltages across the switches that increase the FET output capacitive losses. A combination of series- and parallel-resonant transmitter coil would take advantage of low voltage rating of series-resonant and low current rating of parallel-resonant coil. Class-E

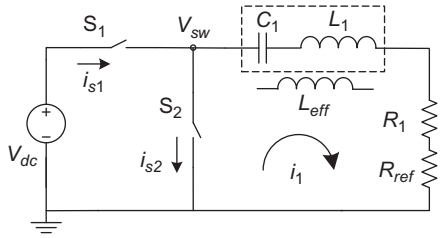


FIG. 22.11 Class-D ZVS operating above the primary coil resonance frequency.

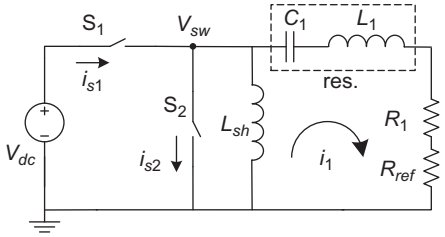


FIG. 22.12 Class-D ZVS with additional inductor in parallel to the switch output.

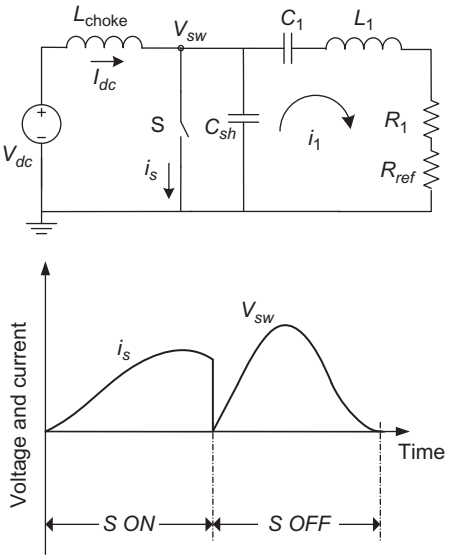


FIG. 22.13 Class-E inverter with ideal waveforms.

inverter satisfies these conditions with doubled-tuned output circuit [25]. Fig. 22.13 shows the class-E inverter with ideal waveforms. The inverter operates between the transmitter series resonance frequency and the one of transmitter in parallel with the C_{sh}.

An advantage of class-E compared with class-D with ZVS is that the output voltage slope approaches zero during the S turn-on and makes class-E generally more efficient than class-D. For the switch voltage and its slope to be zero at switch turn-on, it is a function of L_{choke}, C_{sh}, $R_1 + R_{ref}$, and the oscillations in the C_{sh}-C_1-L_1 tank during switch turn-off. This makes the class-E inverter more complicated to design and prone to nonoptimum operation when coupling factor and load vary, which are common characteristics of WPT systems [22].

22.7 Efficient Magnetic Link Design

Earlier in the chapter, it was shown that the maximum link efficiency $\eta_{link-max}$ is a function of $k^2Q_1Q_2$ in which k is the coupling factor between the transmitter and receiver coils with quality factors of Q_1 and Q_2, respectively. To enhance the link efficiency, not only the coupling factor needs to increase, but also the coil quality factors should improve. This section's focus would be on the methods to increase the coupling and quality factors.

22.7.1 Effect of Link Dimension

The magnetic design of inductive WPT system includes the design of link dimensions, coil shape, placement, and the type of material and conductor used in them. The coupling factor between the transmitter and receiver coils, with

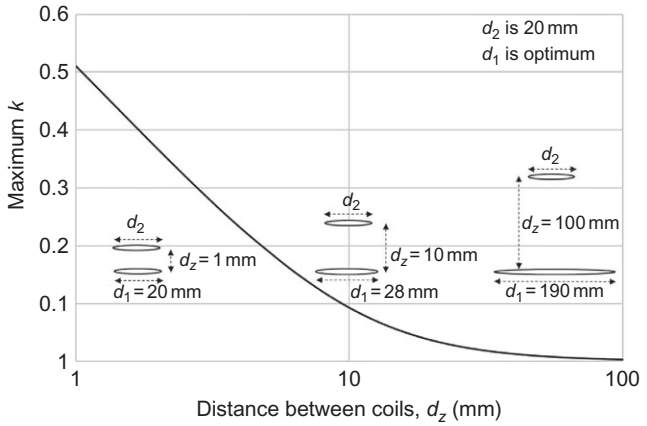


FIG. 22.14 The maximum coupling factor k_{max} versus coil relative sizes and distance.

self-inductances of L_1 and L_2, is $\frac{M}{\sqrt{L_1L_2}}$ in which M is the mutual inductance between the two coils. In simple approximation for concentric-turn coils, the coupling factor is related to the ratio of the two-coil surface areas and inversely to the distance between them. The closer the transmitter and receiver coils to each other, the larger the coupling between them. And for coils that are very close to each other, the maximum coupling happens with coils having the same sizes. As the distance between the coils increases, there is an optimum ratio between the coil surface areas that leads to maximum coupling factor. Fig. 22.14 shows an example of the effects of distance between coils and their relative sizes on the link maximum coupling factor.

22.7.2 Effect of Coil Shape and Alignment

Circular coil is the most common form for the WPT resonator due to its symmetry, simplified analysis, and ease of fabrication. Other common coil forms include square and rectangular types.

Another important criterion that affects the coil shape is the misalignment between the transmitter and receiver coils. Misalignment tolerant inductive WPT systems are designed such that a specified misalignment between the coils does not drop the efficiency and power transfer significantly [12]. Such systems provide spatial freedom of movement to the receiver coil that is beneficial for most WPT applications. For example, Fig. 22.15A shows the coupling factor k changes versus misalignment between the transmitter and receiver coils for two transmitter sizes. The more misalignment tolerant system has a larger transmitter coil to allow for small movements in the receiver coil while having minimal changes in k. Fig. 22.15B shows that for a fixed misalignment distance, the coupling factor drop is lower for large transmitter coil compared with the small coil. Another method to improve the misalignment tolerance is to have multiple transmitter coils [26]. There are other factors, beside the misalignment tolerance,

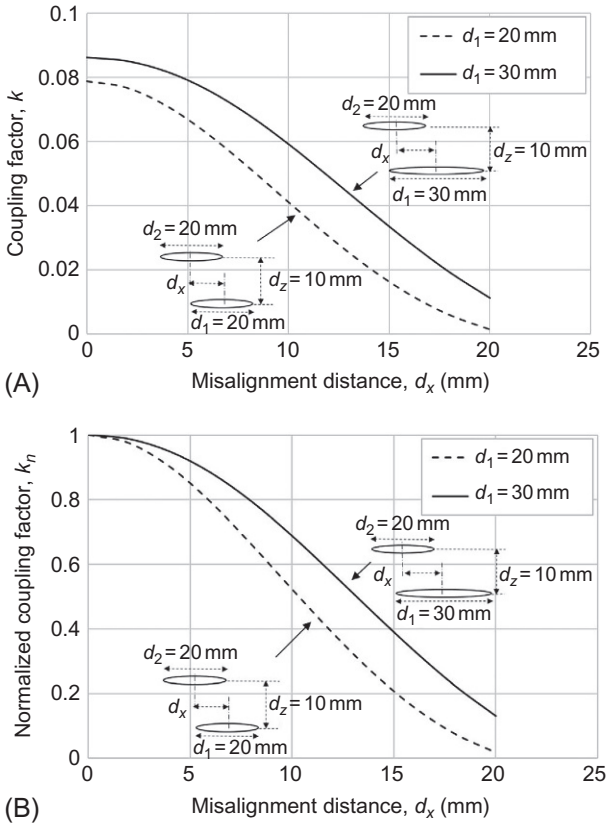


FIG. 22.15 "Normalized" coupling factor k drop versus misalignment between transmitter and receiver coils. (A) Coupling factor k versus misalignment distance d_x. (B) Normalized coupling factor k_n versus d_x.

that affect the size and shape of coil, such as self-inductance and geometric constraints. The receiver side coil has typically more geometric constraints—for example, in a biomedical implant inside the body—and the WPT design process starts with the receiver coil followed by the transmitter.

22.7.3 Effect of Ferrite Core

Another way to increase the coupling factor is to use soft magnetic materials such as ferrite cores. The magnetic flux lines follow the path of minimum reluctance; therefore, the high permeable ferrite core can be used to shape the field and increase the coupling. As the ferrite cores are placed on one side of the transmitter/receiver coils to enhance the coupling, they also shield the magnetic field from being exposed to the surrounding objects. This helps the inductive WPT system satisfy the health and safety requirements associated with high magnetic field strengths. In some applications, adding a metal plate to the coil helps shielding the high frequency magnetic fields from penetrating into nearby objects and reducing the EMI disturbance (Fig. 22.16).

A ferrite material with high saturation flux density, low AC power loss, and high bulk resistivity and permeability is beneficial in WPT systems. The most common types of ferrites used

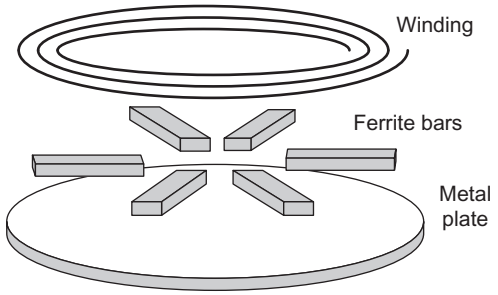


FIG. 22.16 An example structure of inductive WPT coil including winding, ferrite, and metal plate.

in inductive WPT systems are MnZn and NiZn ferrites. The MnZn ferrite has high permeability and high saturation flux density, while the NiZn ferrite has lower permeability and high bulk resistivity. The high-permeability ferrite increases the magnetic energy storage per geometric constraints, such as coil self-inductance. A ferrite with high bulk resistivity reduces the high-frequency-induced eddy and displacement currents.

A ferrite core increases not only the coupling factor and inductance but also the power dissipation. For sinusoidal excitation, the core loss is a function of frequency and magnetic flux density in the core. Its effects on the coil are well described by the coil quality factor Q. Increasing the coil inductance and resistance is somehow compensated in the quality factor that directly influences the link efficiency. However, other system requirements such as high inductance, magnetic field shielding, and high coupling factor are achieved by using ferrite cores in the transmitter and receiver coils.

22.7.4 Effect of Coil Winding

Reducing the coil winding AC resistance is an important step in magnetic link design as it increases the coil quality factor and link efficiency. Depending on the operating frequency, the winding conductor can be solid, foil, tubular, or litz. Solid round conductor is the most basic type of conductor, and its properties (such as resistance and inductance) have been well studied and determined. Solid wire is a building block of many types of wires such litz, and understanding its behavior is a critical step in the winding design. The AC power loss inside a current-carrying conductor is due to the high frequency eddy currents induced in it by the time-varying (1) internal magnetic field (skin effect) and (2) external magnetic field (proximity effect). The skin and proximity effects are orthogonal in round conductors and can be investigated separately. In the skin effect, the current flows mostly in the skin-depth region of the conductor, leaving the inner part having almost zero current flow (tubular conductor) that increases the AC resistance. One solution is to have multiple insulated concentric tubular conductors with optimum current flow to reduce the AC resistance [27]. With the conductor radius close to skin depth, the current flow is close to uniform. At high frequencies—mostly

above a megahertz—the solid conductor can be superior to other conductor types due to its low AC power loss, low cost, and ease of manufacturing.

A potential type of conductor is foil wire that can be used in inductive WPT systems [28]. Copper foils with thicknesses close to skin depth in the multimegahertz frequency range (Cu skin depth is between 65 and 15 μm in the 1–20 MHz) are commercially available and affordable. In addition, with the state-of-the-art printed wiring (flexible) boards and electroplating methods, efficient inductors can be designed and fabricated. The other advantages of using foil conductor include high-current-carrying capability due to large cross-sectional area and improved thermal performance, and the inductors with low overall thickness can be designed. The foil conductor characteristics such AC resistance and inductance have been extensively studied in the literature for various applications. The most common application is in transformer windings with magnetic core surrounding the conductor [29]. This forces the magnetic field contours to be parallel with the foil and simplifies the determination of foil impedance in to a 1D analysis. In inductive WPT, however, the magnetic core—if present—is located on one side of the coil, and the field contours have 2D pattern requiring numerical methods such as finite element (FE) analysis to determine the inductor impedance.

Another way to reduce the AC resistance of a conductor—with thickness (or radius) much bigger than the skin depth—is to have the current flow uniform across the conductor cross section. To do so, the conductor needs to be divided into multiple insulated skin-depth-sized strands, with each strand seeing the same amount of magnetic flux. This can be done by twisting the strands such that each one of them occupies all the positions across the conductor in a full twist. This structure is litz wire, and its principles can be applied on different types of conductors to reduce the AC resistance [30]. The most common type of litz wire is made of solid round strands. However, same principles can be applied to design other forms of litz wire with rectangular foil strands [31]. Litz wire is a common choice of inductor wire at frequencies up to few megahertz, above which the need for very thin strands (close to skin depth) makes the manufacturing of litz wire expensive.

In the inductors with multiple turns, the power losses are divided into skin and proximity dissipations. The skin effect loss can be reduced by optimum design of a single-turn winding. The proximity effect, in the other hand, depends on the field of nearby turns. The complete structures of coil, including the number of turns, layers, distance between them, and existence of ferrite core, are the design parameters for minimizing proximity effect and AC resistance. For efficient coil design in WPT system, the coil quality factor Q is the main parameter of interest. Therefore, not only the winding AC resistance needs to be reduced, but also the coil inductance would have to increase. As a coil structure with minimum AC resistance does not necessarily have the maximum inductance, the coil quality factor would be the main optimization objective. In a broader link design objective, both the transmitter and receiver need to be considered by maximizing $k^2Q_1Q_2$.

22.8 Summary

This chapter covered different methods of WPT with the main focus on weakly coupled inductive WPT systems. Such systems are increasingly getting popular due to the advantages they bring compared with wired power transfer. Not only inductive WPT systems offer extended freedom of movement for source and load (relatively) such as in EVs, but also they are beneficial in applications where there is limited access to the load such as in biomedical implants. A typical two-coil inductive WPT was analyzed, and the system parameters including the magnetic link efficiency were derived. In order to increase the maximum link efficiency, both the coupling factor and coil quality factors need to increase. The effects of coil size, shape, structure, and placement were discussed to maximize link efficiency. In weakly coupled inductive WPT systems, the impedance reflected to the transmitter coil as seen by the inverter is quite small, and the inverter needs to be designed depending on the magnetic link. For high frequency (megahertz range) inverters, class-D (ZCS and ZVS) and class-E inverters were analyzed, and their (dis) advantages were discussed.

References

[1] C.A. Balanis, Antenna Theory: Analysis and Design, third ed., John Wiley & Sons, Inc., Hoboken, NJ, 2005.
[2] H.P. Kimmich, Bio-telemetry, based on optical transmission, Biotelem Patient Monit. 9 (1982) 129–143.
[3] S. Jarvis, J. Mukherjee, M. Perren, J.S. Sweeney, On the fundamental efficiency limits of photovoltaic converters for optical power transfer applications, in: 39th IEEE Photovoltaic Spec. Conf. (PVSC), 2013, pp. 1031–1035.
[4] T. Tsuji, T. Fujimoto, T. Izuto, T. Togawa, Telemetry of organ temperature with quartz crystal resonator using ultrasonic detection for preoperative patient monitoring, in: Proc. 12th Int. Symp. Biotel, 1993, pp. 378–380.
[5] J. Charthad, M.J. Weber, T.C. Chang, A. Arbabian, A mm-sized implantable medical device (IMD) with ultrasonic power transfer and a hybrid bi-directional data link, IEEE J. Solid State Circuits 50 (2015) 1741–1753.
[6] N.G. Holmer, K. Lindstrom, Highly isolated power supply energized by ultrasound, Med. Biol. Eng. 11 (2) (1973) 233–235.
[7] M.P. Theodoridis, Effective capacitive power transfer, IEEE Trans. Power Electron. 27 (2012) 4906–4913.
[8] A.K. RamRakhyani, G. Lazzi, On the design of efficient multi-coil telemetry system for biomedical implants, IEEE Trans. Biomed. Circuits Syst. 7 (2013) 11–23.
[9] T. Campi, S. Cruciani, F. Palandrani, V.D. Santis, A. Hirata, M. Feliziani, Wireless power transfer charging system for AIMDs and Pacemakers, IEEE Trans. Microw. Theory Tech. 64 (2016) 633–642.

[10] J. Huh, S.W. Lee, W.Y. Lee, G.H. Cho, C.T. Rim, Narrow-width inductive power transfer system for online electrical vehicles, IEEE Trans. Power Electron. 26 (2011) 3666–3679.
[11] K. Lee, Z. Pantic, S.M. Lukic, Reflexive field containment in dynamic inductive power transfer systems, IEEE Trans. Power Electron. 29 (2014) 4592–4602.
[12] M. Budiha, J.T. boys, G.A. Covic, C.Y. Huang, Development of a single-sided flux magnetic coupler for electric vehicle IPT charging systems, IEEE Trans. Industr. Inform. 60 (2013) 318–328.
[13] K.V. Schuylenberg, R. Puers, Inductive Powering, Basic Theory and Application to Biomedical Systems, Springer, Netherlands, 2009.
[14] M. Kiani, U.M. Jow, M. Ghovanloo, Design and optimization of a 3-coil inductive link for efficient wireless power transmission, IEEE Trans. Biomed. Circuits Syst. 5 (2011) 579–591.
[15] A.P. Sample, D.A. Meyer, J.R. Smith, Analysis, experimental results, and range adaptation of magnetically coupled resonators for wireless power transfer, IEEE Trans. Industr. Inform. 58 (2011) 544–554.
[16] W.X. Zhong, X. Liu, S.Y.R. Hui, A novel single-layer winding array and receiver coil structure for contactless battery charging systems with free-positioning and localized charging features, IEEE Trans. Industr. Inform. 58 (2011) 4136–4144.
[17] A.P. Hu, S. Hussmann, Improved power flow control for contactless moving sensor applications, IEEE Power Electron. Lett. 2 (2004) 135–138.
[18] J.T. Boys, G.A. Covic, A.W. Green, Stability and control of inductively coupled power transfer systems, IEE Proc. Electric Power Appl. 147 (2000) 37–43.
[19] Z. Pantic, S.M. Lukic, Framework and topology for active tuning of parallel compensated receivers in power transfer systems, IEEE Trans. Power Electron. 27 (2012) 4503–4513.
[20] Z. Pantic, K. Lee, S.M. Lukic, Receivers for multi-frequency wireless power transfer: deign for minimum interference, IEEE J. Em. Topics Power Elect. 3 (2014) 234–241.
[21] C. Florian, F. Mastri, R.P. Paganelli, D. Masotti, A. Costanzo, Theoretical and numerical design of a wireless power transmission link with GaN-based transmitter and adaptive receiver, IEEE Trans. Microw. Theory Tech. 62 (2014) 931–946.
[22] G.A. Kendir, et al., An optimal design methodology for inductive power link with class-E amplifier, IEEE Trans. Circuits Syst. 52 (2005) 857–866.
[23] M.K. Kazimierczuk, Class-D voltage-switching MOSFET power amplifier, IEE Proc. Electric Power Appl. 138 (1991) 285–296.
[24] M.A. de Rooij, The ZVS voltage-mode class-D amplifier, an eGaN® FET-enabled topology for highly resonant wireless energy transfer, in: IEEE Appl. Pow. Elect. Conf. (APEC), 2015, pp. 1608–1613.
[25] P.R. Troyk, M.A.K. Schwan, Closed-loop class E transcutaneous power and data link for microImplants, IEEE Trans. Biomed. Eng. 39 (1992) 589–599.
[26] S.A. Mirbozorgi, H. Bahrami, M. Sawan, B. Gosselin, A smart multi coil inductively coupled array for wireless power transmission, IEEE Trans. Ind. Electron. 61 (2014) 6061–6070.
[27] M. Etemadrezaei, S.M. Lukic, Multilayer tubular conductor for high Q-factor wireless power transfer system resonators, IEEE Trans. Ind. Appl. 52 (2016) 4170–4178.
[28] C.R. Sullivan, Layered foil as an alternative to Litz wire: multiple methods for equal current sharing among layers, in: Workshop Con. Mod. Power. Elec. (COMPEL), 2014.
[29] P.L. Dowell, Effects of eddy currents in transformer windings, IEEE Proc. 113 (1966) 1387–1394.
[30] M. Etemadrezaei, S.M. Lukic, Coated-strand litz wire for multi-megahertz frequency applications, IEEE Trans. Magn. 52 (2016) 1–11.
[31] S. Wang, M.A. de Rooij, W.G. Odendaal, J.D. van Wyk, D. Boroyevich, Reduction of high-frequency conduction losses using a planar Litz structure, IEEE Trans. Power Electron. 20 (2005) 261–267.

Section IV

Power Generation and Distribution

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23

Energy Sources

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23.1 Introduction

In modern societies, development level and economic well-being of a society are directly measured by energy generation and consumption. Energy plays an important role in the economic health of a country that is reflected by the gross national product (GNP). The per capita GNP of a country is correlated to the per capita energy consumption. There is a steady demand to increase the energy generation capacity all over the world since the global energy consumption is rising. The main reasons are the technological developments, industrial revolution, and increase in population. In a modern and industrialized community, energy is used in every single human activity. Some major examples are the following:

- Household applications such as heating, cooking, lighting, and air conditioning
- Transportation—passenger cars, buses, trains, trucks, and aircrafts
- Manufacturing heat and electricity as well as user end or industrial products
- Irrigation and fertilizing in agricultural organizations

The worldwide energy consumption has been growing steadily and rapidly right after the industrial revolution. Today's global energy consumption has reached more than 500 EJ. This amount of energy is consumed with an hourly rate of 15 TW [1]. Global energy consumption of 1900 was 0.7 TW. The United States consumes the greatest amount of energy per capita worldwide. The amount of energy consumed in the United States was 105 EJ or 29,000 TWh in 2005, with equivalent rate of 3.3 TW [2,3]. If the hourly consumed power is 3.3 TW, 1 year of consumption corresponds to 29,000 TWh, by $3.3\ \text{TW} \times 24\ \text{h} \times 365$ days. Between 1980 and 2004, the worldwide energy consumption annual growth rate was 2%. The total consumption in 2004 is given in Table 23.1 according to the US Energy Information Administration [1]. The estimated 15 TW total global consumption is mainly generated from the fossil fuels such as coal, oil, and gas.

This 15 TW of total consumption is shared among several sectors. Around 37% of the total 15 TW is consumed by industrial sectors such as manufacturing, mining, construction, and agriculture. Twenty percent of the total consumption is by the personal and commercial transportation. Residential consumption such as residential lighting, heating, and household appliances corresponds to 11% of the total. Consequently, commercial lighting, heating, cooling, and water provision and sewing services consume 5% of the total [4]. The other 27% of world's energy is lost in the energy generation and transmission stages. The overall energy consumption percentages by sector are shown in Fig. 23.1.

According to Fig. 23.1, the generation and transmission losses are considerably high. In order to generate 2 TW of electric power, approximately 5 TW of power is required. This is due to the fact that efficiency of a typical power plant is around 38% [5]. Fig. 23.1 also imposes that more than a quarter of the

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TABLE 23.1 Total energy consumption

Source type	Average power (TW)	Energy per year (EJ)
Oil	5.6	180
Coal	3.8	110
Gas	3.5	120
Hydroelectric	0.9	30
Nuclear	0.9	30
Wind, solar, wood, geothermal	0.13	4
Total	**15**	**471**

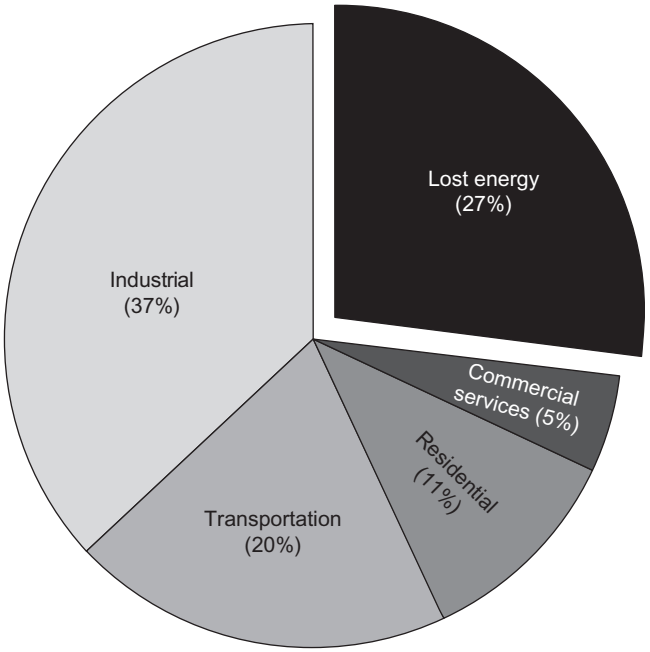


FIG. 23.1 Percentage share of sectors on energy consumption.

produced energy is lost in low efficient conventional energy conversion systems and transmission lines. This issue encourages the increased focus on high efficient renewable energy systems, which may also reduce or eliminate the transmission losses if they are built as distributed energy generation units. In comparison with the efficiency of conventional power plants, new generation of power plants using gas turbines or microturbines may reach a substantially higher efficiency of 55%; however, they still rely on another fossil fuel, which is natural gas [6].

After the invention of steam engines, coal began to be the main source of energy in the eighteenth and nineteenth centuries. Since automobiles were invented and electricity usage became more common, coal left its popularity to the oil during the twentieth century. From 1920 to 1973, oil was the main resource fueling the industry and transportation, and its price steadily dropped during these years. Oil kept its expansiveness until the 1970s. In the oil crises of 1973 and 1979, price per barrel boosted from 5 to $45, and oil was not the best and most common source of energy production anymore [7]. From these dates, coal and nuclear became the sources for electric power generation. In those years, energy conversation and increasing the energy efficiency gained importance. However, the use of fossil fuels has continued over the last 30 years, and their contribution to overall energy production has increased. During the last 3 years, coal has become the fastest growing fossil fuel, since it has large remaining reserves [7]. On the other hand, renewable energy sources have gained interest due to the depletion of fossil fuels, followed by high oil prices, and climate change concerns related to the carbon emissions. Therefore, government support on development, deployment, incentives, and commercialization of renewable energies are ever increasing. For instance, in March 2007, it is agreed by the European Union members that at least 20% of their nations' energy should be produced from renewable sources by 2020. This is also a part of environmental concerns such as global warming [8] and building a sustainable energy economy by reducing the nations' dependence on imported fossil fuels. However, although there is a large availability of renewable sources, their contribution to globally consumed energy is relatively poor.

In developed countries such as Germany and Japan, the national gross product is 6 kW per person and 11.4 kW per person in the United States. Bangladesh has a low consumption with 0.2 kW per person, while it is around 0.7 kW per person for a developing country such as India. Twenty-five percent of the overall world's energy is consumed by the United States, while its share of global energy generation is 22% [4]. Energy consumption in the United States is shared by four broad sectors according to the US Department of Energy. Similar to the world's energy consumption, the largest user is the industrial sector, currently consuming 33% of the total energy. Next largest amount of energy is consumed for transportation followed by residential and commercial users. Energy consumption shares of the United States for four major energy consumption sectors (industrial, transportation, residential, and commercial) are demonstrated in Table 23.2 [4,9,10].

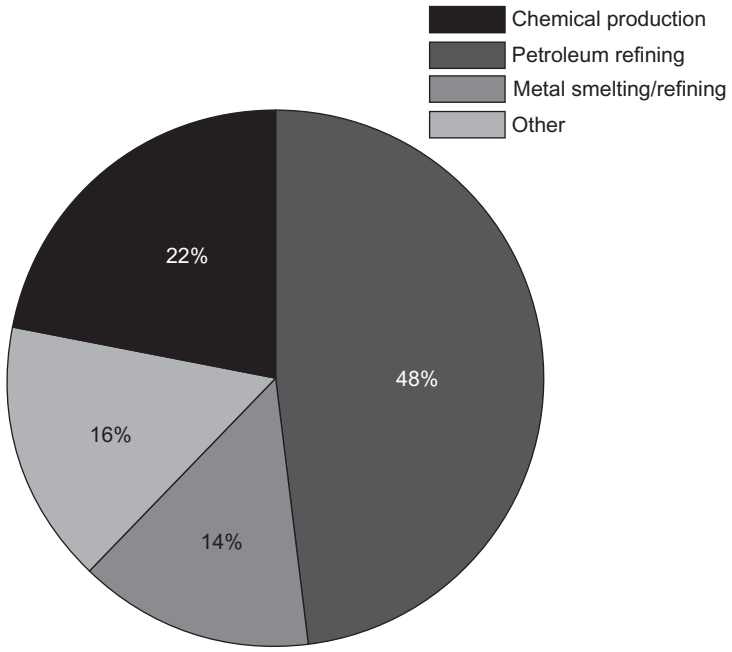
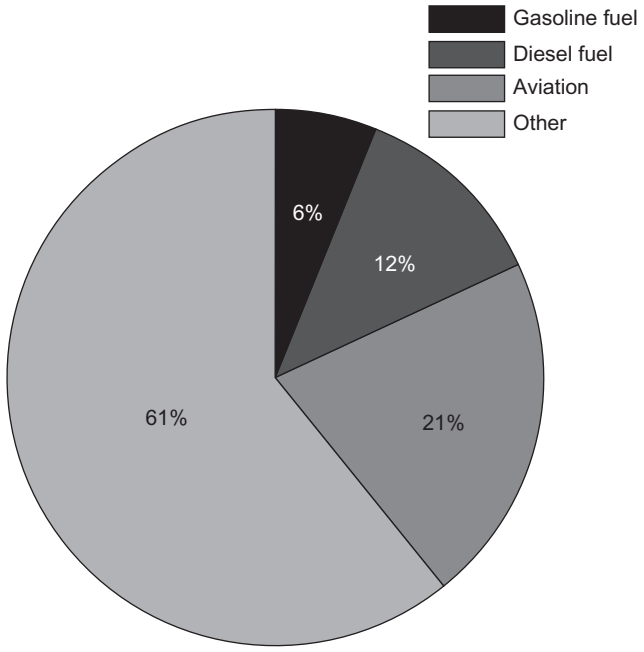
Most of the electric power generation of the United States is provided by conventional thermal power plants. Most of these power plants are operated by coal. However, from 1990 to 2000, the number of natural gas or other types of gas-operated power plants was increased significantly. 270 GW of new gas-operated thermoelectric power plants were built in United States from 1992 to 2005. Only 14 GW capacity belonged to new nuclear and coal-fired power plants, with 2.315 GW of this amount being nuclear, while the remaining is the coal-fired power plants [11]. The significant shift to the gas-operated power plants is due to the deregulation, political, and economic factors; however, nuclear and coal are considerably capital-intensive. On the other hand, there is a great potential for renewable energies in the United States. For instance, the US wind power capacity is close to 20 GW, which is sufficient to supply power to 4.5 million typical households [12]. Although there is a great availability of the solar power, solar power percentage

of total capacity is only 0.04% retrieved by plants that are currently in operation, including the new Nevada Solar One plant with 64 MW capacity and the largest solar thermal power station in the Mojave Desert with a total generation capacity of 354 MW, which is the world's largest solar plant [13].

Electric power generation in the United States for 2006 is summarized in Table 23.3 in terms of total capacity (MW), annual production (billion kWh), and units in operation [14].

According to Table 23.3, it is seen that the most contributing power source to the US energy production is the coal-fired

TABLE 23.2 US nationwide energy consumption sectors

Sector	Major use shares
Industrial: This sector mainly consumes 33% of total energy for the manufacturing, producing, and processing goods such as chemical refining, metal production, paper, and cement production	
Transportation: Twenty-eight percent of the total energy consumption is shared by this sector for land, sea, and air vehicles transporting people and goods	

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TABLE 23.2 US nationwide energy consumption sectors—cont'd

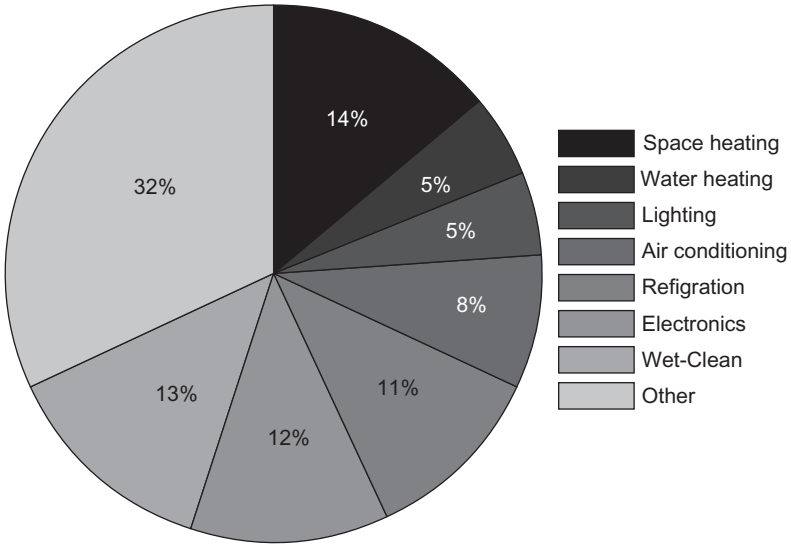
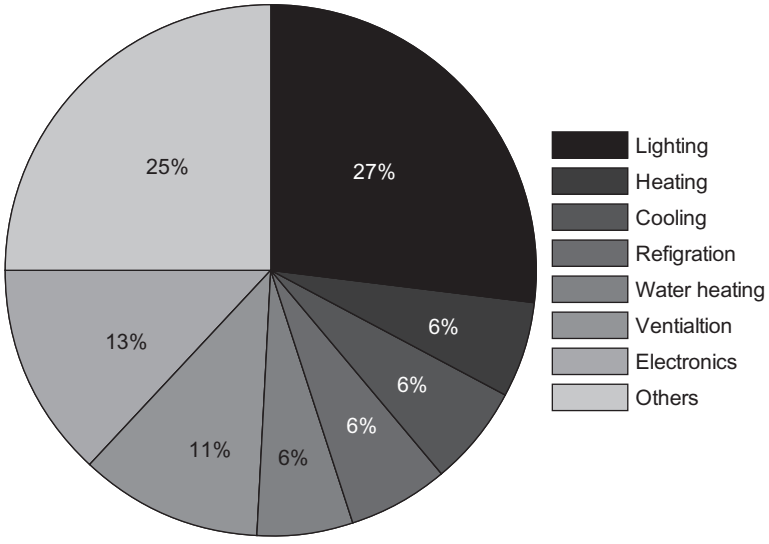
Sector	Major use shares
Residential: This sector consumes 21% of the total energy for household power requirements	
Commercial: This sector includes the business, government, and other service providing institutions, facilities, and their equipments corresponding to 17% of total energy consumption	

TABLE 23.3 2006 Energy generation in the United States

Source type	Total capacity (on nameplate) (MW)	Annual production (billions kWh)	Units in operation
Coal-fired boiler power plants	333,115	1995	1460
Combined cycle natural gas plants	216,269	505	1686
Combustion turbine generators	155,227	147	2882
Nuclear power plants	105,584	787	104
Natural-gas-fueled boiler plants	97,632	159	776
Hydroelectric power plants	96,988	282	4138
Oil-fired boiler power plants	34,975	7.8	327
Wind power	11,603	30.3	341
Diesel generators	8563	13.8	4514
Biomass	6256	53.5	270
Geothermal	3170	13.5	215
Incinerators	2671	12.3	96
Petroleum-coke-fueled power plants	1754	46.4	31
Fuel oil power plants	956	8.5	13
Solar energy	411	2.1	31

thermoelectric power plants. Although the established power capacity of the nuclear power plants is less than that of the combined cycle natural gas plants and combustion turbine generators, nuclear power plants are the second greatest source in annual energy production. This is due to the higher efficiency of these plants and under-capacity operation of natural gas power plants and combustion turbine generators. Other than the nuclear power plants and fossil-fueled power plants, hydroelectric power plants have a significant contribution to the annual production although they require a relatively large number of units in operation. This is mainly due to the relatively lower power capacity of the hydroelectric power plants. Renewable energy sources of wind and solar still have insignificant number of units in operation, and their annual contribution is considerably insignificant to the nation's total energy production although the available potential capacity of these sources are really high.

The energy production rates of energy sources are given in Fig. 23.2 [14].

The energy demand of the world is rapidly and steadily increasing. In 2007, the electric power demand of the United States was 783 GW in summer and 640 GW in the winter. It is projected by the North American Electric Reliability Corporation (NERC) that the electric power demand of the United States will increase to 925 GW for summer and 756 GW winter in 2017 [15]. Therefore, environmental concerns on global warming and sustainability along with the political considerations on the supplies' security will shift the overall energy consumption away from the fossil fuels. Nowadays, many researchers and politicians call for immediate actions for long-term sustainable energy solutions. Based on a growing consensus, peak oil may be reached in the near future, and this will result in severe oil price increases [16]. If a long-term solution cannot be developed prior to the peak oil scenario, the world economy may face a grinding halt.

This chapter focuses on naturally available energy sources and deals with the efficient utilization of these sources. Moreover, renewable and sustainable energy generation techniques are discussed in this chapter. In addition, the operating principles, efficient utilization, and grid-connection issues as well as power electronic interfaces for these renewable energy sources are demonstrated. While inventing new methodologies to maximize the efficient usage of traditional sources such as coal, oil, and natural gas, it is of great importance to develop new technologies to produce emerging sources of energy from renewables.

Consequently, by efficient use of conventional energy sources and utilizing alternate sources of energy, the reserves of the conventional energy resources can last for longer, global warming can be slowed down, and environmental pollution can be reduced [17].

23.2 Available Energy Sources

Primary sources of energy are fossil fuels such as oil, natural gas, coal, and other sources such as nuclear, solar, wind, hydroelectricity, or potential sources available in oceans. The energy that has not been converted or transformed into another form is known as primary energy source. More convenient form of energy such as electric energy is obtained by transforming primary energies in energy conversion processes. These converted forms are called as secondary energy sources.

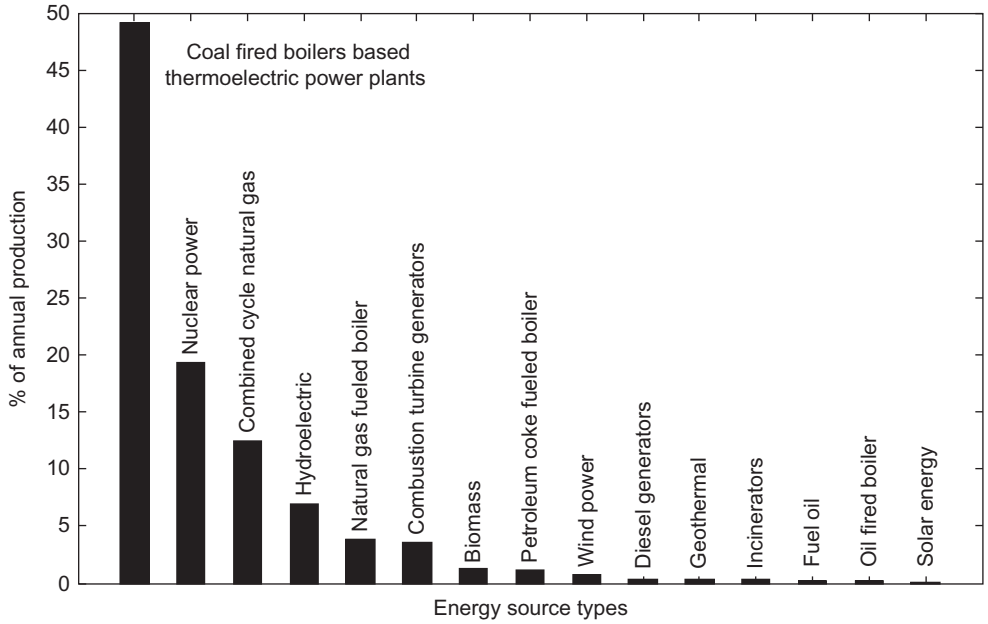


FIG. 23.2 Percentage of the energy sources to the annual energy generation.

23.2.1 Coal

Coal is the most abundant fossil fuel of the world with around 909 billion tons of reserves. It is expected to sustain for the next 155 years at the current production rate [4]. Coal is the fastest growing fossil fuel to meet the energy demand of the global community. However, coal is the dirtiest energy source with numerous pollutants and high emissions [11].

23.2.2 Oil

It is estimated that there is 57 ZJ of oil reserves on Earth. This amount includes the available but not necessarily recoverable reserves. Other estimates vary from 8 ZJ including currently proved and recoverable reserves to a maximum of 110 ZJ including nonrecoverable reserves [18]. World's current oil consumption is 85 mbd, and it is estimated that the peak consumption will be 93 mbd in 2020. Oil and its chemical derivatives are mainly used for transportation and electric power generation.

23.2.3 Natural gas

There is not any certain number indicating world's available natural gas reserves. However, according to the US Energy Information Administration, there are 237,726 billion cubic feet (cu-ft) of dry natural gas reserves in the United States, while the liquid natural gas reserves are of 9143 million barrels [19]. Natural gas has become one of the major sources of electric power generation through the steam turbines and gas turbines due to their higher efficiency. Natural gas is cleaner than any other fossil fuels and produces fewer pollutants per generated unit energy. Burning natural gas produces about 30% less carbon dioxide than burning petroleum and about 45% less than burning coal for an equivalent amount of heat [20]. Some of the natural gas power plants are operated in combined cycle mode to obtain higher efficiencies. In this operation, gas turbines are combined with the steam turbines in order to get the benefit of waste heat using steam turbines.

23.2.4 Hydropower

Hydroelectric power plants supplied 16.4% of the world's electric power in 2005 [21]. The hydroelectric power is not an effective solution, since most of the potential sites are already in use or they are not feasible to be exploited due to environmental and economical concerns. In addition, the life span of hydroelectric power plants is limited, due to soil erosion and accumulation. Because of these concerns, the construction of large hydroelectric power plants has stagnated. The new trend all over the world has been building smaller hydro power units called as *microhydro* since they can be a part of distributed generation, opening up many locations for power generation and they have less or negligible environmental effects [22,23]. On the other hand, hydroelectric power plants have no emissions since no fuel is burnt. Hence, hydropower is a clean energy source in comparison with fossil-fuel-based energy sources. In 2005, the worldwide hydroelectricity consumption reached 816 GW with 66 GW of small hydro plants and 750 GW of large plants [24].

23.2.5 Nuclear Power

In 2006, 16% of the world's total electric power production was supplied by nuclear power that is accounted 2658 TWh [11,25,26]. Total power capacity of the established nuclear power plants was about 372 GW by November 2007 [25]. The remaining uranium resources are estimated to be 2500 ZJ by the International Atomic Energy Agency [27]. Since there is plenty of available sources and developed technology, the contribution of nuclear power to the future's energy demand is not limited. However, there are political and environmental constraints, which restrict the growth of nuclear power plants. The cost of generating nuclear power is approximately equal to that of the coal power. Moreover, nuclear power has zero pollutant emissions such as CO, CO_2, NO, and SO_2.

23.2.6 Solar

Earth receives around 120,000 TW of solar energy resource per year. As an energy source, less than 0.02% of available solar resources are capable of entirely replacing all nuclear power and fossil fuels [28,29]. Although it is still expensive in comparison with conventional energy conversion techniques, the fastest growing energy source in 2007 were grid-connected photovoltaic (PV) systems. The total installed capacity reached to 8.7 GW by increasing all PV installations by 83% in 2007 [30]. High cost of manufacturing solar cells, reliance on weather conditions, storage, and grid-connection problems are the major barriers of further development of solar generation.

23.2.7 Wind

Wind is one of the greatest available potential energy sources. The available wind energy is estimated to be from 300 [31] to 870 TW [32]. Only 5% of the available energy is capable of supplying the current worldwide energy demands. However, due to fewer obstacles, most of this wind energy is available on the open oceans on which construction of wind turbines and energy transmission is relatively difficult and expensive. From 2006 to 2007, the installed wind turbines' capacity was increased by 27% to total of 94 GW according to the Global Wind Energy Council [33]. However, the actual generated power is less than the nominal capacity since the nominal capacity represents the peak output, and the actual output is around 40% of the nominal capacity due to efficiency issues and lower wind speeds [34].

23.2.8 Ocean

Energy of ocean can be categorized in three major methods: *ocean wave power*, *ocean tidal power*, and *ocean thermal power*. All of these three methods can be installed as onshore or offshore applications.

Wave energy harvesting is a concept that the kinetic energy of waves of the deep water or waves hitting the shores is captured and converted to electric energy. The kinetic energy of waves is converted to electric energy using several different methods. It is estimated that the deep-water wave power resources vary from 1 to 10 TW [35], while the total power of the waves hitting the shores may add an additional power of 3 TW [31,36]. Capturing this entire amount of power is not practical and feasible. It is estimated that 2 TW of this power can be usefully captured [37,38].

Ocean tides occur due to the tidal forces of the moon and the sun, in combination with the earth's rotation. Tidal power has a great potential for future energy generation since it is cleaner in comparison with fossil fuels and it is more predictable in comparison with other renewable energies such as wind and solar. The kinetic energy of the moving water can be captured by tidal stream or tidal current turbines. Alternatively, the barrages can be used to capture the potential energy created due to the height difference between the low and high tides. Various methods can be employed for the realization of these concepts. The total estimated tidal power potential is 3.7 TW [39]. However, only around 0.8 TW of this amount is available due to the dissipation of tidal fluctuations. The amount of energy generated from ocean tides was 0.3 GW at the end of 2005 [40], which is much less than the available potential.

The other way of generating power from the oceans is the ocean thermal energy conversion (OTEC). In this method, the temperature difference between the warm shallow water and the cold deep water is used to drive a heat engine, which in turn drives an electric generator [41]. The efficiency of OTEC power plants is relatively low [41,42] due to the power requirements of the auxiliary OTEC devices such as water intake and discharge pumps. Moreover, this technique is expensive since the efficiency is low and greater capacities of installations are required to produce reasonable amounts of energy [43].

23.2.9 Hydrogen

Hydrogen is an energy carrier [44,45]; in other words, it is an intermediate medium for energy storage and carriage. Hydrogen is the most abundant element of the Earth (approximately corresponding 75% of the elemental mass of the universe) [46], and it is the simplest and lightest element of all chemical elements with an atomic number of 1. Hydrogen exists in nature in combination with other elements such as carbon and nitrogen in fossil fuels, biological materials, or with oxygen in water [47]. Hydrogen can be combusted in air, or it can react with oxygen using fuel cells to produce energy. The resultant combustion energy or electric energy does not cause any CO or CO_2 emissions. However, splitting hydrogen from the combination of other elements require additional energy. The main source of global hydrogen production is natural gas (48%). Other sources of hydrogen production are oil (30%), coal (18%), and water electrolysis (4%) [48]. Currently, most of the hydrogen is produced from gas derivatives such as natural gas, ethane, methane, ethanol, or methanol. Hydrogen production from fossil fuels, known as reformation, contains several pollutant emissions. Although electrolysis is clean, this method has various challenges and still has very poor efficiencies and high production costs. Biological or fermentative reactions can be another method of hydrogen production; however, this method has some obstacles such as the amount of products is not significant [48,49]. Using hydrogen in hydrogen combustion engines is several percent more efficient than the conventional internal combustion engines. On the other hand, using hydrogen in the fuel cells is twice or three times more efficient than that of the internal combustion engines. However, there are several challenges for the commercialization of fuel cells such as the size, weight, cost, and durability. Other major technical difficulties related to hydrogen are the production, delivery, and storage issues.

23.2.10 Geothermal

Geothermal energy is the utilization of heat stored in the inner layers of the earth or collecting the absorbed heat derived from underground. The geothermal energy production has reached to 37.3 GW at the end of 2005 [24]. 9.3 GW of this amount is used for electric power generation, while the rest of it is used for residential or commercial heating purposes. Enhanced geothermal systems (EGS) is a technique that extends the potential for the use of geothermal energy. In this technique, the heat is extracted by building subsurface fractures to which water can be added through injection wells. Through this technique, the electric generation capacity can reach to about 138 GW [50]. The overall EGS capacity of the world is calculated to be more than 13 YJ, where 200 ZJ of this amount is extractable. By the technological improvements and investments, this amount is projected to increase over 2 YJ [51]. However, in contrary to this enormous potential, geothermal supplies less than 1% of the world's energy demand as of 2008 [21]. Geothermal energy has high availability (average daily availabilities more than 90%) and in fact has no pollutant emissions since it does not require any fuel or combustion. Furthermore, geothermal power stations do not rely on weather conditions. In addition, it is considered to be a sustainable source of energy since the extracted heat is relatively small in comparison with the heat reservoir's size. In other words, geothermal heat energy is replenished from deeper layers of the earth; therefore, it is not exhaustible.

23.2.11 Biomass

Biomass is a fuel that is also called biofuel, and the bioenergy is the energy enclosed in the biomass. Today, biomass has a small contribution to the overall energy supply, although it was the major fuel until the nineteenth century. In 2005, electric power from biomass was about 44 GW, while more than 230 GW biomass power is used for heating [40]. As a sustainable energy source, biomass is a developing industry in many countries such as Brazil, the United States, and Germany. As an alternative to the fossil fuels, biomass production is significantly increasing worldwide. The biodiesel production increased by 85% to 1.03 billion gallons in 2005, and biodiesel became the world's fastest growing renewable source of energy. Bioethanol production was also increased by 8% and reached 8.72 billion gallons during 2005 [40]. Even though it is commonly believed that biomasses may be carbon neutral, their current farming methods cause substantial carbon emissions [52,53].

23.3 Electric Energy Generation Technologies

Electric energy generation is a process where the energy sources or energy potential is converted to electric energy. Energy generation can be done in various techniques. Due to the upcoming emerging challenges in the global energy supply systems, energy from the conventional sources needs more efficiency. In addition, there should be an increase in utilization of energy generation from alternative and renewable energy sources. In the following subsections, the alternative energy sources along with their conversion to electric energy are described.

23.3.1 Thermoelectric Energy

Thermoelectric power plants are mainly coal-fired power stations. In a thermoelectric power plant, coal or other fuels are burnt in order to heat up the water in the boiler. In this system, the high pressurized steam rotates a steam turbine, which is coupled to an electric generator. After the steam passes through the turbine, it is cooled and condensed back to water in the condenser. This is known as Rankine cycle [54]. More than 80% thermal power plants all over the world operate based on this cycle. In the Rankine cycle, there are four processes in which the working fluid's state is changed as shown in Fig. 23.3 [55]. These processes can be described as follows [56,57]:

Process 1–2: When the fluid is condensed and converted to liquid form, the liquid is pumped from low to high pressure. The pumping process requires a small amount of energy.

Process 2–3: The high-pressure liquid that pumped into the boiler is heated at constant pressure until it becomes saturated dry vapor. The boiler is energized by a heat source such as a coal furnace.

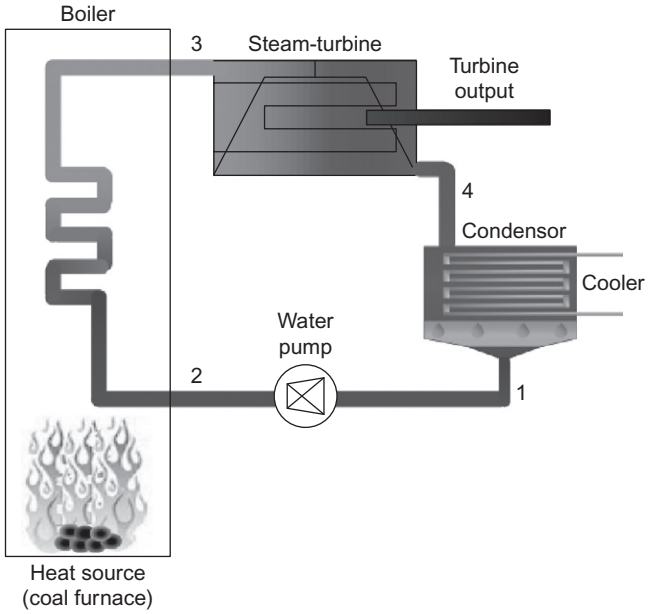


FIG. 23.3 Rankine cycle block diagram.

Process 3–4: During this process, saturated vapor passes through the steam turbine. The heat energy is converted into mechanical energy. While the steam passes through the turbine, it may somehow get condensed since this process decreases the pressure and temperature of the vapor.

Process 4–1: In this process, the vapor is condensed at a constant pressure and temperature in a condenser. As a result, wet vapor is converted to saturated liquid. The cooler helps keeping the temperature constant as the vapor changes its phase from steam to liquid.

These four processes of the Rankine cycle are shown in Fig. 23.3.

Since coal is the most abundant energy source of the world, coal-fired power plants have been widely used in electric power generation all over the world [58]. Coal is a cheap energy source, and coal-fired power plants have mature technology. Therefore, the generation cost is less, and thermoelectric power plants can be constructed anywhere close to fuel and water supply. Although the consumption sites might be relatively far away from the coal mines or water supplies, fuel and water can be transported to the generation plants. Since the coal has been the backbone of the electric power industry since the late 1800s, approximately 49% of the electric power generated in the world is supplied by coal-fired thermoelectric power plants [59].

In a simple form, the operation of a coal-fired power plant can be similar to Rankine cycle. In this form, the plant consists of a boiler, a steam turbine driving an electric generator, a condenser, and a feedwater pump. Coal is first pulverized and burnt in the steam generation furnaces. The water in the boiler tubes is heated, and steam is generated in this way at high pressures. The steam generation process is composed of three

subprocesses that are economizing, boiling, and superheating. In the economizer, the water is heated to a point that is close to the boiling point. Then, the steam is raised in the boiler. Finally, the steam is further heated and dried at the superheater. The steam at its final form is then conveyed to the steam turbine. The mechanical force pushing the turbine blades yields the steam turbine to rotate, which in turn drives the electric generator producing electricity. The cooler steam with lower pressure is released from the turbine. This steam is conveyed to the condenser to be liquefied. This water is pumped back to the steam generator, and the closed loop system is completed [56]. Considering the other auxiliary devices and peripheral components such as cooling tower, coal conveyor, and ash and waste management units, the schematic of a coal-fired thermoelectric power plant can be presented in Fig. 23.4.

The components of the thermoelectric power plant are described in Table 23.4.

TABLE 23.4 Thermoelectric power plant components

1—Coal conveyor	10—Air intake pipe	19—Low-pressure turbine
2—Coal hopper	11—Air preheater	20—Condenser
3—Pulverization mill	12—Feed heater	21—Electric generator
4—Boiler drum	13—Steam governor	22—Induced draught fan
5—Ash hopper	14—High-pressure turbine	23—Cooling water pump
6—Superheater	15—Deaerator	24—Power transformer
7—Forced draught fan	16—Intermediate-pressure turbine	25—Cooling tower
8—Reheater	17—Precipitator	26—Chimney stack
9—Economizer	18—Boiler feed pump from condenser	27—Transmission network

The operation of the cola-fired power plant begins with the coal conveyor. From an exterior stack, coal is conveyed through a coal hopper to the pulverizing fuel mill where it is grounded and converted to a fine powder. The pulverized coal is mixed with preheated air. The air is taken by an air intake pipe and pumped to be mixed with pulverized coal. This preheated air is supplied by the forced draught fan. In the boiler, where the air-fuel mixture is ignited at high pressure, the generated heat increases the temperature of the water. The water then changes its phase to steam where it flows vertically up the boiler tubes. This steam is passed to the boiler drum where its remaining water content is separated. This dry steam is then passed through a manifold from the drum into the superheater. In the superheater, further pressure and temperature increase; steam reaches about 200 bar and 570°C. The turbine process of the power plant comprises three stages: high-pressure turbine, intermediate-pressure turbine, and low-pressure turbine. First, the steam passes to the high-pressure turbine through the pipes. Both the manual turbine control and the automatic set-point following can be provided by a steam governor valve. The temperature and the pressure of the steam decrease when it is exhausted from the high-pressure turbine. This steam is returned to the boiler reheater for further use. The reheated steam passes to the intermediate-pressure turbine. The steam released from the intermediate-pressure turbine is passed directly to the low-pressure turbine. Now, the steam is cooler and just above its boiling point. This steam is then condensed in the condenser by contacting thermally with the cold water tubes of the condenser. As a result, the steam is converted back into water, and the condensation causes a vacuum effect inside the condenser chest. The condensed water is prewarmed by the feed heater using the heat of the steam released from the high-pressure turbine and then in the economizer. Then, this prewarmed water is deaerated and passed by a feedwater pump,

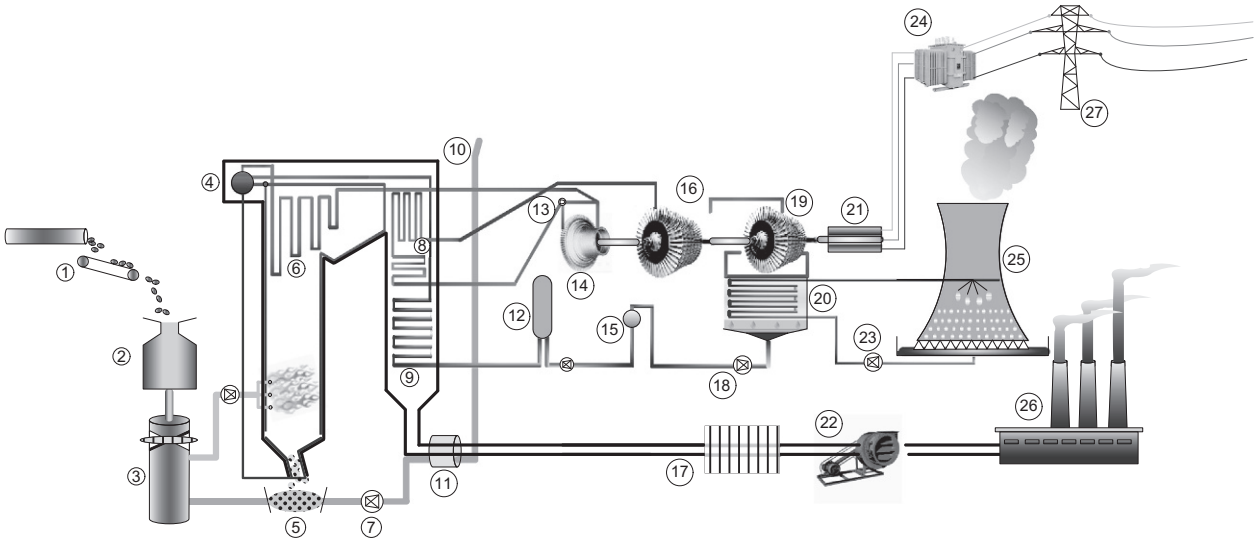


FIG. 23.4 Schematic diagram of the thermoelectric power plant.

which completes the closed cycle. The cooling tower cools down the water from the condenser creating an intense and visible plume. Finally, the water is pumped back to the cooling water cycle. The induced draft fan draws the exhaust gas of the boiler. Here, an electrostatic precipitator is used. Finally, this exhaust gas is vented through the chimneys of the power plant.

In the thermoelectric power plants, load-following capability, efficiency, fuel and water management, and emissions are important issues. In addition, the active and reactive outputs of the power plant's generators and frequency and voltage regulations have impact on the power plant operation.

23.3.2 Hydroelectric Energy

Hydroelectric energy is generated by the kinetic and potential energy of flowing or falling water by the effect of gravitational force. Hydroelectric is the most mature and widest utilized form of renewable energies. Hydroelectric energy has approximately 20% contribution to the overall world energy generation [60]. No fuel is burnt at hydroelectric power plants; therefore, they do not have greenhouse gas emissions. The operating cost is relatively low since the water running the plant is supplied free by the nature. It is a renewable source of energy since the rainfall renews and enriches the water reservoirs.

Hydroelectric energy is generally obtained from the potential energy of dammed or reservoired water. When the water falls from a certain height of the reservoir output, it loses its potential energy and gains kinetic energy. The water flow drives a water turbine that is coupled to an electric generator, which in turn generates electricity. This generated energy is a function of the water volume and the difference between the source and outflow of the water [61]. This height difference between the water output and turbine is called as "head." The potential energy of the water is proportional to the head. In order to generate greater amounts of energy, the head can be increased by running the water for hydraulic turbine through a large and long pipe called as penstock [62]. The cross-sectional view of a hydraulic dam and the hydroelectric power plant components are represented in Fig. 23.5.

In Table 23.5, these components are explained.

Electric power generation in a hydroelectric power plant can be approximately calculated as [63]:

$$P = (hrg)\eta_t\eta_g \tag{23.1}$$

where P is the generated power (kW), h is the height (m), r is the water flow rate (m^3/s), and g is the gravitational acceleration (m/s^2). In Eq. (23.1), the term hrg represents the potential energy of the water. η_t and η_g represent the efficiency of the water turbine and the generator, respectively. These efficiency rates are required for the water potential energy conversion into the electric energy.

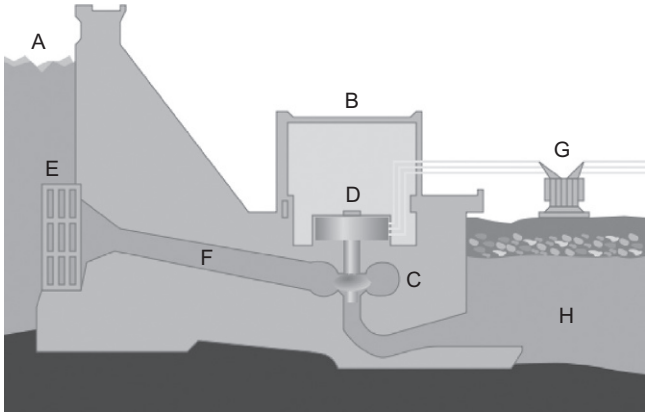


FIG. 23.5 A hydroelectric dam and power plant components [62].

TABLE 23.5 Hydroelectric power plant components

A—Reservoir	E—Water intake
B—Intake	F—Penstock
C—Water turbine	G—Transformer and transmission lines
D—Electric generator	H—River

The other methods of electric generation by hydroelectricity are the pumped storage hydroelectric power plants and run-of-the-river plants. In pumped storage method, the water is pumped into higher elevations by using the excess generation capacity during the periods when electric demand is lower. The water is released back into lower elevations through a turbine when the electric power demand is higher. In this method, water acts as an energy carrier in order to compensate the generation-consumption difference in a commercial device by improving the daily load factor [61–63]. In run-of-the-river plants, water reservoirs are not used, and the kinetic energy of the flowing water through a river is captured using waterwheels.

23.3.3 Solar Energy Conversion and Photo-Voltaic Systems

Solar energy is one of the growing renewable energy sources, which is plentiful and has the greatest availability among other energy sources. The amount of solar energy supplied from the sun to the earth is capable of satisfying the total energy requirements of the earth for 1 year [64]. Furthermore, solar energy does not produce pollutants or harmful by-products; it is free of emissions. Solar energy is applicable to many fields such as vehicular, residential, space, and naval applications.

23.3.3.1 Photovoltaic Effect and Semiconductor Structure of PVs

PV effect is known as a physical process in which a PV cell converts the sunlight into electricity. When a PV cell is subject to the sunlight, the absorbed amount of light generates electric

energy, while remaining sunlight can be reflected or passed through. The electrons in the atoms of the PV cell are energized by the energy of the absorbed light. With this energy, these electrons move from their normal positions in the semiconductor PV material, and they create an electric flow, that is, electric current through an external electric circuit connected to the PV cell terminals. The built-in electric field that is a specific electric feature of the PV cells provides the voltage potential difference that drives the current through an external load [65]. Two layers of different semiconductor materials are placed in contact with each other in order to induce the built-in electric field within a PV cell. The first layer that is *n-type* has abundance of electrons, and it is negatively charged. The other layer that is *p-type* has abundance of holes, and it is positively charged. Since the *n-type* silicon has excess electrons and *p-type* silicon has excess holes, contacting these layers together creates a p/n junction at their interface, thereby creating an electric field. In this contact, excess electrons move from the n-type side to the p-type side. As a result, a positive charge is built up along the n-type side of the interface and negative charge along the p-type side. Thus, an electric field is created at the surface where the layers meet, called the p/n junction. This electric field is due to the flow of electrons and holes. This electric field causes the electrons to move from the semiconductor toward the negative surface to carry current. At the same time, the holes move in the opposite direction, toward the positive surface, where they wait for incoming electrons [65]. The basic structure of a p-n junction in a PV cell is illustrated in Fig. 23.6.

23.3.3.2 PV Cell/Module/Array Structures

A PV or solar cell is the basic building block of a PV (or solar-electric) system. An individual PV cell is usually quite small, typically producing about 1 or 2 W of power [66]. PV cells can be connected together to form a larger unit called modules in order to increase the power output of PV cells. Modules can be connected together and form larger units that are called arrays to generate more electric power. The output voltage of a PV system can be boosted by connecting the cells or modules in series. On the other hand, the output current can reach higher values by connecting them in parallel.

23.3.3.3 Active and Passive Solar Energy Systems

Based on the solar tracking capability, solar energy systems can be categorized into two types, passive and active systems [67,68]. In passive solar energy systems, there are not any moving mechanisms for the panels. In this technique, the energy is absorbed and retained, and spaces are designed that naturally circulate air to transfer energy and referencing the position of a building to the sun to enhance energy capture. On the other hand, in active solar energy systems, typically, there are electric and mechanical components such as tracking mechanisms, sensors, motors, pumps, and fans to capture sunlight and process it into usable forms such as heating, lighting, and electricity. The panel positions are controlled in order to maximize exposure to the sun.

23.3.3.4 Components of a Complete Solar Energy System

In Fig. 23.7, the block diagram of a solar energy system is demonstrated. In this system, the sunlight is captured by the PV array. The photodiode or photosensor signals determine the sun-tracking motor positions. This sun-tracking control helps following the daily and seasonal solar position changes to face the sun directly and capture the most available sunlight.

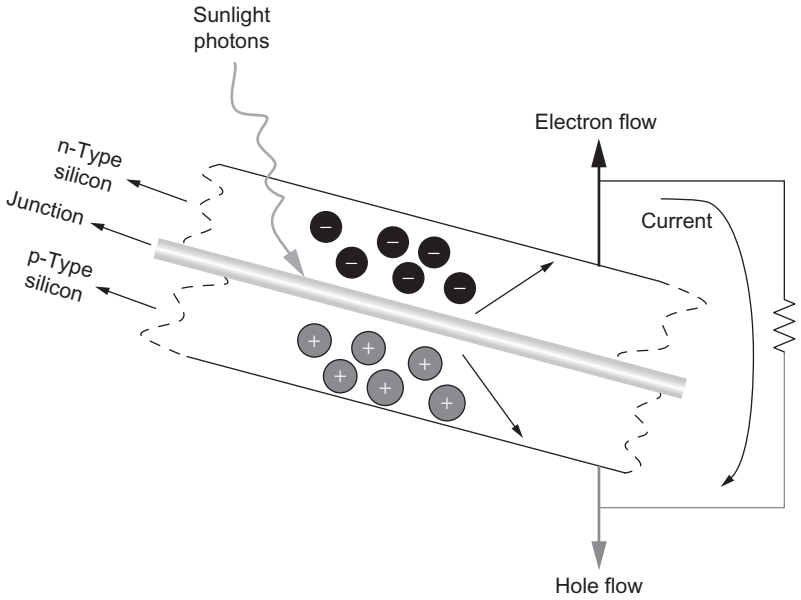


FIG. 23.6 P-n junction structure and current flow in a PV cell.

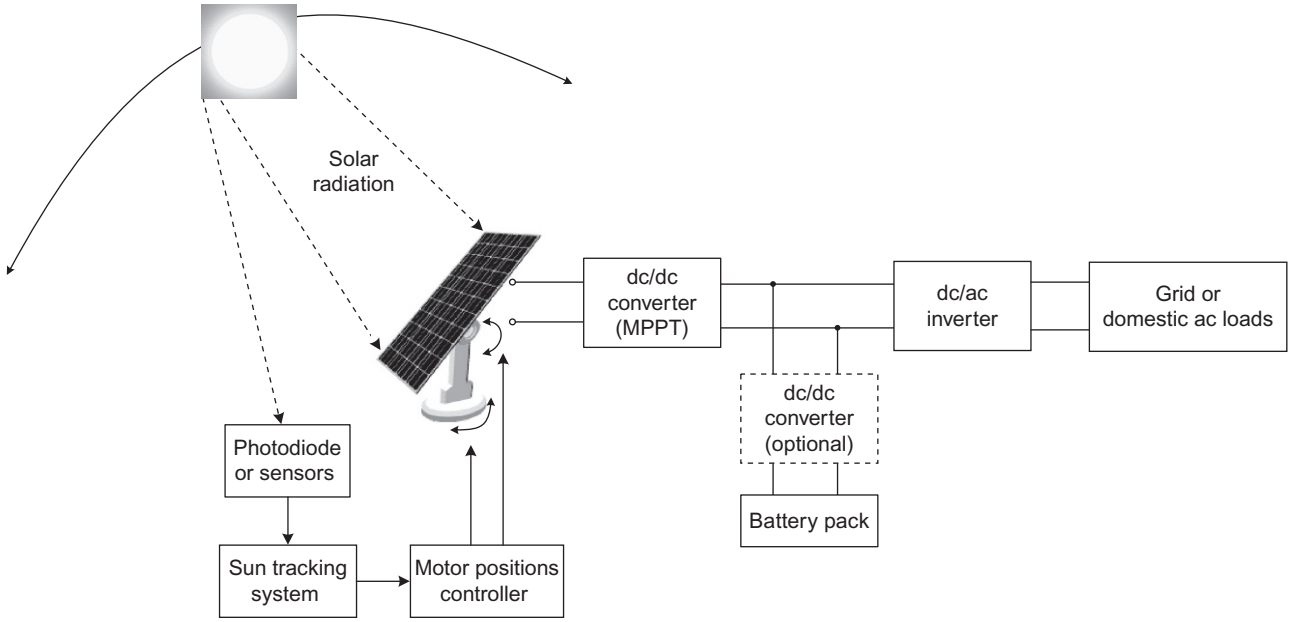


FIG. 23.7 A solar energy system.

A dc/dc converter is employed at the PV panels' output in order to operate at the maximum power point (MPP) based on the current-voltage (*I-V*) characteristics of the PV array [69]. This dc/dc converter is controlled to operate at the desired current and voltage output of the PV array. A dc/ac inverter is usually connected to the output of this MPPT dc/dc converter in order to feed the ac loads for grid interconnection. A battery pack can be connected to the dc bus of the system to provide extra power that might not be available from the PV module during night and cloudy periods. The battery pack can also store energy when the PV module generates more power than the demanded. A grid connection is also useful to draw/inject power from/to the utility network to take the advantage of excess power or to recharge the batteries using grid power during the peak-off periods of the utility network.

23.3.3.5 *I-V* Characteristics of Photovoltaic (PV) Systems, PV Models, and Equivalent PV Circuit

PV systems have a special current-voltage characteristic. As more current is drawn from the PV system, the system output voltage decreases. These characteristic curves differ at different solar insulation and temperature conditions; hence, the curves can be obtained by varying the load resistance (varying the output current) and measuring the output voltage for many different current values. *I-V* curve passes through two points for zero voltage and zero current.

- The short-circuit current (I_{sc}): I_{sc} is the current produced when the positive and negative terminals of the cell are short-circuited, and the voltage between the terminals is zero, which corresponds to zero load resistance.
- The open-circuit voltage (V_{oc}): V_{oc} is the voltage across the positive and negative terminals under open-circuit conditions, when the current is zero, which corresponds to infinite load resistance.

In order to extract maximum power from a PV system, for a constant ambient condition, there is only one current-voltage pair. On the *I-V* curve, the maximum power point (Pm) occurs when the product of current and voltage is maximum. Although the current is maximum, no power is produced at the short-circuit current due to zero voltage. In addition, no power is produced at the open-circuit voltage due to zero current. The MPP is somewhere between these two points. Maximum power is generated at about the "knee" of the curve. This point represents the maximum efficiency of the solar device in converting sunlight into electricity [70]. A typical *I-V* curve characteristic of a PV system is given in Fig. 23.8.

PV systems exhibit nonlinear *I-V* characteristics [71]. There are various models available to mathematically model the *I-V* characteristics of the PV systems. An equivalent circuit expressing the PV model characteristics is shown in Fig. 23.9. This model is known as single-diode model and is one of the most common equivalent circuits representing PV system behaviors.

In this model, open-circuit voltage and short-circuit current are the key parameters. Illumination or solar radiation affects the short-circuit current, while the open-circuit voltage is affected by the material and temperature. In this model, I_{SC} is the short-circuit current, I_s is the diode reverse saturation current, m is the diode ideality factor (generally various between 1 and 5), and V_T is the temperature voltage expressed as $V_T = kT/q$, which is 25.7 mV at 25°C. The equations defining this model are

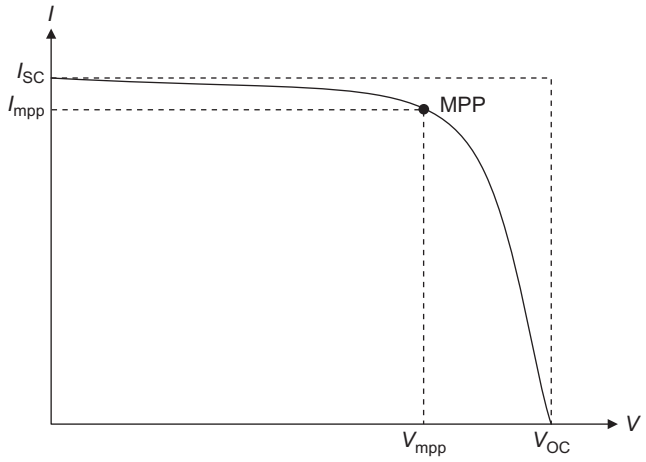


FIG. 23.8 A typical *I-V* curve characteristic of a PV system.

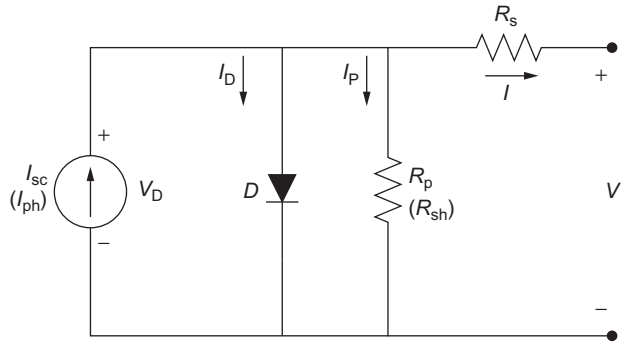


FIG. 23.9 Single-diode model of solar cell equivalent circuit.

$$I_D = I_S\left[e^{\frac{V}{mV_T}} - 1\right] \tag{23.2}$$

$$I = I_{SC} - I_D \tag{23.3}$$

and

$$V = mV_T \ln\left[\frac{I_{SC} - I}{I_S} + 1\right] \tag{23.4}$$

The *I-V* characteristic of the solar cell can be alternatively defined by [72]

$$\begin{aligned} I &= I_{ph} - I_D \\ &= I_{ph} - I_0\left[\exp\left(\frac{q(V + R_sI)}{Ak_BT}\right) - 1\right] - \frac{V + R_sI}{R_{sh}} \end{aligned} \tag{23.5}$$

where V is the PV output voltage (V), I is the PV output current (A), I_{ph} is the photocurrent (A), I_D is the diode current (A), I_0 is the saturation current (A), A is the ideality factor, q is the electronic charge (C), k_b is Boltzmann's constant (JK^{-1}), T is the junction temperature (K), R_s is the series resistance (Ω), and R_{sh} is the shunt resistance (Ω).

23.3.3.6 Sun Tracking Systems

Incident solar radiation is the most important parameter for the power generated by solar energy systems. Sun changes its position during the day from morning to night. Moreover, the sun orbit differs from one season to another. By properly following the sun, through utilizing sun-tracking systems, the incident solar irradiance can be effectively increased [73]. A sun tracker is an electromechanical component used for orienting a solar PV panel, concentrating solar reflector, or lens toward the sun. Solar panels require a high degree of accuracy to ensure that the concentrated sunlight is directed precisely to the PV device. Solar tracking systems can substantially improve the amount of power produced by a system by enhancing morning and afternoon performance. For instance, the orientation of PV panels can increase the solar-electric energy conversion efficiency between 20% and 50% [74–78]. A fixed system oriented to a fixed sun-facing direction will have a relatively low annual production because they do not move to track the sun, which yields significant increase of incident irradiation. An efficient sun-tracking system should be capable of movement from north to south and from east to west as shown in Fig. 23.10.

23.3.3.7 Maximum Power Point Tracking (MPPT) Techniques

The conditions of radiation and temperature affect the current-voltage (*I-V*) characteristics of solar cells. The voltage and current should be controlled to track the maximum power of the PV systems in order to operate the PV systems at the point of (V_{max} and I_{max}). Maximum power point tracking (MPPT) techniques are used to extract maximum available power from the solar cells by controlling the voltage and current. Systems composed of various PV modules located at different positions should have individual power conditioning systems to ensure the MPPT for each module [79]. In this section, most common and applicable MPPT techniques are described.

Incremental conductance (INC) based maximum power point tracking (MPPT) technique

The incremental conductance technique is the most commonly used MPPT for PV systems [72,80–82]. The technique is based

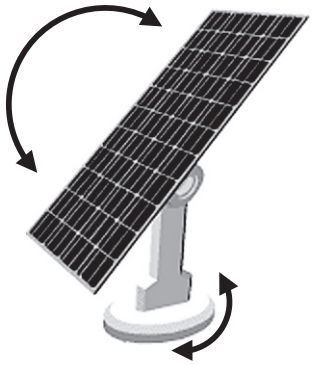


FIG. 23.10 Rotations of a sun-tracking system.

on the fact that the sum of the instantaneous conductance I/V and the incremental conductance $\Delta I/\Delta V$ is zero at the MPP, negative on the right side of the MPP, and positive on the left side of the MPP.

If the change of current and change of voltage is zero at the same time, no increment or decrement is required for the reference current. If there is no change for the current, while the voltage change is positive, reference current should be increased. Similarly, if there is no change for the current while the voltage change is negative, reference current should be decreased. Contrarily, the change of the current might not be zero. If the current change is not zero, while $\Delta V/\Delta I = -V/I$, the PV is operating at MPP. If the current change is not zero and $\Delta V/\Delta I \neq -V/I$, then $\Delta V/\Delta I > -V/I$. If $\Delta V/\Delta I \neq -V/I$ and $\Delta V/\Delta I > -V/I$, the reference current should be decreased. However, if $\Delta V/\Delta I \neq -V/I$ and $\Delta V/\Delta I < -V/I$, the reference current should be increased in order to track the MPP.

Practically, due to the noise and errors, satisfying the condition of $\Delta I/\Delta V = -I/V$ may be very difficult [83]. Therefore, this condition can be satisfied with good approximation by

$$|\Delta I/\Delta V + I/V| < \varepsilon \tag{23.6}$$

where ε is a positive small value. Based on this algorithm, either the operating point is located in BC interval, or it is oscillating among the AB and CD intervals as shown in Fig. 23.11.

Selecting the step size (ΔV_{ref}), shown in Fig. 23.11, is a tradeoff of accurate steady tracking and dynamic response. If larger step sizes are used for quicker dynamic responses, the tracking accuracy decreases, and the tracking point oscillates around the MPP. On the other hand, when small step sizes are selected, the tracking accuracy will increase. In the meantime, the time duration required to reach the MPP will increase [84].

The normalized IV, PV (power-voltage), and absolute derivative of PV characteristics of a PV array are shown in Fig. 23.12.

From these characteristics, it is seen that the $|dp/dV|$ decreases as the MPP is approached and it gets greater when the operating point gets away from the MPP. This relation can be given by

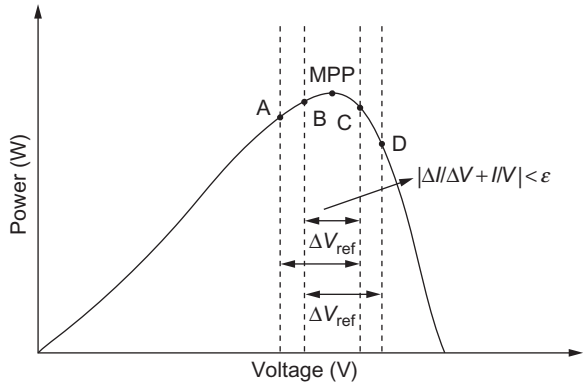


FIG. 23.11 Operating point trajectory of incremental-conductance-based MPPT.

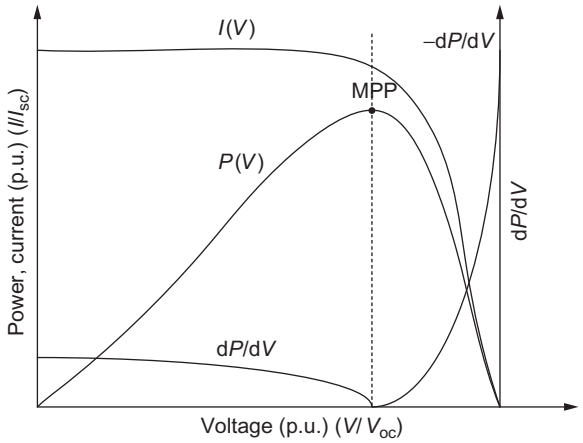


FIG. 23.12 Normalized IV, PV, and $|dP/dV|$ characteristics of a PV array.

$$\begin{cases} dP/dV < 0, \text{right of MPP} \\ dP/dV = 0, \text{ at MPP} \\ dP/dV > 0, \text{ left of MPP} \end{cases} \tag{23.7}$$

In order to obtain the operating MPP, dP/dV should be calculated. The dP/dV can be obtained by only measuring the incremental and instantaneous conductances of the PV array, that is, $\Delta I/\Delta V$ and I/V [80].

$$\frac{dP}{dV} = \frac{d(IV)}{dV} = I + V\frac{dI}{dV} \tag{23.8}$$

Other maximum power point tracking techniques

In the perturb-and-observe technique, the current drawn from the PV array is perturbed in a given direction, and if the power drawn from the PV array increases, the operating point gets closer to the MPP, and thus, the operating current should be further perturbed in the same direction [85]. If the current is perturbed and this results in a decrease in the power drawn from the PV array, this means that the point of operation is moving away from the MPP, and therefore, the perturbation of the operating current should be reversed.

The P-V and I-V characteristics of a roof-mounted PV array are monotonously increasing or decreasing under stable insulation conditions. The I-V characteristic is a function of voltage, insulation level, and temperature. From these characteristics, MPPT controllers can be developed based on the linearized I-V characteristics [86–88].

Fractional open-circuit voltage-based method [89–96], fractional short-circuit-based method [96,97], fuzzy-logic-controller-based method [88,98–106], neural-network-based method [107–112], ripple-correlation-based method [113], current-sweep-based method [114], and dc-link capacitor

droop-control-based method [115,116] are the other applicable methods for MPP tracking.

23.3.3.8 Power Electronic Interfaces for PV Systems

Power electronic interfaces are used either to convert the dc energy to ac energy to supply ac loads or connection to the grid or to control the terminal conditions of the PV module to track the MPP for maximizing the extracted energy. They also provide wide operating range, capability of operation over different daily and seasonal conditions, and reaching the highest possible efficiency [117]. There are various ways to categorize power electronic interfaces for solar systems. In this book, power electronic interfaces are categorized as power electronic interfaces for grid-connected PV systems and stand-alone PV systems.

Power electronic interfaces for grid connected PV systems

The power electronic interfaces for grid-connected PV systems can be classified into two main criteria: classification based on inverter utilization and classification based on converter stage and module configurations.

Topologies based on inverter utilization: The centralized inverter system is illustrated in Fig. 23.13.

In this topology, PV modules are connected in series and parallel to achieve the required current and voltage levels. Only one inverter is used in this topology at the common dc bus. In this topology, the inverter's power losses are higher than string inverter or multi-inverter topologies due to the mismatch between the modules and necessity of string diodes that are connected in series. In this topology, voltage boost may not be required since the voltage of series-connected string voltages is high enough [118].

In string inverter topology, the single string of modules is connected to the separate inverters for each string [119]. In this topology, voltage boosting may not be required if enough number of components are connected in series in each string.

In the multistring inverter topology, several strings are interfaced with their own integrated dc/dc converter to a common dc/ac inverter [120,121] as shown in Fig. 23.14.

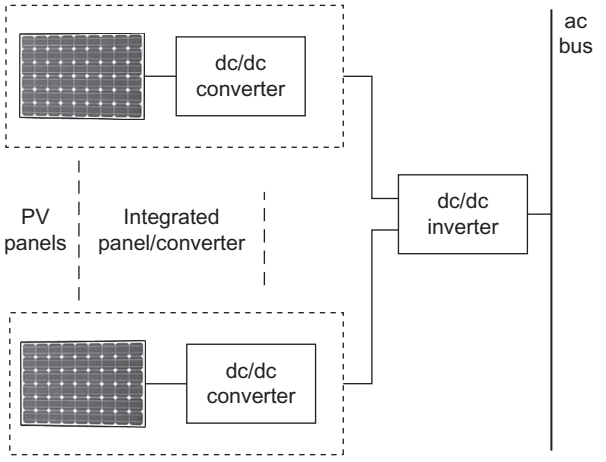


FIG. 23.14 Multistring inverters topology.

Therefore, this is a flexible design with high efficiency. In this topology, each PV module has its integrated power electronic interface with utility. The power loss of the system is relatively lower due to the reduced mismatch among the modules, but the constant losses in the inverter may be the same as for the string inverter. In addition, this configuration supports optimal operation of each module, which leads to an overall optimal performance [118]. This is due to the fact that each PV panel has its individual dc/dc converter and maximum power levels can be achieved separately for each panel.

Topologies based on module and stage configurations: The power electronic conditioning circuits for solar energy systems can be transformerless, or they can utilize high-frequency transformers embedded in a dc/dc converter, which avoids bulky low-frequency transformers. The number of stages in the presented topologies refers to the number of cascaded converters/inverters in the system.

Isolated dc/dc converters consist of a transformer between the dc/ac and ac/dc conversion stages [122]. This transformer provides isolation between the PV source and load. A typical topology is depicted in Fig. 23.15.

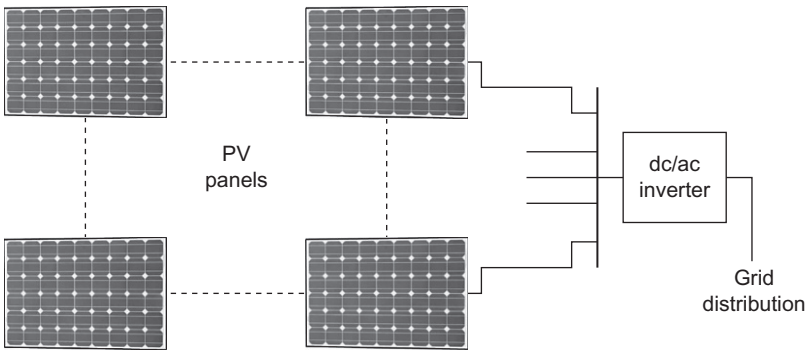


FIG. 23.13 Conventional PV system technology using centralized inverter system topology.

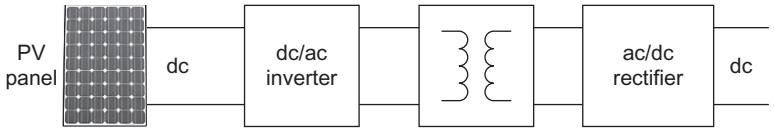


FIG. 23.15 Isolated dc/dc converter topology.

In the topology shown in Fig. 23.15, the outputs of the PV panel and dc/dc converter are dc voltages. The two-stage dc/dc converter consists of a dc/ac inverter, a high-frequency transformer, and a rectifier. In this topology, a capacitor can be used between the bottom leg of the high-frequency inverter and the transformer, forming an LC resonant circuit with the equivalent inductance of the transformer. This resonance circuit reduces the switching losses of the inverter. Alternatively, only two switches are enough if a push-pull converter is used; however, this topology requires a middle terminal outputted transformer [118].

The topologies shown in Fig. 23.16A and B are two-stage single-module topologies, in which a dc/dc converter is connected to a dc/ac converter for grid connection. The dc/dc converter deals with the MPP tracking, and the dc/ac inverter is employed to convert the dc output to ac voltage for grid connection. These are nonisolated converters since they are transformerless.

Instead of using a full-bridge inverter for the dc/ac conversion stage, a half-bridge inverter can also be used. In this way, number of switching elements can be reduced, and the controller can be simplified; however, for the dc bus, two-series-connected capacitor is required to obtain the midpoint. This midpoint of two-series-connected capacitors will be used as the negative terminal of the ac network of the half-bridge configuration.

The single-stage inverter for multiple modules is depicted in Fig. 23.17, which is the simplest grid-connection topology [123]. The inverter is a standard voltage-source PWM inverter, connected to the utility through an LCL filter. The input voltage, generated by the PV modules, should be higher than the peak voltage of the utility. The efficiency is about 97%. On the other hand, all the modules are connected to the same MPPT device. This may cause severe power losses during partial shadowing. In addition, a large capacitor is required for power decoupling between PV modules and utility [124].

A topology for multimodule multistring interfaces is shown in Fig. 23.18 [121,125]. The inverter in Fig. 23.18 consists of up to three boost converters, one for each PV string, and a common half-bridge PWM inverter. The circuit can also be constructed with an isolated current- or voltage-fed push-pull or full-bridge converter [126] and a full-bridge inverter toward the utility. The voltage across each string can be controlled individually [121,126].

As an alternative to the topology shown in Fig. 23.18, other types of dc/dc converter can be employed to the first stage, such as isolated dc/dc converters.

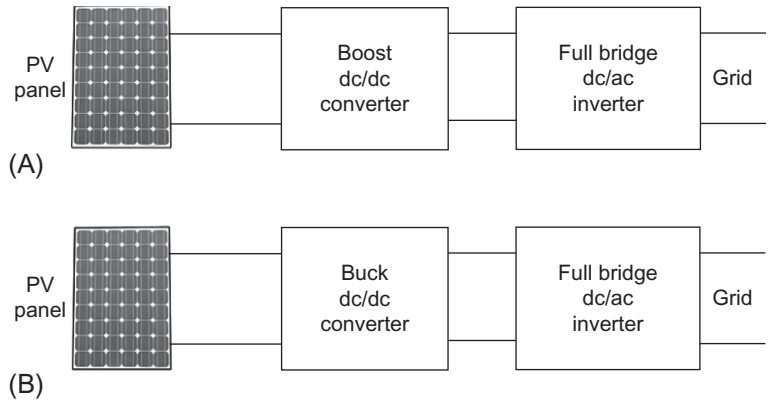


FIG. 23.16 (A) Boost converter with full-bridge inverter; (B) buck converter with full-bridge inverter.

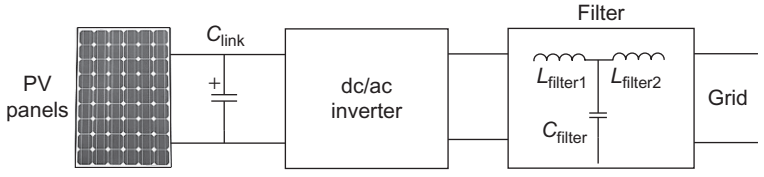


FIG. 23.17 Single-stage inverter for multiple modules.

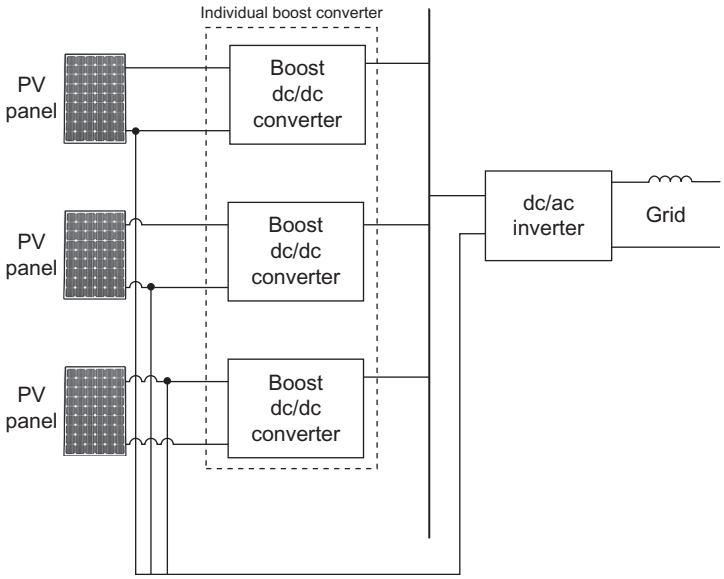


FIG. 23.18 Topology of the power electronics of the multistring inverter.

Power electronic interfaces for stand-alone PV systems
The stand-alone PV systems are composed of a storage device and its controller for sustainable satisfaction of the load power demands [127]. The storage device with the controller should provide the power difference when the available power from the PV panel is smaller than the required power at the load bus [128]. When the available power from the PV panel is more than the required power, the PV panel should supply the load power, and the excess power should be used to charge the storage device. A simple PV panel/battery connection topology is shown in Fig. 23.19.

In this simple topology, the dc/dc converter between the battery and the PV panel is used to capture all the available power from the PV panel. In this system, battery pack acts as an energy buffer, charged from the PV panel and discharged through the dc/ac inverter to the load side. The charging controller determines the charging current of the battery, depending on the MPP of the PV panels at a certain time. When there is no solar insulation available, the dc/dc converter disables, and the stored energy within the battery supplies the load demands. The battery size should be selected so that it can supply all the power demands during a possible no-insulation period. In addition, it could be fully charged during the insulated periods to store the energy for future use. Since the combined model produces ac electric energy, it should be converted to ac electric energy for domestic electric loads. The combined system requires a dc/ac inverter, which is also used to match the different dynamics of the combined energy system and various loads. The proper response of the PV/battery system to the overall load dynamics can be achieved by generating appropriate switching signals to the inverter while modulating for both active and reactive powers. The load bus voltage can be controlled by the modulation index control of the inverter; while the load control can be achieved by the phase angle control of the inverter.

23.3.4 Wind Turbines and Wind Energy Conversion Systems

Wind turbines are devices that are capable of capturing the kinetic energy of winds. This kinetic energy is converted to mechanical energy to rotate the turbine that is coupled to an electric generator. In this way, kinetic energy of the wind can be converted into a usable form of energy, that is, electric

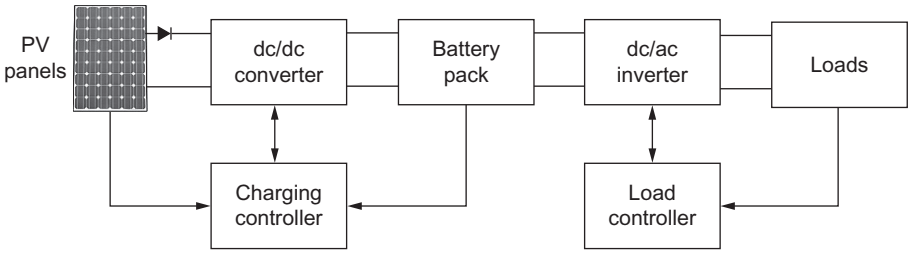


FIG. 23.19 PV/battery connection for stand-alone applications.

energy. Wind turbines can be installed stand-alone to power remote or isolated locations, or they can be grid-connected, to supply power to the utility grid. Wind power is renewable, widely distributed, plentiful, and it is a clean way of energy conversion. Additionally, it contributes in reducing the greenhouse gas emissions since it can be used as an alternative to fossil-fuel-based power generation [129]. Although wind energy has a great potential to significantly contribute the world's power generation, only 1% of worldwide power requirement is supplied by wind turbines [130].

Several key parameters such as air density, area of the blades, wind speed, and rotor area need to be considered in order to efficiently capture wind energy. Wind force is converted into a torque that rotates the blades of wind turbine. The wind force is stronger in higher air densities. In other words, kinetic energy of the wind depends on air density, and heavier winds carry more kinetic energy. At normal atmospheric pressure and at 15°C, the weight of the air is 1.225 kg/m^3, but if the humidity increases, the density decreases slightly. The other fact that determines the air density is whether the air is warm or cold. Warmer winds are less dense than cold ones, so at high altitudes, the air is less dense [131]. Besides the area of the blades (air swept area), the diameter of the blade plays important role in captured wind energy. Under the same conditions, more wind can be captured with longer blades and bigger rotor area of wind turbine [130,131]. The other parameter is the wind speed. It is expected that wind kinetic energy arises as wind speed increases [131].

Kinetic energy of the wind can be expressed as

$$E_k = \frac{1}{2} m \cdot v^2 = \frac{1}{2} \rho \cdot R^2 \cdot \pi \cdot d \cdot v^2 \tag{23.9}$$

where E_k represents kinetic energy of the wind, m stands for the mass of the wind, v is wind speed, ρ is air density, A is rotor area, R is blade length, and d stands for thickness of the "air disc" shown in Fig. 23.20.

Hence, the overall wind power (P) is [131]

$$P = \frac{E_k}{t} = \frac{1}{2} \rho \cdot R^2 \cdot \pi \cdot v^3 \tag{23.10}$$

From (23.10), it can be seen that the power content of the wind varies with the cube (the third power) of the average wind speed as shown in Fig. 23.21.

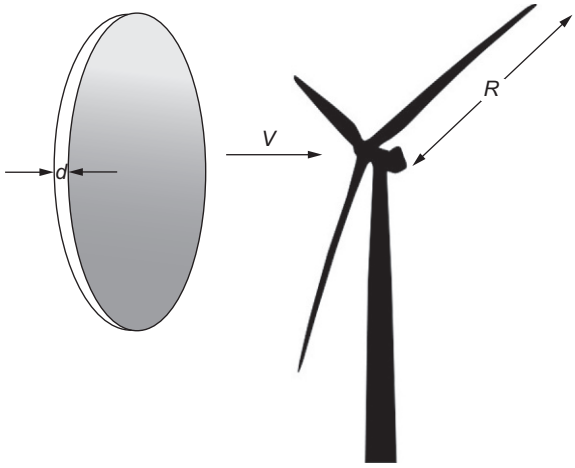


FIG. 23.20 Kinetic energy of wind.

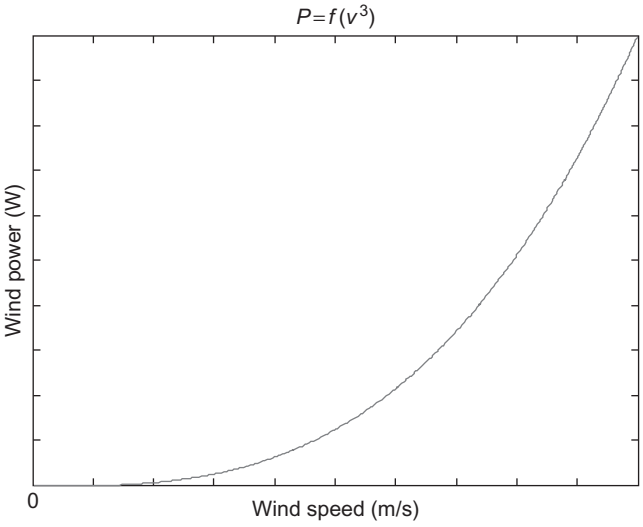


FIG. 23.21 Specific wind power due to wind speed variation.

23.3.4.1 Wind Turbine Power

Betz's law

The theoretical maximum power that can be extracted from the wind is demonstrated by Betz's law [132,133]. The wind turbines extract the kinetic energy of the wind. Higher wind speed results in higher extracted energy. It should be noted that the wind speed after turbine (after passes through turbine) is much lower than before it comes to the turbine (before energy is extracted) since the wind loses its speed by transferring its kinetic energy to wind turbine. That means wind speed before wind approaches (in front of) the turbine and its speed after (behind) turbine are different. Fig. 23.22 shows both speeds. The wind after the turbine has less amount of energy due to decreased speed of wind.

The decreased wind speed, after turbine, provides information on the amount of possible extracted energy from the wind. The extracted power from the wind can be calculated using (23.7)

$$P_{extract} = \frac{E_k}{t} = \frac{1}{2} \rho \cdot R^2 \cdot \pi \cdot \frac{v_a + v_b}{2} \cdot \left(v_b^2 - v_a^2 \right) \tag{23.11}$$

where $P_{extracted}$ shows maximum extracted power from the wind, v_a and v_b are wind speeds after and before passing through the turbine, ρ is the air density, and R demonstrates the radius of the blades.

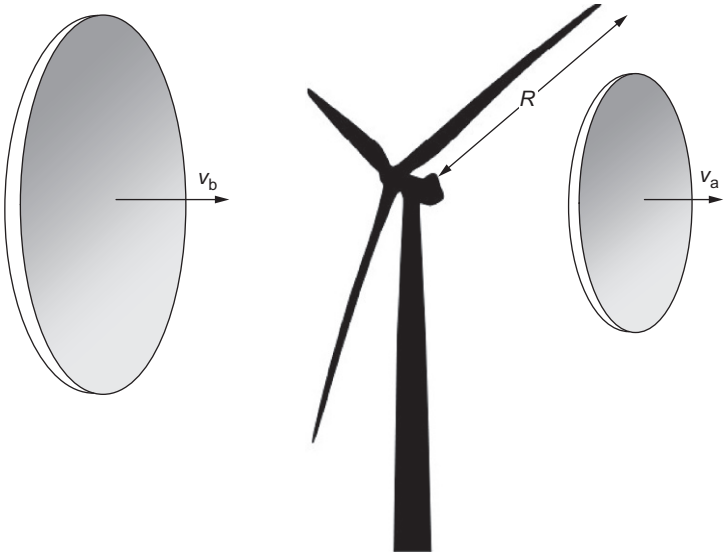


FIG. 23.22 Wind speed before and after turbine.

The relation of total amount of power P_{total} to the extracted power $P_{extracted}$ can be calculated as

$$\frac{P_{extract}}{P_{total}} = \frac{\frac{v_a + v_b}{2} \cdot \left(v_b^2 - v_a^2\right)}{v_b^3} = \frac{1}{2}\left(1 - \frac{v_a^2}{v_b^2}\right) \cdot \left(1 + \frac{v_a}{v_b}\right) \quad (23.12)$$

For the maximum power extraction, the ratio of the wind speed after and before the turbine can be calculated using $\frac{d(P_{extract}/P_{total})}{d(v_a/v_b)} = 0$.

Solving (23.12) for v_a/v_b yields

$$\frac{v_a}{v_b} = \frac{1}{3} \quad (23.13)$$

As a result, (23.12) reaches its maximum value for $\frac{v_a}{v_b} = \frac{1}{3}$.

$$\left.\frac{P_{extract}}{P_{total}}\right|_{\frac{v_a}{v_b} = \frac{1}{3}} \approx 59.3\% \quad (23.14)$$

Eq. (23.14) shows that the maximum extracted power from the wind is 59.3% of the total available power. In other words, it is not possible to extract all 100% of wind energy since the wind speed after turbine cannot be 0.

Betz's law indicates that the maximum theoretical extracted wind power is 59%. However, in practice, the real efficiency of wind turbine is slightly different.

23.3.4.2 Different Electrical Machines in Wind Turbines

There are many types of electric machines that are used in wind turbines. There is no clear criterion for choosing a particular machine to work as a wind generator. Based on the installed power, site of turbine, load type, and simplicity of control, the wind generator can be chosen. Squirrel-cage induction or brushless DC (BLDC) generators are usually used for small wind turbines in household applications. Doubly fed induction generators are usually used for megawatt size turbines. Synchronous machines and permanent-magnet synchronous machines (PMSM) can also be used for wind-turbine applications.

Brushless DC (BLDC) machines

Brushless DC machines (BLDC) are very popular in many applications due to the recent advances in their development. In addition, the development of fast semiconductor switches, cost-effective DSP processors, and other microcontrollers have influenced the development of the motor/generator drives. Brushless DC machines (BLDC) are widely used because of their simple control, efficiency, compactness, lightweight, ease of cooling, less noise, and low maintenance [134,135]. Usually, BLDC machines are used in small wind turbines (up to 15 kW).

The simplified equivalent circuit of the BLDC generator connected to a diode rectifier is shown in Fig. 23.23. This is the simplest way of using BLDC machine for wind applications, because there is no switch to control the phase current. The full bridge rectifies the induced voltages of variable frequency (because of variable wind speeds). Basically, the waveform of the induced electromotive force (EMF) is converted to dc voltage regardless of the input waveform. Usually, these types of wind turbines are connected to batteries; therefore, rectified electric power is used to charge the battery.

Three-phase active synchronous rectifiers can be used with BLDC generators. In this case, the controlled rectifier is used for BLDC phase current control. Usually, hysteresis regulators are used to control current. In synchronous rectifiers, active switching devices such as IGBTs or MOSFETs are used.

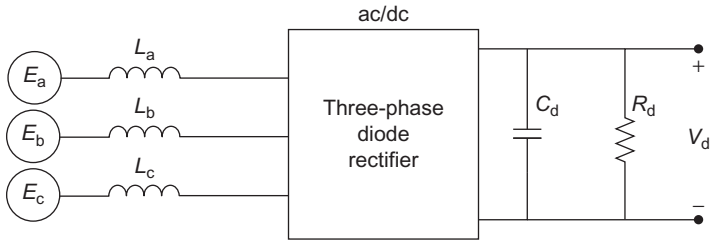


FIG. 23.23 Diode rectifier connected to BLDC generator.

By employing a PWM control strategy for the synchronous rectifier, MPP tracking of the wind turbine can be achieved. An inverter can be placed at the dc bus for grid interconnection or powering the ac loads.

Permanent magnet synchronous machines

For both fixed and variable speed applications, permanent-magnet (PM) synchronous machines can be used. The permanent-magnet synchronous generator (PMSG) is very efficient and suitable for wind-turbine applications. PM synchronous generators allow direct-drive energy conversion for wind applications. Direct-drive energy conversion helps eliminating the gearbox between the turbine and generator; thus, these systems are less expensive, and less maintenance is required [136,137]. However, lower speed determined by the turbine shaft is the operating speed for the generator.

A wind power system where a PM synchronous generator is connected to a full-bridge rectifier followed by a boost converter is shown in Fig. 23.24. In this case, the boost converter controls the electromagnetic torque. The supply side converter regulates the dc-link voltage and controls the input power factor. One drawback of this configuration is the use of diode rectifier that increases the current amplitude and losses. The grid-side converter can be used to control active and reactive power being supplied to the grid. Automatic voltage regulator (AVR) obtains the information of speed of turbine, dc-link voltage, current, and grid-side voltage and current. It calculates PWM pattern (control scheme) for converter. This configuration has been considered for small size (less than 50 kW) wind power systems (WPS) [138].

Instead of using a diode rectifier cascaded by a dc/dc converter, both rectifier and inverter can be controllable. A PMSG where the PWM rectifier is placed between the generator and the dc link, and PWM inverter is connected to the utility is shown in Fig. 23.25. In this case, the back-to-back converter can be used as the interface between the grid and the stator windings of the PMSG [139]. The turbine can be operated at its maximum efficiency, and the variable speed operation of PMSG can be controlled by using a power converter that is utilized to regulate the maximum power flow. The stator terminal voltage can be controlled in several ways [140]. In this system, utilizing the field orientation control (FOC) allows the generator to operate near its optimal working point in order to minimize the losses in the generator and power electronic circuit.

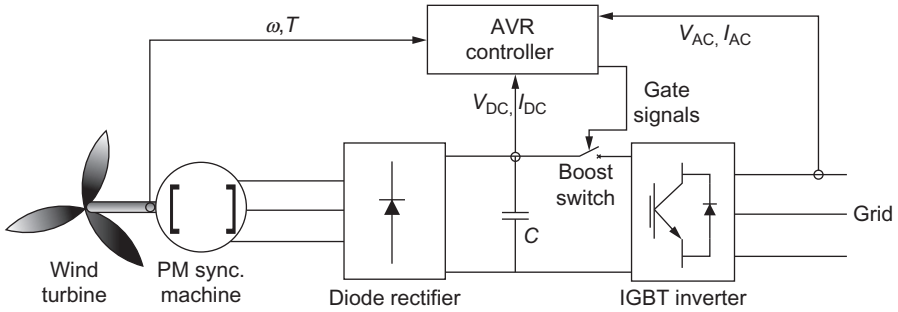


FIG. 23.24 PM synchronous generator with rectifier/inverter.

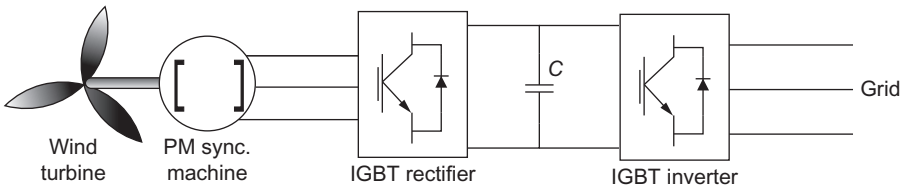


FIG. 23.25 PM synchronous generator with back-to-back inverter.

However, the performance depends on the knowledge of the generator parameter that varies with temperature and frequency. The main drawbacks are the cost of PMs that increases the price of the machine and demagnetization of the PMs. In addition, it is not possible to control the power factor of the machine [134].

Squirrel cage induction machines

The three-phase induction machines are commonly used in industrial motor applications. However, they can also be effectively used as generators in electric power systems. The main issue with induction machines as electric power generators is the need for an external reactive power source that will excite the induction machine, which is certainly not required for synchronous machines in similar applications. If induction machine is connected to the grid, the required reactive power can be provided by the power system. Induction machine may be used in cogeneration with other synchronous generators, or the excitation might be supplied from capacitor banks (only for stand-alone self-excited generator application) [141–146]. The reactive power required for excitation can be supplied using static VAr compensators [147,148] or static compensators (STATCOMs) [149].

Due to its low cost, brushless rotor construction does not need a separate source for excitation. No maintenance and self-protection against severe over loads, short circuits, and self-excited induction generators are used in wind-turbine applications [142–146]. The only drawback of these types of generators can be their inherent generated voltage and frequency regulation under varied loads [150].

Common structure of a squirrel-cage induction generator with back-to-back converters is shown in Fig. 23.26. In this structure, stator winding is connected to utility through a four-quadrant power converter. Two PWM VSI are connected back-to-back through a dc link. The stator-side converter regulates the electromagnetic torque and supplies reactive power, while the grid-side converter controls the real and reactive power delivered from the system to the utility and regulates the dc link. This topology has several practical advantages, and one of them is the possibility of fast transient response for speed variations. In addition, the inverter can operate as a VAR/harmonic compensator [151].

On the other hand, the main drawback is the complex control system. Usually, FOC is used to control this topology, where its performance relies on the generator parameters, which vary with temperature and frequency. Hence, in order to supply the magnetizing power requirements, that is, to magnetize the machine, the stator-side converter must be oversized 30%–50% with respect to rated power.

Doubly fed induction generator (DFIG)

Fig. 23.27 presents a topology consisting of a doubly fed induction generator (DFIG) with ac/dc and dc/ac converters, that is, a four-quadrant ac/ac converter using IGBTs connected to the rotor windings. In the DFIG topology, the induction generator is not a squirrel-cage machine, and the rotor windings are not short-circuited. Instead, they are used as the secondary terminals of the generator that provides the capability of controlling the machine power, torque, speed, and reactive power. To control the active and reactive power flow of the DFIG topology,

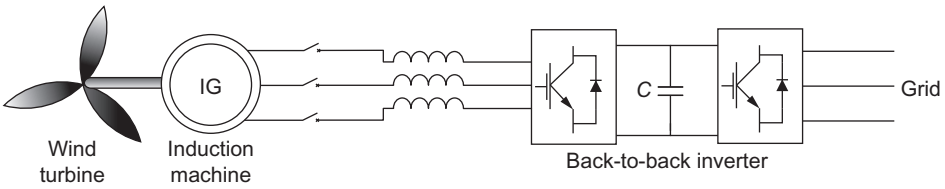


FIG. 23.26 Induction machine controlled by back-to-back inverter.

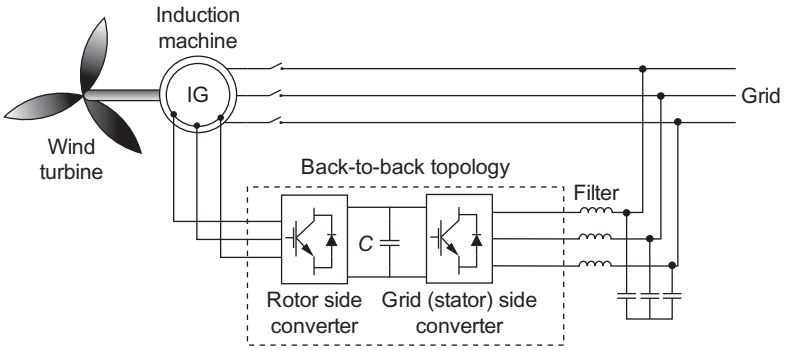


FIG. 23.27 Doubly fed induction machine topology.

rotor- and grid-side converters should be controlled separately [152–155].

Wounded rotor induction machines can be supplied from both rotor and stator sides. The speed and the torque of the wounded rotor induction machine can be controlled by regulating voltages from both rotor and stator sides of machine. The DFIG can be considered as a synchronous/asynchronous hybrid machine. In the DFIG, similar to the synchronous generator, the real power depends on the rotor voltage magnitude and angle. In addition, the induction machine slip is also a function of the real power [156]. DFIG topology offers several advantages in comparison with systems using direct-in-line converters [157,158]. These benefits are the following:

- The main power is transferred through the stator windings of the generator that is directly connected to the grid. Around 65%–75% of the total power is transmitted through stator windings. The remaining power is transmitted using the rotor windings, that is, through the converters, which is about 25% of the total power. Since the inverter rating is 25% of total system power, the inverter cost and size can considerably be reduced.
- While the generator losses are the same in both topologies (direct-in-line and DFIG), the inverter losses can be reduced from around 3% to 0.75%, because the inverter is supposed to only transfer 25% of the total power. Therefore, approximately 2%–3% efficiency improvement can be obtained.
- DFIG topology offers a decoupled control of generator active and reactive powers [159,160].
- Cost and size of the inverter and EMI filters can be reduced since the inverter size is reduced. In addition, the inverter harmonics are lowered because the inverter is not connected to the main stator windings.

In the rotor circuit, two voltage-fed PWM converters are connected back to back, while the stator windings are directly connected to the ac grid side as shown in Fig. 23.27. The direction and magnitude of power between the rotor windings and stator windings can be controlled by adjusting the switching of the PWM signals of the inverters [161–163]. This is very similar to connecting a controllable voltage source to the rotor circuit [164]. This can also be considered as a conventional induction generator without a zero rotor voltage.

To take the benefits of variable speed operation, the optimum operating point of the torque-speed curve should be tracked precisely [165]. By controlling the torque of the machine, speed can be adjusted. Thus, using the instantaneous rotor speed value and by controlling the rotor current i_{ry} in stator-flux-oriented reference frame, the desired active power can be obtained. Operation at the desired active power results in the desired speed and torque [153]. On the other hand, the grid-side converter is controlled to keep the fixed dc-link voltage independent of the direction of rotor power flow. By using supply voltage vector-oriented control, the decoupled control of active and reactive power flow between rotor and grid can be obtained.

Using doubly fed induction generator, the oversizing problem can be solved. Still, speed range of turbine is wide enough; thus, a power converter, which is rated for much lower powers, can be placed in rotor side only, and stator is connected to grid directly. Since power flowing through rotor is usually around 25%–30% of power going through stator, the power electronic interface is designed for only 25%–30% of total power. This is the most important advantage of DFIG.

Synchronous generators

Synchronous generators are commonly used for variable speed wind-turbine applications, due to their low rotational synchronous speeds that produce the voltage at grid frequency. Synchronous generators can be an appropriate selection for variable speed operation of wind turbines [166,167]. They do not need a pitch control mechanism. The pitch control mechanism increases the cost of the turbine and causes stress on turbine and generator [168]. Synchronous generators in variable speed operation will generate variable voltage and variable frequency power. Using an AVR for the excitation of the field voltage, the output voltage of the synchronous generator can be controlled. However, induction generators require controlled capacitors for voltage control. In addition, their operating speed should be over synchronous speed in order to operate in generating mode [169].

Multipole synchronous generators can be used more efficiently since the gear can be eliminated, and direct drive of the turbine and generator can be achieved [170,171]. However, synchronous generators without multipoles require gearboxes in order to produce the required frequency for grid connection. On the other hand, a dc voltage source or an ac/dc converter is required for synchronous generators in wind applications in order to produce the required excitation voltage for the field windings. The synchronous generator connection with wind turbine is shown in Fig. 23.28.

23.3.4.3 Energy Storage Applications for Wind Turbines

The batteries and other dc energy storage devices can be connected to the dc links of any topologies. The main purpose of batteries is to assist the generator to meet the load demand. When the load current is smaller than generator current, the extra current is used to charge the battery energy storage. On the other hand, when the load current is larger than generator current, the current is supplied from the battery to the load. With this strategy, the voltage and frequency of the generator can be controlled for various load conditions. Energy storage decreases system inertia, improves the behavior of the system in the case of disturbances, compensates transients, and therefore improves the efficiency [172]. However, it brings an initial cost to the system and requires periodical maintenance depending on the storage devices. Therefore, the voltage and frequency control can be modified by using batteries as the controllable load of the VSI as presented in Fig. 23.29. In this way, the load can be regulated by controlling the power flow to the batteries. A bidirectional inverter/converter can be used for

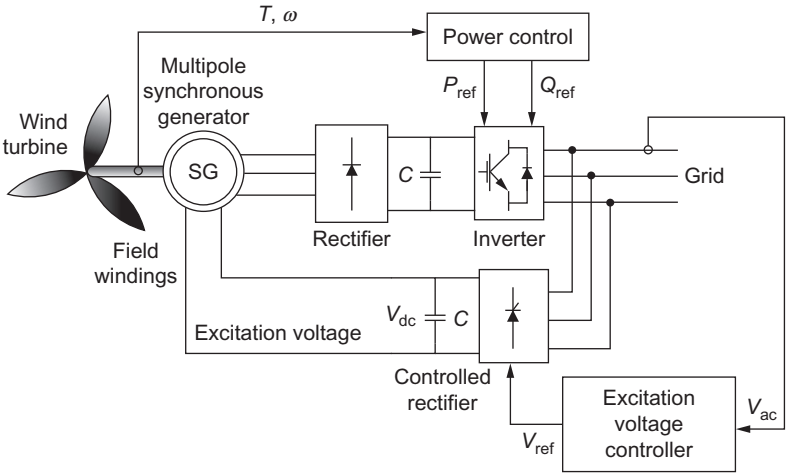


FIG. 23.28 Multipole synchronous generator for wind-turbine applications.

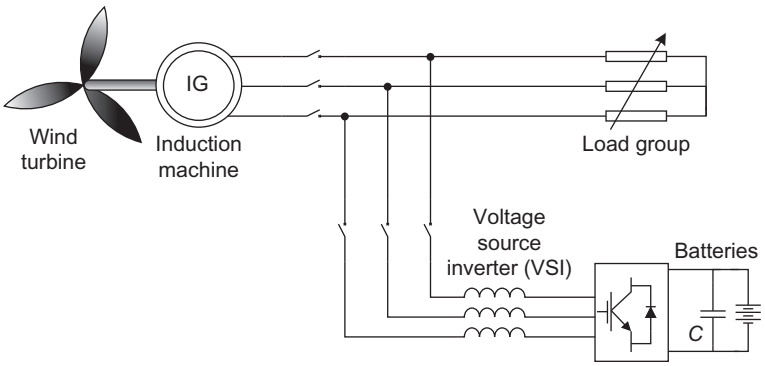


FIG. 23.29 Voltage and frequency control using energy storage.

power flow from/to the batteries. As another alternative, the battery voltage can be converted to ac voltage with another individual inverter to provide power to AC loads. Although an induction generator is shown in Fig. 23.29, these energy storage systems are applicable to any other topologies.

Storage systems can be connected in various forms to the wind-turbine systems [173–177]. Generally, a bidirectional dc/dc converter is required for the integration of the storage system to the doubly fed induction generator system [178]. In this topology, one of the converters regulates the storage power, whereas the other is responsible for dc bus voltage control. The bidirectional energy storage topology for DFIGs in wind applications is shown in Fig. 23.30.

23.3.5 Ocean Energy Harvesting

23.3.5.1 Ocean Wave Energy

Ocean waves are a plentiful, clean, and renewable source of energy. The total power of waves breaking around the world's coastlines is estimated at 2–3 million megawatts. The west coasts of the United States and Europe and the coasts of Japan and New Zealand are good sites for harnessing wave energy [179]. Wave energy conversion is one of the feasible future energy technologies; however, it is not mature enough. Therefore, the construction cost of wave power plants is considerably high. These energy systems are not developed and maturated commercially due to the problems of dealing with sea conditions, complexity, and difficulty of interconnection and transmission of electricity.

A wave power absorber, a turbine, a generator, and the power electronic interfaces are the main components of a typical ocean wave energy harvesting technique. The kinetic energy of the ocean waves are captured by absorbers. Either the absorbed kinetic energy of the waves is conveyed to turbines or the absorber directly drives the generator. The shaft of the electric generator is driven by the turbine. Turbines are generally used within the systems including rotational generators. Linear motion generators are used in systems without turbines, which can be direct driven by the power absorber or movement of the device. Due to the varying amplitude and period of the ocean waves, both linear and rotational generators generate variable frequency—variable amplitude ac voltage. This ac voltage can be rectified to dc voltage to take the benefit of dc energy transmission through the salty ocean water. dc transmission in salty water does not require an additional cable for the negative polarity. Thus, it will be more cost-effective than transmitting

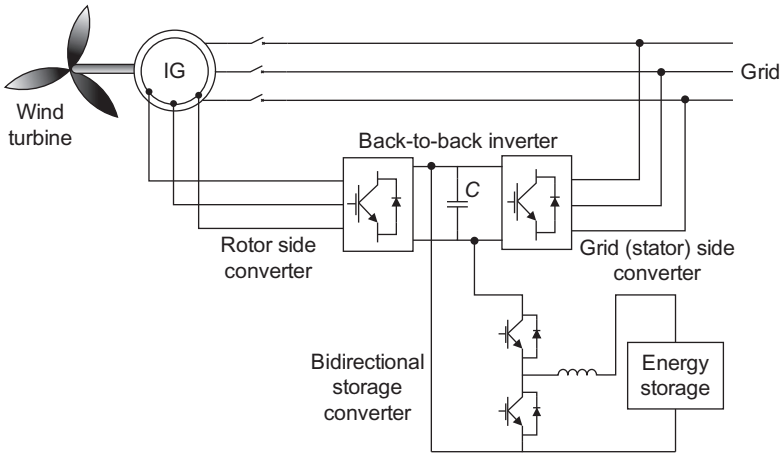


FIG. 23.30 Energy storage with bidirectional converter in DFIG systems.

the power in ac form, which requires three-phase cables. Transmission cable length varies depending on the location of the application, which is either nearshore or offshore. However, the main idea and the principles are the same for both types of applications. After the dc power is transmitted from ocean to the land, a dc/dc converter or a tap-changing transformer can be used for voltage regulation. Depending on the utilized voltage regulation system, a dc/ac inverter is used before or after the voltage regulator. The voltage synchronization is provided by the inverter, and the output terminals of the inverter can be connected to the grid.

In Fig. 23.31, a system level diagram of the ocean wave energy harvesting technology is shown. At an in-water substation, wave energy conversion devices (including the absorber, turbine, and generator) are interconnected. The substation consists of the connection equipments and controllers for individual devices. The outputs of the generators are connected to a common dc bus using dc/ac converters for transforming power before transmission to the shore. A transmission line connects the cluster to shore. An onshore inverter converts the dc voltage to a 50 or 60 Hz ac voltage for grid connection. An optional shore transformer with tap changer or a dc/dc converter compensates the voltage variations. A group of absorber, turbine, and generators could be used in a farm structure; thus, the captured energy can be increased.

Alternatively, the land converters might be moved offshore to come up with space limitations that may occur in land stations. This brings some complexity to the system and may require more maintenance, which is harder to deal, in comparison with landside converters. Moreover, the transformer can be installed offshore. This would increase the power transmission capability, since the higher voltage transmission will result in less transmission losses. However, in this case, the advantage of dc transmission will not exist. As a different option, boost dc/dc converters can be used after the ac/dc converter of the generator. This allows a high-voltage dc transmission link. In this case, both transmission losses will be kept at minimum, and only single-line dc transmission through the ocean water will be required.

Energy of ocean waves

The total potential and kinetic energy of an ocean wave can be expressed as

$$E = \frac{1}{2}\rho g A^2 \tag{23.15}$$

where g is the acceleration of gravity (9.8 m/s^2), ρ is the density of water (1000 kg/m^3), and A is the wave amplitude (m).

The power of a wave in a period is equal to the energy E multiplied by the speed of wave propagation, v_g, for deep water

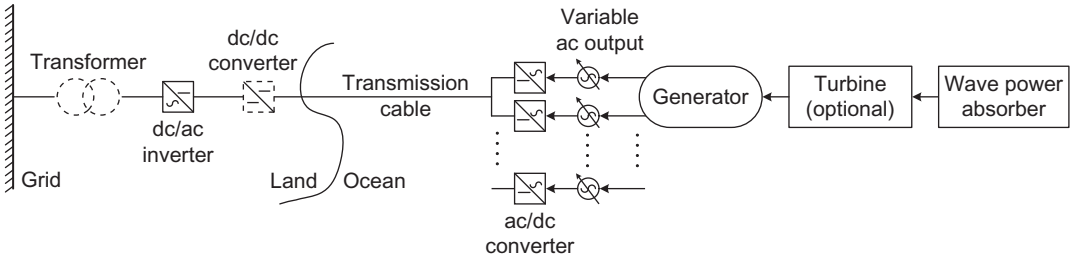


FIG. 23.31 System level diagram of ocean wave energy harvesting.

$$v_g = \frac{L}{2T} \tag{23.16}$$

where T is the wave period (seconds) and L is the wave length (m) [180].

$$P_w = \frac{1}{2}\rho g A^2 \frac{L}{2T} \tag{23.17}$$

The dispersion relationship describes the connection between the wave period T and the wave length L as

$$L = \frac{gT^2}{2\pi}. \tag{23.18}$$

If (23.18) is substituted in (23.17), the power or energy flux of an ocean wave can be calculated as

$$P_w = \frac{\rho g^2 T A^2}{8\pi}. \tag{23.19}$$

Instead of using the wave amplitude, wave power can also be rewritten as a function of wave height, H [m]. Considering that the wave amplitude is the half of the wave height, the wave power becomes

$$P_w = \frac{\rho g^2 T H^2}{32\pi}. \tag{23.20}$$

Ocean wave energy harvesting technologies

In general, ocean wave energy harvesting technologies can be classified into two types with respect to their distance from the shore: offshore ocean wave energy harvesting technologies and onshore ocean wave energy harvesting technologies. These are discussed in details in following subsections.

Off-shore ocean wave energy harvesting technologies: Off-shore applications are located away from the shore, and they generally use a floating body as wave power absorber and another body that is fixed to the ocean bottom. Generally, linear generators with buoys are used in offshore applications. Linear generators are directly driven by the movement of a floating body on the ocean. Salter cam and buoys with air-driven turbines are the only applications involving rotational generators in offshore applications.

23.3.5.1.2.1.1 Air-Driven Turbines based Off-Shore Technologies

In air-driven turbine systems for offshore applications, the primary conversion is from wave to the pressurized air. Secondary conversion stage is the conversion to mechanical energy by rotating shaft of the turbine. The last stage is converting mechanical rotation into electric power by electric generators.

The operating principle of an offshore application that consists of a floating buoy with an air chamber and an air-driven generator is shown in Fig. 23.32. In this system, the water level inside channel of the buoy increases when the waves hit the body. This increase in water level applies a pressure to the air in the air chamber. When the air is pressurized, it applies a force to the ventilator turbine and rotates it. This turbine drives the electric generator, and electricity is generated at the output terminals of this generator. When the waves are pulled back to the ocean, the air in the air chamber is also pulled back since the water level in the buoy channel decreases. Due to the syringe effect, this time, turbine shaft rotates in the contrary direction but produces electricity. There should be very good mechanical insulation through the air chamber and the ventilating generator to achieve higher efficiencies. However, this brings design complexity and additional cost to the system.

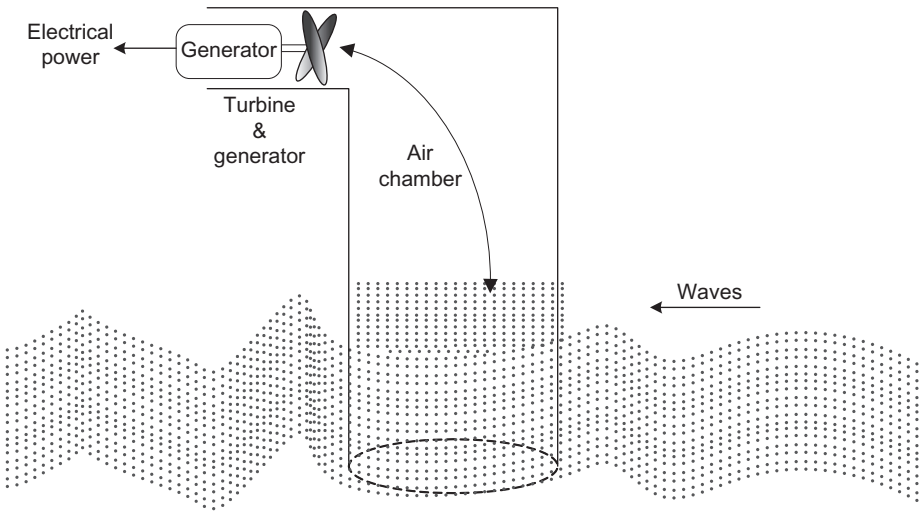


FIG. 23.32 Spinning the air-driven turbines using wave power [181].

In another method, water level increases, and air is taken out from the upper outlets while spinning the turbines as shown in Fig. 23.33A. Contrarily, when the waves are pulled back to the sea, water level decreases. This results in sucking the air back from the upper inlets while spinning the turbines, as shown in Fig. 23.33B.

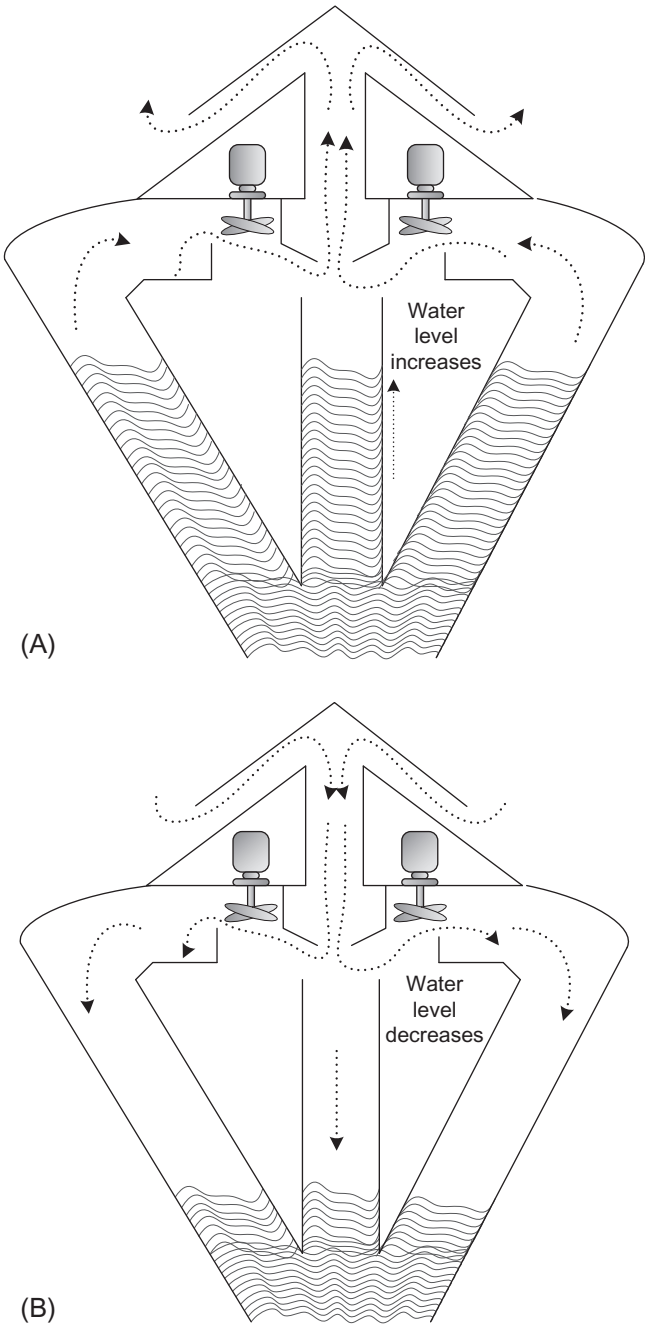


FIG. 23.33 Air-pressure ring buoy: (A) water level increases, and air is taken out from the upper outlets; (B) Water level decreases, and air is pulled back from upper inlets.

23.3.5.1.2.1.2 Direct-drive permanent-magnet linear generator-based buoy applications

The height differences of the wave top and bottom levels yield an up and down motion for the piston that is the transaxle of the linear generator. When the wave is floating on the ocean surface, the buoy follows the motion of the wave. Buoy can move vertically on a pillar, which is connected to a hull. On the surface of the hull, PMs are mounted, while outside of the hull contains the coil windings. The pillar and stator are connected together on a concentrate foundation standing on the seabed of the ocean. The hull and mounted magnets, called rotor or piston, are the moving parts of the generator. Since the motion is linear, this generator is called a linear generator.

In Fig. 23.34, the linear generator in the floating buoy and fixed pillar are shown.

When the wave rises, the buoy will drive the generator piston through a stiff rope. When the wave subsides, the generator will be driven by the spring that stores the mechanical energy in the first case. Thus, electric generation is provided during both up and down motion. Due to the existence of variable frequency in the current and voltage from the stator, an ac/dc rectifier followed by a dc/ac converter is required to make the grid connection possible. Instead of placing moving parts to the ocean bottom, the PMs and the stator windings can be placed at the sea level [182]. Fig. 23.35 shows the x-y plane of the cross-sectional view of one pole of the longitudinal flux surface mounted linear PM generator.

23.3.5.1.2.1.3 Salter Cam Method

Salter cam method implementation is shown in Fig. 23.36. Salter cam rolls around a fixed inner cylinder by activation of an incoming wave. Through the differential rotation between the cylinder and the cam, power can be captured. The motion of the cam is converted from wave to a hydraulic fluid. Then, hydraulic motor is used to convert the pressurized hydraulic fluid to rotational mechanical energy. Finally, rotational mechanical energy is converted to electricity by utilizing electric generators. Flywheels or pressurized liquids can be used as an intermediate step in order to reduce the intermittencies of the wave power.

Near-shore ocean wave energy harvesting technologies: Nearshore topologies are applied within the surfing zone of the ocean or right on the shore. Nearshore applications have some advantages and disadvantages in comparison with the offshore applications.

23.3.5.1.2.2.1 Channel/reservoir/turbine based near-shore wave energy harvesting method

Wave currents can be tapered into a narrow channel to increase their power and size in order to harness the wave energy. As shown in Fig. 23.37, waves can be channeled into a catch basin and used directly to rotate the turbines. Since this method

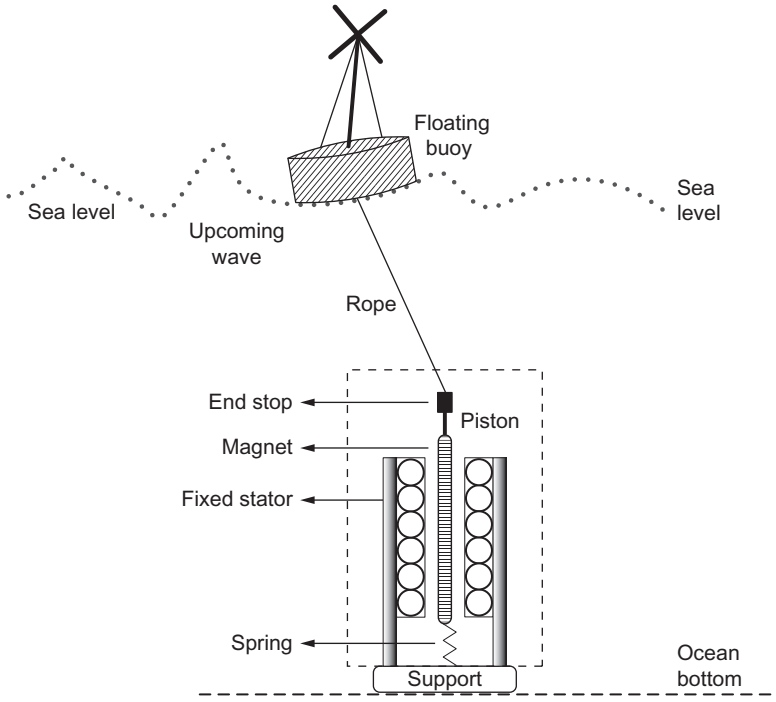


FIG. 23.34 Linear generator-based buoy type wave energy harvesting method.

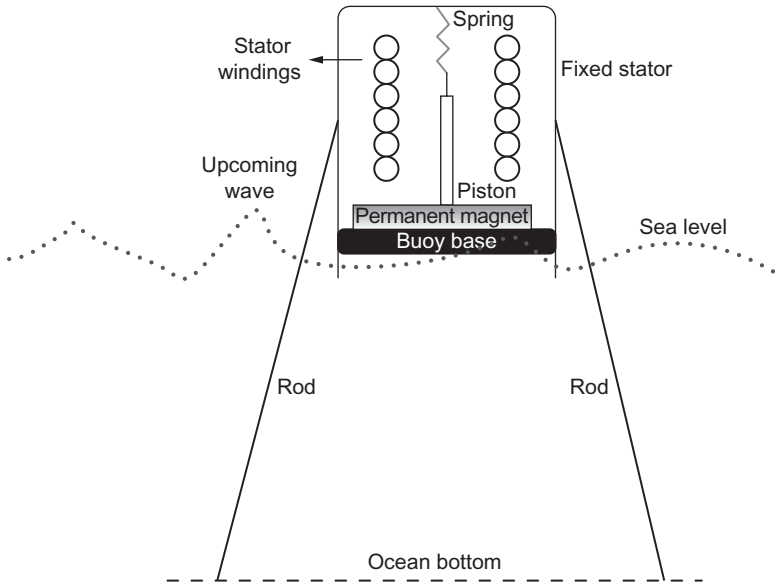


FIG. 23.35 Schematic of a longitudinal flux permanent-magnet generator used for wave energy conversion.

requires building a reservoir to collect the water coming with the waves to drive the turbine, it is more expensive in comparison with the other buoy-shaped offshore applications. However, it requires less maintenance in comparison with the offshore applications, since all components of the wave energy conversion system are located on land. Additionally, since a reservoir collects the ocean water, the intermittencies can be eliminated. This will create a convenient platform for voltage and frequency regulation. Building these types of plants in the locations, where they have regular and sustaining wave regimes, is more advantageous.

23.3.5.1.2.2.2 Air-driven turbines based near-shore wave energy harvesting method

Using oscillating water columns (OWC) that generates electricity from the wave-driven rise and fall of water in a cylindrical

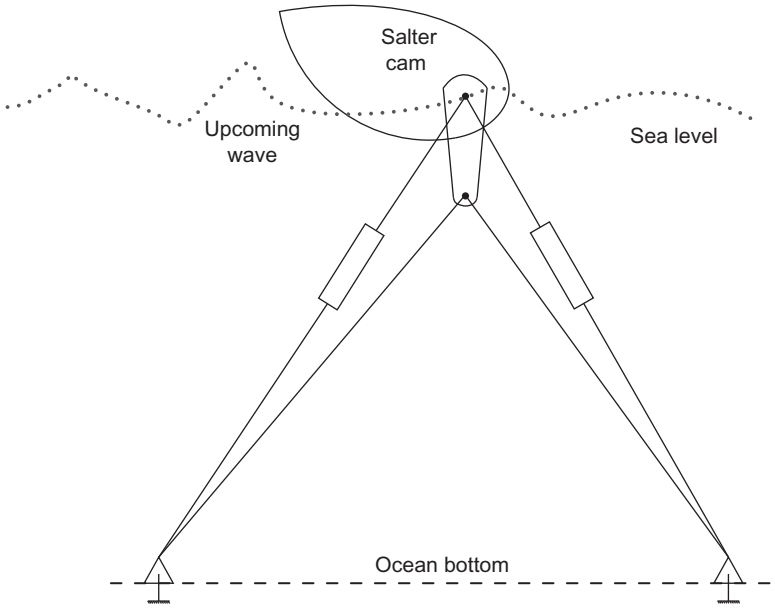


FIG. 23.36 A schematic illustrating the fixation of salter cam wave energy conversion device.

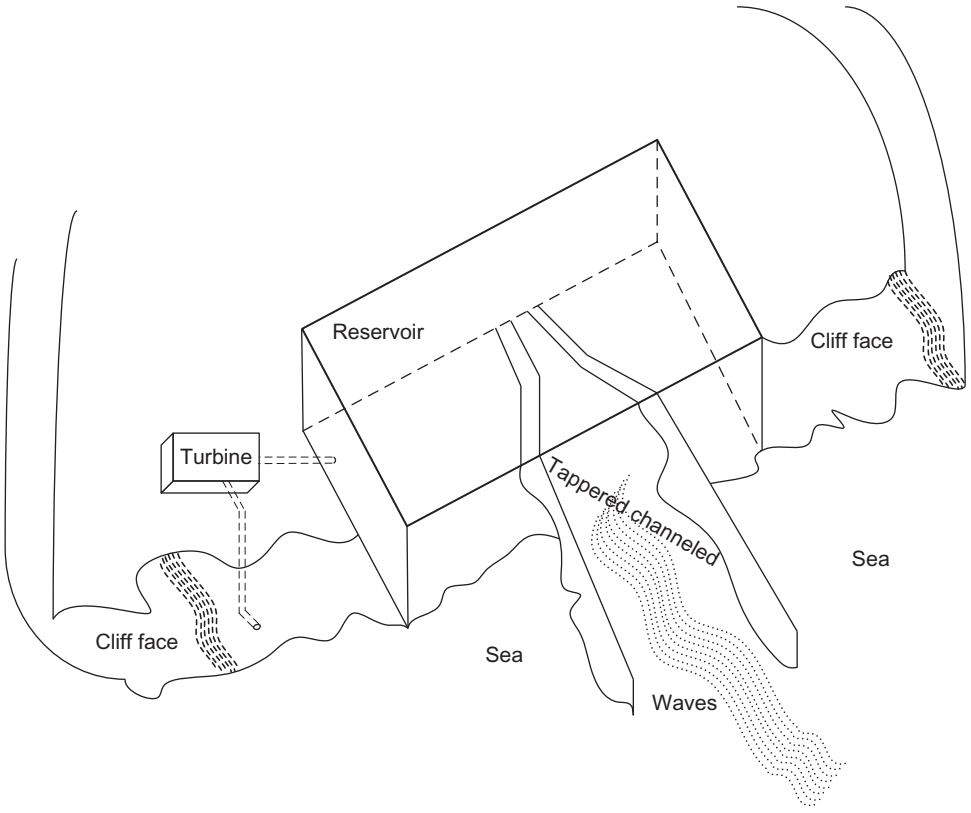


FIG. 23.37 Channeled ocean wave to a reservoir to spin the turbines.

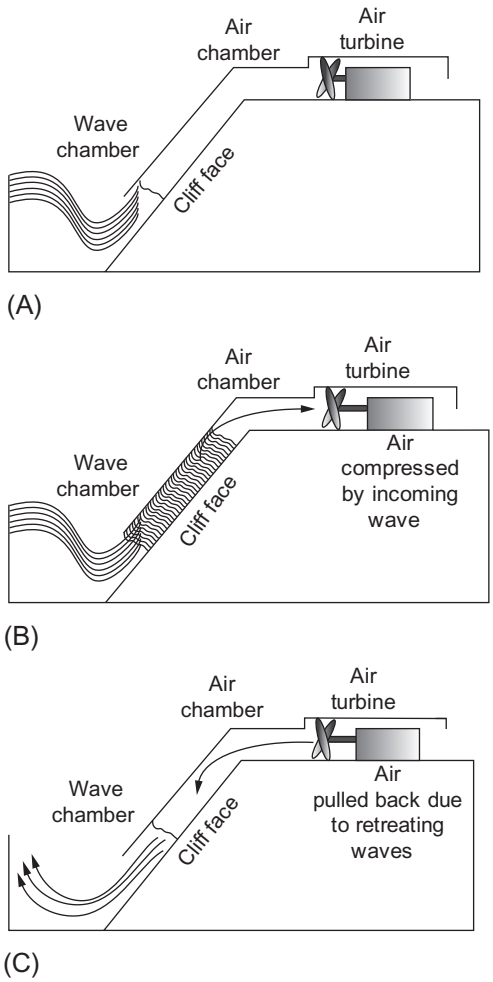


FIG. 23.38 Air-driven turbines using the wave power: (A) upcoming wave starts filling the chamber; (B) air is compressed by rising water; (C) air is pulled back by retreating waves [181].

shaft or pipe is another way to harness the wave energy. The air is driven into and out of the top of the shaft due to the rising and falling water, powering an air-driven turbine that is shown in Fig. 23.38.

The general structure of the nearshore air-driven turbine is shown in Fig. 23.38A. Waves push the air through the ventilator that drives the electric machine as shown in Fig. 23.38B. The wave retreats from the wave chamber inside the channel that decreases the pressure as shown in Fig. 23.38C. This method is advantageous because of the capability of using not only the wave power but also the power from the tidal motions. However, mechanical isolation should be provided within the wave and air chambers in order to obtain better efficiencies. This will also bring some more cost and design complexities to the system.

23.3.5.2 Ocean Tidal Energy

The generation of electric power from ocean tides is similar to the traditional hydroelectric generation. A dam, known as a barrage, across an inlet is required for the simplest tidal power plants. In a tidal power plant, usually, a tidal pond created by a dam and a powerhouse, which contains a turbo generator, and a sluice gate to allow the bidirectional tidal flow. During the flood tide, the rising tidal waters fill the tidal basin after opening the gate of the dam. When the dam is filled to capacity, the gates are closed. The tidal basin is released through a turbogenerator after the ocean waters have receded. Power can be generated during ebb tide, flood tide, or both. When the water is pulled back, ebb tide occurs, and when the water level increases near the shore, flood tide happens [183]. Tidal power can be economical at sites where mean tidal range exceeds 16 ft [183,184].

Tidal current is not affected by the climate change, the lack of rain, or a snowmelt. Therefore, tidal energy harvesting is practical since the tidal current is regular and predictable. Moreover, environmental and physical impacts and pollution issues are negligible. Tidal power can additionally be used for water electrolysis for hydrogen production applications and desalination. However, tidal power generation is an immature technology, which needs further investigations and developments.

Tidal turbines can be used for tidal energy harvesting, similar to the wind turbines. Tidal turbines can be located where there is a strong tidal flow. These turbines have to be much stronger than wind turbines since the water is about 800 times as dense as air. They will be heavier and more expensive; however, they will be able to capture more energy at much higher densities [181]. In Fig. 23.39, a typical tidal turbine is shown.

Usually, tidal fences having multiple turbines are mounted in the entrance of channels that are affected by ocean tides. Tidal water is forced to pass through a fence structure, which is called caisson in this fence application. Unlike barrage stations, basins are not required for fence applications, and they can be used in a channel between the mainland and a nearby offshore island or between two islands. Tidal fences can be mounted at the entrance of channels that ocean water gets inside the land via a bay (Fig. 23.40A), or between the main land and an island (Fig. 23.40B), or simply between two islands (as shown in Fig. 23.40C). Since they do not require flooding the basin, tidal

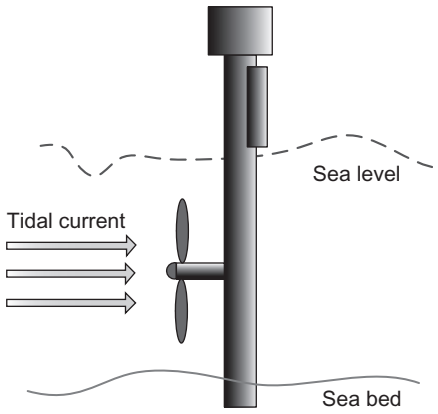


FIG. 23.39 Tidal turbine.

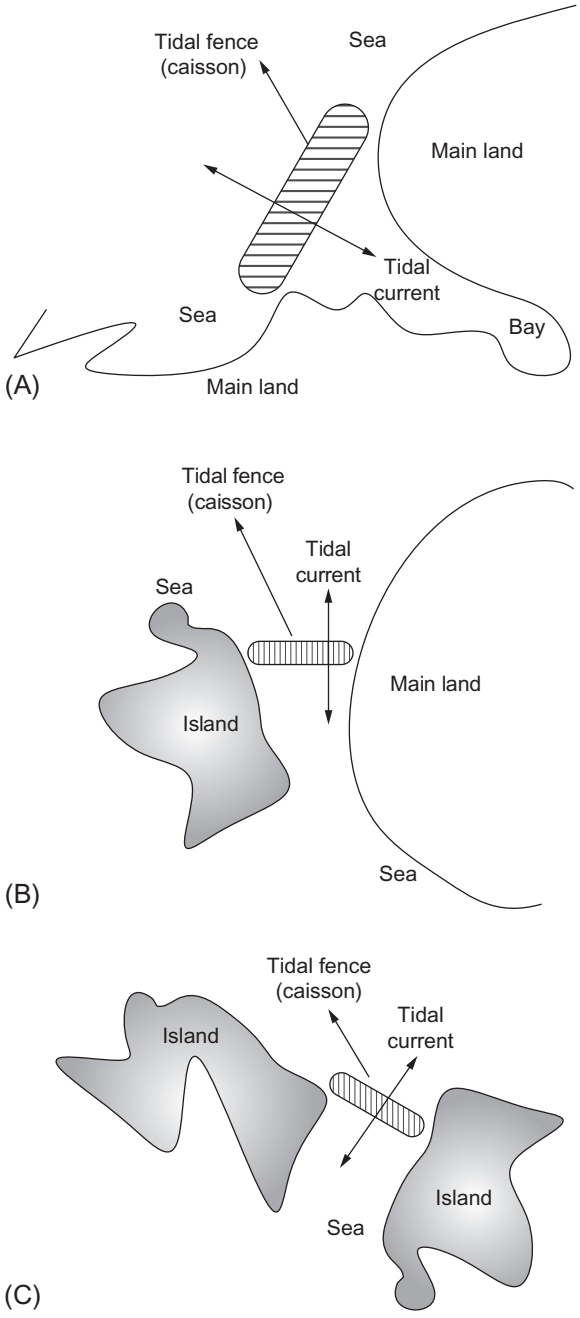


FIG. 23.40 Tidal fences can be mounted (A) at the entrance of bays, (B) between the main land and an island, and (C) between two islands.

fences have much less impact on the environment. In addition, they are significantly cheaper to install; however, the caisson may disrupt the movement of large marine animals and shipping [T4].

23.3.5.3 Power Electronic Interfaces for Ocean Energy Harvesting Applications

Both in ocean wave and ocean tidal energy harvesting applications, the generators may produce alternating currents and voltages that have varying magnitude and frequency. Therefore, output power of the ocean energy converters need further conditioning prior to the grid connection. In addition, the frequency of the output voltage should be regulated to be the same as grid frequency. Output power conditioning, amplitude, phase, and frequency of the conversion system can be regulated by utilizing power electronic converters.

Block diagram of a typical power conditioning system for a grid-connected ocean energy conversion system is shown in Fig. 23.41. Ocean wave or ocean tide potential and kinetic energies rotate the water turbine, or a power absorber directly drives a linear generator with up and down motions. The varying wave and tides result in variable frequency and amplitude of the generator output. The ac power produced by the generator is converted into dc power via three-phase bridge rectifiers followed by a dc/ac inverter. The output of the dc/ac inverter generally contains harmonics, which should be filtered. Finally, output power can be connected to grid and transmitted to consumers after its voltage is increased and isolated by a power transformer.

During the intermittencies, power cannot be generated. Therefore, an energy storage system should be connected to the generator output or output of a conversion stage in the power conditioning system. Stored energy can be supplied to the grid during the intermittency periods. Hence, it is ensured that continual power is supplied to the grid.

23.3.6 Geothermal Energy Systems

Geothermal energy is the thermal energy that is stored in the inner layers of the Earth composed of rocks and fluids. The temperature of the inner layers of the Earth gets hotter as the depth increases. In deeper layers, it is even extremely hotter due to the hot molten rock called magma [185,186].

Geothermal energy can be utilized by several methods. It can be used as direct heat for electric power generation. In the direct heat utilization, applications can be categorized as hydrothermal, agricultural, or industrial [187]. Hydrothermal resources have low to moderate temperatures between 20 and 150°C. These resources can be utilized to provide direct heating for residential, industrial, and commercial sectors [188]. These applications include but are not limited to water and space heating, greenhouse and agricultural heating, cleaning, textile processes, and food dehydration. Agricultural production is one of the utilization methods of direct use of geothermal energy. It is used to warm the greenhouses in order to provide cultivation. Industrial utilization examples can be food and cloth processing, manufacturing paper, pasteurizing milk, drying fish, vegetables and fruits, and even for refrigeration and air conditioning.

Other than the direct use of geothermal energy, it can be used as the heat and steam source for electric power plants. Instead of burning fossil fuels and generating heat for water boiling, geothermal power plants use the readily obtained heat or steam.

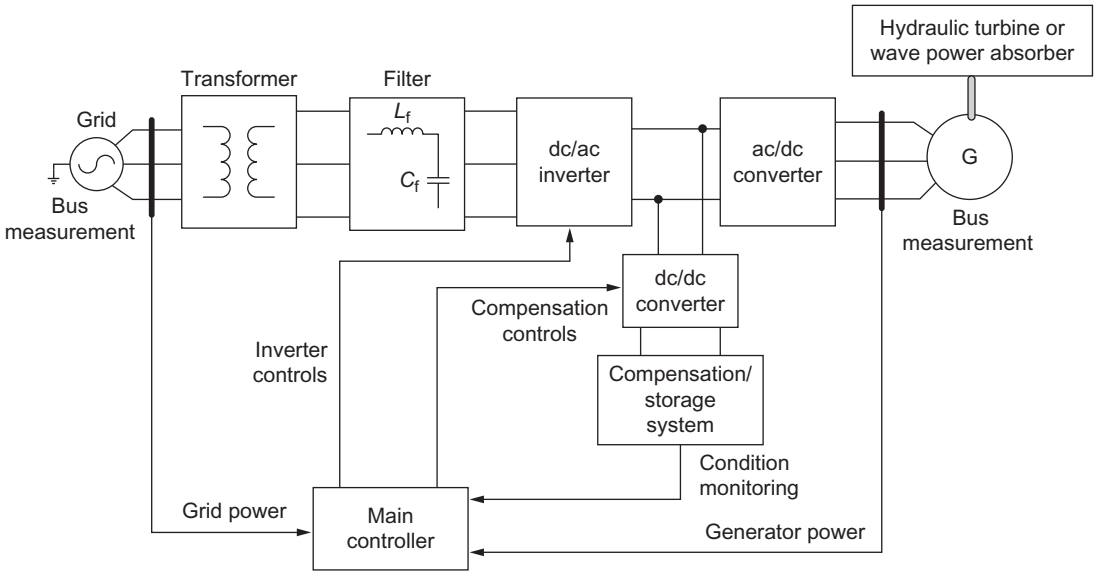


FIG. 23.41 Grid connection and controls of tidal current power conditioning system.

Natural hot water and/or steam from the inner layers of the Earth are used to drive the turbines and generators to produce electricity. Absolutely, no fuel firing is required for heating or steam generation for geothermal power plants. Therefore, geothermal power plants do not have emissions, and they are environmentally clean. Moreover, since the extracted heat is replaced by the thermal energy of the Earth's inner layers, geothermal energy is sustainable and renewable.

Schematic of a geothermal power plant is presented in Fig. 23.42.

The components of the geothermal power plant are described in Table 23.6.

The operating principle of a geothermal power plant is very similar to that of a coal-fired power plant. However, in geothermal power plants, hot steam and/or water is obtained from the deeper Earth layers instead of burning any fuel. Production well is used to draw hot water and/or steam from deeper layers. This mixture is separated by the separator in order to get the dry steam. Through a steam governor, a steam turbine is rotated by this high-pressure and high-temperature steam. Since the steam turbine is coupled to an electric generator, the mechanical steam power is converted into electric power. The output voltage of the generator is increased by a power transformer. The high voltage output of the power transformer can then be connected to the high-voltage transmission network. The steam loses its temperature and pressure after it goes through the steam turbine. Thus, the output flow of the steam turbine is condensed in the condensers. Condensed water is cooled down through the cooling tower, and cool water helps to condense the low-pressure/low-temperature steam in the condenser. The cooled water is then injected back to the inner Earth layers to get hot again. If the geothermal field is rich of hot water reservoirs, this cooled but still relatively warm water can be used for other heating purposes.

Geothermal energy is an abundant, secure, reliable, and renewable source of energy. It has high availability and capacity factor in comparison with other renewables. It is not a source of pollution for the environment; that is, their CO_2 emissions are less than 0.2% of the cleanest fossil-fuel-fired power plant, SO_2 emissions are less than 1%, and particulate emissions are less than 0.1%. It has an inherent energy storage capability and requires very small land area for establishment [186].

Geothermal power plants can be classified into three main generation technologies: dry-steam power plant, flash-steam power plant, and binary-cycle power plant.

Dry-steam power plants are the most common geothermal power plants since they are simple and cost-effective. These power plants are applicable to the geothermal fields where the geothermal steam is not mixed with water. In this method, production wells are drilled down to the aquifer to get superheated and pressurized steam. This steam is brought to the surface at high speeds. When the expanding steam passes through the turbine, the generator generates electricity [189,190]. The low-pressure steam output from the turbine is ventilated to the atmosphere in simple power plants. However, exhaust steam from the turbine is condensed in more complex power plants. The condensate can be reinjected to the reservoir by the injection wells, and/or it can be used as makeup cooling water.

Flash-steam power plants use a flash-steam technology where the hydrothermal source is in liquid form. This fluid is sprayed into a flash tank that is at a much lower pressure than the fluid. Therefore, the fluid immediately vaporizes rapidly into steam [189,191]. This generated steam is used to rotate the steam

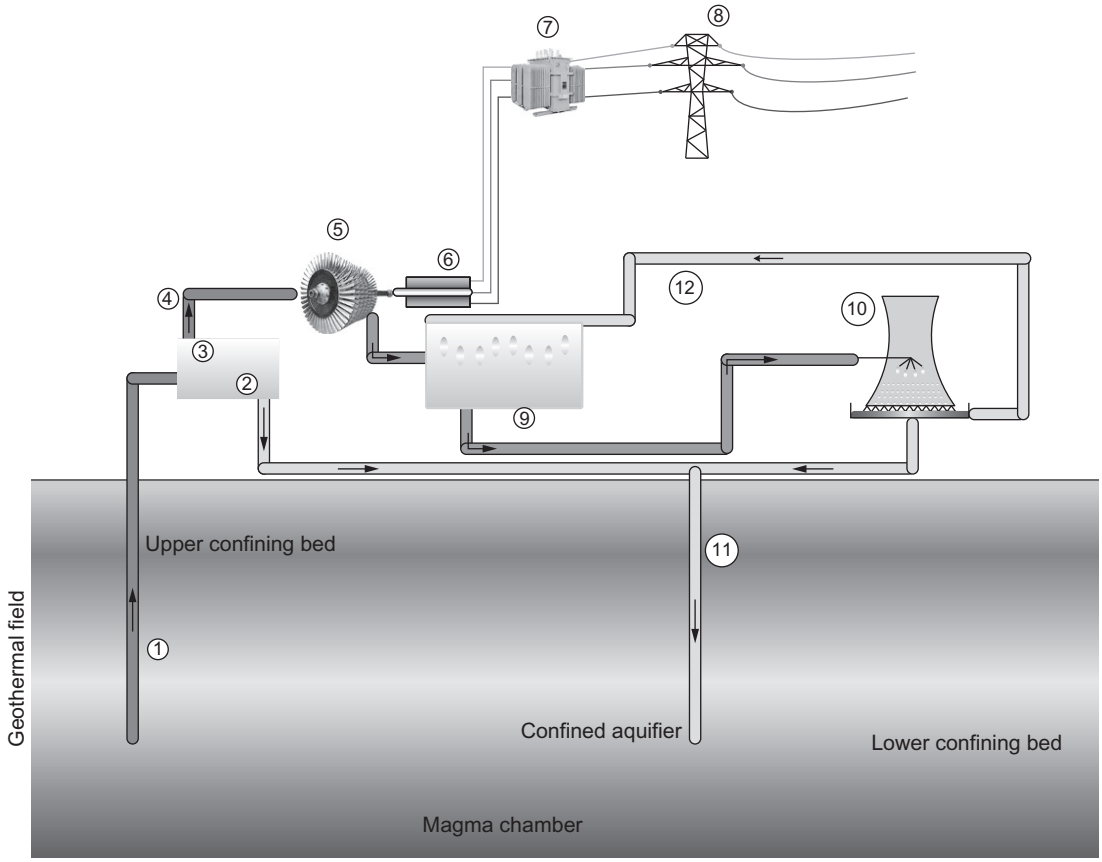


FIG. 23.42 A geothermal power plant.

TABLE 23.6 Geothermal power plant components

1—Production well	7—Power transformer
2—Water-steam mix	8—High-voltage transmission lines
3—Separator	9—Condenser
4—Steam	10—Cooling tower
5—Steam turbine	11—Injection well
6—Generator	12—Water flow cycle

turbines that are coupled to electric generators. The production well is kept under high pressure in order to prevent the geothermal fluid flashing inside the well [186]. Instead of using a single flashing system, dual-flashing systems are also used. The brine from the high-pressure steam is piped into a low-pressure separator/flash tank where the pressure is additionally reduced to generate lower-pressure steam in the dual-flash systems. In order to generate additional electric power, this lower-pressure steam is piped into a lower-pressure stage of the turbine. The steam exhaust from the high and low pressure turbines is condensed. Just like the dry-steam plants, the condensate is then used as makeup cooling water or reinjected to the reservoir.

Although the dual-flash power plants have higher capital cost, they have higher thermoelectric efficiency. Resource characteristics, power plant output, thermodynamic and economic factors, and equipment availability are the factors affecting the decision to build and operate a single-flash or dual-flash geothermal power plants [192]. Generally, dual-flash system is preferred if the fluid temperature is between 175 and 260°C, while single-flash systems are efficient enough for the fluid temperatures higher than 260°C.

Binary-cycle power plants are preferred when the geothermal resource is insufficiently hot to produce steam. Sometimes, the resource may have other chemical components causing impurities, and flashing may not become possible [186,193]. In these cases, binary-cycle power plants are preferred. In binary-cycle geothermal power plants, isobutene, isopentane, or pentane is used as the secondary fluid that has a lower boiling point than water. Since a separate working fluid is used, the cycle is called "binary." The geothermal fluid (water) is passed through a heat exchanger in order to heat up the secondary fluid. Secondary fluid vaporizes and expands through the turbines that are coupled to electric generators. After passing through the turbines, the working fluid is condensed and recycled for the next cycle. Moreover, the fluid remaining in the tank of flash-steam plants can be reutilized in binary-cycle plants. In a closed-cycle system, all of the geothermal fluid is injected back to the ground. Usually, binary-cycle plants are more efficient than the flash-steam plants in low to moderate temperatures of

geothermal fluids. Furthermore, corrosion problems are avoided since a pure working fluid is used.

23.3.7 Nuclear Power Plants

In nuclear power plants, energy is extracted from atomic nuclei by the controlled nuclear reactions. There are several available methods such as nuclear fission, nuclear fusion, and radioactive decay. The most common method is the nuclear fission. Similar to the conventional fossil-fuel-fired power plants, nuclear reactors generate heat in order to produce steam. However, unlike many conventional thermal power plants, nuclear power plants convert the energy released from the atoms' nucleus generally via nuclear fission, instead of burning fossil fuels. This energy is used for steam production that is utilized to operate the turbines that are coupled to electric generators. In this way, the mechanical work of the high-pressure steam is converted into electricity [194,195].

The fission of an atom occurs when a relatively large fissile atomic nucleus such as uranium-235 or plutonium-239 absorbs a neutron. The atom is then split by the fission into two or more smaller nuclei with kinetic energy, gamma radiation, and free neutrons [194]. Other fissile atoms may absorb a portion of these neutrons and create more fission, which release more neutrons, and so on [195]. By using neutron moderators and neutron poisons, this nuclear chain reaction can be controlled in order to adjust the potion of neutrons that will cause more fission. Manual or automatic control systems are used for this purpose or to shut down the reactor if unsafe conditions are detected [196].

Heat generation by the reactor core from fission involves several stages. The kinetic energy of the fission products is converted into thermal energy when a collision happens between the nuclei and nearby atoms. The reactor absorbs some of the gamma radiation produced during fission in the form of heat. Neutron absorption activates some materials, and the radioactive decay of fission products produces heat. Even after the reactor is shut down, this decay heat source may remain for some time. A nuclear reaction can generate heat power that is 1,000,000 times that of the equal mass of coal.

After the fission process, the heat released from the reactor is removed by a cooling system. This heat is conveyed to another part of the power plant, in which the thermal energy is utilized to generate electricity. The hot coolant in general is used as the heat source for a boiler. The boiler generates the pressurized steam that mechanically drives the steam turbines. The steam turbines rotate the electric generators [197]. A simple operating schematic of a nuclear power plant is depicted in Fig. 23.43.

By utilizing different coolants and fuels and integrating different control methodologies, many different reactor designs can be accomplished. In order to meet a specific need, some of these designs can be employed for various applications. Space and naval applications are some of these specific applications. In these applications, generally highly enriched uranium is used as the fuel that increases the reactor's power density and efficiency [198]. Currently, researchers are investigating new nuclear power generation techniques, known as the generation IV reactors. These new designs will have the possibility to offer cleaner and more secure fission reactors with less risk of the proliferation of nuclear weapons. New designs such as ESBWR offer passively safe plants, and other designs that are believed to be almost foolproof are being pursued or are available to be built [199]. In the near future, it is expected that the fusion reactors will be viable, which will reduce or eliminate many safety risks associated with nuclear fission [200].

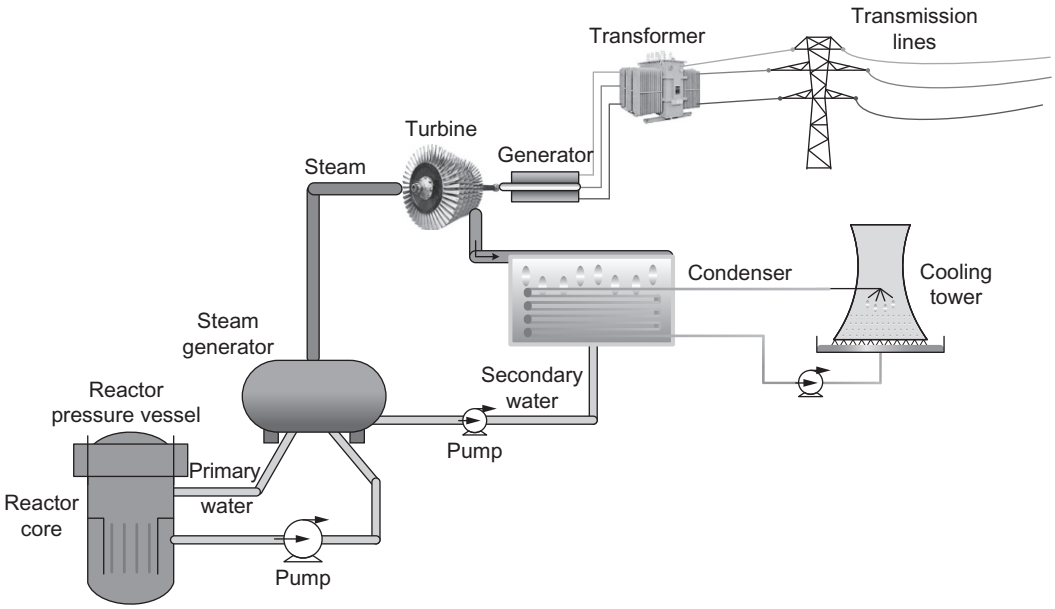


FIG. 23.43 A typical nuclear power plant.

23.3.8 Fuel Cell Power Plants

Since the beginning of twenty-first century, fuel-cell technology has been rapidly developed and has shown an invasive improvement for the applications ranging from portable electronic devices to vehicular power systems and MW size power plants [201–203]. Fuel cells are promising future energy conversion devices due to their high efficiency, excellent performance, low or zero emissions, and wide application area.

Fuel-cell power plants are electrochemical devices that produce electric energy directly from a chemical reaction. Fuel cells use fuel on the anode side and oxidant on the cathode side. The chemical reaction occurs on the electrolyte. The reactants, that is, fuel and oxidant, flow into the cell, while the reaction product (water) flows out of the cell. Many fuel and oxidant types can be used for fuel cells. Generally, hydrogen as the fuel and oxygen as the oxidant, from the air, can be used. On the other hand, alcohols and hydrocarbons can be other fuel types for different fuel cells, while other oxidants may be chlorine and chlorine dioxide [204–206].

Just like a battery, a fuel cell is composed of an electrolyte and a pair of electrodes. However, unlike the batteries, the reactants are continuously replenished during the operation; therefore, the cell is not required to be recharged. Ideally, fuel cells operate and continue to produce energy as long as the reactants are appropriately supplied to the anode and cathode sides.

There are many kinds of fuel cells categorized by their electrolyte type. Most common fuel-cell types are as follows:

- Proton exchange membrane fuel cells (PEMFCs)
- Phosphoric acid fuel cells (PAFCs)
- Direct methanol fuel cells (DMFCs)
- Solid oxide fuel cells (SOFC)
- Molten carbonate fuel cells (MCFCs)

PEMFCs are generally used for residential, vehicular, and portable applications. Solid electrolyte structure reduces the corrosion, they can operate at low temperature, and they have quick start-up and faster response times. PAFCs are typically used for transportation, heating, and electric utility applications. They may reach high efficiency points in electric cogeneration applications [207,208]. Currently, DMFCs are considered as a replacement alternative for batteries for small portable devices' power requirements. DMFC can be considered advantageous since methanol can be used directly without any reformer or fuel processor. However, they have relatively low efficiencies and slow response times since the reaction rate for the methanol is slow on presently available catalysts. On the other hand, DMFCs can be competitive with batteries since the simplicity, high storage density, and liquid methanol portability may compensate the relatively low efficiency [207]. MCFCs and SOFC are generally used as large power plants for electric utility applications. Both the technologies have higher efficiencies, fuel flexibility, and inexpensive catalysts [208]. However, they operate at really high temperatures generally between 600 and 1000°C. This high-temperature issue avoids these two fuel-cell technologies to be best candidates for portable or vehicular applications.

Especially, proton exchange membrane fuel cells are considered to be one of the most promising fuel-cell technologies among these next-generation fuel-cell power plants. This is due to their high efficiency and compact structure [209,210]. The operating principle of PEMFCs is focused in this section.

The operating principle along with the basic components of a PEMFC is presented in Fig. 23.44.

After the fuel is supplied to the anode side, the fuel is oxidized resulting in releasing electrons. The anode reaction for a fuel cell can be expressed as

$$2H_2 \rightarrow 4H^+ + 4e^- \tag{23.21}$$

These released electrons are transported to the cathode side through an external circuit. The hydrogen protons are traveled through the proton exchange membrane to the cathode side. The oxidant (i.e., oxygen) is reduced at the cathode side, using the electrons coming from the external circuit. Therefore, the cathode reaction is

$$O_2 + 4e^- \rightarrow 2O^{--}. \tag{23.22}$$

The hydrogen protons travel through the membrane and balance the flow of electrons through the external circuit. Therefore, the overall reaction equation becomes

$$2H_2 + O_2 \rightarrow 2H_2O + \text{Electric Power}. \tag{23.23}$$

A typical single fuel cell has a theoretical output voltage of 1.2 V. They generate ideally 0.6 A/cm^2. In order to reach higher voltage outputs from a fuel-cell system, cells are connected in series in the form of a string. For higher current outputs, the cells or the cell strings should be connected in parallel. Unfortunately, the output voltage of a fuel cell or a fuel-cell system decreases as the current drawn from the fuel cell is increased.

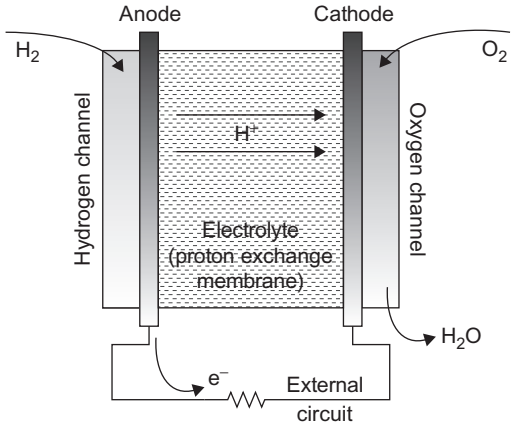


FIG. 23.44 Components of a PEM fuel cell and its operating principle.

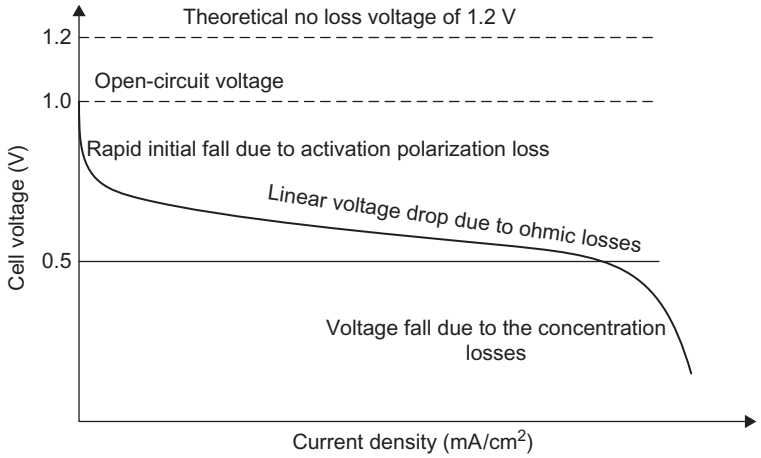


FIG. 23.45 Current-voltage characteristic of a fuel cell.

This voltage drop at the fuel-cell output is due to the ohmic, activation, and concentration losses [211].

A typical current-voltage characteristic curve of a fuel cell is shown in Fig. 23.45, which is also known as the polarization curve.

The output voltage of a fuel cell is less than its theoretical value even in the open-circuit conditions. This is due to the fact that the open-circuit voltage is calculated based on the ideal burning enthalpy of the hydrogen. The activation loss is generally effective at the low current densities. Activation loss is due to the electrode kinetics in which the electrochemical reaction of hydrogen and oxygen is slow. Activation loss causes a nonlinear voltage drop as the current starts to be drawn from the fuel cell. Ohmic losses are due to the electron flow through the electrolyte and electrodes and the equivalent resistance of the external circuit. Ohmic losses are directly proportional to the current density, and they increase linearly as the current increases. Concentration losses are due to the inability of maintaining the initial fuel concentration on the electrodes. Fuel and oxidant should be supplied sufficiently and continuously in order to meet sustained load demands. If the current is more than a certain value, a fuel cell fails to meet the new power demand, and the output voltage dramatically decreases. Therefore, this loss is quite severe at the high current densities.

Due to the polarization and current-voltage characteristics of the fuel cells, power conditioning devices such as dc/dc and/or dc/ac converters are required to maintain a fixed and stable dc voltage for the load bus. The power conditioning is also useful for converting the fuel-cell output to an appropriate magnitude and type. Power conditioning unit (PCU) not only controls the fuel-cell output voltage but also delivers a high power factor in grid-connected applications. PCU can reduce or eliminate the harmonics and help them operate effectively under all conditions. A fuel-cell power plant operating together with a PCU is presented in Fig. 23.46.

In the stationary or vehicular applications, a fuel-cell power plant may not be sufficient to satisfy all of the load demands [210]. Especially during transient load changes or peak demand periods, a fuel cell needs to be operated with an auxiliary power device such as battery packs or ultracapacitors. By operating fuel cell cascaded with batteries and/or ultracapacitors, steady-state, peak power demands, and transient load changes can be controlled more efficiently. In the topology of Fig. 23.47, the fuel-cell power plant is operated with auxiliary power devices.

23.4 Conclusions

In order to meet the future energy requirements, the energy should be generated and utilized wisely. Increasing the demand for energy, decreasing conventional fossil-fuel energy sources, and environmental concerns are driving forces toward renewable energy sources. However, the conventional sources will be utilized until modern, clean, and renewable technologies replace them. Therefore, a comprehensive strategy that supports a diversity of resources over the next century should be developed. Sustainable and long-term energy solutions in numerous forms are required to restructure the future's increasing energy demand.

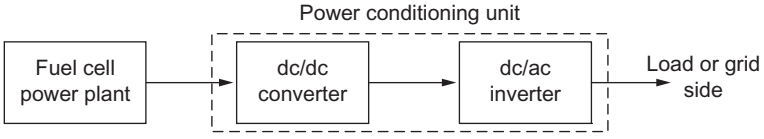


FIG. 23.46 A fuel-cell power plant operation with PCU.

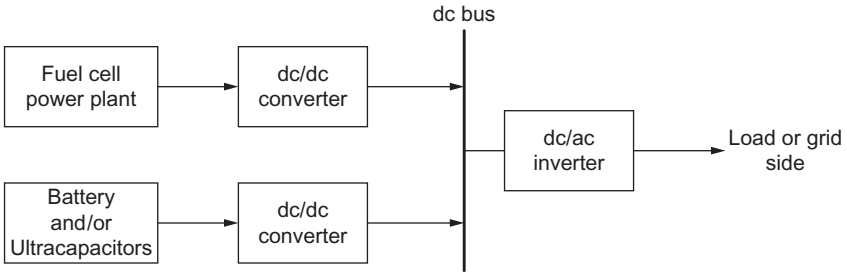


FIG. 23.47 Fuel-cell power plant operation with auxiliary power devices.

References

[1] World Consumption of Primary Energy by Energy Type and Selected Country Groups, Report of Energy Information Administration, International Energy Annual, 2005.

[2] Energy Consumption: Consumption per Capita, Technical Report by the World Resources Institute, http://www.wri.org. Retrieved on 10 October 2010.

[3] World per Capita Total Primary Energy Consumption, 1980–2006, Report of Energy Information Administration, International Energy Annual, 2006.

[4] International Energy Outlook, Technical Report by the Energy Information Administration, Official Energy Statistics from the US Government, http://www.eia.doe.gov, 2008. Retrieved on 09 October 2010.

[5] Energy Efficiency Measures and Technological Improvements, Continuum of Action, Annual Activity Report 2007 to 2008. (e_8 is an "Energy Organization" comprising 9 leading electricity companies from the G8 countries).

[6] Coal Facts 2006 Edition with 2005 Data, Technical Annual Report of World Coal Institute, 2006.

[7] D. Yergin, The Prize: The Epic Quest for Oil, Money, and Power, Free Press, New York, 1993.

[8] Official European Parliament Resolution on the Road Map for Renewable Energy in Europe, http://www.europarl.europa.eu, 2007. Retrieved on 25 September 2007.

[9] 2008 Buildings Energy Data Book, Prepared for the Buildings Technologies Program Energy Efficiency and Renewable Energy of US Department of Energy, by D&R International, Ltd., under contract to National Energy Technology Laboratory, 2008.

[10] Manufacturing Trend Data 1998 and 2002, Technical Report by the Energy Information Administration, Official Energy Statistics from the US Government, http://www.eia.doe.gov/emeu/efficiency/mecs_trend_9802/mecs9802_table2b.html. Retrieved on 10 February 2010.

[11] The WNA Market Report, The Global Nuclear Fuel Market: Supply and Demand 2007–2030, Technical Report by the World Nuclear Association (WNA).

[12] C.R. de Auza, Installed U.S. Wind Power Capacity Surged 45% in 2007, American Wind Energy Association Market Report, 2007.

[13] SEGS III, IV, V, VI, VII, VIII & IX, NEXTera Energy Sources, http://www.nexteraenergyresources.com/content/where/portfolio/pdf/segs.pdf. Retrieved on 14 October 2010.

[14] National Energy Survey of 2006, Technical Report by the Energy Information Administration, Official Energy Statistics from the US Government, http://www.eia.doe.gov.

[15] 2008–2017 Regional & National Peak Demand and Energy Forecast Bandwidths, Technical Report by the: Load Forecasting Working Group of the Reliability Assessment Subcommittee, North American Electric Reliability Corporation (NERC), 2008.

[16] G. Russel, D. Ann, Oil officials see limit looming on production, Wall Street J. (2007) A1.

[17] S.S. Devgan, Impact of environmental factors on the economic evaluation of renewable energy alternative generation, in: Proceedings of 33rd Southeastern Symposium on System Theory, Athens, OH, USA, 2001, pp. 123–126.

[18] World Consumption of Primary Energy by Energy Type and Selected Country Groups, 1980–2004, Energy Information Administration, U.S. Department of Energy, July 2006.

[19] Natural Gas Reserves Summary as of December 31, 2007, Technical Report by the Energy Information Administration, Official Energy Statistics from the US Government.

[20] Natural Gas and the Environment, http://www.naturalgas.org. Retrieved on 10 October 2010.

[21] Key World Energy Statistics 2007, Annual technical report of the International Energy Agency.

[22] M. Brower, in: Cool Energy: Renewable Solutions to Environmental Problems, The MIT Press, 1992.

[23] Environmental Impacts of Renewable Energy Technologies, Briefing paper of the "Union of Concerned Scientists", August 2005.

[24] World Energy Intensity: Total Primary Energy Consumption per Dollar of Gross Domestic Product using Purchasing Power Parities: 1980–2004, Technical Report by the Energy Information Administration, Report released December 2008.

[25] World Nuclear Power Reactors, Technical report of the "Uranium Information Center," August 2007.

[26] Nuclear Power in the World Today, Briefing paper 7, "Uranium Information Center", August 2007.

[27] Global Uranium Resources to Meet Projected Demand,, Latest Edition of 'Red Book' Predicts Consistent Supply up to 2025, International Atomic Energy Agency, 2006.

[28] International Energy Annual 2006, "World Energy Reserves," Technical Report by the Energy Information Administration, Official Energy Statistics from the US Government, Report released June-December 2008.

[29] International Energy Annual 2006, World Energy Consumption in Standard U.S. Physical Units, Technical Report by the Energy Information Administration, Official Energy Statistics from the US Government, Report released June-December 2008.

[30] 2007 World PV Industry Reports, Annual World Solar PV Industry Report by Marketbuzz 2008.

[31] J.W. Tester, E.M. Drake, M.J. Driscoll, M.W. Golay, W.A. Peters, Sustainable Energy: Choosing Among Options, The MIT Press, Cambridge, MA, 2005.
[32] W.A. Hermann, Quantifying global exergy resources, J. Energy 31 (12) (2006) 1685–1702.
[33] Global Wind Energy Markets, Technical report by the Global Wind Energy Council, February 2008.
[34] A. Inoue, M.H. Ali, R. Takahashi, T. Murata, J. Tamura, A calculation method of the total efficiency of wind generator, in: Proceedings of Power Electronics and Drives Systems (PEDS), Kuala Lumpur, Malaysia, 2, 2005, pp. 1595–1600.
[35] J. Brooke, Engineering Committee on Oceanic Resources Working Group on Wave Energy Conversion,, Wave Energy Conversion, Elsevier, 2003.
[36] M.E. McCormick, Ocean Wave Energy Conversion, Dover Publications, Mineola, NY, 2007.
[37] T.W. Thorpe, An overview of wave energy technologies, status, performance, and costs, in: Proceedings of Wave power: Moving towards commercial viability, London, 1999, pp. 1–16.
[38] J. Cruz, M. Gunnar, S. Barstow, D. Mollison, J. Cruz, Green Energy and Technology, Ocean Wave Energy, Springer Science and Business Media, 2008.
[39] W. Munk, C. Wunsch, Abyssal recipes II: Energetics of tidal and wind mixing, Deep-Sea Res. 45 (June 1998) 1977–2010.
[40] Renewables, Global Status Report 2006, Technical report by the REN21, Renewable Energy Policy Network for the 21st Century, 2006.
[41] D.E. Lennard, Ocean thermal energy conversion—past progress and future prospects, IEEE Proceedings on Physical Science, Measurement and Instrumentation, Management and Education Reviews, vol. 134, May 1987, pp. 381–391.
[42] L.R. Berger, J.A. Berger, Countermeasures to microbiofouling in simulated ocean thermal energy conversion with surface and deep ocean waters in Hawaii, Appl. Environ. Microbiol. 51 (6) (1986) 1186–1198.
[43] L. Meegahapola, L. Udawatta, S. Witharana, "The ocean thermal energy conversion strategies and analysis of current challenges", in: Proceedings of International Conference on Industrial and Information Systems, 2007, pp. 123–128.
[44] The Hydrogen Economy: Opportunities, Costs, Barriers, and R&D Needs, by: Committee on Alternatives and Strategies for Future Hydrogen Production and Use, National Research Council, and National Academy of Engineering, National Academies Press, August 2004. Retrieved on 16 February 2009.
[45] J. McCarthy, Hydrogen. Stanford University, http://www-formal.stanford.edu/jmc/progress/hydrogen.html, 1995. Retrieved on 04 May 2009.
[46] D. Palmer, Hydrogen in the Universe. NASA, http://imagine.gsfc.nasa.gov, 1997.
[47] Hydrogen as an energy carrier, Technical Report by the Royal Belgian Academy Council of Applied Science, Belgium, April 2006.
[48] F. Lau, C.E.G. Padro, Advances in Hydrogen Energy, Springer, New York, USA, 2000.
[49] D.A.J. Rand, R.M. Dell, Hydrogen Energy: Challenges and Prospects, Royal Society of Chemistry, 2008.
[50] All About Geothermal Energy, Geothermal Energy Association, Washington DC, February 2007.
[51] The Future of Geothermal Energy, Impact of Enhanced Geothermal Systems (EGS) on the United States in the 21st Century, Technical Report by the Massachusetts Institute of Technology, 2006.
[52] J. Farigone, J. Hill, D. Tillman, S. Polasky, P. Hawthome, Land clearing and biofuel carbon debt, Science 319 (2008) 1235–1238.
[53] T. Searchinger, R. Heimlich, R.A. Houghton, F. Dong, A. Amani, J. Fabiosa, S. Tokgaz, D. Hayes, Use of U.S. croplands for biofuels increases greenhouse gases through emission from land-use change, Science 319 (2008) 1238–1240.
[54] R.E. Sonntag, C. Borgnakke, G.J. Van Wylen, Fundamentals of Thermodynamics, sixth ed., Wiley, Haboken, New Jersey, USA, 2002.
[55] M.J. Moran, H.N. Shapiro, Fundamentals of Engineering Thermodynamics, fifth ed., Wiley, New York, USA, 2003.
[56] F. Wicks, J. Maleszweski, C. Wright, J. Zarbnicky, Thermodynamic analysis of an enhanced gas and steam cycle, in: Proceedings of 37th Intersociety Energy Conversion Engineering Conference, 2004, pp. 456–459.
[57] L. Beltracchi, A direct manipulation for water-based Rankine cycle heat engines, IEEE Trans. Syst. Man Cybern. 17 (3) (1987) 478–487.
[58] T.J. Ratajczak, M. Shahidehpour, Emerging technologies for coal-fired generation, in: Proceedings of Power Engineering Society General Meeting, Quebec, Canada, October, 2006, pp. 1–9.
[59] Net Generation by Energy Source by Type of Producer, Annual Electric Power Report of the Energy Information Administration, U. S. Department of Energy, December 2008.
[60] Renewables, Global Status Report 2006 Update, Technical Report by the Renewable Energy Policy Network for the 21st Century, REN21, 2007.
[61] 21st Century Complete guide to Hydropower, Hydroelectric Power, Dams, Turbine, Safety, Environmental Impact, Microhydropower, Impoundment, Pumped Storage Diversion, Run-of-River, by U.S. Government, Progressive Management, Washington, DC, USA, September 2006.
[62] A.J. Wood, B.F. Wollenberg, Power Generation, Operation, and Control, second ed., Wiley-Interscience, Malden, MA, USA, 1996.
[63] L.L. Grigsby, Electric Power Generation, Transmission, and Distribution, second ed., CRC Press, Boca Raton, FL, 2007.
[64] R. Chapo, Solar energy overview, Ezinearticles.com, December 2008, http://ezinearticles.com. Retrieved on 20 December 2009.
[65] U.S. Department of Energy, "PV Physics", Energy Efficiency and Renewable Energy, Solar Energy Technologies Program, http://www1.eere.energy.gov/solar. Retrieved on 17 November 2009.
[66] U.S. Department of Energy, "PV Systems", Energy Efficiency and Renewable Energy, Solar Energy Technologies Program, http://www1.eere.energy.gov/solar. Retrieved on 17 November 2009.
[67] Missouri Department of Natural Resources, "Missouri's solar energy resource", http://www.dnr.mo.gov. Retrieved on 20 November 2009.
[68] U.S. Department of Energy, "Concentrating Solar Power", Energy Efficiency and Renewable Energy, Solar Energy Technologies Program, http://www1.eere.energy.gov.
[69] A. Lasnier, T.G. Ang, Photovoltaic Engineering Handbook, Adam Hilger Bristol, New York, 1990. pp. 69–97.
[70] U.S. Department of Energy, "Current-voltage Measurements", Energy Efficiency and Renewable Energy, Solar Energy Technologies Program, http://www1.eere.energy.gov/solar. Retrieved on 25 November 2009.
[71] M.A.S. Masoum, H. Dehbonei, E.F. Fuchs, Theoretical and experimental analyses of photovoltaic systems with voltage and current-based maximum power-point tracking, IEEE Trans. Energy Convers. 17 (4) (2002) 514–522.

[72] H. Koizumi, K. Kurokawa, A novel maximum power point tracking method for PV module integrated converter, in: IEEE 36th Power Electronics Specialists Conf., Recife, Brazil, 2005, pp. 2081–2086.
[73] Y. Goswami, F. Kreith, J. Kreder, Principles of solar engineering, Fundamentals of Solar Engineering, Taylor & Francis, Philadelphia, 1999.
[74] A. Canova, L. Giaccone, F. Spertino, Sun tracking for capture improvement, in: Proceedings of 22nd European Photovoltaic Solar Energy Conference (EUPVSEC), WIP Renewable Energies, Milano, 2007, pp. 3053–3058.
[75] H.D. Mohring, F. Klotz, H. Gabler, Energy yield of PV tracking systems, in: Proceedings of 21st European Photovoltaic Solar Energy Conference, (EUPVSEC), WIP Renewable Energies, Barcelona, Spain, Dresden, September, 2006, pp. 2691–2694.
[76] C. Aracil, J.M. Quero, L. Castañer, R. Osuna, L.G. Franquelo, Tracking system for solar power plants, in: Proceedings of IEEE 32nd Annual Conference in Industrial Electronics, 2006, pp. 3024–3029.
[77] M. Dominguez, I. Ameijeiras, L. Castaner, J.M. Wuero, A. Guerrero, L.G. Franquelo, A novel light source position sensor, Patent number P9901375.
[78] D.A. Pritchard, Sun tracking by peak power positioning for photovoltaic concentrator arrays, IEEE Contr. Syst. Mag. 3 (3) (2003) 2–8.
[79] D.P. Hohm, M.E. Ropp, Comparative study of maximum power point tracking algorithms using an experimental, programmable, maximum power point tracking test bed, in: Proceedings of 28th IEEE Photovoltaic Specialists Conference, 2000, pp. 1699–1702.
[80] K.H. Hussein, Maximum photovoltaic power tracking: An algorithm for rapidly changing atmospheric conditions, IEEE Proc. Transm. Distrib. 142 (1) (1995) 59–64.
[81] D. O'Sullivan, H. Spruyt, A. Crausaz, PWM conductance control, in: Proceedings of IEEE 19th Annual Power Electronics Specialists Conference, New Orleans, Louisiana, 1, 1988, pp. 351–359.
[82] L. Bangyin, D. Shanxu, L. Fei, X. Pengwei, Analysis and improvement of maximum power point tracking algorithm based on incremental conductance method for photovoltaic array, in: Proceedings of IEEE 7th International Conference on Power Electronics and Drive Systems, Bangkok, Thailand, 2007, pp. 637–641.
[83] D.P. Hohm, M.E. Ropp, Comparative study of maximum power point tracking algorithm, in: Proceedings of 28th IEEE Photovoltaic Specialists Conference, 2000, pp. 1699–1702.
[84] T. Esram, P.L. Chapman, Comparison of photovoltaic array maximum power point tracking techniques, IEEE Trans. Energy Convers. 22 (2) (2007) 439–449.
[85] N. Femia, G. Petrone, G. Spagnuolo, M. Vitelli, Optimization of perturb and observe maximum power point tracking method, IEEE Trans. Power Electron. 20 (4) (2005) 963–973.
[86] J.H.R. Enslin, D.B. Snyman, Simplified feed-forward control of the maximum power point in PV installations, in: IEEE Industrial Electronics Conference, San Diego, CA, USA, 1, 1992, pp. 548–553.
[87] A.S. Kislovski, R. Redl, Maximum-power-tracking using positive feedback, in: IEEE 25th Power Electronics Specialists Conference, Taipei, Taiwan, 2, 1994, pp. 1065–1068.
[88] C.Y. Won, D.H. Kim, S.C. Kim, W.S. Kim, H.S. Kim, A new maximum power point tracker of photovoltaic arrays using fuzzy controller, in: IEEE Power Electronics Specialists Conference, Taipei, Taiwan, 1994, pp. 396–403.
[89] J.J. Schoeman, J.D. van Wyk, A simplified maximal power controller for terrestrial photovoltaic panel arrays, in: Proceedings of 13th Annual IEEE Power Electronics Specialists Conference, 1982, pp. 361–367.
[90] M. Buresch, Photovoltaic Energy Systems, McGraw Hill, New York, 1983.
[91] G.W. Hart, H.M. Branz, C.H. Cox, Experimental tests of open loop maximum power-point tracking techniques, Solar Cells 13 (1984) 185–195.
[92] D.J. Patterson, "Electrical system design for a solar powered vehicle", in: Proceedings of 21st Annual IEEE Power Electronics Specialists Conference, San Antonio, TX, USA, 1990, pp. 618–622.
[93] W. Xiao, W.G. Dunford, A modified adaptive hill climbing MPPT method for photovoltaic power systems, in: Proceedings of 35th Annual IEEE Power Electronics Specialists Conference, Aachen, Germany, 2004, pp. 1957–1963.
[94] H.-J. Noh, D.-Y. Lee, D.-S. Hyun, An improved MPPT converter with current compensation method for small scaled PV applications, in: Proceedings of 28th Annual Conf. Industrial Electronics Society, Sevilla, Spain, 2002, pp. 1113–1118.
[95] K. Kobayashi, H. Matsuo, Y. Sekine, A novel optimum operating point tracker of the solar cell power supply system, in: Proceedings of 35th Annual IEEE Power Electronics Specialists Conference, Aachen, Germany, 2004, pp. 2147–2151.
[96] B. Bekker, H.J. Beukes, Finding an optimal PV panel maximum power point tracking method, in: Proceedings of 7th AFRICON Conference, Africa, Botswana, Nigeria, 2004, pp. 1125–1129.
[97] S. Yuvarajan, S. Xu, Photo-voltaic power converter with a simple maximum-power-point-tracker, in: Proceedings of 2003 International Symposium Circuits Systems, Bangkok, Thailand, 2003. pp. III-399–III-402.
[98] R.M. Hilloowala, A.M. Sharaf, A rule-based fuzzy logic controller for a PWM inverter in photo-voltaic energy conversion scheme, in: Proceedings of IEEE Industrial Application Society Annual Meeting, Houston, TX, USA, 1992, pp. 762–769.
[99] T. Senjyu, K. Uezato, Maximum power point tracker using fuzzy control for photovoltaic arrays, in: Proceedings of IEEE International Conf. Industrial Technologies, Guangzhou, China, 1994, pp. 143–147.
[100] G.-J. Yu, M.-W. Jung, J. Song, I.-S. Cha, I.-H. Hwang, Maximum power point tracking with temperature compensation of photovoltaic for air conditioning system with fuzzy controller, in: Proceedings of IEEE Photovoltaic Specialists Conference, Washington, DC, USA, 1996, pp. 1429–1432.
[101] M.G. Simoes, N.N. Franceschetti, M. Friedhofer, A fuzzy logic based photovoltaic peak power tracking control, in: Proceedings of IEEE International Symposium Industrial Electronics, Pertoria, South Africa, 1998, pp. 300–305.
[102] A.M.A. Mahmoud, H.M. Mashaly, S.A. Kandil, H. El Khashab, M.N. F. Nashed, Fuzzy logic implementation for photovoltaic maximum power tracking, in: Proceedings of 9th IEEE International Workshop Robot Human Interactive Communications, Osaka, Japan, 2000, pp. 155–160.
[103] N. Patcharaprakiti, S. Premrudeepreechacharn, Maximum power point tracking using adaptive fuzzy logic control for grid connected photovoltaic system, in: IEEE Power Engineering Society Winter Meeting, New York, NY, 2002, pp. 372–377.
[104] B.M. Wilamowski, X. Li, Fuzzy system based maximum power point tracking for PV system, in: Proceedings of 28th Annual Conference of IEEE Industrial Electronics Society, 2002, pp. 3280–3284.

[105] M. Veerachary, T. Senjyu, K. Uezato, Neural-network-based maximum-power-point tracking of coupled-inductor interleaved-boost-converter-supplied PV system using fuzzy controller, IEEE Trans. Ind. Electron. 50 (4) (August 2003) 749–758.
[106] N. Khaehintung, K. Pramotung, B. Tuvirat, P. Sirisuk, RISC microcontroller built-in fuzzy logic controller of maximum power point tracking for solar-powered light-flasher applications, in: Proceedings of 30th Annual Conference of IEEE Industrial Electronics Society, 2004, pp. 2673–2678.
[107] T. Hiyama, S. Kouzuma, T. Imakubo, Identification of optimal operating point of PV modules using neural network for real time maximum power tracking control, IEEE Trans. Energy Convers. 10 (2) (June 1995) 360–367.
[108] K. Ro, S. Rahman, Two-loop controller for maximizing performance of a grid-connected photovoltaic-fuel cell hybrid power plant, IEEE Trans. Energy Convers. 13 (3) (1998) 276–281.
[109] A. Hussein, K. Hirasawa, J. Hu, J. Murata, The dynamic performance of photovoltaic supplied dc motor fed from DC–DC converter and controlled by neural networks, in: Proceedings of International Joint Conference on Neural Networks, Atlanta, Georgia, USA, 2002, pp. 607–612.
[110] X. Sun, W. Wu, X. Li, Q. Zhao, A research on photovoltaic energy controlling system with maximum power point tracking, in: Proceedings of Power Conversion Conference, Osaka, Japan, 2002, pp. 822–826.
[111] K. Samangkool, S. Premrudeepreechacharn, Maximum power point tracking using neural networks for grid-connected system, in: Proceedings of International Conference on Future Power Systems, Amsterdam, Netherlands, 2005, pp. 1–4.
[112] L. Zhang, Y. Bai, A. Al-Amoud, GA-RBF neural network based maximum power point tracking for grid-connected photovoltaic systems, in: Proceedings of International Conference Power Electronics, Machines and Drives, Bath, UK, 2002, pp. 18–23.
[113] P. Midya, P.T. Krein, R.J. Turnbull, R. Reppa, J. Kimball, Dynamic maximum power point tracker for photovoltaic applications, in: Proceedings of 27th Annual IEEE Power Electronics Specialists Conference, Baveno, Italy, 1996, pp. 1710–1716.
[114] M. Bodur, M. Ermis, Maximum power point tracking for low power photovoltaic solar panels, in: Proceedings of 7th Mediterranean Electrotechnical Conference, Antalya, Turkey, 1994, pp. 758–761.
[115] T. Kitano, M. Matsui, D.-h. Xu, Power sensor-less MPPT control scheme utilizing power balance at DC link-system design to ensure stability and response, in: Proceedings of 7th Annual Conference on IEEE Industrial Electronics Society, Denver, Colorado, USA, 2001, pp. 1309–1314.
[116] M. Matsui, T. Kitano, D.-h. Xu, Z.-q. Yang, A new maximum photovoltaic power tracking control scheme based on power equilibrium at DC link, in: Conference Record 1999 IEEE Industrial Applications Conference, Phoenix, Arizona, USA, 1999, pp. 804–809.
[117] S.B. Kjaer, J.K. Pedersen, F. Blaabjerg, Power inverter topologies for photovoltaic modules—a review, in: Proceedings of IAS'02 Conference, vol. 2, 2002, pp. 782–788.
[118] F. Blaabjerg, Z. Chen, S.B. Kjaer, Power electronics as efficient interface in dispersed power generation systems, IEEE Trans. Power Electron. 19 (5) (2004) 1184–1194.
[119] M. Meinhardt, G. Cramer, Past, present and future of grid connected photovoltaic- and hybrid-power-systems, in: Proceedings of IEEE Power Engineering Society Summer Meeting, vol. 2, 2000, pp. 1283–1288.
[120] T. Shimizu, M. Hirakata, T. Kamezawa, H. Watanabe, Generation control circuit for photovoltaic modules, IEEE Trans. Power Electron. 16 (3) (May 2001) 293–300.
[121] M. Meinhardt, D. Wimmer, Multistring-converter: the next step in evolution of string-converter technology, in: Proceedings of EPE'01 Conference, Graz, Austria, 2001, pp. 1–9.
[122] B.K. Bose, P.M. Szczeny, R.L. Steigerwald, Microcomputer control of a residential photovoltaic power conditioning system, IEEE Trans. Ind. Appl. 21 (5) (1985) 1182–1191.
[123] B. Lindgren, "Topology for decentralized solar energy inverters with a low voltage ac-bus", in: Proceedings of European Conference on Power Electronics and Applications, Lausanne, Switzerland, 1999, pp. 1–5.
[124] S.B. Kjaer, F. Blaabjerg, A novel single-stage inverter for AC-module with reduced low-frequency ripple penetration, in: Proceedings of 10th European Conference on Power Electronics and Applications, Toulouse, France, 2003, pp. 2–4.
[125] A. Lohner, T. Meyer, A. Nagel, "A new panel-integratable inverter concept for grid-connected photovoltaic systems", in: Proceedings of ISIE'96 Conference, vol. 2, 1996, pp. 827–831.
[126] C. Dorofte, Comparative analysis of four dc/dc converters for photovoltaic grid interconnection & design of a dc/dc converter for photovoltaic grid interconnection, Technical Report Aalborg University, Aalborg, Denmark, 2001.
[127] S.J. Chiang, Design and Implementation of Multi-Functional Battery Energy Storage Systems, Ph.D. Dissertation, Department of Electrical Engineering, National Tsing Hua University, Hsin-Chu, Taiwan, R.O.C., 1994.
[128] C.M. Liaw, T.H. Chen, S.J. Chiang, C.M. Lee, C.T. Wang, Small battery energy storage system, IEEE Proceedings on Electric Power Applications 140 (1) (1993) 7–17.
[129] H. Holttinen, P. Meibom, A. Orths, F. Van Hulle, C. Ensslin, L. Hofmann, J. McCann, J. Pierik, J.O. Tande, A. Estanquerio, L. Soder, G. Strbac, B. Parsons, J.C. Smith, B. Lemstrom, Design and operation of power systems with large amounts of wind power, first results of IEA collaboration, in: Proceedings of Global Wind Power Conference, Adelaide, Australia, September, 2006, pp. 1–147.
[130] World Wind Energy Association, Press Release, February 21, 2008, Bonn, Germany.
[131] Danish Wind Power Association, http://www.windpower.org/en, November 2008.
[132] A. Betz, Introduction to the Theory of Machines, Oxford-Pergamon Press, New York, USA, 1966.
[133] N.A. Ahmed, M.A. Miyateke, A Stand-alone hybrid generation system combining solar photovoltaic and wind turbine with simple maximum power point tracking control, in: Proceedings of 5th International Power Electronics and Motion Control Conference, vol. 1, 2006, pp. 1–7.
[134] J.R. Hendershot Jr., T.J.E. Miller, Design of Brushless Permanent-magnet Motors, Oxford Magna Physics Publications, England, 1994.
[135] H.-W. Lee, Advanced Control for Power Density Maximization of the Brushless DC Generator, Ph.D. Dissertation University of Arlington, Texas, Arlington, TX, USA, 2003.
[136] M.A. Khan, P. Pillay, M. Malengret, Impact of direct-drive WEC systems on the design of a small PM wind generator, Proc. IEEE Bologna Power Tech. Conf. 2 (2003) 7.

[137] L. Soderlund, J.-T. Eriksson, J. Salonen, H. Vihriala, R. Perala, A permanent-magnet generator for wind power applications, IEEE Trans. Magn. 32 (1996) 2389–2392.
[138] Tog Inge Reigstad, Direct Driven Permanent Magnet Synchronous Generators with Diode Rectifiers for Use in Offshore Wind Turbines, Ph.D. Dissertation, Norwegian University of Science and Technology Department of Electrical Power Engineering, Trondheim, Norway, 2007.
[139] H. Li, Z. Chen, Optimal direct-drive permanent magnet wind generator systems for different rated wind speeds, in: Proceedings of European Conference on Power Electronics and Applications, 2007, pp. 1–10.
[140] A. Grauers, Design of Direct-Driven Permanent-Magnet Generators For Wind Turbines, Ph.D. Dissertation, Chalmers University of Technology, Gothenburg, 1996.
[141] J. Marques, H. Pinheiro, H.A. Gründling, J.R. Pinherio, H.L. Hey, A survey on variable-speed wind turbine system, in: Cientifico Greater Forum of Brazilian Electronics of Power, COBEP'03, Cortaleza, Fortaleza, Brazil, 2003, pp. 732–738.
[142] M.M. Neam, F.F.M. El-Sousy, M.A. Ghazy, M.A. Abo-Adma, The dynamic performance of an isolated self-excited induction generator driven by a variable-speed wind turbine, in: Proceedings of International Conference on Clean Electric Power, Capri, Italy, May, 2007, pp. 536–543.
[143] G.S. Kumar, A. Kishore, Dynamic analysis and control of output voltage of a wind turbine driven isolated induction generator, in: Proceedings of IEEE International Conference on Industrial Technology, Bhubaneswar, India, 2006, pp. 494–499.
[144] M. Orabi, M.Z. Youssef, P.K. Jain, Investigation of self-excited induction generators for wind turbine applications, in: Proceedings of Canadian Conference on Electrical and Computer Engineering, Niagara Falls, Ontario, Canada, vol. 4, 2004, pp. 1853–1856.
[145] D. Seyoum, M.F. Rahman, C. Grantham, "Inverter supplied voltage control system for an isolated induction generator driven by a wind turbine", in: Proceedings of Industry Applications Conference (38th IAS Annual Meeting), Salt Lake City, Utah, USA, vol. 1, 2003, pp. 568–575.
[146] E. Muljadi, J. Sallan, M. Sanz, C.P. Butterfield, Investigation of self-excited induction generators for wind turbine applications, in: Proceedings of IEEE Industry Applications Conference (34th IAS Annual Meeting), Phoenix, Arizona, USA, vol. 1, 1999, pp. 509–515.
[147] T. Ahmed, O. Noro, K. Matsuo, Y. Shindo, M. Nakaoka, Wind turbine coupled three-phase self-excited induction generator voltage regulation scheme with static VAR compensator controlled by PI controller, in: Proceedings of International Conference on Electrical Machines and Systems, vol. 1, 2003, pp. 293–296.
[148] T. Ahmed, O. Noro, E. Hiraki, M. Nakaoka, Terminal voltage regulation characteristics by static Var compensator for a three-phase self-excited induction generator, IEEE Trans. Ind. Appl. 40 (2004) 978–988.
[149] W. Qiao, G.K. Veneyagamoorthy, R.G. Harley, Real-time implementation of a STATCOM on a wind farm equipped with doubly fed induction generators, in: Proceedings of IEEE Industry Applications Conference (41st IAS Annual Meeting), vol. 2, 2006, pp. 1073–1080.
[150] J.M. Elder, J. t Boys, J.L. Woodward, The process of self-excitation in induction generators, IEEE Proc. 130 (B) (1983) 103–108.
[151] C. Ma, R. Cheung, Advanced Voltage and Frequency Control for the Stand-Alone Self-excited Induction Generator, Electrical & Computer Engineering Department of Ryerson University, Toronto, Canada, 2008.
[152] M.T. Abolhassani, H.A. Toloyat, P. Enjeti, "Stator flux-oriented control of an integrated alternator/active filter for wind", in: Proceedings of the IEEE International Electric Machines and Drives Conference, Madison, Wisconsin, USA, vol. 1, 2003, pp. 461–467.
[153] S. Eel-Hwan, S.-B. Oh, Y.-H. Kim, C.-S. Kim, Power control of a doubly fed induction machine without rotational transducers, in: Proceedings of the Power Electronics and Motion Control Conference, Beijing, China, vol. 2, 2000, pp. 951–955.
[154] H. Azaza, A. Masmoudi, On the dynamics and steady state performance of a vector controlled DFM drive systems, in: Proceedings of IEEE International Conference on Man and Cybernetics, vol. 6, 2002, pp. 6.
[155] A. Tapia, G. Tapia, J.X. Ostolaza, J.R. Saenz, Modeling and control of a wind turbine driven DFIG, IEEE Trans. Energy Convers. 18 (2003) 194–204.
[156] L. Jiao, B.-T. Ooi, G. Joos, F. Zhou, Doubly-fed induction generator (DFIG) as a hybrid of asynchronous and synchronous machines, Electr. Power Syst. Res. 76 (2005) 33–37.
[157] S. Muller, M. Diecke, R.W. De Doncker, Doubly fed induction generator systems for wind turbines, IEEE Ind. Appl. Mag. 8 (2002) 26–33.
[158] R. Pena, J.C. Clare, G.M. Asher, A doubly fed induction generator using back-to-back PWM converters supplying an isolated load from a variable speed wind turbine, IEEE Proc. Electric Power Appl. 143 (1996) 380–387.
[159] L. Xu, Y. Tang, Stator field oriented control of doubly-excited induction machine in wind power generation system, in: Proceedings of 25th Mid West Symposium on Circuit and Systems, 1992, pp. 1449–1466.
[160] L. Xu, W. Cheng, Torque and reactive power control of a doubly fed induction machine by position sensorless scheme, IEEE Trans. Ind. Appl. 31 (1995) 636–642.
[161] S. Doradla, S. Chakrovorty, K. Hole, A new slip power recovery scheme with improved supply power factor, IEEE Trans. Power Electron. 3 (1988) 200–207.
[162] R. Pena, J. Clare, G. Asher, Doubly fed induction generator using back-to-back pwm converters and its application to variable-speed wind-energy conversion, IEEE Proc. Electric Power Appl. 143 (1996) 231–241.
[163] Y. Tang, L. Xu, A flexible active and reactive power control strategy for a variable speed constant frequency generating systems, IEEE Trans. Power Electron. 10 (July 1995) 472–478.
[164] A. Feijo, J. Cidrs, C. Carrillo, Third order model for the doubly-fed induction machine, Electric Power Syst. Res. 56 (2000) 121–127.
[165] B.H. Chowdhury, S. Chellapilla, Double-fed induction generator control for variable speed wind power generation, Electric Power Syst. Res. 76 (2006) 786–800.
[166] J.A. Sanchez, C. Veganzones, S. Martinez, F. Blazquez, N. Herrero, J. R. Wilhelmi, Dynamic model of wind energy conversion systems with variable speed synchronous generator and full-size power converter for large-scale power system stability studies, Renew. Energy 33 (2008) 1186–1198.
[167] A. Bouscayrol, P. Delarue, X. Guillaud, Power strategies for maximum control structure of a wind energy conversion system with a synchronous machine, Renew. Energy 30 (2005) 2273–2288.
[168] G. Raina, O.P. Malik, Variable speed wind energy conversion using synchronous machine, IEEE Trans. Aerosp. Electron. Syst. 21 (1985) 100–105.

[169] G. Raina, O.P. Malik, Wind energy conversion using a self-excited induction generator, IEEE Trans. Power Syst. 102 (1983) 3933–3936.
[170] B. Borowy, Z. Salameh, Dynamic response of a stand alone wind energy conversion system with battery energy storage to a wind gust, IEEE Trans. Energy Convers. 12 (1997) 73–78.
[171] Z. Chen, E. Spooner, Grid power quality with variable speed wind turbine, IEEE Trans. Energy Convers. 16 (2001) 148–154.
[172] J.A. Baroudi, V. Dinavahi, A.M. Knight, A review of power converter topologies for wind generators, in: IEEE International Conference on Electric Machines and Drives, 2005, pp. 458–465.
[173] J.H.R. Enslin, J. Knijp, C.P.J. Jansen, P. Bauer, Integrated approach to network stability and wind energy technology for on-shore and offshore application, in: 2003, pp. 185–192.
[174] L. Ran, J.R. Bumby, P.J. Tavner, Use of turbine inertia for power smoothing of wind turbines with a DFIG, in: Proceedings of 11th International Conference on Harmonics and Quality Power, 2004, pp. 106–111.
[175] K. Strunz, E.K. Brock, Hybrid plant of renewable stochastic source and multilevel storage for emission-free deterministic power generation, in: Proceedings of Quality and Security Electric Power Delivery Systems CIGRE/IEEE PES International Symposium, October 8–10, 2003, pp. 214–218.
[176] J.P. Barton, D.G. Infield, Energy storage and its use with intermittent renewable energy, IEEE Trans. Energy Convers. 19 (June 2004) 441–448.
[177] R. Cardenas, R. Pena, G. Asher, J. Clare, Power smoothing in wind generation systems using a sensorless vector controlled induction machine driving a flywheel, IEEE Trans. Energy Convers. 19 (March 2004) 206–216.
[178] C. Abbey, G. Joos, Supercapacitor energy storage for wind energy application, IEEE Trans. Ind. Appl. 43 (2007) 769–776.
[179] Ocean Energy: Technology Overview, Renewable Development Initiative, http://ebrdrenewables.com/sites/renew/ocean.aspx. Retrieved on 26 February 2009.
[180] W.J. Jones, M. Ruane, Alternative Electrical Energy Sources for Maine, Appendix I, Wave Energy Conversion by J. Mays, Report No. MIT-E1 77–010, MIT Energy Laboratory, July 1977.
[181] Ocean Energy, Report of the US Department of Interior Minerals Management Service, Retrieved on 28 November 2008.
[182] A. Wolfbrandt, Automated design of a linear generator for wave energy converters—a simplified model, IEEE Trans. Magn. 42 (7) (2007) 1812–1819.
[183] Ocean Energy: Technology Overview, Renewable Development Initiative, http://ebrdrenewables.com.
[184] D.A. Dixon, Fish and the Energy Industry, in: EPRI (Electric Power Research Institute) research report, ASMFC Energy Development Workshop, October, 2006.
[185] Geothermal Energy, Power from the Depths, Technical Report, by NREL for US Department of Energy, DOE/Gp-10097-518 FS18, Golden, CO, USA, 8, December 1997.
[186] S. Sheth, M. Shahidehpour, Geothermal energy in power systems, in: Proceeding of IEEE Power Engineering Society General Meeting, vol. 2, Denver, CO, USA, 2004, pp. 1972–1977.
[187] International Energy Agency (IEA), "Renewable Energy … into the Mainstream", Renewable Energy Working Party, Netherlands, 2002.
[188] M.H. Dickson, M. Fanelli, Istituto di Geoscienze e Georisorse, Pisa, Italy, http://iga.igg.cnr.it/geothermal.php. Retrieved on 04 March 2009.
[189] G.W. Braun, H.K. McCluer, Geothermal power generation in United States, Proc.IEEE 81 (3) (1993) 434–448.
[190] Geothermal Energy Assessment, The World Bank Group, www.worldbank.org/html/fpd/energy/geothermal/assessment. Retrieved on 17 March 2009.
[191] Clean Energy Basics: Introduction to geothermal energy production, NREL, www.nrel.gov/energy.
[192] W.P. Short III, Trends in the American geothermal energy industry, Geotherm. Resour. Counc. Bull. 20 (9) (1991) 245–257.
[193] Geothermal Energy Facts, Advanced Level, Geothermal Education Office, www.geothermal.marin.org/geoenergy. Retrieved on 17 March 2009.
[194] DoE Fundamentals Handbook: Nuclear Physics and Reactor Theory, vol. 1–2, US Department of Energy, FSC-6010, January 1993.
[195] D. Bodansky, Nuclear Energy: Principles, Practices, and Prospects, second ed., Springer, New York, USA, 2008.
[196] Reactor Protection & Engineered Safety Feature Systems, The Nuclear Tourist, http://www.nucleartourist.com/systems/rp.htm. Retrieved on 02 April 2009.
[197] I. Hore-Lacy, Nuclear Energy in the 21st Century: World Nuclear University Press, first ed., Academic Press, Maryland Heights, MO, USA, 2006.
[198] C. Ma, F. von Hippel, Ending the production of highly enriched uranium for naval reactors, The Nonproliferation Review, James Martin Center for Nonproliferation, Spring 2001.
[199] D. Hinds, C. Maslak, Next-generation nuclear technology: The ESBWR American Nuclear Society, Nuclear News (2006) 35–40.
[200] J. Perkins, Fusion energy: the agony, the ecstasy, and alternatives, PhysicsWorld.com, November 1997, http://physicsworld.com/cws/article/print/1866. Retrieved on 23 April 2009.
[201] L.J.M.J. Blomen, M.N. Mugerwa, Fuel Cell Systems, Plenum, New York, 1993.
[202] U.S. Department of Energy, Office of Fossil Energy, Fuel Cell Handbook, fifth ed., National Energy Technology Laboratory, Morgantown, WV, 2000.
[203] R. Anahara, S. Yokokawa, M. Sakurai, Present status and future-prospects for fuel-cell power-systems, Proc. IEEE 81 (1993) 399–408.
[204] R. O'hayre, S.-W. Cha, W. Colella, F.B. Prinz, Fuel Cell Fundamentals, second ed., Wiley, New York, 2009.
[205] J. Larminie, Fuel Cell Systems Explained, second ed., Wiley, New York, USA, 2003.
[206] A.J. Appleby, Fuel cell, in: ninth ed., McGraw-Hill Encyclopedia of Science & Technology, vol. 7, McGraw-Hill, New York, 2002, pp. 549–552.
[207] M.W. Ellis, M.R. Von Spakovsky, D.J. Nelson, Fuel cell systems: efficient, flexible energy conversion for the 21st century, Proc. IEEE 89 (12) (2001) 1808–1818.
[208] S. Rahman, Fuel cell as a distributed generation technology, in: Proceedings of IEEE Power Engineering Society Meeting, vol. 1, 2001, pp. 551–552.
[209] L. Gao, Z. Jiang, R.A. Dougal, An actively controlled fuel cell/battery hybrid to meet pulsed power demands, J. Power Sour. 130 (1–2) (May 2004) 202–207.
[210] M. Uzunoglu, M.S. Alam, Dynamic modeling, design, and simulation of a combined PEM fuel cell and ultracapacitor systems for stand-alone residential applications, IEEE Trans. Energy Convers. 21 (3) (2006) 767–775.
[211] X. Yu, M.R. Starke, L.M. Tolbert, B. Ozpineci, Fuel cell power conditioning for electric power applications: a summary, IET Electric Power Appl. 1 (5) (2007) 643–656.

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24

Photovoltaic System Conversion

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24.1 Introduction

For many years, fossil fuels have been the primary source of energy. However, due to the limited supply, the rate of deployment of fossil fuels is more rapid than their rate of production, and hence, fossil fuels will eventually run out. Moreover, the threat of global climate change caused by carbon dioxide (CO_2) emissions from fossil fuels is one of the main reasons for the increasing consensus to reduce the consumption of such fuels. This reduction can be achieved by switching to renewable energy for many energy-requiring applications since it is "clean" and "green." Today, the global trend is to use a nondepletable clean source of energy for a healthier and greener environment to save the future generation. The most efficient and harmless energy source is probably solar energy, which is so technically straightforward to use in many applications. Almost, all renewable energy sources, except nuclear and geothermal, are the energy forms originating from the solar energy.

Solar energy is considered one of the most promising energy sources due to its infinite power. Thus, modern solar technologies have been penetrating the market at faster rates, and photovoltaic (PV) technology that has the greatest impact, not because of the amount of electricity it produces but because photovoltaic cells—working silently, not polluting—can generate electricity wherever the sun shines, even in places where no other form of electricity can be obtained. PV is a combination of the Greek word for light and the name of the physicist Alessandro Volta. PV is the direct conversion of sunlight into electricity by means of solar cells.

This chapter will highlight in brief how solar cells produce electricity and will discuss in detail the various techniques available to track the sun in order to maximize the output power generated by the PV array. Moreover, the components required to operate grid-connected and stand-alone PV systems will be described. Additionally, the affecting factors and design issues of PV systems will be presented.

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24.2 Solar Cell Characteristics

Solar cells are composed of various semiconductor materials that become electrically conductive when supplied with heat or light. The majority of the first-generation solar cells produced are composed of silicon (Si), which exists in sufficient quantities. However, more than 95% of these cells have power conversion efficiency about 17%, whereas solar cells that developed over the last decade in laboratory environment have efficiency as high as 31%. All technologies related to capturing solar energy to be used as direct electricity generator are described as photovoltaic technology, which is subdivided into crystalline, thin film, and nanotechnology.

Doping technique is used to obtain an excess of positive charge carriers (p-type) or a surplus of negative charge carriers (n-type). When two layers of different doping are in contact, then a p-n junction is formed on the boundary.

An internal electric field is built up causing the separation of charge carriers released by light, freeing electrons within the electric field proximity, which then pull the electrons from the p-side to the n-side (Fig. 24.1). The primary solar cell equivalent circuit (Fig. 24.2) contains a current source with a parallel diode, in addition to parasitic series (R_s, normally small) and shunt (R_{sh}) resistances (relatively large). R_s is mainly affected by the factors such as the bulk resistance of the semiconductor material, metallic contacts, and interconnections, whereas R_{sh} is affected mainly by the p-n junction nonidealities and impurities near the junction.

A simplified equivalent circuit is shown in Fig. 24.3.

The diode current is given by the Shockley equation:

$$I_D = I_0 \left[\exp\left(\frac{qV}{nkT}\right) - 1 \right] \tag{24.1}$$

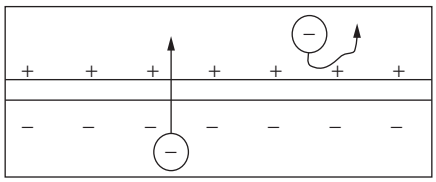


FIGURE 24.1 Effect of the electric field in a PV cell [1].

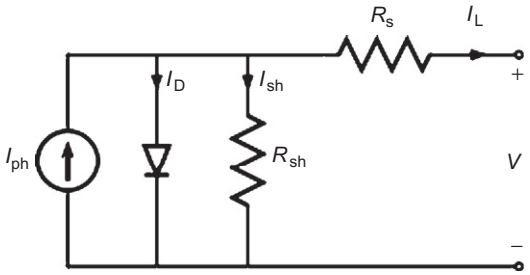


FIGURE 24.2 Solar cell equivalent circuit.

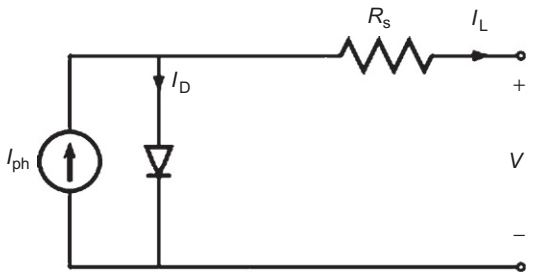


FIGURE 24.3 Model for a PV cell.

where I_0 is the reverse saturation current, q is the charge carrier, k is the Boltzmann constant, T is the cell temperature, and n is the ideality factor.

The PV module has two limiting components (Fig. 24.3): open-circuit voltage (V_{OC}) and short-circuit current (I_{sc}). To determine I_{sc}, set $V = 0$ and $I_{sc} = I_{ph}$, and this value changes proportionally to the cell irradiance. To determine V_{OC}, set the cell current $I_L = 0$; hence,

$$V_{OC} = \frac{nkT}{q} \ln\left[\frac{I}{I_0}\right] \tag{24.2}$$

The PV module can also be characterized by the maximum point when the product (V_{mp} (voltage, where power is maximum) $\times I_{mp}$ (current, where power is maximum)) is at its maximum value. The maximum power output is derived by

$$\frac{d(V \times I)}{dt} = 0 \tag{24.3}$$

and

$$V_{mp} = V_{OC} - \frac{kT}{q} \ln\left[\frac{V_{mp}}{nkT/q} + 1\right] \tag{24.4}$$

A PV module is normally rated using its W_p, which is normally 1 kW/m^2 under standard test conditions (STC), which defines the PV performance at an incident sunlight of 1000 W/m^2, a cell temperature of 25°C (77°F), and an air mass (AM) of 1.5. The product ($V_{mp} \times I_{mp}$) is related to the product generated by ($V_{OC} \times I_{SC}$) by a fill factor (FF) that is a measure of the junction quality and series resistance, and it is given by

$$FF = \frac{V_{mp} \times I_{mp}}{V_{OC} \times I_{SC}} \tag{24.5}$$

The closer the FF is to unity, the higher the quality of the PV module.

Finally, the last and most important factor of merit for a PV module is its efficiency (η), which is defined as

$$\eta = \frac{FF \times V_{OC} \times L_{OC}}{P_{in}} \tag{24.6}$$

P_{in} represents the incident power depending on the light spectrum incident on the PV cell.

To achieve the desired voltage and current levels, solar cells are connected in series (N_s) and parallel (N_p) combinations forming a PV module. The PV parameters are then affected as shown below:

$$I_{\text{ph total}} = N_p I_{\text{ph}} \tag{24.7}$$

$$I_{0\,\text{total}} = N_p I_0 \tag{24.8}$$

$$n_{\text{total}} = N_s n \tag{24.9}$$

$$R_{s\,\text{total}} = \frac{N_s}{N_p} R_s \tag{24.10}$$

This model is shown in Fig. 24.4.

In order to obtain the appropriate voltages and outputs for different applications, single solar cells are interconnected in series (for larger voltage) and in parallel (for larger current) to form the photovoltaic module. Then, several of these modules are connected to each other to form the photovoltaic array. This array is then fitted with aluminum or stainless steel frame and covered with transparent glass on the front side (Fig. 24.5).

The voltage generated by the array depends primarily on the design and materials of the cell, whereas the electric current depends primarily on the incident solar irradiance and the cell area. This current fluctuates since the path of the sun varies dramatically over the year, with winter and summer seasons being the two extreme excursions. The elevation angle of the sun ($\theta_{\text{sun}}^{\text{elevation}}$) is expressed in degrees above the horizon. Azimuth angle ($\phi_{\text{sun}}^{\text{azimuth}}$) of the sun is expressed in degrees from true north. Zenith angle ($\theta_{\text{sun}}^{\text{zenith}}$) of the sun equals 90 degrees less than the elevation angle of the sun, or

$$\theta_{\text{sun}}^{\text{zenith}} = 90\,\text{degrees} - \theta_{\text{sun}}^{\text{elevation}} \tag{24.11}$$

Azimuth, zenith, and elevation angles are illustrated in Fig. 24.6.

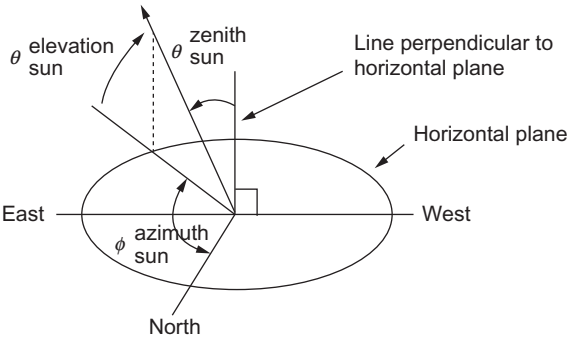


FIGURE 24.6 Azimuth, zenith, and elevation angles of a vector pointed toward the sun.

The output from a typical solar cell that is exposed to the sun, therefore, increases from zero at sunrise to a maximum at midday and then falls again to zero at dusk. The radiation of the sun varies when reaching the surface of the earth due to absorption and scattering effect in the earth's atmosphere. PV system designers require the estimate of the insolation expected to fall on a randomly tilted surface and hence need a good evaluation of global radiation on a horizontal surface, horizontal direct, and diffuse components, in order to estimate the amount of irradiation striking a tilted plane.

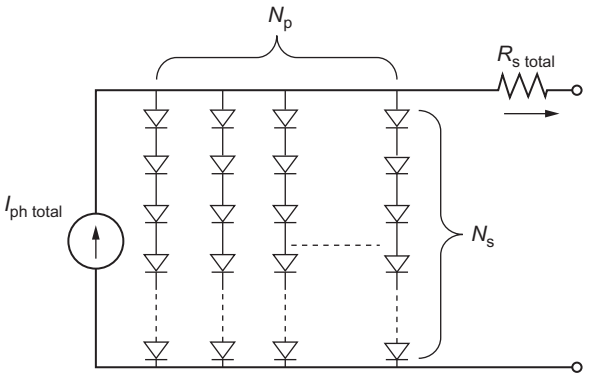


FIGURE 24.4 PV module circuit model.

24.3 Photovoltaic Technology Operation

Photovoltaic technology is used to produce electricity in areas where power lines do not reach. In developing countries, it helps improving living conditions in rural areas, especially in health care, education, and agriculture. In industrialized countries, such technology has been used extensively and integrated with the utility grid.

Photovoltaic arrays are usually mounted in a fixed position and tilted toward the south to optimize the noontime and the daily energy production. The orientation of fixed panel should

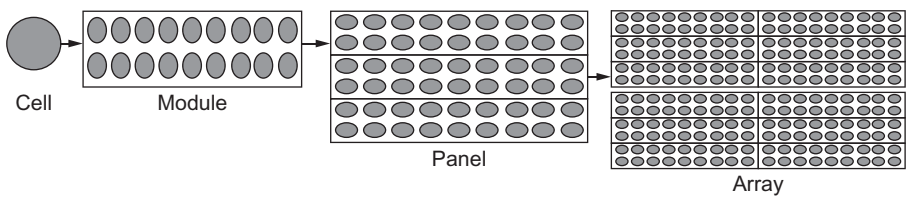


FIGURE 24.5 Photovoltaic cells, modules, panels, and array.

be carefully chosen to capture the most energy for the season or for a year. Photovoltaic arrays have an optimum operating point called the maximum power point (MPP) as shown in Fig. 24.7.

It is noted that power increases as voltage increases, reaching a peak value and decreases as the resistance increases to a point where current drops off. According to the maximum power transfer theory, this is the point where the load is matched to the solar panel's resistance at a certain level of temperature and insolation. The *I-V* curve changes as the temperature and insolation levels change as shown in Fig. 24.8, and thus, the MPP will vary accordingly.

It is shown that the open-circuit voltage increases logarithmically, while the short-circuit current increases linearly as the isolation level increases. Moreover, increasing the temperature of the cell decreases the open-circuit voltage and increases slightly the short-circuit current, causing a reduction in the efficiency of the cell.

The PV panels, usually mounted on the roof or at a near open area, are fixed to face the sun at an angle matching the country's latitude. If possible, seasonal adjustment of the module's direction toward the sun is done manually. Since solar power technology is relatively expensive, it is important to operate panels at their maximum power conditions. However, to collect as much solar radiation as possible, it is more convenient and efficient to use a sun tracking mechanism causing the module's surface to track the sun throughout the day.

The tracking can be along either one axis or two axes, whereby double axis tracking provides a higher power output. The energy yield can be thus increased by about 20%–30% depending on the seasonal climate and geographic location. Although some claim that a fixed system costs less and requires almost no maintenance, different tracking mechanisms that utilized to control the orientation of the PV panels have proved their superiority over fixed systems in terms of converted power efficiency.

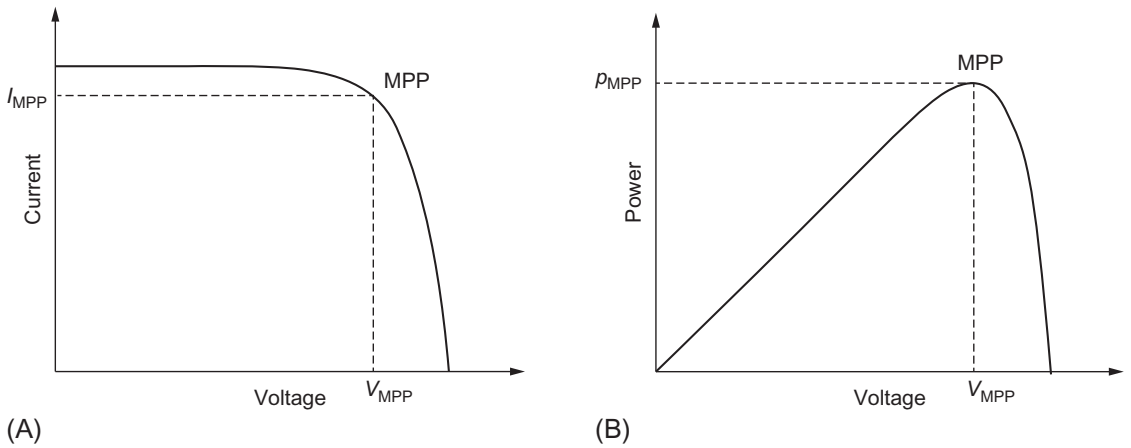


FIGURE 24.7 Typical PV module curves: (A) *I-V* characteristic of a solar cell showing maximum power point (MPP) and (B) *P-V* characteristic of a solar cell showing MPP.

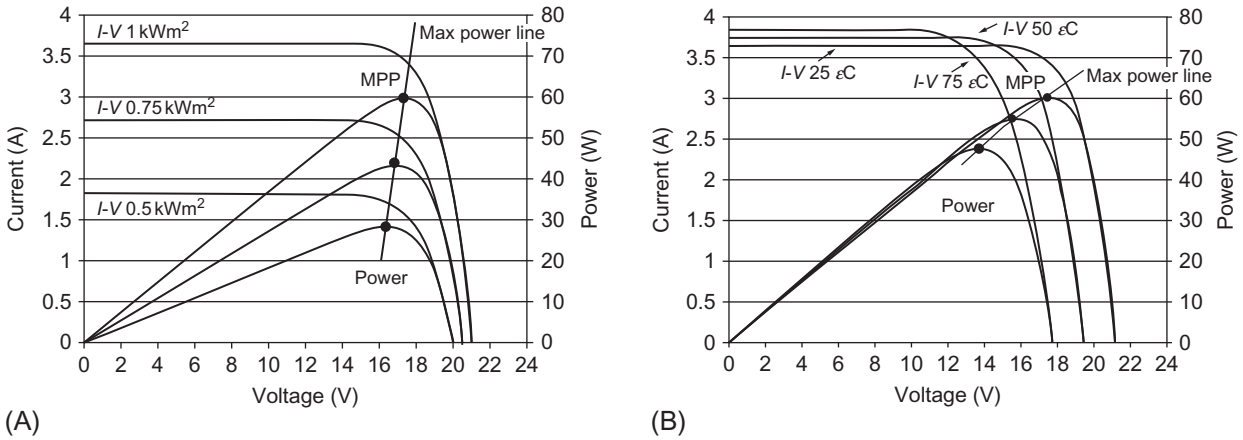


FIGURE 24.8 PV module characteristics: (A) PV panel insolation and (B) PV panel temperature.

To get maximum power from the PV panel at the prevailing temperature and insolation conditions, either the operating voltage or current should be controlled by a maximum power point tracker (MPPT) that should meet the following conditions:

- Operate the PV system close to the MPP irrespective of the atmospheric changes.
- Have low-cost and high-conversion efficiency.
- Provide an output interface compatible with the battery charging requirement.

24.4 Maximum Power Point Tracking Components

The MPPT increases the energy that can be transferred from the array to an electric system. The main function is to adjust the panel's output voltage to supply the maximum energy to the load. Most current designs consist of three basic components: switch-mode DC-DC converter, control system, and tracking component.

The switch-mode converter is the core of the entire supply because the energy drawn, stored as magnetic energy, is released at different potential levels. By setting up the switch-mode section in various topologies such as buck or boost converter, voltage converters are designed providing a fixed input voltage or current, which correspond to the maximum power point, allowing the output resistance to match the battery. To achieve the above-stated mechanism, a controller is essential to continuously monitor the PV system and ensure its operation at the PV maximum power point by tracking this MPP. The controller's aim is to continuously measure the voltage and current values generated from the PV and compare them with certain threshold values in order to apply either voltage controlled method or power feedback control.

24.4.1 Voltage Feedback Control

With the PV array terminal voltage being the controlled variable, voltage feedback controller forces the PV array to operate at its MPP by changing the array terminal voltage and neglecting the variation in the temperature and insolation level.

24.4.2 Power Feedback Control

In this method, the power delivered to the load is the controlled variable. To achieve maximum power, dp/dv should be zero. This control scheme is not affected by the characteristics of the PV array, yet it increases power to the load and not power from the PV array. Factors such as fast shadows may cause trackers to lose the MPP momentarily. It is very critical to ensure that the time lost in seeking MPP again, which equates the energy lost while the array is off power point, is very short. On the other hand, if lighting conditions do change, the tracker needs to respond within a short amount of time to the change avoiding energy loss. Therefore, the controller's most important feature is its capability to quickly adjust the system to operate back at the MPPT.

24.5 MPPT Controlling Algorithms

Several proposed algorithms to accomplish MPPT are described in the following sections.

24.5.1 Perturb and Observe

The perturb and observe (PAO) method has a simple feedback structure and few measured parameters. It operates by periodically perturbing (i.e., incrementing or decrementing) the duty cycle while controlling the array current as shown in Fig. 24.9 and comparing the PV output power with that of the previous perturbation cycle. It measures the derivative of power Δp and the derivative of voltage Δv to determine the movement of the operating point. If the perturbation leads to an increase (or decrease) in array power, the subsequent perturbation is made in the same (or opposite) direction. This cost-effective technique can be easily implemented and is characterized by continuously tracking and very efficiently extracting the maximum power from PV. However, such method may fail under rapidly changing atmospheric conditions due to its slow tracking speed.

24.5.2 Incremental Conductance Technique

The incremental conductance technique (ICT) process based on the fact that the derivative of the power with respect to the voltage (dp/dv) vanishes at the MPP because it is the maximum point on the curve as shown in Fig. 24.10.

The ICT algorithm detects the MPP by comparing di/dv with $\frac{-I}{V}$ till it attains the voltage operating point at which the incremental conductance is equal to the source conductance. The algorithm starts by measuring the present values of the I and V and then uses the corresponding stored value (I_b and V_b)

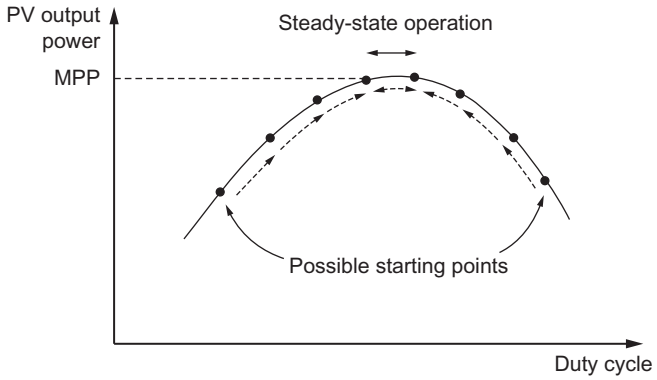


FIGURE 24.9 PAO technique.

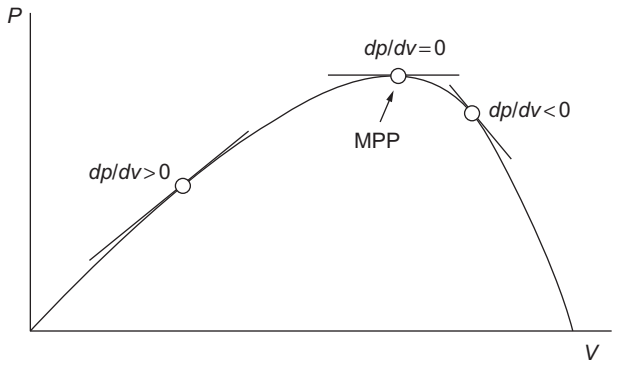


FIGURE 24.10 The slope "conductance" of the *P-V* curve.

measured during the preceding cycle to calculate the incremental changes as $dI = I - I_b$ and $dV = V - V_b$. Based on the result obtained, the control reference signal V_{ref} will be adjusted in order to move the array voltage toward the MPP voltage. At the MPP, $di/dv = \frac{-I}{V}$, no control action is needed; therefore, the adjustment stage will be bypassed, and the algorithm will update the stored parameters at the end of the cycle. In order to detect any changes in weather conditions, the algorithm detects whether a control action took place when the array was operating at the previous cycle MPP ($dv = 0$). This technique is accurate and well suited for rapid changes in atmospheric conditions; however, because the increment size approach is used to determine how fast the system is responding, ICT requires precise calculations of both instantaneous and increasing conductance.

24.5.3 Constant Reference

One very common MPPT technique is to compare the PV array voltage (or current) with a constant reference voltage (or current), which corresponds to the PV voltage (or current) at the maximum power point, under specific atmospheric conditions. The resulting difference signal (error signal) is used to drive a power conditioner, which interfaces the PV array to the load. Although the implementation of this method is simple, the method itself is not very accurate because it does not consider the effects of temperature and irradiation variations in addition to the difficulty in choosing the optimum point.

24.5.4 Current-Based Maximum Power Point Tracker

Current-based maximum power point tracker (CMPPT) is another MPPT technique that exists. Employed numerical methods show a linear dependence between the "cell currents corresponding to maximum power" and the "cell short-circuit currents." The current I_{MPP} operating at the MPP is calculated using the following equation:

$$I_{MPP} = M_C I_{SC} \tag{24.12}$$

where M_C is the "current factor" that differs from one panel to another and is affected by the panel surface conditions, especially if partial shading covers the panel. Although this method is easy to implement, an additional switch is added to the power converter to periodically short the PV array, increase the cost, and reduce the output power. This method also suffers from a major drawback due to periodic tuning requirement.

24.5.5 Voltage-Based Maximum Power Point Tracker

Similar to the above-mentioned method, voltage-based maximum power tracking (VMPPT) technique can also be applied. The MPP operating voltage is calculated directly from V_{OC}:

$$V_{MPP} = M_V V_{OC} \tag{24.13}$$

where M_V is the "voltage factor." The open-circuit voltage V_{OC} is sampled by an analog sampler, and then, V_{MPP} is calculated by Eq. (24.13). This operating V_{MPP} voltage is the reference voltage for the voltage control loop as shown in Fig. 24.11. This method always "results in a considerable power error because the output voltage of the PV module only follows the unchanged reference voltage during one sampling period" [2]. Albeit the implementation of this procedure is simple, it endures several disadvantages such as momentarily power converter shutdown causing power loss. Furthermore, such process depends greatly on the *I-V* characteristics and requires periodic tuning.

Other researchers argue that these two practices are considered to be "fast, practical, and powerful methods for MPP estimation of PV generators under all insolation and temperature conditions" [3].

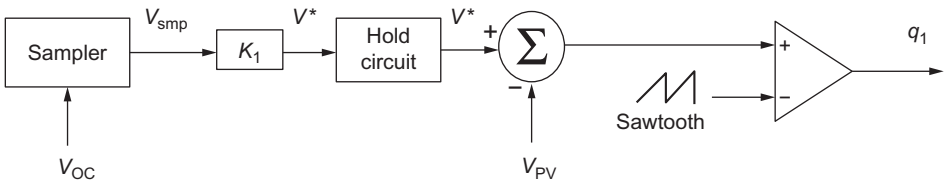


FIGURE 24.11 The conventional MPPT controller using open-circuit voltage V_{OC}.

24.5.6 Other Methods

Automated techniques such as Fibonacci line search, ripple correlation control method, neural network, and fuzzy logic have also been introduced for MPPT. In order to generate a clear understanding in determining the advantages and disadvantages of each algorithm, a comprehensive experimental comparison between different MPPT algorithms was made and run for the same PV setup at South Dakota State University, and results showed that the ICT method has the highest efficiency of 98% in terms of power extracted from the PV array, the PAO technique has the efficiency of 96.5%, and finally, the constant voltage method has the efficiency of 88%.

The ICT method provided good performance under rapidly changing weather conditions and provided the highest tracking efficiency, although four sensors were required to perform the measurements for computations and decision-making. If the system required more conversion time in tracking the MPP, a large amount of power loss would occur. On the contrary, under perturb and observe method, losses are reduced if the sampling and execution speed were increased. The main benefit of this procedure is that only two sensors are required, which resulted in the reduction of hardware requirements and cost.

24.6 Grid-Connected Photovoltaic System

Grid-connected photovoltaic systems are composed of PV arrays connected to the grid through a power conditioning unit (PCU) and are designed to operate in parallel with the electric utility grid. The power conditioning unit may include the MPPT, the inverter, the grid interface, and the control system needed for efficient system performance. There are two general types of electric designs for PV power systems: systems that interact with the utility power grid as shown in Fig. 24.12A and have no battery backup capability and systems that interact and include battery backup as well as shown in Fig. 24.12B. The latter type of system incorporates energy storage in the form of a battery to keep "critical load" circuits operating during utility outage. When an outage occurs, the unit disconnects from the utility and powers specific circuits of the load. If the outage occurs in daylight, the PV array is able to assist the load in supplying the loads.

The major component in both systems is the DC-AC inverter or also called the power conditioning unit (PCU). The inverter is the key to the successful operation of the system, but it is also the most complex hardware. The inverter requirements include operation over a wide range of voltages and currents and

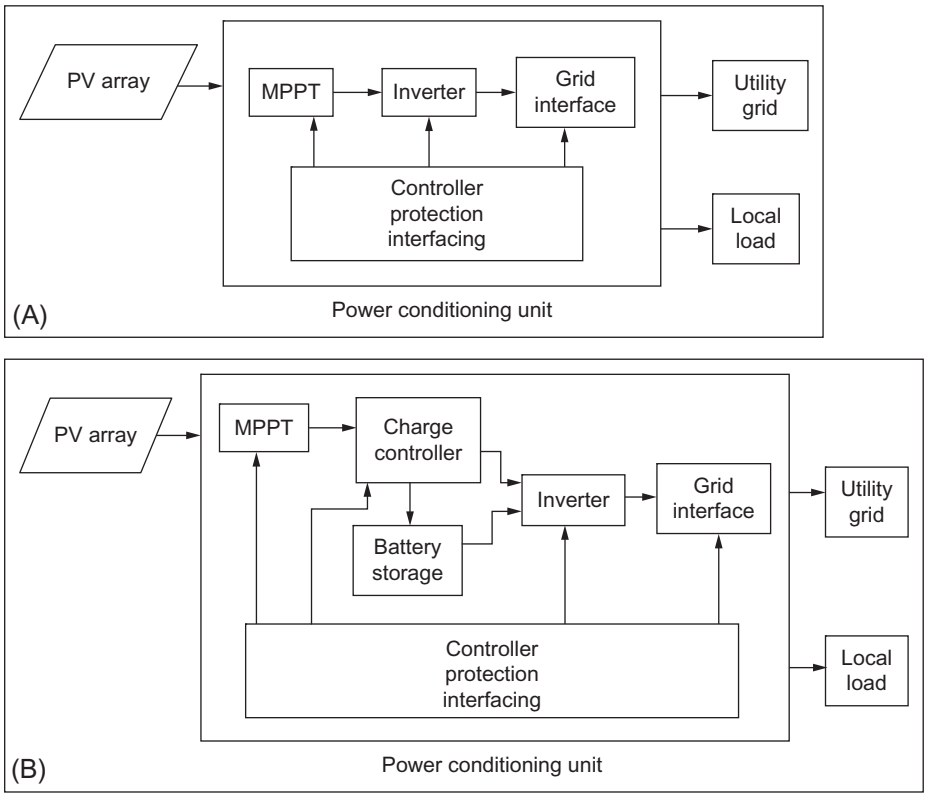


FIGURE 24.12 Block diagrams of grid-connected PV system: (A) without battery backup and (B) with battery storage.

regulated output voltage and frequency while providing AC power with good power quality that includes low total harmonic distortion and high power factor, in addition to highest possible efficiency for all solar irradiance levels. Inverters can be used in a centralized connection (Fig. 24.13A) for the whole array of PV, each PV module string is connected to a single inverter (Fig. 24.13B), and a single PV module is connected to a named microinverter (Fig. 24.13C).

The first circuit handled all the power, and the maximum power point is difficult to follow if there is voltage/current mismatching at the PV modules. The second option is more efficient than the first one since it minimizes the losses due to voltage/current mismatching and it enhances its modularity capability. The last circuit may perform a good tracking since each PV module is controlled independently; however, more stages and components are required.

For the last years, researchers have been working on developing different inverter topologies. The evolution of solid-state devices such as metal-oxide-semiconductor field-effect transistors (MOSFETs), insulated-gate bipolar transistors (IGBTs), microprocessors, and PWM-integrated circuits has allowed improvements on the inverter. Some research is being carried to ensure quality control, reliability, high efficiency, and lower cost since inverters are the key for a sustainable photovoltaic market.

24.6.1 Isolated Converters

For safety reasons, not only both the grid neutral line and the chassis of the PV modules must be grounded, but also the PCU may provide galvanic isolation. The first option is to place the isolation on the grid side, by using an AC low-frequency transformer (Fig. 24.14A), which makes the system big, heavy, and bulky. The second option is to include the isolation on the DC side, after the PV array, by using a high-frequency transformer (Fig. 24.14B), which is smaller and costs less than an AC transformer.

These options have different drawbacks: low efficiency, the size and weight are compromised, and the cost should be high due to the inclusion of the isolation. Therefore, researchers are developing the PCUs without isolation.

24.6.2 Transformerless Converters

A costless PCU is obtained if the isolation is removed, but then, a common-mode resonant circuit appears due to the grounding cable, which includes the filter, the inverter, the grid impedance, and the PV parasitic capacitance. This common mode generates a leakage current ($i_{leakage}$) that circulates through parasitic capacitances in PV array to the ground, as shown in Fig. 24.15. The common-mode voltage, the modulation

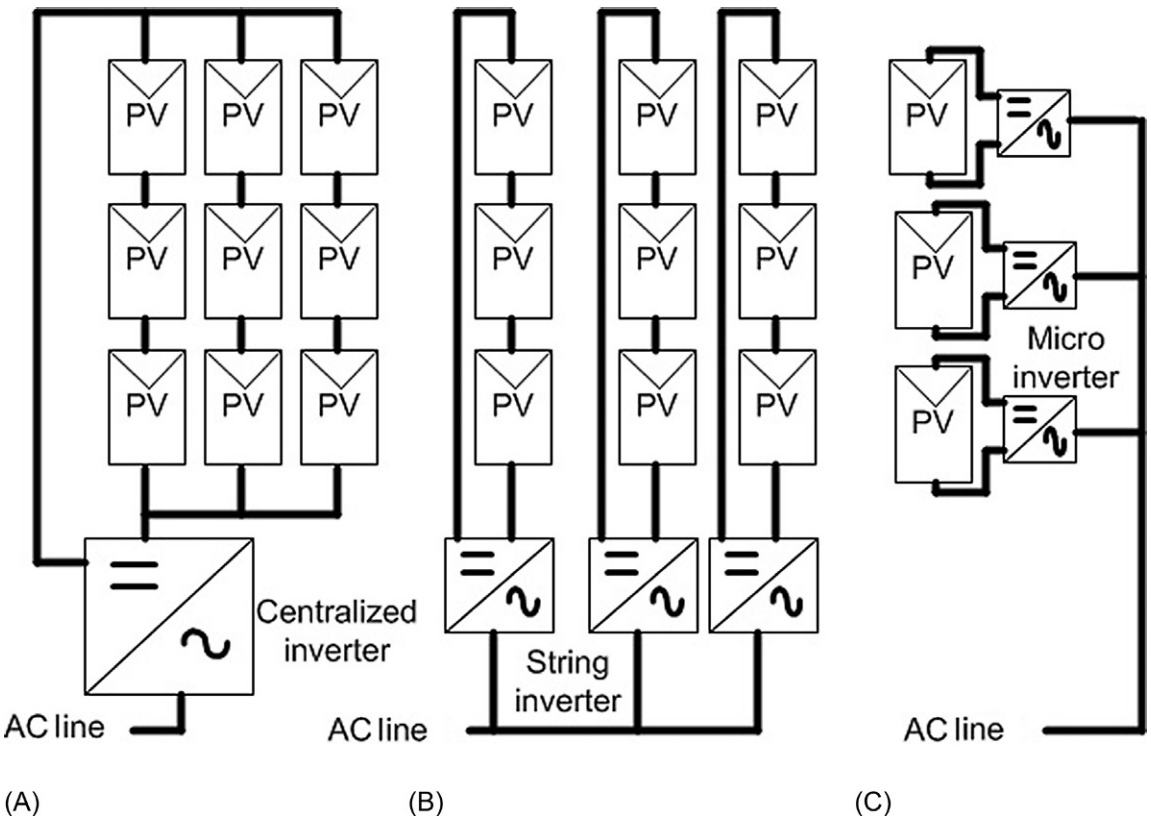


FIGURE 24.13 Grid-connected PV system: (A) centralized, (B) string connection, and (C) microinverter.

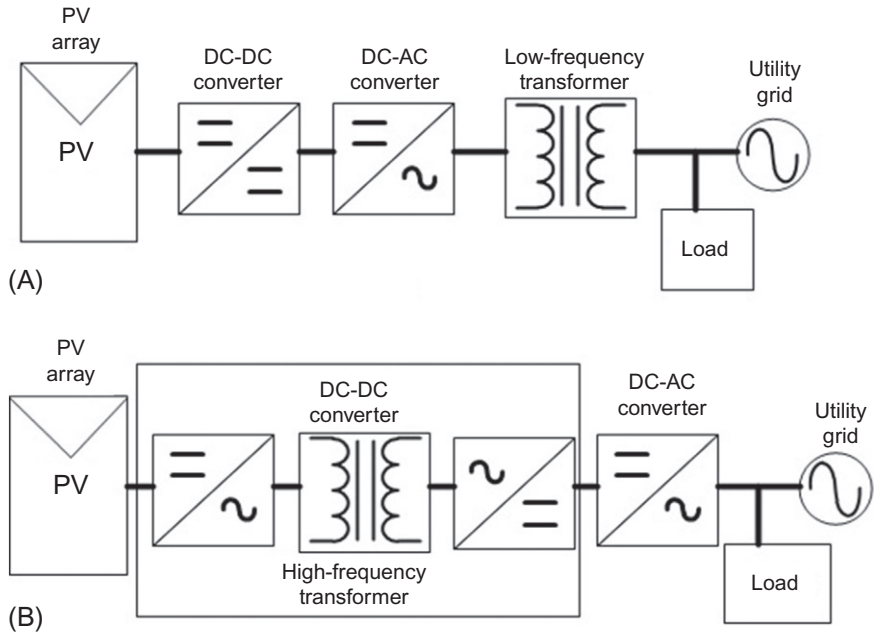


FIGURE 24.14 Grid-connected isolated PV system: (A) low-frequency transformer and (B) high-frequency transformer.

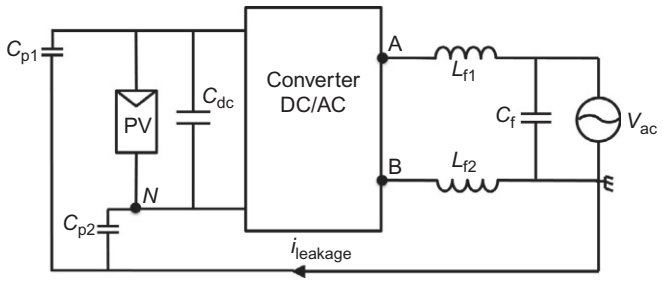


FIGURE 24.15 Block diagram to illustrate the leakage current.

strategy, and the value of the parasitic capacitance greatly affect the value of the leakage current.

The parasitic capacitance value depends on many factors such as the PV panel and frame structure, the surface of cells, the distance between cells, the weather conditions, and the type of EMC filter. In order to reduce this parasitic current, different PCUs have been reported: H-5, HERIC, and common-mode inverters, among others.

A. H-5 inverter

This DC/AC converter is similar to the traditional full-bridge inverter topology, where the upper switches operate at grid frequency and the lower ones work at a high frequency. It has incorporated an extra switch S_5 on the DC side that operates in both semicycles at a high frequency (Fig. 24.16A). The main characteristic of this configuration is that the PV array is decoupled from the grid when this extra switch is turned off.

Normally during active states, the current flows during freewheeling modes through two switches, but in active vectors, the current flows through three switches causing conduction losses, which become a disadvantage.

B. Heric inverter

This topology combines advantages from two alternatives: the three-level output voltage of the unipolar PWM, besides the reduced common-mode voltage as in the case of bipolar PWM. It consists of a full-bridge inverter plus two additional switches, as illustrated in Fig. 24.16B. Each group of diagonal switches of the full bridge operates at a high frequency during the half wave of the grid. One of the two additional switches is turned on during the half wave of the grid. S_5 or S_6 is used when the disconnection occurs between the grid and PV array, which reduces the leakage current. The main drawback of this topology is the pair of additional semiconductors.

C. Common mode converter

There are different schemes for this configuration; the main idea is that the neutral terminal of the grid is connected straight to the negative of the PV array. Shown in Fig. 24.16C is an alternative; this topology is composed of two power MOSFETs (S_1 and S_2), and just a single device is conducting in each switching state. The converter includes two capacitors and three inductors (C_f, C_{dc} and L_1, L_2, L_f).

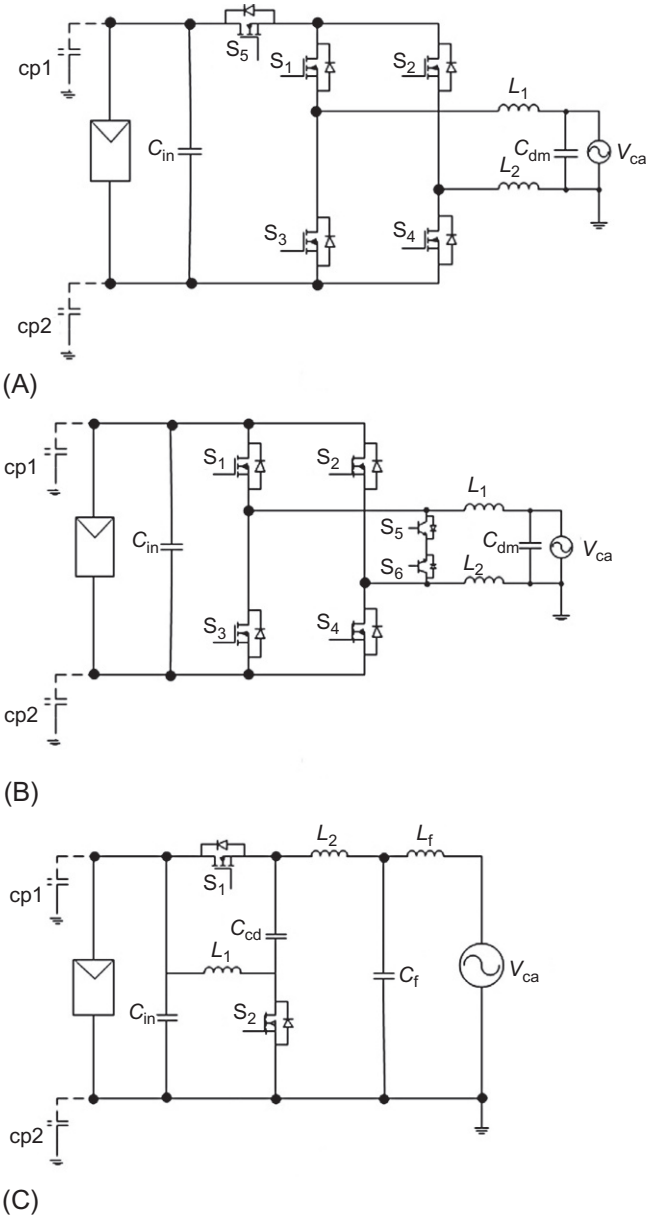


FIGURE 24.16 Transformerless inverters for PV systems: (A) H-5, (B) HERIC, (C) a common-mode topology.

Since the negative of the PV array is connected straight to the neutral line of the grid, the ground leakage current is very low, while the applied voltage to the parasitic capacitance is maintained almost constant.

24.6.3 Grid Synchronization

PV grid-connected converters need a phase and frequency tracking system to provide a reference signal in order to synchronize it with the grid voltage. It is critical in a synchronization system with a high degree of immunity to harmonics, unbalances, and power system disturbances as sags and swells.

There are several state-of-the-art techniques in detecting the phase angle of the grid voltages. A particular easy and simple to implement is the voltage zero-crossing technique. However, voltage sags and harmonics can disturb greatly the output signal. Digital schemes have improved zero-crossing method using filtering techniques: extended Kalman filters, low-pass filters, space vector, and recursive weighted least-square estimation.

Phase-locked-loop (PLL)-based algorithms can successfully reject harmonics, notches, voltage sags, and swells. At the same time, PLL algorithms provide the estimation of time-varying fundamental parameters from the distorted grid voltage waveform. Another representative technique in grid synchronization is the second-order generalized integrator frequency-locked loop (SOGI-FLL). SOGI-FLL-based techniques estimate important grid parameters for single- and three-phase systems, reducing undesirable frequency swing during phase-angle jumps.

24.6.4 Islanding Mode

For security reasons, the PV grid-connected inverters must be disconnected from the grid when the utility is disabled or out of operation. Once the grid is out, the PV system is operating in islanding mode, and this mode must be detected in order to shut off the system and separate it from the utility.

The islanding mode detector may be classified in local or remote techniques. The local techniques are based on the measurements of physical parameters at the common point of coupling, like voltage and current. The remote techniques are based on communication infrastructure between the electricity provider and the PV system. The local techniques may be subclassified in passive and active methods. These methods are briefly described as follows.

A. Passive methods

The passive method is based on not only the measurement of variables as voltage and current at common point of coupling but also obtaining parameters like *rms* voltage, *rms* current, frequency, phase, and total harmonic distortion. It established the range for the normal operation, and once the system is out of the specified range, the PV system is considered that is operating in islanding mode.

B. Active methods

The active methods also are based on the measurements of voltage and current, but additionally, these methods inject perturbations in order to accelerate the fastness of the detection. There are many methods.

One method is called the shift active frequency, during a small time, the injected current is zero (no sinusoidal current), and when the system is in islanding mode, the output frequency is naturally changed, and this will be detected fast.

A second method is called sandia voltage shift; in this scheme, a positive feedback is considered in the current loop; this loop tries to produce an instability at the

output voltage. If the system is operated normally, this loop will not cause a major trouble since the stability is determined by the grid. However, when the islanding mode occurs, this loop will produce an instability at the output voltage, and this is detected fast as an under or overvoltage.

24.7 Stand-Alone Photovoltaic System

The main advantage of PV systems is their flexibility to be implemented in remote locations where grid connection is either impossible or very expensive to execute. Such systems are called stand-alone PV systems and are described in this section.

Stand-alone photovoltaic systems are usually a utility power alternative. They generally include solar charging modules, storage batteries, and controls or regulators as shown in Fig. 24.17. Ground- or roof-mounted systems will require a mounting structure, and if AC power is desired, an inverter is also required. In many stand-alone PV systems, batteries are used for energy storage as they may account for up to 40% of the overall stand-alone PV system cost over its lifetime.

These batteries cause losses in the PV system due to limited availability of time and energy to recharge the battery in addition to the insufficient battery maintenance. Hence, a charge controller is then used to control the system and prevent the battery from overcharging and overdischarging. Overcharging shortens the battery life and may cause gassing, while undercharging may lead to sulfation and stratification, which result in the reduction in battery effectiveness and lifetime.

Batteries are often used in PV systems for storing energy produced by the PV array during daytime and supplying it to electric loads as needed (during nighttime or cloudy weather). Moreover, batteries are also needed in the tracker systems to operate at MPP in order to provide electric loads with stable voltages. Nearly, most of the batteries used in PV systems are deep-cycle lead-acid batteries. These batteries have thicker lead plates that make them tolerate deep discharges. The thicker the lead plates, the longer the lifespan of the batteries. The heavier the battery for a given group size, the thicker the plates and the better the battery will tolerate deep discharges.

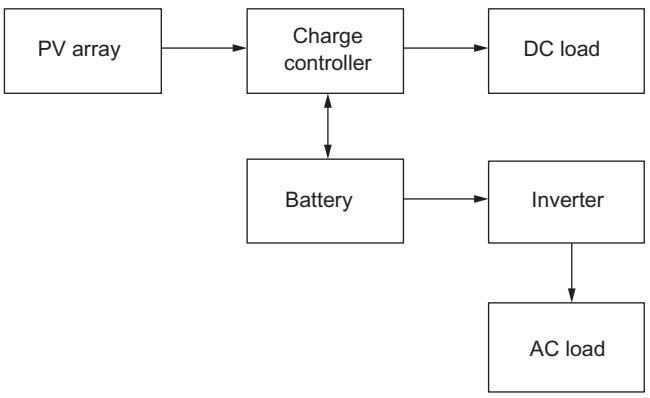


FIGURE 24.17 Diagram of stand-alone PV system with battery storage power DC and AC loads.

All deep-cycle batteries are rated in ampere-hour (AH) capacity, a quantity of the amount of usable energy it can store at nominal voltage. A good charge rate is approximately 10% of the total capacity of the battery per hour. This will reduce the electrolyte losses and the damage to the plates. A PV system may have to be sized to store a sufficient amount of power in the batteries to meet power demand during several days of cloudy weather, known as "days of autonomy." The Institute of Electrical and Electronics Engineers (IEEE) has set several guidelines and standards for sizing lead-acid batteries (IEEE Std 1013–1990), for selecting, charging, and testing in stand-alone PV systems (IEEE Std 1361–2003), and for installing and maintaining them (IEEE Std 937–2007).

Nickel-cadmium batteries are also used for PV stand-alone systems but are often expensive. However, their main advantage is they are not affected by temperature as other battery types, hence mostly recommended for industrial or commercial applications in cold locations. IEEE has also drafted some guidelines for installation and maintenance (IEEE Std 1145–1999).

To extend battery's lifetime and for efficient system's operation, a charge controller is needed to regulate the flow of electricity from the PV modules to the battery and the load. The controller keeps the battery fully charged without overcharging it. Many controllers have the ability to sense the excess of electricity drawn from batteries to the load and stop the flow until sufficient charge is restored to the batteries. The latter can greatly extend the battery's lifetime. However, controllers in the stand-alone photovoltaic system are more complex devices that depend on battery state of charge, which in turn depends on many factors and is difficult to measure. The controller must be sized to handle the maximum current produced. Several characteristics should be considered before selecting a controller such as adjustable set points including high-voltage and low-voltage disconnects, temperature compensation, low-voltage warning, and reverse current protection. Moreover, the controller should ensure that no current flows from the battery to the array at night.

24.7.1 Power Converters

There are different power converters for stand-alone systems, and they have different operating modes. They may be summarized as described below:

- Power delivered from the main voltage source

  The power converter may be able to deliver energy directly to the load form the main voltage source, without the use of the battery set. This mode in some converters is not considered, and the load is just fed by the battery set.

- Not energy available from the main voltage source
  It is possible to not have energy due to weather conditions, and then, the battery will deliver the energy to the load. This may be through a direct connection or by considering a power converter.
- Power delivered from main source and battery set
  When the photovoltaic system cannot provide all required energy by the load, but still there is available energy, then the system could be operated to demand energy from both sources: the photovoltaic system and the battery set. Not all the power converters may operate in this form.
- Charging the battery set
  Once the battery is empty, a charging mode must be considered. The battery is fed by the photovoltaic system through a power converter. This mode occurs if there is energy available from the renewable source.
- No energy available from any source
  It is possible to not have energy due to weather conditions and also when the battery is discharged; then, the system is turned off, until the system has the energy to operate.

For stand-alone applications, it is possible to consider more than one solar panel, besides the battery set. Then, power converter with multiple inputs should be considered. One of the most important issues in these converters is the power administration, that is, to determine when each source should be used, in order to have the best operation of the system.

24.8 Factors Affecting PV Output

PV systems produce power in proportion to the intensity of sunlight striking the solar array surface. Thus, there are some factors that affect the overall output of the PV system and are discussed below.

24.8.1 Temperature

The output power of a PV system decreases as the module temperature increases. An increasing cell temperature at constant irradiance causes a reduction in V_{OC} at a rate approximately of 2–2.5 mV/C. The short-circuit current, on the other hand, remains nearly constant. Since V_{mp} is normally about 80% of V_{OC} and the cells are series connected, it is important the combined effect on cell performance merit careful consideration. The temperature effect on monocrystalline solar cells is higher than polycrystalline silicon and thin-film solar cells; operating at temperatures higher than 25°C may reduce maximum output power by 15% in monocrystalline solar cells and by 5% in thin-film solar cells.

24.8.2 Dirt and Dust

Dirt and dust can accumulate on the solar module surface, also known as soiling. The soil layer blocks the sunlight and reduces the output power. Estimation of soiling loss is difficult due to the variations in the soil type, geographic locations, and climatic conditions. In general, there are two types of soil shading on PV modules, namely, hard shading and soft shading. Hard shading occurs when a solid such as accumulated dust blocks the sunlight in a clear and definable shape. On the other hand, soft shading takes place when some particles such as smog or some dust reduce the overall intensity of the solar irradiance.

For hard shading, the performance of the PV module depends on the portions shaded of the PV module. Soft shading affects the current of the PV module, but the voltage remains the same. To get better performance, the solar module surface must be clean. Manually hand cleaning element by water with detergent is suggested one time per week on the panel.

24.8.3 DC-AC Conversion

Because the power from the PV array is converted back to AC as shown earlier, some power is being lost in the conversion process, in addition to losses in the wiring. Common inverters used have peak efficiencies of about 90%–98%. Recently, the new devices based on gallium nitride (GaN) and silicon carbide (SiC) are recommended for these power converters.

24.9 PV System Design

The goal for a solar direct electricity generation system or photovoltaic system is to provide high-quality, reliable, and green electric power. Then, some suggestions may be followed.

24.9.1 Criteria for a Quality PV System

The criteria for quality PV system are as follows:

- Be properly sized and oriented to provide electric power and energy
- Good control circuit to reduce electric losses, overcurrent protection, switches, and inverters
- Good charge controller and battery management system, if the system contains batteries

24.9.2 Design Procedures

The first task in designing a PV system is to estimate the system's load. This is achieved by defining the power demand of all loads, the number of hours used per day, and the operating voltage. From the load ampere-hours and the given operating voltage for each load, the power demand is calculated. For a stand-alone system, the system voltage is the potential required by the largest load. When AC loads dominate, the DC system voltage should be chosen to be compatible with the inverter input.

24.9.3 Power-Conditioning Unit

The choice of the PCU has a great impact on the performance and economics of the system. It depends on the type of waveform produced, which in turn depends on the method used for conversion and the filtering techniques of unwanted frequencies. Several factors must be considered when selecting or designing the inverter:

- The power conversion efficiency
- Rated power
- Duty rating, the amount of time the inverter can supply maximum load
- Input voltage
- Voltage regulation
- Voltage protection
- Frequency requirement
- Power factor
- Islanding detection

24.9.4 Battery Sizing

PV system parameters need to be defined with the battery in mind. The amount of battery storage needed depends on the load energy demand and on weather patterns at the site. There is always a trade-off between keeping cost low and meeting energy demand. There are a number of basic battery characteristics that can have a significant impact on PV system performance.

Among the most important characteristics are temperature effects, recharge efficiency, charge voltage, and the number of days a PV battery will carry the load without energy from the PV array. It is important to clearly define battery charging requirements and meet those charging requirements with proper charge control voltage and array sizing.

References

[1] J. Toothman, S. Alsous, How solar cells work, http://science.howstuffworks.com/environmental/energy/solar-cell.htm. (Accessed October 2010).

[2] S. Roberts, N. Guariento, Building Integrated Photovoltaics: A Handbook, Walter de Gruyter, 2009. http://www.solarserver.com/knowledge/basic-knowledge/photovoltaics.html.

[3] W. Jian, L. Jianzheng, Z. Zhengming, Optimal control of solar energy combined with MPPT and battery charging, in: Proceedings of IEEE International Conference on Electrical Machines and Systems, vol. 1, 2003, pp. 285–288.

Further Reading

[1] www.worldenergy.org/.

[2] Photovoltaics: solar electricity and solar cells in theory and practice, www.solarserver.de/wissen/photovoltaic-e.html.

[3] H. Moller, Semiconductors for Solar Cells, Artech House, Inc, London, 1993.

[4] Berkeley Lab. http://www.lbl.gov/msd/pis/walukiewicz/0202_08_full_solar_spectrum.html.

[5] Sera Dezso, Teodorescu Remus, Rodriguez Pedro, PV panel model based on datasheet values, in: Industrial Electronics, ISIE 2007, IEEE International Symposium volume, 2007, pp. 2392–2396.

[6] R.A. Messenger, J. Ventre, Photovoltaic Systems Engineering, CRC Press, 2003.

[7] S.R. Wenham, Applied Photovoltaics, Routledge, 2012.

[8] S.C. Krauter, Solar Electric Power Generation-Photovoltaic Energy Systems: Modeling of Optical and Thermal Performance, Electrical Yield, Energy Balance, Effect on Reduction of Greenhouse Gas Emissions, Springer Science & Business Media, 2007.

[9] C. Chu, C. Chen, Robust maximum power point tracking method for photovoltaic cells: a sliding mode control approach, Sol. Energy 83 (8) (2009) 1370–1378.

[10] EE362L, Power electronics, solar power, I–V characteristics, Version October 14 2005. http://www.ece.utexas.edu/grady/EE362L_Solar.pdf (Accessed 23 February 2017).

[11] D. Lee, H. Noh, D. Hyun, I. Choy, An improved MPPT converter using current compensation method for small scaled PV-applications, in: Applied Power Electronics Conference and Exposition (APEC'03), vol. 1, 2003, pp. 540–545.

[12] Photovoltaic Fundamentals. http://www.fsec.ucf.edu/PVT/pvbasics/index.htm. (Accessed 23 February 2017).

[13] The solar sprint PV panel. http://chuck-wright.com/SolarSprintPV/SolarSprintPV.html. (Accessed 23 February 2017).

[14] M. A. Serhan, Maximum Power Point Tracking system: An Adaptive Algorithm for Solar Panels (Thesis), American University of Beirut, January 2005.

[15] J.H.R. Enslin, M.S. Wolf, D.B. Snyman, W. Swiegers, Integrated photovoltaic maximum power point tracking converter, IEEE Trans. Ind. Electron. 44 (6) (1997) 769–773.

[16] A.A. Khalil, M. El-Singaby, Position control of sun tracking system; circuits and systems, in: Proceedings of the 46th IEEE International Midwest Symposium, 3, 2003, pp. 1134–1137.

[17] E. Kroutoulis, K. Kalaitzakis, N.C. Voulgaris, Development of a microcontroller-based, photovoltaic maximum power tracking control system, IEEE Trans. Power Electron. 16 (1) (2001) 46–54.

[18] Liu Shengyi, Maximum power point tracker model, Control Model, University of South Carolina, 2000. Available from: http://vtb.engr.sc.edu/modellibrary_old. (Accessed 23 February 2017).

[19] K.H. Hussein, I. Mutta, T. Hoshino, M. Osakada, Maximum photovoltaic power tracking: an algorithm for rapidly changing atmospheric conditions, IEE Proc. Gener. Trans. Distrib. 142 (1) (1995) 59–64.

[20] K.K. Tse, S.H. Henry, S. Chung, Y.R. Hui, M.T. Ho, Novel maximum power point tracking technique for PV panels, in: IEEE Power Electronics Specialists Conference, vol. 4, 2001, pp. 1970–1975.

[21] T. Noguchi, S. Togashi, R. Nakamoto, Short-current pulse-based maximum power point tracking method for multiple photovoltaic-and-converter module system, IEEE Trans. Ind. Electron. 49 (1) (2002) 217–223.

[22] HowStuffworks. http://science.howstuffworks.com/solar-cell5.html. (Accessed 23 February 2017).

[23] M. Masoum, H. Dehbonei, E. Fuschs, Theoretical and experimental analyses of photovoltaic systems with voltage-and current-based

maximum power point tracking, IEEE Trans. Convers. 17 (4) (2002) 514–522.
[24] D. Hohm, M. Ropp, Comparative study of maximum power point tracking algorithms using an experimental, programmable, maximum point test bed, in: IEEE Photovoltaic Specialists Conference, 2000, pp. 1699–1702.
[25] G. Chicco, R. Napoli, F. Spertino, Experimental evaluation of the performance of grid-connected photovoltaic systems, in: IEEE Melecon, Dubrovnik, Croatia, 2004, pp. 1011–1016.
[26] N. Mohan, T. Undeland, W. Robbins, Power Electronics: Converter, Applications and Design, third ed., John Wiley and Sons, 2003.
[27] M.H. Rashid, Power Electronics: Circuits, Devices, and Applications, Prentice Hall, 2004.
[28] R. Carbone, Grid-connected photovoltaic systems with energy storage, in: International Conference on Clean Electrical Power, Capri, Italy, 2009, pp. 760–767.
[29] B. Gu, J. Dominic, J.-S. Lai, C.-L. Chen, T. LaBella, B. Chen, High reliability and efficiency single-phase transformerless inverter for grid-connected photovoltaic systems, IEEE Trans. Power Electron. 28 (5) (2013) 2235–2245.
[30] W. Li, Y. Gu, H. Luo, W. Cui, X. He, C. Xia, Topology review and derivation methodology of single phase transformerless photovoltaic inverters for leakage current suppression, IEEE Trans. Ind. Electron. 62 (7) (2015) 4537–4551, http://dx.doi.org/10.1109/TIE.2015.2399278.
[31] H. Xiao, S. Xie, Transformerless split-inductor neutral point clamped three-level PV grid-connected inverter, IEEE Trans. Power Electron. 27 (4) (2012) 1799–1808.
[32] T. Kerekes, R. Todorescu, P. Rodríguez, G. Vázquez, E. Aldabas, A new high-efficiency single-phase transformerless PV inverter topology, IEEE Trans. Ind. Electron. 58 (1) (2011) 184–191.
[33] Y. Bae, R.Y. Kim, Suppression of common-mode voltage using a multicentral photovoltaic inverter topology with synchronized PWM, IEEE Trans. Ind. Electron. 61 (9) (2014) 4722–4733.
[34] J. Ji, W. Wu, Y. He, Z. Lin, F. Blaabjerg, H. Shu-Hung, A simple differential mode EMI suppressor for the LLCL-filter based single phase grid-tied transformerless inverter, IEEE Trans. Ind. Electron. 62 (7) (2015) 4141–4147, http://dx.doi.org/10.1109/TIE.2014.2385666.
[35] H. Xiao, S. Xie, Leakage current analytical model and application in single-phase transformerless photovoltaic grid-connected inverter, IEEE Trans. Electromagn. Compat. 52 (4) (2010) 902–913.
[36] W. Yu, J.-S. Lai, H. Qian, C. Hutchens, High-efficiency MOSFET inverter with H6-type configuration for photovoltaic nonisolated AC-module applications, IEEE Trans. Power Electron. 26 (4) (2011) 1253–1260.
[37] Ó. López, F.D. Freijedo, A.G. Yepes, P. Fernández-Comesaña, J. Malvar, R. Teodorescu, J. Doval-Gandoy, Eliminating ground current in a transformerless photovoltaic application, IEEE Trans. Energy Convers. 25 (1) (2010) 140–147.
[38] T. Salmi, M. Bouzguenda, A. Gastli, A. Masmoudi, A novel transformerless inverter topology without zero-crossing distortion, Int. J. Renew. Energy Res. 2 (1) (2012) 140–146.
[39] Ó. López, R. Teodorescu, F. Freijedo, J. Doval-Gandoy, Leakage current evaluation of a single-phase transformerless PV inverter connected to the grid, in: IEEE Appl. Power Electron. Conf., Anaheim, CA, 2007, pp. 907–912.
[40] X. Su, Y. Sun, Y. Lin, Analysis on leakage current in transformerless single-phase PV inverters connected to the grid, in: IEEE Power and Energy Eng. Conf., Wuhan, China, Mar, 2011, pp. 1–5.
[41] N. Vázquez, M. Rosas, C. Hernández, E. Vázquez, F. Perez-Pinal, A new common-mode transformerless photovoltaic inverter, IEEE Trans. Ind. Electron. 62 (10) (2015) 6381–6391.
[42] F. De Mango, M. Liserre, A.D. Aquila, A. Pigazo, Overview of anti-islanding algorithms for pv systems. Part I: passive methods, in: Power Electronics and Motion Control Conference, EPE-PEMC 12th International, 2006, pp. 1878–1883.
[43] C.L. Trujillo, D. Velasco, E. Figueres, G. Garcera, Analysis of active islanding detection methods for grid-connected microinverters for renewable energy processing, Appl. Energy 87 (11) (2010) 3591–3605.
[44] M. Ropp, D. Larson, S. Meandering, D. McMahon, J. Ginn, J. Stevens, W. Bower, S. Gonzalez, K. Fennell, L. Brusseau, Discussion of a power line carrier communications-based anti-islanding scheme using a commercial automatic meter reading system, in: Photovoltaic Energy Conversion, Conference Record of the 2006 IEEE 4th World Conference, 2006, pp. 2351–2354.
[45] Z. Salam, A.A. Rahman, Efficiency for photovoltaic inverter: a technological review, in: IEEE Conference on Energy Conversion (CENCON), Johor Bahru, 2014, pp. 175–180.
[46] A.D. Hansen et al, Models for a stand alone PV system, Technical report Riso National Laboratory, Norway, Roskilde, December 2000, http://www.risoe.dk/solenergu/rapporter/pdf/sec-r-12.pdf. (Accessed 23 February 2017).
[47] Sandia National Laboratories: Stand Alone Photovoltaic Systems: *A Handbook of Recommended Design Practices*, Springfield: National Technical Information Service, VA, 1988. (Accessed 23 February 2017).
[48] K.S. Karimov, J.A. Chattha, M.M. Ahmed, et al., Journal of References, Acad. Sci. Tajikistan XLV (9) (2002) 75–83.
[49] W. Dankoff, Glossary of solar water pumping terms and related components, (2009). www.conergy.us/Desktopdefault.aspx/tabid-332/449_read-3816/. Available from: (Accessed 23 February 2017).
[50] R.A. Bentley, Global oil depletion–methodologies and results, in: Proc. 3rd Int. Workshop on Oil and Gas Depletion, Berlin, Germany published by the Australian Association for the Study of Peak Oil and Gas (ASPO), 2004, pp. 25–26.
[51] C. Hua, C. Shen, Comparative study of peak power tracking techniques for solar storage system, in: IEEE Applied Power Electronics Conference and Exposition, vol. 2, 1998, pp. 679–685. February.
[52] C. Hua, J. Lin, DSP-based controller in battery storage of photovoltaic system, in: IEEE IECON 22 International Conference on Industrial Electronics, Control and Instrumentation, vol. 3, 1996, pp. 1705–1710.
[53] S. Duryea, S. Islam, W. Lawrance, A battery management system for stand-alone photovoltaic energy systems, IEEE Ind. Appl. Mag. 7 (3) (1999) 67–72.
[54] E. Lorenzo, L. Narvarte, K. Preiser, R. Zilles, A field experience with automotive batteries in shs's, in: Proceeding of the 2nd World Conference and Exhibition on Photovoltaic Solar Energy Conversion Vienna., 1998, pp. 3266–3268.
[55] P. Diaz, M.A. Egido, Experimental analysis of battery charge regulation in photovoltaic systems, Prog. Photovolt. Res. Appl. 11 (7) (2003) 481–493.
[56] H. Yang, H. Wang, G. Chen, G. Wu, Influence of the charge regulator strategy on state of charge and lifetime of VRLA battery in household photovoltaic systems, Sol. Energy 80 (2006) 281–287.
[57] J. Garche, A. Jossen, H. Doering, The influence of different operating conditions, especially over-discharge, on the lifetime and

performance of lead acid batteries for photovoltaic systems, J. Power Sources 67 (1997) 201–212.
[58] J. Enslin, D. Snyman, Combined Low Cost, High Efficient Inverter, Peak Power Tracker and Regulator for PV Applications, IEEE Trans. Power Electron. 6 (1) (1991) 73–82.
[59] D. Linden, Handbook of Batteries, McGraw Hill, New York, NY, 1995.
[60] IEEE guide for array and battery sizing in stand-alone photovoltaic (PV) systems, in: IEEE Std 1562–2007, pp.i–22, May 12, 2008.
[61] IEEE recommended practice for sizing lead-acid batteries for stand-alone photovoltaic (PV) systems, E-ISBN: 0-7381-2990-9, ISBN 1-55937-068-8, http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=210970. (Accessed 23 February 2017).
[62] IEEE guide for selection, charging, test, and evaluation of lead-acid batteries used in stand-alone photovoltaic (PV) systems, E-ISBN: 0-7381-3581-X, PDF: ISBN 0-7381-3581-X SS95086, http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=1263341. (Accessed 23 February 2017).
[63] IEEE recommended practice for installation and maintenance of lead-acid batteries for photovoltaic (PV) systems, E-ISBN: 978-0-7381-5592-0, ISBN: 978-0-7381-5591-3, http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=4238866. (Accessed 23 February 2017).
[64] IEEE recommended practice for installation and maintenance of nickel-cadmium batteries for photovoltaic (PV) system, E-ISBN: 0-7381-1088-4, ISBN 1-55937-072-6, http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=89824. (Accessed 23 February 2017).
[65] R. Mayfield, Photovoltaic Design and Installation for Dummies, John Wiley & Sons, Hoboken, NJ, 2010.
[66] John P. Thornton, The effect of sand-storm on photovoltaic array and components, in: Solar Energy Conference, 1992.
[67] L. Chaar, A. Jamaleddine, F. Ajmal, H. Khan, Effect of wind blown sand and dust on pv arrays especially in UAE, in: Power Systems Conference (PSC), South Carolina, USA, 2008.
[68] B. Mohandes, L. El-Chaar, L. Lamont, Application study of 500 W photovoltaic (PV) system in the UAE, Appl. Solar Energy J. 45 (4) (2009) 242–247.
[69] T. Al Hanai, R. Bani Hashim, L. El-Chaar, L. Lamont, Study of a 900 W, thin-film, amorphous silicon pv system in a dusty environment, in: International Conference on Renewable Energy: Generation and Applications - ICREGA'10, UAE: Al-Ain, 2010.
[70] M. Hosenuzzaman, N.A. Rahim, J. Selvaraj, M. Hasanuzzaman, Factors affecting the PV based power generation, in: 3rd IET International Conference on Clean Energy and Technology (CEAT) 2014, Kuching, 2014, pp. 1–6.
[71] D. Revati, N.P. Priyadharshini, E. Natarajan, A simulation study on critical factors that influence electrical performance of photovoltaic module, in: 10th International Conference on Intelligent Systems and Control (ISCO), Coimbatore, 2016, pp. 1–5.
[72] B. Wang, et al., Research on influence between photovoltaic power and module temperature and ambient temperature, in: IEEE International Conference on Power System Technology (POWERCON), Wollongong, NSW, 2016, pp. 1–5.
[73] T. Sarver, A. Al-Qaraghuli, L.L. Kazmerski, A comprehensive review of the impact of dust on the use of solar energy: history, investigations, results, literature, and mitigation approaches, Renew. Sust. Energ. Rev. 22 (2013) 698–733.
[74] M.R. Maghami, H. Hizam, C. Gomes, M.A. Radzi, M.I. Rezadad, S. Hajighorbani, Power loss due to soiling on solar panel: a review, Renew. Sust. Energ. Rev. 59 (2016) 1307–1316.
[75] S.C. Costa, A.S.A. Diniz, L.L. Kazmerski, Dust and soiling issues and impacts relating to solar energy systems: literature review update for 2012–2015, Renew. Sust. Energ. Rev. 63 (2016) 33–61.

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25

Power Electronics for Renewable Energy Sources

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25.1 Introduction

The Kyoto agreement on global reduction of greenhouse gas emissions has prompted renewed interest in renewable energy systems worldwide. Many renewable energy technologies today are well developed, reliable, and cost competitive with the conventional fuel generators. The cost of renewable energy technologies is on a falling trend and is expected to fall further as demand and production increases. There are many renewable energy sources (RES) such as biomass, solar, wind, minihydro, and tidal power. However, solar and wind energy systems make use of advanced power electronics technologies, and therefore, the focus in this chapter will be on solar photovoltaic and wind power.

One of the advantages offered by (RES) is their potential to provide sustainable electricity in areas not served by the conventional power grid. The growing market for renewable energy technologies has resulted in a rapid growth in the need of power electronics. Most of the renewable energy technologies produce DC power, and hence, power electronics and control equipment are required to convert the DC into AC power.

Inverters are used to convert DC to AC. There are two types of inverters: (a) stand-alone and (b) grid-connected. Both types have several similarities but are different in terms of control functions. A stand-alone inverter is used in off-grid applications with battery storage. With backup diesel generators (such as photovoltaic (PV)/diesel/hybrid power systems), the inverters may have additional control functions such as operating in parallel with diesel generators and bidirectional operation (battery charging and inverting). Grid-interactive inverters must follow the voltage and frequency characteristics of the utility generated power presented on the distribution line. For both types of inverters, the conversion efficiency is a very important consideration. Details of stand-alone and grid-connected inverters for PV and wind applications are discussed in this chapter.

Section 25.2 covers stand-alone PV system applications such as battery charging and water pumping for remote areas. This section also discusses power electronic converters suitable for PV-diesel hybrid systems and grid-connected PV for rooftop and large-scale applications. Of all the renewable energy options, the wind turbine technology is maturing very fast. A marked rise in installed wind power capacity has been noticed worldwide in the last decade. Per unit generation cost of wind power is now quite comparable with the conventional generation. Wind turbine generators are used in stand-alone battery charging applications, in combination with fossil-fuel

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generators as part of hybrid systems and as grid-connected systems. As a result of advancements in blade design, generators, power electronics, and control systems, it has been possible to increase dramatically the availability of large-scale wind power. Many wind generators now incorporate speed control mechanisms like blade pitch control or use converters/inverters to regulate power output from variable-speed wind turbines. In Section 25.3, electric and power-conditioning aspects of wind energy conversion systems were included.

25.2 Power Electronics for Photovoltaic Power Systems

25.2.1 Basics of Photovoltaics

The density of power radiated from the sun (referred as "solar energy constant") at the outer atmosphere is 1.373 kW/m^2. Part of this energy is absorbed and scattered by the earth's atmosphere. The final incident sunlight on earth's surface has a peak density of 1 kW/m^2 at noon in the tropics. The technology of photovoltaics (PV) is essentially concerned with the conversion of this energy into usable electric form. Basic element of a PV system is the solar cell. Solar cells can convert the energy of sunlight directly into electricity. Consumer appliances used to provide services such as lighting, water pumping, refrigeration, telecommunication, and television can be run from PV electricity. Solar cells rely on a quantum-mechanical process known as the "photovoltaic effect" to produce electricity. A typical solar cell consists of a p-n junction formed in a semiconductor material similar to a diode. Fig. 25.1 shows a schematic diagram of the cross section through a crystalline solar cell [1]. It consists of a 0.2–0.3 mm thick monocrystalline or polycrystalline silicon wafer having two layers with different electric properties formed by "doping" it with other impurities (e.g., boron and phosphorous). An electric field is established at the junction between the negatively doped (using phosphorous atoms) and the positively doped (using boron atoms) silicon layers. If light is incident on the solar cell, the energy from the light

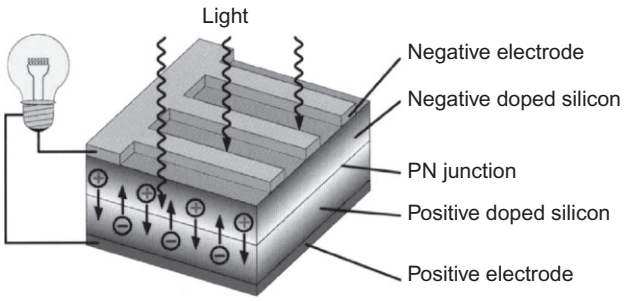


FIG. 25.1 Principle of the operation of a solar cell.

(photons) creates free charge carriers, which are separated by the electric field. An electric voltage is generated at the external contacts, so that current can flow when a load is connected. The photocurrent (I_{ph}), which is internally generated in the solar cell, is proportional to the radiation intensity.

A simplified equivalent circuit of a solar cell consists of a current source in parallel with a diode as shown in Fig. 25.2A. A variable resistor is connected to the solar cell generator as a load. When the terminals are short-circuited, the output voltage and also the voltage across the diode is zero. The entire photocurrent (I_{ph}) generated by the solar radiation then flows to the output. The solar cell current has its maximum (I_{sc}). If the load resistance is increased, which results in an increasing voltage across the p-n junction of the diode, a portion of the current flows through the diode, and the output current decreases by the same amount. When the load resistor is open-circuited, the output current is zero, and the entire photocurrent flows through the diode. The relationship between current and voltage may be determined from the diode characteristic equation:

$$I = I_{ph} - I_0\left(e^{qV/kT} - 1\right) = I_{ph} - I_d \qquad (25.1)$$

where q is the electron charge, k is the Boltzmann constant, I_{ph} is photocurrent, I_0 is the reverse saturation current, I_d is diode current, and T is the solar cell operating temperature (°K). The current versus voltage (I-V) of a solar cell is thus equivalent to an "inverted" diode characteristic curve shown in Fig. 25.2B.

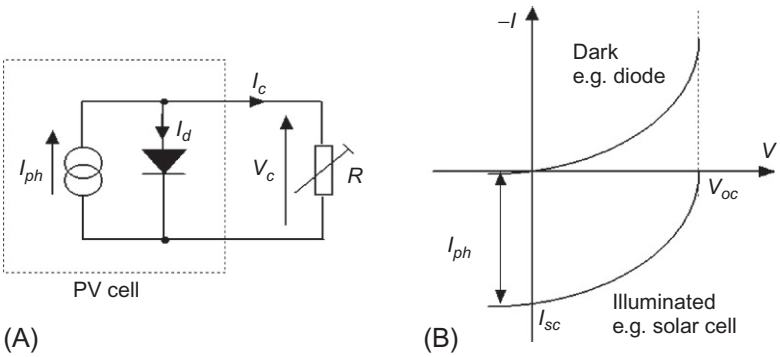


FIG. 25.2 Simplified equivalent circuit for a solar cell.

A number of semiconductor materials are suitable for the manufacturing of solar cells. The most common types using silicon semiconductor material (Si) are as follows:

- Monocrystalline Si cells
- Polycrystalline Si cells
- Amorphous Si cells

A solar cell can be operated at any point along its characteristic current-voltage curve, as shown in Fig. 25.3. Two important points on this curve are the open-circuit voltage (V_{oc}) and short-circuit current (I_{sc}). The open-circuit voltage is the maximum voltage at zero current, while short-circuit current is the maximum current at zero voltage. For a silicon solar cell under standard test conditions, V_{oc} is typically 0.6–0.7 V, and I_{sc} is typically 20–40 mA for every square centimeter of the cell area. To a good approximation, I_{sc} is proportional to the illumination level, whereas V_{oc} is proportional to the logarithm of the illumination level.

A plot of power (P) against voltage (V) for this device (Fig. 25.3) shows that there is a unique point on the I-V curve at which the solar cell will generate maximum power. This is known as the maximum power point (V_{mp} and I_{mp}). To maximize the power output, steps are usually taken during fabrication; the three basic cell parameters are open-circuit voltage, short-circuit current, and fill factor (FF)—a term describing how "square" the I-V curve is given by

$$\text{Fill Factor} = \left(V_{mp} \times I_{mp}\right)/\left(V_{oc} \times I_{sc}\right) \tag{25.2}$$

For a silicon solar cell, FF is typically 0.6–0.8. Because silicon solar cells typically produce only about 0.5 V, a number of cells are connected in series in a PV module. A panel is a collection of modules physically and electrically grouped together on a support structure. An array is a collection of panels (see Fig. 25.4).

The effect of temperature on the performance of silicon solar module is illustrated in Fig. 25.5. Note that I_{sc} slightly increases linearly with temperature, but V_{oc} and the maximum power, P_m, decrease with temperature [1].

Fig. 25.6 shows the variation of PV current and voltages at different insolation levels. From Figs. 25.5 and 25.6, it can be

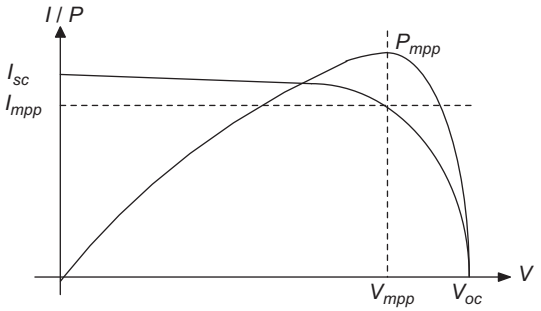


FIG. 25.3 Current versus voltage (I-V) and current power (P-V) characteristics for a solar cell.

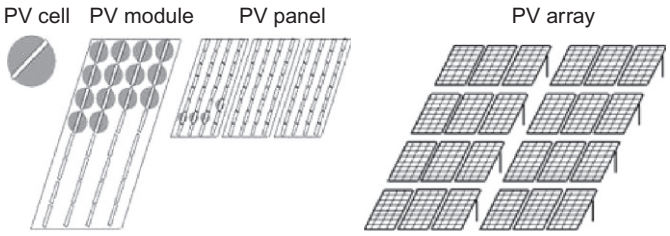


FIG. 25.4 PV generator terms.

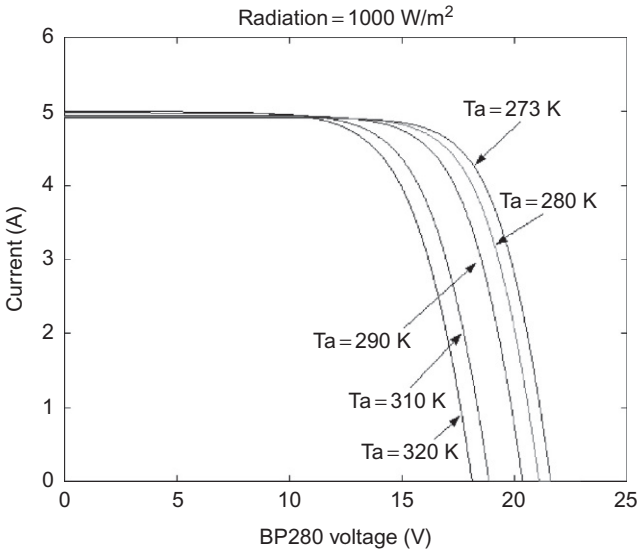


FIG. 25.5 Effects of temperature on silicon solar cells.

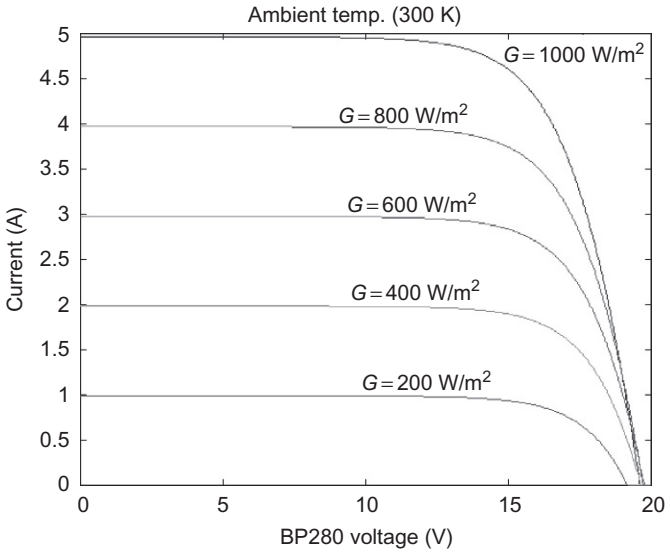


FIG. 25.6 Typical current/voltage (I-V) characteristic curves for different insolation.

seen that the *I-V* characteristics of solar cells at a given insolation and temperature consist of a constant voltage segment and a constant current segment [2]. The current is limited, as the cell is short-circuited. The maximum power condition occurs at the knee of the characteristic curve where the two segments meet.

25.2.2 Types of PV Power Systems

Photovoltaic power systems can be classified as follows:

- Stand-alone PV systems
- Hybrid PV systems
- Grid-connected PV systems

Stand-alone PV systems, shown in Fig. 25.7, are used in remote areas with no access to a utility grid. Conventional power systems used in remote areas often based on manually controlled diesel generators operating continuously or for a few hours. Extended operation of diesel generators at low load levels significantly increases maintenance costs and reduces their useful life. Renewable energy sources such as PV can be added to remote-area power systems using diesel and other fossil-fuel-powered generators to provide 24 h power economically and efficiently. Such systems are called "hybrid energy systems." Fig. 25.8 shows a schematic of a PV-diesel hybrid system. In grid-connected PV systems shown in Fig. 25.9, PV panels are connected to a grid through inverters without battery storage. These systems can be classified as small systems like the residential rooftop systems or large grid-connected systems. The grid-interactive inverters must be synchronized with the grid in terms of voltage and frequency.

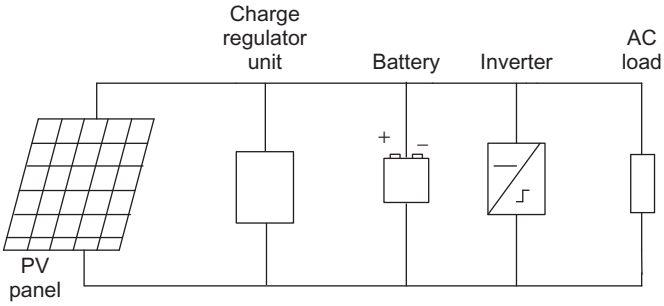


FIG. 25.7 Stand-alone PV system.

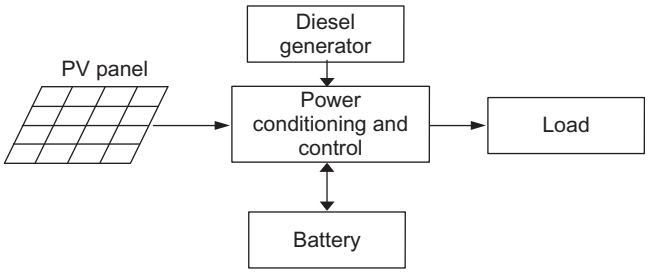


FIG. 25.8 PV-diesel hybrid system.

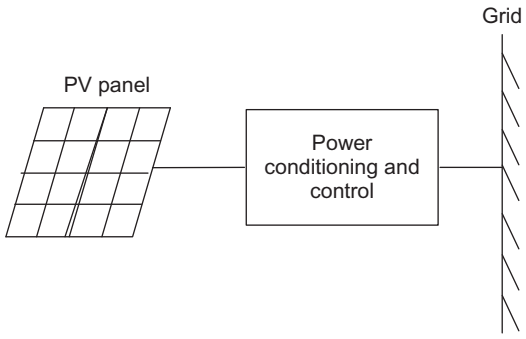


FIG. 25.9 Grid-connected PV system.

25.2.3 Stand-Alone PV Systems

The two main stand-alone PV applications are as follows:

- Battery charging
- Solar water pumping

25.2.3.1 Battery Charging

Batteries for PV systems

Stand-alone PV energy system requires storage to meet the energy demand during periods of low solar irradiation and nighttime. Several types of batteries are available such as the lead-acid, nickel-cadmium, lithium, zinc bromide, zinc chloride, sodium sulfur, nickel-hydrogen, redox, and vanadium batteries. The provision of cost-effective electric energy storage remains one of the major challenges for the development of improved PV power systems. Typically, lead-acid batteries are used to guarantee several hours to a few days of energy storage. Their reasonable cost and general availability has resulted in the widespread application of lead-acid batteries for remote-area power supplies despite their limited lifetime compared with other system components. Lead-acid batteries can be deep or shallow cycling gelled batteries, batteries with captive or liquid electrolyte, sealed and nonsealed batteries, etc. [3]. Sealed batteries are valve regulated to permit the evolution of excess hydrogen gas (although catalytic converters are used to convert as much evolved hydrogen and oxygen back to water as possible). Sealed batteries need less maintenance. The following factors are considered in the selection of batteries for PV applications [1]:

- Deep discharge (70%–80% depth of discharge)
- Low charging/discharging current
- Long duration charge (slow) and discharge (long duty cycle)
- Irregular and varying charge/discharge
- Low self-discharge
- Long lifetime

- Less maintenance requirement
- High-energy storage efficiency
- Low cost

Battery manufacturers specify the nominal number of complete charge and discharge cycles as a function of the depth of discharge (DOD), as shown in Fig. 25.10. While this information can be used reliably to predict the lifetime of lead-acid batteries in conventional applications, such as uninterruptable power supplies or electric vehicles, it usually results in an overestimation of the useful life of the battery bank in renewable energy systems.

Two of the main factors that have been identified as limiting criteria for the cycle life of batteries in PV power systems are incomplete charging and prolonged operation at a low state of charge (SOC). The objective of improved battery control strategies is to extend the lifetime of lead-acid batteries to achieve a typical number of cycles shown in Fig. 25.10. If this is achieved, an optimum solution for the required storage capacity and the maximum DOD of the battery can be found by referring to manufacturer's information. Increasing the capacity will reduce the typical DOD and therefore prolong the battery lifetime. Conversely, it may be more economic to replace a smaller battery bank more frequently.

PV charge controllers

Blocking diodes in series with PV modules are used to prevent the batteries from being discharged through the PV cells at night when there is no sun available to generate energy. These blocking diodes also protect the battery from short circuits. In a solar power system consisting of more than one string connected in parallel, if a short circuit occurs in one of the strings, the blocking diode prevents the other PV strings to discharge through the short-circuited string.

The battery storage in a PV system should be properly controlled to avoid catastrophic operating conditions like overcharging or frequent deep discharging. Storage batteries account for most PV system failures and contribute significantly to both the initial and the eventual replacement costs.

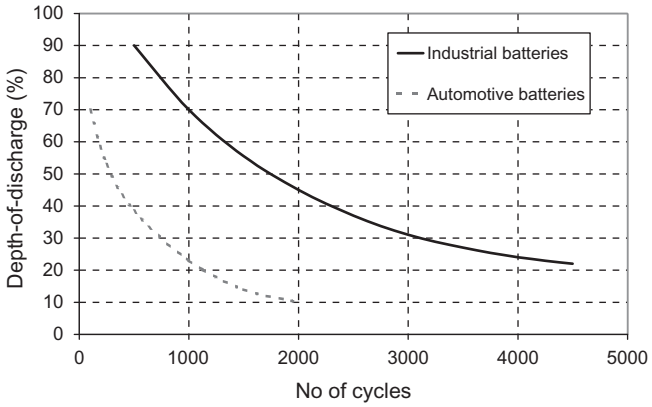


FIG. 25.10 Nominal number of battery cycles versus DOD.

Charge controllers regulate the charge transfer and prevent the battery from being excessively charged and discharged. Three types of charge controllers are commonly used:

- Series charge regulators
- Shunt charge regulators
- DC-DC converters

A series charge regulators: The basic circuit for the series regulators is given in Fig. 25.11. In the series charge controller, the switch S_1 disconnects the PV generator when a predefined battery voltage is achieved. When the voltage reduces below the discharge limit, the load is disconnected from the battery to avoid deep discharge beyond the limit. The main problem associated with this type of controller is the losses associated with the switches. This extra power loss has to come from the PV power, and this can be quite significant. Bipolar transistors, metal-oxide-semiconductor field-effect transistors (MOSFETs), or relays are used as the switches.

Shunt charge regulators: In this type, as illustrated in Fig. 25.12, when the battery is fully charged, the PV generator is short-circuited using an electronic switch (S_1). Unlike series controllers, this method works more efficiently even when the battery is completely discharged as the short-circuit switch need not be activated until the battery is fully discharged [1].

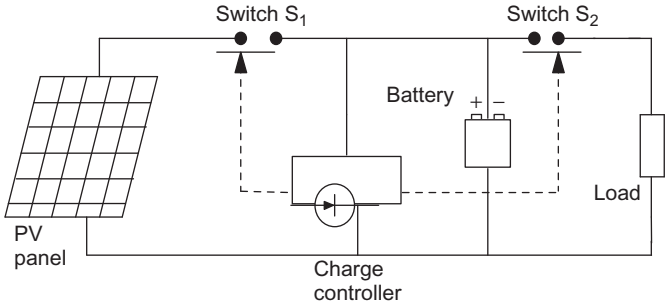


FIG. 25.11 Series charge regulator.

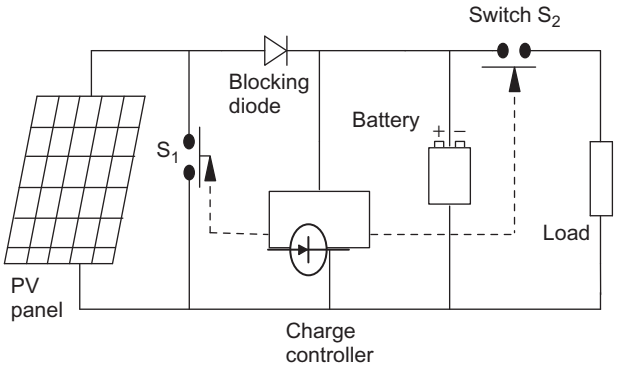


FIG. 25.12 Shunt charge regulator.

The blocking diode prevents short-circuiting of the battery. Shunt charge regulators are used for the small PV applications (less than 20 A).

Deep discharge protection is used to protect the battery against the deep discharge. When the battery voltage reaches below the minimum set point for deep discharge limit, switch S_2 disconnects the load. Simple series and shunt regulators allow only relatively coarse adjustment of the current flow and seldom meet the exact requirements of PV systems.

DC–DC converter type charge regulators: Switch-mode DC-to-DC converters are used to match the output of a PV generator to a variable load. There are various types of DC-DC converters such as the following:

- Buck (step-down) converter
- Boost (step-up) converter
- Buck-boost (step-down/step-up) converter

Figs. 25.13–25.15 show simplified diagrams of these three basic types of converters. The basic concepts are an electronic switch, an inductor to store energy, and a "flywheel" diode, which carries the current during that part of switching cycle when the switch is off. The DC-DC converters allow the charge current to be reduced continuously in such a way that the resulting battery voltage is maintained at a specified value.

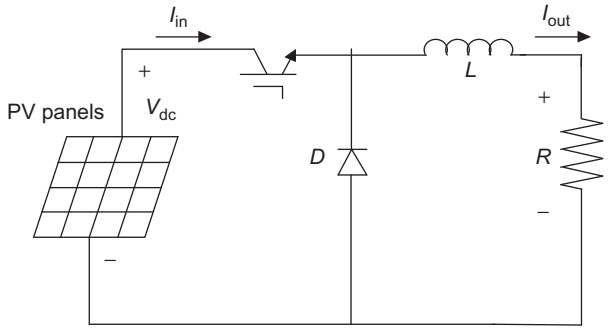


FIG. 25.13 Buck converter.

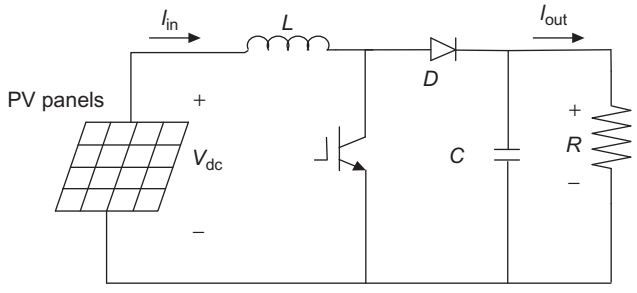


FIG. 25.14 Boost converter.

Maximum power point tracking (MPPT)

A controller that tracks the maximum power point locus of the PV array is known as the MPPT. In Fig. 25.16, the PV power output is plotted against the voltage for insolation levels from 200 to 1000 W/m^2 [4]. The points of maximum array power form a curve are termed as the maximum power locus. Due to high cost of solar cells, it is necessary to operate the PV array at its maximum power point (MPP). For overall optimal operation of the system, the load line must match the PV array's MPP locus.

Referring to Fig. 25.17, the load characteristics can be either curve OA or curve OB depending upon the nature of the load and its current and voltage requirements. If load OA is considered and the load is directly coupled to the solar array, the array will operate at point A1, delivering only power P1. The maximum array power available at the given insolation is P2. In order to use PV array power P2, a power conditioner coupled between array and the load is needed.

There are generally two ways of operating PV modules at maximum power point. These ways take advantage of analog and/or digital hardware control to track the MPP of PV arrays.

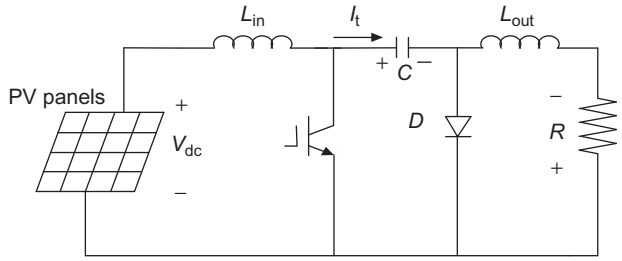


FIG. 25.15 Boost-buck converter.

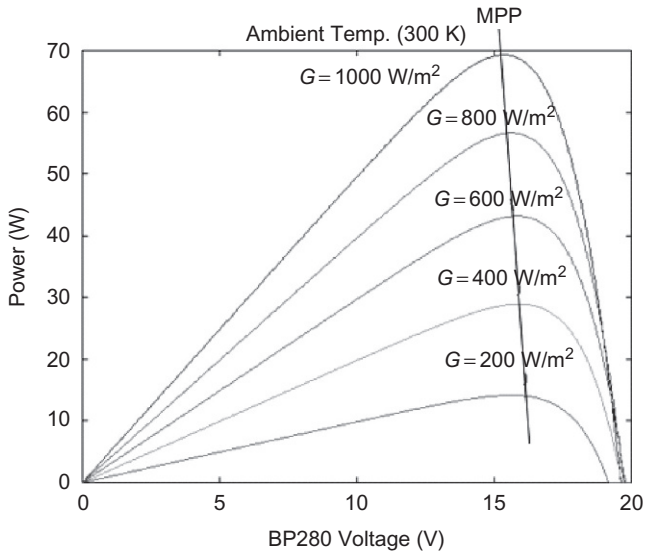


FIG. 25.16 Typical power/voltage characteristics for increased insolation.

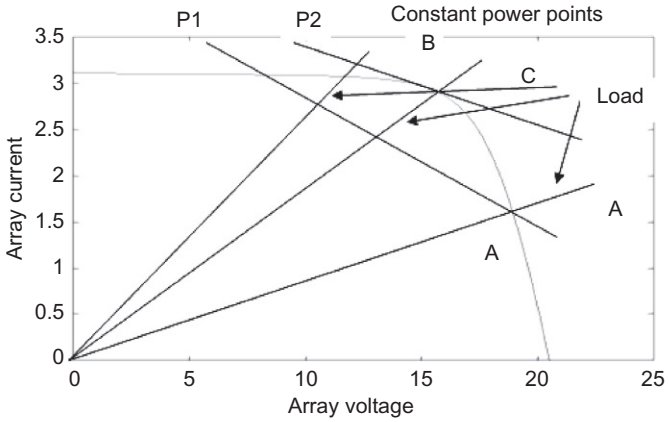


FIG. 25.17 PV array and load characteristics.

Analog control

There are many analog control mechanisms proposed in different articles, for instance, fractional short-circuit current (I_{SC}) [5–8], fractional open-circuit voltage (V_{OP}) [5,6,9–12], and ripple correlation control (RCC) [13–16].

Fractional open-circuit voltage (V_{OP}) is one of the simple analogue control methods. It is based on the assumption that the maximum power point voltage, V_{MPP}, is a linear function of the open-circuit voltage, V_{OC}. For example, $V_{MPP} = kV_{OC}$ where $k \asymp 0.76$. This assumption is reasonably accurate even for large variations in the cell short-circuit current and temperature. This type of MPPT is probably the most common type. A variation to this method involves periodically open-circuiting the cell string and measuring the open-circuit voltage. The appropriate value of V_{MPP} can then be obtained with a simple voltage divider.

Digital control

There are many digital control mechanisms that were proposed in different articles, for instance, perturbation and observation (P&O) or hill climbing [17–22], fuzzy logic [23–27], neural network [17,28–30], and incremental conductance (IncCond) [31–34].

The P&O or hill-climbing control involves around varying the input voltage around the optimum value by giving it a small increment or decrement alternately. The effect on the output power is then assessed, and a further small correction is made to the input voltage. Therefore, this type of control is called a hill-climbing control. The power output of the PV array is sampled at an every definite sampling period and compared with the previous value. In the event, when power is increased, then the solar array voltage is stepped in the same direction as the previous sample time, but if the power is reduced, then the array voltage is stepped in the opposite way and try to operate the PV array at its optimum/maximum power point.

To operate the PV array at the MPP, perturb and adjust method can be used at regular intervals. Current drawn is sampled every few seconds, and the resulting power output of the solar cells is monitored at regular intervals. When an increased current results in a higher power, it is further increased until power output starts to reduce. But if the increased PV current results in lesser amount of power than in the previous sample, then the current is reduced until the MPP is reached.

25.2.3.2 Inverters for Stand-Alone PV Systems

Inverters convert power from DC to AC, while rectifiers convert it from AC to DC. Many inverters are bidirectional, that is, they are able to operate in both inverting and rectifying modes. In many stand-alone PV installations, alternating current is needed to operate 230 V (or 110 V), 50 Hz (or 60 Hz) appliances. Generally, stand-alone inverters operate at 12, 24, 48, 96, 120, or 240 V DC depending upon the power level. Ideally, an inverter for a stand-alone PV system should have the following features:

- Sinusoidal output voltage.
- Voltage and frequency within the allowable limits.
- Cable to handle large variation in input voltage.
- Output voltage regulation.
- High efficiency at light loads.
- Less harmonic generation by the inverter to avoid damage to electronic appliances like television, additional losses, and heating of appliances.
- Photovoltaic inverters must be able to withstand overloading for short term to take care of higher starting currents from pumps, refrigerators, etc.
- Adequate protection arrangement for over-/undervoltage and frequency, short circuit, etc.
- Surge capacity.
- Low idling and no load losses.
- Low battery voltage disconnect.
- Low audio and radio frequency (RF) noise.

Several different semiconductor devices such as metal-oxide-semiconductor field-effect transistor (MOSFETs) and insulated-gate bipolar transistors (IGBTs) are used in the power stage of inverters. Typically, MOSFETs are used in units up to 5 kVA and 96 V DC. They have the advantage of low switching losses at higher frequencies. Because the on-state voltage drop is 2 V DC, IGBTs are generally used only above 96 V DC systems.

Voltage-source inverters are usually used in stand-alone applications. They can be single phase or three phase. There are three switching techniques commonly used: square-wave, quasi-square-wave, and pulse-width modulation. Square-wave or modified square-wave inverters can supply power tools, resistive heaters, or incandescent lights, which do not require a high-quality sine wave for reliable and efficient operation. However, many household appliances require low distortion sinusoidal waveforms. The use of true sine-wave inverters is recommended for remote-area power systems. Pulse-width modulated (PWM) switching is generally used for obtaining sinusoidal output from the inverters.

A general layout of a single-phase system, both half bridge and full bridge, is shown in Fig. 25.18. In Fig. 25.18A, single-phase half bridge is with two switches, S_1 and S_2; the capacitors C_1 and C_2 are connected in series across the DC source. The junction between the capacitors is at the midpotential. Voltage across each capacitor is $V_{dc}/2$. Switches S_1 and S_2 can be switched on/off periodically to produce AC voltage. Filter (L_f and C_f) is used to reduce high-switch-frequency components and to produce sinusoidal output from the inverter. The output of inverter is connected to load through a transformer. Fig. 25.18B shows the similar arrangement for full-bridge configuration with four switches. For the same input source voltage, the full-bridge output is twice, and the switches carry less current for the same load power.

The power circuit of a three-phase four-wire inverter is shown in Fig. 25.19. The output of the inverter is connected to load via three-phase transformer (delta/Y). The star point of the transformer secondary gives the neutral connection. Three phase or single phase can be connected to this system. Alternatively, a center tap DC source can be used to supply the converter, and the midpoint can be used as the neutral.

Fig. 25.20 shows the inverter efficiency for a typical inverter used in remote-area power systems. It is important to consider that the system load is typically well below the nominal inverter capacity P_{nom}, which results in low conversion efficiencies at loads below 10% of the rated inverter output power. Optimum overall system operation is achieved if the total energy dissipated in the inverter is minimized. The high conversion efficiency at low power levels of recently developed inverters for grid-connected PV systems shows that there is a significant potential for further improvements in efficiency.

Bidirectional inverters convert DC power to AC power (inverter) or AC power to DC power (rectifier) and are

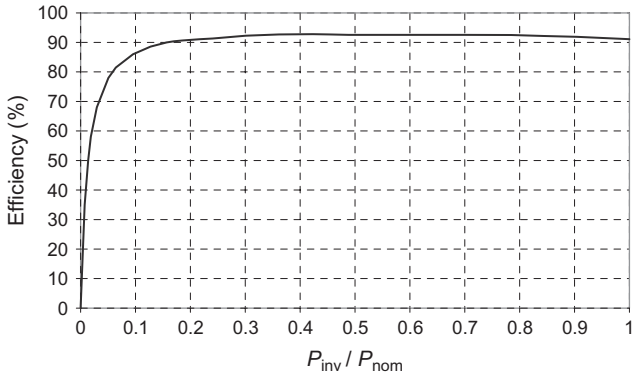


FIG. 25.20 Typical inverter efficiency curve.

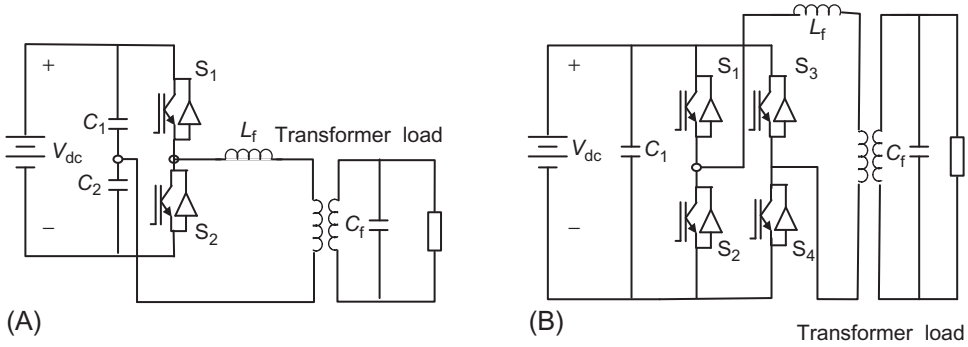


FIG. 25.18 Single-phase inverter: (A) half bridge and (B) full bridge.

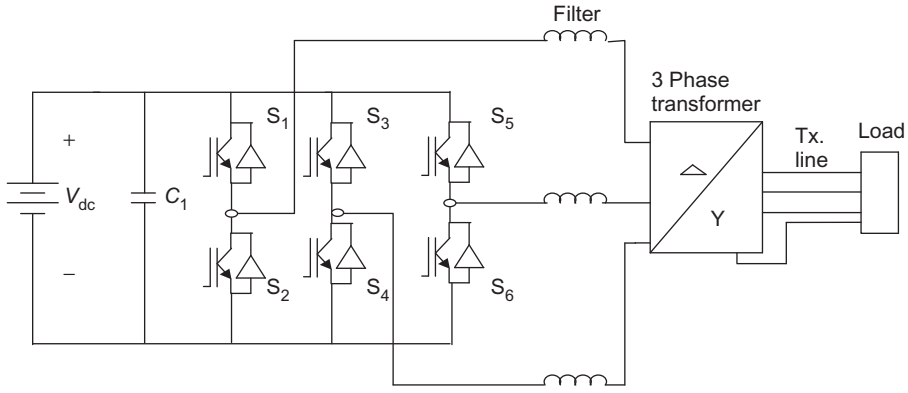


FIG. 25.19 A stand-alone three-phase four-wire inverter.

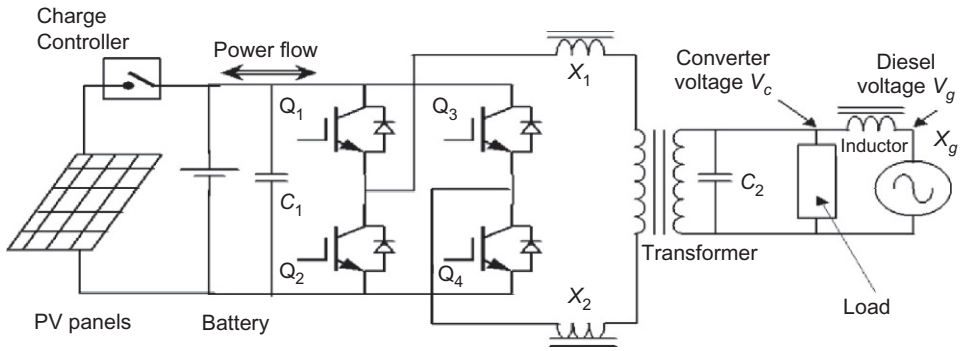


FIG. 25.21 Bidirectional inverter system.

becoming very popular in remote-area power systems [3,4]. The principle of a stand-alone single-phase bidirectional inverter used in a PV/battery/diesel hybrid system can be explained by referring Fig. 25.21. A charge controller is used to interface the PV array and the battery. The inverter has a full-bridge configuration realized using four power electronic switches (MOSFET or IGBTs) S_1–S_4. In this scheme, the diagonally opposite switches (S_1 and S_4) and (S_2 and S_3) are switched using a sinusoidally PWM gate pulses. The inverter produces sinusoidal output voltage. The inductors X_1, X_2, and the AC output capacitor C_2 filter out the high-switch-frequency components from the output waveform. Most inverter topologies use a low-frequency (50 or 60 Hz) transformer to step up the inverter output voltage. In this scheme, the diesel generator and the converter are connected in parallel to supply the load. The voltage sources, diesel and inverter, are separated by the link inductor X_m. The bidirectional power flow between inverter and the diesel generator can be established.

The power flow through the link inductor, X_m, is

$$S_m = V_m I_m^* \tag{25.3}$$

$$P_m = (V_m V_c \sin\delta)/X_m \tag{25.4}$$

$$Q_m = (V_m/X_m)(V_m - V_c \cos\delta) \tag{25.5}$$

$$\delta = \sin^{-1}[(X_m P_m)/(V_m V_c)] \tag{25.6}$$

where δ is the phase angle between the two voltages. From Eq. (25.4), it can be seen that the power supplied by the inverter from the batteries (inverter mode) or supplied to the batteries (charging mode) can be controlled by controlling the phase angle δ. The PWM pulses separately control the amplitude of the converter voltage, V_c, while the phase angle with respect to the diesel voltage is varied for power flow.

25.2.3.3 Solar Water Pumping

In many remote and rural areas, hand pumps or diesel-driven pumps are used for water supply. Diesel pumps consume fossil fuel, affect environment, need more maintenance, and are less reliable. Photovoltaic powered water pumps have received considerable attention recently due to major developments in the field of solar cell materials and power electronic systems technology.

Types of pumps

Two types of pumps are commonly used for the water pumping applications: positive and centrifugal displacement. Both centrifugal and positive displacement pumps can be further classified into those with motors that are (a) surface mounted and those that are (b) submerged into the water ("submersible").

Displacement pumps have water output directly proportional to the speed of the pump but almost independent of the head. These pumps are used for solar water pumping from deep wells or bores. They may be piston-type pumps or use diaphragm driven by a cam and rotary screw-type pumps or use progressive cavity system. The pumping rate of these pumps is directly related to the speed, and hence, constant torque is desired.

Centrifugal pumps are used for low-head applications especially if they are directly interfaced with the solar panels. Centrifugal pumps are designed for fixed-head applications, and the pressure difference generated increases in relation to the speed of the pump. These pumps are rotating impeller type, which throws the water radially against a casing, so shaped that the momentum of the water is converted into useful pressure for lifting [3]. The centrifugal pumps have relatively high efficiency, but it reduces at lower speeds, which can be a problem for the solar water pumping system at the time of low light levels. The single-stage centrifugal pump has just one impeller, whereas most borehole pumps are multistage types where the outlet from one impeller goes into the center of another and each one keeps increasing the pressure difference.

From Fig. 25.22, it is quite obvious that the load line is located relatively faraway from P_{max} line. It has been reported that the daily utilization efficiency for a DC motor drive is 87% for a centrifugal pump compared with 57% for a constant torque characteristic load. Hence, centrifugal pumps are more compatible with PV arrays. The system operating point is

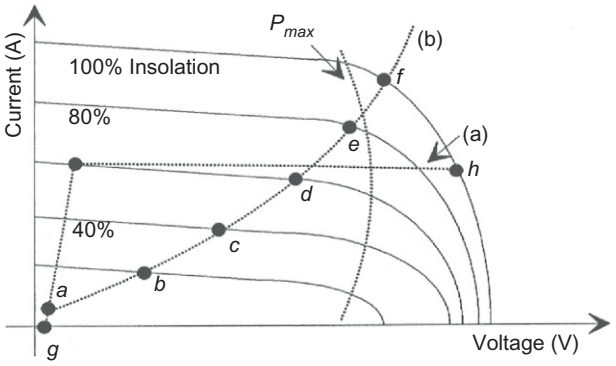


FIG. 25.22 *I-V* characteristics of a PV array and two mechanical loads: (A) constant torque and (B) centrifugal pump.

determined by the intersection of the *I-V* characteristics of the PV array and the motor as shown in Fig. 25.22. The torque-speed slope is normally large due to the armature resistance being small. At the instant of starting, the speed and the back emf are zero. Hence, the motor starting current is approximately the short-circuit current of the PV array. By matching the load to the PV source through MPPT, the starting torque increases.

The matching of a DC motor depends upon the type of load being used. For instance, a centrifugal pump is characterized by having the load torque proportional to the square of speed. The operating characteristics of the system (i.e., PV source, permanent magnet (PM) DC motor, and load) are at the intersection of the motor and load characteristics as shown in Fig. 25.23 (i.e., points a, b, c, d, e, and f for centrifugal pump). From Fig. 25.23, the system utilizing the centrifugal pump as its load tends to start at low solar irradiation (point a) level. However, for the systems with an almost constant torque characteristics in Fig. 25.22, the start is at almost 50% of one sum (full insolation) that results in short period of operation.

Types of motors

There are various types of motors available for the PV water pumping applications:

- DC motors
- AC motors

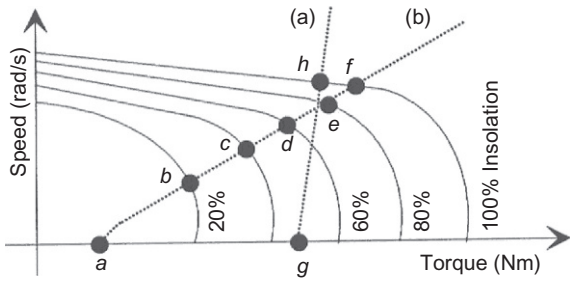


FIG. 25.23 Speed torque characteristics of a DC motor and two mechanical loads: (A) helical rotor and (B) centrifugal pump.

DC motors are preferred where direct coupling to PV panels is desired, whereas AC motors are coupled to the solar panels through inverters. AC motors in general are cheaper than the DC motors and are more reliable, but the DC motors are more efficient. The DC motors used for solar pumping applications are as follows:

- Permanent magnet DC motors with brushes
- Permanent DC magnet motors without brushes

In DC motors with the brushes, the brushes are used to deliver power to the commutator and need frequent replacement due to wear and tear. These motors are not suitable for submersible applications unless long transmission shafts are used. Brushless DC permanent magnet motors have been developed for submersible applications.

The AC motors are of the induction motor type, which is cheaper than DC motors and available worldwide. However, they need inverters to change DC input from PV to AC power. A comparison of the different types of motors used for PV water pumping is given in Table 25.1.

Power conditioning units for PV water pumping

Most PV pump manufacturers include power-conditioning units (PCU) that are used for operating the PV panels close to their MPP over a range of load conditions and varying insolation levels and also for power conversion. DC or AC motor-pump units can be used for PV water pumping. In its simplest form, a solar water pumping system is composed of PV array, PCU, and DC water-pump unit as shown in Fig. 25.24.

In case of lower light levels, high currents can be generated through power conditioning to help in starting the motor-pump units especially for reciprocating positive displacement type pumps with constant torque characteristics, requiring constant current throughout the operating region. In positive displacement type pumps, the torque generated by the pumps depends on the pumping head, friction, pipe diameter, etc. and needs certain level of current to produce the necessary torque. Some systems use electronic controllers to assist starting and operation of the motor under low solar radiation. This is particularly important when using positive displacement pumps. The solar panels generate DC voltage and current. The solar water pumping systems usually have DC or AC pumps. For DC pumps, the PV output can be directly connected to the pump through MPPT, or a DC-DC converter can also be used for interfacing for controlled DC output from PV panels. To feed the AC motors, a suitable interfacing is required for the power conditioning. These PV inverters for the stand-alone applications are very expensive. The aim of power-conditioning equipment is to supply the controlled voltage/current output from the converters/inverters to the motor-pump unit.

These power-conditioning units are also used for operating the PV panels close to their maximum efficiency for fluctuating solar conditions. The speed of the pump is governed by the

TABLE 25.1 Comparison of the different types of motor used for PV water pumping

Types of motor	Advantages	Disadvantages	Main features
Brushed DC	Simple and efficient for PV applications No complex control circuits is required as the motor starts without high-current surge These motors will run slowly but do not overheat with reduced voltage	Brushes need to be replaced periodically (typical replacement interval is 2000–4000 h or 2 years)	Requires MPPT for optimum performance Available only in small motor sizes Increasing current (by paralleling PV modules) increases the torque Increasing voltage (by series PV modules) increases the speed
Brushless DC	Efficient Less maintenance is required	Electronic computation adds to extra cost, complexity, and increased risk of failure/malfunction In most cases, oil cooled can't be submerged as deep as water cooled AC units	Growing trend among PV pump manufacturers to use brushless DC motors, primarily for centrifugal type submersible pumps
AC induction motors	No brushes to replace Can use existing AC motor/pump technology that is cheaper and easily available worldwide. These motors can handle larger pumping requirements	Needs an inverter to convert DC output from PV to AC adding additional cost and complexity Less efficient than DC motor-pump units Prone to overheating if current is not adequate to start the motor or if the voltage is too low	Available for single or three supply Inverters are designed to regulate frequency to maximize power to the motor in response to changing insolation levels

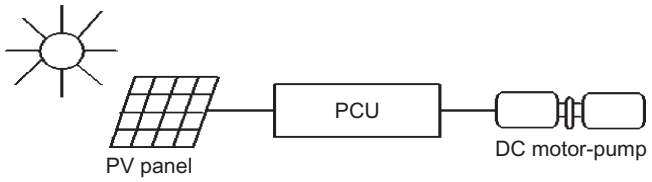


FIG. 25.24 Block diagram for DC motor-driven pumping scheme.

available driving voltage. Current lower than the acceptable limit will stop the pumping. When the light level increases, the operating point will shift from the MPP leading to the reduction of efficiency. For centrifugal pumps, there is an increase in current at increased speed, and the matching of *I-V* characteristics is closer for wide range of light intensity levels. For centrifugal pumps, the torque is proportional to the square of speed, and the torque produced by the motors is proportional to the current. Due to decrease in PV current output, the torque from the motor and consequently the speed of the pump are reduced, resulting in decrease in back emf and the required voltage of the motor. Maximum power point tracker can be used for controlling the voltage/current outputs from the PV inverters to operate the PV close to maximum operating point for the smooth operation of motor-pump units. The DC-DC converter can be used for keeping the PV panel output voltage constant and help in operating the solar arrays close to MPP. In the beginning, high starting current is required to produce high starting torque. The PV panels cannot supply this high starting current without adequate power-conditioning equipment like DC-DC converter or by using a starting capacitor. The DC-DC converter can generate the high starting currents by regulating the excess PV array voltage. DC-DC converter can be boost or buck converter.

Brushless DC motor (BDCM) and helical rotor pumps can also be used for PV water pumping [35]. Brushless DC motors are a self-synchronous type of motor characteristics by trapezoidal waveforms for back emf and air flux density. They can operate off a low-voltage DC supply that is switched through an inverter to create a rotating stator field. The current generations of BDCMs use rare-earth magnets on the rotor to give high air gap flux densities and are well suited to solar application. The block diagram of such an arrangement is shown in Fig. 25.25 that consists of PV panels, DC-DC converter, MPPT, and BDCM.

The PV inverters are used to convert the DC output of the solar arrays to the AC quantity so as to run the AC motor-driven pumps. These PV inverters can be variable frequency type, which can be controlled to operate the motors over wide range of loads. The PV inverters may involve impedance matching to match the electric characteristics of the load and array. The motor-pump unit and PV panels operate at their maximum efficiencies. Maximum power point tracker is also used in the power conditioning. To keep the voltage stable for the inverters, the DC-DC converter can be used. The inverter/converter has a capability of injecting high-switch-frequency components, which can lead to the overheating and the losses. So care shall be taken for this. The PV arrays are usually connected in series, parallel, or a combination of series-parallel configurations. The function of power electronic interface, as mentioned before, is to convert the DC power from

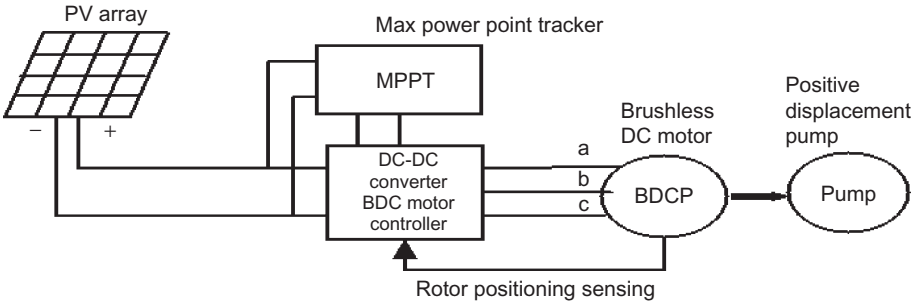


FIG. 25.25 Block diagram for BDCM for PV application.

the array to the required voltage and frequency to drive the AC motors. The motor-pump system load should be such that the array operates close to its MPP at all solar insolation levels. There are mainly three types of solar-powered water pumping systems as shown in Fig. 25.26.

The first system shown in Fig. 25.26A is an imported commercially available unit, which uses a specially wound low-voltage induction-motor-driven submersible pump. Such a low-voltage motor permits the PV array voltage to be converted to AC without using a step-up transformer. The second system, shown in Fig. 25.26B, makes use of a conventional "off-the-shelf" 415 V, 50 Hz induction motor [5]. This scheme needs a step-up transformer to raise inverter output voltage to high voltage. The third scheme as shown in Fig. 25.26C is composed of a DC-DC converter, an inverter that switches at a high frequency, and a mains voltage motor-driven pump. To get the optimum discharge (Q), at a given insolation level, the efficiency of the DC-DC converter and the inverter should be high. So the purpose should be to optimize the output from PV array, motor, and the pump. The principle used here is to vary the duty cycle of a DC-DC converter so that the output voltage is maximum. The DC-DC converter is used to boost the solar array voltage to eliminate the need for a step-up transformer and operate the array at the MPP. The three-phase inverter used in the interface is designed to operate in a variable frequency mode over the range of 20–50 Hz, which is the practical limit for most 50 Hz induction motor applications. Block diagram for frequency control is given in Fig. 25.27.

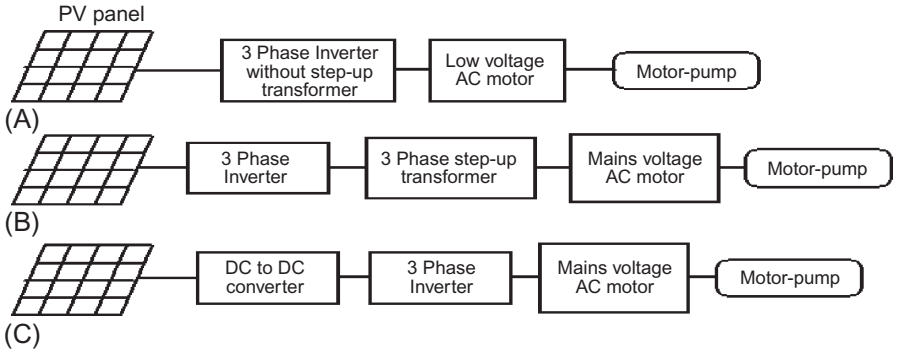


FIG. 25.26 Block diagrams for various AC motor-driven pumping schemes.

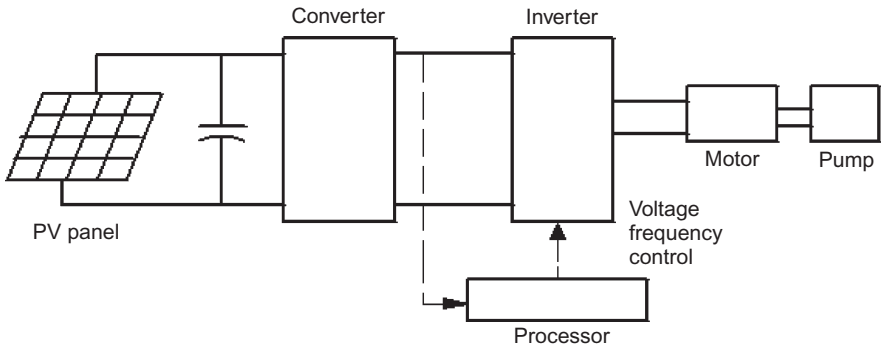


FIG. 25.27 Block diagram for voltage/frequency control.

This inverter would be suitable for driving permanent magnet motors by incorporating additional circuitry for position sensing of the motor's shaft. Also, the inverter could be modified, if required, to produce higher output frequencies for high-speed permanent magnet motors. The inverter has a three-phase full-bridge configuration implemented by MOSFET power transistors.

25.2.4 Grid-Connected PV Systems

The utility interactive inverters not only conditions the power output of the PV arrays but ensures that the PV system output is fully synchronized with the utility power. These systems can be batteryless or with battery backup. Systems with battery storage (or flywheel) provide additional power supply reliability. The grid connection of PV systems is gathering momentum because of various rebate and incentive schemes. This system allows the consumer to feed its own load utilizing the available solar energy, and the surplus energy can be injected into the grid under the energy by back scheme to reduce the payback period. Grid-connected PV systems can become a part of the utility system. The contribution of solar power depends upon the size of system and the load curve of the house. When the PV system is integrated with the utility grid, a two-way power flow is established. The utility grid will absorb excess PV power and will feed the house during nighttime and at instants while the PV power is inadequate. The utility companies are encouraging this scheme in many parts of the world. The grid-connected system can be classified as follows:

- Rooftop application of grid-connected PV system
- Utility-scale large system

For small household PV applications, a roof mounted PV array can be the best option. Solar cells provide an environmentally clean way of producing electricity, and rooftops have always been the ideal place to put them. With a PV array on the rooftop, the solar-generated power can supply residential load. The rooftop PV systems can help in reducing the peak summer load to the benefit of utility companies by feeding the household lighting, cooling, and other domestic loads. The battery storage can further improve the reliability of the system at the time of low insolation level, nighttime, or cloudy days. But the battery storage has some inherent problems like maintenance and higher cost.

For roof-integrated applications, the solar arrays can be either mounted on the roof or directly integrated into the roof. If the roof integration does not allow for an air channel behind the PV modules for ventilation purpose, then it can increase the cell temperature during the operation consequently leading to some energy losses. The disadvantage with the rooftop application is that the PV array orientation is dictated by the roof. In case, when the roof orientation differs from the optimal orientation required for the cells, then the efficiency of the entire system would be suboptimal.

Utility interest in PV has centered on the large grid-connected PV systems. In Germany, the United States, Spain, and in several other parts of the world, some large-scale PV plants have been installed. The utilities are more inclined with large-scale, centralized power supply. The PV systems can be centralized or distributed systems.

Grid-connected PV systems must observe the islanding situation, when the utility supply fails. In case of islanding, the PV generators should be disconnected from mains. PV generators can continue to meet only the local load, if the PV output matches the load. If the grid is reconnected during islanding, transient overcurrents can flow through the PV system inverters, and the protective equipments like circuit breakers may be damaged. The islanding control can be achieved through inverters or via the distribution network. Inverter controls can be designed on the basis of detection of grid voltage, measurement of impedance, frequency variation, or increase in harmonics. Protection shall be designed for the islanding, short circuits, over/under-voltages/currents, grounding, lightening, etc.

The importance of the power generated by the PV system depends upon the time of the day specially when the utility is experiencing the peak load. The PV plants are well suited to summer peaking, but it depends upon the climatic condition of the site. PV systems being investigated for use as peaking stations would be competitive for load management. The PV users can defer their load by adopting load management to get the maximum benefit out of the grid-connected PV plants and feeding more power into the grid at the time of peak load.

The assigned capacity credit is based on the statistical probability with which the grid can meet peak demand [3]. The capacity factor during the peaks is very similar to that of conventional plants, and similar capacity credit can be given for the PV generation except at the times when the PV plants are generating very less power unless adequate storage is provided. With the installation of PV plants, the need of extra transmission lines, transformers can be delayed or avoided. The distributed PV plants can also contribute in providing reactive power support to the grid and reduce burden on VAR compensators.

25.2.4.1 Inverters for Grid-Connected Applications

Power conditioner is the key link between the PV array and mains in the grid-connected PV system. It acts as an interface that converts DC current produced by the solar cells into utility grade AC current. The PV system behavior relies heavily on the power-conditioning unit. The inverters shall produce good quality sine-wave output. The inverter must follow the frequency and voltage of the grid, the inverter has to extract maximum power from the solar cells with the help of MPPT, and the inverter input stage varies the input voltage until the MPP on the *I-V* curve is found. The inverter shall monitor all the phases of the grid. The inverter output shall be controlled in terms of voltage and frequency variation. A typical grid-connected inverter may use a PWM scheme and operates in the range of 2–20 kHz.

25.2.4.2 Inverter Classifications

The inverters used for the grid interfacing are broadly classified as follows:

- Voltage-source inverters (VSI)
- Current-source inverters (CSI)

The inverters based on the control schemes can be classified as follows:

- Current controlled (CC)
- Voltage controlled (VC)

The source is not necessarily characterized by the energy source for the system. It is a characteristic of the topology of the inverter. It is possible to change from one source type to another source type by the addition of passive components. In the voltage-source inverter (VSI), the DC side is made to appear to the inverter as a voltage source. The VSIs have a capacitor in parallel across the input, whereas the CSIs have an inductor in series with the DC input. In the CSI, the DC source appears as a current source to the inverter. Solar arrays are fairly good approximation to a current source. Most PV inverters are voltage source even though the PV is a current source. Current-source inverters are generally used for large motor drives though there have been some PV inverters built using a current-source topology. The VSI is more popular with the PWM VSI dominating the sine-wave inverter topologies.

Fig. 25.28A shows a single-phase full-bridge bidirectional VSI with (A) voltage control and phase-shift (δ) control—voltage-controlled voltage-source inverter (VCVSI). The active power transfer from the PV panels is accomplished by controlling the phase angle δ between the converter voltage and the grid voltage. The converter voltage follows the grid voltage. Fig. 25.28B shows the same VSI operated as (B) current controlled (CCVSI). The objective of this scheme is to control active and reactive components of the current fed into the grid using PWM techniques.

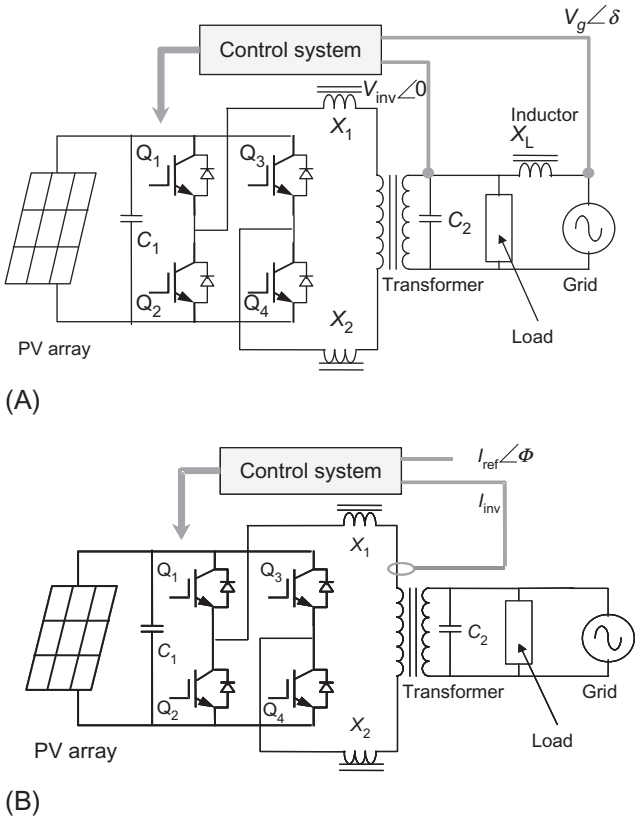


FIG. 25.28 Voltage-source inverter: (A) voltage control and (B) current control.

25.2.4.3 Inverter Types

Different types are being in use for the grid-connected PV applications such as the following:

- Line-commutated inverter
- Self-commutated inverter
- Inverter with high-frequency transformer

Line-commutated inverter

The line-commutated inverters are generally used for the electric motor applications. The power stage is equipped with thyristors. The maximum power tracking control is required in the control algorithm for solar application. The basic diagram for a single-phase line-commutated inverter is shown in Fig. 25.29 [2].

The driver circuit has to be changed to shift the firing angle from the rectifier operation ($0 < \phi < 90$) to inverter operation ($90 < \phi < 180$). Six-pulse or twelve-pulse inverters are used for the grid interfacing, but twelve-pulse inverters produce less harmonics. The thysistor-type inverters require a low-impedance grid interface connection for commutation purpose. If the maximum power available from the grid connection is less than twice the rated PV inverter power, then the line-commutated inverter should not be used [2]. The line-commutated inverters are cheaper but inhibits poor power quality. The harmonics injected into the grid can be large unless taken care of by employing adequate filters. These line-commutated inverters also have poor power factor, poor power quality, and need additional control to improve the power factor. Transformer can be used to provide the electric isolation. To suppress the harmonics generated by these inverters, tuned filters are employed, and reactive power compensation is required to improve the lagging power factor.

Self-commutated inverter

A switch-mode inverter using pulse-width modulated (PWM) switching control can be used for the grid connection of PV systems. The basic block diagram for this type of inverter is shown in Fig. 25.30. The inverter bridges may consist of bipolar transistors, MOSFET transistors, IGBTs, or gate turn-off thyristors (GTOs), depending upon the type of application. GTOs are

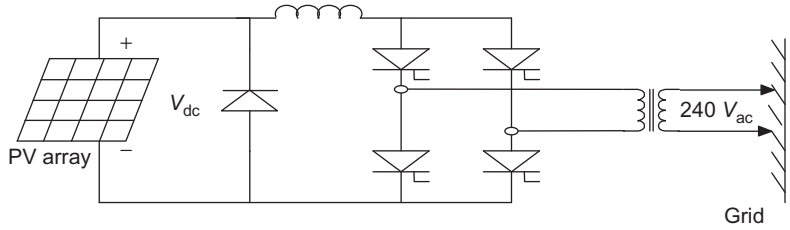


FIG. 25.29 Line-commuted single-phase inverter.

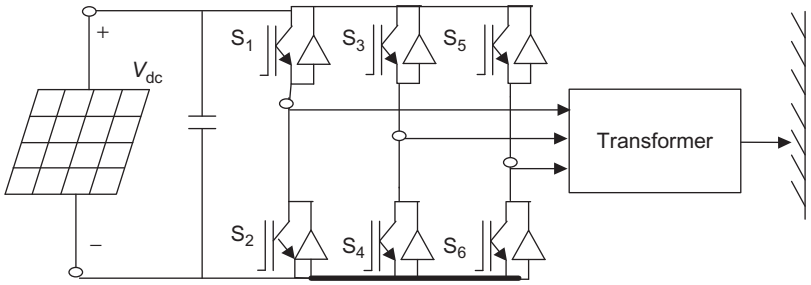


FIG. 25.30 Self-commutated inverter with PWM switching.

used for the higher-power applications, whereas IGBTs can be switched at higher frequencies, that is, 16 kHz, and are generally used for many grid-connected PV applications. Most of the present day inverters are self-commutated sine-wave inverters.

Based on the switching control, the voltage-source inverters can be further classified based on the switching control as follows:

- PWM (pulse-width modulated) inverters
- Square-wave inverters
- Single-phase inverters with voltage cancellations
- Programmed harmonic elimination switching
- Current-controlled modulation

Inverter with high-frequency transformer

The 50 Hz transformer for a standard PV inverter with PWM switching scheme can be very heavy and costly. While using frequencies more than 20 kHz, a ferrite core transformer can be a better option [2]. A circuit diagram of a grid-connected PV system using high-frequency transformer is shown in Fig. 25.31.

The capacitor on the input side of high-frequency inverter acts as the filter. The high-frequency inverter with PWM is used to produce a high-frequency AC across the primary winding of the high-frequency transformer. The secondary voltage of this transformer is rectified using high-frequency rectifier. The DC voltage is interfaced with a thyristor inverter through a low-pass inductor filter and hence connected to the grid. The line current is required to be sinusoidal and in phase with the line voltage. To achieve this, the line voltage (V_1) is measured to establish the reference waveform for the line current I_L*. This reference current I_L* multiplied by the transformer ratio gives the reference current at the output of a high-frequency inverter. The inverter output can be controlled using current control technique [36]. These inverters can be with low-frequency transformer isolation or high-frequency transformer isolation. The low-frequency (50–60 Hz) transformer of a standard

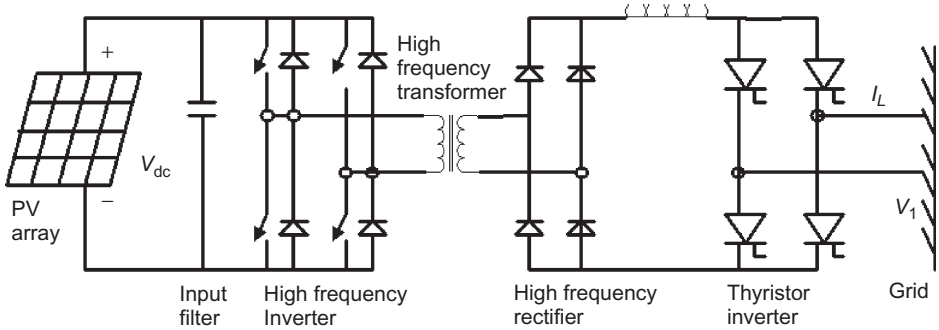


FIG. 25.31 PV inverter with high-frequency transformer.

inverter with PWM is a very heavy and bulky component. For residential grid-interactive rooftop inverters below 3 kW rating, high-frequency transformer isolation is often preferred.

Other PV inverter topologies

In this section, some of the inverter topologies discussed in various research papers have been discussed.

Multilevel converters: Multilevel converters can be used with large PV systems where multiple PV panels can be configured to create voltage steps. These multilevel voltage-source converters can synthesize the AC output terminal voltage from different level of DC voltages and can produce staircase waveforms. This scheme involves less complexity and needs less filtering. One of the schemes (half-bridge diode-clamped three-level inverter [37]) is given in Fig. 25.32. There is no transformer in this topology. Multilevel converters can be beneficial for large systems in terms of cost and efficiency. Problems associated with shading and malfunction of PV units need to be addressed.

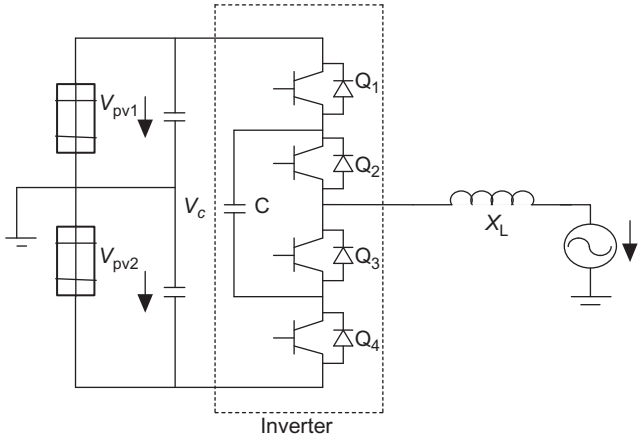


FIG. 25.32 Half-bridge diode-clamped three-level inverter.

The utilization of cascaded multilevel inverter (CMLI) in high-voltage and high-power PV energy conversion has been recently increased [38–40]. CMLI consists of a number of inverter units that are fed by isolated PV array [38]. Each unit utilizes low-voltage components, and the final output voltage is synthesized by combining all units in series. This topology has modular characteristic, since all the units are similar and have the same control strategy. This modularity feature makes it very easy to replace any faulty unit. Without discontinuing the load, it is also possible to bypass the faulty module by adopting a proper control technique [41].

Fig. 25.33 shows a five-level cascaded H-bridge inverter. Each inverter arm consists of a number of H-bridge units whose outputs are connected in series. Each unit comprises four switches (S_1–S_4) and one DC input supply ($\mathbf{V_{dc}}$). The basic H-bridge unit shown in Fig. 25.34 is able to produce three voltage levels ($-\mathbf{V_{dc}}$, 0, and $\mathbf{V_{dc}}$). The output voltage and switching logic of this H-bridge unit is shown in Table 25.2.

In Fig. 25.34, each phase arm contains two series-connected units. The output line voltages comprises five levels ($-2\,\mathbf{V_{dc}}$, $-\mathbf{V_{dc}}$, 0, $\mathbf{V_{dc}}$, and $2\,\mathbf{V_{dc}}$). If the number of units in each phase arm is "u," then the number of levels in the line voltage is ($l = 2u + 1$). All possible switching combinations for a five-level H-bridge inverter are presented in Table 25.3.

A three-phase "l"-level CHB MLI needs $6(l-1)$ switching devices. No additional diodes are needed, except the anti-parallel diodes in the switches. The current and voltage ratings of all switching devices are similar in case of symmetrical condition. In case of PV energy conversion, the input DC supplies of the H-bridge units are replaced by the PV arrays [42–45].

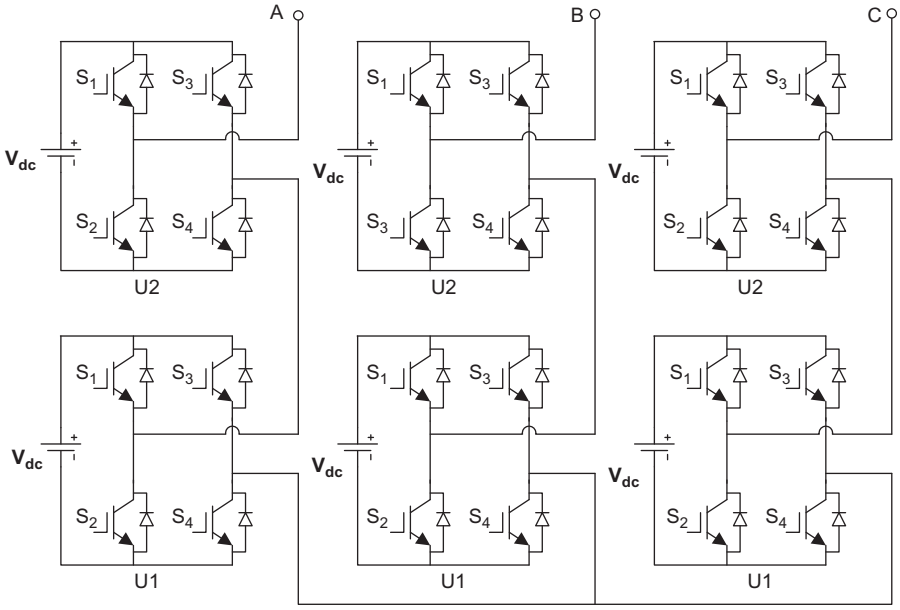


FIG. 25.33 Five-level cascaded H-bridge inverter.

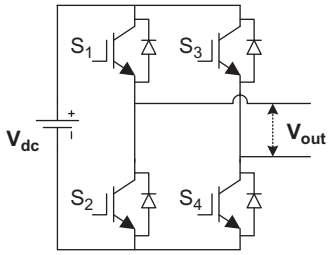


FIG. 25.34 Basic H-bridge unit.

TABLE 25.2 Switching logic of an H-bridge unit

V_{out}	Turn on switches
V_{dc}	S_1, S_4
0	S_1, S_3
	S_2, S_4
$-V_{dc}$	S_2, S_3

Non-insulated voltage source: In this scheme [46], string of low-voltage PV panels or one high-voltage unit can be coupled with the grid through DC-to-DC converter and voltage-source inverter. This topology is shown in Fig. 25.35. PWM switching scheme can be used to generate AC output. Filter has been used to reject the switching components.

Non-insulated current source: This type of configuration is shown in Fig. 25.36. Noninsulated current-source inverters [46] can be used to interface the PV panels with the grid. This topology involves low cost, which can provide better efficiency. Appropriate controller can be used to reduce current harmonics.

Buck converter with half-bridge transformer link: PV panels are connected to grid via buck converter and half bridge as shown in Fig. 25.37. In this, high-frequency PWM switching has been used at the low-voltage PV side to generate an attenuated rectified 100 Hz sine-wave current waveform

TABLE 25.3 All possible switching combination for various output levels of a 5-level CHB inverter

Unit / V_A	U1	U2	U1				U2			
	$V_{o,U1}$	$V_{o,U2}$	S_1	S_2	S_3	S_4	S_1	S_2	S_3	S_4
$\mathbf{2V_{dc}}$	$\mathbf{V_{dc}}$	$\mathbf{V_{dc}}$	1	0	0	1	1	0	0	1
$\mathbf{V_{dc}}$	$\mathbf{V_{dc}}$	0	1	0	0	1	1	0	1	0
	$\mathbf{V_{dc}}$	0	1	0	0	1	0	1	0	1
	0	$\mathbf{V_{dc}}$	1	0	1	0	1	0	0	1
	0	$\mathbf{V_{dc}}$	0	1	0	1	1	0	0	1
0	$\mathbf{V_{dc}}$	$\mathbf{-V_{dc}}$	1	0	0	1	0	1	1	0
	0	0	1	0	1	0	1	0	1	0
	0	0	1	0	1	0	0	1	0	1
	0	0	0	1	0	1	1	0	1	0
	0	0	0	1	0	1	0	1	0	1
	$\mathbf{-V_{dc}}$	$\mathbf{V_{dc}}$	0	1	1	0	1	0	0	1
$\mathbf{-V_{dc}}$	0	$\mathbf{-V_{dc}}$	1	0	1	0	0	1	1	0
	0	$\mathbf{-V_{dc}}$	0	1	0	1	0	1	1	0
	$\mathbf{-V_{dc}}$	0	0	1	1	0	1	0	1	0
	$\mathbf{-V_{dc}}$	0	0	1	1	0	0	1	0	1
$\mathbf{-2V_{dc}}$	$\mathbf{-V_{dc}}$	$\mathbf{-V_{dc}}$	0	1	1	0	0	1	1	0

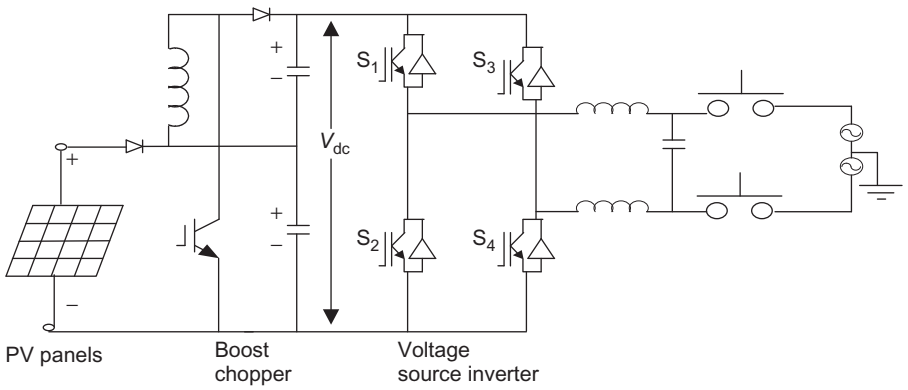


FIG. 25.35 Noninsulated voltage source.

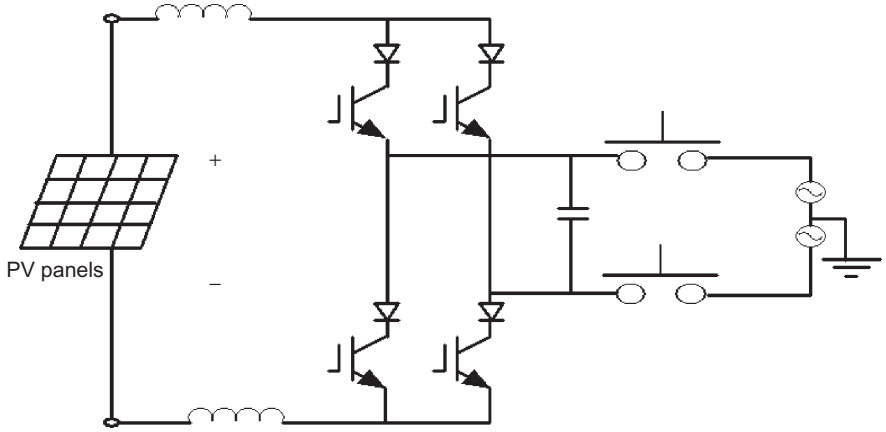


FIG. 25.36 Noninsulated current source.

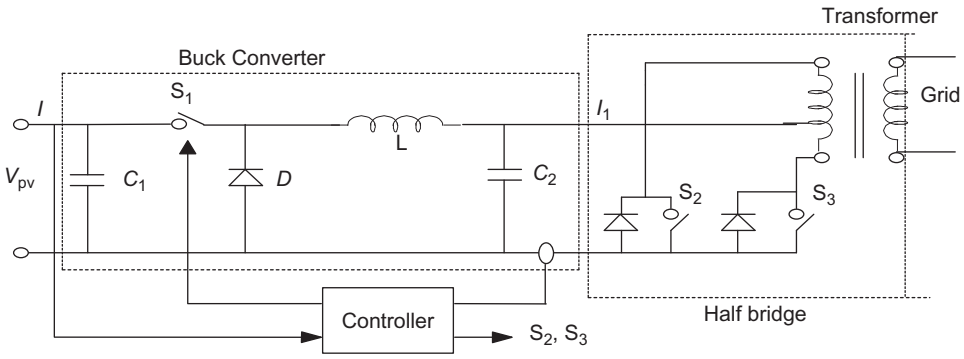


FIG. 25.37 Buck converter with half-bridge transformer link.

[47]. Half-wave bridge is utilized to convert this output to 50 Hz signal suitable for grid interconnection. To step up the voltage, the transformer has also been connected before the grid connection point.

Flyback converter: This converter topology steps up the PV voltage to DC bus voltage. Pulse-width-modulation-operated converter has been used for grid connection of PV system (Fig. 25.38). This scheme is less complex and has less number of switches. Flyback converters can be beneficial for remote areas due to less complex power-conditioning components.

Interface using paralleled PV panels: Low-voltage AC bus scheme [48] can be comparatively efficient and cheaper option. One of the schemes is shown in Fig. 25.39. A number of smaller PV units can be paralleled together and then connected to combine single low-frequency transformer. In this scheme, the PV panels are connected in parallel rather than series to avoid problems associated with shading or malfunction of one of the panels in series connection.

25.2.4.4 Power Control through PV Inverters

The system shown in Fig. 25.40 shows control of power flow onto the grid [49]. This control can be an analog or a

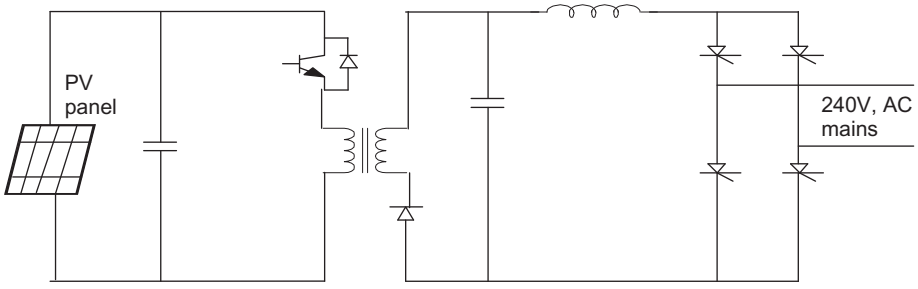


FIG. 25.38 Flyback converter.

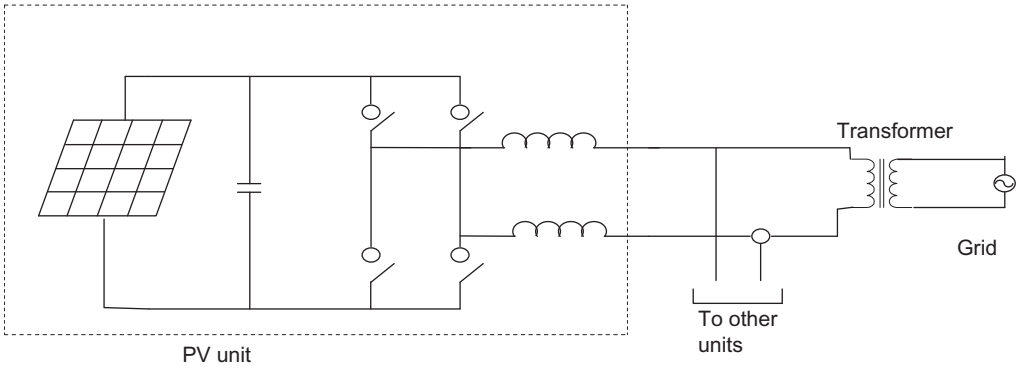


FIG. 25.39 Converter using parallel PV units.

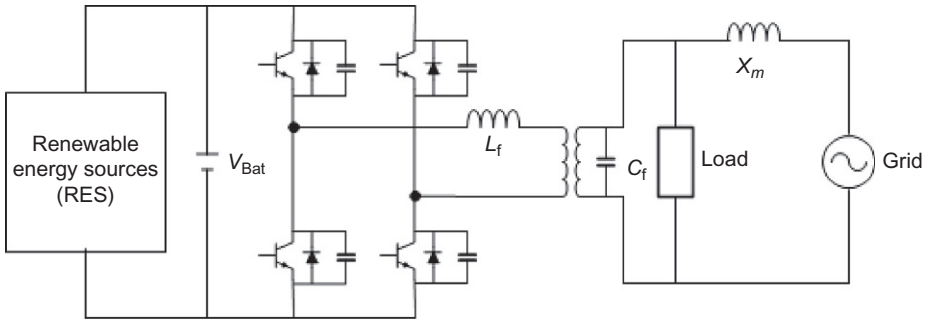


FIG. 25.40 Schematic diagram of a parallel processing DGS.

microprocessor system. This control system generates the waveforms and regulates the waveform amplitude and phase to control the power flow between the inverter and the grid. The grid-interfaced PV inverters, voltage-controlled VSI (VCVSI), and current-controlled VSI (CCVSI) have the potential of bidirectional power flow. They not only can feed the local load but also can export the excess active and reactive power to the utility grid. An appropriate controller is required in order to avoid any error in power export due to errors in synchronization, which can overload the inverter.

There are advantages and limitations associated with each control mechanism. For instance, VCVSIs provide voltage support to the load (here, the VSI operates as a voltage source), while CCVSIs provide current support (here, the VSI operates as a current source). The CCVSI is fast in response compared with the VCVSI, as its power flow is controlled by the switching instant, whereas in the VCVSI the power flow is controlled by adjusting the voltage across the decoupling inductor. Active and reactive powers are controlled independently in the CCVSI but are coupled in the VCVSI. Generally, the advantages of one type of VSI are considered as a limitation of the other type [50].

Fig. 25.41 shows the simplified/equivalent schematic diagram of a VCVSI. For the following analysis, it is assumed that the output low-pass filters (L_f and C_f) of VSIs will filter out high-order harmonics generated by PWMs. The decoupling inductor (X_m) is an essential part of any VCVSI as it makes the power flow control possible. In a VCVSI, the power flow of the distributed generation system (DGS) is controlled by adjusting the amplitude and phase (power angle (δ)) of the inverter output voltage with respect to the grid voltage. Hence, it is important to consider the proper sizing of the decoupling inductor and the maximum power angle to provide the required power flow when designing VCVSIs. The phasor diagram of a simple grid-inverter interface with a first-order filter is shown in Fig. 25.42.

Referring to Fig. 25.41, the fundamental grid current (I_g) can be expressed by Eq. (25.7):

$$I_g = \frac{V_g < 0 - V_c < \delta}{jX_m} = -\frac{V_c \sin\delta}{X_m} - j\frac{V_g - V_c \cos\delta}{X_m} \tag{25.7}$$

where V_g and V_c are, respectively, the grid and the VCVSI's fundamental voltages and X_m is the decoupling inductor impedance. Using per-unit values ($S_{base} = V_{base}^2/Z_{base}$, $V_{base} = V_c$, and $Z_{base} = X_m$) where V_{base}, Z_{base}, and S_{base} are the base voltage, impedance, and complex power values, respectively, the grid apparent power can be expressed as Eq. (25.8):

$$S_{gpu} = -V_{gpu} \sin\delta + j\left(V_{gpu}^2 - V_{gpu} \cos\delta\right) \tag{25.8}$$

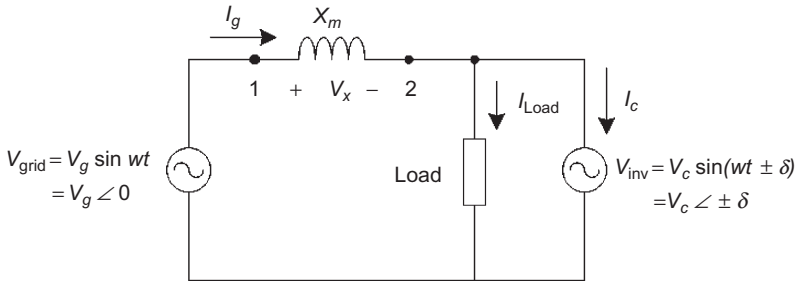


FIG. 25.41 The equivalent circuit diagram of a VCVSI.

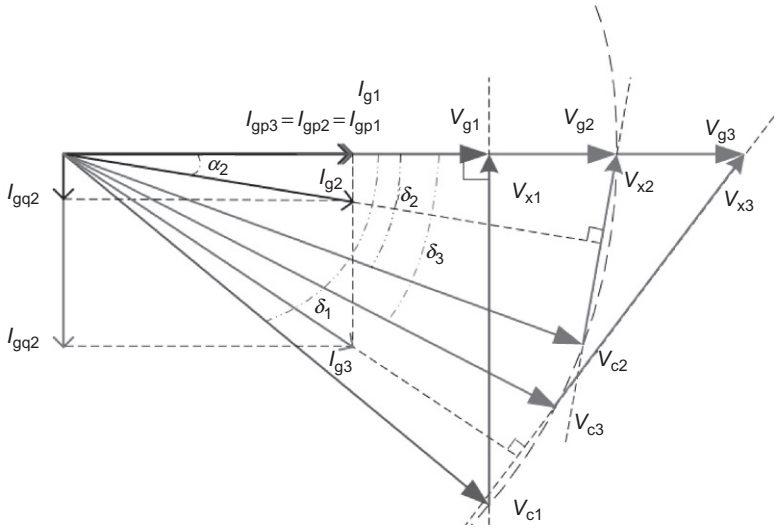


FIG. 25.42 Phasor diagram of a VCVSI with resistive load and assuming the grid is responsible for supplying the active power [50].

Using per-unit values, the complex power of the VCVSI and decoupling inductor are

$$S_{cpu} = -V_{gpu}\sin\delta + j\left(V_{gpu}\cos\delta - 1\right) \tag{25.9}$$

$$S_{xpu} = j\left(V_{gpu}^2 - 2V_{gpu}\cos\delta + 1\right) \tag{25.10}$$

where S_{gpu}, S_{cpu}, and S_{xpu} are per-unit values of the grid, VCVSI, and decoupling inductor apparent power, respectively, and V_{gpu} is the per-unit value of the grid voltage.

Fig. 25.43 shows the equivalent schematic diagram of a CCVSI. As a CCVSI controls the current flow using the VSI switching instants, it can be modeled as a current source, and there is no need for a decoupling inductor (Fig. 25.43). As the current generated from the CCVSI can be controlled independently from the AC voltage, the active and reactive power controls are decoupled. Hence, unity power factor operation is possible for the whole range of the load. This is one of the main advantages of CCVSIs.

As the CCVSI is connected in parallel to the DGS, it follows the grid voltage. Fig. 25.44 shows the phasor diagram of a CCVSI-based DGS in the presence of an inductive load (considering the same assumption as VCVSI section). Fig. 25.44 shows that when the grid voltage increases, the load's active power consumption, which is supplied by the grid, increases and the CCVSI compensates the increase in the load reactive power demand. In this case, the CCVSI maintains grid supply

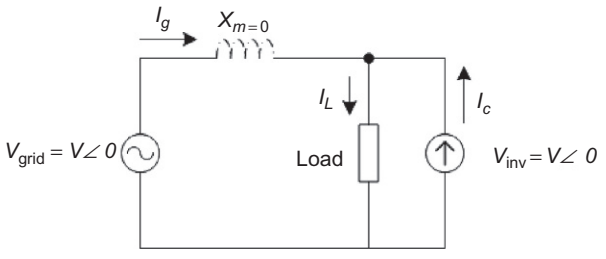


FIG. 25.43 The equivalent circuit of a CCVSI.

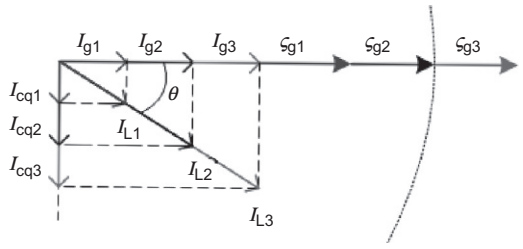


FIG. 25.44 Phasor diagram of a CCVSI with inductive load and assuming grid is responsible for supplying the active power [50].

at unity power factor, keeping the current phase delay with respect to the grid voltage at a fixed value (θ). Therefore, the CCVSI cannot maintain the load voltage in the presence of a DGS without utilizing extra hardware and control mechanisms. This limitation on load voltage stabilization is one of the main drawbacks of CCVSI-based DGS.

Assuming the load active current demand is supplied by the grid (reactive power support function), the required grid current can be rewritten as follows:

$$I_g^* = \mathrm{Re}[I_L] = \mathrm{Re}\left[\frac{S_L}{V_g}\right] \tag{25.11}$$

where S_L is the demanded load apparent power. For grid power conditioning, it is preferred that the load operate at unity power factor. Therefore, the CCVSI must provide the remainder of the required current in Eq. (25.12):

$$I_c = I_L - I_g^* \tag{25.12}$$

For demand side management (DSM), it is desirable to supply the active power by the RES, where excess energy from the RES is injected into the DGS. The remaining load reactive power will be supplied by the CCVSI. Hence, Eq. (25.12) can be rewritten as Eq. (25.13):

$$I_g^* = \mathrm{Re}[I_L] - \mathrm{Re}[I_c] = \mathrm{Re}\left[\frac{S_L - P_{RES}}{V_g}\right] \tag{25.13}$$

When using a voltage controller for grid-connected PV inverter, it has been observed that a slight error in the phase of synchronizing waveform can grossly overload the inverter whereas a current controller is much less susceptible to voltage phase shifts [49]. Due to this reason, the current controllers are better suited for the control of power export from the PV inverters to the utility grid since they are less sensitive to errors in synchronizing sinusoidal voltage waveforms.

A prototype current-controlled-type power-conditioning system has been developed by the first author and tested on a weak rural feeder line at Kalbarri in Western Australia [51]. The choice may be between additional conventional generating capacities at a centralized location and adding smaller distributed generating capacities using RES like PV. The latter option can have a number of advantages like as follows:

- The additional capacity is added wherever it is required without adding additional power distribution infrastructure. This is a critical consideration where the power lines and transformers are already at or close to their maximum ratings.
- The power-conditioning system can be designed to provide much more than just a source of real power, for minimal extra cost. A converter providing real power needs only a slight increase in ratings to handle significant amounts of reactive or even harmonic power. The same converter that converts DC PV power to AC power can simultaneously provide the reactive power support to the week utility grid.

The block diagram of the power-conditioning system used in the Kalbarri project has been shown in Fig. 25.45. This CCVSI operates with a relatively narrow switching frequency band near 10 kHz. The control diagram indicates the basic operation of the power-conditioning system. The two outer control loops operate to independently control the real and reactive power flow from the PV inverter. The real power is controlled by an outer MPPT algorithm with an inner DC link voltage control loop providing the real current magnitude request I_P*, and hence, the real power export through PV converter is controlled through the DC link voltage regulation. The DC link voltage is maintained at a reference value by a PI control loop, which gives the real current reference magnitude as its output. At regular intervals, the DC link voltage is scanned over the entire voltage range to check that the algorithm is operating on the absolute MPP and is not stuck around a local MPP. During the night, the converter can still be used to regulate reactive power of the grid-connected system although it cannot provide active power. During this time, the PI controller maintains a minimum DC link voltage to allow the power-conditioning system to continue to operate, providing the necessary reactive power.

The AC line voltage regulation is provided by a separate reactive power control, which provides the reactive current magnitude reference I_Q*. The control system has a simple transfer function, which varies the reactive power command in response to the AC voltage fluctuations. Common to the

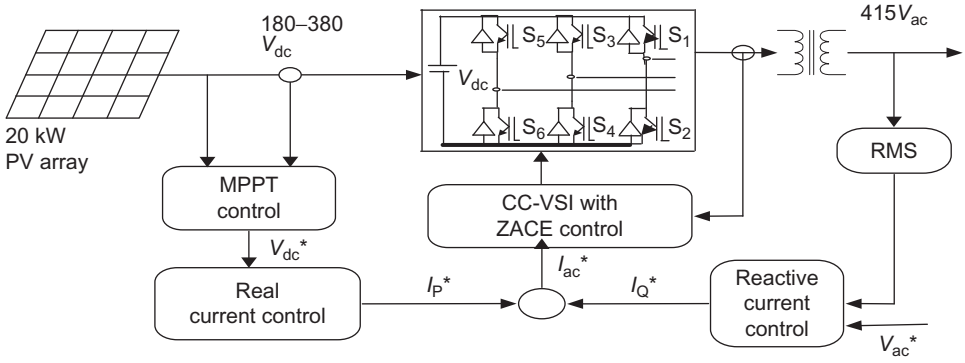


FIG. 25.45 Block diagram of Kalbarri power-conditioning system.

outer real and reactive power control loops is an inner higher bandwidth zero average current error (ZACE) current control loop. I_p* is in phase with the line voltages, and I_Q* is at 90° to the line voltage. These are added together to give one (per phase) sinusoidal converter current reference waveform (I_{ac}*). The CCVSI control consists of analog and digital circuitry that acts as a ZACE transconductance amplifier in converting I_{ac}* into AC power currents [52].

25.2.4.5 System Configurations

The utility compatible inverters are used for power conditioning and synchronization of PV output with the utility power. In general, four types of batteryless grid-connected PV system configurations have been identified:

- Central plant inverter
- Multiple string DC/DC converter with single-output inverter
- Multiple string inverter
- Module-integrated inverter

Central plant inverter

In the central plant inverter, usually a large inverter is used to convert DC power output of PV arrays to AC power. In this system, the PV modules are serially stringed to form a panel (or string), and several such panels are connected in parallel to a single DC bus. The block diagram of such a scheme is shown in Fig. 25.46.

Multiple string DC/DC converter

In multiple string DC/DC converter, as shown in Fig. 25.47, each string will have a boost DC/DC converter with transformer isolation. There will be a common DC link, which feeds a transformerless inverter.

Multiple string inverters

Fig. 25.48 shows the block diagram of multiple string inverter system. In this scheme, several modules are connected in series on the DC side to form a string. The output from each string is converted to AC through a smaller individual inverter. Many such inverters are connected in parallel on the AC side. This arrangement is not badly affected by the shading of the panels. It is also not seriously affected by inverter failure.

Module integrated inverter

In the module-integrated inverter system (Fig. 25.49), each module (typically 50–300 W) will have a small inverter. No cabling is required. It is expected that high volume of small inverters will bring down the cost.

25.2.4.6 Grid-Compatible Inverters Characteristics

The characteristics of the grid-compatible inverters are as follows:

- Response time
- Power factor
- Frequency control
- Harmonic output
- Synchronization
- Fault current contribution
- DC current injection
- Protection

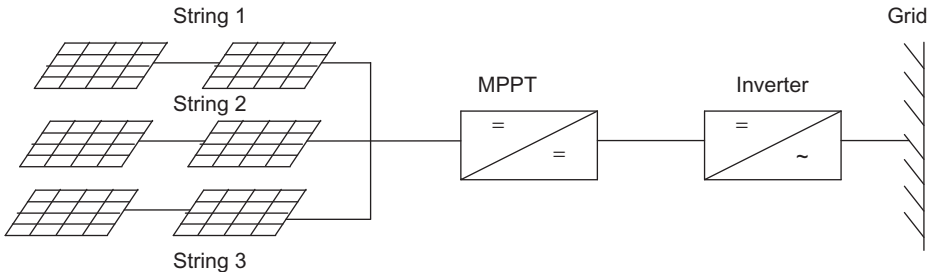


FIG. 25.46 Central plant inverter.

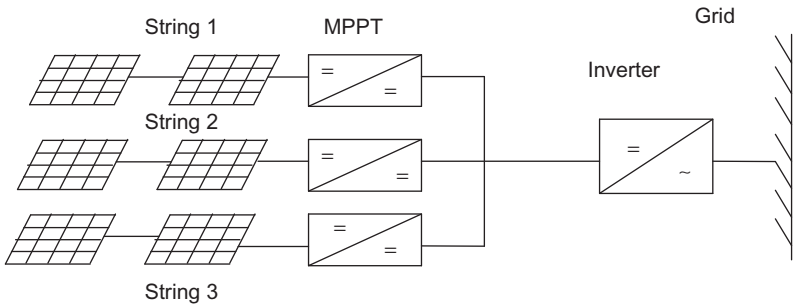


FIG. 25.47 Multiple string DC/DC converter.

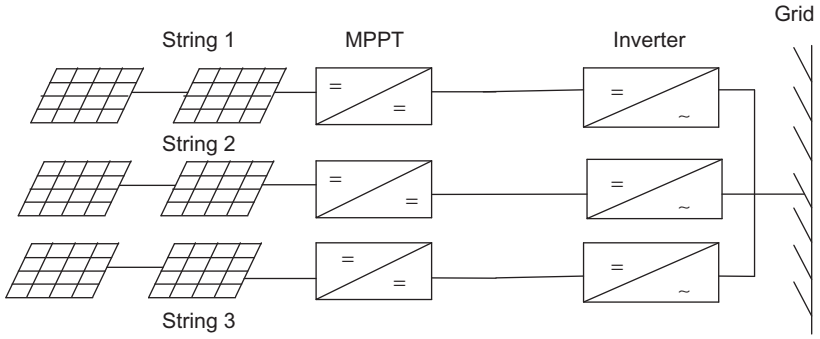


FIG. 25.48 Multiple string inverter.

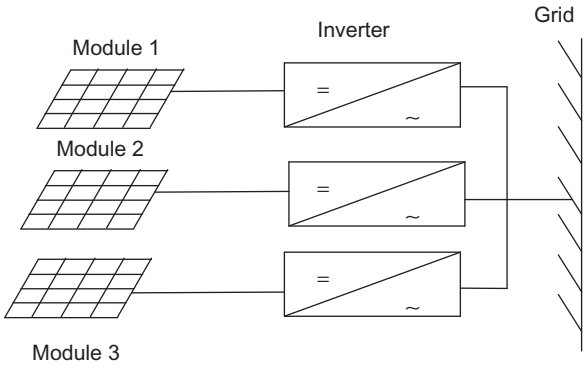


FIG. 25.49 Module-integrated inverter.

The response time of the inverters shall be extremely fast and governed by the bandwidth of the control system. The absence of rotating mass and use of semiconductor switches allow inverters to respond in millisecond time frame. The power factor of the inverters is traditionally poor due to displacement power factor and the harmonics. But with the latest development in the inverter technology, it is possible to maintain the power factor close to unity. The converters/inverters have the capability of creating large voltage fluctuation by drawing reactive power from the utility rather than supplying [53]. With proper control, inverters can provide voltage support by importing/exporting reactive power to push/pull toward a desired set point. This function would be of more use to the utilities as it can assist in the regulation of the grid system at the domestic consumer level.

Frequency of the inverter output waveshape is locked to the grid. Frequency bias is where the inverter frequency is deliberately made to run at 53 Hz. When the grid is present, this will be pulled down to the nominal 50 Hz. If the grid fails, it will drift upward toward 53 Hz and trip on overfrequency. This can help in preventing islanding.

Harmonics output from the inverters have been very poor traditionally. Old thyristor-based inverters are operated with slow switching speeds and could not be pulse-width modulated. This resulted in inverters known as 6-pulse or 12-pulse inverters. The harmonics so produced from the inverters can be injected into the grid, resulting in losses, heating of appliances, tripping of protection equipments, and poor power quality. The number of pulses is being the number of steps in a sine-wave cycle. With the present advent in the power electronics technology, the inverter controls can be made very well. Pulse-width-modulated inverters produce high-quality sine waves. The harmonic levels are very low and can be lower than the common domestic appliances. If the harmonics are present in the grid voltage waveform, harmonic currents can be induced in the inverter. These harmonic currents, particularly those generated by a voltage-controlled inverter, will in fact help in supporting the grid. These are good harmonic currents. This is the reason that the harmonic current output of inverters must be measured onto a clean grid source so that the only harmonics being produced by the inverters are measured.

Synchronization of inverter with the grid is performed automatically and typically uses zero-crossing detection on the voltage waveform. An inverter has no rotating mass and hence has no inertia. Synchronization does not involve the acceleration of a rotating machine. Consequently, the reference waveforms in the inverter can be jumped to any point required within a sampling period. If phase-locked loops are used, it could take up a few seconds. Phase-locked loops are used to increase the immunity to noise. This allows the synchronization to be based on several cycles of zero-crossing information. The response time for this type of locking will be slower.

Photovoltaic panels produce a current that is proportional to the amount of light falling on them. The panels are normally rated to produce 1000 W/m^2 at 25°C. Under these conditions, the short-circuit current possible from these panels is typically only 20% higher than the nominal current, whereas it is extremely variable for wind. If the solar radiation is low, then the maximum current possible under short circuit is going to be less than the nominal full-load current. Consequently, PV systems cannot provide the short-circuit capacity to the grid. If a battery is present, the fault current contribution is limited by the inverter. With the battery storage, it is possible for the battery to provide the energy. However, inverters are typically limited between 100% and 200% of nominal rating under current limit conditions. The inverter needs to protect itself against the short circuits because the power electronic components will

typically be destroyed before a protection device like circuit breaker trips.

In case of inverter malfunction, inverters have the capability to inject the DC components into the grid. Most utilities have guidelines for this purpose. A transformer shall be installed at the point of connection on the AC side to prevent DC from entering into the utility network. The transformer can be omitted when a DC detection device is installed at the point of connection on the AC side in the inverter. The DC injection is essentially caused by the reference or power electronic device producing a positive half cycle that is different from the negative half cycle resulting in the DC component in the output. If the DC component can be measured, it can then be added into the feedback path to eliminate the DC quantity.

Protection requirements

A minimum requirement to facilitate the prevention of islanding is that the inverter energy system protection operates and isolates the inverter energy system from the grid if

- Overvoltage,
- Undervoltage,
- Overfrequency,
- Underfrequency exist.

These limits may be either factory set or site programmable. The protection voltage operating points may be set in a narrower band if required, for example, 220–260 V. In addition to the passive protection detailed above and to prevent the situation where islanding may occur because multiple inverters provide a frequency reference for one another, inverters must have an accepted active method of islanding prevention following grid failure, for example, frequency drift and impedance measurement. Inverter controls for islanding can be designed on the basis of detection of grid voltage, measurement of impedance, frequency variation, or increase in harmonics. This function must operate to force the inverter output outside the protection tolerances specified previously, thereby resulting in isolation of the inverter energy system from the grid. The maximum combined operation time of both passive and active protections should be 2 s after grid failure under all local load conditions. If frequency shift is used, it is recommended that the direction of shift be down. The inverter energy system must remain disconnected from the grid until the reconnection conditions are met. Some inverters produce high-voltage spikes, especially at light load, which can be dangerous for the electronic equipment. IEEE P929 gives some idea about the permitted voltage limits.

If the inverter energy system does not have the above frequency features, the inverter must incorporate an alternate anti-islanding protection feature that is acceptable to the relevant electricity distributor. If the protection function above is to be incorporated in the inverter, it must be type tested for compliance with these requirements and accepted by the relevant electricity distributor. Otherwise, other forms of external protection relaying are required that have been type tested for compliance with these requirements and approved by the relevant electricity distributor. The inverter shall have adequate protection against short circuit, other faults, and overheating of inverter components.

25.3 Power Electronics for Wind Power Systems

In the rural United States, the first windmill was commissioned in 1890 to generate electricity. Today, large wind generators are competing with utilities in supplying clean power economically. The average wind turbine size has been 300–600 kW until recently. The new wind generators of 1–3 MW have been developed and are being installed worldwide, and prototype of even higher capacity is under development. Improved wind turbine designs and plant utilization have resulted in significant reduction in wind energy generation cost from 35 cents/kWh in 1980 to less than 5 cents/kWh in 1999, in locations where wind regime is favorable. At this generation cost, wind energy has become one of the least cost power sources. Main factors that have contributed to the wind power technology development are as follows:

- High-strength fiber composites for manufacturing large low-cost blades
- Variable-speed operation of wind generators to capture maximum energy
- Advancement in power electronics and associated cost
- Improved plant operation and efficiency
- Economy of scale due to the availability of large wind generation plants
- Accumulated field experience improving the capacity factor
- Computer prototyping by accurate system modeling and simulation

Table 25.4 is for wind sites with average annual wind speed of 7 m/s at 30 m hub height. Since the 1980s, wind technology capital costs have reduced by 80% worldwide. Operation and maintenance costs have declined by 80%, and the availability factor of grid-connected wind plants has increased to 95%. At present, the capital cost of wind generator plants has dropped to about $600/kW, and the electricity generation cost has reduced to 6 cents/kWh. It is expected to reduce the

TABLE 25.4 Wind power technology developments

	1980	1999	Future
Cost per kilowatt-hour	$0.35–0.40	$0.05–0.07	<$0.04
Capital cost per kilowatt	$2000–3000	$500–700	<$400
Operating life	5–7 years	20 years	30 years
Capacity factor (average)	15%	25%–30%	>30%
Availability	50%–65%	95%	>95%
Wind turbine unit size range	50–150 kW	300–1000 kW	500–2000 kW

generation cost below 4 cents/kWh. Keeping this in view, the wind generation is going to be highly competitive with the conventional power plants. In Europe, the United States, and Asia, the wind power generation is increasing rapidly, and this trend is going to continue due to economic viability of wind power generation.

The technical advancement in power electronics is playing an important part in the development of wind power technology. The contribution of power electronics in control of fixed-speed/variable-speed wind turbines and interfacing to the grid is of extreme importance. Because of the fluctuating nature of wind speed, the power quality and reliability of the wind-based power system needs to be evaluated in detail. Appropriate control schemes require power conditioning.

25.3.1 Basics of Wind Power

The ability of a wind turbine to extract power from wind is a function of three main factors:

- Wind power availability
- Power curve of the machine
- Ability of the machine to respond to wind perturbations

The mechanical power produced by a wind turbine is given by

$$P_m = 0.5\rho C_p A U^3 \text{ W} \tag{25.14}$$

The power from the wind is a cubic function of wind speed. The curve for power coefficient C_p and λ is required to infer the value of C_p for λ based on wind speed at that time.

Where tip-speed ratio, $\lambda = \frac{r\omega_A}{U}$, ρ = air density, Kg m^{-3}, C_p = power coefficient, A = wind turbine rotor swept area, m^2, and U = wind speed in meters per second.

The case of a variable-speed wind turbine with a pitch mechanism that alters the effective rotor dynamic efficiency can be easily considered if an appropriate expression for C_p as a function of the pitch angle is applied. The power curve of a typical wind turbine is given in Fig. 25.50 as a function of wind speed.

The C_p–λ curve for 150 kW windmaster machine is given in Fig. 25.51, which has been inferred from the power curve of the machine. The ratio of shaft power to the available power in the wind is the efficiency of conversion, known as the power coefficient C_p:

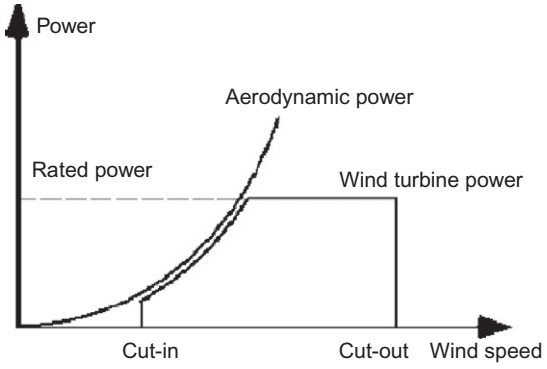


FIG. 25.50 Power curve of wind turbine as a function of wind speed [54].

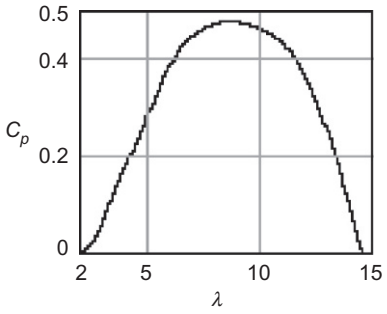


FIG. 25.51 Cp–λ curve of wind machine [54].

$$C_p = \frac{P_m}{(1/2\rho A U^3)} \tag{25.15}$$

The power coefficient is a function of turbine blade tip-speed to wind-speed ratio (β). A tip-speed ratio of 1 means the blade tips are moving at the same speed as the wind, and when β is 2, the tips are moving at twice the speed of the wind and so on [55]. Solidity (σ) is defined as the ratio of the sum of the width of all the blades to the circumference of the rotor. Hence,

$$\sigma = Nd/(2\pi R) \tag{25.16}$$

where N = number of blades and d = width of the blades.

The power from a wind turbine doubles as the area swept by the blades doubles. But doubling of the wind speed increases the power output eight times. Fig. 25.52 gives a family of power curves for a wind turbine. If the loading of the turbine is controlled such that the operating point is along the maximum power locus at different wind speeds, then the wind energy system will be more efficient.

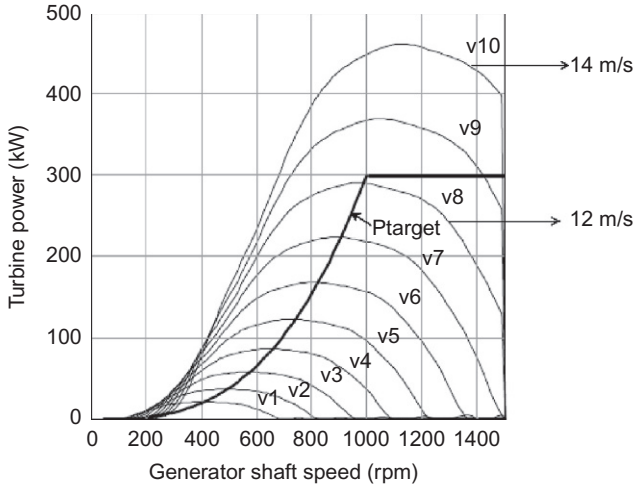


FIG. 25.52 Turbine power vs shaft speed curves.

25.3.1.1 Types of Wind Turbines

There are two types of wind turbines available Fig. 25.53:

- Horizontal-axis wind turbines (HAWTs)
- Vertical-axis wind turbines (VAWTs)

Vertical-axis wind turbines (VAWTs) have an axis of rotation that is vertical, and so, unlike the horizontal wind turbines, they can capture winds from any direction without the need to reposition the rotor when the wind direction changes (without a special yaw mechanism). Vertical-axis wind turbines were also used in some applications as they have the advantage that they do not depend on the direction of the wind. It is possible to extract power relatively easier. But there are some disadvantages such as no self-starting system, smaller power coefficient than obtained in the horizontal-axis wind turbines, strong discontinuation of rotations due to periodic changes in the lift force, and the regulation of power that is not yet satisfactory.

The horizontal-axis wind turbines are generally used. Horizontal-axis wind turbines are, by far, the most common design. There are a large number of designs commercially available ranging from 50 W to 4.5 MW. The number of blades ranges from one to many in the familiar agriculture windmill. The best compromise for electricity generation, where high rotational speed allows the use of a smaller and cheaper electric generator, is two or three blades. The mechanical and aerodynamic balance is better for three-bladed rotor. In small wind turbines, three blades are common. Multiblade wind turbines are used for water pumping on farms.

Based on the pitch control mechanisms, the wind turbines can also be classified as follows:

- Fixed-pitch wind turbines
- Variable-pitch wind turbines

Different manufacturers offer fixed-pitch and variable-pitch blades. Variable pitch is desirable on large machines because the aerodynamic loads on the blades can be reduced and when used in fixed-speed operation they can extract more energy. But necessary mechanisms require maintenance, and for small machines, installed in remote areas, fixed pitch seems more desirable and economical. In some machines, power output regulation involves yawing blades so that they no longer point into the wind. One such system designed in Western Australia has a tail that progressively tilts the blades in a vertical plane so that they present a small surface to the wind at high speeds.

The active power of a wind turbine can be regulated either by designing the blades to go into an aerodynamic stall beyond the designated wind speed or by feathering the blades out of the wind, which results in reducing excess power using a mechanical and electric mechanism. Recently, an active stall has been used to improve the stability of wind farms. This stall mechanism can prevent power deviation from gusty winds to pass through the drivetrain [56].

Horizontal-axis wind turbines can be further classified into fixed speed (FS) or variable speed (VS). The FS wind turbine (FSWT) generator is designed to operate at maximum efficiency while operating at a rated wind speed. In this case, the optimum tip-speed ratio is obtained for the rotor airfoil

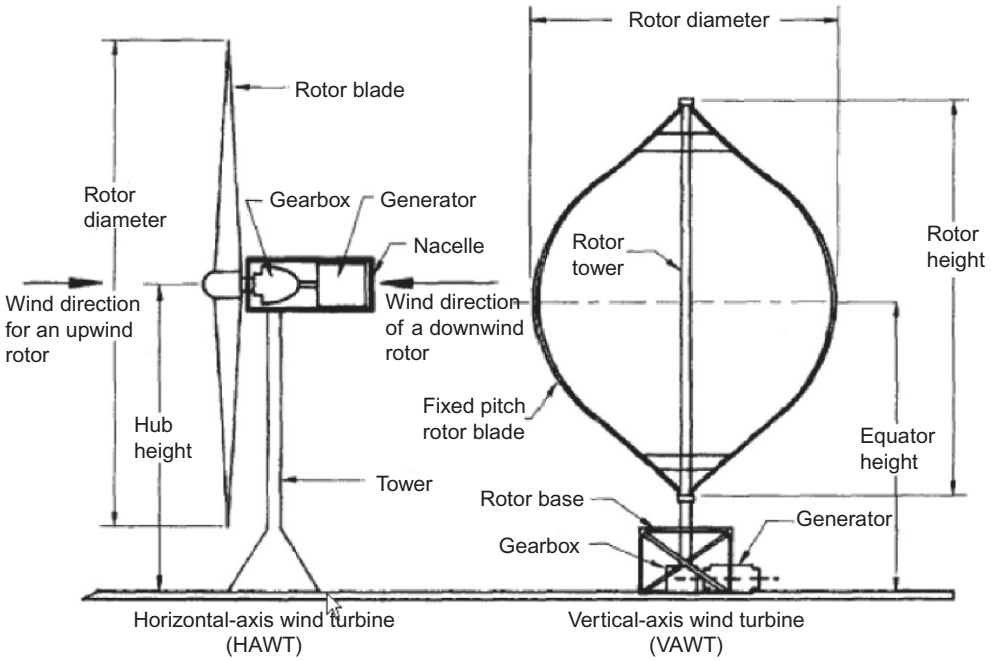


FIG. 25.53 Typical diagram of HAWTs and VAWTs.

at a rated wind speed. For a VS wind turbine (VSWT) generator, it is possible to obtain optimum wind speed at different wind speeds. Hence, this enables the VS wind turbine to increase its energy capture. The general advantages of a VSWT are summarized as follows:

- VSWTs are more efficient than the FSWTs.
- At low wind speeds, the wind turbines can still capture the maximum available power at the rotor, hence increasing the possibility of providing the rated power for wide speed range.

25.3.1.2 Types of Wind Generators

Schemes based on permanent magnet synchronous generators (PMSG) and induction generators are receiving close attention in wind power applications because of their qualities such as ruggedness, low cost, manufacturing simplicity, and low-maintenance requirements. Despite many positive features over the conventional synchronous generators, the PMSG was not being used widely [22]. However, with the recent advent in power electronics, it is now possible to control the variable voltage, variable frequency output of PMSG. The permanent magnet machine is generally favored for developing new designs, because of higher efficiency and the possibility of a rather smaller diameter. These PMSG machines are now being used with variable-speed wind machines.

In large power system networks, synchronous generators are generally used with fixed-speed wind turbines. The synchronous generators can supply both the active and reactive power, and their reactive power flow can be controlled. The synchronous generators can operate at any power factor. For the induction generator, driven by a wind turbine, it is a well-known fact that it can deliver only active power while consuming reactive power.

Synchronous generators with high power rating are significantly more expensive than induction generators of similar size. Moreover, direct-connected synchronous generators have the limitation of rotational speed being fixed by the grid frequency. Hence, fluctuation in the rotor speed due to wind gusts leads to higher torque in high power output fluctuations and the derived train. Therefore, in grid-connected application, synchronous generators are interfaced via power converters to the grid. This also allows the synchronous generators to operate wind turbines in VS, which makes gearless operation of the VSWT possible.

The squirrel-cage induction generators are widely used with the fixed-speed wind turbines. In some applications, wound rotor induction generators have also been used with adequate control scheme for regulating speed by external rotor resistance. This allows the shape of the torque-slip curve to be controlled to improve the dynamics of the drivetrain. In case of PMSG, the converter/inverter can be used to control the variable voltage, variable frequency signal of the wind generator at varying wind speed. The converter converts this varying signal to the DC signal, and the output of converter is converted to AC signal of desired amplitude and frequency.

The induction generators are not locked to the frequency of the network. The cyclic torque fluctuations at the wind turbine can be absorbed by very small change in the slip speed. In case of the capacitor-excited induction generators, they obtain the magnetizing current from capacitors connected across its output terminals [55,57,58].

To take advantage of VSWTs, it is necessary to decouple the rotor speed and the grid frequency. There are different approaches to operate the VSWT within a certain operational range (cut-in and cut-out wind speed). One of the approaches is dynamic slip control, where the slip is allowed to vary up to 10% [59]. In these cases, doubly-fed induction generators (DFIG) are used (Fig. 25.54). One limitation is that DFIG require reactive power to operate. As it is not desired that the grid supply this reactive power, these generators are usually equipped with capacitors. A gearbox forms an essential component of the wind turbine generator (WTG) using induction generators. This results in the following limitations:

- Frequent maintenance
- Additional cost
- Additional losses

With the emergence of large wind power generation, increased attention is being directed toward wound rotor induction generators (WRIG) controlled from the rotor side for variable-speed constant-frequency (VSCF) applications. A wound rotor induction generator has a rotor containing a three-phase winding. These windings are made accessible to the outside via slip rings. The main advantages of a wound rotor induction generator for VSCF applications are as follows:

- Easier generator torque control using rotor current control.
- Smaller generator capacity as the generated power can be accessed from the stator and from the rotor. Usually, the rotor power is proportional to the slip speed (shaft speed-synchronous speed). Consequently, smaller rotor power converters are required. The frequency converter in the rotor (inverter) directly controls the current in the rotor winding, which enables the control of the whole generator output. The power electronic converters generally used are rated at 20%–30% of the nominal generator power.
- Fewer harmonics exist because control is in the rotor while the stator is directly connected to the grid.

If the rotor is short-circuited (making it the equivalent of a cage rotor induction machine), the speed is primarily determined by the supply frequency, and the nominal slip is within 5%. The mechanical power input ($P_{TURBINE}$) is converted into stator electric power output (P_{STATOR}) and is fed to the AC supply. The rotor power loss, being proportional to the slip speed, is commonly referred to as the slip power (P_{ROTOR}).

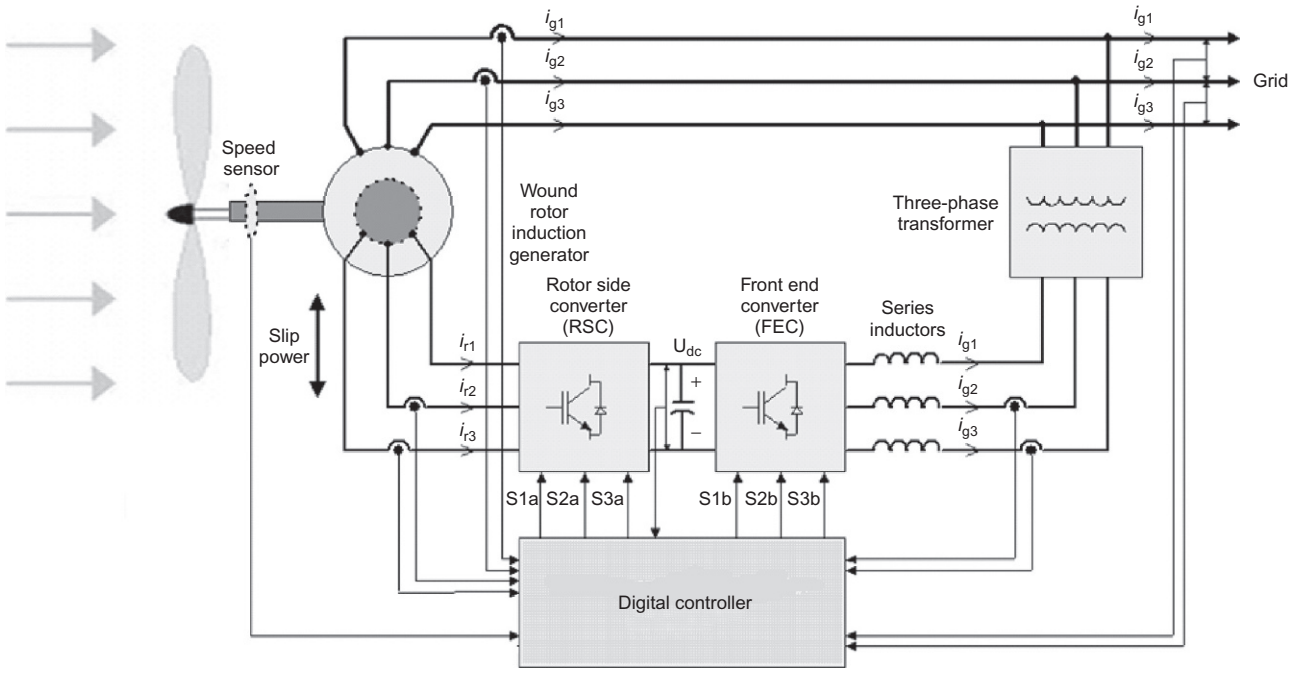


FIG. 25.54 Variable-speed doubly-fed induction generator (VSDFIG) system.

The possibility of accessing the rotor in a doubly fed induction generator makes a number of configurations possible. These include slip power recovery using a cycloconverter, which converts the ac voltage of one frequency to another without an intermediate DC link [60–62], or back-to-back inverter configurations [63,64].

Using voltage-source inverters (VSIs) in the rotor circuit, the rotor currents can be controlled at the desired phase, frequency, and magnitude. This enables reversible flow of active power in the rotor, and the system can operate in subsynchronous and supersynchronous speeds, both in motoring and generating modes. The DC link capacitor acts as a source of reactive power, and it is possible to supply the magnetizing current, partially or fully, from the rotor side. Therefore, the stator-side power factor can also be controlled. Using vector control techniques, the active and reactive powers can be controlled independently, and hence, fast dynamic performance can also be achieved.

The converter used at the grid interface is termed as the line-side converter or the front-end converter (FEC). Unlike the rotor-side converter, this operates at the grid frequency. Flow of active and reactive powers is controlled by adjusting the phase and amplitude of the inverter terminal voltage with respect to the grid voltage. Active power can flow either to the grid or to the rotor circuit depending on the mode of operation. By controlling the flow of active power, the DC bus voltage is regulated within a small band. Control of reactive power enables unity power factor operation at the grid interface. In fact, the FEC can be operated at a leading power factor, if it is so desired. It should be noted that, since the slip range is limited, the DC bus voltage is less in this case when compared with the stator side control. A transformer is therefore necessary to match the voltage levels between the grid and the DC side of the FEC. With a PWM converter in the rotor circuit, the rotor currents can be controlled at the desired phase, frequency, and magnitude. This enables reversible flow of active power in the rotor, and the system can operate in subsynchronous and supersynchronous speeds, both in motoring and generating modes (Fig. 25.55).

25.3.2 Types of Wind Power Systems

Wind power systems can be classified as follows:

- Stand-alone
- Hybrid
- Grid-connected

25.3.3 Stand-alone Wind Power Systems

Stand-alone wind power systems are being used for the following purposes in remote-area power systems:

- Battery charging
- Household power supply

25.3.3.1 Battery Charging with Stand-alone Wind Energy System

The basic elements of a stand-alone wind energy conversion system are as follows:

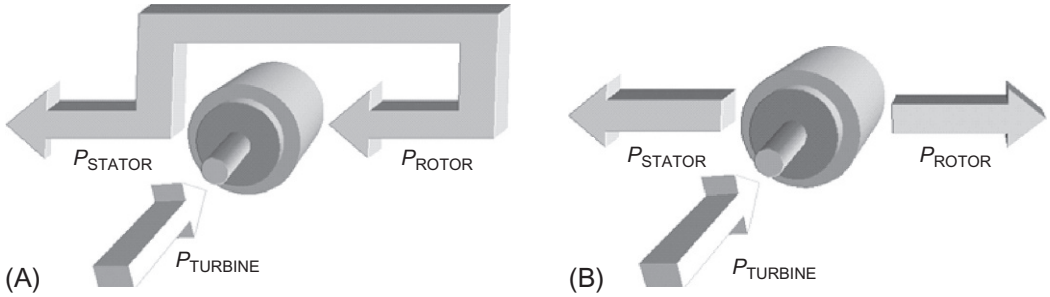


FIG. 25.55 Doubly fed induction generator power flow in generating mode: (A) subsynchronous and (B) supersynchronous.

- Wind generator
- Tower
- Charge control system
- Battery storage
- Distribution network

In remote-area power supply, an inverter and a diesel generator are more reliable and sophisticated systems. Most small isolated wind energy systems use batteries as a storage device to level out the mismatch between the availability of the wind and the load requirement. Batteries are a major cost component in an isolated power system.

25.3.3.2 Wind Turbine Charge Controller

The basic block diagram of a stand-alone wind generator and battery charging system is shown in Fig. 25.56.

The function of charge controller is to feed the power from the wind generator to the battery bank in a controlled manner. In the commonly used permanent magnet generators, this is usually done by using the controlled rectifiers [65]. The controller should be designed to limit the maximum current into the battery, reduce charging current for high battery SOC, and maintain a trickle charge during full SOC periods.

25.3.4 Wind-Diesel Hybrid Systems

The details of hybrid systems are already covered in Section 25.2.4. Diesel systems without batteries in remote areas are characterized by poor efficiency, high maintenance, and fuel costs. The diesel generators must be operated above a certain minimum load level to reduce cylinder wear and tear due to incomplete combustion. It is a common practice to install dump loads to dissipate extra energy. More efficient systems can be devised by combining the diesel generator with a battery-inverter subsystem and incorporating RES, such as wind/solar where appropriate. An integrated hybrid energy system incorporating a diesel generator, wind generator, battery or flywheel storage, and inverter will be cost-effective at many sites with an average daily energy demand exceeding 25 kWh [66]. These hybrid energy systems can serve as a minigrid as a part of distributed generation rather than extending the grid to the remote rural areas. The heart of the hybrid system is a high-quality sine-wave inverter, which can also be operated in reverse as battery charger. The system can cope with loads ranging from zero (inverter only operation) to approximately three times greater capacity (inverter and diesel operating in parallel).

Decentralized form of generation can be beneficial in remote-area power supply. Due to high cost of PV systems, problems associated with storing electricity over longer periods (like maintenance difficulties and costs), wind turbines can be a viable alternative in hybrid systems. Systems with battery storage provide better reliability. Wind power penetration can be high enough to make a significant impact on the operation of diesel generators.

High wind penetration also poses significant technical problems for the system designer in terms of control and transient stability [29]. In earlier stages, wind-diesel systems were installed without assessing the system behavior due to the lack

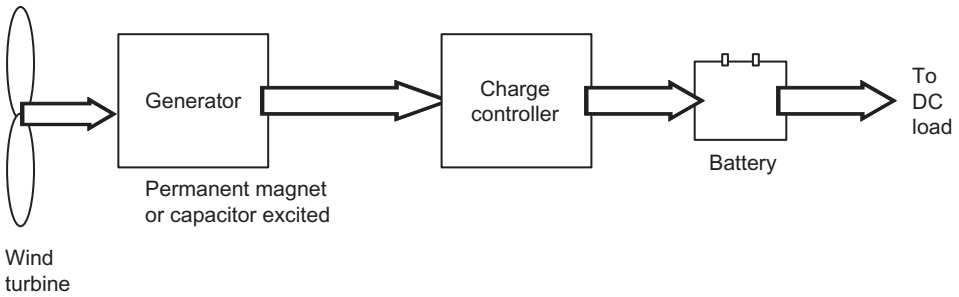


FIG. 25.56 Block diagram for a stand-alone wind generator and battery charging system.

of design tools/software. With the continual research in this area, there is now software available to assist in this process. Wind-diesel technology has now matured due to research and development in this area. Now, there is a need to utilize this knowledge into cost-effective and reliable hybrid systems [67]. In Western Australia, dynamic modeling of wind-diesel hybrid system has been developed in Curtin/MUERI, supported by the Australian Cooperative Research Centre for Renewable Energy (ACRE) program 5.21.

25.3.5 Grid-Connected Wind Energy Systems

Small-scale wind turbines, connected to the grid (weak or strong grid), have been discussed here. Wind-diesel systems have been getting attention in many remote parts of the world lately. Remote-area power supplies are characterized by low inertia, low damping, and poor reactive power support. Such weak power systems are more susceptible to sudden change in network operating conditions [68]. In this weak grid situation, the significant power fluctuations in the grid would lead to reduced quality of supply to users. This may manifest itself as voltage and frequency variations or spikes in the power supply. These weak grid systems need appropriate storage and control systems to smooth out these fluctuations without sacrificing the peak power tracking capability. These systems can have two storage elements. The first is the inertia of the rotating mechanical parts, which includes the blades, gearbox, and the rotor of the generators. Instead of wind speed fluctuation causing large and immediate change in the electric output of the generator as in a fixed-speed machine, the fluctuation will cause a change in shaft speed and not create a significant change in generator output. The second energy storage element is the small battery storage between the DC-DC converter and the inverter. The energy in a gust could be stored temporarily in the battery bank and released during a lull in the wind speed, thus reducing the size of fluctuations.

In larger-scale wind turbines, the addition of inverter control further reduces fluctuation and increases the total output power. Thus, the total output of the wind energy system can be stabilized or smoothed to track the average wind speed and can omit certain gusts. The system controller should track the peak power to maximize the output of the wind energy system. It should monitor the stator output and adjust the inverter to smooth the total output. The amount of smoothing would depend on SOC of the battery. The nominal total output would be adjusted to keep the battery bank SOC at a reasonable level. In this way, the total wind energy system will track the long-term variations in the wind speed without having fluctuations caused by the wind. The storage capacity of the battery bank needs only be several minutes to smooth out the gusts in the wind, which can be easily handled by the weak grid. In the cases, where the weak grid is powered by diesel generators, the conventional wind turbine can cause the diesel engines to operate at low capacity. In case of strong wind application,

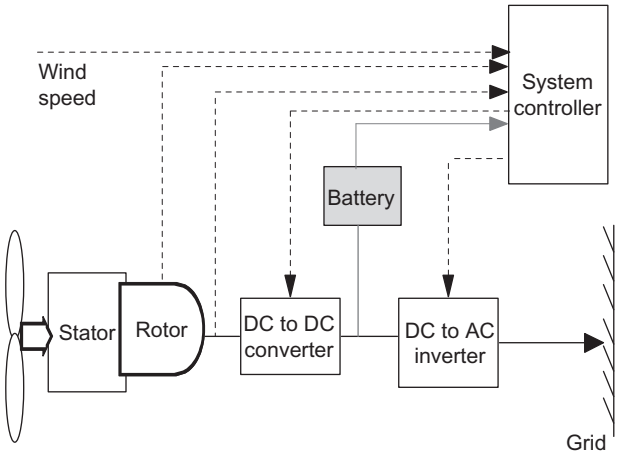


FIG. 25.57 System block diagram of grid-connected wind energy system.

the fluctuations in the output of the wind energy generator system can be readily absorbed by the grid. The main aim here is to extract the maximum energy from the wind. The basic block layout of such a system [69] is shown in Fig. 25.57.

The function of the DC-DC converter will be to adjust the torque on the machine and hence ensure by measurement of wind speed and shaft speed that the turbine blades are operating so as to extract optimum power. The purpose of the inverter is to feed the energy gathered by the rotor and DC-DC converter, in the process of peak power tracking, to the grid system. The interaction between the two sections would be tightly controlled so as to minimize or eliminate the need for a battery bank. The control must be fast enough so that the inverter output power set point matches the output of the DC-DC converter. For a wound rotor induction machine operating over a two-to-one speed range, the maximum power extracted from the rotor is equal to the power rating of the stator. Thus, the rating of the generator from a traditional point of view is only half that of the wind turbine [69]. Since half the power comes from the stator and half from the rotor, the power electronics of the DC-DC converter and inverter need to handle only half the total wind turbine output, and no battery would be required.

Power electronics technology also plays an important role in both system configurations and in control of offshore wind farms [70]. Wind farms connect in various configurations and control methods using different generator types and compensation arrangements. For instance, wind farms can be connected to the AC local network with centralized compensation or with a HVDC transmission system and DC local network. Decentralized control with a DC transmission system has also been used [71].

25.3.5.1 Soft Starters for Induction Generators

When an induction generator is connected to a load, a large inrush current flows. This is something similar to the direct online starting problem of induction machines. It has been

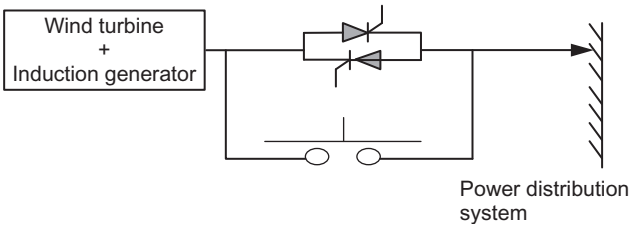


FIG. 25.58 Soft starting for wind turbine coupled with induction generator.

observed that the initial time constants of the induction machines are higher when it tries to stabilize initially at the normal operating conditions. There is a need to use some type of soft-starting equipment to start the large induction generators. A simple scheme to achieve this is shown in Fig. 25.58.

Two thyristors are connected in each phase, back to back. Initially, when the induction generator is connected, the thyristors are used to control the voltage applied to the stator and to limit the large inrush current. As soon as the generator is fully connected, the bypass switch is used to bypass the soft-starter unit.

25.3.6 Control of Wind Turbines

Theory indicates that operation of a wind turbine at fixed tip-speed ratio (C_{pmax}) ensures enhanced energy capture [54]. The wind energy systems must be designed so that above the rated wind speed, the control system limits the turbine output. In normal operation, medium- to large-scale wind turbines are connected to a large grid. Various wind turbine control policies have been studied around the world. Grid-connected wind turbines generators can be classified as follows:

- Fixed-speed wind turbines
- Variable-speed wind turbines

25.3.6.1 Fixed Speed Wind Turbines

In case of a fixed-speed wind turbine, synchronous or squirrel-cage induction generators are employed and are characterized by the stiff power train dynamics. The rotational speed of the wind turbine generator in this case is fixed by the grid frequency. The generator is locked to the grid, thereby permitting only small deviations of the rotor shaft speed from the nominal value. The speed is very responsive to wind speed fluctuations. The normal method to smooth the surges caused by the wind is to change the turbine aerodynamic characteristics, either passively by stall regulation or actively by blade pitch regulation. The wind turbines often subjected to very low (below cut-in speed) or high wind speed (above rated value). Sometimes, they generate below rated power. No pitch regulation is applied when the wind turbine is operating below rated speed, but pitch control is required when the machine is operating above rated wind speed to minimize the stress. Fig. 25.59 shows the effect of blade pitch angle on the torque-speed curve at a given wind speed.

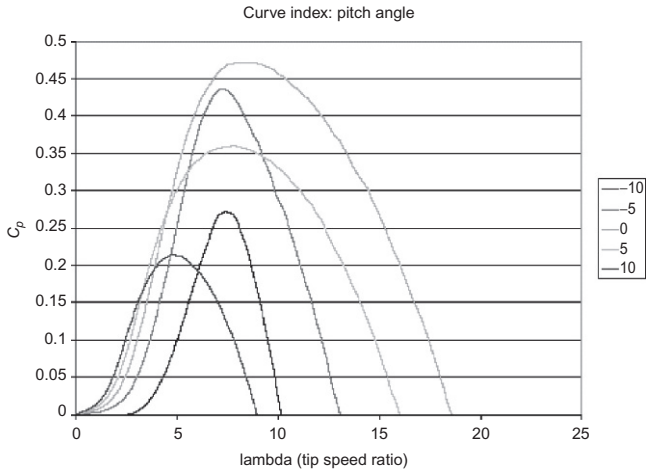


FIG. 25.59 C_p/λ curves for different pitch settings.

Blade pitch control is a very effective way of controlling wind turbine speed at high wind speeds, hence limiting the power and torque output of the wind machine. An alternative but cruder control technique is based on airfoil stall [54]. A synchronous link maintaining fixed turbine speed in combination with an appropriate airfoil can be designed so that, at higher than rated wind speeds, the torque reduces due to airfoil stall. This method does not require external intervention or complicated hardware, but it captures less energy and has greater blade fatigue.

The aims of variable-pitch control of medium- and large-scale wind turbines were to help in start-up and shutdown operation, to protect against overspeed and to limit the load on the wind turbine [72]. The turbine is normally operated between a lower and an upper limit of wind speed (typically 4.5–26 m/s). When the wind speed is too low or too high, the wind turbine is stopped to reduce wear and damage. The wind turbine must be capable of being started and run up to speed in a safe and controlled manner. The aerodynamic characteristics of some turbines are such that they are not self-starting. The required starting torque may be provided by motoring or changing the pitch angle of the blade. In case of grid-connected wind turbine system, the rotational speed of the generator is locked to the frequency of the grid. When the generator is directly run by the rotor, the grid acts like an infinite load. When the grid fails, the load rapidly decreases to zero resulting in the turbine rotor to accelerate quickly. Overspeed protection must be provided by rapid braking of the turbine. A simple mechanism of one of blade pitch control techniques is shown in Fig. 25.60.

In this system, the permanent magnet synchronous generator (PMSG) has been used without any gearbox. Direct connection of generator to the wind turbine requires the generator to have a large number of poles. Both induction generators and wound-filed synchronous generators of high pole number require a large diameter for efficient operation. Permanent

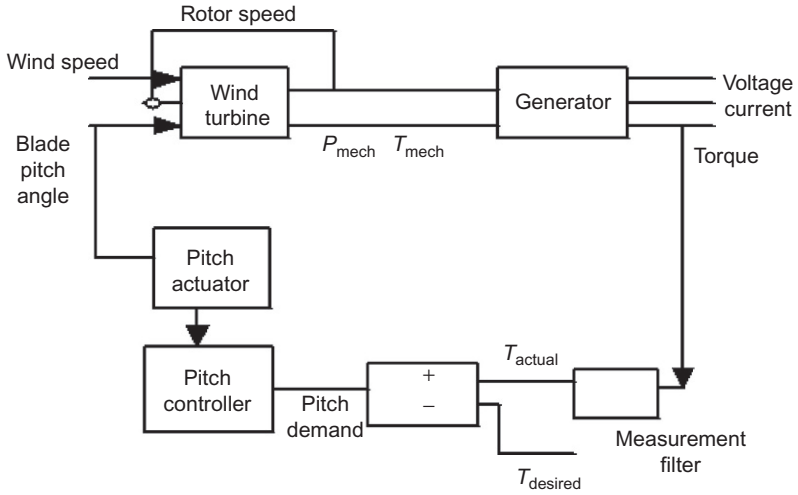


FIG. 25.60 Pitch control block diagram of a PMSG.

magnet synchronous generators allow a small pole pitch to be used [73]. The power output, P_{mech}, of any turbine depends mainly upon the wind speed, which dictates the rotational speed of the wind turbine rotor. Depending upon the wind speed and rotational speed of turbine, tip-speed ratio λ is determined. Based on computed λ, the power coefficient C_p is inferred. In the control strategy above, the torque output, T_{actual}, of the generator is monitored for a given wind speed and compared with the desired torque, T_{actual}, depending upon the load requirement. The generator output torque is passed through the measurement filter. The pitch controller then infers the modified pitch angle based on the torque error. This modified pitch angle demand and computed λ decides the new C_p, resulting in the modified wind generator power and torque output. The controller will keep adjusting the blade pitch angle till the desired power and torque output are achieved.

Some of the wind turbine generator includes the gearbox for interfacing the turbine rotor and the generator. The general drivetrain model [72] for such a system is shown in Fig. 25.61. This system also contains the blade pitch angle control provision.

The drivetrain converts the input aerodynamic torque on the rotor into the torque on the low-speed shaft. This torque on the low-speed shaft is converted to high-speed shaft torque using the gearbox and fluid coupling. The speed of the wind turbine here is low, and the gearbox is required to increase the speed so as to drive the generator at rated rpm, for example, 1500 rpm. The fluid coupling works as a velocity-in-torque-out device and transfers the torque [72]. The actuator regulates the tip angle based on the control system applied. The control system here is based on a pitch regulation scheme where the blade pitch angle is adjusted to obtain the desired output power.

25.3.6.2 Variable Speed Wind Turbines

The variable-speed constant-frequency turbine drivetrains are not directly coupled to the grid. The power-conditioning device is used to interface the wind generator to the grid. The output of the wind generator can be variable voltage and variable frequency, which is not suitable for grid integration, and appropriate interfacing is required. The wind turbine rotor in this case is permitted to rotate at any wind speed by power-generating unit.

A number of schemes have been proposed in the past that allow wind turbines to operate with variable rotor speed while feeding the power to a constant-frequency grid. Some of the benefits that have been claimed for variable-speed constant-frequency wind turbine configuration are as follow [69]:

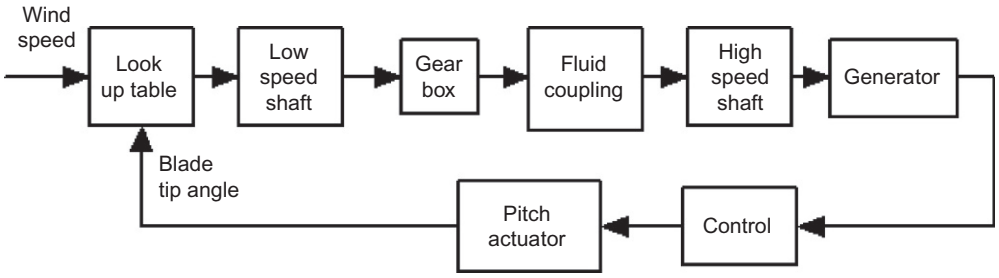


FIG. 25.61 Block diagram of drivetrain model.

- The variable-speed operation results in increased energy capture by maintaining the blade tip speed to wind-speed ratio near the optimum value.
- By allowing the wind turbine generator to run at variable speed, the torque can be fixed, but the shaft power allowed to increase. This means that the rated power of the machine can be increased with no structural changes.
- A variable-speed turbine is capable of absorbing energy in wind gusts as it speeds up and gives back this energy to the system as it slows down. This reduces turbulence-induced stresses and allows capture of a large percentage of the turbulent energy in the wind.
- More efficient operation can be achieved by avoiding aerodynamic stall over most of operating range.
- Better grid quality is due to the support of grid voltage.

Progress in the power electronic conversion system has given a major boost to implementing the concept of variable-speed operation. The research studies have shown that the most significant potential advancement for wind turbine technology was in the area of power electronic controlled variable-speed operation. There is much research underway in the United States and Europe on developing variable-speed wind turbine as cost-effective as possible. In the United States, the NASA MOD-0 and MOD-5B were operated as variable-speed wind turbines [69]. Companies in the United States and Enercon (Germany) made machines incorporate a variable-speed feature. Enercon variable-speed wind machine is already in operation in Denham, Western Australia.

The ability to operate at varying rotor speed effectively adds compliance to the power train dynamics of the wind turbine. Although many approaches have been suggested for variable-speed wind turbines, they can be grouped into two main classes: (a) discretely variable speed and (b) continuously variable speed [69,74].

25.3.6.3 Discretely Variable Speed Systems

The discretely variable-speed category includes electric system where multiple generators are used, either with different number of poles or with different ratio gearing connected to the wind rotor. It also includes those generators, which can use different number of poles in the stator or can approximate the effect by appropriate switching. Some of the generators in this category are those with consequent poles, dual winding, or pole amplitude modulation. A brief summary of some of these concepts is presented below.

Pole changing type induction generators

These generators provide two speeds, a factor of two apart, such as four pole/eight pole (1500/750 rpm at a supply frequency of 50 Hz or 1800/900 rpm at 60 Hz). They do this by using one-half the poles at the higher speed. These machines are commercially available and cost about 50% more than the corresponding single-speed machines. Their main disadvantage, in comparison with other discretely variable machines, is that the two-to-one speed range is wider than the optimum range for a wind turbine [75].

Dual stator winding two speed induction generators

These machines have two separate stator windings, only one of which is active at a time. As such, a variety of speed ranges can be obtained depending on the number of poles in each winding. As in the consequent pole machines, only two speeds may be obtained. These machines are significantly heavier than single-machines, and their efficiency is less, since one winding is always unused, which leads to increased losses. These machines are commercially available. Their cost is approximately twice that of single-speed machines [75].

Multiple generators

This configuration is based on the use of a multiple generator design. In one case, there may simply be two separate generators (as used on some European wind turbines). Another possibility is to have two generators on the same shaft, only one of which is electrically connected at a time. The gearing is arranged such that the generators reach synchronous speed at different turbine rotor speeds.

Two speed pole amplitude modulated induction generator (PAM)

This configuration consists of an induction machine with a single stator, which may have two different operating speeds. It differs from conventional generators only in the winding design. Speed is controlled by switching the connections of the six stator leads. The winding is built in two sections that will be in parallel for one speed and in series for the other. The result is the superposition of one alternating frequency on another. This causes the field to have an effectively different number of poles in the two cases, resulting in two different operating speeds. The efficiency of the PAM is comparable with that of a single-speed machine. The cost is approximately twice that of conventional induction generators.

The use of a discretely variable-speed generator will result in some of the benefits of continuously variable-speed operation, but not all of them. The main effect will be in increased energy productivity, because the wind turbine will be able to operate close to its optimum tip-speed ratio over a great range of wind speeds than will a constant speed machine. On the other hand, it will perform as single-speed machine with respect to rapid changes in wind speed (turbulence). Thus, it could not be expected to extract the fluctuating energy as effective from the wind as would be continuously variable-speed machine. More importantly, it could not use the inertia of the rotor to absorb torque spikes. Thus, this approach would not result in improved fatigue life of the machine, and it could not be an integral part of an optimized design such as one using yaw/speed control or pitch/speed control.

25.3.6.4 Continuously Variable Speed Systems

The second main class of systems for variable-speed operation is those that allow the speed to be varied continuously. For the continuously variable-speed wind turbine, there may be more than one control, depending upon the desired control action [76–80]:

- Mechanical control
- Combination of electric/mechanical control
- Electric control
- Electric/power electronics control

The mechanical methods include hydraulic and variable ratio transmissions. An example of an electric/mechanical system is one in which the stator of the generator is allowed to rotate. All the electric category includes high-slip induction generators and the tandem generator. The power electronic category contains a number of possible options. One option is to use a synchronous generator or a wound rotor induction generator, although a conventional induction generator may also be used. The power electronics is used to condition some or all the power to form an appropriate to the grid. The power electronics may also be used to rectify some or all the power from the generator, to control the rotational speed of the generator or to supply reactive power. These systems are discussed below.

Mechanical systems

Variable speed hydraulic transmission: One method of generating electric power at a fixed frequency while allowing the rotor to turn at variable speed is the use of a variable-speed hydraulic transmission. In this configuration, a hydraulic system is used in the transfer of the power from the top of the tower to ground level (assuming a horizontal-axis wind turbine). A fixed displacement hydraulic pump is connected directly to the turbine (or possibly gearbox) shaft. The hydraulic fluid is fed to and from the nacelle via a rotary fluid coupling. At the base of the tower is a variable displacement hydraulic motor, which is governed to run at constant speed and drive a standard generator.

One advantage of this concept is that the electric equipment can be placed at ground level making the rest of the machine simpler. For smaller machines, it may be possible to dispense with a gearbox altogether. On the other hand, there are a number of problems using hydraulic transmissions in wind turbines. For one thing, pumps and motors of the size needed in wind turbines of greater than about 200 kW are not readily available. Multiples of smaller units are possible, but this would complicate the design. The life expectancy of many of the parts, especially seals, may well be less than 5 years. Leakage of hydraulic fluid can be a significant problem, necessitating frequent maintenance. Losses in the hydraulics could also make the overall system less efficient than conventional electric generation. Experience over the last many years has not shown great success with the wind machines using hydraulic transmission.

Variable ratio transmission: A variable ratio transmission (VRT) is one in which the gear ratio may be varied continuously within a given range. One type of VRT suggested for wind turbines is using belts and pulleys, such as are used in some industrial drives [69,81]. These have the advantage of being able to drive a conventional fixed-speed generator while being driven by a variable-speed turbine rotor. On the other hand, they do not appear to be commercially available in larger sizes, and those, which do exist, have relatively high losses.

Electrical/mechanical variable speed systems – rotating stator induction generator

This system uses a conventional squirrel-induction generator whose shaft is driven by a wind turbine through a gearbox [54,81]. However, the stator is mounted to a support that allows bidirectional rotation. This support is in turn driven by a DC machine. The armature of the DC machine is fed from a bidirectional inverter, which is connected to the fixed frequency AC grid. If the stator support allowed to turn in the same direction as the wind turbine, the turbine will turn faster. Some of the power from the wind turbine will be absorbed by the induction generator stator and fed to the grid through the inverter. Conversely, the wind turbine will turn more slowly when the stator support is driven in the opposite direction. The amount of current (and thus the torque) delivered to or from the DC machine is determined by a closed loop control circuit whose feedback signal is driven by a tachometer mounted on the shaft of the DC machine.

One of the problems with this system is that the stator slip rings and brushes must be sized to take the full power of the generator. They would be subjected to wear and would require maintenance. The DC machine also adds to cost, complexity, and maintenance.

Electrical variable speed systems

High slip induction generator: This is the simplest variable-speed system, which is accomplished by having a relatively large amount of resistance in the rotor of an induction generator. However, the losses increase with increased rotor resistance. Westwind Turbines in Australia investigated such a scheme on a 30 kW machine in 1989.

Tandem induction generator: A tandem induction generator consists of an induction machine fitted with two magnetically independent stators, one fixed in position and the other able to be rotated, and a single squirrel-cage rotor whose bars extend to the length of both stators [69,81]. Torque control is achieved by physical adjustment of the angular displacement between the two stators, which causes a phase shift between the induced rotor voltages.

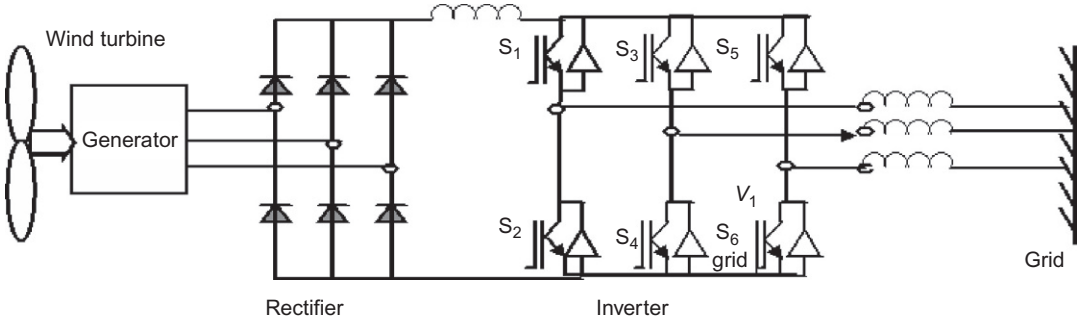


FIG. 25.62 Grid-connected wind energy system through AC/DC/AC converter.

Electrical/power electronics

The general configuration is shown in Fig. 25.62. It consists of the following components:

- Wind generator
- Rectifier
- Inverter

The generator may be DC, synchronous (wound rotor or permanent magnet type), squirrel-cage wound rotor, or brushless doubly fed induction generator. The rectifier is used to convert the variable voltage variable frequency input to a DC voltage. This DC voltage is converted into AC of constant voltage and frequency of desired amplitude. The inverter will also be used to control the active/reactive power flow from the inverter. In case of DC generator, the converter may not be required or when a cycloconverter is used to convert the AC directly from one frequency to another.

25.3.6.5 Types of Generator Options for Variable Speed Wind Turbines Using Power Electronics

Power electronics may be applied to four types of generators to facilitate variable-speed operation:

- Synchronous generators
- Permanent magnet synchronous generators
- Squirrel-cage induction generators
- Wound rotor induction generators

Synchronous generator

In this configuration, the synchronous generator is allowed to run at variable speed, producing power of variable voltage and frequency. Control may be facilitated by adjusting an externally supplied field current. The most common type of power conversion uses a bridge rectifier (controlled/uncontrolled), a DC link, and inverter as shown in Fig. 25.62. The disadvantage of this configuration includes the relatively high cost and maintenance requirements of synchronous generators and the need for the power conversion system to take the full power generated (as opposed to the wound rotor system).

Permanent magnet synchronous generators

The permanent magnet synchronous generator (PMSG) has several significant advantageous properties. The construction is simple and does not required external magnetization, which is important especially in stand-alone wind power applications and also in remote areas where the grid cannot easily supply the reactive power required to magnetize the induction generator. Similar to the previous externally supplied field current synchronous generator, the most common type of power conversion uses a bridge rectifier (controlled/uncontrolled), a DC link, and inverter as shown in Fig. 25.63 [82–84].

Fig. 25.64 shows a wind energy system where a PMSG is connected to a three-phase rectifier followed by a boost converter. In this case, the boost converter controls the electromagnetic torque, and the supply side converter regulates the DC link voltage and controls the input power factor. One drawback of this configuration is the use of diode rectifier that increases the current amplitude and distortion of the PMSG. As a result, this configuration has been considered for small size wind energy conversion systems (smaller than 50 kW).

The advantage of the system in Fig. 25.63 with regardant to the system showed in Fig. 25.64 is it allows the generator to operate near its optimal working point in order to minimize the losses in the generator and power electronic circuit.

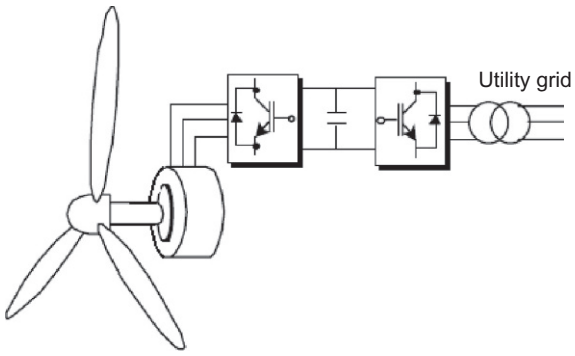


FIG. 25.63 Grid-connected PMSG wind energy system through DC/AC converter.

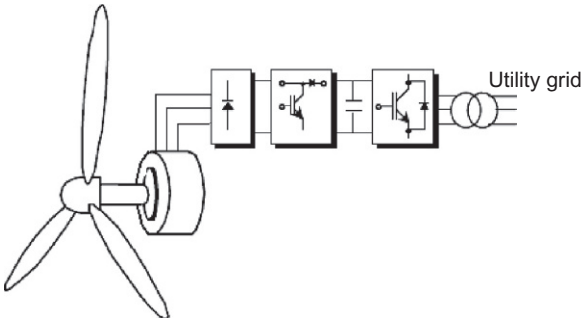


FIG. 25.64 Grid-connected PMSG wind energy system through DC/AC converter with a boost chopper.

However, the performance is dependent on the good knowledge of the generator parameter that varies with temperature and frequency. The main drawbacks, in the use of PMSG, are the cost of permanent magnet that increase the price of machine, demagnetization of the permanent magnet material, and it is not possible to control the power factor of the machine.

To extract maximum power at unity power factor from a PMSG and feed this power (also at unity power factor) to the grid, the use of back-to-back connected PWM voltage-source converters are proposed [85]. Moreover, to reduce the overall cost, reduced switch PWM voltage-source converters (four switches) instead of conventional (six-switch) converters for variable-speed drive systems can be used. It is shown that by using both rectifier and inverter current control or flux-based control, it is possible to obtain unity power factor operation both at the WTG and the grid. Other mechanisms can also be included to maximize power extraction from the VSWT (i.e., MPPT techniques) or sensorless approaches to further reduce cost and increase reliability and performance of the systems.

Squirrel-cage induction generator

Possible architecture for systems using conventional induction generators that have a solid squirrel-cage rotor has many similarities to those with synchronous generators. The main difference is that the induction generator is not inherently self-exciting, and it needs a source of reactive power. This could be done by a generator side self-commutated converter operating in the rectifier mode. A significant advantage of this configuration is the low-cost and low-maintenance requirements of induction generators. Another advantage of using the self-commutated double converter is that it can be on the ground, completely separate from the wind machine. If there is a problem in the converter, it could be switched out of the circuit for repair, and the wind machine could continue to run at constant speed. The main disadvantage with this configuration is that, as with the synchronous generator, the power conversion system would have to take the full power generated and could be relatively costly compared with some other configurations. There would also be additional complexities associated with the supply of reactive power to the generator.

Wound rotor induction generator

A wound rotor induction rotor has three-phase winding on the rotor, accessible to the outside via slip rings. The possibility of accessing the rotor can have the following configurations:

- Slip power recovery
- Use of cycloconverter
- Rotor resistance chopper control

Slip power recovery (static Kramer system): The slip power recovery configuration behaves similarly to a conventional induction generator with very large slip, but in addition, energy is recovered from the rotor. The rotor power is first carried out through slip rings and then rectified and passed through a DC link to a line-commutated inverter and into the grid. The rest of the power comes directly from the stator as it normally does. A disadvantage with this system is that it can only allow super-synchronous variable-speed operation. Its possible use in the wind power was reported by Smith and Nigim [86].

In this scheme shown in Fig. 25.65, the stator is directly connected to the grid. Power converter has been connected to the rotor of wound rotor induction generator to obtain the

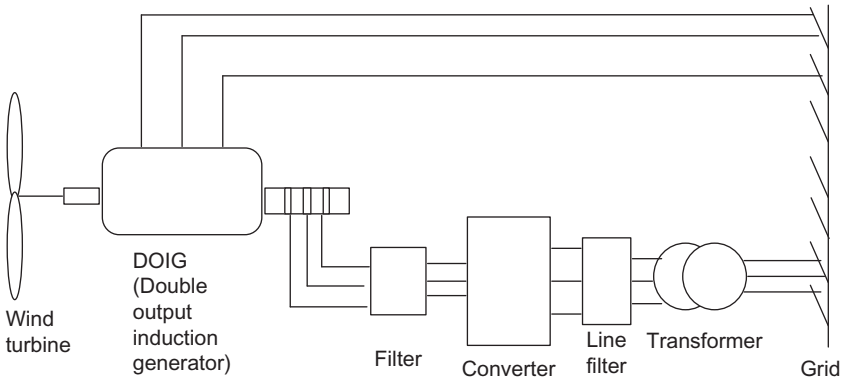


FIG. 25.65 Schematic diagram of doubly fed induction generator.

optimum power from variable-speed wind turbine. The main advantage of this scheme is that the power-conditioning unit has to handle only a fraction of the total power so as to obtain full control of the generator. This is very important when the wind turbine sizes are increasing for the grid-connected applications for higher penetration of wind energy and the smaller size of converter can be used in this scheme.

Cycloconverter (static Scherbius system): A cycloconverter is a converter that converts AC voltage of one frequency to another frequency without an intermediate DC link. When a cycloconverter is connected to the rotor circuit, sub- and supersynchronous operation variable-speed operation is possible. In supersynchronous operation, this configuration is similar to the slip power recovery. In addition, energy may be fed into the rotor, thus allowing the machine to generate at subsynchronous speeds. For that reason, the generator is said to be doubly fed [87]. This system has a limited ability to control reactive power at the terminals of the generator, although as a whole it is a net consumer of reactive power. On the other hand, if coupled with capacitor excitation, this capability could be useful from the utility point of view. Because of its ability to rapidly adjust phase angle and magnitude of the terminal voltage, the generator can be resynchronized after a major electric disturbance without going through a complete stop/start sequence. With some wind turbines, this could be a useful feature.

Rotor resistance chopper control: A fairly simple scheme of extracting rotor power as in the form of heat has been proposed in [48].

25.3.6.6 Isolated Grid Supply System with Multiple Wind Turbines

The isolated grid supply system with a wind park is shown in Fig. 25.66. Two or more wind turbines can be connected to this system. A diesel generator can be connected in parallel. The converters, connected with wind generators, will work in parallel, and the supervisory control block will control the output of these wind generators in conjunction with the diesel generator. This type of decentralized generation can be a better option where high penetration of wind generation is sought. The individual converter will control the voltage and frequency of the system. The supervisory control system will play an important part in coordination between multiple power generation systems in a remote-area power supply having weak grid.

25.3.6.7 Power Electronics Technology Development

To meet the needs of future power generation systems, power electronics technology will need to evolve on all levels, from devices to systems. The development needs are as follows:

- There is a need for modular power converters with plug-and-play controls. This is particularly important for high-power utility systems, such as wind power. The power electronic equipment used today is based on industrial motor drive technology. Having dedicated, high power density, modular systems will provide flexibility and efficiency in dealing with different energy sources and large variation of generation systems architectures.
- There is a need for new packaging and cooling technologies, and integration with PV and fuel cell will have to be addressed. The thermal issues in integrated systems are

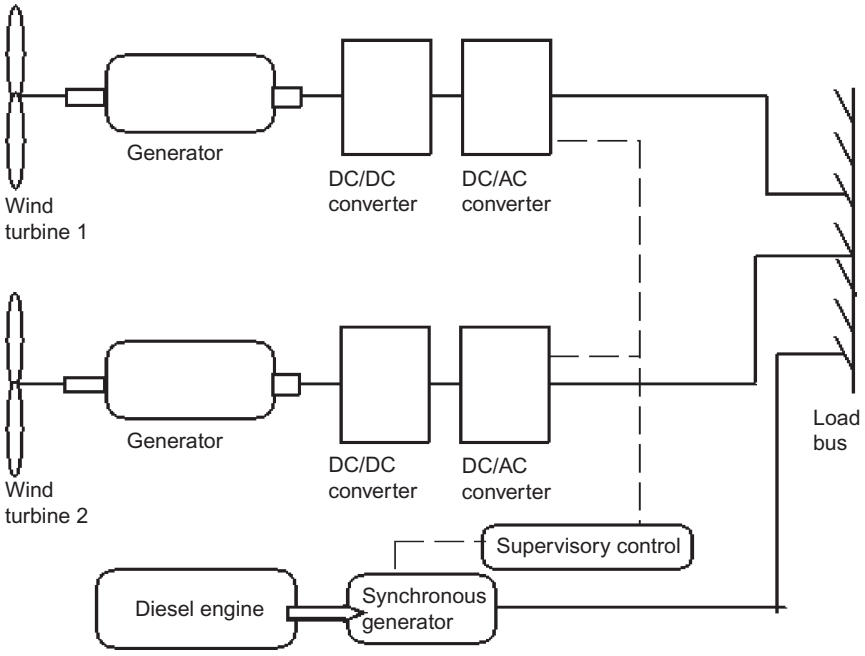


FIG. 25.66 Schematic diagram of isolated grid system having a wind park.

complex, and new technologies such as direct fluid cooling or microchannel cooling may find application in future systems. There is large potential for advancement in this area.
- There is a need for new switching devices with higher temperature capability, higher switching speed, and higher current density/voltage capability. The growth in alternative energy markets will provide a stronger pull for further development of these technologies.

25.4 Power Electronics for Hybrid Energy Systems

The combination of RES, such as PV arrays or wind turbines, with engine-driven generators and battery storage, is widely recognized as a viable alternative to conventional remote-area power supplies (RAPS). These systems are generally classified as hybrid energy systems (HES). They are used increasingly for electrification in remote areas where the cost of grid extension is prohibitive and the price for fuel increases drastically with the remoteness of the location. For many applications, the combination of renewable and conventional energy sources compares favorably with fossil-fuel-based RAPS systems, in regard to both their cost and technical performance. Because these systems employ two or more different sources of energy, they enjoy a very high degree of reliability as compared with single-source systems such as a stand-alone diesel generator or a stand-alone PV or wind system. Applications of hybrid energy systems range from small power supplies for remote households, providing electricity for lighting and other essential electric appliances, to village electrification for remote communities have been reported [88].

Hybrid energy systems generate AC electricity by combining RES such as PV array with an inverter, which can operate alternately or in parallel with a conventional engine-driven generator. They can be classified according to their configuration as follows [89]:

- Series hybrid energy systems
- Switched hybrid energy systems
- Parallel hybrid energy systems

The parallel hybrid systems can be further divided to DC or AC coupling. An overview of the three most common system topologies is presented by Bower [90]. In the following, a comparison of typical PV-diesel system configurations is described.

25.4.1 Series Configuration

In the conventional series hybrid systems shown in Fig. 25.67, all power generators feed DC power into a battery. Each component has therefore to be equipped with an individual charge controller and in the case of a diesel generator with a rectifier.

To ensure reliable operation of series hybrid energy systems, both the diesel generator and the inverter have to be sized to meet peak loads. This results in a typical system operation where a large fraction of the generated energy is passed through the battery bank, therefore resulting in increased cycling of the battery bank and reduced system efficiency. AC power delivered to the load is converted from DC to regulated AC by an inverter or a motor generator unit. The power generated by the diesel generator is first rectified and subsequently converted back to AC before being supplied to the load, which incurs significant conversion losses.

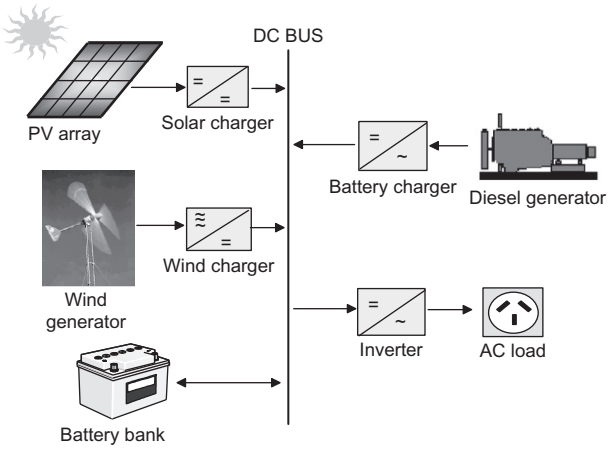


FIG. 25.67 Series hybrid energy system.

The actual load demand determines the amount of electric power delivered by the PV array, the wind generator, the battery bank, or the diesel generator. The solar and wind charger prevents overcharging of the battery bank from the PV generator when the PV power exceeds the load demand and the batteries are fully charged. It may include MPPT to improve the utilization of the available PV energy, although the energy gain is marginal for a well-sized system. The system can be operated in manual or automatic mode, with the addition of appropriate battery voltage sensing and start/stop control of the engine-driven generator.

Advantages are as follows:

- The engine-driven generator can be sized to be optimally loaded while supplying the load and charging the battery bank, until a battery SOC of 70%–80% is reached.
- No switching of AC power between the different energy sources is required, which simplifies the electric output interface.
- The power supplied to the load is not interrupted when the diesel generator is started.
- The inverter can generate a sine wave, modified square wave, or square wave depending on the application.

Disadvantages are as follows:

- The inverter cannot operate in parallel with the engine-driven generator; therefore, the inverter must be sized to supply the peak load of the system.
- The battery bank is cycled frequently, which shortens its lifetime.

- The cycling profile requires a large battery bank to limit the depth of discharge (DOD).
- The overall system efficiency is low, since the diesel cannot supply power directly to the load.
- Inverter failure results in complete loss of power to the load, unless the load can be supplied directly from the diesel generator for emergency purposes.

25.4.2 Switched Configuration

Despite its operational limitations, the switched configuration remains one of the most common installations in some developing countries. It allows operation with either the engine-driven generator or the inverter as the AC source, yet no parallel operation of the main generation sources is possible. The diesel generator and the RES can charge the battery bank. The main advantage compared with the series system is that the load can be supplied directly by the engine-driven generator, which results in a higher overall conversion efficiency. Typically, the diesel generator power will exceed the load demand, with excess energy being used to recharge the battery bank. During periods of low electricity demand, the diesel generator is switched off, and the load is supplied from the PV array together with stored energy. Switched hybrid energy systems can be operated in manual mode, although the increased complexity of the system makes it highly desirable to include an automatic controller, which can be implemented with the addition of appropriate battery voltage sensing and start/stop control of the engine-driven generator (Fig. 25.68).

Advantages are as follows:

- The inverter can generate a sine wave, modified square wave, or square wave, depending on the particular application.
- The diesel generator can supply the load directly, therefore improving the system efficiency and reducing the fuel consumption.

Disadvantages are as follows:

- Power to the load is interrupted momentarily when the AC power sources are transferred.
- The engine-driven alternator and inverter are typically designed to supply the peak load, which reduces their efficiency at part load operation.

25.4.3 Parallel Configuration

The parallel hybrid system can be further classified as DC and AC couplings as shown in Fig. 25.69. In both schemes, a bidirectional inverter is used to link between the battery and an AC source (typically the output of a diesel generator). The bidirectional inverter can charge the battery bank (rectifier operation) when excess energy is available from the diesel generator or by the renewable sources and act as a DC-AC converter (inverter operation). The bidirectional inverter may also provide "peak shaving" as part of a control strategy when the diesel engine is overloaded. In Fig. 25.69A, the renewable energy sources (RES) such as photovoltaic and wind are coupled on the DC side. DC integration of RES results in "custom" system solutions for individual supply cases requiring high costs for engineering, hardware, repair, and maintenance. Furthermore, power system expandability for covering the needs of growing energy and power demand is also difficult. A better approach would be to integrate the RES on the AC side rather than on the DC side as shown in Fig. 25.69B.

Parallel hybrid energy systems are characterized by two significant improvements over the series and switched system configuration.

The inverter and the diesel generator capacity rather than their individual component ratings limit the maximum load that can be supplied. Typically, this will lead to a doubling of the system capacity. The capability to synchronize the inverter with the diesel generator allows greater flexibility to optimize the operation of the system. Future systems should be sized with a reduced peak capacity of the diesel generator, which results in a higher fraction of directly used energy and hence higher system efficiencies.

By using the same power electronic devices for both inverter and rectifier operation, the number of system components is minimized. Additionally, wiring and system installation costs are reduced through the integration of all power-conditioning

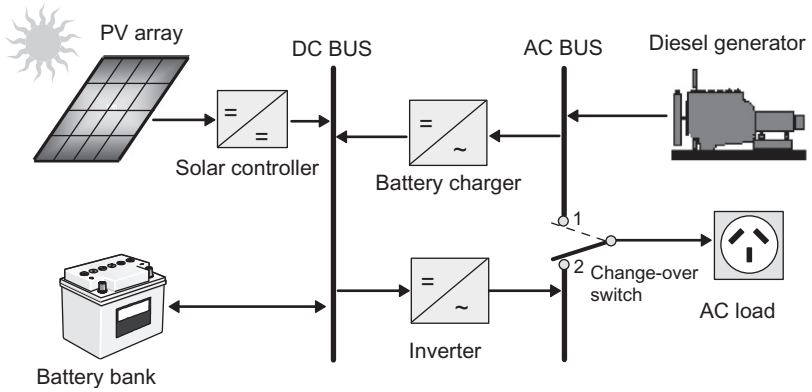


FIG. 25.68 Switched PV-diesel hybrid energy system.

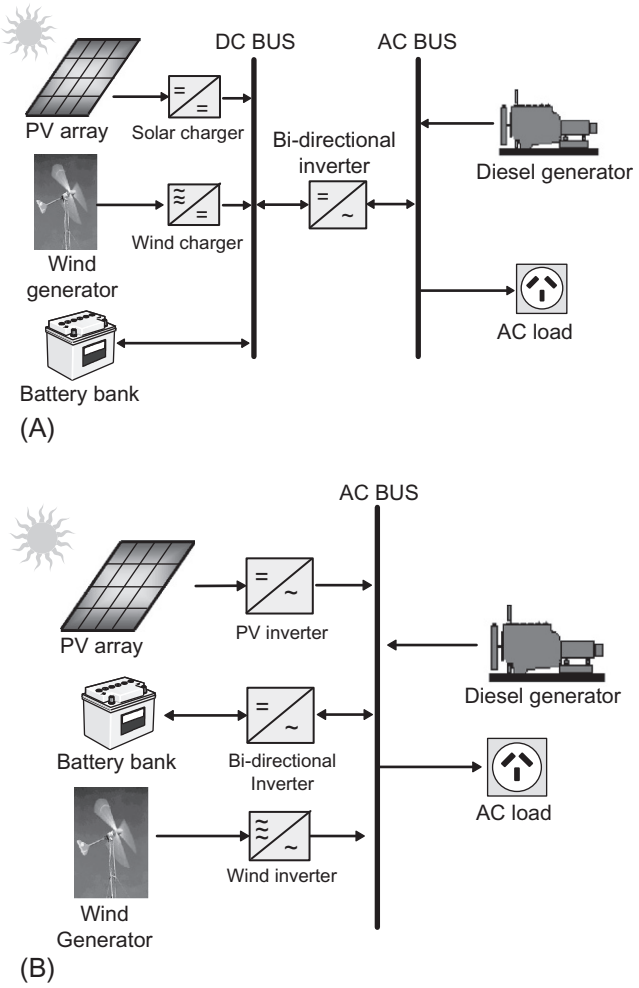


FIG. 25.69 Parallel PV-diesel hybrid energy system: (A) DC decoupling and (B) AC coupling.

devices in one central power unit. This highly integrated system concept has advantages over a more modular approach to system design, but it may prevent convenient system upgrades when the load demand increases.

The parallel configuration offers a number of potential advantages over other system configurations. These objectives can only be met if the interactive operation of the individual components is controlled by an "intelligent" hybrid energy management system. Although today's generation of parallel systems includes system controllers of varying complexity and sophistication, they do not optimize the performance of the complete system. Typically, both the diesel generator and the inverter are sized to supply anticipated peak loads. As a result, most parallel hybrid energy systems do not utilize their capability of parallel, synchronized operation of multiple power sources.

Advantages are as follows:

- The system load can be met in an optimal way.
- Diesel generator efficiency can be maximized.
- Diesel generator maintenance can be minimized.
- A reduction in the rated capacities of the diesel generator, battery bank, inverter, and renewable resources is feasible while also meeting the peak loads.

Disadvantages are as follows:

- Automatic control is essential for the reliable operation of the system.
- The inverter has to be a true sine-wave inverter with the ability to synchronize with a secondary AC source.
- System operation is less transparent to the untrained user of the system.

25.4.4 Control of Hybrid Energy Systems

The design process of hybrid energy systems requires the selection of the most suitable combination of energy sources, power-conditioning devices, and energy storage system together with the implementation of an efficient energy dispatch strategy. System simulation software is an essential tool to analyze and compare possible system combinations. The objective of the control strategy is to achieve optimal operational performance at the system level. Inefficient operation of the diesel generator and "dumping" of excess energy is common for many RAPS, operating in the field. Component maintenance and replacement contributes significantly to the life-cycle cost of systems. These aspects of system operation are clearly related to the selected control strategy and have to be considered in the system design phase.

Advanced system control strategies seek to reduce the number of cycles and the DOD for the battery bank, run the diesel generator in its most efficient operating range, maximize the utilization of the renewable resource, and ensure high reliability of the system. Due to the varying nature of the load demand, the fluctuating power supplied by the photovoltaic generator, and the resulting variation of battery SOC, the hybrid energy system controller has to respond to continuously changing operating conditions. Fig. 25.70 shows different operating modes for a PV single-diesel system using a typical diesel dispatch strategy:

Mode (I). The base load, which is typically experienced at nighttime and during the early morning hours, is supplied by energy stored in the batteries. Photovoltaic power is not available, and the diesel generator is not started.

Mode (II). PV power is supplemented by stored energy to meet the medium load demand.

Mode (III). Excess energy is available from the PV generator, which is stored in the battery. The medium load demand is supplied from the PV generator.

Mode (IV). The diesel generator is started and operated at its nominal power to meet the high evening load. Excess energy available from the diesel generator is used to recharge the batteries.

Mode (V). The diesel generator power is insufficient to meet the peak load demand. Additional power is supplied from the batteries by synchronizing the inverter AC output voltage with the alternator waveform.

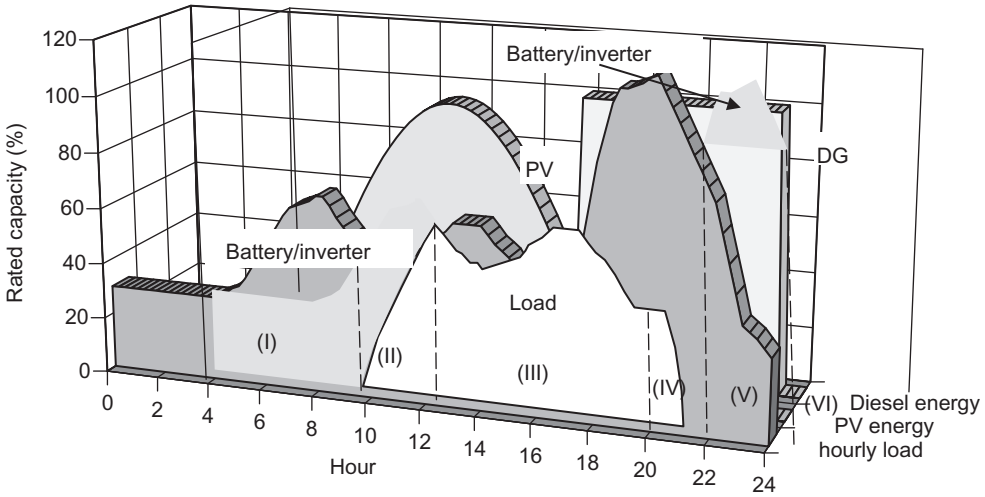


FIG. 25.70 Operating modes for a PV single-diesel hybrid energy system.

Mode (VI). The diesel generator power exceeds the load demand, but it is kept operational until the batteries are recharged to a high SOC level.

In principle, most efficient operation is achieved if the generated power is supplied directly to the load from all energy sources, which also reduces cycling of the battery bank. However, since diesel generator operation at light loads is inherently inefficient, it is common practice to operate the engine-driven generator at its nominal power rating and to recharge the batteries from the excess energy. The selection of the most efficient control strategy depends on fuel, maintenance and component replacement cost, the system configuration, environmental conditions, and constraints imposed on the operation of the hybrid energy system.

25.4.5 Grid-Connected Hybrid Energy Systems

Grid-connected hybrid renewable energy systems (RES), such as PV arrays or wind turbines, engine-driven generators, and battery storage, increase the reliability of the renewable energy supply to the grid [91]. Different RES are connected to a common DC or AC bus, as illustrated in Section 25.4.1. Usually, a power transformer is required to step up the inverter output voltage to a medium-/high-voltage grid. Such power transformer is subjected to a high initial cost, regular maintenance cost, and large physical size [40]. The application of a suitable dielectric material enables the power conditioning of RES to be cheaper, more efficient, and lighter in weight. In [40], a high-frequency, 10–20 kHz magnetic linked cascaded multilevel inverter (CMLI) is proposed, which eliminates the necessity of using a step-up power transformer to interface the CMLI to the grid. The block diagram of such grid-connected hybrid energy systems is shown in Fig. 25.71. Various RES are connected in a common DC bus through suitable converter and high-frequency magnetic link (HFML) that is energized by the common DC bus. The HFML facilitates isolated DC supplies for the three-phase CMLI as shown in Fig. 25.72. The HFML converts the DC bus voltage into 10–20 kHz square-wave

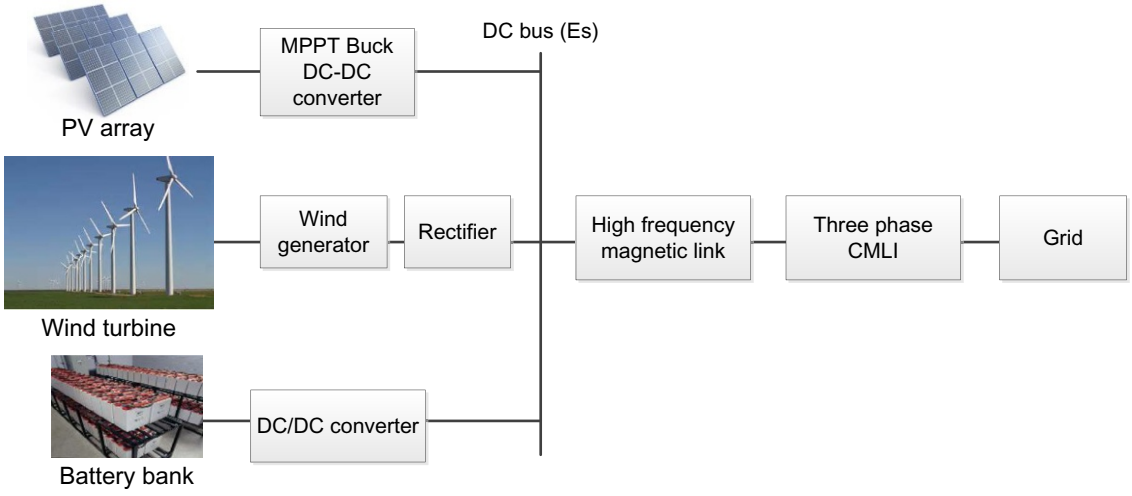


FIG. 25.71 Block diagram of a typical Grid-connected RES hybrid energy system.

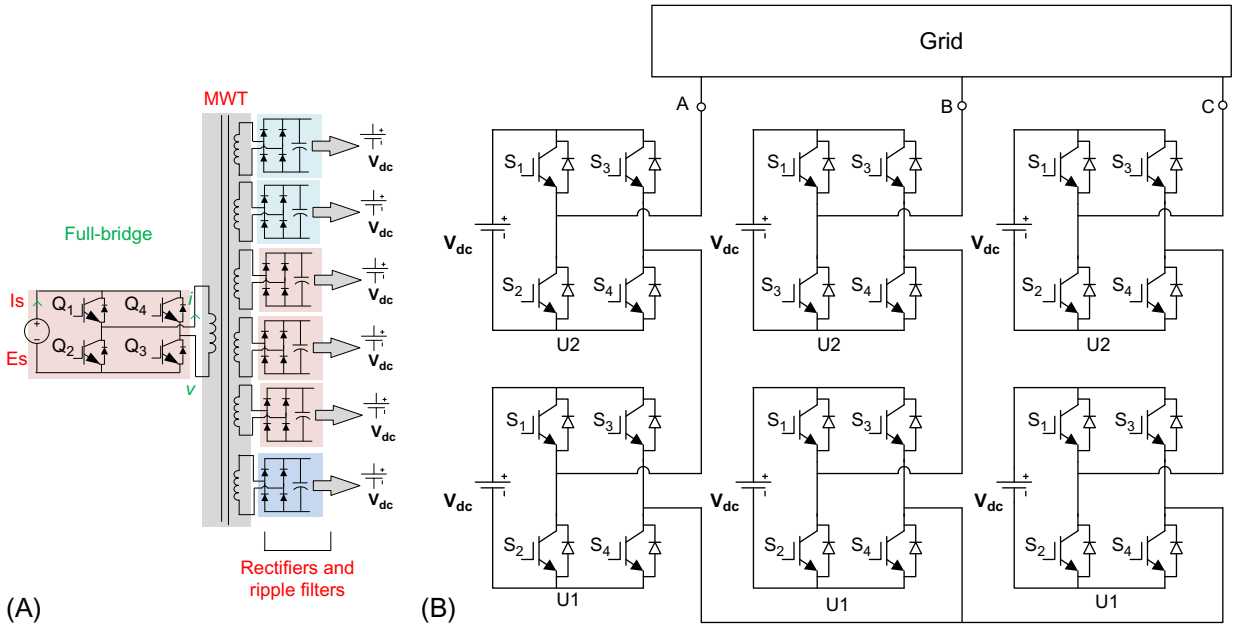


FIG. 25.72 Circuital diagram of the Grid-connected hybrid energy systems. (A) High frequency magnetic link, (B) Grid connected CMLI..

voltage using a full bridge. This high-frequency square-wave voltage is fed to the primary of a multiwinding transformer (MWT), which involves full-bridge diode rectifier connected to the MWT secondary windings as shown in Fig. 25.72A. The output terminals of the rectifiers are connected to the cascaded units of the CMLI as shown in Fig. 25.72B. The CMLI inverter output terminals are connected to the grid. The main reasons of utilizing high-frequency voltage for the MWT are to reduce the transformer core size and to create galvanic isolation between the PV panels and the grid [92]. It is possible to reduce the size of harmonic filter at the inverter output as CMLI generates output voltage with inherently low harmonic contents. Moreover, the cost of the overall conversion system can be reduced by the elimination of the step-up transformer [93,94].

References

[1] G. Hille, W. Roth, H. Schmidt, Photovoltaic system, in: Fraunhofer Institute for Solar Energy Systems, 1995. Freiburg, Germany.

[2] O.H. Wilk, Utility connected photovoltaic systems, presented at International Energy Agency (IEA): Solar Heating and Cooling Program, Montreux, 1992.

[3] R.S. Wenham, M.A. Green, M.E. Watt, Applied photovoltaic, in: Centre for Photovoltaic Device and Systems, University of New Southwales, Sydney, 1998.

[4] W.B. Lawrance, H. Dehbonei, A versatile PV array simulation tools, in: Presented at ISES 2001 Solar World Congress, Adelaide, South Australia, 2001.

[5] M.A.S. Masoum, H. Dehbonei, E.F. Fuchs, Theoretical and experimental analyses of photovoltaic systems with voltage and current-based maximum power-point tracking, IEEE Trans. Energy Convers. 17 (2002) 514–522.

[6] B. Bekker, H.J. Beukes, Finding an optimal PV panel maximum power point tracking method, in: Presented at 7th AFRICON Conference, Africa, 2004.

[7] T. Noguchi, S. Togashi, R. Nakamoto, Short-current pulse based adaptive maximum-power-point tracking for photovoltaic power generation system, in: Presented at Proceedings of 2000 IEEE International Symposium on Ind. Electronics, 2000.

[8] N. Mutoh, T. Matuo, K. Okada, M. Sakai, Prediction-data-based maximum-power-point-tracking method for photovoltaic power generation systems, in: Presented at 33rd Annual IEEE Power Electronics Specialists Conference, 2002.

[9] G.W. Hart, H.M. Branz, C.H. Cox, Experimental tests of open-loop maximum-power-point tracking techniques, Solar Cells 13 (1984) 185–195.

[10] D.J. Patterson, Electrical system design for a solar powered vehicle, in: Presented at 21st Annual IEEE Power Electron. Specialists Conference, 1990.

[11] H.J. Noh, D.Y. Lee, D.S. Hyun, An improved MPPT converter with current compensation method for small scaled PV-applications, in: Presented at 28th Annual Conf. of the Ind. Electronics Society, 2002.

[12] K. Kobayashi, H. Matsuo, Y. Sekine, A novel optimum operating point tracker of the solar cell power supply system, in: Presented at 35th Annual IEEE Power Electronics Specialists Conference, 2004.

[13] P. Midya, P.T. Krein, R.J. Turnhull, R. Reppa, J. Kimball, Dynamic maximum power point tracker for pholovoltaic applications, in: Presented at 27th Annual IEEE Power Electron. Specialists Conference, 1996.

[14] V. Arcidiacono, S. Corsi, L. Larnhri, Maximum power point tracker for photovoltaic power plants, in: Presented at Proceedings of IEEE Photovoltaic Specialists Conference, 1982.

[15] Y.H. Lim, D.C. Hamill, Synthesis, simulation and experimental verification of a maximum power point tracker from nonlinear dynamics, in: Presented at 32nd Annual IEEE Power Electronics Specialists Conference, 2001.

[16] Y.H. Lim, D.C. Hamill, Simple maximum power point tracker for photovoltaic arrays, Electron. Lett. 36 (May 2000) 997–999.
[17] L. Zhang, Y. Bai, A. Al-Amoudi, GA-RBF neural network based maximum power point tracking for grid-connected photovoltaic systems, in: Presented at International Conference on Power Electronics Machines and Drives, 2002.
[18] C.C. Hua, J.R. Lin, Fully digital control of distributed photovoltaic power systems, in: Presented at IEEE International Symposium on Industrial Electronics, 2001.
[19] M.L. Chiang, C.C. Hua, J.R. Lin, Direct power control for distributed PV power system, in: Presented at Proceedings of Power Conversion Conference, 2002.
[20] S. Jain, V. Agarwal, A new algorithm for rapid tracking of approximate maximum power point in photovoltaic systems, IEEE Power Electron. Lett. 2 (2004) 16–19.
[21] N. Femia, G. Petrone, G. Spagnuolo, M. Vitelli, Optimization of perturb and observe maximum power point tracking method, IEEE Trans. Power Electron. 20 (2005) 963–973.
[22] N.S. D'Souza, L.A.C. Lopes, X. Liu, An intelligent maximum power point tracker using peak current control, in: 36th Annual IEEE Power Electronics Specialists Conference, 2005, pp. 172–177.
[23] M.G. Simoes, N.N. Franceschetti, M. Friedhofer, A fuzzy logic based photovoltaic peak power tracking control, in: Proceedings of 1998 IEEE International Symposium on Industrial Electronics, 1998, pp. 300–305.
[24] A.M.A. Mahmoud, H.M. Mashaly, S.A. Kandil, H.E. Khashab, M.N.F. Nashed, Fuzzy logic implementation for photovoltaic maximum power tracking, in: Presented at Proceedings of 9th IEEE International Workshop on Robot and Human Interactive Communication, 2000.
[25] N. Patcharaprakiti, S. Premrudeepreechacharn, Maximum power point tracking using adaptive fuzzy logic control for grid-connected photovoltaic system, in: Presented at IEEE Power Eng Society Winter Meeting, 2002.
[26] B.M. Wilamowski, X. Li, Fuzzy system based maximum power point tracking for PV system, in: Presented at 28th Annual Conference of the IEEE Industrial Electronics Society, 2002.
[27] M. Veerachary, T. Senjyu, K. Uezato, Neural-network-based maximum-power-point tracking of coupled-inductor interleaved-boost-converter-supplied PV system using fuzzy controller, IEEE Trans. Ind. Electron. 50 (Aug 2003) 749–758.
[28] K. Ro, S. Rahman, Two-loop controller for maximizing performance of a grid-connected photovoltaic-fuel cell hybrid power plant, IEEE Trans. Energy Convers. 13 (Sept 1998) 276–281.
[29] A. Hussein, K. Hirasawa, J. Hu, J. Murata, The dynamic performance of photovoltaic supplied dc motor fed from DC–DC converter and controlled by neural networks, in: Presented at Proceedings of 2002 International Joint Conference on Neural Networks, 2002.
[30] X. Sun, W. Wu, X. Li, Q. Zhao, A research on photovoltaic energy controlling system with maximum power point tracking, in: Presented at Proceedings of Power Conversion Conference, 2002.
[31] O. Wasynczuk, Dynamic behavior of a class of photovoltaic power systems, IEEE Trans. Power Appl. Syst. 102 (1983) 3031–3037.
[32] Y.C. Kuo, T.J. Lian, J.F. Chen, Novel maximum-power-point-tracking controller for photovoltaic energy conversion system, IEEE Trans. Ind. Electron. 48 (2001) 594–601.
[33] G.J. Yu, Y.S. Jung, J.Y. Choi, I. Choy, J.H. Song, G.S. Kim, A novel two-mode MPPT control algorithm based on comparative study of existing algorithms, in: Presented at Conference on Record of the Twenty-Ninth IEEE Photovoltaic Specialists Conference, 2002.
[34] K. Kohayashi, I. Takano, Y. Sawada, A study on a two stage maximum power point tracking control of a photovoltaic system under partially shaded insolation conditions, in: Presented at IEEE Power Engineering Society General Meeting, 2003.
[35] D. Langridge, W. Lawrance, B. Wichert, Development of a photovoltaic pumping system using a brushless D.C. motor and helical rotor pump, Solar Energy 56 (1996) 151–160.
[36] N. Mohan, M. Undeland, W.P. Robbins, Power Electronics, John Wiley and Sons Inc, New York, 1995.
[37] M. Calais, V.G. Agelidis, M. Meinhardt, Multilevel converters for single phase grid-connected photovoltaic systems an overview, Solar Energy 66 (1999) 525–535.
[38] B. Xiao, L. Hang, J. Mei, C. Riley, L.M. Tolbert, B. Ozpineci, Modular cascaded H-bridge multilevel PV inverter with distributed MPPT for grid-connected applications, IEEE Trans. Ind. Appl. 51 (2) (2015) 1722–1731.
[39] S. Daher, J. Schmid, F.L.M. Antunes, Multilevel inverter topologies for stand-alone PV systems, IEEE Trans. Ind. Electron. 55 (7) (2008) 2703–2712.
[40] M.R. Islam, G. Youguang, Z. Jianguo, A high-frequency link multilevel cascaded medium-voltage converter for direct grid integration of renewable energy systems, IEEE Trans. Power. Electron. 29 (8) (2014) 4167–4182.
[41] P. Lezana, G. Ortiz, Extended operation of cascade multicell converters under fault condition, IEEE Trans. Ind. Electron. 56 (7) (2009) 2697–2703.
[42] K. Bandara, T. Sweet, J. Ekanayake, Photovoltaic applications for off-grid electrification using novel multi-level inverter technology with energy storage, Renew. Energy 37 (1) (2012) 82–88.
[43] M. Rajkumar, M. Valan, P.S. Manoharan, FPGA based multilevel cascaded inverters with SVPWM algorithm for photovoltaic system, Sol. Energy 87 (2013) 229–245.
[44] E. Beser, et al., A grid-connected photovoltaic power conversion system with single-phase multilevel inverter, Sol. Energy 84 (12) (2010) 2056–2067.
[45] N.A. Rahim, J. Selvaraj, Multistring five-level inverter with novel PWM control scheme for PV application, IEEE Trans. Ind. Electron. 57 (6) (2010) 2111–2123.
[46] K. Hirachi, K. Matsumoto, M. Yamamoto, M. Nakaoka, Improved control implementation of single phase current fed PWM inverter for photovoltaic power generation, in: Presented at Seventh International Conference on Power Electronics and Variable Speed Drives (PEVD'98), 1998.
[47] U. Boegli, R. Ulmi, Realisation of a new inverter circuit for direct photovoltaic energy feedback into the public grid, IEEE Trans. Ind. Appl. 22 (1986).
[48] B. Lindgren, Topology for decentralised solar energy inverters with a low voltage A-bus, in: Presented at EPE99-European Power Electronics Conference, 1999.
[49] K. Masoud, G. Ledwich, Aspects of grid interfacing: current and voltage controllers, in: Presented at Proceedings of AUPEC 99, 1999.
[50] H.K. Sung, S.R. Lee, H. Dehbonei, C.V. Nayar, A comparative study of the voltage controlled and current controlled voltage source inverter for the distributed generation system, in: Presented at Australian Universities Power Engineering Conference (AUPEC), Hobart, Australia, 2005.
[51] L.J. Borle, M.S. Dymond, C.V. Nayar, Development and testing of a 20 kW grid interactive photovoltaic power conditioning system in Western Australia, IEEE Trans. Ind. Appl. 33 (1999) 1–7.

[52] L.J. Borle, C.V. Nayar, Zero average current error controlled power flow for ac-dc power converters, IEEE Trans. Power Electron. 10 (1995) 725–732.
[53] H. Sharma, Grid Integration of Photovoltaics, The University of Newcastle, Australia, 1998.
[54] L.L. Freris, Wind Energy Conversion Systems, Prentice Hall, New York, 1990.
[55] C.V. Nayar, J. Perahia, F. Thomas, Small Scale Wind Powered Electrical Generators, The Minerals and Energy Research Institute of Western Australia, 1992.
[56] R.D. Richardson, G.M. McNerney, Wind energy systems, Proceedings of the IEEE 81 (1993) 378–389.
[57] J. Arillaga, N. Watson, Static power conversion from self-excited induction generators, Proc. Inst. Electr. Eng. 125 (8) (1978) 743–746.
[58] C.V. Nayar, J. Perahia, F. Thomas, S.J. Phillips, T.L. Pryor, W.L. James, Investigation of capacitor excited induction generators and permanent magnet alternators for small scale wind power generation, Renew. Energy 125 (1991) 381–388.
[59] T. Ackermann, L. Sörder, An overview of wind energy status-2002, Renew. Sustain. Energy Rev. 6 (1–2) (2002) 67–128.
[60] S. Peresada, A. Tilli, A. Tonielli, Robust active-reactive power control of a doubly-fed induction generator, in: Presented at IECON′98, 1998.
[61] W.E. Long, N.L. Schmitz, Cycloconverter control of the doubly fed induction motor, IEEE Trans. Ind. Gen. Appl. 7 (1971) 162–167.
[62] A. Chattopadhyay, An adjustable-speed induction motor drive with a thyristor-commutator in the rotor, IEEE Trans. Ind. Appl. 14 (1978) 116–122.
[63] P. Pena, J.C. Clare, G.M. Asher, Doubly fed induction generator using back-to-back PWM converters and its application to variable speed wind-energy generation, in: IEE Proc. Electric Power Appl., 143, 1996.
[64] H. Azaza, On the dynamic and steady state performances of a vector controlled DFM drive, in: Presented at IEEE International Conference on Systems, Man and Cybernetics, 2002.
[65] Bergey Windpower User Manual "10 kW Battery charging wind energy generating system", Bergey Windpower Co., Oklahoma, USA, 1984.
[66] J.H.R. Enslin, F.W. Leuschner, Integrated hybrid energy systems for isolated and semi-isolated users, in: Presented at Proceedigns of Renewable Energy Potential in Southern African Conference, UCT, South Africa, 1986.
[67] D.G. Infield, Wind diesel systems technology and modelling-a review, Int. J. Renew. Energy Eng. 1 (1) (1999) 17–27.
[68] H. Sharma, S.M. Islam, C.V. Nayar, T. Pryor, Dynamic response of a remote area power system to fluctuating wind speed, in: Presented at Proceedings of IEEE Power Engineering Society (PES 2000) Winter Meeting, 2000.
[69] W.L. James, C.V. Nayar, F. Thomas, M. Dymond, Variable speed asynchronous wind powered generator with dynamic power conditioning, Murdoch University Energy Research Institute (MUERI), Australia, 1993.
[70] F. Blaabjerg, Z. Chen, S.B. Kjaer, Power electronics as efficient interface in dispersed power generation systems, IEEE Trans. Power Electron. 19 (2004) 1184–1194.
[71] F. Blaahjerg, Z. Chen, P.H. Madsen, Wind power technology status, development and trends, in: Presented at Proceeding of Workshop on Wind Power and Impacts on Power Systems, Oslo, Norway, 2002.
[72] J. Wilkie, W.E. Leithead, C. Anderson, Modelling of wind turbines by simple models, Wind Eng. 14 (1990) 247–273.
[73] A.L.G. Westlake, J.R. Bumby, E. Spooner, Damping the power angle oscillations of a permanent magnet synchronous generator with particular reference to wind turbine applications, IEE Proc. Electr. Power Appl. 143 (1996) 269–280.
[74] J.F. Manwell, J.G. McGowan, B.H. Bailey, Electrical/mechanical options for variable speed turbines, Solar Energy 46 (1991) 41–51.
[75] T.S. Andersen, H.S. Kirschbaum, Multi-speed electrical generator applications in wind turbines, in: Presented at AIAA/SERI Wind Energy Conference Proceedings, Boulder, 1980.
[76] E. Muljadi, C.P. Butterfield, Pitch-controlled variable-speed wind turbine generation, IEEE Trans. Ind. Appl. 37 (1) (2001) 240–246.
[77] G. Riahy, P. Freere, Dynamic controller to operate a wind turbine in stall region, in: Presented at Proceeding of Solar ′97-Australia and New Zealand Solar Energy Society, 1997.
[78] K. Tan, S. Islam, Optimum control strategies in energy conversion of PMSG wind turbine system without mechanical sensors, IEEE Trans. Energy Convers. 19 (2) (June 2004) 392–399.
[79] K. Tan, S. Islam, Mechanical sensorless robust control of permanent magnet synchronous generator for maximum power operation, in: Presented at Australia University Power Engineering Conference, Australia, 2001.
[80] Q. Wang, L. Chang, An independent maximum power extraction strategy for wind energy conversion system, in: Presented at IEEE Canadian Conference on Electrical and Computer Engineering, Canada, Alberta, 1999.
[81] J. Perahia, C.V. Nayar, Power controller for a wind-turbine driven tandem induction generator, Electric Mach. Power Syst. 19 (1991) 599–624.
[82] K. Tan, S. Islam, H. Tumbelaka, Line commutated inverter in maximum wind energy conversion, Int. J. Renew. Energy Eng. 4 (3) (2002) 506–511.
[83] E. Muljadi, S. Drouilhet, R. Holz, V. Gevorgian, Analysis of permanent magnet generator for wind power battery charging, in: Presented at Thirty-First IAS Annual Meeting, IAS′96, San Diego, CA, USA, 1996.
[84] B.S. Borowy, Z.M. Salameh, Dynamic response of a stand-alone wind energy conversion system with battery energy storage to a wind gust, IEEE Trans. Energy Convers. 12 (1) (1997) 73–78.
[85] A.B. Raju, Application of power electronic interfaces for grid-connected variable speed wind energy conversion systems, in: Department of Electrical Engineering, Indian Institute of Technology, Bombay, 2005.
[86] G.A. Smith, K.A. Nigim, Wind energy recovery by static Scherbius induction generator, IEE Proc. C 128 (1981) 317–324.
[87] T.S. Anderson, P.S. Hughes, Investigation of Doubly Fed Induction Machine in Variable Speed Applications, Westinghouse Electric Corporation, 1983.
[88] H. Dehbonei, C.V. Nayar, A new modular hybrid power system, in: Presented at IEEE International Symposium on Industrial Electronics, Rio de Janeiro, Brazil, 2003.
[89] C.V. Nayar, S.J. Phillips, W.L. James, T.L. Pryor, D. Remmer, Novel wind/diesel/battery hybrid system, Solar Energy 51 (1993) 65–78.
[90] W. Bower, Merging photovoltaic hardware development with hybrid applications in the U.S.A, in: presented at Proceedings Solar ′93 ANZSES, Fremantle, Western Australia, 1993.
[91] L.A. de Souza Ribeiro, O.R. Saavedra, S.L. De Lima, J.G. De Matos, Isolated micro-grids with renewable hybrid generation: the case of Lençóis island, IEEE Trans. Sustainable Energy 2 (2011) 1–11.
[92] M. Jafari, Z. Malekjamshidi, G. Lei, T. Wang, G. Platt, J. Zhu, Design and implementation of an amorphous high frequency transformer coupling multiple converters in a smart micro grid, IEEE Trans. Ind. Electron. 64 (2) (2016) 1028–1037.

[93] X. Yuan, A set of multilevel modular medium-voltage high power converters for 10-MW wind turbines, IEEE Trans. Sustainable Energy 5 (2014) 524–534.
[94] M. Carrasco, L.G. Franquelo, J.T. Bialasiewicz, E. Galván, R.C. P. Guisado, M.Á.M. Prats, et al., Power-electronic systems for the grid integration of renewable energy sources: a survey, IEEE Trans. Ind. Electron. 53 (2006) 1002–1016.

Further Reading

[1] D.P. Hodel, Photovoltaics-electricity from sunlight, U.S. Department of Energy Report, DOE/NBMCE.

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26

Electric Power Transmission

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26.1 Elements of Power System

The growth of electricity production and usage in the world is at an all-time high. It is the fastest growing form of end-use energy worldwide. The world net electricity generation in the year 2006 is estimated at 18 trillion kWh. It is forecasted to be 23.2 trillion kWh in the year 2015 and 31.8 trillion in the year 2030 [1]. Electricity production from fossil fuels raises concern on climate change, and hence, alternative energy sources such as solar, geothermal, wind, wave, tidal, and biomass are being developed rapidly around the world.

Modern electric power system consists of complex interconnected network of components generally divided into generation, transmission, distribution, and load. The invention of the transformer at the end of the nineteenth century enables electric energy to be transmitted at higher voltages and hence higher capacity. In this chapter, the components that make up the modern power system are briefly reviewed, namely, generators, transformers, and transmission line. The chapter will focus on the transmission of electric power and how to optimize its power transfer capability. The chapter will also discuss the phenomena of overvoltages and the insulation requirement of transmission lines. The use of power electronics in electric power transmission is covered in Chapters 31 and 32, respectively, such as high-voltage direct current (HVDC) system and flexible AC transmission system (FACTS) (Fig. 26.1).

26.2 Generators and Transformers

Generators are the starting point in a power system where electricity is generated. The most commonly used type of generator is the synchronous generator, driven by a prime mover. In a thermal power station, the prime mover is powered by steam turbines using coal, gas, nuclear, or oil as the fuel. Steam turbines usually operate at high speed to optimize its power output. For a 60 Hz system, the speed of rotation is 3600 (two-pole machine) or 1800 rpm (four-pole machine). For a 50 Hz system, the speed of rotation is 3000 (two-pole machine) or 1500 rpm (four-pole machine). Hydropower station uses the potential

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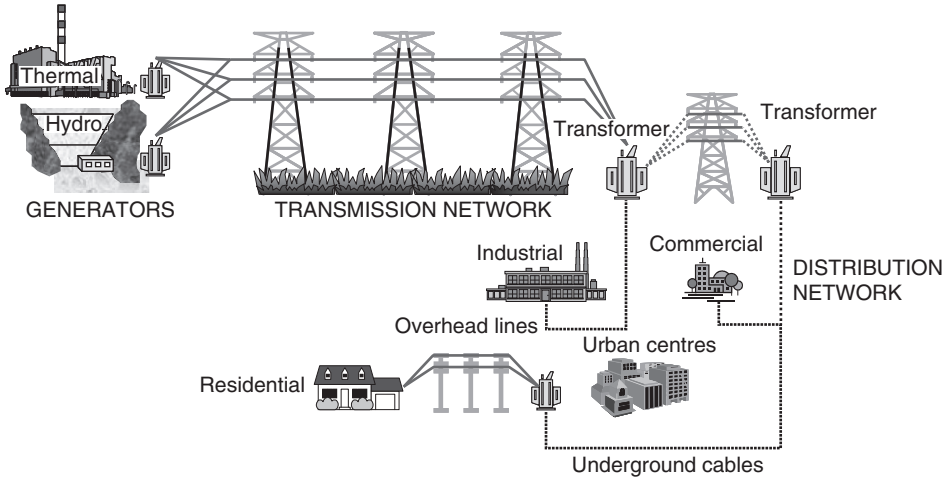


FIG. 26.1 Illustration of the basic components of a power system.

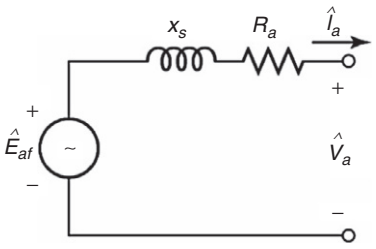


FIG. 26.2 Equivalent circuit of a synchronous generator.

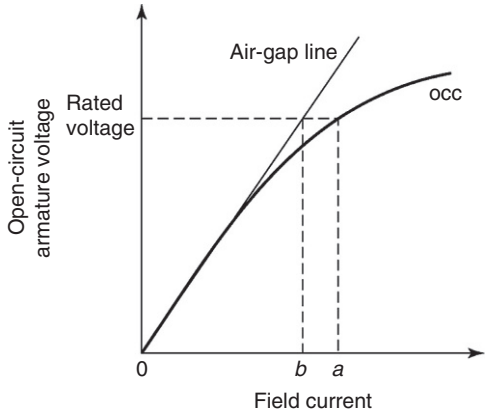


FIG. 26.3 Open-circuit characteristic (occ) of a synchronous generator.

energy of water to power the hydraulic turbines. The hydraulic turbines usually operate at relatively low speed, coupled to generators with salient-type rotor with many poles. In power-generating stations, the electric power is generated at high voltages typically between 10 and 30 kV, while the size of the generators varies from 50 to 1500 MW (Fig. 26.2).

A synchronous generator produces alternating current in the armature winding (usually a three-phase winding on the stator) with dc excitation supplied to the field winding (usually on the rotor). The per-phase equivalent circuit of a synchronous generator is shown below where the armature voltage, V_a, can be written as

$$V_a = R_a I_a + jX_s I_a + E_{af}$$

where

V_a is the armature voltage
R_a is the armature resistance
I_a is the armature current
X_s is the synchronous reactance
E_{af} is the internal generated voltage

The open-circuit characteristic (occ) of a synchronous generator as shown below represents the relationship between the field current I_f and the internal generated voltage E_{af}. Note that with the armature winding open-circuited, the armature voltage V_a is equal to the internal generated voltage E_{af}. As the field current I_f is increased from zero, the armature voltage V_a increases linearly. Near the rated voltage, the saturation effect is clearly seen with the departure of the occ from the straight line (air-gap line) (Fig. 26.3).

Another characteristic of the synchronous generator is illustrated by the V curve shown in Fig. 26.4. For a constant real-power loading, the field current and hence excitation can be adjusted to vary the reactive power VAr generated, hence power factor (pf).

The voltage output of the generator is transformed to a higher voltage before transmitting the power over a long distance to reduce the transmission losses, I^2R losses. Transformers are used to step up or step down the voltage (Fig. 26.5).

Transmission system voltages vary from country to country. For example, in Britain, they are 400 and 275 kV; in the United States, they are 765, 500, and 345 kV, while in Malaysia, they are 500 and 275 kV. The subtransmission network is at 115 kV in the United States, while it is 132 kV in Britain and Malaysia. This network in turn supplies the distribution network to the customers in a given area. In Britain and Malaysia, the distribution

network operates at 33 and 11 kV supplying the customer's feeders at 400 V three-phase and 230 V per-phase. Transformer used in the power system ranges from small 500 kVA distribution transformers to 1000 MVA supergrid transformers.

Detailed theoretical analysis of transformers has been covered in numerous textbooks. It is suffice to show here the equivalent circuit of a transformer to appreciate its electric circuit representation. The component R_c represents the core losses that consist of eddy current losses and hysteresis losses, while the component X_m represents the flow of the magnetization current. Core losses also known as no-load losses are essentially the power required to energize the core. It depends primarily on the voltage and frequency and does not vary much with system operation variations. On the other hand, R_{eq} and X_{eq} represent the primary and secondary winding of the transformer where the load losses originate. Load losses consist of the I^2R losses mainly in the windings and stray losses that include winding eddy losses and the effect of leakage flux entering internal metallic structures (Fig. 26.6).

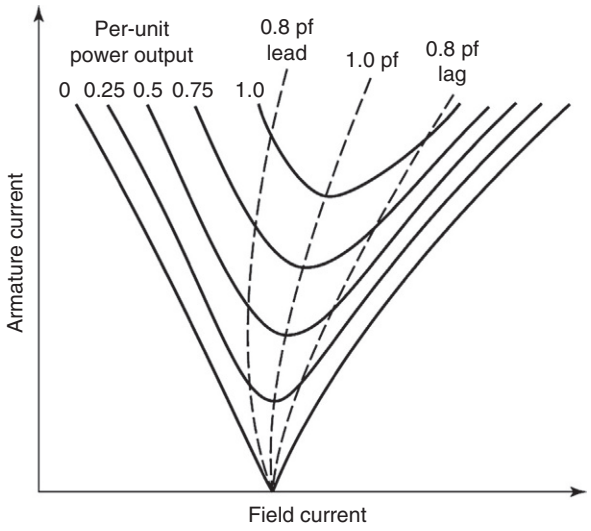


FIG. 26.4 A typical V curve of a synchronous generator.

26.3 Transmission Line

The bulk transfer of electric energy from generating power plants to substations located near population centers is achieved through high-voltage transmission lines. Interconnected transmission lines are referred to as high-voltage transmission networks. Electricity is transmitted at high voltage to reduce the energy lost in long-distance transmission. It is important to understand the characteristic of the important component, which is the conductor, to appreciate the limiting factors to the power transfer capability of the transmission line. The power transfer can then be optimized using latest sensor and communication technology.



FIG. 26.5 Transmission lines out of Connaught Bridge Power Station, Malaysia.

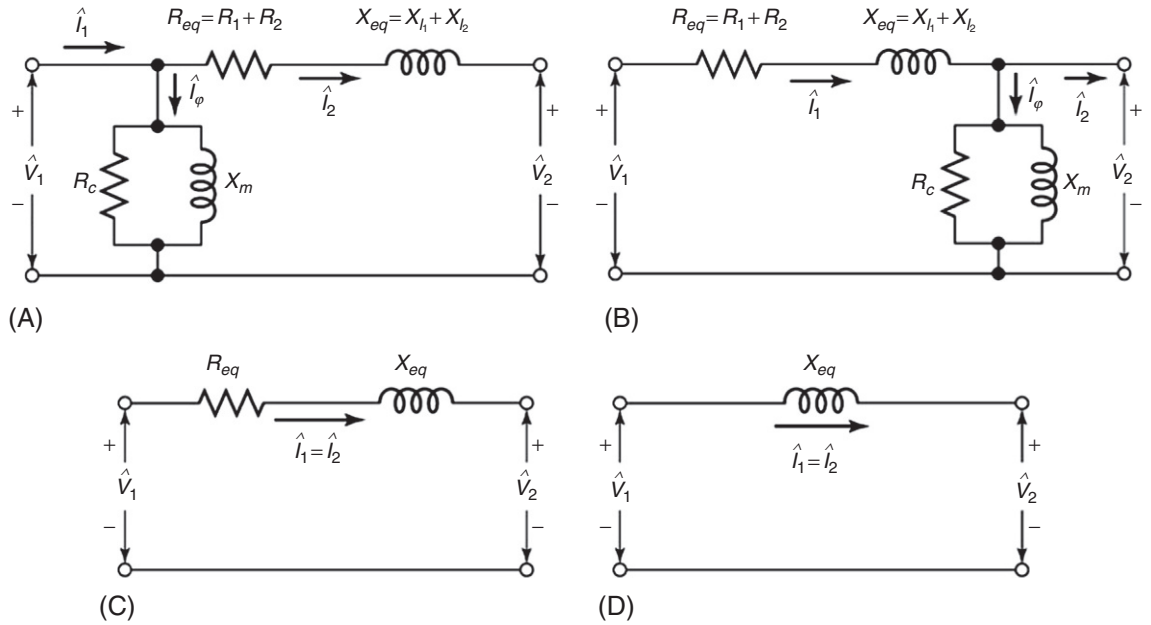


FIG. 26.6 Equivalent circuit representation of a transformer from a comprehensive representation to most simplified. (A) Core-loss at the input side, (B) lose-loss at the output side, (C) core-loss neglected, (D) resistive loss neglected.

The conductor is one of the major components of a transmission line design. It is essential that the most appropriate conductor type and size be selected for optimum operating efficiency. There are four common types of conductors used for many years in electric utilities: (i) all-aluminum conductor (AAC), (ii) aluminum conductor steel reinforced (ACSR), (iii) aluminum conductor alloy reinforced (ACAR), and (iv) all-aluminum alloy conductor (AAAC). Regardless of the type of metal used in the makeup of the conductor, the strands are always round and have a concentric lay.

26.3.1 Aluminum Conductor Steel-Reinforced

Electric utility companies have utilized ACSR as a common choice of conductor in transmission lines for many years. ACSR is used extensively on long spans as both ground and phase conductors because of its high mechanical strength-to-weight ratio and good current-carrying capacity. ACSR consists of solid or stranded coated steel core surrounded by one or more layers of 1350-H19 aluminum. Because of the presence of the 1350 aluminum in the construction, ACSR has equivalent or higher thermal ratings to equivalent sizes of AAC [2] (Fig. 26.7).

The cross-sectional area of ACSR is specified according to the cross-sectional area of aluminum to be contained in the construction. For example, a 428 mm^2 54/7 ACSR has 428 mm^2 of aluminum, the equivalent aluminum area content of 428 mm^2 AAC. The steel content of ACSR typically ranges from 11% to 18% by weight for the conductor stranding of 18/1, 45/7, 72/7, or 84/19. However, it can vary up to 40% depending on the desired tensile strength. It is desirable for ground wires in extra-long spans crossing rivers, for example, to have a stranding of 8/1, 12/7, or 16/19, giving them higher tensile strength. Fig. 26.8 shows the standard stranding of ACSR [3].

The high tensile strength combined with the good conductivity gives ACSR several advantages such as the following:

- The high tensile strength of ACSR allows it to be installed in areas subject to extreme wind loading.
- Because of the presence of the steel core, lines designed with ACSR elongate less than other standard conductors, yielding less sag at a given tension. Therefore, the maximum allowable conductor temperature can be increased to allow a higher thermal rating when replacing other standard conductors with ACSR.
- ACSR is less likely to be broken by falling tree limbs.

26.4 Factors That Limit Power Transfer in Transmission Line

Factors that limit the power transfer are voltage drop, voltage stability, and thermal rating. For short transmission line, which is approximately less than 80 km, the power transfer is limited by the thermal rating. The thermal rating is limited by the maximum operating temperature of the conductor. This maximum operating temperature is limited by the maximum line sag limit and maximum allowable operating temperature of the conductor material.



FIG. 26.7 Steel lattice structure of a transmission line tower.

26.4.1 Static and Dynamic Thermal Rating

Static thermal rating of the overhead transmission line is a fix rating in terms of current-carrying capacity. It is a conservative rating where worse case weather for contributing for maximum heat onto the conductor is assumed.

Dynamic thermal rating of the overhead transmission line is a time-dependence rating where the actual weather and loading of the conductor are measured and the thermal rating is calculated in real time.

26.4.2 Thermal Rating

Bare overhead conductor is normally exposed to environment when it is in service. Due to this reason, the conductor temperature is normally influenced by weather condition and the electric current loading of the conductor. In thermal rating calculation, meteorologic parameters such as wind speed and direction, solar radiation, and ambient temperature are required for the calculation where the calculation is based on heat balance energy equation; in steady-state condition, the conductor heat gain is equal to the heat loss (no heat energy is stored in the conductor). The mathematical representation of the heat balance energy equation as in Eq. (26.1) and by reorganizing the equation as in Eq. (26.2), the thermal rating can be calculated [4]. The heating elements are solar radiation and internal heating by the electric current flow through the conductor resistance or ohmic loss (I^2R). The heat loss is due to convection and radiation:

$$q_c + q_r = q_s + I^2 \cdot R(T_c) \tag{26.1}$$

$$I_{rating} = \sqrt{\frac{q_c + q_r - q_s}{R}} \tag{26.2}$$

where

q_s heat input due to solar, W/m

$I^2R(T_c)$ heat input due to line current (R is a function of conductor temperature)

q_c heat output due to convection (a function of wind, air temperature, and conductor temperature), W/m

q_r heat output due to radiation (a function of wind, air temperature, and conductor temperature), W/m

26.4.3 Convection Heat Loss

Convection heat-loss calculation can be grouped into natural convection and forced convection. The natural convection heat loss, q_{cn}, is calculated in the condition where there is no wind. This happens in all thermal systems where there is a thermal gradient. Heat will migrate from the hotter region to the cooler region until the temperature is uniform across the entire system. The natural convection heat loss (watt per unit length, W/m) for the bare-stranded overhead conductor is a function of air density, ρ_f; conductor diameter, D; and temperature difference between conductor and ambient, $(T_c - T_a)$, as given by Eq. (26.3) [4]:

$$q_{cn} = 0.0205\rho_f^{0.5} D^{0.75} (T_c - T_a)^{1.25} \tag{26.3}$$

In conditions where there is wind, wind blowing against the bare overhead conductor introduces cooling effect where the heat

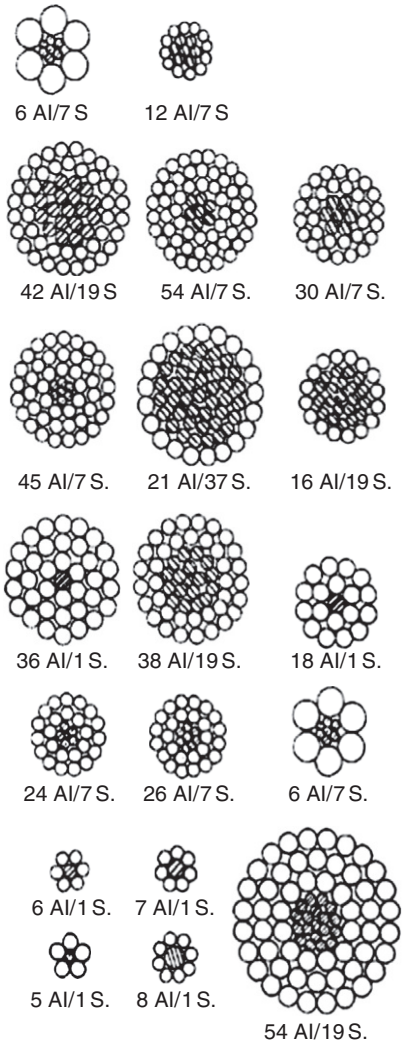


FIG. 26.8 Standard stranding of ACSR conductor.

from the conductor will be transferred over the temperature gradient, from high to low, to the moving air; this is called forced convection heat loss. There are two equations used in the calculation for the forced convection heat loss. One is used for low wind speed, q_{c1}, and another for high wind speed, q_{c2} [4]. The reason that there are two similar, yet independent, equations is because the correction factors incorporated into the equations are proprietary to a certain band of conditions. Eq. (26.4) is for low wind speed, and Eq. (26.5) is for high wind speed:

$$q_{c1} = \left[1.01 + 0.0372\left(\frac{D\rho_f V_w}{\mu_f}\right)^{0.52} \cdot k_f \cdot k_{angle} \cdot (T_c - T_a)\right] \text{W/m} \tag{26.4}$$

$$q_{c2} = \left[0.0119\left(\frac{D\rho_f V_w}{\mu_f}\right)^{0.6} \cdot k_f \cdot k_{angle} \cdot (T_c - T_a)\right] \text{W/m} \tag{26.5}$$

where air density, ρ_f; air viscosity, μ_f; and coefficient of thermal conductivity of air, k_f, are calculated using Eqs. (26.8), (26.9), and (26.10), respectively, at T_{film} where

$$T_{film} = \frac{T_c + T_a}{2} \tag{26.6}$$

At any wind speed, the highest of the two calculated forced convection heat-loss rates is used. The angle at which the wind is blowing relative to the conductor's axis is also considered. The convective heat-loss rate is multiplied by the wind direction factor, K_{angle}, where ϕ is the angle between the wind direction and the conductor axis. This modifying factor is used to create a modified forced convective heat-loss value. The maximum heat loss will occur when the wind is perfectly perpendicular. The wind direction factor is calculated using Eq. (26.7):

$$K_{angle} = 1.194 - \cos(\phi) + 0.194\cos(2\phi) + 0.368\sin(2\phi) \tag{26.7}$$

$$\rho_f = \frac{1.293 - 1.525 \times 10^{-4} H_e + 6.379 \times 10^{-9} H_e^2}{1 + 0.00367 T_{film}} \text{kg/m}^3 \tag{26.8}$$

$$\mu_f = \frac{1.458 \times 10^{-6} (T_{film} + 273)^{1.5}}{T_{film} + 383.4} Pa.s \tag{26.9}$$

$$k_f = 2.424 \times 10^{-2} + 7.477 \times 10^{-5} T_{film} - 4.407 \times 10^{-9} T_{film}^2 \, W/m^\circ C \tag{26.10}$$

26.4.4 Radiative Heat Loss

Radiative heat loss is usually a small fraction of the total heat loss. It is depending on conductor diameter, D; emissivity, ε; conductor temperature, T_c; and ambient temperature, T_a, as given by Eq. (26.11) [4]. If the ambient temperature is kept constant, for example, at 28°C, the radiative heat loss increases exponentially with conductor temperature as shown in Fig. 26.9. Emissivity, ε, is dependent on the conductor surface and varies from 0.27 for new stranded conductor to 0.95 for industrial weathered conductors [5]. It is equal to the ratio of the heat radiated by the conductor and to the heat radiated by a perfect blackbody of the same shape and orientation. Typical values for new bare overhead conductor are between 0.2 and 0.3. The solar emissivity of a new bare overhead conductor increases with age. A typical value for a conductor that has been in use for more than 5 (in industrial environments) to 20 years (in rural clean environments) is 0.7. A value of 0.5 is used if nothing is known about the conductor emissivity [4]:

$$q_r = 0.0178 D\varepsilon \left[\left(\frac{T_c + 273}{100}\right)^4 - \left(\frac{T_a + 273}{100}\right)^4\right] \text{W/m} \tag{26.11}$$

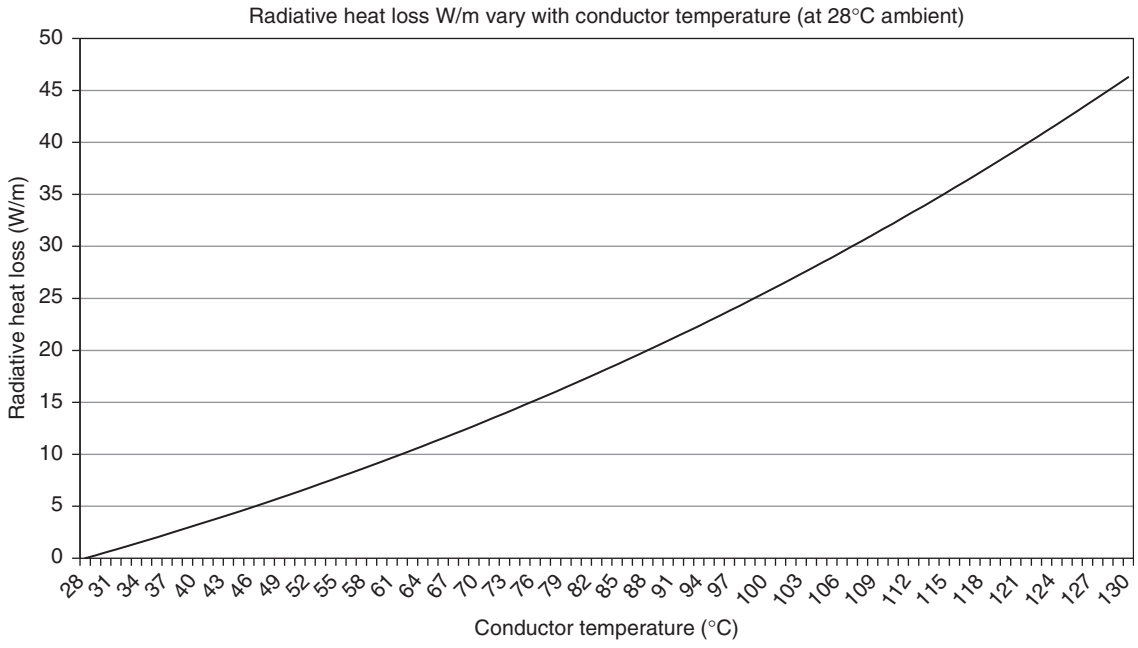


FIG. 26.9 Radiative heat loss (W/m) as function of conductor temperature.

26.4.5 Solar Heat Gain

The solar heat gain, q_s, depends on the conductor diameter, D; absorptivity, α; and global solar radiation, S, as given by Eq. (26.12):

$$q_s = \alpha SD \tag{26.12}$$

The conductor solar absorptivity, α, is a number that varies between 0.27 for bright stranded aluminum conductor and 0.95 for weathered conductor in industrial environment. It is equal to the ratio of the solar heat absorbed by the conductor to the solar heat absorbed by a perfect blackbody of the same shape orientation. Typical values for new conductor are between 0.2 and 0.3. The solar absorptivity of an overhead conductor increases with age. A typical value for a conductor that has been in use for more than 5 (in industrial environments) to 20 years (in rural clean environment) is 0.9. A value of 0.5 is often used if nothing is known about the conductor absorptivity [4].

26.4.6 Ohmic Losses ($I^2R(T_c)$) Heat Gain

The ohmic loss of the bare overhead conductor is depending on the amount of current flows and conductor electric resistance, whereas the conductor electric resistance is depending on conductor temperature. For all bare overhead conductors, controlled lab tests have been carried out; high and low temperature and electric resistance values have been established. This is then published as a guide for electric utilities to use as a reference in their estimation of their system's performance. As upper and lower limits have been defined, it is merely a matter of interpolation to obtain values between the given temperatures. For values outside the envelope, extrapolation can be readily used to obtain the result with reasonable accuracy. For example, lab tests conducted for 1350-H19 aluminum show that for entry resistance values at temperatures of 25°C and 75°C, the errors are negligible [6]. For entry resistance values at temperatures of 25°C and 175°C, the errors are approximately 3% too low at 500°C but 0.5% too high at 75°C. It is concluded that the use of resistance data for temperatures of 25°C and 75°C is adequate for rough calculation of steady-state and transient thermal rating for conductor temperature up to 175°C. The formula that is used to obtain the resistance of the conductor, per unit length, based on the established lab test results is given in Eq. (26.13):

$$R(T_c) = \left[\frac{R(T_{High}) - R(T_{Low})}{T_{High} - T_{Low}}\right] \cdot (T_c - T_{Low}) + R(T_{Low}) \tag{26.13}$$

26.5 Effect of Temperature on Conductor Sag or Tension

26.5.1 Conductor Temperature and Sag Relationship

The relationship of the sag to the temperature of a homogenous conductor is almost linear. A third-degree equation gives a very close approximation of the temperature as a function of the sag, Eq. (26.14) [7]:

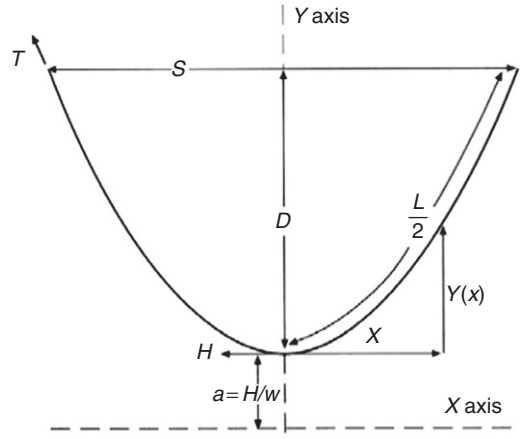


FIG. 26.10 Catenary sag model—level span [7,8].

$$\text{Temperature} = T_0 + A(S - S_0) + B(S - S_0)^2 + C(S - S_0)^3 \tag{26.14}$$

The line sag can be determined from the measured tension or direct measured ground clearance. For practical purposes, the sag can be considered to be inversely proportional to the tension in most spans. For a higher degree of accuracy, the sag/tension relationship can be determined to any desired degree of accuracy based on catenary equations. For level conductor spans as in Fig. 26.10, the low point is in the center of the total sag, D, given by Eq. (26.15):

$$D = \frac{H}{w}\left[\cosh\left(\frac{ws}{2H}\right) - 1\right] \tag{26.15}$$

The horizontal component of tension, H, is located at the point in the span where the conductor slope is horizontal or at the midpoint for level spans. The conductor tension, T, is found at the ends of the spans at the point of attachment and is calculated using Eq. (26.16), and it corresponds to a conductor length, L, given by Eq. (26.17):

$$T = H + wD \tag{26.16}$$

$$L = \left(\frac{2H}{w}\right)\sinh\left(\frac{Sw}{2H}\right) \tag{26.17}$$

Eq. (26.17) describes the behavior of ideal (with perfectly elastic stress and strain characteristics) concentric-lay-stranded conductors [6]. The actual conductors such as ACSR conductors exhibit nonlinear behavior when loaded from initial tension to some final value due to wind or temperature loading. Permanent elongation from creep and heavy loading also affects the resulting sag. Also, high-temperature operations result in thermal elongation of the steel and aluminum strands, thus affecting sag. Therefore, in order to calculate the correct sag, it is necessary to separate the effects of conductor elongation due to tensile loading and thermal loading. This process requires an iterative procedure in which the mathematical formulas describing the conductor elongation caused by the temperature change are solved simultaneously with the tension and conductor length relationship. To calculate the change in length due to temperature loading, Eq. (26.18) is used:

TABLE 26.1 Coefficients of thermal expansion for bare-stranded conductors [8]

Conductor	α (per °C)
AAC	23.0×10^{-6}
36/1 ACSR	22.0×10^{-6}
18/1 ACSR	21.1×10^{-6}
45/7 ACSR	20.7×10^{-6}
54/7 ACSR	19.5×10^{-6}
26/1 ACSR	18.9×10^{-6}
30/7 or 30/19 ACSR	17.5×10^{-6}

$$L_T = L_{T_{REF}}\left[1 + \alpha_{AS}\left(T - T_{rRef}\right)\right] \tag{26.18}$$

where

L_T = final length of conductor
$L_{T_{REF}}$ = reference length of the conductor
α_{AS} = coefficient of linear thermal elongation for AL/SW strands, given in Table 26.1
$\left(T - T_{rRef}\right)$ = change in temperature

For inclined spans, the length of the conductor between the supports is divided into two separate sections as in Fig. 26.11. The same equation in (26.15) can be used for the calculation of the height of the conductor. In each part of the span, the sag is dependent upon the vertical distance between support points and can be described by Eqs. (26.19) and (26.20) [7]:

$$D_R = D\left(1 - \frac{h}{4D}\right)^2 \tag{26.19}$$

$$D_L = D\left(1 + \frac{h}{4D}\right)^2 \tag{26.20}$$

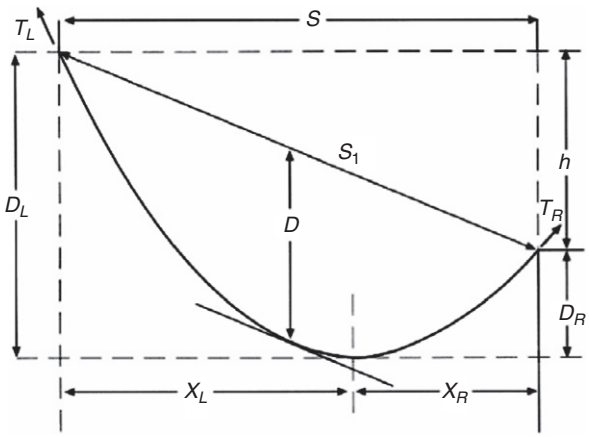


FIG. 26.11 Catenary sag model—inclined span [7,8].

Most of the sag and tension calculations are typically performed with line rating software, for example, PLS-CADD software from Power Line Systems, Inc., the Unites States. To demonstrate the process on how sags and tensions occur for overhead line, simplified sag calculations and conductor length can be done by using Eqs. (26.21) and (26.22), respectively [6]:

$$D = \frac{H}{w}\left[\cosh\left(\frac{ws}{2H}\right) - 1\right] \asymp \frac{wS}{8H} \tag{26.21}$$

$$L = \left(\frac{2H}{w}\right)\sinh\left(\frac{Sw}{2H}\right) \asymp S + \frac{8D^2}{3S} \tag{26.22}$$

The example of the relationship between conductor temperature and conductor sag can be describe by the following example [8].

A transmission line with ACSR conductor 795 kcmil (405 mm^2) and a 1000 ft level span. The conductor weight per unit length is 1.094 lb/ft (1.6 kg/m), ambient temperature is 77°F (25°C), and horizontal tension component, H, is 25% of the ultimate tension strength (31,500 lb):

$$H = 0.25 \times 31{,}500\text{lbs} = 7875\text{lbs}(35{,}196\text{N})$$

Conductor sag, D, is calculated by using Eq. (26.21):

$$D = \frac{wS^2}{8H} = \frac{1.094(1000)^2}{(8)7875} = 17.37\text{ft}(5.29\text{m})$$

Conductor length, L, is calculated by using Eq. (26.22):

$$L = S + \frac{8D^2}{3S} = 1000 + \frac{8(17.37)^2}{3(1000)} = 1000.8\text{ft}(305.05\text{m})$$

Eq. (26.18) is used to calculate the conductor length when the conductor temperature increases from ambient to 50°C (122°F) and then to 150°C (302°F). The coefficient of linear thermal expansion is $10.7 \times 10^{-6}/°\text{F}$:

$$\begin{aligned} L_T &= L_{T_{REF}}[1 + \alpha_{AS}(T - T_{rRef})] \\ L_{(122)} &= 1000.80[1 + 10.7 \times 10^{-6}(122 - 77)] \\ &= 1001.28\text{ft}(305.2\text{m}) \\ L_{(302)} &= 1000.80[1 + 10.7 \times 10^{-6}(302 - 77)] \\ &= 1003.21\text{ft}(305.8\text{m}) \end{aligned}$$

The conductor sag is calculated by rearranging Eq. (26.22):

$$\begin{aligned} D &= \sqrt{\frac{3S(L-S)}{8}} \\ D_{(122)} &= \sqrt{\frac{3(1000)(1.28)}{8}} = 21.9\text{ft}(6.68\text{m}) \\ D_{(302)} &= \sqrt{\frac{3(1000)(3.21)}{8}} = 34.7\text{ft}(10.58\text{m}) \end{aligned}$$

The relationship of the conductor temperature and the conductor sag for the above example can be summarized in Table 26.2.

TABLE 26.2 Relationship between conductor temperature and conductor sag for the ACSR conductor 405 mm^2 for a 1000 ft level span [6]

Conductor temperature (°C)	Conductor sag, D (m)
25	5.29
50	6.68
150	10.58

The conductor temperature corresponds to the measured sag given by Eq. (26.14), since the current conductor temperature is known; the dynamic thermal rating for the maximum conductor temperature, for example, at 75°C can be calculated by using Eq. (26.2).

From the known conductor temperature, the value of q_r can be calculated by the thermal rating Eq. (26.11). The value of q_s can be calculated by Eq. (26.12); the conductor resistance at the known temperature can be calculated by Eq. (26.13). By rearranging the thermal balance equation and with the known value of conductor current, the convective heat loss q_c can be calculated using Eq. (26.23):

$$q_c = I^2R(t) + q_s - q_r \tag{26.23}$$

From the known value of q_c, the equivalent perpendicular wind speed can be calculated by Eq. (26.4) or (26.5). Assuming the equivalent perpendicular wind speed is constant, then the thermal rating at the maximum conductor temperature can be calculated.

26.6 Standard and Guidelines on Thermal Rating Calculation

Reference standard for thermal rating calculation is published by IEEE; the first standard is IEEE Std 738-1993, IEEE Standard for Calculation of Bare Overhead Conductor Temperature and Ampacity Under Steady-State Conditions. Later, the new revision of this standard is published, IEEE Std 738-2006. The revised standard has additional information that addresses fault current and transient rating calculation, SI units were used throughout, and the solar heating calculation was extensively revised to cater for most part of the world instead of only 20 degrees north and above in the first standard IEEE Std 738-1993. The IEEE standard presents a method of calculating the current-temperature relationship of overhead lines given the weather conditions. The heat balance energy equation used for thermal rating calculation is described in details in this standard. The equation relating electric current to conductor temperature described in this standard can be used in two ways:

- To calculate the conductor temperature when the electric current is known
- To calculate the current that yields a given maximum allowable conductor temperature

Other guidelines on thermal rating calculation were developed by CIGRE working group WG 22.12, published in Electra No. 144 in October 1992, The thermal behavior of overhead conductors, Sections 1 and 2: Mathematical model for evaluation of conductor temperature in the steady state and the application thereof. And another one was published in Electra No. 174 in October 1997, The thermal behavior of overhead conductors, Section 3: Mathematical model for evaluation of conductor temperature in the unsteady state. In these guidelines, the heat balance energy equation is discussed in more details compared with in IEEE standard where other addition elements are added in the heat balance energy equation such as magnetic heating, corona heating, and evaporating cooling.

26.7 Optimizing Power Transmission Capacity

26.7.1 Overview of Dynamic Thermal Current Rating of Transmission Line

Real-time thermal rating methods can be classified into two basic types: weather model (WM) and conductor temperature model (CTM) [4]. The difference between the two models is the method by which the conductor convective heat-transfer coefficient is calculated. The WM approach calculates the convective heat-transfer coefficient using ambient temperature, wind speed, and wind direction data together with empirical expressions for convective heat transfer for airflow past cylindrical objects. The CTM computes the convective heat-transfer coefficient directly using the conductor heat balance energy equation, conductor temperature, air temperature, and conductor current. There are five main dynamic thermal rating techniques in WM and CTM, that is, weather monitoring, line tension monitoring, sag monitoring, line temperature monitoring, and conductor replica technique. The most appropriate technique depends upon a particular application and is based on various issues including accuracy, cost, and ease of installation [8].

In general, the overview of DTCR system is as shown in Fig. 26.12. There are three main components that form the dynamic thermal current rating (DTCR) system: remote monitoring station, communication system, and the system computer. Remote monitoring station gathers information on the environment in which the transmission lines are located and also information on the line sag/clearance or tension or conductor temperature. The remote monitoring station is normally placed at a critical location along the transmission line where the wind cooling is minimal or where there is an increased probability of contact between the conductor and objects on the ground.

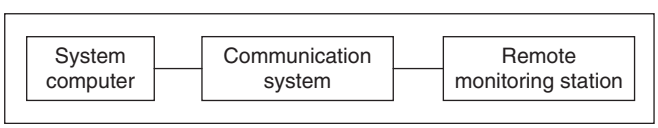


FIG 26.12 Dynamic thermal current rating (DTCR) system block diagram.

The communication system used in this real-time thermal rating system can be wireless or wired system. Normally, wireless communication system is more suitable for the thermal rating system compared with wired system due to connectivity issues and cost. The wireless system is easy to be implemented; it is robust and suitable for use in the outdoor environment. Data transfer from the remote monitoring station to the system computer can be based on dial-up connection at certain time intervals.

The system computer normally consists of two software modules, thermal rating calculation module and thermal rating display module. It has two primary functions, namely, to process the weather and line clearance data then calculate the thermal rating of the line and to display the thermal rating in real time.

As electric current in an overhead conductor increases, the line temperature increases, and therefore, the line sags. Each line has a minimum clearance to ground, which must never be violated for safety reasons. The thermal rating is the maximum current that results in the line sagging down exactly to the minimum clearance. Any additional current would result in too much sag and therefore breaches the safety requirement [9].

There are a few methods of transmission line sag monitoring that has been developed. One of the methods proposed is based on global positioning system (GPS). The method is known as differential GPS [10]. This mode consists of the use of two GPS receivers, the base and the rover as shown in Fig. 26.13. The actual position of the base is known (e.g., by precise surveying) and compared with the readings received at the same base point. With the estimated error, the readings obtained at the rover can be compensated by simple subtraction.

Another method to monitor the line sag is by using smart camera. This method is developed by Electric Power Research Institute (EPRI), the United States [4]. The system uses an imaging system to monitor the location of the conductor or a target attached to it as shown in Fig. 26.14. The imaging system is installed on either a transmission line structure or any other structure with a view of the span being monitored. The field of view of the imaging system remains the same at all time, and the location of the conductor or the target in the view changes as the conductor moves up, down, or horizontally. Image-processing technique is used to determine the location of the conductor or the target attached to the conductor in the camera's field of view. The search algorithm uses a preselected subimage of the target and searches the image to determine the most likely location of the target in the camera image. The key for the success of this approach is to have a target with unique features that cannot be easily found in the background. The change in vertical position of the conductor in the image is

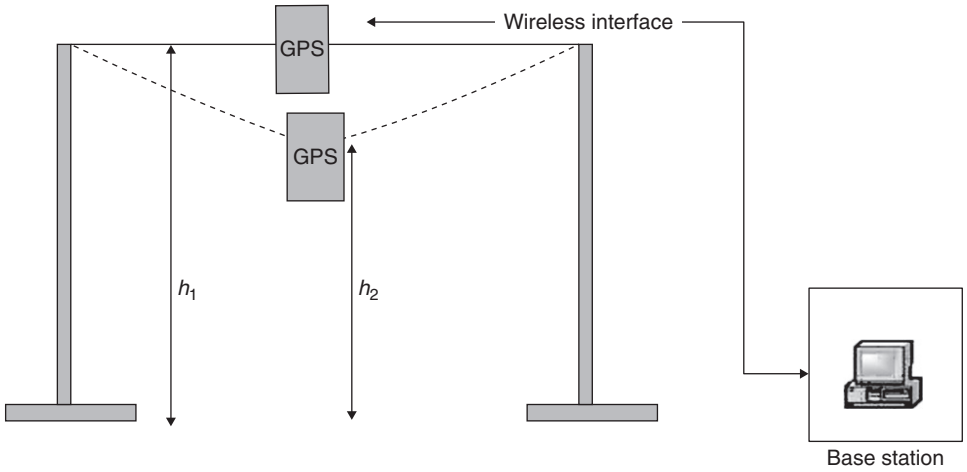


FIG. 26.13 Line sag measurement using differential GPS technique [6].

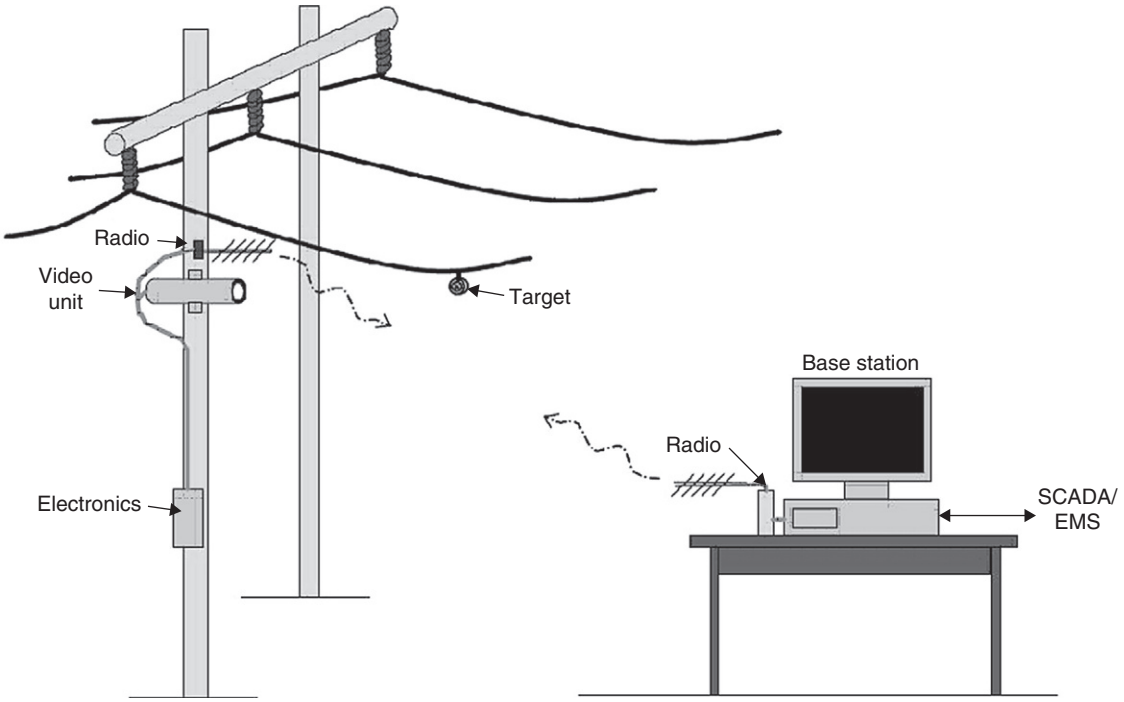


FIG. 26.14 Line sag measurement using smart camera [11].

directly related to the change in ground clearance or sag. At the time of installation, location of the conductor or the target attached to the conductor in the imaging system's field of view is calibrated to the measured ground clearance/sag. Ground clearance or sag at any later time is obtained from the measured change in location of the conductor using calibration constants obtained at the time of system calibration. The resulting clearance information may be made available on a real-time basis using telemetry and/or logged in a data logger for historical study. An effective conductor temperature is calculated using sag-tension routines of line rating software such as PLS-CADD software from Power Line Systems, Inc., the United States, and the real-time ratings is calculated using IEEE standard 738 [4].

Tension monitors consist of solar-powered line tension monitoring system located along the transmission line that communicate the measured data via spread-spectrum radios to receiving units at substations that are further linked to the utility's EMS/SCADA systems. The conductor tension is measured using load cell installed at the dead-end insulators.

There are also sensors that measure the ambient temperature and the net radiation at the conductor. All data are transmitted to the center processor computer for the line thermal rating calculation. The calibration of the system allows determination of the conductor temperature based on the measured tension [2].

Direct measurement of conductor temperature method uses temperature sensor that is directly attached to the conductor. It uses solid-state thermoelectric sensors, and it is powered up using line-current transformer. The system was developed by Niagara Mohawk in the 1980s, and the temperature sensor was called Power Donut. This method can provide conductor temperature data in real time. Power Donut has ambient and conductor temperature measurement accuracy of $\pm 2°C$ over a range of $-40°C$ to $125°C$ [12]. The advantage of this method is that the user has a direct measurement of conductor temperature. If the line rating is intended to limit the loss of conductor strength at high temperature, then this method is mostly appropriate.

Ground clearance has direct relationship with line sag as they depend on conductor temperature. Therefore, thermal rating can also be determined by monitoring the ground clearance. Laser distance measurement sensor can be used to measure the distance between the transmission line and ground. The installation of the laser distance measurement sensor must be at the middle of the span on the ground directly under the transmission line as shown in Fig. 26.15.

To enable continuous monitoring of the line clearance, the sensor can be set to operate in automatic mode that will take measurement continuously for a certain time interval. The line thermal rating can be calculated based on the conductor temperature determined by the clearance measurement.

A number of studies have shown that it is possible to calculate the thermal rating of an overhead conductor in a single span if the weather conditions in the span are known. This can be done using historical weather data records in order to select appropriately conservative static ratings, or it can be done in real time as a basis to dynamically rate the line. By accounting for variations in span orientation along a transmission line, it was found that the weather data from a single weather station as far as 20 mi away could be used to predict the statistical distribution of thermal ratings for that line [5]. For a real-time monitoring, the dynamic thermal rating of the line is calculated using real-time value of the line load current and the weather data. Example of a weather station installation at the transmission line is shown in Fig. 26.16.



FIG. 26.16 Weather monitoring using a weather station for transmission line in Malaysia.

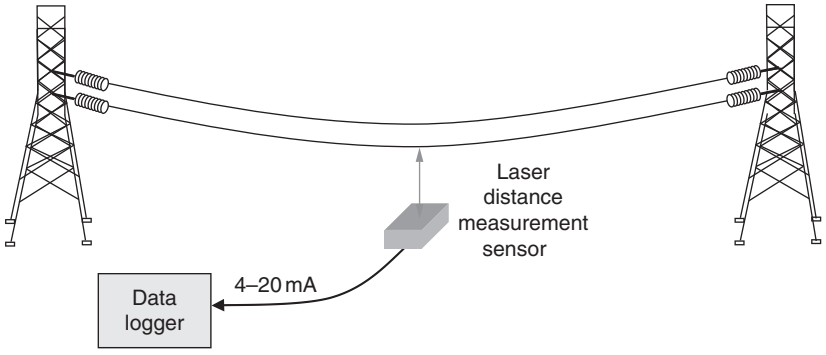


FIG. 26.15 Laser distance measurement sensor installation.

26.7.2 Example of Dynamic Thermal Current Rating of Transmission Line

The dynamic rating profile as shown in Fig. 26.17 is based on DTCR calculations using weather data recorded by a weather station for one of the transmission lines in Malaysia [13]. The figure shows three curves:

- Measured load on the line
- Static rating
- Calculated dynamic rating from DTCR software

It is important to note that

- the dynamic rating is almost always greater than the static rating,
- the measured load is always significantly lower than the static rating.

For statistical representation of the thermal rating, the thermal rating data for certain duration, for example, 6 months, can be represented using probability density plot. The probability density plot shows the frequency of the thermal rating in a certain period of time. It can be used as a guide for operating the transmission line or revising the static rating. Example of the probability density plot is shown in Fig. 26.18.

The graphs show that the load is always below the static rating. Only during emergencies, the load would exceed the normal static rating. The dynamic thermal rating is mostly 20% higher than the static rating that is shown at the tip of the dynamic thermal rating probability density graph in Fig. 26.18. This is the available potential extra capacity ready to be utilized when DTCR system is used to monitor the line rating.

26.8 Overvoltages and Insulation Requirements of Transmission Lines

The considerations for insulation requirements of transmission lines are critical because overvoltages can occur as a result of lightning strokes, switching, faults, load failure, and others. Overvoltages are transitory phenomena. It is defined as any transitory voltage between phase and ground or between phases with a crest value higher than the crest value of maximum system voltage [14]. These overvoltages are often expressed in per unit values, with maximum system voltage as per unit base.

For example, the phase-to-ground per unit overvoltage is

$$V_{\text{pu}} = \frac{V_{\text{L-G}}\sqrt{3}}{V_{\text{m}}\sqrt{2}}$$

where

V_{pu} = per unit phase-to-ground overvoltage

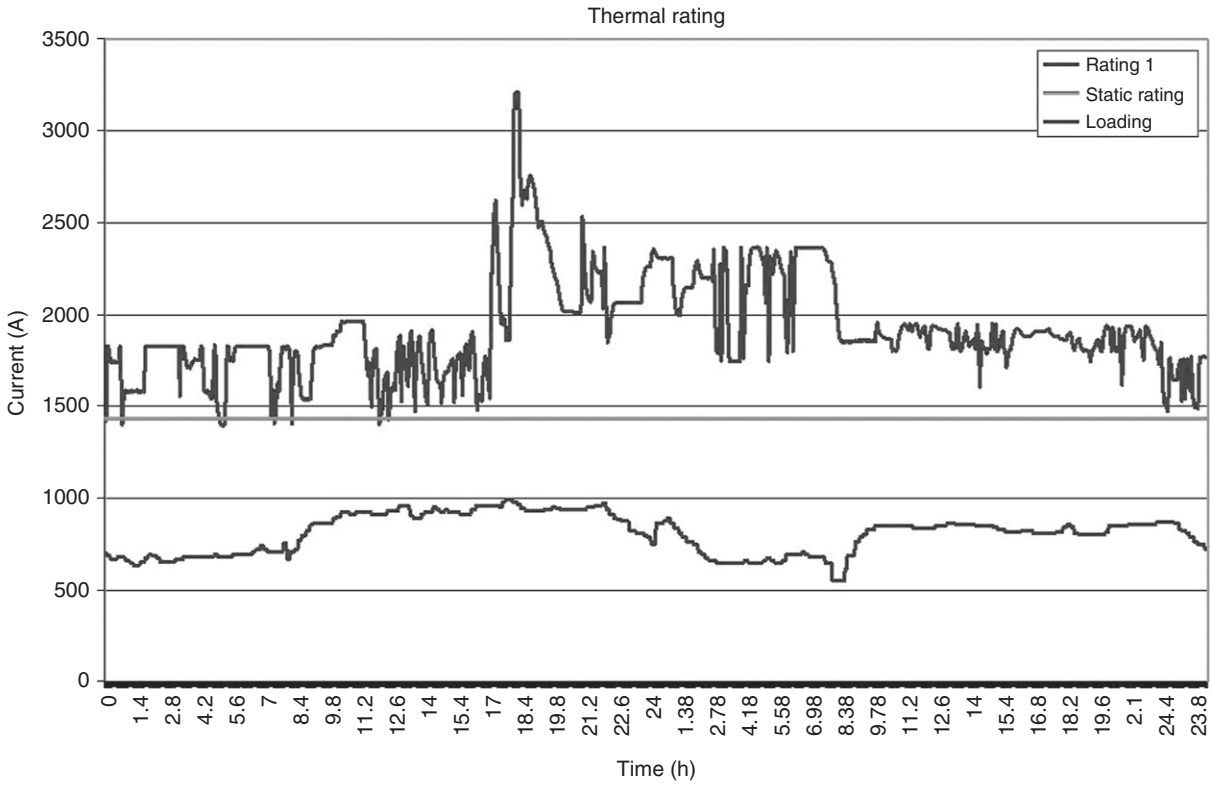


FIG. 26.17 Dynamic thermal rating profile of a transmission line in Malaysia.

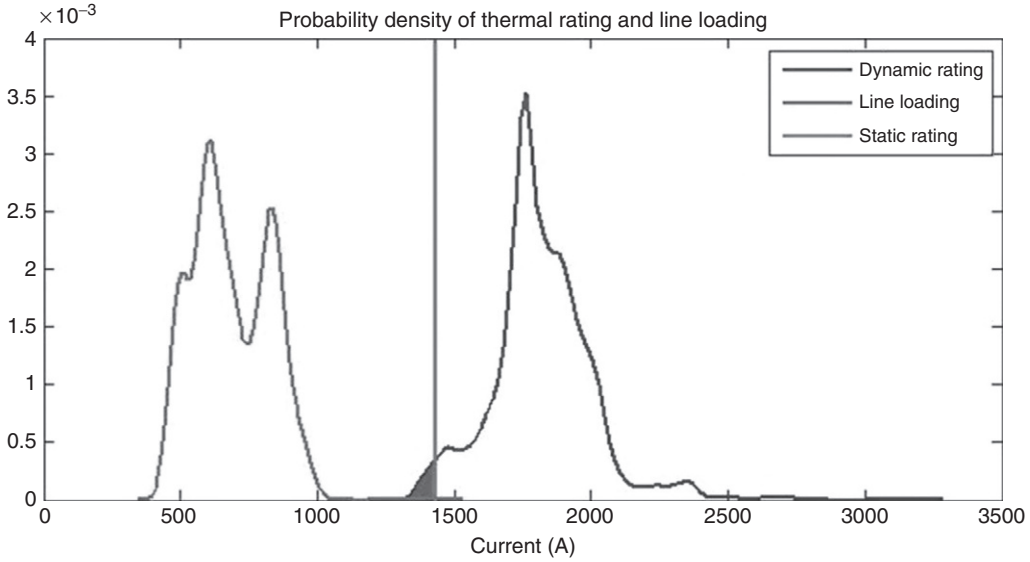


FIG. 26.18 Probability density plot of the dynamic thermal rating and line loading of a transmission line in Malaysia.

V_{L-G} = crest value of phase-to-ground overvoltage
V_m = maximum rms system voltage

This condition can be transient or permanent depending on its duration. Understanding overvoltage behavior including power-frequency phenomena and switching and lightning surges is important prerequisite condition in determining insulation coordination in a power system network.

The overvoltage phenomena are classified into four major classes [15]:

(a) Power-frequency overvoltages (also known as temporary overvoltages) that include Ferranti effect, self-excitation generator, overvoltage of unfaulted phases due to single-line-to-ground fault, and sudden load failure.
(b) Lower frequency harmonic resonant overvoltages that include lower order frequency resonance and local area resonant overvoltages.
(c) Switching surges that include breaker closing overvoltages, breaker tripping overvoltages, and switching surges by line switches
(d) Overvoltages by lightning strikes direct to phase conductors (direct flashover) and direct stroke to overhead shield wire or to tower structure (back flashover) or induced flashovers.
(e) Overvoltages due to abnormal conditions such as interrupted ground fault of cable, overvoltages induced on cable sheath, or touching of different kilovolts line.

In this chapter, the emphasis is given on overvoltages due to lightning strikes and switching surges and temporary overvoltages that have great impact in the selection of insulation requirements for transmission lines.

26.8.1 Overvoltage Phenomena by Lightning Strikes

By definition, lightning is an electric discharge. It is the high-current discharges of an electrostatic electricity accumulation between thundercloud and ground (cloud-to-ground discharges) or within the thundercloud (intracloud discharges). Other types of discharges such as cloud-to-cloud lightning and cloud-to-air lightning also exist but not very frequent. The thunderclouds contain ice crystals that are positively charged upper portion and water droplets that are negatively charged, usually located at lower portion of the thundercloud. The vertical circulation in terms of updrafts and downdrafts due to height and temperature effects caused disposition of charges in the thunderclouds (Fig. 26.19).

The mechanism of a lightning stroke is typically explained as follows. As the negative charges build up in the cloud base, positive charges are induced on the ground. When the voltage gradient within the cloud build up to the order of $5-10\text{kV/cm}$, the ionized air breaks down and creates an ionized path (leader) moving from thundercloud to ground. This initial leader progresses by series of jumps called a stepped leader. As this stepped leader (or downward leader) nears the ground, the upward leader (or return stroke) is initiated that meets the downward leader. This return stroke propagates upward from the ground to the thundercloud following the same path, at the speed of 10%–30% that of light, which is visible to the naked eye. The current involved may exceed 200 kA and lasting about 100 μs The second leader called dart leader may stroke following the same path taken by the first leader, about 40 μs later. The process of dart leader and return stroke can be repeated several times. The complete process of successive strokes are called lightning flash.

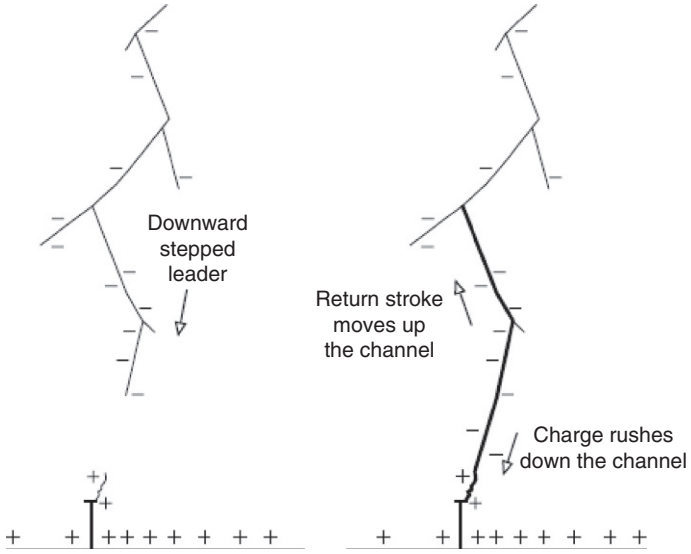


FIG. 26.19 Cloud-to-ground lightning.

Lightning surge phenomena can be classified into three different stroke modes: (a) direct strike on phase conductors (direct flashover), (b) direct strike on shield wire or tower structure, and (c) induced strokes.

In the case of direct strike, the lightning current path is directly from the thundercloud to the line. This will cause the voltage to rise at stroke termination point, on either one phase or more phase conductors. The stroke current propagates in the form of a traveling wave in both directions and raises potential of the line to the voltage of the downward leader. Overvoltage may exceed the line-to-ground withstand voltage of line insulation and cause insulation failure, if not properly protected.

In the case of direct strike on shield wire or tower structure, a lightning stroke directly strikes the shield wire or tower structure. If lightning strikes a tower top, some of the current may flow through the shield wires, and the remaining current flows through the tower to the earth. For stroke with average current magnitude and rate of rise, the current may flow into the ground provided the tower and its footing resistance are low. Otherwise, the lightning current will raise the tower to a high voltage above the ground, causing flashover from the tower over the line insulators to one or more phase conductors.

In induced strokes, lightning strokes terminate at some point on the Earth at a short distance from a transmission line. This can be considered as a virtual wire connected to a cloud and an earth point and a surge current $I(t)$ flowing along the virtual wire. This wire has mutual capacitances and mutual inductances across the line conductors and the shield wires of the neighborhood transmission lines. In this regard, the capacitive induced voltages and inductive induced voltage appear on the phase conductors and on the shield wires [15].

The insulation for lines is composed of air and solid dielectric insulators. The geometry of the insulators and their insulation strengths is selected to ensure that if an insulation failure occurs, the failure will be a flashover in air. This flashover produces a low-impedance path through which 50 Hz power current will flow. Generally, these arcs are not self-extinguishing. To interrupt the power fault, a protective device (circuit breaker) operating to de-energize the circuit will be required. Four types of lightning-caused flashover can occur on transmission lines: back flashover, shielding failure, induced, or midspan.

A back flashover event can occur when lightning strikes a grounded conductor or structure. In this case, a flashover proceeds backward from tower metal to the insulated conductor. A lightning stroke, terminating on an overhead ground wire or shield wire, produces waves of current and voltage that travel along the shield wire. At the tower/pole, these waves are reflected back toward the struck point and are transmitted down the tower/pole toward the ground and outward onto the adjacent shield wires. Riding along with these surge voltages are other surge voltages coupled onto the phase conductors. These waves continue to be transmitted and reflected at all points of impedance discontinuity. The surge voltages are built up at the tower/pole, across the phase-ground insulation, across the air insulation between phase conductors, and along the span across the air insulation from the shield wire to the phase conductor. If this surge voltage exceeds the insulation strength, flashover occurs. The parameters that affect the line back flashover rate (BFR) are the following:

- Ground flash density
- Surge impedances of the shield wires and tower/pole
- Coupling factors between conductors
- Power-frequency voltage

- Tower and line height
- Span length
- Insulation strength
- Footing resistance and soil composition

Sometimes, the design engineer can vary the shield wire surge impedance and the coupling factors, for example, using two shield wires instead of one. Normally, only insulation and footing impedance can be varied to improve back flashover performance. Reducing the footing impedance directly reduces the voltage stress across the insulator for a given surge current down the tower.

A shielding failure is defined as a lightning stroke that terminates on a phase conductor. For an unshielded line, all strokes to the line are shielding failures. For a transmission line with overhead shield wires, most of the lightning strokes that terminate on the line hit the shield wire and are not considered shielding failures.

The calculated number of shielding failures for a particular transmission line model depends on a number of factors, including the model's electrogeometric parameters, the stroke current distribution, and natural shielding from trees, terrain, or buildings. Not all shielding failures will result in insulator flashover. The critical current is defined as the lightning stroke current that, injected into the conductor, will result in flashover. The critical current for a particular transmission line conductor is calculated by

$$I_c = \frac{2^*(CFO)}{Z}$$

where CFO is the lightning impulse negative polarity critical flashover voltage and Z is the conductor surge impedance.

Severe transient overvoltage can be induced on overhead power lines by nearby lightning strikes. On lower voltage distribution power lines, indirect lightning strikes cause the majority of lightning-related flashovers. Estimation of indirect lightning effects is crucial for proper protection and insulation coordination of overhead lines. The problem of induced flashovers from nearby lightning strikes has received a great deal of scientific attention in the past 20 years, and the result has been the development of more accurate estimation models of lightning-induced overvoltages.

Important points to remember when dealing with induced flashovers from nearby lightning strokes include the following:

- Insulator CFO voltages above approximately 400 kV prevent nearly all induced flashovers.
- The presence of an effectively grounded overhead shield wire or neutral on the line will reduce insulator voltages by 30%–40%, depending on the line configuration.
- Line surge arresters installed every few spans can improve induced flashover performance for distribution voltage lines (spacing line arresters in this manner will seldom improve direct stroke lightning performance, only induced flashovers, and it is not recommended for transmission lines).

Power line flashovers caused by lightning strokes near midspan are unusual for most line configurations. Midspan flashovers become more likely when midspan conductor spacing is small, such as on-distribution lines, or when span lengths are very long (304.8 m or more). The voltage on a conductor follows the equation presented for a shielding failure. If the voltage rises to approximately 610 kV/m in the air gap between conductors, a long, relatively slow breakdown process might occur that might take many microseconds to complete.

26.8.2 Switching Surges

Switching surges can occur during the operation of circuit breaker and line switch opening (tripping) and closing at the same substation. In general, switching surges occur in the vicinity of non-self-restoring insulation equipment such as generators, transformers, breakers, and cables. Overvoltages caused by switching surges are a concern since they can damage insulation or cause insulation flashover. Damage and flashovers often lead to power system outage that is highly undesirable. The amplitude of a typical switching surge is about 1.5 pu with duration of about one power-frequency cycle [16].

26.8.3 Temporary Overvoltage

A temporary overvoltage is an oscillatory phase-to-ground overvoltage that is of relatively long duration and is undamped or only weakly damped. These types of overvoltages usually originate from faults, sudden changes of load, Ferranti effect, linear resonance, ferroresonance, open conductors, induced resonance from couple circuits, and others (e.g., backfeeding and stuck pole). In general, temporary overvoltage has two important characteristics: They are determinable, and they persist for many cycles. The magnitudes of these voltages may be calculated by steady-state analysis, assuming the physical conditions on the system are known.

26.9 Methods of Controlling Overvoltages

There are several means for controlling the overvoltages that occur on transmission system. Overvoltages due to switching surges can be controlled by modifying the operation of a circuit breaker or other switching device in various ways. The overvoltage may be limited to an acceptable level with the installation of surge arresters at the specific locations to be protected. The transmission system may be changed to minimize the effect of switching operations.

It is clear that if the source of the overvoltage is a random event such as lightning or fault initiation, the only sure method of controlling overvoltage will be the use of surge arresters or similar protective devices. In lightning protection

design, two aspects are important to consider: (i) diversion and shielding, mainly for structural protection that also provides reduction of electric and magnetic fields within the structure, and (ii) limiting the currents and voltages on electronic, power, and communication systems through surge protection. For the latter, the protection must include the control of currents and voltages from direct strikes to the structure and from lightning-induced current and voltage surges propagating into the structure from aerial or buried conductors from outside. Four general types of current- and voltage-limiting technique are commonly used [17] which are as follows:

(a) Voltage crowbar devices such as gas-tube arresters, silicon-controlled rectifiers (SCRs), and triacs that limit overvoltages to values smaller than operating voltages and short-circuit the current to ground.
(b) Voltage clamps such as metal oxide varistors (MOVs), Zener diodes, and p-n junction transistors. These solid-state nonlinear devices reflect and absorb energy while clamping the applied voltage across terminals to 30%–50% above the system operating voltage.
(c) Circuit filters that are linear circuits that both reflect and absorb the frequencies contained in the lightning transient pulses.
(d) Isolating devices such as optical isolators and isolation transformers suppress relatively large transients.

Reduction of basic impulse insulation levels of transmission equipment is possible with the use of surge arresters. Arresters are primarily used to protect the system insulation from the effects of lightning. Nowadays, modern arresters can also control many other system surges that may be caused by switching or faults. Arresters provide indispensable aid to insulation coordination in electric power system. It has basically a nonlinear resistor so that its resistance decreases rapidly as the voltage across it rises. At the surge ends and the voltage across the arrester returns to the normal line-to-neutral voltage level, the resistance becomes high enough to limit the arc current to a value that can be quenched by the series gap of the arrester.

Surge arresters may be used to control temporary overvoltages, such as due to a fault. It may be able to protect the equipment for the short time it takes to clear the applicable breakers. Similarly, surge arresters may be used to control switching surge overvoltages along a transmission line and thus reduce the length of required insulator strings. For example, the use of metal oxide arresters at the receiving end of a 280 km line can reduce the switching overvoltage along the line from a maximum of 2.2 to 1.8 pu.

26.10 Insulation Coordination

Insulation coordination is the selection of the insulation strength [18]. The strength is selected on the basis of some quantitative or perceived degree of reliability. It is also important to know the stress placed on the insulation and methods to reduce the stress, be it through surge arresters or other means. There are three different voltage stresses to consider when determining insulation and electric clearance requirements for the design of high-voltage transmission lines: (i) the power-frequency voltage, (ii) lightning surge, and (iii) switching surge. In general, lightning surges have the highest value and the highest rates of voltage rise. Properly done insulation coordination provides assurance that the insulation used will withstand all normal discharge and a majority of abnormal discharges. Several terms used in insulation coordination are defined as follows.

The basic lightning impulse insulation level (BIL) is defined as the electric strength of insulation expressed in terms of the crest value of the "standard lightning impulse" [18]. The BILs are universally for dry conditions. It is determined by tests made using impulses of a 1.2/50-μs waveshape. Several tests are performed, and a number of flashovers are noted.

The basic lightning impulse insulation level (BSL) is the electric strength of insulation expressed in terms of the crest value of a standard switching impulse. BSLs are universally for wet conditions.

Withstand voltage is the highest voltage that the insulation can withstand without failure or disruptive discharge, under specified test conditions. It is a common practice to assign a specific testing waveshape and duration of its application to each category of overvoltage.

There are two major categories of insulation: external insulation is the distances in open air or across the surfaces of solid insulation in contact with open air that is subjected to dielectric stress and to the effects of the atmosphere. Most transmission line insulation is external insulation. Internal insulation is the internal solid, liquid, or gaseous parts of the insulation of equipment that are protected by the equipment enclosures from the effects of the atmosphere such as in a transformer.

Insulation can also be divided into self-restoring and non-self-restoring categories. Self-restoring insulation completely recovers its insulating properties after a disruptive discharge. Non-self-restoring insulation loses insulation properties or does not recover completely after a disruptive discharge. Most external insulation, such as external air gap, is self-restoring insulation, and most internal insulation, such as solid insulation in a transformer, is non-self-restoring insulation. Insulation failure consequences are different for the different categories. Failure of non-self-restoring internal insulation is catastrophic, while failure of external self-restoring insulation may only be a nuisance. Testing may be done after a disruptive discharge for self-restoring internal insulation that provides statistical data for examination.

Insulation coordination involves the following processes: (i) determination of line insulation, (ii) selection of BIL and insulation levels of other equipment, and (iii) selection of lightning arresters. To assist this process, standard insulation levels

are recommended such as in IEC Publication 71.1 "Insulation Coordination Part 1, Definitions, Principles and Rules," 1993–12.

Knowledge of the overvoltages that the system will be exposed may be gained in two general ways: by measurement on the real system or by analysis on related models. Field measurement on a real system can only be done after the system is built. Analytic method can be used to determine the magnitude of overvoltages. The transient behavior of a complex transmission system must be studied through models either analog or digital. Transient network analyzer is an example on an analog model. For transmission lines below 345 kV, the line insulation is determined by lightning flashover rate. At 345 kV, the line insulation may be dictated either by switching surge or by lightning flashover rate. Above 345 kV, switching surges become a major factor in flashover considerations. The probability of flashover due to a switching surge is a function of the line characteristics and the magnitude of the surges expected. The number of insulators may be selected to keep the probability of flashovers due to switching surge very low.

In the design of substation, the maximum switching surge level used is either the maximum surge that can take place in the system or the protective level of arresters. In this case, the insulation coordination in a substation involves the selection of the minimum arrester rating applicable to withstand the power-frequency voltage and the equipment insulation level to be protected by arresters.

References

[1] World Electrical Power Generation, US Department of Energy, May 2009, EIA (Energy Information Agency).

[2] D.C. Lawry, Overhead line thermal rating calculation based on conductor replica method, 0-7803-81 10-6/03 IEEE, 2003.

[3] J. M. Hesterlee, Bare overhead transmission and distribution conductor desks overview, 0-7803-2043-3/95, IEEE, 1995.

[4] IEEE Standard, Standard for calculating the current-temperature relationship of bare overhead conductors, IEEE Std 738-2006, 2006.

[5] Cigre Working-group 22.12, The thermal behaviour of overhead conductors, Section 3: Mathematical model for evaluation of conductor temperature in the unsteady state, Electra No. 174, pp. 59–69, 1997.

[6] W.Z. Black, R.L. Rehberg, Simplified model for steady state and real time ampacity of overhead conductors, IEEE/PES Winter Meeting, Paper No. 88 WM 236–5, 1985.

[7] T.O. Seppa, Accurate ampacity determination: temperature - sag model for operational real time ratings, IEEE Trans. Power Del. 10 (3) (1995).

[8] R. Adapa, Increased power flow guidebook: Increasing power flow in transmission and substation circuits, Technical Report, EPRI, Palo Alto, CA, 2005.

[9] C. Mensah-Bonsu, U. Femindez, G.T. Heydt, Y. Hoverson, J. Schilleci, B. Agrawal, Application of the global positioning system to the measurement of overhead power transmission conductor sag, IEEE Trans. Power Del. 17 (1) (2002) 273–278.

[10] S.D. Foss, Evaluation of an overhead line forecast rating algorithm, IEEE Trans. Power Del. 7 (3) (1992).

[11] A.K. Pandey, Development of a real-time monitoring/dynamic rating system for overhead lines, Consultant Report, California Energy Commission, December 2003.

[12] Wikipedia website on Selective Availability. http://en.wikipedia.org/wiki/Global_Positioning_System#Selective_availability (accessed 02.02.09).

[13] A.A. Rahim, Pilot Implementation of Dynamic Thermal Rating Technology in TNB Transmission Line, TNB Research Sdn Bhd, Kuala Lumpur, Malaysia, 2008.

[14] EPRI, Transmission Line Reference Book: 345 kV and Above, second ed., Electric Power Research Institute, Palo Alto, CA, 1982.

[15] Y. Hase, Handbook of Power System Engineering, John Wiley & Sons Ltd, New York, 2007.

[16] Power Standards Lab, Transient Overvoltages: Tutorial, 2004.

[17] V.A. Rakov, M.A. Uman, Lightning Physics and Effect, Cambridge University Press, New York, 2003.

[18] IEC Publication 71.1, Insulation Coordination Part 1, Definitions, Principles and Rules, 1993–12.

27

HVDC Transmission

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Abbreviations

AEP	American Electric Power
ASVC	Advanced static var compensator
BB	Back to back
BC Hydro	British Columbia Hydro
BESS	Battery energy storage system
BPA	Bonneville Power Authority
CCC	Capacitor-commutated converter
CSCC	Controlled series capacitor-commutated converter
EMTP	Electromagnetic transient program
EPRI	Electric Power Research Institute
FACTS	Flexible AC transmission system
GTO	Gate turn off (thyristor)
HVDC	High-voltage direct current
IEE	Institute of Electrical Engineers
IEEE	Institute of Electrical and Electronic Engineers
IGBT	Insulated-gate bipolar transistor
IPC	Interphase power controller
LT	Load tap
MP	Minnesota Power
MSC	Mechanical switch controller
NSP	Northern States Power Co.
PLL	Phase-locked loop
PSS	Power system stabilizer
PWM	Pulse-width modulation
SMES	Superconducting magnetic energy storage

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SSR	Subsynchronous resonance
STATCON	Static condenser
STATCOM	Static compensator
SVC	Static var compensator
TCBR	Thyristor-controlled braking resistor
TCPAR	Thyristor-controlled phase-angle regulator
TCSC	Thyristor-controlled switched capacitor
TNA	Transient network analyzer
TSC	Thyristor-switched capacitor
TSR	Thyristor-switched reactor
TVA	Tennessee Valley Authority
UPFC	Unified power flow controller
VSI	Voltage-source inverter
WAPA	Western Area Power Authority

27.1 Introduction

High-voltage direct current (HVDC) transmission [1–3] is a major user of power electronics technology. HVDC technology first made its mark in the early undersea cable interconnections of Gotland (1954) and Sardinia (1967) and then in long-distance transmission with the Pacific Intertie (1970) and Nelson River (1973) schemes using mercury-arc valves. A significant milestone development occurred in 1972 with the first back-to-back (BB) asynchronous interconnection at Eel River between Quebec and New Brunswick; this installation also marked the introduction of thyristor valves to the technology and replaced the earlier mercury-arc valves.

Until 2005, a total of 70,000 MW HVDC transmission capacity is installed in some 95 projects all over the world. To understand the rapid growth of DC transmission (Table 27.1) [4] in the past 50 years, it is first necessary to compare it to conventional AC transmission.

27.1.1 Comparison of AC-DC Transmission

Making a planning selection between either AC or DC transmission is based on an evaluation of transmission costs, technical considerations, and reliability/availability offered by the two power transmission alternatives.

27.1.1.1 Evaluation of Transmission Costs

The cost of a transmission line comprises the capital investment required for the actual infrastructure (i.e., right of way (RoW), towers, conductors, insulators, and terminal equipment) and costs incurred for operational requirements (i.e., losses). Assuming similar insulation requirements for peak voltage levels for both AC and DC lines, a DC line can carry as much power with two conductors (having positive/negative polarities with respect to ground) as an AC line with three conductors of the same size. Therefore, for a given power level, a DC line requires a smaller RoW, simpler and cheaper towers, and reduced conductor and insulator costs. As an example, Fig. 27.1 shows the comparative case of AC and DC systems carrying 2000 MW.

With the DC option, since there are only two conductors (with the same current capacity of three AC conductors), the power transmission losses are also reduced to about two-thirds of the comparable AC system. The absence of skin effect with DC is also beneficial in reducing power losses marginally, and the dielectric losses in the case of power cables are also very much less for DC transmission.

Corona effects tend to be less significant on DC than for AC conductors. The other factors that influence line costs are the costs of compensation and terminal equipment. DC lines do not require reactive power compensation, but the terminal equipment costs are increased due to the presence of converters and filters.

Fig. 27.2 shows the variation of infrastructure costs with distance for AC and DC transmission. AC tends to be more economical than DC for distances less than the "break-even distance" but is more expensive for longer distances. This is due to a combination of the terminal equipment costs and line costs for the two types of transmission. The break-even distances can vary from about 500 to 800 km in overhead lines depending on the per unit line costs. With a cable system, this break-even distance approaches 50 km.

27.1.1.2 Evaluation of Technical Considerations

Due to its fast controllability, a DC transmission system has full control over transmitted power, an ability to enhance transient and dynamic stability in associated AC networks and can limit fault currents in the DC lines. Furthermore, DC transmission overcomes some of the following problems associated with AC transmission:

- Stability limits

  The power transfer in an AC line is dependent on the angular difference between the voltage phasors at the two line ends. For a given power transfer level, this angle increases with distance. The maximum power transfer is limited by the considerations of steady state and transient stability. The power-carrying capability of an AC line is inversely proportional to transmission distance, whereas the power-carrying ability of DC lines is unaffected by the distance of transmission.
- Voltage control

  Voltage control in AC lines is complicated by line-charging requirements and voltage drops. The voltage profile in an AC line is relatively flat only for a fixed level of power transfer, corresponding to its surge impedance loading (SIL). The voltage profile varies with the line loading. For constant voltage at the line ends, the midpoint voltage is reduced for line loadings higher than SIL and increased for loadings less than SIL.

  The maintenance of constant voltage at the two ends requires reactive power control as the line loading is

TABLE 27.1 Listing of HVDC installations

HVDC link	Supplier	Year	Power MW	DC Voltage kV	Length km	Location
Gotland I[a]	A	1954	20	±100	96	Sweden
English Channel	A	1961	160	±100	64	England-France
Volgograd-Donbass[b]		1965	720	±400	470	Russia
Inter-Island	A	1965	600	±250	609	New Zealand
Konti-Skan I	A	1965	250	250	180	Denmark-Sweden
Sakuma	A	1965	300	2 × 125	B-B[c]	Japan
Sardinia	I	1967	200	200	413	Italy
Vancouver I	A	1968	312	260	69	Canada
Pacific Intertie	JV	1970	1440	±400	1362	The United States
Pacific Intertie		1982	1600			
Nelson River I[d]	I	1972	1620	±450	892	Canada
Kingsnorth	I	1975	640	±260	82	England
Gotland	A	1970	30	±150	96	Sweden
Eel River	C	1972	320	2 × 80	B-B	Canada
Skagerrak I	A	1976	250	250	240	Norway-Denmark
Skagerrak II	A	1977	500	±250		Norway-Denmark
Skagerrak III	A	1993	440	350	240	Norway-Denmark
Vancouver II	C	1977	370	−280	77	Canada
Shin Shinano	D	1977	300	2 × 125	B-B	Japan
Shin Shinano		1992	600	3 × 125	B-B	Japan
Square Butte	C	1977	500	±250	749	The United States
David A. Hamil	C	1977	100	50	B-B	The United States
Cahora Bassa	J	1978	1920	±533	1360	Mozambique-S. Africa
Nelson River II	J	1978	900	±250	930	Canada
Nelson River II	J	1985	1800	±500	930	Canada
CU Project	A	1979	1000	±400	710	The United States
Hokkaido-Honshu	E	1979	150	125	168	Japan
		1980	300	250		
		1993	600	±250		
Acaray	G	1981	50	25.6	B-B	Paraguay
Vyborg	F	1981	355	1 × 170(±85)	B-B	Russia (tie with Finland)
Vyborg	F	1982	710	2 × 170		
Vyborg	F		1065	3 × 170		
Duernrohr	J	1983	550	145	B-B	Austria
Gotland II	A	1983	130	150	100	Sweden
Gotland III	A	1987	260	±150	103	Sweden
Eddy County	C	1983	200	82	B-B	The United States
Châteauguay	J	1984	1000	2 × 140	B-B	Canada
Oklaunion	C	1984	200	82	B-B	The United States
Itaipu	A	1984	1575	±300	785	Brazil
Itaipu	A	1985	2383	785	Brazil	
Itaipu	A	1986	3150	±600	785	Brazil
Inga-Shaba	A	1982	560	±500	1700	DR Congo
Pacific Intertie upgrade	A	1984	2000	±500	1362	The United States
Blackwater	B	1985	200	57	B-B	The United States
Highgate	A	1985	200	±56	B-B	The Unite States
Madawaska	C	1985	350	140	B-B	Canada
Miles City	C	1985	200	±82	B-B	The United States
Broken Hill	A	1986	40	2 × 17(±8.33)	B-B	Australia
Intermountain Power Project	A	1986	1920	±500	784	The United States
Cross-Channel:	H	1986	1000	±270	72	France-England
Les Mandarins (Sellindge)	I	1986	2000	2 × ±270		France England
Des Cantons-Comerford	C	1986	690	±450	172	Canada-the United States
Sacoi[e]	H	1986	200	200	415	Corsica Island
Sacoi[f]	H	1992	300			Italy
Itaipu II	A	1987	3150	±600	805	Brazil
Sidney (Virginia Smith)	G	1988	200	55.5	B-B	The United States
Gezhouba-Shanghai	B + G	1989	600	500	1000	China
		1990	1200	±500		

Continued

TABLE 27.1 Listing of HVDC installations—cont'd

HVDC link	Supplier	Year	Power MW	DC Voltage kV	Length km	Location
Konti-Skan II	A	1988	300	285	150	Sweden-Denmark
Vindhyachal	A	1989	500	2 × 69.7	B-B	India
Pacific Intertie Exp.	B	1989	1100	±500	1362	The United States
McNeill	I	1989	150	42	B-B	Canada
Fenno-Skan	A	1989	500	400	200	Finland-Sweden
Sileru-Barsoor	K	1989	100	+100	196	India
			200	+200		
			400	±200		
Rihand-Delhi	A	1991	1500	±500	India	
Quebec-New England	A	1990	2000[g]	±450	1500	Canada-the United States
Nicolet Tap	A	1992	1800			Canada
DC Hybrid Link	AB	1992	992	+270/−350	617	New Zealand
Etzenricht	G	1993	600	160	B-B	Germany (tie with Czech)
Vienna Southeast	G	1993	600	145	B-B	Austria (tie with Hungary)
Haenam-Cheju	I	1993	300	±180	100	South Korea
Baltic Cable Project	AB	1994	600	450		Sweden-Germany
Welch-Monticello		1995	600		B-B	The United States
Kontek Interconnection		1995	600	400	170	Denmark-Germany
Scotland-N. Ireland		1996	250	250		The United Kingdom
Chandrapur-Ramagundum		1996	1000	2 × 500	B-B	India
Chandrapur-Padghe	AB	1997	1500	±500	900	India
Greece-Italy	AB	1997	500	400	200, sea	Italy
Gajuwaka-Jeypore	AB	1997	500		B-B	India
Leyte-Luzon	AB	1997	1600	400	440	Philippines
Cahora Bassa	G	1998	1920	±533	1456	Mozambique-S. Africa
TSQ-Beijao	G	2000	1800	±500	903	China
Thailand-Malaysia	G	2001	300	±300	B-B	Thailand-Malaysia
Moyle	G	2001	2 × 250	250	64	Ireland-Scotland
East-South Intercon.	G	2003	2000	±500	1450	India
Rapid City DC tie	AB	2003	2 × 100	±13	B-B	S. Dakota, the United States
Three Gorges-Changzhou	AB	2003	3000	±500	890	China
Three Gorges-Guangdong	AB	2004	3000	±500	940	China
Guizhou-Guangdong	G	2004	3000	±500	940	China
Celilo conv. station	AB	2004	2000	±500	Upgrade	The United States
Nelson River Bipole II	G	2004	1000	450	Pole 1	Canada
Basslink	G	2005	500	400	350	Australia-Tasmania
Lamar	G	2005	210	63.6	B-B	Colorado, the United States
Vizag II	AB	2005	500	±88	B-B	India
Estlink	AB	2006	350	±150	HVDC Light	Estonia-Finland
Three Gorges-Shanghai	AB	2007	3000	±500	1059	China
NorNed	AB	2007	700	±450	560	Norway-Netherlands
Valhall offshore	AB	2009	950		HVDC Light	Norway
Yunnan-Guangdong	G	2009	5000	±800	1418	China
Outaouais	AB	2009	1250	175	B-B	Canada
Blackwater	AB	2009	200	57	B-B	The United States
Ballia-Bhiwadi	G	2010	2500	±500	800	India
Storebælt	G	2010	600	400	56	Denmark
Trans Bay Cable project	G	2010	400	±200	85	The United States
Hulunbeir-Liaoning	AB	2010	3000	±500	920	China
Xiangjiaba-Shanghai	G	2010	6400	±800	2070	China
Caprivi Link	AB	2010	300	350	950	Namibia
Intermountain Power	AB	2010	2400	±500	785	The United States
Lingbao II	AB	2010	750	168	B-B	Chain
BritNed, Great Britain	G	2011	1000	±450	260	Netherlands
SAPEI	AB	2011	1000	±500	2 × 450	Italy-Sardinia
Fenno-Skan	AB	2011	500	400	200	Finland-Sweden
Valhall	AB	2011	78	150	292	Norway
COMETA	G	2012	2 × 200	±200	250	Spain
Jinping-Sunan	G	2012	7200	±800	2059	China
Mundra-Haryana	G	2012	2500	±500	960	India

TABLE 27.1 Listing of HVDC installations—cont'd

HVDC link	Supplier	Year	Power MW	DC Voltage kV	Length km	Location
Highgate	AB	2012	200	57	B-B	Canada
Back to back	G	2013	500	158	B-B	Bangladesh
Porto Velho	AB	2013	2 × 400	?	B-B	Brazil
Black Sea Transmission	G	2013	2 × 350	96	B-B	Georgia
Hudson Transmission	G	2013	660	180	B-B	The United States
East-West Interconnector	AB	2013	500	±200	2 × 75	The United Kingdom-Ireland
Jinping-Sunan	AB	2013	7200	±800	2090	China
Nuozhadu-Guangdong	G	2013	5000	±800	1451	China
Rio Madeira	AB	2013	2 × 400	±600	B-B	Brazil
Xiluodu-Guangdong	G	2013	6400	±500	1286	China
INELFE	G	2014	2 × 1000	±320	65	France-Spain
Mackinac	AB	2014	200	±71	B-B	The United States
Inga-Kolwezi	AB	2014	560	±500	1700	Congo
Skagerrak	AB	2014	700	500	140	Norway-Denmark
Eel River	AB	2014	350	80	B-B	Canada
EstLink 2	G	2014	670	450	171	Finland-Estonia
Railroad DC Tie	AB	2014	300	±21	B-B	Mexico
Oklaunion	AB	2014	220	±31	B-B	The United States
Inter-Island Connector Pole 3	G	2014	700	±350	649	New Zealand
Western HVDC Link	G	2015	2200	±600	420	The United Kingdom
Troll A 3&4	AB	2015	100	±60	70	Norway
DolWin1	AB	2015	800	±320	2 × 75	Germany
ÅL-link	AB	2015	100	±80	158	Finland
BorWin1	AB	2015	400	±150	2 × 75	Germany
LitPol Link	AB	2015	500	±60	B-B	Poland-South Lithuania
Madawaska	AB	2016	350	130	B-B	Canada
Pacific Intertie	AB	2016	1440	±400	1360	The United States
NordBalt	AB	2016	700	±320	400	Sweden-Lithuania
DolWin2	AB	2016	916	±320	2 × 45	Germany (North Sea)
North-East Agra	AB	2016	6000	±800	1728	India
Québec-New England	AB	2016	2000	±450	1480	Canada-the United States

A, ASEA; *B*, Brown Boveri; *C*, General Electric; *D*, Toshiba; *E*, Hitachi; *F*, Russian; *G*, Siemens; *H*, CGEE Alstom; *I*, GEC (formerly English Electric); *J*, HVDC W.G. (AEG, BBC, and Siemens); *K*, (Independent); *AB*, ASEA Brown Boveri (ABB); *JV*, Joint Venture (GE and ASEA).
[a]Retired from service.
[b]Two VGs replaced with thyristors in 1977.
[c]Back-to-back HVDC system.
[d]Two VGs in pole 1 replaced with thyristors by GEC in 1991.
[e]50 MW thyristor tap.
[f]Uprated with thyristor valves.
[g]Multiterminal system. Largest terminal is rated 2250 MW.

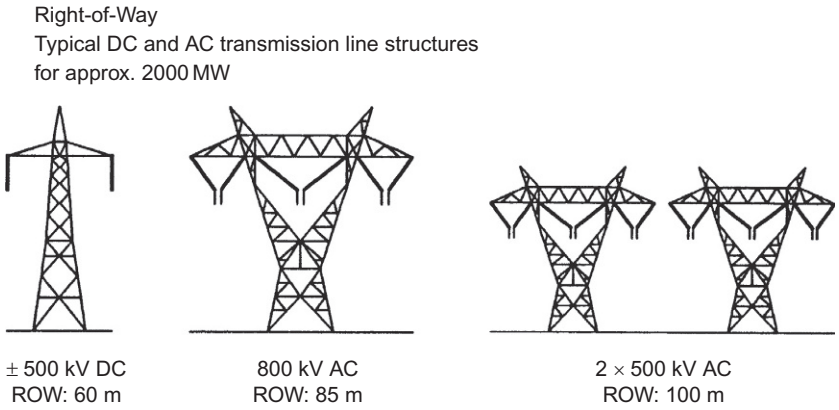


FIG. 27.1 Comparison of RoW for AC and DC transmission systems.

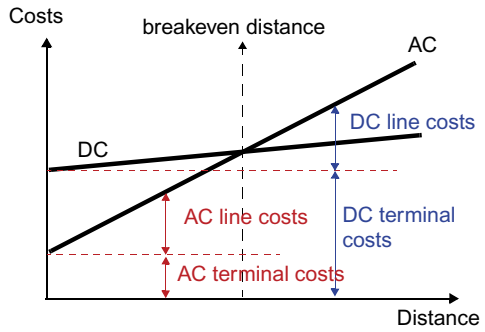


FIG. 27.2 Comparison of AC-DC transmission system costs.

increased. The reactive power requirements increase with line length.

Although DC converter stations require reactive power related to the power transmitted, the DC line itself does not require any reactive power.

The steady-state charging currents in AC cables pose serious problems and make the break-even distance for cable transmission around 50 km.

- Line compensation

  Line compensation is necessary for long-distance AC transmission to overcome the problems of line charging and stability limitations. The increase in power transfer and voltage control is possible through the use of shunt inductors, series capacitors, static var compensators (SVCs), and, lately, the new-generation static compensators (STATCOMs).

  In the case of DC lines, such compensation is not needed.

- Problems of AC interconnection

  The interconnection of two power systems through AC ties requires the automatic generation controllers of both systems to be coordinated using tie line power and frequency signals. Even with coordinated control of interconnected systems, the operation of AC ties can be problematic due to (i) the presence of large power oscillations that can lead to frequent tripping, (ii) increase in fault level, and (iii) transmission of disturbances from one system to the other.

  The fast controllability of power flow in DC lines eliminates all of the above problems. Furthermore, the asynchronous interconnection of two power systems can only be achieved with the use of DC links.

- Ground impedance

  In AC transmission, the existence of ground (zero sequence) current cannot be permitted in steady state due to the high magnitude of ground impedance that will not only affect efficient power transfer but also result in telephonic interference.

  The ground impedance is negligible for DC currents, and a DC link can operate using one conductor with ground return (monopolar operation). The ground return is objectionable only when buried metallic structures (such as pipelines) are present and are subject to corrosion with DC current flow. It is to be noted that even while operating in the monopolar mode, the AC network feeding the DC converter station operates with balanced voltages and currents. Hence, single-pole operation of DC transmission systems is possible for extended periods, while in AC transmission, single-phase operation or any unbalanced operation is not feasible for more than a second.

- Problems of DC transmission

  The application of DC transmission is limited by factors such as

  (1) high cost of conversion equipment,
  (2) inability to use transformers to alter voltage levels,
  (3) generation of harmonics,
  (4) requirement of reactive power,
  (5) complexity of controls.

  Over the years, there have been significant advances in DC technology, which have tried to overcome the disadvantages listed above, except for item (2). These are the following:

  (1) Increase in the ratings of a thyristor cell that makes up a valve
  (2) Modular construction of thyristor valves
  (3) Twelve-pulse operation of converters
  (4) Use of forced commutation
  (5) Application of digital electronics and fiber optics in the control of converters.

  Some of the above advances have resulted in improving the reliability and reduction of conversion costs in DC systems.

27.1.2 Evaluation of Reliability and Availability Costs

Statistics on the reliability of HVDC links are maintained by CIGRE and IEEE working groups. The reliability of DC links has been very good and is comparable with AC systems. The availability of DC links is quoted in the upper 90%.

27.1.3 Applications of DC Transmission

Due to their costs and special nature, most applications of DC transmission generally fall into one of the following four categories:

- Underground or underwater cables

  In the case of long cable connections over the break-even distance of about 40–50 km, DC cable transmission system has a marked advantage over AC cable connections. Examples of this type of applications were the Gotland (1954) and Sardinia (1967) schemes.

  The recent development of voltage-source converters (VSC) and the use of rugged polymer DC cables, with

the so-called "HVDC Light" option, are being increasingly considered. An example of this type of application is the 180-MW Directlink connection (2000) in Australia.

- Long-distance bulk power transmission

  Bulk power transmission over long distances is an application ideally suited for DC transmission and is more economical than AC transmission whenever the break-even distance is exceeded. Examples of this type of application abound from the earlier Pacific Intertie to the recent links in China and India.

  The break-even distance is being effectively decreased with the reduced costs of new compact converter stations possible due to the recent advances in power electronics (discussed in a later section).
- Asynchronous interconnection of AC systems

  In terms of an asynchronous interconnection between two AC systems, the DC option reigns supreme. There are many instances of BB connections where two AC networks have been tied together for the overall advantage to both AC systems. With recent advances in control techniques, these interconnections are being increasingly made at weak AC systems. The growth of BB interconnections is best illustrated with the example of N. America where the four main independent power systems are interconnected with 12 BB links.

  In the future, it is anticipated that this BB connection will also be made with VSCs offering the possibility of full four-quadrant operation and the total control of active/reactive power coupled with the minimal generation of harmonics.
- Stabilization of power flows in integrated power system

  In large interconnected systems, power flow in AC ties (particularly under disturbance conditions) can be uncontrolled and lead to overloading and stability problems, thus endangering system security. Strategically placed DC lines can overcome this problem due to the fast controllability of DC power and provide much needed damping and timely overload capability. The planning of DC transmission in such applications requires detailed study to evaluate the benefits. Examples are the IPP link in the United States and the Chandrapur-Padghe link in India.

Presently, the number of DC lines in a power grid is very small compared with the number of AC lines. This indicates that DC transmission is justified only for specific applications. Although advances in technology and introduction of multi-terminal DC (MTDC) systems are expected to increase the scope of application of DC transmission, it is not anticipated that the AC grid will be replaced by a DC power grid in the future. There are two major reasons for this. First, the control and protection of MTDC systems is complex, and the inability of voltage transformation in DC networks imposes economic penalties. Second, the advances in power electronics technology have resulted in the improvement of the performance of AC transmissions using FACTS devices, for instance, through introduction of static var systems, static phase shifters, etc.

27.1.4 Types of HVDC Systems

Three types of DC links are considered.

27.1.4.1 Monopolar Link

A monopolar link (Fig. 27.3A) has one conductor and uses either ground or sea return. A metallic return can also be used where concerns for harmonic interference and/or corrosion exist. In applications with DC cables (i.e., HVDC Light), a cable return is used. Since the corona effects in a DC line are substantially less with negative polarity of the conductor as compared with the positive polarity, a monopolar link is normally operated with negative polarity.

27.1.4.2 Bipolar Link

A bipolar link (Fig. 27.3B) has two conductors, one positive and the other with negative polarity. Each terminal has two sets of converters of equal rating, in series on the DC side. The junction between the two sets of converters is grounded at one or both ends by the use of a short electrode line. Since both poles operate with equal currents under normal operation, there is zero-ground current flowing under these conditions. Monopolar operation can also be used in the early stages of the development of a bipolar link. Alternatively, under faulty converter conditions, one DC line may be temporarily used as a metallic return with the use of suitable switching.

27.1.4.3 Homopolar Link

In this type of link (Fig. 27.3C), two conductors having the same polarity (usually negative) can be operated with ground or metallic return.

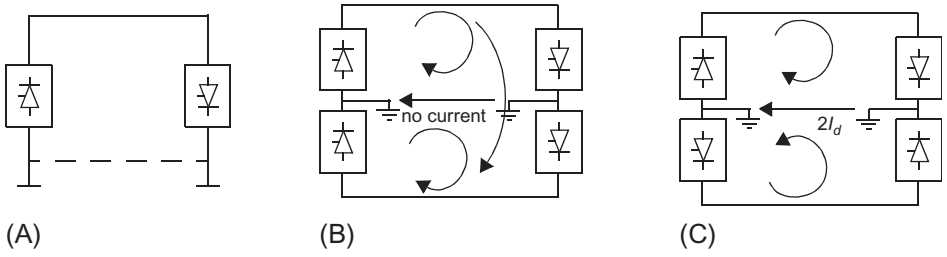


FIG. 27.3 Types of HVDC links: (A) monopolar link, (B) bipolar link, and (C) homopolar DC link.

Due to the undesirability of operating a DC link with ground return, bipolar links are mostly used. A homopolar link has the advantage of reduced insulation costs, but the disadvantages of earth return outweigh the advantages.

27.2 Main Components of HVDC Converter Station

The major components of an HVDC transmission system are the converter stations at the ends of the transmission system. In a typical two-terminal transmission system, both a rectifier and an inverter are required. The role of the two stations can be reversed as controls are usually available for both functions at the terminals. The major components of a typical 12-pulse bipolar HVDC converter station (Fig. 27.4) are discussed below.

27.2.1 Converter Unit

This usually consists of two three-phase converter bridges connected in series to form a 12-pulse converter unit. The design of valves is based on a modular concept where each module contains a limited number of series-connected thyristor levels. The valves can be packaged as either a single-valve, double-valve, or quadruple-valve arrangement. The converter is fed by converter transformers connected in star/star and star/delta arrangements to form a 12-pulse pair.

The valves may be cooled by air, oil, water, or Freon. However, the cooling using deionized water is more modern and considered efficient and reliable. The ratings of a valve group are limited more by the permissible short-circuit currents than by the steady-state load requirements.

Valve firing signals are generated in the converter control at ground potential and are transmitted to each thyristor in the valve through a fiber-optic light guide system. The light signal received at the thyristor level is converted to an electric signal using gate drive amplifiers with pulse transformers. Recent trends in the industry indicate that direct optical firing of the valves with LTT thyristors is also feasible.

The valves are protected using snubber circuits, protective firing, and gapless surge arrestors.

27.2.1.1 Thyristor Valves

Many individual thyristors are connected in series to build up an HVDC valve. To distribute the off-state valve voltage uniformly across each thyristor level and protect the valve from di/dt and dv/dt stresses, special snubber circuits are used across each thyristor level (Fig. 27.5).

The snubber circuit is composed of the following components:

- A saturating reactor is used to protect the valve from *di*/*dt* stresses during turn-on. The saturating reactor offers a high inductance at low current and a low inductance at high currents.
- A DC grading resistor R_G distributes the direct voltage across the different thyristor levels. It is also used as a voltage divider to measure the thyristor level voltage.
- RC snubber circuits are used to damp out voltage oscillations from power frequency to a few kHz.
- A capacitive grading circuit C_{FG} is used to protect the thyristor level from voltage oscillations at a much higher frequency.

A thyristor is triggered on by a firing pulse sent via a fiber-optic cable from the valve base electronics (VBE) unit at earth potential. The fiber-optic signal is amplified by a gate electronic unit (GEU) that receives its power from the RC snubber circuit during the valve's off period.

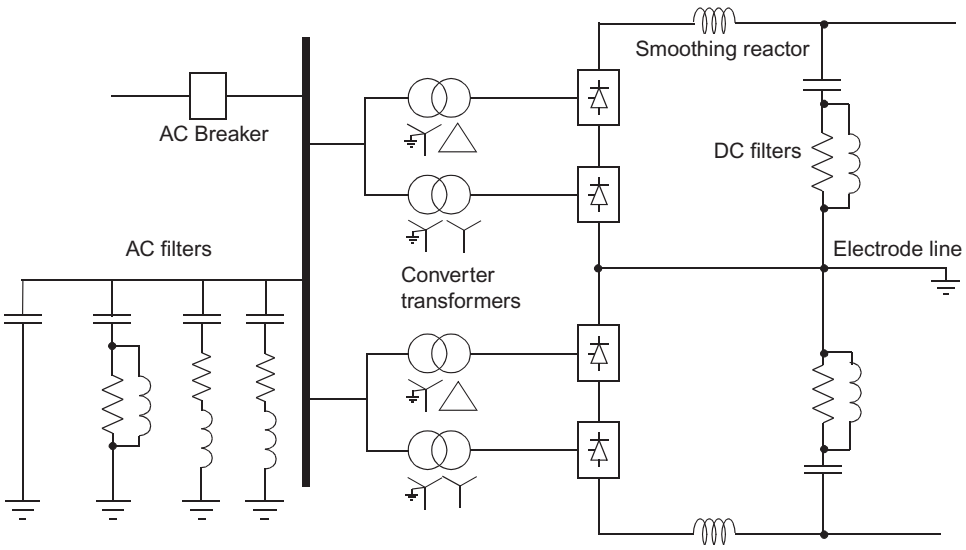


FIG. 27.4 Typical HVDC converter station equipment.

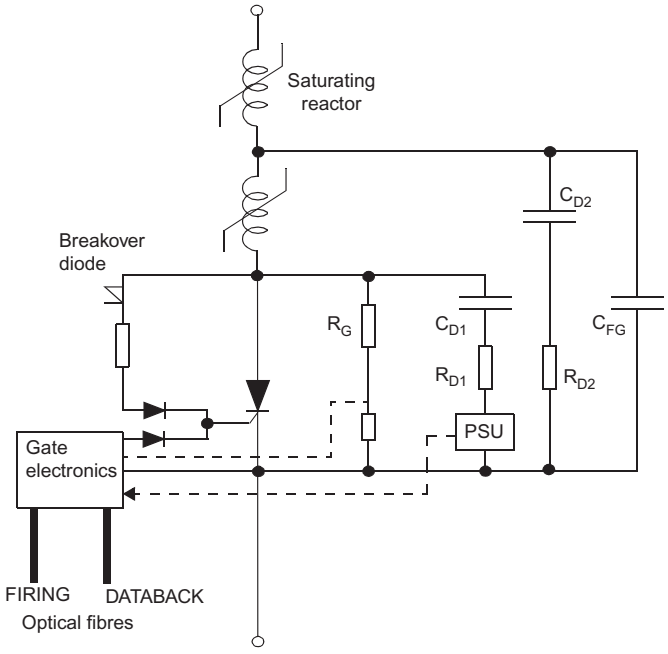


FIG. 27.5 Electric circuit of the thyristor level [2].

The GEU can also effect the protective firing of the thyristor independent of the central control unit. This is achieved by a breakover diode (BOD) via a current-limiting resistor that triggers the thyristor when the forward voltage threatens to exceed the rated voltage for the thyristor. This may arise in a case when some thyristors may block forward voltage, while others may not.

It is normal to include some extra redundant thyristor levels to allow the valve to remain in service after the failure of some thyristors. A metal oxide surge arrestor is also used across each valve for overvoltage protection.

The thyristors produce considerable heat loss, typically 24–40 W/cm^2 (or over 1 MW for a typical quadruple valve), and so, an efficient cooling system is essential.

27.2.2 Converter Transformer

The converter transformer (Fig. 27.6) can have different configurations: (i) three phase, two winding; (ii) single phase, three winding; and (iii) single phase, two winding. The valve-side windings are connected in star and delta with neutral point ungrounded. On the AC side, the transformers are connected in parallel with the neutral grounded. The leakage impedance of the transformer (typical value between 15% and 18%) is chosen to limit the short-circuit currents through any valve.

The converter transformers are designed to withstand DC voltage stresses and increased eddy current losses due to harmonic currents. One problem that can arise is due to the DC magnetization of the core due to unsymmetrical firing of valves.

27.2.3 Filters

Due to the generation of characteristic and noncharacteristic harmonics by the converter, it is necessary to provide suitable filters on the AC-DC sides of the converter to improve the

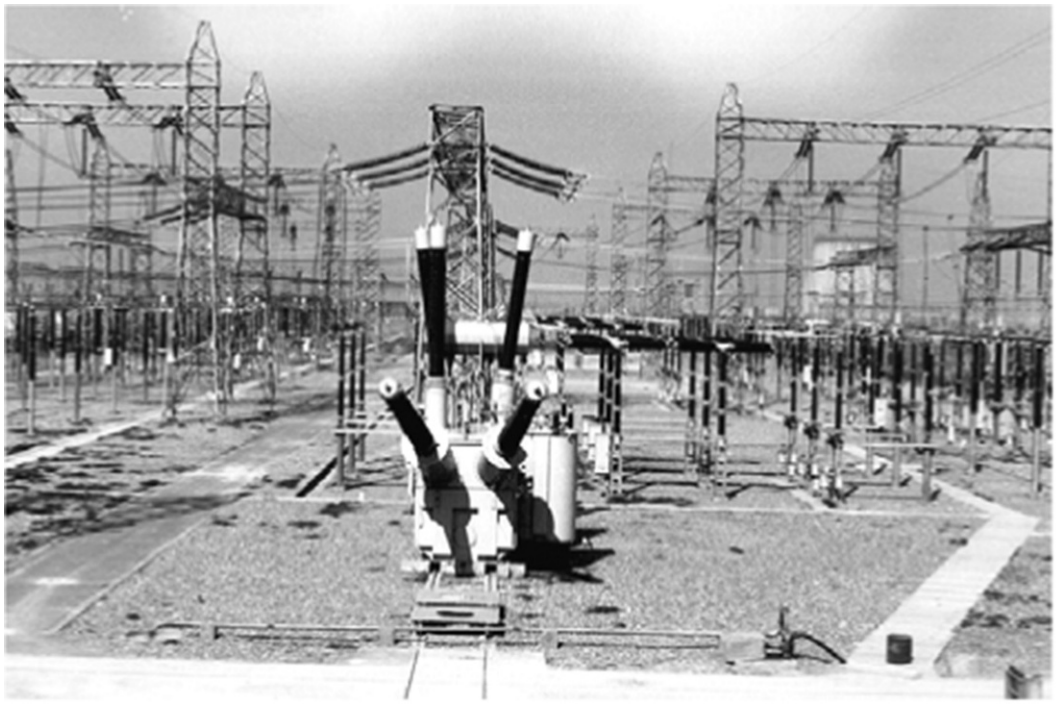


FIG. 27.6 Spare converter for multilevel convertertransformer in the switchyard of an HVDC station.

power quality and meet telephonic and other requirements. Generally, three types of filters are used for this purpose:

27.2.3.1 AC Filters

AC filters (Fig. 27.7) are passive circuits used to provide low impedance, shunt paths for AC harmonic currents. Both tuned and damped filter arrangements are used. In a typical 12-pulse station, filters at eleventh and thirteenth harmonics are required as tuned filters. Damped filters (normally tuned to the twenty-third harmonic) are required for the higher harmonics. In recent years, C-type filters have also been used since they provide more economic designs. Double- or even triple-tuned filters exist to reduce the cost of the filter (see application example system).

The availability of cost-effective active AC filters will change the scenario in the future.

27.2.3.2 DC Filters

These are similar to AC filters and are used for the filtering of DC harmonics. Usually, a damped filter at the twenty-fourth harmonic is utilized. Modern practice is to use active DC filters (see also the application example system presented later). Active DC filters are increasingly being used for efficiency and space-saving purposes.

27.2.3.3 High Frequency (RF/PLC) Filters

These are connected between the converter transformer and the station AC bus to suppress any high-frequency currents. Sometimes, such filters are provided on the high-voltage DC bus connected between the DC filter and DC line and also on the neutral side.

27.2.4 Reactive Power Source

Converter stations consume reactive power that is dependent on the active power loading (typically about 50%–60% of the active power). Part of this reactive power requirement is provided by the AC filters. In addition, shunt (switched) capacitors and static var systems are also used.

27.2.5 DC Smoothing Reactor

A sufficiently large series reactor is used on the DC side of the converter to smooth the DC current and for the converter protection from line surges. The reactor (Fig. 27.8) is usually



FIG. 27.7 Installation of an AC filter in the switchyard.

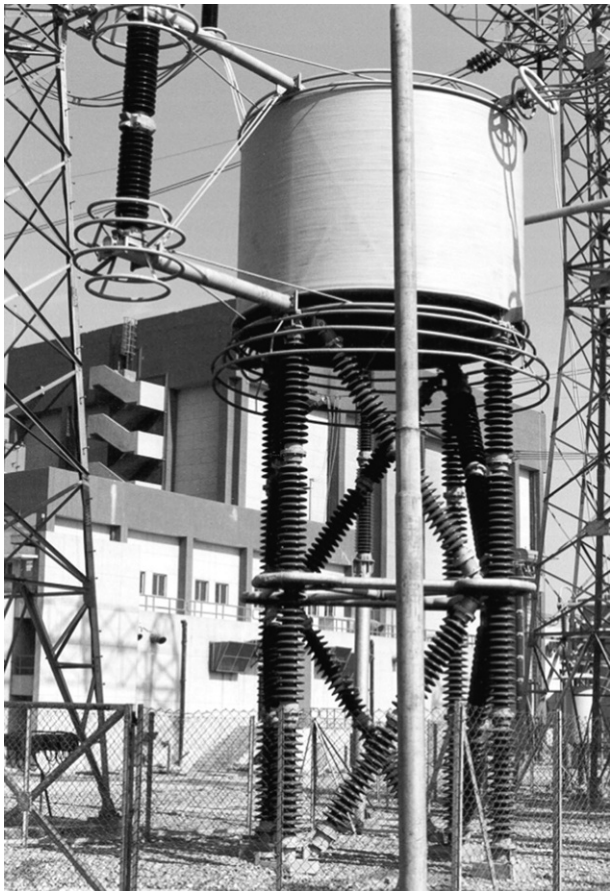


FIG. 27.8 Installation of an air-cooled smoothing reactor.

designed as a linear reactor and may be connected on the line side, on the neutral side, or at an intermediate location. Typical values of the smoothing reactor are in the 240–600 mH range for long-distance transmission and about 24 mH for a BB connection.

27.2.6 DC Switchgear

This is usually modified AC equipment and used to interrupt only small DC currents (i.e., employed as disconnecting switches). DC breakers or metallic return transfer breakers (MRTB) are used, if required, for the interruption of rated load currents.

In addition to the equipment described above, AC switchgear and associated equipment for protection and measurement are also part of the converter station.

27.2.7 DC Cables

Contrary to the use of AC cables for transmission, DC cables do not have a requirement for continuous charging current. Hence, the length limit of about 50 km does not apply. Moreover, DC voltage gives less aging and hence a longer lifetime for the cable. The new design of HVDC Light cables from ABB is based on extruded polymeric insulating material instead of classic paper-oil insulation that has a tendency to leak. Due to their rugged mechanical design, flexibility, and low weight, polymer cables can be installed underground cheaply with a plowing technique or, in submarine applications, can be laid in very deep waters and on rough sea bottoms. Since DC cables are operated in bipolar mode, one cable with positive polarity and one cable with negative polarity, very limited magnetic fields result from the transmission. HVDC Light cables have successfully achieved operation at a stress of 20 kV/mm.

27.3 Analysis of Converter Bridge

To consider the theoretical analysis of a conventional six-pulse bridge (Fig. 27.9), the following assumptions are made:

- DC current I_d is considered constant.
- Valves are ideal switches.
- AC system is strong (infinite).

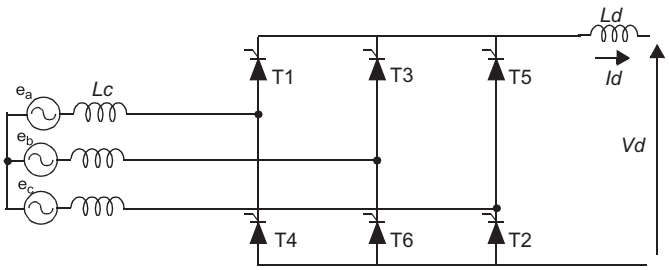


FIG. 27.9 Six-pulse bridge circuit.

Due to the leakage impedance of the converter transformer, commutation from one valve to the next is not instantaneous. An overlap period is necessary, and depending on the leakage, either two, three, or four valves may conduct at any time. In the general case, with a typical value of converter transformer leakage impedance of about 13%–18%, either two or three valves conduct at any one time.

The analysis of the bridge gives the following DC output voltages:

For a rectifier:

$$V_{dr} = V_{dor} \cdot \cos\alpha - R_{cr} \cdot I_d \tag{27.1}$$

where $V_{dor} = \frac{3}{\pi} \cdot \sqrt{2} \cdot V_{LL}$ and $R_{cr} = \frac{3}{\pi} \cdot wL_{cr}$.

For an inverter:

There are two options possible depending on choice of the delay angle or extinction angle as the control variable:

$$-V_{di} = V_{doi} \cdot \cos\beta + R_{ci} \cdot I_d \tag{27.2}$$

$$-V_{di} = V_{doi} \cdot \cos\gamma - R_{ci} \cdot I_d \tag{27.3}$$

where

V_{dr} and V_{di}—DC voltage at the rectifier and inverter, respectively
V_{dor} and V_{doi}—open-circuit DC voltage at the rectifier and inverter, respectively
R_{cr} and R_{ci}—equivalent commutation resistance at the rectifier and inverter, respectively
L_{cr} and L_{ci}—leakage inductance of converter transformer at rectifier and inverter, respectively
I_d—DC current
α—delay angle
β—advance angle at the inverter ($\beta = \pi - \alpha$)
γ—extinction angle at the inverter ($\gamma = \pi - \alpha - \mu$)

27.4 Controls and Protection

In a typical two-terminal DC link connecting two AC systems (Fig. 27.10), the primary functions of the DC controls are to

- control power flow between the terminals,
- protect the equipment against the current/voltage stresses caused by faults,

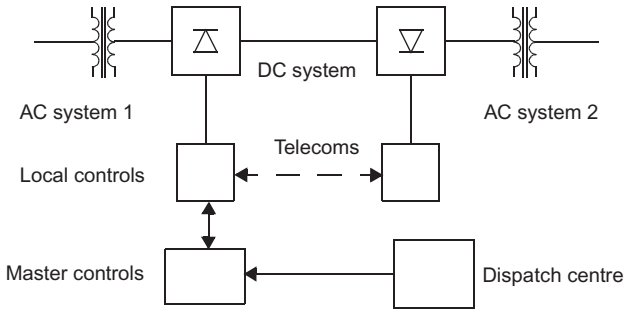


FIG. 27.10 Typical HVDC system linking two AC systems.

- stabilize the attached AC systems against any operational mode of the DC link.

The DC terminals each have their own local controllers. A centralized dispatch center will communicate a power order to one of the terminals that will act as a master controller and has the responsibility to coordinate the control functions of the DC link. Besides the primary functions, it is desirable that the DC controls have the following features:

- Limit the maximum DC current
  Due to a limited thermal inertia of the thyristor valves to sustain overcurrents, the maximum DC current is usually limited to less than 1.2 pu for a limited period of time.
- Maintain a maximum DC voltage for transmission
  This reduces the transmission losses and permits optimization of the valve rating and insulation.
- Minimize reactive power consumption
  This implies that the converters must operate at a low firing angle. A typical converter will consume reactive power between 50% and 60% of its MW rating. This amount of reactive power supply can cost about 15% of the station cost and comprise about 10% of the power loss.

The desired features of the DC controls are indicated below:

1. Limit maximum DC current—Since the thermal inertia of the converter valves is quite low, it is desirable to limit the DC current to prevent failure in the valves.
2. Maintain maximum DC voltage for transmission purposes to minimize losses in the DC line and converter valves.
3. Keep the AC reactive power demand low at either converter terminal. This implies that the operating angles at the converters must be kept low. Additional benefits of doing this are to reduce the snubber losses in the valves and reduce the generation of harmonics.
4. Prevent commutation failures at the inverter station and hence improve the stability of power transmission.
5. Other features, that is, the control of frequency in an isolated AC system or enhanced power system stability.

In addition to the above desired features, the DC controls will have to cope with the steady-state and dynamic requirements of the DC link, as shown in Table **27.2**.

TABLE 27.2 Requirements of the DC link

Steady-state requirements	Dynamic requirements
Limit the generation of noncharacteristic harmonics	Step changes in DC current or power flow
Maintain the accuracy of the controlled variable, that is, DC current and/or constant extinction angle	Start-up and fault-induced transients
Cope with the normal variations in the AC system impedances due to topology changes	Reversal of power flow
	Variation in frequency of attached AC system

TABLE 27.3 Choice of control strategy for two-terminal DC link

Condition No.	Desirable features	Reason	Control implementation
1	Limit the maximum DC current, I_d	For the protection of valves	Use constant current control at the rectifier
2	Employ the maximum DC voltage, V_d	For reducing power transmission losses	Use constant voltage control at the inverter
3	Reduce the incidence of commutation failures	For stability purposes	Use minimum extinction angle control at inverter
4	Reduce reactive power consumption at the converters	For voltage regulation and economic reasons	Use minimum firing angles

27.4.1 Basics of Control for a Two-Terminal DC Link

From converter theory, the relationship between the DC voltage V_d and DC current I_d is given by Eqs. (27.1)–(27.3). These three characteristics represent straight lines on the V_d-I_d plane. Notice that Eq. (27.2), that is, beta characteristic, has a positive slope, while the Eq. (27.3), that is, gamma characteristic, has a negative slope. The choice of the control strategy for a typical two-terminal DC link is made according to conditions in Table **27.3**.

Condition (27.1) implies the use of the rectifier in constant current control mode. And condition (27.3) implies the use of the inverter in constant extinction angle (CEA) control mode. Other control modes may be used to enhance the power transmission during contingency conditions depending upon applications. This control strategy is illustrated in Fig. 27.11.

The rectifier characteristic is composed of two control modes: alpha-min (line AB) and constant current (line BC). The alpha-min mode of control at the rectifier is imposed by the natural characteristics of the rectifier AC system and the ability of the valves to operate at alpha equal to zero, that is, in the limit, the rectifier acts as a diode rectifier. However, since a minimum positive voltage is desired before firing of the valves to ensure conduction, an alpha-min limit of about 2–5 degrees is typically imposed.

The inverter characteristic is composed of two modes: gamma-min (line PQ) and constant current (line QR). The operating point for the DC link is defined by the crossover point X of the two characteristics. In addition, a constant

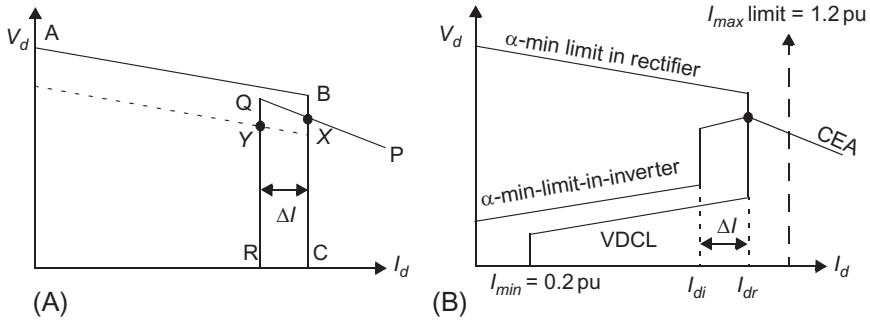


FIG. 27.11 Static V_d-I_d characteristic for a two-terminal link: (A) unmodified and (B) modified.

current characteristic is also used at the inverter. However, the current demanded by the inverter I_{di} is usually less than the current demanded by the rectifier I_{dr} by the current margin ΔI that is typically about 0.1 pu; its magnitude is selected to be large enough so that the rectifier and inverter constant current modes do not interact due to any current harmonics that may be superimposed on the DC current. This control strategy is termed the current margin method.

The advantage of this control strategy becomes evident if there is a voltage decrease at the rectifier AC bus. The operating point then moves to point Y. This way, the current transmitted will be reduced to 0.9 pu of its previous value, and voltage control will shift to the rectifier. However, the power transmission will be largely maintained near to 90% of its original value.

The control strategy usually employs the following other modifications to improve the behavior during system disturbances:

At the rectifier:

1. Voltage-dependent current limit, VDCL
   This modification is made to limit the DC current as a function of either the DC voltage or, in some cases, the AC voltage. This modification assists the DC link to recover from faults. Variants of this type of VDCL do exist. In one variant, the modification is a simple fixed value instead of a sloped line.
2. I_d-min limit
   This limitation (typically 0.2–0.3 pu) is to ensure a minimum DC current to avoid the possibility of DC current extinction caused by the valve current dropping below the hold-on current of the thyristors, an eventuality that could arise transiently due to harmonics superimposed on the low value of DC current. The resultant current chopping would cause high overvoltages to appear on the valves. The magnitude of I_d-min is affected by the size of the smoothing reactor employed.

At the inverter:

1. Alpha-min limit at inverter
   The inverter is usually not permitted to operate inadvertently in the rectifier region, that is, a power reversal occurring due to, say, an inadvertent current margin sign change. To ensure this, an alpha-min limit in inverter mode of about 100–110 degrees is imposed.
2. Current error region
   When the inverter operates into a weak AC system, the slope of the CEA control mode characteristic is quite steep and may cause multiple crossover points with the rectifier characteristic. To avoid this possibility, the inverter CEA characteristic is usually modified into either a constant beta characteristic or a constant voltage characteristic within the current error region.

27.4.2 Control Implementation

27.4.2.1 Historical Background

The *equidistant pulse firing control* systems used in modern HVDC control systems were developed in the mid-1960s [5,6]; although improvements have occurred in their implementation since then, such as the use of microprocessor-based equipment, their fundamental philosophy has not changed much. The control techniques described in Refs. [5,6] are of the *pulse frequency control* (PFC) type as opposed to the now-out-of-favor *pulse phase control* (PPC) type. All these controls use an independent *voltage-controlled oscillator* (VCO) to decouple the direct coupling between the firing pulses and the commutation voltage, V_{com}. This decoupling was necessary to eliminate the possibility of harmonic instability detected in the converter operation when the AC system capacity became nearer to the power transmission capacity of the HVDC link, that is, with the use of weak AC systems. Another advantage of the equidistant firing pulse controls was the elimination of noncharacteristic harmonics during steady-state operation. This was a prevalent feature during the use of the earlier *individual phase control* (IPC) system where the firing pulses were directly coupled to the commutation voltage, V_{com}.

27.4.2.2 Firing Angle Control

To control the firing angle of a converter, it is necessary to synchronize the firing pulses emanating from the ring counter to the AC commutation voltage that has a frequency of 60 Hz in steady state. However, it was noted quite early on (the early 1960s) that the commutation voltage (system) frequency is

not a constant, neither in frequency nor amplitude, during a perturbed state. However, it is the frequency that is of primary concern for the synchronization of firing pulses. For strong AC systems, the frequency is relatively constant and distortion free to be acceptable for most converter type applications. But as converter connections to weak AC systems became required more often than not, it was necessary to devise a scheme for synchronization purposes that would be *decoupled* from the commutation voltage frequency for durations when there were perturbations occurring on the AC system. The most obvious method is to utilize an *independent oscillator* at 60 Hz, which can be *synchronously locked* to the AC commutation voltage frequency. This oscillator would then provide the (phase) reference for the generation of firing pulses to the ring counter during the perturbation periods and would use the steady-state periods for locking in step with the system frequency. The advantage of this independent oscillator would be to provide an ideal (immunized and clean) sinusoid for synchronizing and timing purposes. There are two possibilities for this independent oscillator:

- Fixed-frequency operation
- Variable frequency operation

Use of a fixed-frequency oscillator (although feasible and called the pulse phase control oscillator) is not recommended, since it is known that the system frequency does drift, between say 55 and 65 Hz, due to the rotating machines used to generate electricity. Therefore, it is preferable to use a variable frequency oscillator (called the pulse frequency control oscillator) with a locking range of between 50 and 70 Hz and the center frequency of 60 Hz. This oscillator would then need to track the variations in the system frequency, and a control loop of some sort would be used for this tracking feature; this control loop would have its own gain and time parameters for steady-state accuracy and dynamic performance requirements.

The control loop for frequency tracking purposes would also need to consider the mode of operation for the DC link. The method widely adopted for DC-link operation is the so-called current margin method.

27.4.3 Control Loops

Control loops are required to track the following variables:

(a) The ordered current I_{or} at the rectifier and the inverter
(b) The ordered extinction angle (γ_o) at the inverter

27.4.3.1 Current Control Loops

In conventional HVDC systems, a PI regulator is used (Fig. 27.12) for the rectifier current controller. The rectifier plant system is inherently nonlinear and has a relationship given in Eq. (27.1). For constant I_d and for small changes in α, we have

$$\frac{\Delta V_d}{\Delta \alpha} = -V_{dor} \cdot \sin \alpha. \tag{27.4}$$

It is obvious from Eq. (27.4) that the maximum gain ($\Delta V_d/\Delta\alpha$) occurs when $\alpha = 90$ degrees. Thus, the control loop must be stabilized for this operation point, resulting in slower dynamic properties at normal operation with α within the range 12–18 degrees. Attempts have been made to linearize this gain and have met with some limited success. However, in practical terms, it is not always possible to have the DC link operating with the rectifier at 90 degrees due to harmonic generation and other protection elements coming into operation also. Therefore, optimizing the gains of the PI regulator can be quite arduous and take a long time. For this reason, the controllers are often pretested in a physical simulator environment to obtain approximate settings. Final (often very limited) adjustments are then made on-site.

Other problems with the use of a PI regulator are listed below:

- It is mostly used with fixed gains, although some possibility for gain scheduling exists.
- It is difficult to select optimal gains, and even then, they are optimal over a limited range only.
- Since the plant system is varying continually, the PI controller is not optimal.

A similar current control loop is used at the inverter (Fig. 27.13). Since the inverter also has a gamma controller, the selection between these two controllers is made via a MINIMUM SELECT block. Moreover, in order to bias the inverter current controller off, a current margin signal ΔI is subtracted from the current reference I_{or} received from the rectifier via a communication link.

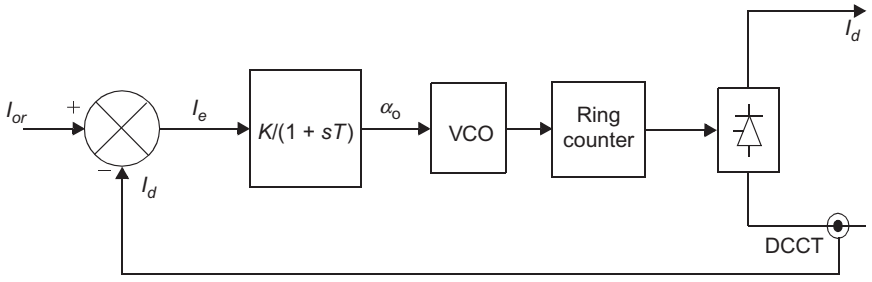


FIG. 27.12 Control loop for the rectifier.

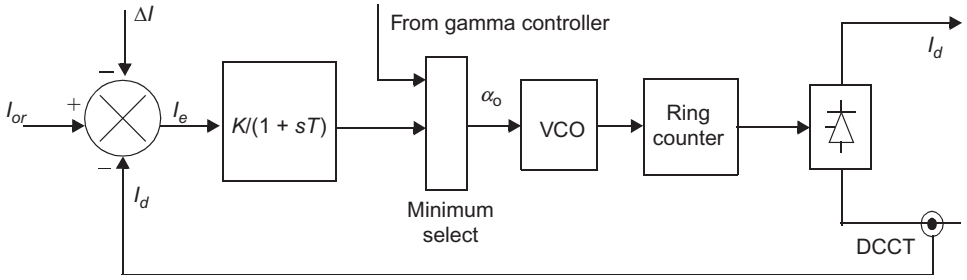


FIG. 27.13 Current controller at the inverter.

Telecommunication requirements

As was discussed above, the rectifier and inverter current orders must be coordinated to maintain a current margin of about 10% between the two terminals at all times; otherwise, there is a risk of loss of margin, and the DC voltage could run down. Although, it is possible to use slow voice communication between the two terminals and maintain this margin, the advantage of fast control action possible with converters may be lost for protection purposes. For maintaining the margin during dynamic conditions, it is prudent to raise the current order at the rectifier first followed by the inverter; in terms of reducing the current order, it is necessary to reduce at the inverter first and then at the rectifier.

27.4.3.2 Gamma Control Loop

At the inverter end, there are two known methods for the gamma control loop. The two variants are different only due to the method of determining the extinction angle:

- Predictive method for the indication of extinction angle (gamma)
- Direct method for actual measurement of extinction angle (gamma)

In either case, a delay of one cycle occurs from the indication of actual gamma and the reaction of the controller to this measurement. Since the avoidance of a commutation failure often takes precedence at the inverter, it is normal to use the minimum value of gamma measured for the 6 or 12 inverter valves for the converter(s).

1. *Predictive method of measuring gamma*

   The predictive measurement tries to maintain the commutation *voltage-time area after commutation* larger than a specified minimum value. Since the gamma prediction is only approximative, the method is corrected by a slow feedback loop that calculates the error between the predicted value and actual value of gamma (one cycle later) and feeds it back.

   The predictor calculates continuously, by a triangular approximation, the total available voltage-time area that remains after commutation is finished. Since an estimate of the overlap angle μ is necessary, it is derived from a well-known fact in converter theory that the overlap commutation voltage-time area is directly proportional to direct current and leakage impedance (assumed constant and known) value of the converter transformer.

   The prediction process is inherently of an individual phase firing character. If no further measures are taken, each valve would fire on the minimum margin condition. To counteract this undesired property, a special firing symmetrizer is used; when one valve has fired on the minimum margin angle, the following two or five valves fire equidistantly. (The choice of either two or five symmetrized valves is mainly a stability question.)

2. *Direct method of measuring gamma*

   In this method, the gamma measurement is derived from a measurement of the actual valve voltage. Waveforms of the gamma measuring circuit are shown in Fig. 27.13. An internal timing waveform, consisting of a ramp function of fixed slope, is generated after being initiated from the instant of anode current zero. This value corresponds to a direct voltage proportional to the last value of gamma. From the gamma values of all (either 6 or 12) valves, the smallest value is selected to produce the indication of measured gamma for use with the feedback regulator (Fig. 27.14).

   This value is compared with a gamma-ref value, and a PI regulator defines the dynamic properties for the controller. Inherently, this method has an individual phase control characteristic. One version of this type of control

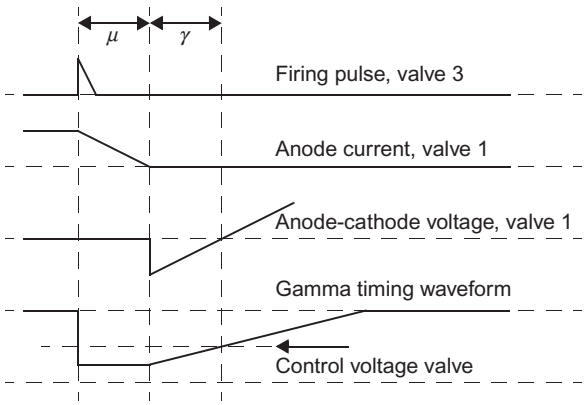


FIG. 27.14 Waveforms for the gamma measuring circuit [5].

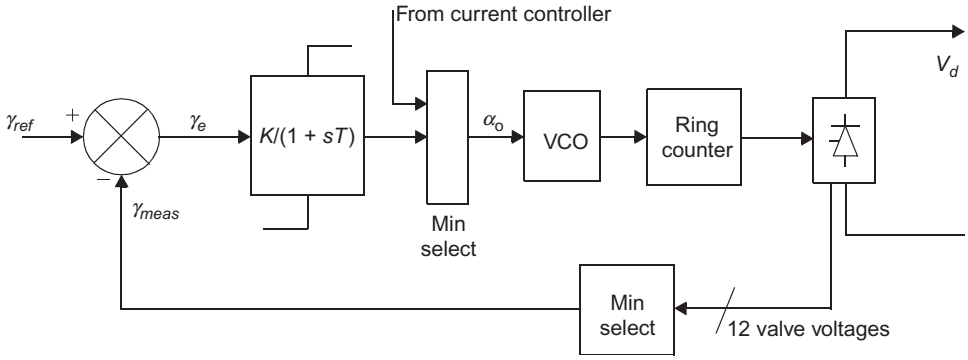


FIG. 27.15 Gamma feedback controller.

implementation overcomes this problem by using a symmetrizer for generating equidistant firing pulses. The 12-pulse circuit generates 12 gamma measurements; the minimum gamma value is selected and then used to derive the control voltage for the firing pulse generator with symmetrical pulses (Fig. 27.15).

27.4.4 Hierarchy of DC Controls

Since HVDC controls are hierarchical in nature, they can be subdivided into blocks that follow the major modules of a converter station (Fig. 27.16). The main control blocks are as follows:

1. The bipole (master) controller is usually located at one end of the DC link and receives its power order from a centralized system dispatch center. The bipole controller derives a current order for the pole controller using a local measurement of either AC or DC voltage. Other inputs may also be used by the bipole controller such as frequency control for damping or modulation purposes. A communication to the remote terminal of the DC link is also necessary to coordinate the current references to the link.
2. The pole controller then derives an alpha order for the next level. This alpha order is sent to both the positive and negative poles of the bipole.
3. The valve group controllers generate the firing pulses for the converter valves. Controls also receive measurements of DC current, DC voltage, and AC current into the converter transformer. These measurements assist in the rapid alteration of firing angle for protection of the valves during perturbations. A slow loop for control of tap-changer position as a function of alpha is also available at this level.

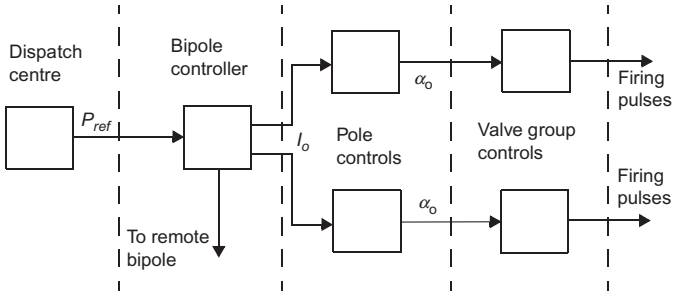


FIG. 27.16 Hierarchy of controllers.

27.4.5 Monitoring of Signals

As described earlier, monitoring of the following signals is necessary for the controls (Fig. 27.17) to perform their functions and assist in the protection of the converter equipment:

V_d and I_d—DC voltage and DC current, respectively,
I_{AC} and I'_{AC}—AC current on line side and converter side of the converter transformer, respectively,
V_{AC}—AC voltage at the AC filter bus.

27.4.6 Protection Against Over-Currents

Faults and disturbances can be caused by malfunctioning equipment or insulation failures due to lightening and pollution. First, these faults need to be detected with the help of monitored signals. Second, the equipment must be protected by control or switching actions. Since DC controls can react within one cycle, control action is used to protect equipment against overcurrent and overvoltage stresses and minimize loss of transmission. In a converter station, the valves are the most critical (and most expensive) equipment that need to be protected rapidly due to their limited thermal inertia.

The basic types of faults that the converter station can experience are the following:

- Current extinction (CE)

  CE can occur if the valve current drops below the holding current of the thyristor. This can happen at low-current operation accompanied by a transient leading to current extinction. Due to the phenomena of current chopping of an inductive current, severe overvoltages may result. The size of the smoothing reactor and the rectifier minimum current setting I_{min} helps to minimize the occurrence of CE.
- Commutation failure (CF) or misfire

  In line-commutated converters, the successful commutation of a valve requires that the extinction angle

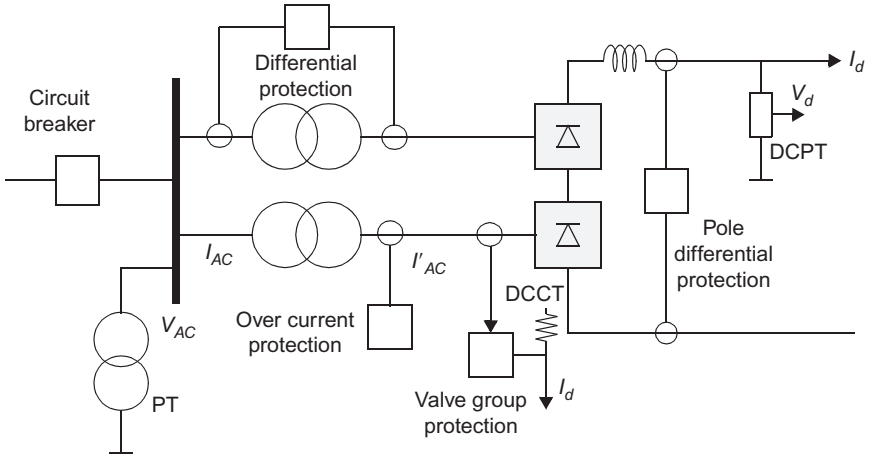


FIG. 27.17 Monitoring points for the protection circuits.

γ-nominal be maintained more than the minimum value of the extinction angle γ-min. Note that γ-nominal $= 180 - \alpha - \mu$. The overlap angle μ is a function of the commutation voltage and the DC current. Hence, a decrease in commutation voltage or an increase in DC current can cause an increase in μ, resulting in a decrease in γ-nominal. If γ-nominal $< \gamma$-min, a CF may result. In this case, the outgoing valve will continue to conduct current, and when the incoming valve is fired in sequence, a short circuit of the bridge will occur.

A missing firing pulse can also lead to a misfire (at a rectifier) or a CF (at an inverter). The effects of a single misfire are similar to those of a single CF. Usually, a single CF is self-clearing, and no special control actions are necessary. However, a multiple CF can lead to the injection of AC voltages into the DC system. Control action may be necessary in this case.

The detection of a CF is based on the differential comparison of DC current and AC currents on the valve side of the converter transformer. During a CF, the two valves in an arm of the bridge are conducting. Therefore, the AC current goes to zero, while the DC current continues to flow.

The protection features employed to counteract the impact of a CF are indicated in Table **27.4**.

- Short circuits—internal or DC line

  An internal bridge fault is rare as the valve hall is completely enclosed and is air-conditioned. However, a bushing can fail, or valve cooling water may leak resulting in a short circuit. The AC breaker may have to be tripped to protect against bridge faults.

  The protection features employed to counteract the impact of short circuits are indicated in Table **27.4**.

The fast-acting HVDC controls (which operate within one cycle) are used to regulate the DC current for protection of the valves against AC and DC faults.

The basic protection (Fig. 27.18) is provided by the VGP differential protection that compares the rectified current on the valve side of the converter transformer with the DC current measured on the line side of the smoothing reactor. This method is applied because of its selectivity possible due to high impedances in the smoothing reactor and converter transformer.

TABLE 27.4 Protection against overcurrents

Fault type	Occurrence	Fault current level	Protection method
Internal faults	Infrequent	10 pu	Valve is rated to withstand this surge
DC line faults	Frequent	2–3 pu	– Forced retard of firing angle – Dynamic VDCL deployment – Trip AC breaker CB after third attempt
Commutation failures (single or multiple)	Very frequent	1.5–2.5 pu	Single CF: – Self-clearing Multiple CF: – Beta angle advanced in stages – Static VDCL deployment

The OCP is used as a backup protection in case of malfunction in the VGP. The level of overcurrent setting is set higher than the differential protection.

The pole differential protection (PDP) is used to detect ground faults, including faults in the neutral bus.

27.4.7 Protection Against Over-Voltages

The typical arrangement of metal oxide surge arrestors for protecting equipment in a converter pole is shown in Fig. 27.18. In general, overvoltages entering from the AC bus are limited by the AC bus arrestors; similarly, overvoltages entering the converter from the DC line are limited by the DC arrestor. The AC and DC filters have their respective arrestors also. Critical

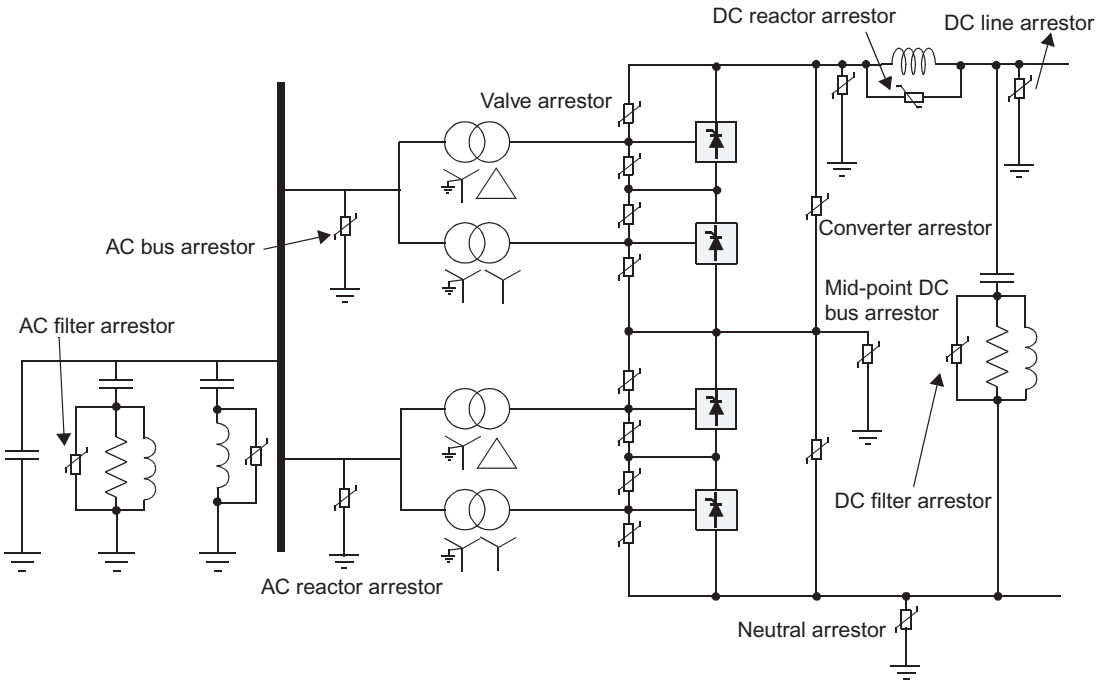


FIG. 27.18 Typical arrangement of surge arrestors for a converter pole.

components such as the valves have their own arrestors placed close to these components. The protective firing of a valve is used as a backup protection for overvoltages in the forward direction. Owing to their varied duty, these arrestors are rated accordingly for the location used. For instance, the converter arrestor for the upper bridge is subjected to a higher energy dissipation than for the lower bridge.

Since the evaluation of insulation coordination is quite complex, detailed studies are often required with DC simulators to design an appropriate insulation coordination strategy.

27.5 MTDC Operation

Most HVDC transmission systems are two-terminal systems. A multiterminal DC system (MTDC) has more than two terminals, and there are two existing installations of this type. There are two possible ways of tapping power from an HVDC link, that is, with series or parallel taps.

27.5.1 Series Tap

A monopolar version of a three-terminal series DC link is shown in Fig. 27.19. The system is grounded at only one suitable location. In a series DC system, the DC current is set by one terminal and is common to all terminals; the other terminals are operated at a constant delay angle for a rectifier and constant extinction angle for inverter operation with the help of transformer tap changers.

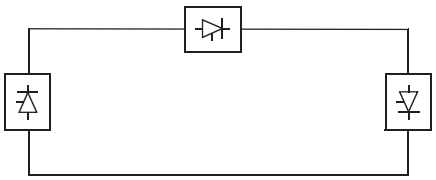


FIG. 27.19 Series tap.

Power reversal at a station is done by reversing the DC voltage with the aid of angle control.

No practical installation of this type exists in the world at present. From an evaluation of ratings and costs for series taps, it is not practical for the series tap to exceed 20% of the rating for a major terminal in the MTDC system.

27.5.2 Parallel Tap

A monopolar version of a three-terminal parallel DC link is shown in Fig. 27.20. In a parallel MTDC system, the system voltage is common to all terminals. There are two variants possible for a parallel MTDC system: radial or mesh. In a radial system, disconnection of one segment of the system will interrupt power from one or more terminals. In a mesh system, the removal of one segment will not interrupt power flow providing the remaining links are capable of carrying the required power.

Power reversal in a parallel system will require mechanical switching of the links as the DC voltage cannot be reversed.

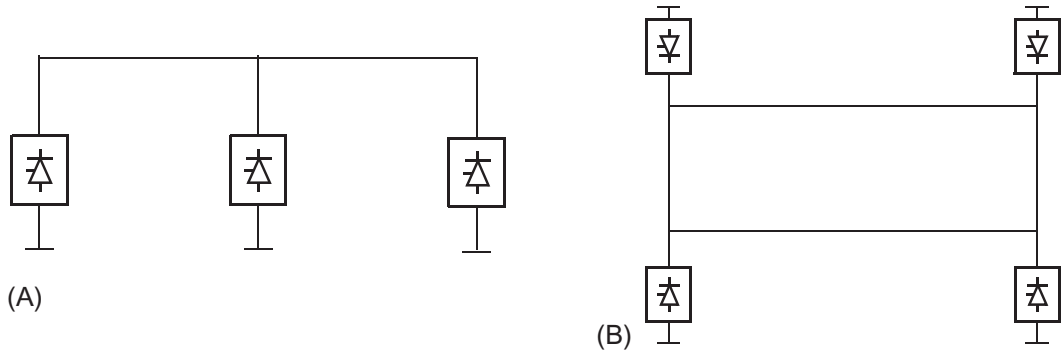


FIG. 27.20 Parallel tap: (A) radial type and (B) mesh type.

From an evaluation of ratings and costs for parallel taps, it is not practical for the parallel tap to be less than 20% of the rating for a major terminal in the MTDC system.

There are two installations of parallel taps existing in the world. The first is the Sardinia-Corsica-Italy link where a 50 MW parallel tap at Corsica is used. Since the principal terminals are rated at 200 MW, a commutation failure at Corsica can result in very high overcurrents (typically 7 pu); for this reason, large smoothing reactors (2.5 H) are used in this link.

The second installation is the Quebec-New Hampshire 2000 MW link where a parallel tap is used at Nicolet. Since the rating of Nicolet is at 1800 MW, the size of the smoothing reactors was kept to a modest size.

27.5.3 Control of MTDC System

Although several control methods exist for controlling MTDC systems, the most widely utilized method is the so-called current margin method that is an extension of the control method used for two-terminal DC systems.

In this method, the voltage setting terminal (VST) operates at the angle limit (minimum alpha or minimum gamma), while the remaining terminals are controlling their respective currents. The control law that is used sets the current reference at the voltage setting terminal according to

$$\Sigma \cdot I_j ref = \Delta I \tag{27.5}$$

where ΔI is known as the current margin.

The terminal with the lowest voltage ceiling acts as the VST.

An example of the control strategy is shown in Fig. 27.21 for a three-terminal DC system with one rectifier REC and two inverters, INV1 at 40% and INV2 at 60% rating. The REC1 and INV2 terminals are maintained in current control, while INV1 is the VST operating in CEA mode.

Due to the requirement to maintain current margin for the MTDC system at all times, a centralized current controller, known as the current reference balancer (CRB) (Fig. 27.22), is required. With this technique, reliable two-way telecommunication links is required for current reference coordination

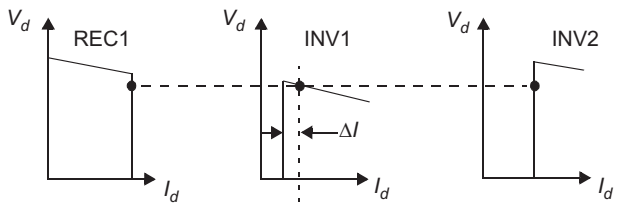


FIG. 27.21 Current margin method of control for MTDC system.

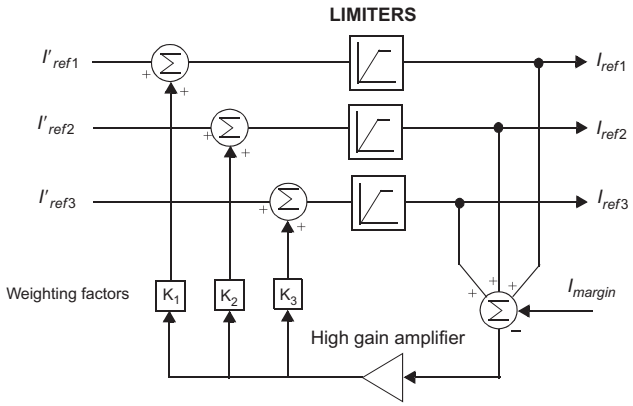


FIG. 27.22 Current reference balancer.

purposes. The current orders, I_{ref1}–I_{ref3}, at the terminals must satisfy the control law according to Eqs. (27.5) and (27.6). The weighting factors (K_1, K_2, and K_3) and limits are selected as a function of the relative ratings of the terminals.

27.6 Application

27.6.1 HVDC Interconnection at Gurun (Malaysia)

The 240/600 MW HVDC interconnection between Malaysia and Thailand is a major first step in implementing electric power network interconnections in the ASEAN region. It is jointly undertaken by two utilities, Tenaga Nasional Berhad (TNB) of Malaysia and Electricity Generating Authority of

Thailand (EGAT). This will be the first HVDC project for both these utilities. The HVDC interconnection consists of a 110 km HVDC line (85 km owned by TNB and 25 km owned by EGAT) with the DC converter stations at Gurun on the Malaysian side and Khlong Ngae on the Thailand side. The scheme entered into commercial operation in July 2000. The interconnection provides a range of diverse benefits such as

- spinning reserve sharing,
- economic power exchange-commercial transactions,
- emergency assistance to either AC system,
- damping of AC system oscillations,
- reactive power support (voltage control),
- deferment of generation plant up.

27.6.1.1 Power Transmission Capacity

The converter station is presently constructed for monopolar operation for power transfer of 240 MW in both directions with provisions for future extensions to a bipole configuration giving a total power-transfer capability of 600 MW. The HVDC line is constructed with two pole conductors to cater for the second 240 MW pole. Full-length neutral conductors are used instead of ground electrodes because of high land costs and inherently high values of soil resistivity.

The monopole is rated for a continuous power of 240 MW (240 kV and 1000 A) at the DC terminal of the rectifier station. In addition, there is a 10 min overload capability of up to 450 MW, which may be utilized once per day when all redundant cooling equipment is in service.

The HVDC interconnection scheme is capable of continuous operation at a reduced DC voltage of 210 kV (70%) over the whole load range up to the rated DC current of 1000 A with all redundant cooling equipment in service.

27.6.1.2 Performance Requirements

A high degree of energy availability was a major design objective (Fig. 27.23). Guaranteed targets for both stations are the following:

- Energy availability: >99.5%
- Forced energy unavailability: <0.43%
- Forced outage rate: <5.4 outages per year

27.6.1.3 Technical Information

See Table **27.6**.

27.6.1.4 Major Technical Features

The station incorporates the latest state-of-the-art technology in power electronics and control equipment. The features include the following:

- A fully decentralized control and protection system
- Active DC filter technology
- Hybrid DC current shunt measuring devices
- Triple-tuned AC filter

27.7 Modern Trends

27.7.1 Converter Station Design of the 2000s

The 1500 MW, ±500 kV Rihand-Delhi HVDC transmission system (commissioned in 1991) serves as an example of a

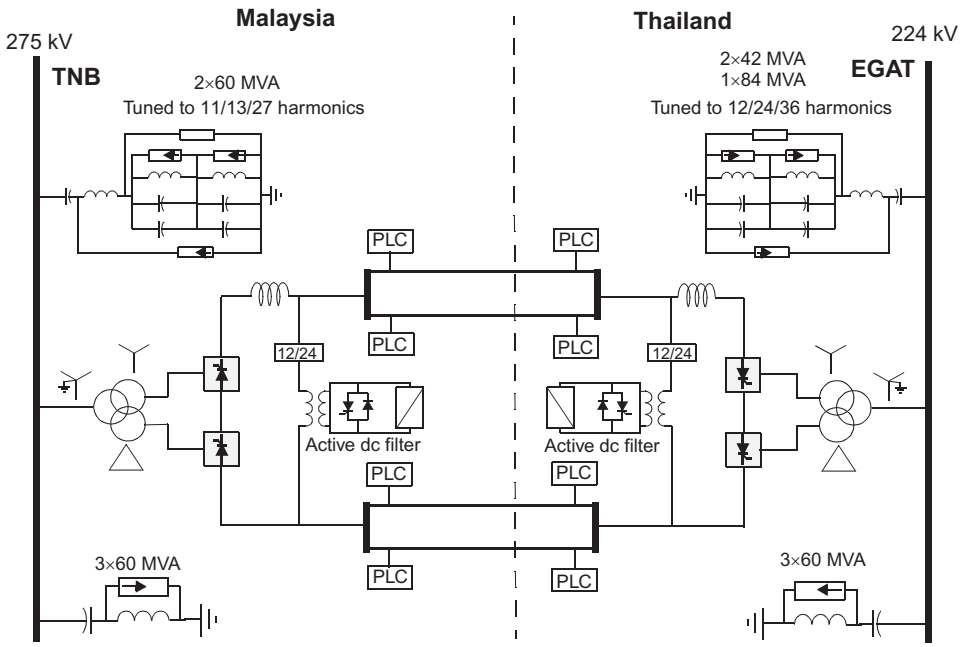


FIG. 27.23 One-line diagram of the HVDC interconnection between Malaysia and Thailand.

TABLE 27.5 Main data 1

Monopolar operation		Rectifier (Malaysia)	Inverter (Thailand)
DC power, P_{dn}	Rated	240 MW (stage 1)	240 MW
	Max. overload (10 min)	450 MW	
	Minimum (10% of rated)	24 MW	
DC current, I_{dn}		1000 A	1000 A
DC voltage, U_{dn}		240 kV	293.5 kV
Firing angle, alpha		15.0 degrees	–
Extinction angle, gamma		–	19.6 degrees
Transformer sec. voltage, U_v		122.2 kV	122.2 kV
Converter reactive power, Q_{DC}		133.3 MVAr	150.9 MVAr
Reduced DC voltage operation	210 kV (70% DC voltage)		
AC system voltage		275 kV, 50 Hz	224 kV, 50 Hz
DC transmission line Distance	110 km		

TABLE 27.6 Main data 2

Main equipment	GURUN converter station
Smoothing reactor	100 mH
DC filter	Active type DC filters including passive type (twelfth/twenty-fourth harmonics)
AC filter	2×60 MVAr (11/13/27)
Reactive power compensation	3×60 MVAr C-shunt
Power thyristor	Type T1501 N75T-S34
Diameter	100 mm
Blocking voltage	7.5 kV repetitive, 8.0 kV nonrepetitive
Max. DC current	1550 A, 120 degrees el., $T_c = 60°C$
Max. effective current	3240 A
Converter transformer	Single phase, three winding
	Rated power = 275 kV/116 MVA
Transmission line	Cardinal ACSR 546 mm^2, twin conductors per pole
Pole conductor	
Neutral conductor	Hen ACSR 298 mm^2

typical design of the last decade. Its major design aspects were the following:

- Stations employ water-cooled valves of indoor design with the valves arranged as three quadruple valves suspended from the ceiling of the valve hall.
- Converter transformers are one-phase, three-winding units situated close to the valve hall with their bushings protruding into the valve hall.
- AC filtering is done with conventional, passive, double-tuned, and high-pass units employing internally fused capacitors and air-cored reactors; these filters are mechanically switched for reactive power control.
- DC filtering is done with conventional, passive units employing a split smoothing reactor consisting of both an oil-filled reactor and an air-cored reactor.
- DCCT measurement is based on a zero-flux principle.
- Control and protection hardware is located in a control room in the service building between the two valve halls. The controls still employed some analog parts, particularly for the protection circuits. The controls were duplicated with an automatic switchover to hot standby for reliability reasons.

This design was done in the 1980s to meet the requirements of the day for increased reliability and performance requirements, that is, availability, reduced losses, higher overload capability, etc. However, these requirements led to increased costs for the system.

The next-generation equipment is now being spearheaded by a desire to reduce costs and make HVDC as competitive as AC transmission. This is being facilitated by the major developments of the past decade that have taken place in power electronics. Therefore, the next-generation HVDC equipment will be influenced by the following.

27.7.1.1 Thyristor Development

HVDC thyristors are now available with a diameter of 150 mm at a rating of 8–9 kV and power handling capacity of 1500 kW that will lead to a dramatic decrease in the number of series-connected components for a valve with consequential cost reductions and improvement in reliability.

The development of the light-triggered thyristor (LTT) (Figs. 27.24 and 27.25) is likely to eliminate the electronic unit (with their high number of electronic components) for generating the firing pulses for the thyristor (Fig. 27.26). The

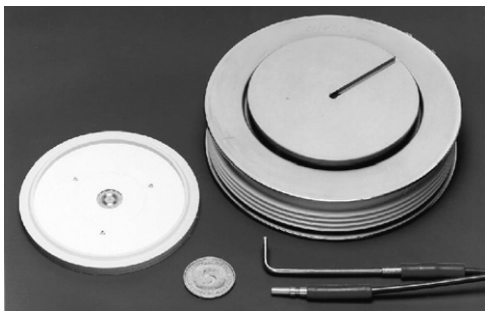


FIG. 27.24 Silicon wafer and construction of the LTT. The light guides appear in the bottom right-hand corner.

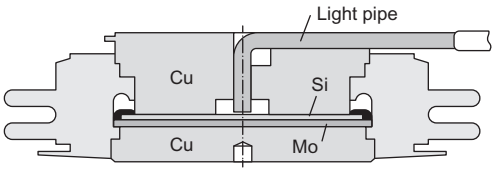


FIG. 27.25 Cross section of the LTT with the light pipe entry.

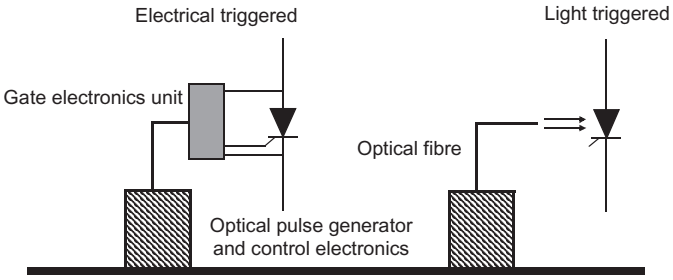


FIG. 27.26 Conventional firing versus light-triggered firing.

additional functional requirements of monitoring and protection of the device are being incorporated also.

Both of the above developments present the possibility of achieving compact valves that can be packaged for outdoor construction, thereby reducing the overall cost and reliability of the station.

27.7.1.2 Higher DC Transmission Voltages

For long-distance transmission, there is a tendency to use a high voltage to minimize the losses. The typical transmission voltage has been ±500 kV, although the Itaipu project in Brazil uses 600 kV. The transmission voltage has to balance against the cost of insulation. The industry is considering raising the voltage to ±800 kV.

27.7.1.3 Controls

It is now possible to operate an HVDC scheme into an extremely weak AC system, even with short-circuit capacity down to unity.

Using programmable DSPs has resulted in a compact and modular design that is low cost; furthermore, the number of control cubicles has decreased by a factor of almost 10 times in the past decade. Now, all control functions are implemented on digital platforms. The controls are fully integrated having monitoring, control, and protection features. The design incorporates self-diagnostic and supervisory characteristics. The controls are optically coupled to the control room for reliable operation. Redundancy and duplication of controls is resulting in very high reliability and availability of the equipment.

27.7.1.4 Outdoor Valves

The introduction of air-insulated, outdoor valves will reduce costly requirements for a valve hall. The use of a modular, compact design that will be preassembled in the manufacturing plant will save installation time and provide for a flexible station layout. This design has been feasible because of development of a composite insulator for DC applications that is used as a communication channel for fiber optics, cooling water, and ventilation air between the valve unit and ground.

27.7.1.5 Active DC Filters

This development, made possible due to advances in power electronics and microprocessors, has resulted in a more efficient DC filter operating over a wide spectrum of frequencies and provides a compact design (Fig. 27.27).

27.7.1.6 AC Filters

Conventional AC filters used passive components for tuning out certain harmonic frequencies. Due to the variations in frequency and capacitance, physical aging, and thermal

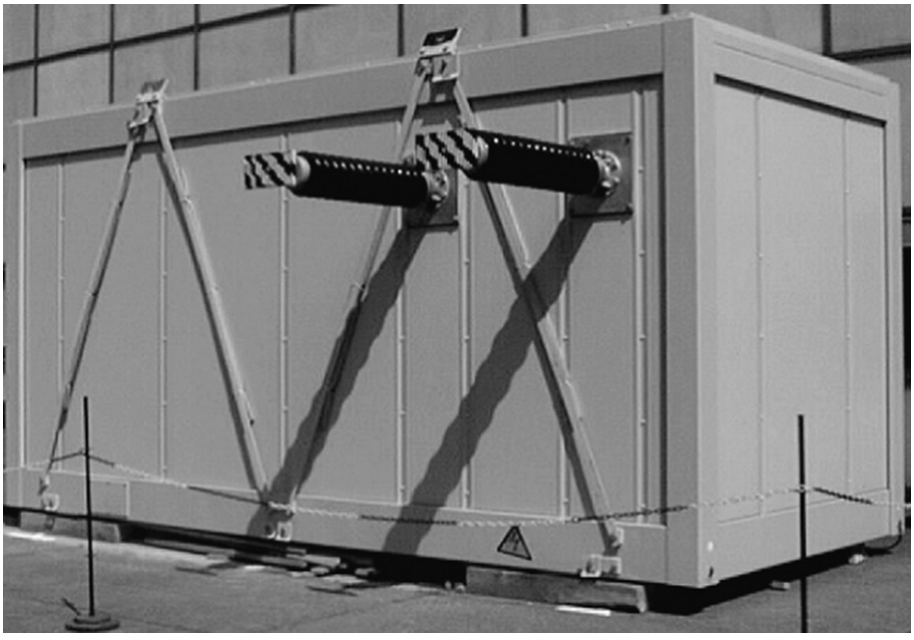


FIG. 27.27 Compact outdoor container with an active DC filter.

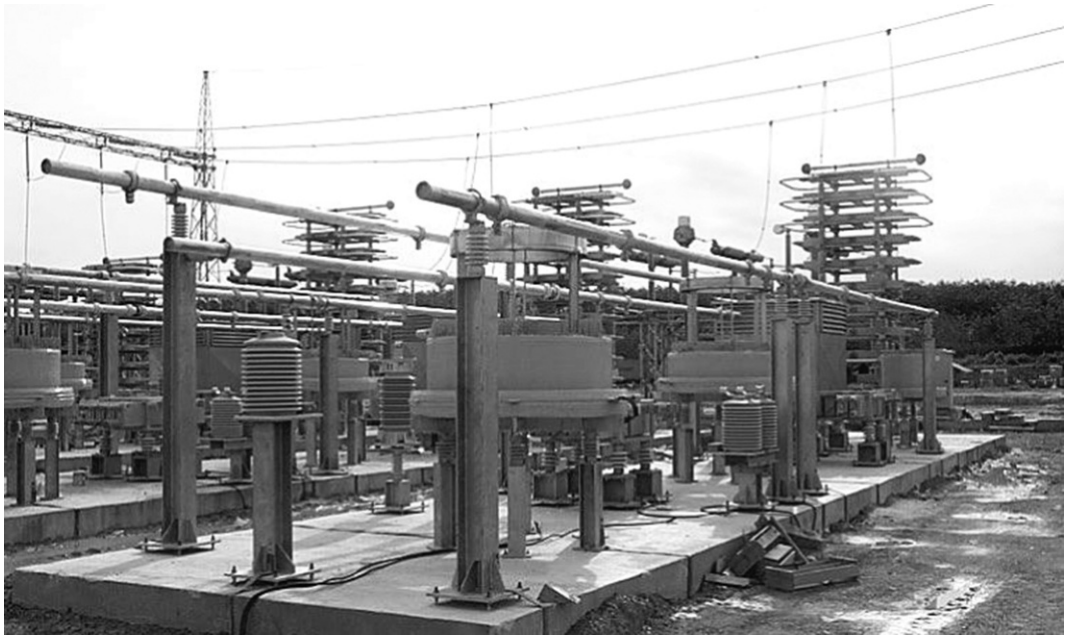


FIG. 27.28 Installation of the triple-tuned filter at the Gurun station in Malaysia.

characteristics of these tuned filters, the quality factors for the filters were typically about 100–125, which meant that the filters could not be too sharply tuned for efficient harmonic filtering. The advent of electronically tunable inductors, based on the transductor principle, means that the *Q*-factors can now approach the natural one of the inductor. This will lead to much more enhanced filtering capacities (Fig. 27.28).

27.7.1.7 AC-DC Current Measurements

The new optical current transducers utilize a precision shunt at high potential. A small optical fiber link between ground and high potential is utilized resulting in a lower probability of a flashover. The optical power link transfers power to high potential for use in the electronic equipment. The optical data link transfers data to ground potential. This transducer results in high reliability, compact design, and efficient measurement (Fig. 27.29).



FIG. 27.29 The optical current transducer.

27.7.1.8 New Topologies

Two new topological changes to the converter design will impact greatly on future designs:

1. Series-compensated commutation:

   There are two variants to this topology: the capacitor-commutated converter (CCC) (Fig. 27.30A) and the controlled series capacitor converter (CSCC) (Fig. 27.30B). Essentially, the behavior of the two variants is very similar. The insertion of a capacitor in series with the converter transformer leakage reactance causes a major reduction in the commutation impedance of the converter resulting in a reduction in the reactive power requirement of the converter. An increase in the size of the series capacitor can even result in the converter operation at a leading power factor if so desired. However, the negative impact of a lower commutation impedance results in additional stresses on the valves and transformers and additional cost implications [7].

   The first CCC back-to-back converter station (rated at 2×550 MW) has been put into service at Garabi, on the

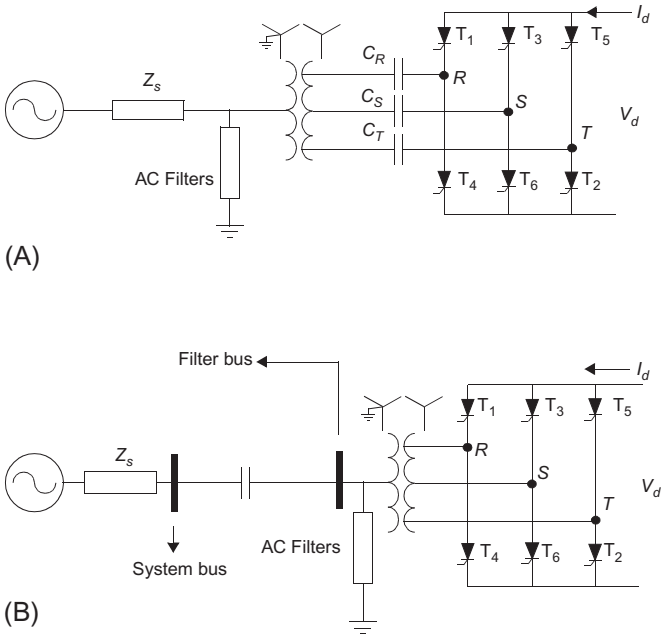


FIG. 27.30 (A) Capacitor-commutated converter circuit and (B) controlled series capacitor converter circuit.

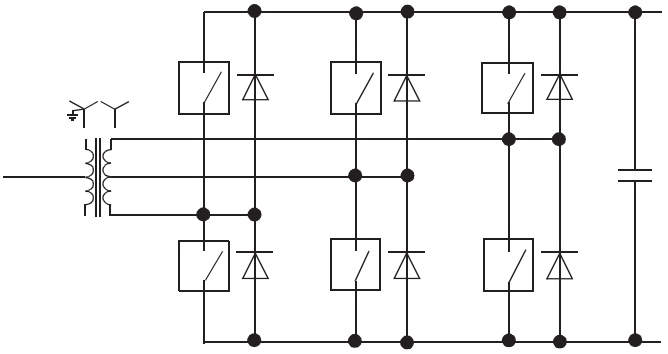


FIG. 27.31 Voltage-source converter topology.

Brazilian side of the Uruguay River. The system interconnects the electric systems of Argentina and Brazil.

2. Voltage-source converters (VSC): The use of self-commutation with the new-generation switching devices (i.e., GTOs and IGBTs) has resulted in the topology of a voltage-source converter (VSC) (Fig. 27.31) as opposed to the conventional converter using line-commutated thyristors and current source converter (CSC) topology. The VSC, being self-commutated, can control active/reactive power and, with PWM techniques, control harmonic generation as well. The application of such circuits is presently limited by the switching losses and ratings of available switching devices. The ongoing advances in power electronic devices are expected to have a major impact on the future application of this type of converter in HVDC transmission. New application areas, particularly in distribution systems, are being actively investigated with this topology. Table **27.5** provides a partial list of the HVDC links in operation using this technique.

One major difficulty for the use of the VSC is the threat posed to the valves from a short circuit on the DC line. Unlike the CSC where the valves are inherently protected against short-circuit currents by the presence of the smoothing reactor, the VSC is relatively unprotected. For this reason, the VSC applications are almost always used with DC cables where the risk of a DC line short circuit is greatly reduced (Table **27.7**).

27.7.1.9 Compact Station Layout

The advances discussed above have resulted in marked improvement of the footprint requirement of the compact station [8] of the year 2000 that has about 24% space requirement of the comparable HVDC station designed in the past decade (Fig. 27.32).

27.8 VSC-HVDC System

27.8.1 Introduction

The existing power transmission networks in most developed countries are heavily loaded that has created the risk of system instability and power quality deterioration. Furthermore, these countries have the problem of obtaining right of ways and face environmental issues for the construction of new transmission lines. The necessity for a new technology by which increased power transmission can be achieved using the existing network infrastructure is clear. As explained earlier, the VSC-HVDC transmission system can take the place of this technology to solve the problem to some extent. The VSC-HVDC system is a relatively mature technology that comprises the high-power, high-frequency semiconductor switches (i.e., IGBTs and GTOs). These devices incorporated with antiparallel diodes make one complete unit. Several units are connected in series to build a valve to get the required voltage level and to increase the redundancy in the converter. The control of these switches is done by using pulse-width modulation (PWM) techniques by which it is possible to control the magnitude and phase angle of the generated fundamental (60 Hz) voltage component. This high controllability of VSC results in a wide range of power system applications like VSC-HVDC, static synchronous compensator (STATCOM), static synchronous series compensator (SSSC), unified power flow controller (UPFC), interline power flow controller (IPFC), and active filters. In addition to bulk power transmission, strategically located VSC-HVDC system in an existing AC power system network augments the network stability and reliability during disturbances and contingencies.

TABLE 27.7 Applications of HVDC Light technology

No.	Project	Rating		Distance (km)	Application	Commissioned
		MVA	kV			
1	Hellsjon	3	±10	10	AC-DC conversion	Mar. 1997
2	Gotland	50	±80	70	Feed from wind power generation	Jun. 1999
3	Tjaereborg	7	±10	4	Feed from wind power generation	Aug. 1999
4	Directlink	180	±140	65	Asynchronous interconnection	Dec. 1999
5	Murraylink	220	±140	180	Asynchronous interconnection	2002
6	Shoreham	330	±140	40	Cross sound cable link	2002
7	Troll A 1&2	2 × 42	±60	70	Gas production offshore platform	2005
8	Estlink	350	±150	2 × 74	Length of land cable, sea crossing, and nonsynchronous AC systems	2006
9	Caprivi Link	300	350	950	Interconnecting grids, energy trade	2010
10	Valhall	78	150	292	Power from shore	2011
11	BorWin1	400	±150	200	Offshore wind connections	2012
12	East-West Interconnector	500	±200	261	AC voltage control, black start	2012
13	Skagerrak 4	700	500	244	Interconnecting grids, grid stability	2014
14	Mackinac	200		±71	DC links in AC grids	2014
15	DolWin1	800	±320	165	Offshore wind connection	2015
16	DolWin2	900	±320	135	Offshore wind connection	2015
17	NordBalt	700	±300	450	Prepare for future DC grid, black start	2015
18	Troll A 3&4	2 × 50	±60	70	Power from shore	2015
19	Åland	100	±80	158	Asynchronous networks	2015
20	Maritime Link	500	±250	180	Connecting remote generation	2017
21	Caithness-Moray	800/1200	±350	160	Reinforcement of AC network	2018
22	Johan Sverdrup	100	±80	200	Offshore oilfield	2019
23	Kriegers	Flak	410	±140	Asynchronous networks	2019
24	NordLink	2 × 700	±500	571	Interconnecting grids, energy trade	2020
25	NSL	2(700)	±515	722	Interconnecting grids, energy trade	2021

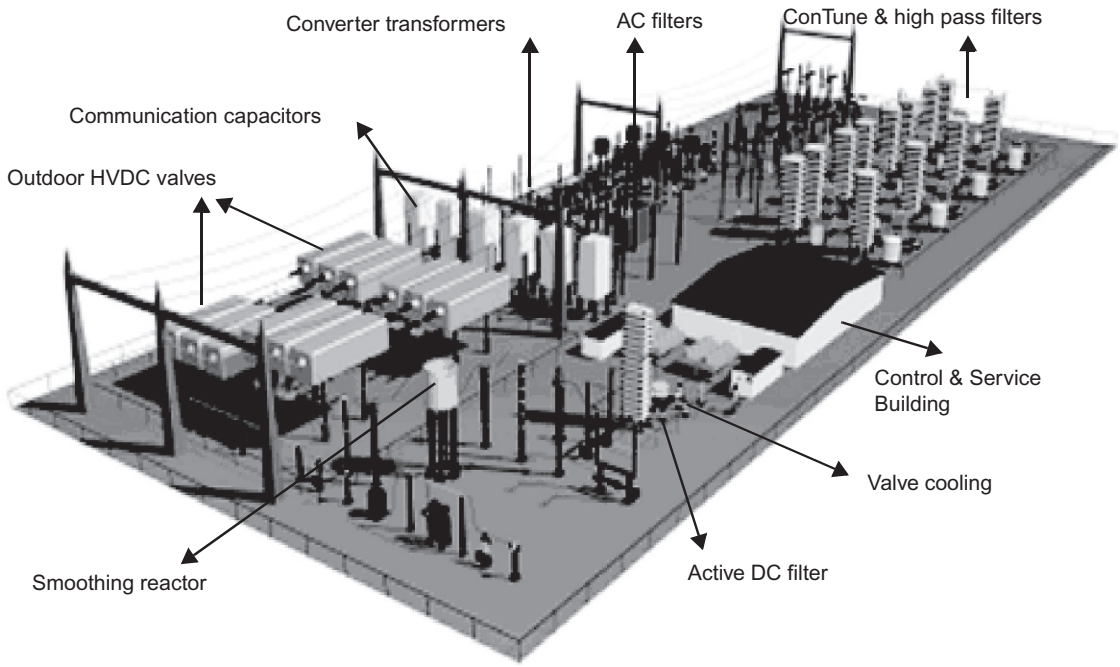


FIG. 27.32 Layout of a compact HVDC.

27.8.2 VSC-HVDC System

Fig. 27.33 shows the single-line diagram of a VSC-HVDC system that interconnects two AC networks of same operating frequency for power transmission and stability improvement during contingencies. The system consists of different equipments, such as shunt-connected RLC filters, interfacing transformers, VSCs and their control systems, DC overhead or underground cables, and DC capacitors. The following subsections provide explanations regarding the function of each apparatus comprising the VSC-HVDC.

27.8.2.1 AC Shunt RLC-Filters

Switching of high-power, high-frequency switches generates harmonics in the converter output voltages and currents. The order of harmonics generated is directly related to the PWM switching frequency of the semiconductor switches.

Single- or double-tuned low-pass and high-pass damped RLC filters are connected to suppress these harmonics. The frequency modulation index is defined as m_f that is defined as the ratio of the switching frequency of the converter to the fundamental frequency of the AC voltage. In the case of three-phase VSC, the harmonics in the line-to-line voltages are present. The odd harmonics exist as sidebands, centered around the m_f and its multiples where m_f is odd. The value of m_f is chosen such that it should be an odd integer to eliminate the even harmonics; also, if it is a multiple of 3, then most of the triplen harmonics are canceled out in the line-to-line voltage.

27.8.2.2 Converter Transformer

A converter transformer interfaces the VSC AC terminals to AC network with suitable voltage level at both sides. It provides electric isolation and operates as a filter between converter and AC networks and provides the appropriate AC voltage level to optimize the available converter valve voltage rating. Configuration and rating of the transformer can be decided from the total system power rating, converter topology, and specified requirements.

27.8.2.3 Voltage Source Converter

The VSC is the main building block of the VSC-HVDC system. The number of switches employed depends on the operating characteristic and voltage level required. The series-connected IGBT switches, connected with antiparallel diodes, make up a valve. Two valves are connected in series to make up the converter leg for one phase. VSC can operate as a rectifier or an inverter at either end depending on the current flow direction. Two converters can be connected as a back-to-back system to connect two different AC grids, DC transmission line, or overhead cables for bulk power transmission or underground cables for connection of offshore oil rigs, islands, or offshore wind farms. The six-switch converter comprises a group of six valves. Different types of PWM techniques are used to operate and control the converter switches. Typical IGBT has rating of 6.5 kV and 2.4 kA. The voltage across the IGBT switch in the ON state is typically in the range of 1–3 V that creates the ON state losses. The switching losses are the second major loss mechanism and are due to fact that, during the turn ON and turn OFF transition, current is still flowing while voltage is present across the device. In order to minimize the switching losses, the maximum switching frequency needs to be carefully considered. VSC is equipped with the RC snubbers and series R-L elements to reduce the dv/dt and di/dt stresses on the switches during ON/OFF transitions.

27.8.2.4 DC Transmission

The DC system can be in the form of a transmission line, with underground or overhead cables. The overhead cables can be used with a moderate size of towers. The extruded polymer cable is a newly developed technique in which the insulation is highly resistant to the DC voltage.

The DC transmission system adopted here is a bipolar transmission system in which the power can flow in both the overhead poles and ground is used as a return path in case of monopolar operation. In case of failure or preplanned maintenance of one pole, reduced power can still be transmitted using the other pole. Two smoothing inductors are connected on DC transmission system to reduce the ripples in the DC current.

27.8.2.5 DC Capacitors

As shown in Fig. 27.33, two series-connected DC capacitors of same size are employed across the DC terminals of converter with grounded midpoint. The size of the capacitor depends on the required DC voltage level and the acceptable DC ripple.

The DC voltage should be adequate for the generation of sinusoidal voltages on AC side of the converter. For the system to

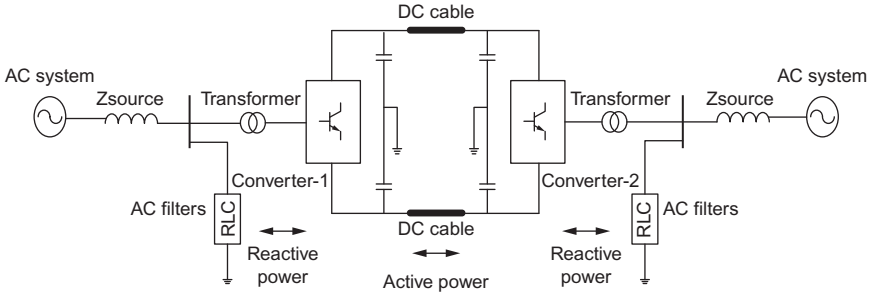


FIG. 27.33 Single-line diagram of VSC-HVDC system.

operate in the linear range of the PWM, the DC voltage should be 1.634 times the value of root mean square (RMS) AC voltage.

The PWM switching of high-power high-frequency switches generates the harmonics in the DC current flowing in the transmission line. This generates the harmonics in the DC voltage that is strongly related to the converter AC voltage. By evaluation of the magnitude of ripple and the switching frequency of the semiconductor switches, the DC side capacitor ratings can be finalized.

The value of DC capacitor C_{DC} used here can be small, which may result in a faster converter response. The energy stored in the capacitor is released during transients that will help to stabilize the power flow on the DC transmission system. The DC capacitor size is characterized with a time constant τ, which can be defined as the ratio between the energy stored in the capacitor at the rated DC voltage V_{DC} and the apparent power rating of the converter SC:

$$\tau = \frac{\frac{1}{2} C_{DC} V^2_{DC}}{S_C} \tag{27.6}$$

The time constant is equal to the time needed to charge the capacitor from zero to rated voltage V_{DC} if the converter is supplied with a constant active power equal to SC. The time constant τ can be selected to be small to satisfy ripple and transient overvoltage requirement on the DC voltage. A relatively small time constant allows fast control of active power and reactive power.

27.8.3 Topologies of the VSC

VSC can be divided into topologies according to the number of levels for converter output AC voltage, either two level or multilevel. These are explained in following subsections.

27.8.3.1 Two-Level Voltage Source Converter

A two-level bridge is the simplest circuit configuration that can be used to construct a three-phase VSC. It has been widely used in many applications for a range of power levels. As shown in Fig. 27.34, the converter can generate DC voltage waveform of only two values, $\pm V_{DC}/2$, where V_{DC} is the total DC voltage. Relatively simple power and control circuitry, small DC capacitor size, small footprint environmentally, and same semiconductor duty ratio are some of the advantages related to a two-level VSC.

27.8.3.2 Multi-level Voltage Source Converter VSC

Converter topologies with more than two-level voltages are known as multilevel converters. In this type of VSC, the output AC voltage waveform has different level according to the construction of the VSC. The main requirement for multilevel converters is to synthesize a sinusoidal voltage from several voltage levels that are obtained from the DC side capacitor voltages. Multilevel VSCs are divided into different types according to their application. The multilevel VSC found various

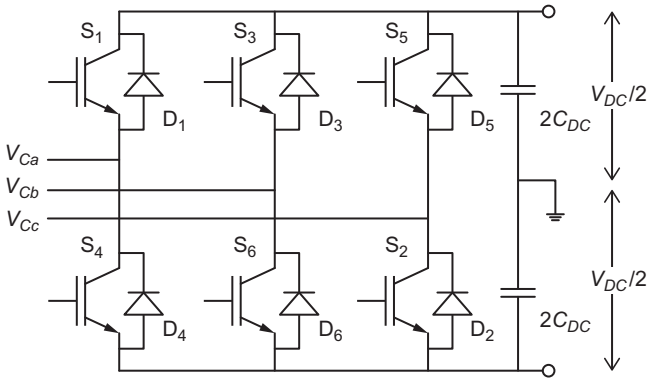


FIG. 27.34 Two-level, six-switch, three-phase converter topology.

applications in power systems due to its high power density, excellent performance, and high reliability. Various multilevel topologies are explained next.

27.8.3.3 Neutral Point Diode Clamped VSC

Neutral-point diode-clamped VSC topology is shown in Fig. 27.35. As shown, this topology uses clamping diodes to limit the dynamic and static overvoltages of switching devices. The clamping diodes are connected to the center point of the DC bus capacitor.

The advantages of this topology include reasonable small size of the DC capacitors, small footprint environmentally, and good quality AC output waveform. An n-level diode-clamp converter typically consists of (n-1) capacitors on the DC bus and produces n-levels of the converter output AC voltage. With a higher number of levels, harmonics generation is very low that can even avoid the need for filters in some cases. The disadvantages are related to voltage balancing across the DC capacitors, uneven loss distribution between devices, and excessive clamping diodes necessity in higher levels.

27.8.3.4 Flying Capacitor VSC

Fig. 27.36 shows the three-level flying-capacitor-type VSC topology. This topology uses capacitors instead of diodes in

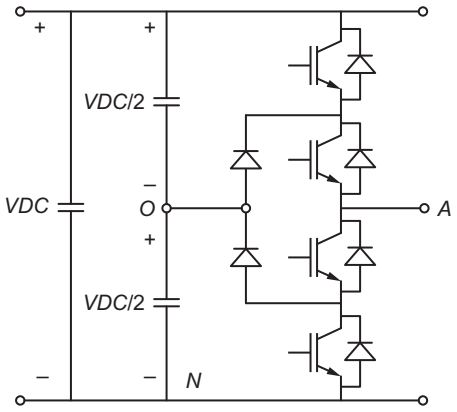


FIG. 27.35 Three-level, NPC converter topology.

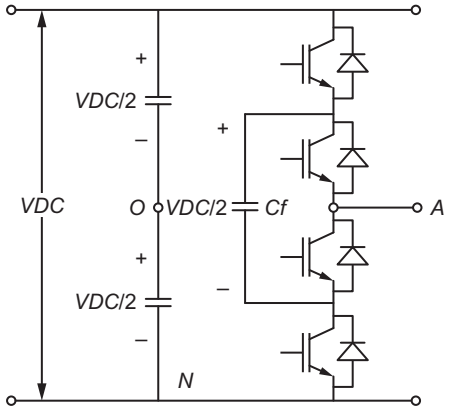


FIG. 27.36 Three-level, flying-capacitor converter topology.

the diode-clamped topology. For an n-level converter, $(n-1)$ numbers of DC capacitors at DC bus and $(n-1)\times(n-2)/2$ number of auxiliary capacitors per phase leg are required. These capacitors are known as floating capacitors.

The AC waveform synthesized by this topology is better than the diode-clamped topology. The advantages of this topology are the extra ride through capabilities during power outage and severe disturbances due to large number of storage capacitors, switch combination redundancy for balancing different voltage levels, and avoidance of harmonic filters in higher-level applications. The requirement of an excessive number of storage capacitors on DC side and across the semiconductor switches in higher number of levels makes this topology very expensive. The converter control system is complex, and switching losses are higher compared with diode-clamped topology.

27.8.3.5 ANPC (Actively Neutral Point Clamped) converter

Fig. 27.37 shows the three-level ANPC converter topology in which the clamping diodes are replaced by semiconductor switches. The disadvantage of uneven loss distribution across various devices in the neutral-point diode-clamped converter topology is mitigated by this newly developed topology.

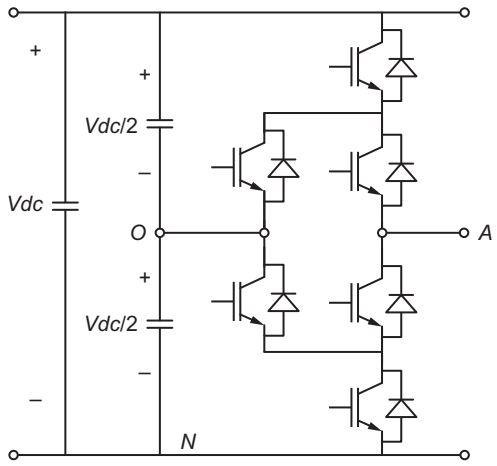


FIG. 27.37 Three-level, actively neutral-point-clamped converter topology.

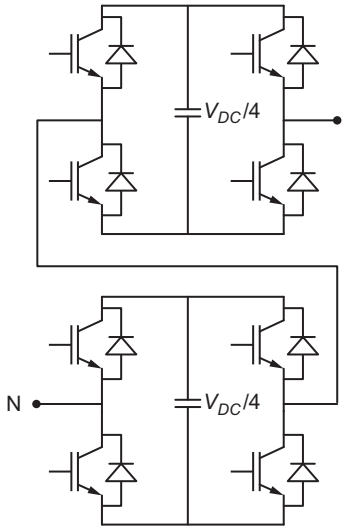


FIG. 27.38 Five-level, cascaded H-bridge converter topology.

27.8.3.6 Cascaded H-Bridge Converter

This VSC topology (Fig. 27.38) is a cascaded structure that consists of full-bridge inverter units connected in series.

Each unit is fed by a separate DC capacitor, and no other circuit to balance the voltage matching of the switching devices is necessary. There is no need to add the clamping diodes or voltage-balancing capacitors in this topology that results in a relatively simple construction. Main drawback of this topology is the requirement of several independent DC power supplies.

27.8.3.7 Multi-pulse Topologies

In a six-switch converter, the commutation of current takes place six times per cycle. In the case of 12-switch converter, two six-switch converters are connected in series to form a 12-switch converter topology. By using the six-switch converter, the additional multiswitch topologies in multiples of six can be created to form the required pulse level. The 24-switch and 48-pulse converters are implemented in some research papers for application as a STATCOM in power system. The main purpose of using these topologies is to reduce the voltage and current harmonics in the system. As the number of switches increases, the harmonic distortion in the system decreases proportionally.

27.8.4 PWM for VSC

PWM is the most accepted switching technique in which the comparison between a fundamental frequency modulating waveform and a fixed carrier frequency triangular waveform generates the firing pulses for VSC. The magnitude and phase

angle of the generated fundamental frequency component of the converter output AC voltage can be controlled by varying the magnitude and phase angle of the modulating waveform. In this technique, the converter output AC voltage contains harmonic frequency components in addition to fundamental frequency component located around the multiples of the triangular waveform carrier frequency.

27.8.4.1 Sinusoidal PWM

The PWM technique used for switching of the semiconductor devices of converter decides the frequency and nature of the converter output AC voltage. So to get the sinusoidal waveform as an output, sinusoidal PWM technique is used. The sinusoidal modulating waveform of 60 Hz system frequency is compared with a high-frequency triangular waveform to generate the pulse-width modulated firing pulses for converter. Two different SPWM methods can be implemented to get the required output.

(a) Bi-polar SPWM

In the case of bipolar sinusoidal PWM method, a single fundamental frequency modulating waveform per phase is compared with the high-frequency triangular waveform. The output voltage switches between $-V_{DC}/2$ and $+V_{DC}/2$ voltage levels where V_{DC} is the total DC voltage. It is the reason why this type of switching is called a bipolar PWM switching. As shown in Fig. 27.39, during comparison, when the sinusoidal waveform is greater than the triangular waveform, the PWM trigger signal is high, otherwise at lower level.

(b) Uni-polar SPWM

In the case of unipolar sinusoidal PWM technique, two same phase fundamental frequency modulating waveforms with opposite polarity are compared with the high-switching-frequency triangular waveforms. The output voltage switches between $+V_{DC}/2$ and 0 or between 0 and $-V_{DC}/2$. For this reason, this type of PWM scheme is called a PWM with a unipolar voltage switching.

27.8.5 VSC-HVDC Operation

The VSC-HVDC operation can be explained by considering its operating principle, four-quadrant operation in P-Q diagram, and capability to operate in either rectifier or inverter modes.

27.8.5.1 Operating Principle of VSC-HVDC

The VSC-HVDC operating principle can be explained from the SLD shown in Fig. 27.40, where two AC networks are connected by a VSC-HVDC transmission system.

The converter transformer connecting AC network and converter can be modeled as an equivalent series resistance and reactance. The transformer resistance is very small compared

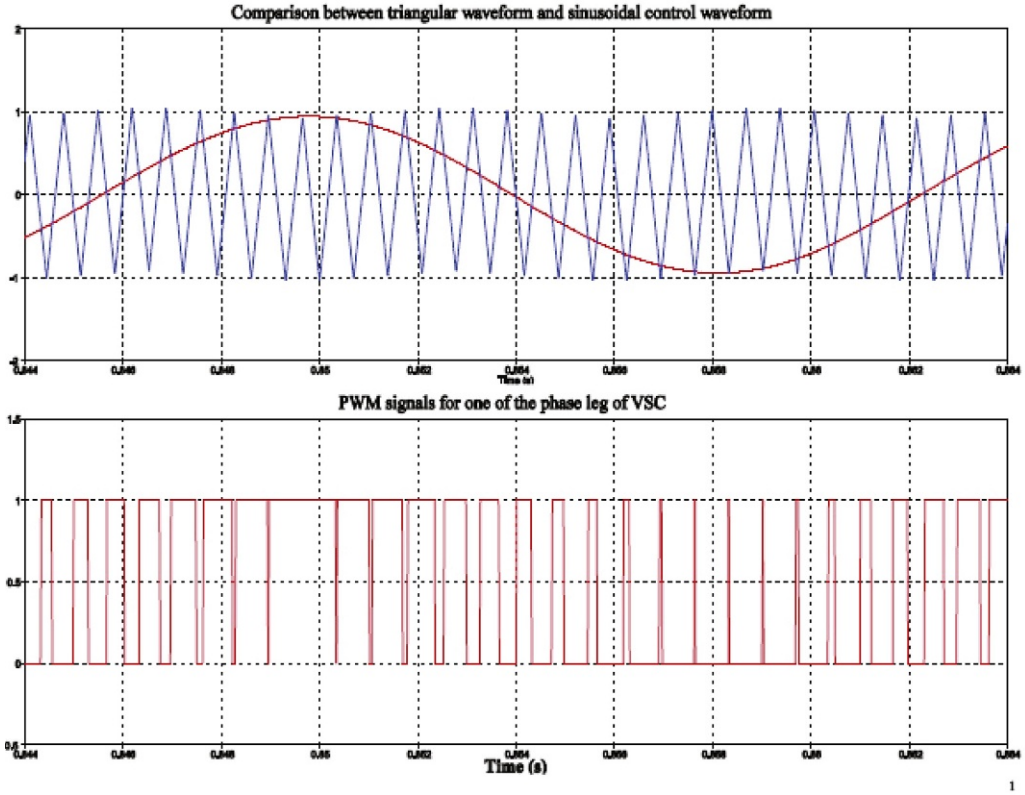


FIG. 27.39 Comparison between sinusoidal and triangular waveform and PWM signals.

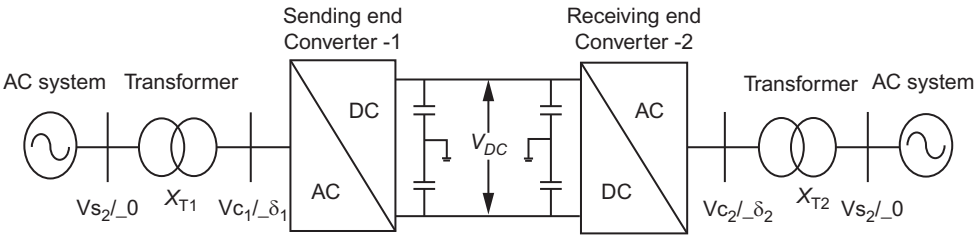


FIG. 27.40 Single-line diagram for VSC-HVDC operating principle.

with the transformer reactance, so it can be neglected in power calculations. The phase shift between both sides' voltages due to transformer reactance is responsible for active power flow. At sending end, the voltage V_{S1} at AC bus is considered as a reference, so the converter output AC voltage V_{C1} has phase shift δ_1 with respect to the bus voltage V_{S1}. The magnitude and phase angle of converter output AC voltage V_{C1} is controlled by the VSC control system. The active and reactive power flow between the AC system and the converter depends on the magnitude of the voltages at both sides of the transformer, the transformer reactance X_{T1} and the phase angle δ_1 between them. The active and reactive power flow between AC bus and converter AC terminals can be expressed as follows: the active power at sending end and receiving end is given by

$$P_S = \frac{|V_{S_1}||V_{C_1}| \times \sin\delta_1}{X_{T_1}},\ P_R = \frac{|V_{S_2}| \times |V_{C_2}| \times \sin\delta_2}{X_{T_2}} \tag{27.7}$$

The reactive power at sending end and receiving end is given by

$$\begin{aligned} Q_S &= \frac{|V_{S_1}|^2}{X_{T_1}} - \frac{|V_{S_1}| \times |V_{C_1}| \times \cos\delta_1}{X_{T_1}}, \\ Q_R &= \frac{|V_{S_2}| \times |V_{C_2}| \times \cos\delta_2}{X_{T_2}} - \frac{|V_{S_2}|^2}{X_{T_2}} \end{aligned} \tag{27.8}$$

The amplitude, phase angle, and frequency of fundamental component of converter output AC voltage V_{C1} and V_{C2} can be controlled using the SPWM technique. If the voltage at the DC side of the converter is V_{DC} that is assumed to be constant, then the fundamental frequency component of converter output AC voltage can be derived from the following equation:

$$Vc(t) = \frac{1}{2} V_{DC} M_i \sin(\omega t + \delta) \tag{27.9}$$

where V_{DC} is the voltage on DC side, ω is the angular frequency, M_i is modulation index, and δ is the phase angle between the converter output AC voltage and the AC bus voltage. *Mi* can be defined as the ratio of peak value of voltage of modulating waveform (fundamental frequency sinusoidal waveform) to the peak value of voltage of carrier waveform (switching-frequency triangular waveform). From Eq. (27.9), it is seen that the fundamental component of converter voltage depends on the variables *Mi*, angle δ, and frequency that are independently controlled by VSC controllers. The active and reactive power can be controlled by controlling the phase angle δ and the amplitude of the fundamental frequency component of converter AC output voltage V_C, respectively.

In a VSC-HVDC, the polarity of DC voltage is constant, so the power reversal is done by current reversal in the DC link. The current in DC link flows from higher to lower DC voltage level. For stable VSC operation and flow of active power, the DC-link voltage is maintained at a desired reference value by using a feedback control loop. The power flow to and from the AC source can be controlled according to the DC-link voltage requirements. The voltage V_{DC} is measured and controlled in such manner that the DC current flow can be in either direction depending on the requirement of active power flow direction.

27.8.5.2 Four Quadrant Operation of VSC

Active power flow direction for rectifier or inverter operation and reactive power flow direction for inductive or capacitive operating mode of VSC can be explained by a P-Q circle diagram shown in Fig. 27.41. The diagram explains the ability of VSC to operate in all four quadrants of P-Q circle and to achieve the independent control of active and reactive power.

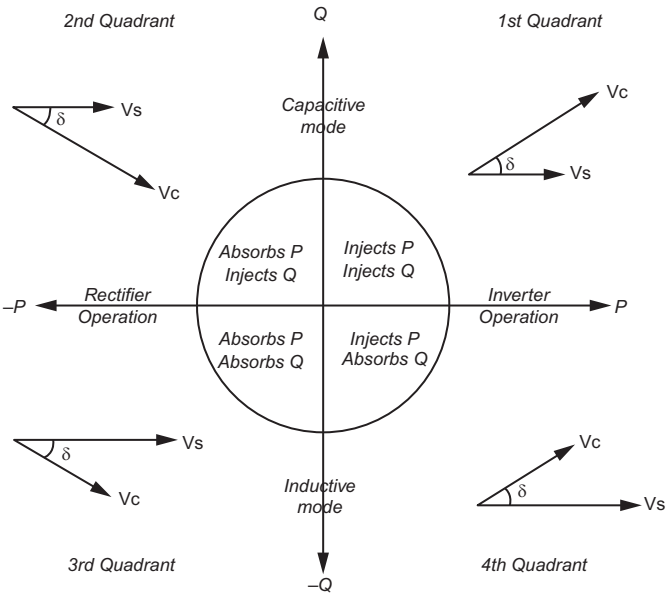


FIG. 27.41 P-Q circle diagram for VSC operation.

The direction of current flow and hence active power flow decides the rectifier or inverter operation of converter.

In the first quadrant, both the active and reactive powers are positive, which means that the converter injects both powers to AC system that shows the capacitive mode of inverter operation. The converter output AC voltage magnitude is higher than AC bus voltage and leads AC bus voltage by an angle δ.

In the second quadrant, the active power is negative, and the reactive power is positive, which explains the capacitive mode of rectifier operation. In this case, the converter output AC voltage amplitude is higher than AC bus voltage, but it lags the AC bus voltage by an angle δ.

Both the powers in the third quadrant are negative that means the converter absorbs both powers from the AC system, which explains the inductive mode of rectifier operation. In this case, the AC bus voltage magnitude is higher than the converter output AC voltage, and it leads by an angle δ.

In the fourth quadrant, the active power is positive, and the reactive power is negative, which explains the inductive mode of inverter operation. Here, the converter output AC voltage leads the AC bus voltage, but its magnitude is less than the AC bus voltage.

According to the converter MVA capacity and system requirements, converter can operate in any mode (i.e., capacitive or inductive) of rectifier or inverter operation.

27.8.5.3 Rectifier-Inverter Operation of VSC

The rectifier or inverter operation of VSC can be explained by considering Fig. 27.42. AC bus voltage V_S can be taken as a reference, and V_C is the converter AC output voltage with phase shift δ. The converter transformer can be represented by an equivalent resistance R_T and reactance X_T. Two capacitors of same rating $2C_{DC}$ are connected in series across the DC terminals of the converter. The direction of current flow decides the operation of VSC as a rectifier or inverter.

As shown in Fig 27.43, the AC system voltage V_S leads the converter AC output voltage V_C by an angle δ. The active power flows from the AC system to the converter, so the converter operates as a rectifier. As shown in the figure, ΔV is the voltage drop across the transformer impedance that is controlled in order to control the angle δ. In the rectifier mode of operation, the current I_{DC} is considered positive, and the capacitor C_{DC} is discharged through the DC transmission system. The error signal demands the control circuit for more power from the AC supply. The control circuit thereby generates the appropriate PWM signals for the switching devices, and accordingly, more current flows from the AC to DC side, and the capacitor voltage recovers its predefined value.

As shown in Fig. 27.44, the AC system voltage V_S lags the converter AC output voltage by an angle δ. In this case, the active power flows from the converter to AC system, so the converter operates as an inverter. In the inverter mode of operation, I_{DC} becomes negative, and the capacitor C_{DC} is overcharged. The error signal demands the controls to discharge the capacitor C_{DC} and return power to the AC system. The PWM can control both the active power and reactive power independently. Thus, this type of converter can be used for power factor correction also in addition to power transmission.

Depending on the control strategy, VSC can be operated as either inverter or rectifier; therefore, it is often referred to as a converter. Two such converters are often cascaded to control the power flow between two AC networks. The first converter converts AC voltage to variable DC-link voltage, and the second converter converts the DC voltage to variable AC voltage with fixed or variable frequency.

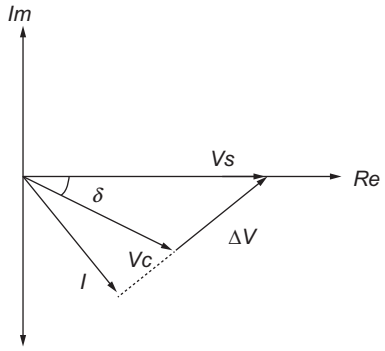


FIG. 27.43 VSC operation as a rectifier.

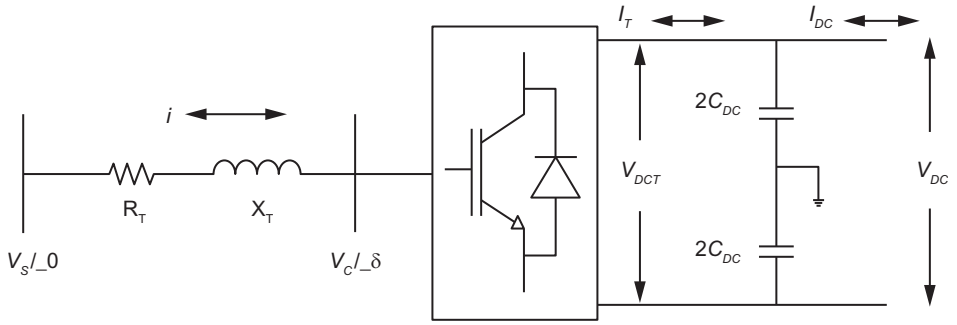


FIG. 27.42 VSC operation as rectifier or inverter.

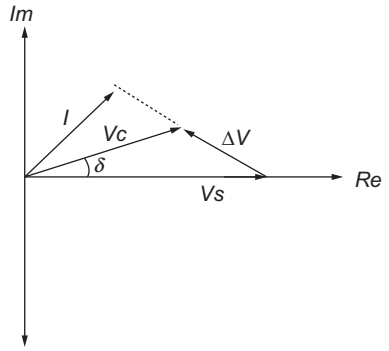


FIG. 27.44 VSC operation as an inverter.

27.8.6 Summary

In this chapter, the VSC-HVDC system construction, its principle of operation, and operational function of each component are explained in detail. The different topologies of VSC and PWM techniques are explained. The principle of operation for the VSC-HVDC is explained regarding the active and reactive power flow. P-Q circle diagrams are explained regarding the rectifier/inverter operation and capacitive or inductive mode of operation.

27.9 Control of VSC-HVDC System

27.9.1 Introduction

VSC-HVDC transmission system has flexibility in terms of controlled quantities offering two degrees of freedom at each end to provide stable and robust control. As described in Section **27.8.5**, VSC-HVDC system has advantage of independent control of active and reactive power. The direction of active power flow can be changed without changing the DC voltage polarity. The reactive power can be controlled independently at either converter station by controlling converter AC output voltage.

Although both current and voltage control schemes are possible, current control is generally preferred for its excellent dynamic characteristics and inherent overcurrent limitation capabilities. When current control is used, the rectifier input current and inverter output currents are measured and compared with reference signals; the current errors are used as inputs to the PWM modulator, which then provides the required switching signals. The requirements for the control system to operate the VSC-HVDC system are the following:

- It must be capable of controlling the desired active power in either direction.
- The reactive power of system must be controlled independently at both ends.
- The DC voltage must be maintained at desired level for power transfer.

The control modes are chosen according to the application and requirement of the given power system. The rectifier and inverter controllers take the control of any two of above-mentioned four control strategies according to the system requirements and operating conditions. VSC_1 controllers operate on active power and reactive power control, whereas VSC_2 controllers deal with DC voltage and reactive power control (Fig. 27.45).

27.9.2 Direct Control Method

Direct control method is a simple method for the control of VSC-HVDC. The angle *d* and modulation index *Mi* are controlled directly by using PI controllers. The measured values are compared with the reference values, and the resultant errors are fed to the PI controllers. The output of which is used as either modulation index or angle delta. The modeling of direct control system is provided in Section **27.9.5.3**. Though this method is not used in practical applications, it is useful in comparative studies of operation and performance of VSC-HVDC.

27.9.3 Vector Control Method

The P and Q controlled quantities of VSC-HVDC are coupled to each other such that any change in one quantity strongly affects the other. The vector control method removes the coupling between these quantities to ensure the independent

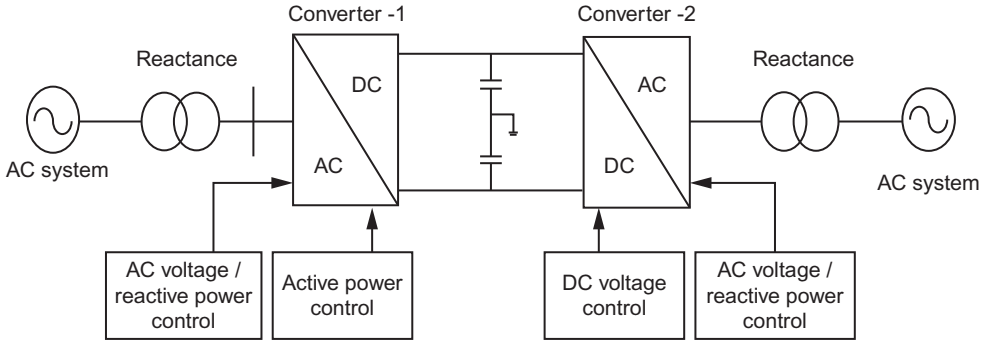


FIG. 27.45 VSC-HVDC control system.

control of each quantity. The vector control strategy consists of a cascade control system with faster inner controllers. The vector controller is accomplished by additional outer current controller that provides the reference values for inner controller. The outer controllers include active power controller, reactive power controller, AC voltage controller, DC voltage controller, or frequency controller where the implementation of particular control strategy depends on the application and operating conditions of VSC-HVDC system. It is not possible to implement all the control strategies at the same time and requires an extensive system operation and performance studies for implementation of particular control method.

For feeding the passive system at receiving end without any local voltage source, it is necessary to control the frequency and AC voltage, whereas the active power and reactive power control is required in active AC system. However, since the active power flow into the DC link must be balanced, the DC voltage controller is necessary in any case to achieve active power balance. On the DC side, the active power input to the DC link must equal the active power output from the DC link plus the losses in the DC link. Any difference would result in a change in the DC voltage.

In order to understand the vector control technique of the VSC-HVDC transmission system, the mathematical model for VSC-HVDC system needs to be derived. The vector control strategy can be derived from the mathematical modeling of the system shown in Fig. 27.46.

The AC filters connected to the VSC-HVDC system behave as pure capacitors at fundamental frequencies. Hence, in the mathematical model presented here, the filter resistances and inductances can be neglected. From the single-line diagram (Fig. 27.46), the voltage across the transformer, the current to the filter, and the voltage across the source impedance can be obtained in three-phase instantaneous form as follows:

The voltage across the source impedance is

$$Vac(t)_{abc} - Vs(t)abc = Rsi_S(t)_{abc} + Ls\frac{d}{dt}i_S(t)_{abc} \tag{27.10}$$

The current through the filters is

$$i_S(t)_{abc} - i_t(t)_{abc} = C_f\frac{d}{dt}Vs(t)_{abc} \tag{27.11}$$

The voltage across the transformer is

$$Vs(t)_{abc} - Vc(t)_{abc} = R_T i_t(t)_{abc} + L_T\frac{d}{dt}i_S(t)_{abc} \tag{27.12}$$

From Eqs. (27.10)–(27.12), the following differential equations can be derived:

$$\frac{d}{dt}i_S(t)_{abc} = -\frac{Rs}{L_S}i_S(t)_{abc} + \frac{1}{Ls}\left\{Vac(t)_{abc} - Vs(t)_{abc}\right\} \tag{27.13}$$

$$\frac{d}{dt}Vs(t)_{abc} = \frac{1}{C_f}i_S(t)_{abc} - \frac{1}{C_f}i_t(t)_{abc} \tag{27.14}$$

$$\frac{d}{dt}is(t)_{abc} = -\frac{R_T}{L_T}i_t(t)_{abc} + \frac{1}{L_T}\left\{Vs(t)_{abc} - Vc(t)_{abc}\right\} \tag{27.15}$$

By using Clarke's transformation matrix, quantities from ABC frame can be converted to αβ reference frame as follows:

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & \cos\gamma & \cos 2\gamma \\ 0 & \sin\gamma & \sin 2\gamma \end{bmatrix}\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{27.16}$$

where $\gamma = 2\pi/3$.

Eqs. (27.13)–(27.15) can be converted in to αβ frame as follows:

$$\frac{d}{dt}i_S(t)_{\alpha\beta} = -\frac{Rs}{L_S}i_S(t)_{\alpha\beta} + \frac{1}{Ls}\left\{Vac(t)_{\alpha\beta} - Vs(t)_{\alpha\beta}\right\} \tag{27.17}$$

$$\frac{d}{dt}Vs(t)_{\alpha\beta} = \frac{1}{C_f}i_S(t)_{\alpha\beta} - \frac{1}{C_f}i_t(t)_{\alpha\beta} \tag{27.18}$$

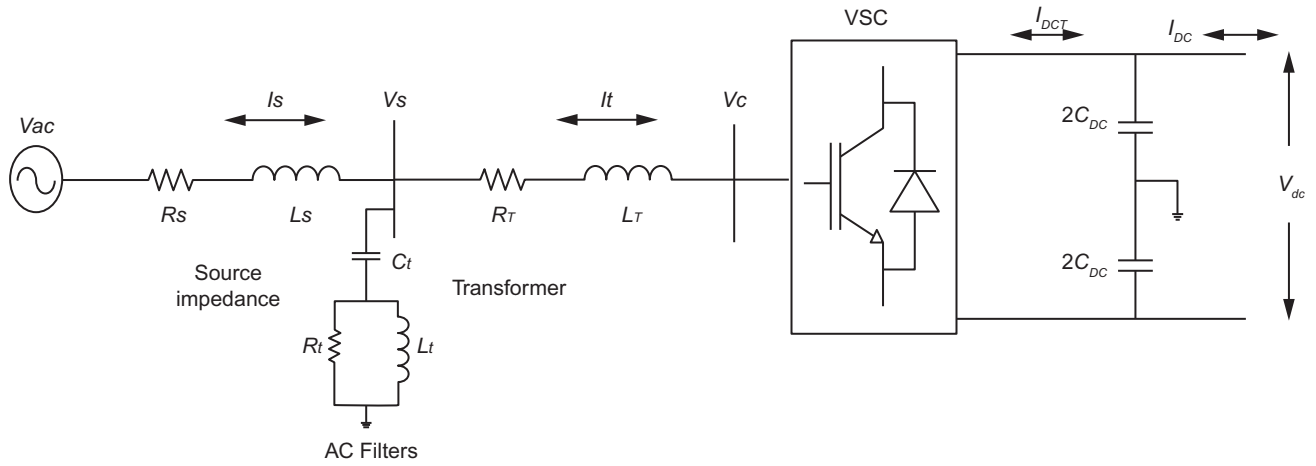


FIG. 27.46 Vector control system of VSC-HVDC system.

$$\frac{d}{dt}is(t)_{\alpha\beta} = -\frac{R_T}{L_T}i_t(t)_{\alpha\beta} + \frac{1}{L_T}\left\{Vs(t)_{\alpha\beta} - Vc(t)_{\alpha\beta}\right\} \quad (27.19)$$

By using the transformation angle θ derived from a phase-locked loop (PLL), the above equations are further transferred to the synchronously rotating dq reference frame, using Park's transformation, as follows:

$$\begin{bmatrix} x_d \\ x_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \quad (27.20)$$

$$\frac{d}{dt}i_S(t)_{dq} = -\frac{Rs}{L_S}i_S(t)_{dq} - j\omega i_S(t)_{dq} + \frac{1}{L_S}\left\{Vac(t)_{dq} - Vs(t)_{dq}\right\} \quad (27.21)$$

$$\frac{d}{dt}Vs(t)_{dq} = \frac{1}{C_f}i_S(t)_{d_q} - \frac{1}{C_f}i_t(t)_{dq} - j\omega Vs(t)_{dq} \quad (27.22)$$

$$\frac{d}{dt}is(t)_{dq} = -\frac{R_T}{L_T}i_t(t)_{dq} - j\omega i_t(t)_{dq} + \frac{1}{L_T}\left\{Vs(t)_{dq} - Vc(t)_{dq}\right\} \quad (27.23)$$

The AC filter voltage, the current through the transformer, and the AC side voltage of VSC can be expressed as

$$Vs(t)_{dq} = -L_S\frac{d}{dt}i_S(t)_{dq} - R_S i_S(t)_{d_q} - j\omega L_S i_S(t)_{dq} + Vac(t)_{dq} \quad (27.24)$$

$$i_t(t)_{dq} = i_S(t)dq = C_f\frac{d}{dt}Vs(t)_{dq} - j\omega C_f Vs(t)_{dq} \quad (27.25)$$

$$Vc(t)_{dq} = -L_S\frac{d}{dt}i_t(t)_{dq} - R_T i_S(t)_{dq} - j\omega L_T i_S(t)_{dq} + Vs(t)_{dq} \quad (27.26)$$

From Eq. (27.26), the dq current component through the transformer can be given as

$$\frac{d}{dt}i_t(t)_d = \omega i_t(t)_q + \frac{Vs(t)_d - Vc(t)_d}{L_T} - \frac{R_T}{L_T}i_t(t)_d \quad (27.27)$$

$$\frac{d}{dt}i_t(t)_q = \omega i_t(t)_d + \frac{Vs(t)_q - Vc(t)_q}{L_T} - \frac{R_T}{L_T}i_t(t)_q \quad (27.28)$$

Eqs. (27.27) and (27.28) present the relationship between input reference current and converter output AC voltage in dq reference frame.

27.9.4 Limitations

The VSC-HVDC link with its semiconductor switches has a limited overload capacity. Large transient currents due to system disturbances can stress or damage the converter valves. Therefore, a current limit must be implemented in the control system. Moreover, since the maximum voltage amplitude out of the VSC is limited by the VSC voltage capability, the produced reference voltage from the vector controller must be appropriately limited. The current limit I_{lim} is compared with the current magnitude computed from the active and reactive reference currents. When the current limit is exceeded, both the active and reactive reference currents have to be limited. The choice of how to limit both reference currents will depend on the application. For instance, if the converter is connected to a strong system, the active component of the reference current will be given priority, when the current limit is exceeded, to produce more active power. The produced active power is estimated from the equation:

$$P_{max} = \sqrt{{V_c}^2 {I_{lim}}^2} \quad (27.29)$$

If the converter is connected to a weak system or used to supply a bulk industrial user (or island), the VSC will give priority to the reactive component of the reference current to maintain the AC voltage when the current limit is exceeded. The remaining capacity is then available for active power production. The produced reactive and active power may be estimated from the following equations:

$$Q_{max} = V_c {I_{lim}}^{(q)}, P_{max} = \sqrt{{V_c}^2 {I_{lim}}^2 - {Q^2}_{max}} \quad (27.30)$$

where $I_{lim}^{(q)}$ is the preset maximum reactive reference current.

27.9.5 Outer Controller

The outer controller consists of the DC voltage controller, active power controller and reactive power controller. The proposed simulation model consists of active power and reactive power controllers at VSC_1 and DC voltage and reactive power controllers at VSC_2. The outer controller creates the reference values of the dq current components for inner current controllers. The outer controller gains are smaller when compared with the inner controller to ensure the stability of the complete system.

27.9.5.1 DC Voltage Controller

As shown in Fig. 27.46, the instantaneous active and reactive powers in dq reference frame at the AC side of the VSC and the power P_{DC} transmitted on the DC side of the VSC are expressed as

$$P = \frac{3}{2}\left(Vs_d \cdot i_d + Vs_q \cdot i_q\right) \quad (27.31)$$

$$Q = \frac{3}{2}\left(Vs_d \cdot i_d - Vs_q \cdot i_q\right) \quad (27.32)$$

$$P_{DC} = V_{DC} I_{DCT} \quad (27.33)$$

where I_{DCT} is the current flowing in the DC terminals of the VSC.

During steady-state operation, the dq components of voltages are constant at the rated values. Therefore, the voltage Vs_d is rated voltage Vs, and Vs_q is zero. By considering the above assumptions, the active and reactive powers are expressed as follows:

$$P=\frac{3}{2}(V_S i_d), Q=\frac{3}{2}(V_S i_q) \tag{27.34}$$

If the losses in the converter transformer and converter are neglected, the power at the AC and DC sides can be considered equal, that is,

$$\frac{3}{2}(V_s i_d) = V_{DC} I_{DCT} \tag{27.35}$$

Hence,

$$I_{DCT} = \frac{3}{2}\frac{(Vsi_d)}{V_{DC}} \tag{27.36}$$

The current in the DC line of the VSC is given as

$$I_{DCT} = C_{DC}\frac{dV_{DC}}{dt} + I_{DC} \tag{27.37}$$

Any imbalance between the AC and DC powers leads to a change in voltage at the DC-link capacitors, which is given as

$$C_{DC}\frac{dV_{DC}}{dt} = I_{DCT} - I_{DC} \tag{27.38}$$

where I_{DCT} is the current in the DC terminals of the VSC, C_{DC} is the total DC side capacitance, V_{DC} is the DC voltage across the capacitor, and I_{DC} is the DC current flowing through the transmission line. The value of DC current from Eq. (27.37) can be used in Eq. (27.35), that is,

$$\frac{3}{2}(V_S i_d) = V_{DC}\left(C_{DC}\frac{dV_{DC}}{dt} + I_{DC}\right) \tag{27.39}$$

$$C_{DC}\frac{dV_{DC}}{dt} = \frac{3}{2}\frac{Vsi_d}{V_{DC}} - I_{DC} \tag{27.40}$$

From Eq. (27.39), the value of the reference current $i_d{}^*$ is derived as follows:

$$i_d{}^* = \frac{2}{3}\frac{V_{DC}}{V_S}\left(C_{DC}\frac{dV_{DC}}{dt} + I_{DC}\right) \tag{27.41}$$

The d-component of the current derived Eq. (27.41) gives the reference current for the inner current controller for DC voltage control.

27.9.5.2 Active Power Controller

The active current reference is obtained from Eq. (27.34):

$$i_d{}^* = \frac{2}{3}\frac{P_{ref}}{V_S} \tag{27.42}$$

where P_{ref} is the reference active power. For accurate control of the active power, a combination of a feedback loop and an open loop is used:

$$i_d{}^* = \frac{2}{3}\frac{P_{ref}}{V_S} + \left(K_{p1} + \frac{K_{i1}}{s}\right)\left(P_{ref} - P_{actual}\right) \tag{27.43}$$

where K_{p1} and K_{i1} are the proportional and integral gains, respectively, of the active power controller.

27.9.5.3 Reactive Power Controller

A reactive power controller similar to the active power controller is obtained from Eq. (27.34) as

$$i_q{}^* = \frac{2}{3}\frac{Q_{ref}}{V_S} \tag{27.44}$$

where Q_{ref} is reference reactive power. Again, same method is used to combine a feedback loop with an open loop:

$$i_q{}^* = \frac{2}{3}\frac{Q_{ref}}{V_S} + \left(K_{p2} + \frac{K_{i2}}{s}\right)\left(Q_{ref} - Q_{actual}\right) \tag{27.45}$$

where Kp_2 and Ki_2 are the proportional and integral gains, respectively, of the reactive power controller.

Fig. 27.47 shows active and reactive power control system for VSC_1. The control block of PLL is shown from which the synchronization angle θ is derived and fed to the ABC to dq block.

27.9.6 Summary

This chapter deals with the control system of VSC-HVDC transmission system. Two different control systems, direct control and vector control, are explained. The VSC-HVDC mathematical model is provided in this chapter. Block diagram of active power and reactive power control systems in vector control technique is also provided here.

27.10 HVDC System Simulation Techniques

Modern HVDC systems incorporate complex control and protection features. The testing and optimization of these features require powerful tools that are capable of modeling all facets of the system and have the flexibility to do the evaluation in a rapid, effective, and cost-efficient manner.

27.10.1 DC Simulators and TNAs [9]

For decades, this has been achieved with the aid of physical power system simulators or transient network analyzers (TNAs) that incorporate scaled physical models of all power

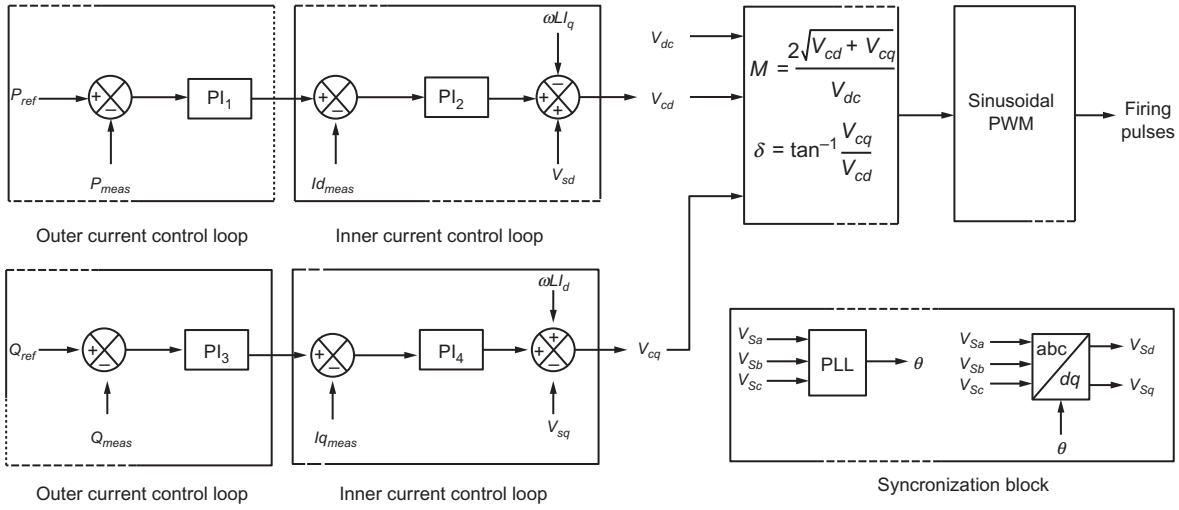


FIG. 27.47 Active and reactive power control system.

system elements (three-phase DC network lines/cables, sources as emf behind reactances, model circuit breakers for precisely timed AC system disturbances, transformers (system and convertor transformers with capacity to model saturation characteristics), filter capacitors, reactors, resistors, arrestors, and machines). Until the 1970s, these were built with analog components. However, with the developments in microprocessors, it is now feasible to utilize totally digital simulators operating in real time for even the most complex HVDC system studies. Most simulator operating scale are in the range 20–100 V DC and 0.2–1 A AC and at power frequency of 50 or 60 Hz. The stray capacitances and inductances are, however, not normally represented since the simulator is primarily used to assess control system behavior and temporary overvoltages of frequencies below 1000 Hz. Due to the developments of flexible AC transmission system (FACTS) application, most modern simulators now include similarly scaled models of HVDC converters, static compensators, and other thyristor-controlled equipment. The controls of these equipments are usually capable of realistic performance during transients such as the AC faults and commutation failure. The limited availability of adequate models of some of the system elements restricts the scope of the studies that can be completed entirely by means of the simulator. Due to the scaling problems, the losses in the simulator may be disproportionately high and need to be partly compensated by electronic circuits (negative resistances) to simulate appropriate damping of overvoltages and other phenomena.

27.10.2 Digital Computer Analysis

The main type of program employed for studies is an electromagnetic transient program (EMTP) that solves sets of differential equations by step-by-step integration methods. The digital program must allow for modeling of both the linear and nonlinear components (single and three phase) and of the topological changes caused, for example, by valve firing or by circuit-breaker operation. Detailed modeling of the converter control system is necessary depending on the type of study.

EMTP has become an industry standard analysis tool for power systems and is widely used. The program has had a checkered history, and numerous variants have appeared. Initially, the development of the program was supported by the Bonneville Power Administration (BPA). Some of the drawbacks in the capabilities of EMTP became more pronounced as the modeling of flexible AC transmission system (FACTS) with power electronic switches and voltage-source converters became more desirable.

Some of the drawbacks of the original EMTP version were the following:

1. The use of a fixed timestep that did not take into account the relatively long periods of inaction during nonswitching events. This results in unnecessarily long simulation times and huge amounts of data to be manipulated. This is particularly problematic for simulating power electronic converters.
2. The use of a fixed timestep results in the modeled switches chopping inductive currents that causes numerical oscillations. The use of artificial RC "snubbers" helped to alleviate some of these problems. The choice of the snubber capacitor was a function of the magnitude of the current to be chopped and the timestep size.
3. The use of the trapezoidal integration method results in numerical oscillations when the network admittance matrix to be inverted becomes singular. This is the direct result of modeling switches as truly either ON or OFF without representation of their intermediate nonlinear characteristics.

4. The requirement of a one timestep delay between the main program and the TACS subroutine for control simulation.
5. The use of new voltage-source converters with multiple switchings per cycle made the problem of switching "jitter" much more evident.
6. The lack of user-friendly input and output processors.

In recent years, considerable effort has been made by the EMTP Development Coordination Group (DCG) to restructure the program. This has resulted in the latest version called the EMTP restructured version (RV) (see www.emtp.com). The entire code of the program has been rewritten, and graphic input and output processors have been added. A sample of the graphic input file is shown in Fig. 27.48.

The main advantage of digital studies is the possibility of correct representation of the damping present in the system. This feature permits more accurate evaluation of the nature and rate of decay of transient voltages following their peak levels in the initial few cycles and also a more realistic assessment of the peak current and total energy absorption of the surge arrestors. The digital program also allows modeling of stray inductances and capacitances and can be used to cover a wider frequency range of transients than the DC simulator.

The main disadvantage of the digital studies is the lack of adequate representation of commutation failure phenomena with the use of power electronic converters. However, with the increasing capacity of computers, this is likely to be overcome in the future.

The models used in the simulators and digital programs depend on the assumptions made and on the proper understanding of the component and system characteristics; therefore, they require care in their usage to avoid unrealistic results in inexperienced hands.

27.11 Concluding Remarks

HVDC technology is now mature, reliable, and accepted all over the world. From its modest beginning in the 1950s, the technology has advanced considerably and maintained its leading edge image. The encroaching technology of flexible AC transmission systems (FACTS) has learned and gained from the technological enhancements made initially by HVDC systems. FACTS technology may challenge some of the traditional roles for HVDC applications since the deregulation of the electric utility business will open up the market for increased interconnection of networks [7]. HVDC transmission has unique characteristics that will provide it with new opportunities.

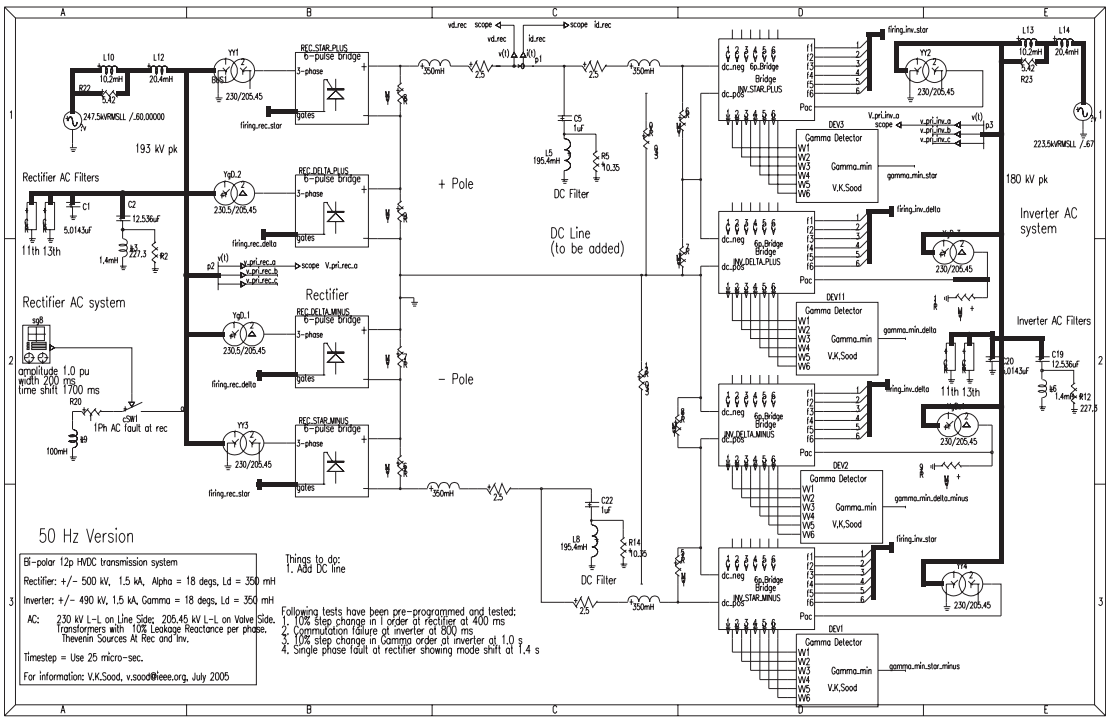


FIG. 27.48 A sample of the graphic input file of EMTP RV.

Although the traditional applications of HVDC transmission will be maintained for bulk power transmission in places like China, India, S. America, and Africa, the increasing desire for the exploitation of renewable resources will provide both a challenge and an opportunity for innovative solutions in the following applications:

- Connection of small dispersed generators to the grid
- Alternatives to local generation
- Feeding to urban city centers

Acknowledgments

The author pays tribute to the many pioneers whose vision of HVDC transmission has led to the rapid evolution of the power industry. It is not possible here to name all of them individually.

A number of photographs of equipment have been included in this chapter, and I thank the suppliers (Mr. P. Lips of Siemens and Mr. R. L.Vaughan from ABB) for their assistance in getting clearances.

I also thank my wife Vinay for her considerable assistance in the preparation of this manuscript.

References

[1] E.W. Kimbark, Direct Current Transmission—Volume I, Wiley Interscience, ISBN 0-471-35550-X, 1971.

[2] J. Arrillaga, High Voltage Direct Current Transmission, second ed., The Institution of Electrical Engineers, ISBN 0-85296-941-4, 1998.

[3] K.R. Padiyar, HVDC Power Transmission Systems—Technology and System Interactions, John Wiley & Sons, ISBN 0-470-21706-5, 1990.

[4] D. Melvold, HVDC Projects Listing, Prepared by IEEE DC and Flexible AC Transmission Subcommittee, 1965.

[5] J. Ainsworth, The phase-locked oscillator—a new control system for controlled static converters, IEEE Trans. Power Appar. Syst. PAS-87 (3) (1968) 859–865.

[6] A. Ekstrom, G. Liss, A refined HVDC control system, IEEE Trans. Power Appar. Syst. PAS-89 (5/6) (1970) 723–732.

[7] V.K. Sood, HVDC and FACTS Controllers—Applications of Static Converters in Power Systems, Kluwer Academic Publishers, ISBN 1-4020-7890-0, 2004.

[8] L. Carlsson, G. Asplund, H. Bjorklund, H. Stomberg, Recent and future trends in HVDC converter station design" in: IEE 2nd International Conference on Advances in Power System Control, Operation and Management, Dec. 1993, Hong Kong, 1993, pp. 221–226.

[9] C. Gagnon, V.K. Sood, J. Belanger, A. Vallee, et al., Hydro-Québec power system simulator, IEEE Canadian Rev. (19) Spring-Summer 1994, 6–9.

28

Flexible AC Transmission Systems

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28.1 Introduction

In 1988, Hingorani [1] published a paper entitled "Power Electronics in Electric Utilities: Role of Power Electronics in Future Power Systems," proposing the extensive use of power electronics for the control of ac systems, which resulted in the flexible ac transmission system or the FACTS concepts [2]. The basic idea was to obtain ac systems with a high level of control flexibility, as in high-voltage direct current (HVDC) systems [3] based on the use of the thyristor and the self-commutated (controllable turn-on and turn-off) silicon (Si) semiconductor devices, such as gate turn-off thyristors (GTOs), insulated gate bipolar transistors (IGBTs), and integrated gate-controlled thyristors (IGCTs) [4,5], or silicon carbide (SiC)-based devices [6], which were not yet developed at that time.

The switching characteristics of thyristors—controlled turn-on and natural turn-off—are appropriate for using in line-commutated converters, such as in conventional HVDC transmission systems with a current source in the dc side. In this application, the technology for series connection of thyristors is very important due to the high-voltage characteristics of the transmission voltage. This is a well-known technology.

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Maximum breakdown voltage and current conduction capabilities are around 8 kV and 4 kA, respectively. These are some features that make thyristors important for very high-power applications, although they present some serious drawbacks, such as the lack of controlled turn-off capability and low switching speeds.

Self-commutated switches are adequate for use in converters where turn-off capability is necessary. The device with highest ratings in this group was, for a long time, the GTO with maximum switching capability of 6 kV and 6 kA. At present, there are IGBTs with ratings in the range of 6.5 kV to 3 kA and IGCTs with switching capability of about 6 kV and 4 kA. The GTOs and IGCTs are devices that normally need small inductor for limiting the rate of change of turn-on current (di/dt). Normally, GTOs also need a snubber circuit for limiting the rate of change of voltage (dv/dt).

The GTOs, IGCTs, and IGBTs are the most used options for self-commutated high-power converters. Because the switching time of these devices is in the microsecond range (or below), their series connection is more complicated than in the case of thyristors. However, there are examples of series connections of various GTOs or IGCTs, and in the case of IGBTs, the number of series connected devices can go as high as 32 [7]. It is worth to note that GTOs are not used in new projects anymore.

Because of the commutation nature of the thyristors, the converters used in HVDC systems are of the current source type [8]. On the other hand, the force-commutated converters using the self-commutated devices are basically of the voltage source type. More details about current source and voltage source converters can be found in many power electronics books, for example, Refs. [3,8].

28.2 Ideal Shunt Compensator

A simple and lossless ac system is composed of two ideal generators, and a short transmission line, as shown in Fig. 28.1, is considered as basis to the discussion of the operating principles of a shunt compensator [9]. The transmission line is modeled by an inductive reactance X_L. In the circuit, a continuously controlled voltage source is connected in the middle of the transmission line. It is assumed that the voltage phasors V_S and V_R have the same magnitude, V, and are phase-shifted by δ. The subscript "S" stands for "source" and "R" stands for "receptor." Fig. 28.2 shows the phasor diagram of the system given in Fig. 28.1 in which the compensation voltage phasor V_M has also the same magnitude as V_S and V_R, and its phase is exactly $(-\delta/2)$ with respect to V_S and $(+\delta/2)$ with respect to V_R.

In this situation, the current I_{SM} flows from the source and the current I_{MR} flows into the receptor. The phasor I_M is the resulting current flowing through the ideal shunt compensator; Fig. 28.2 shows that this current I_M, in this case, is orthogonal to the voltage V_M, which means that the ideal shunt compensator voltage source does not have to generate or absorb active power and have only reactive power in its terminals.

From Fig. 28.2 and knowing that no active power flows to or from the ideal shunt compensator, it is possible to calculate the power transferred from V_S to V_R that is given by

$$P_S = \frac{2V^2}{X_L}\sin(\delta/2) \tag{28.1}$$

where P_S is the active power flowing from the source.

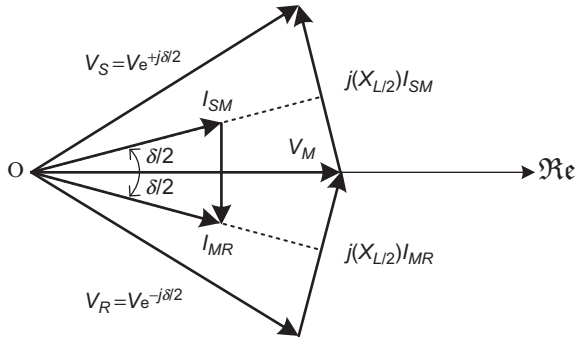


FIG. 28.2 Phasor diagram of the system with shunt reactive power compensation.

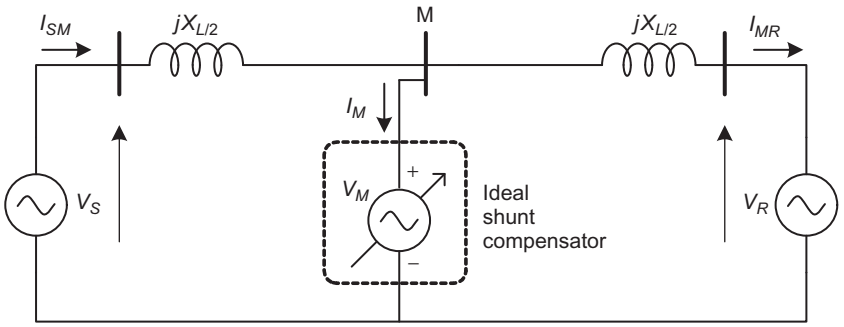


FIG. 28.1 Ideal shunt compensator connected in the middle of a transmission line.

If the ideal shunt compensator were not present, the transferred power would be given by

$$P_S = \frac{V^2}{X_L}\sin\delta \tag{28.2}$$

Since $2\sin(\delta/2)$ is always greater than $\sin\delta$ for δ in the range of $[0, 2\pi]$, the ideal shunt compensator does improve the power transfer capability of the transmission line. This voltage source is in fact operating as an ideal reactive power shunt compensator.

If the phase angle between V_M and V_S is different from $\delta/2$ (as shown in Fig. 28.3), the power flowing through V_M has both active and reactive components.

With the characteristics of the ideal shunt compensator, presented above, it is possible to synthesize power electronic-based devices to operate as active or reactive power compensators. This is discussed in the following sections. It will be seen that the requirements of the device synthesis with actual semiconductor switches for the situations of reactive or active power compensation are different because of the need of energy storage element or energy source if active power is to be drained or generated by the shunt compensator.

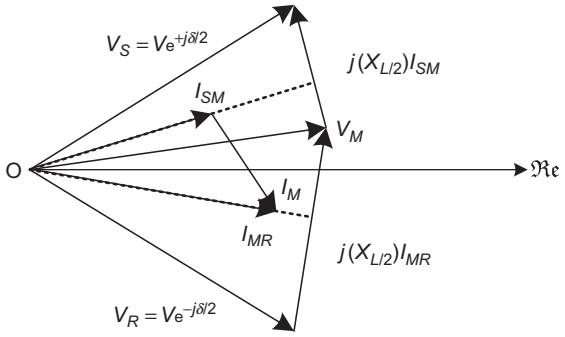


FIG. 28.3 Phasor diagram of the system with shunt reactive and active power compensation.

28.3 Ideal Series Compensator

Similar to the previous section, the ideal series compensator is modeled by a voltage source for which the phasor is V_C connected in the middle of a lossless transmission line as shown in Fig. 28.4

The current flowing through the transmission line is given by

$$I = (V_{SR} - V_C)/jX_L \tag{28.3}$$

where $V_{SR} = V_S - V_R$.

If the ideal series compensator voltage is generated in such a way that its phasor V_C is in quadrature with line current I, this series compensator neither supplies nor absorbs active power. As discussed earlier, power at the series source is only reactive, and the voltage source may, in this particular case, be replaced by capacitive or inductive equivalent impedance. Then, the equivalent impedance is given by

$$X_{eq} = X_L(1+s) \tag{28.4}$$

where

$$s = \frac{X_{Comp}}{X_L};\ \ (0 \le |s| \le 1) \tag{28.5}$$

is the compensation factor and X_{Comp} is the series equivalent compensation reactance, negative if capacitive and positive if inductive. In this case, the compensation voltage is given by

$$V_C = jX_{eq}I_L \tag{28.6}$$

and the transmitted power is equal to

$$P_s = \frac{V^2}{X_L(1-s)}\sin\delta \tag{28.7}$$

Eq. (28.7) shows that the transmitted power can be considerably increased by series compensation, choosing a proper

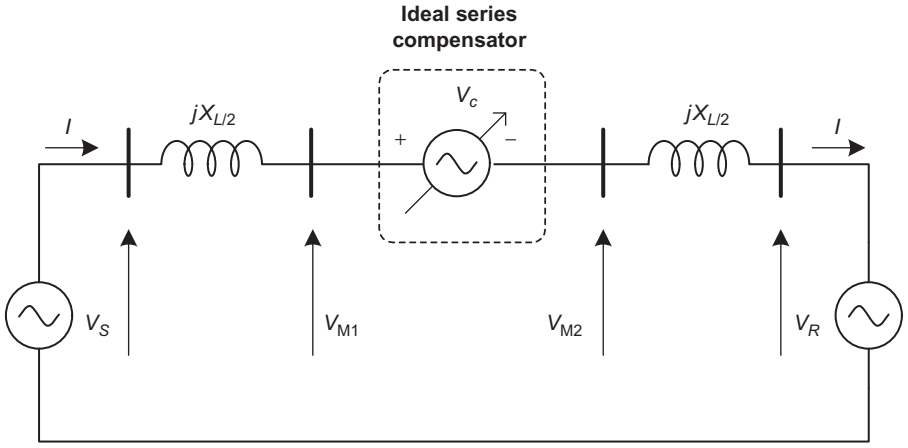


FIG. 28.4 Ideal series compensator connected in the middle of a transmission line.

compensation factor s. The reactive power at the series source is given by

$$Q_{CS} = \frac{2V^2}{X_L}\frac{s}{(1-s)^2}(1-\cos\delta) \tag{28.8}$$

The left-hand side of Fig. 28.5A shows the phasor diagram of the system shown in Fig. 28.4 without the ideal series compensator. On the right-hand side of the Fig. 28.5A, the voltage phasor V_L on the line reactance X_L and the compensator voltage phasor V_C are shown for a given compensation level, assuming that this voltage V_C corresponds to a capacitive compensation. In this case, the line current phasor leads voltage phasor V_C by 90 degrees, and the total voltage drop in the line $V_Z = V_S - V_R - V_C$ is larger than the original voltage drop V_L. The current flowing in the line is larger after compensation than before. This situation shows the case where the series compensator is used to increase power flow.

The left-hand side of the Fig. 28.5B shows the same noncompensated situation as in the previous case. On the right-hand side, the case of an equivalent inductive compensation is shown. In this case, the compensation voltage V_C is in phase with the line drop voltage V_L, producing an equivalent total voltage drop V_Z smaller than in the original case. As a result, the current phasor I flowing in the line is smaller than before compensation. This kind of compensation might be interesting in the case that the power flowing through the line has to be decreased. In either capacitive or inductive compensation modes, no active power is absorbed or generated by the ideal series compensator.

Fig. 28.6 shows an ac system with an ideal generic series compensation voltage source V_C for the general case where it may not be in quadrature with the line current. In this case, the compensator can fully control the phase difference between the two systems, thus controlling the active and reactive power exchanged between them. However, in this case, the compensation voltage source V_C may have to absorb or generate active power (P_C) and control the reactive power (Q_C).

Fig. 28.7 shows the phasor diagram of this ideal generic series compensator. This figure also shows a dashed-line circle with the locus of all possible positions that the compensation voltage V_C could take, assuming that the magnitude shown for this voltage

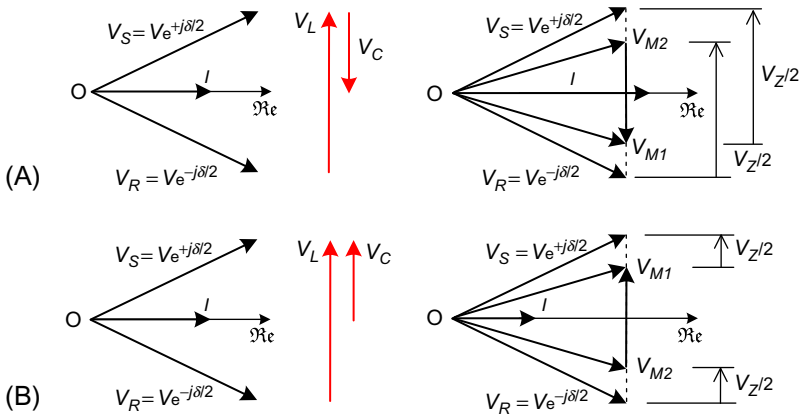


FIG. 28.5 Phasor diagram of the series reactive compensator: (A) capacitive and (B) inductive mode.

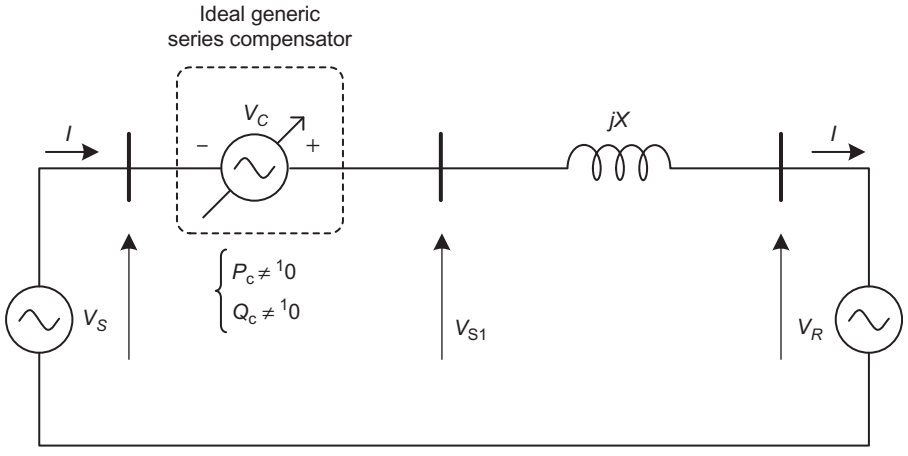


FIG. 28.6 Ideal generic series compensator.

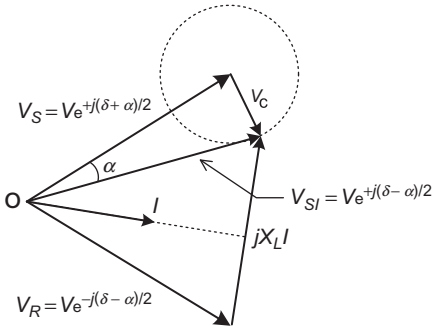


FIG. 28.7 Phasor diagram of the ac system compensated with an ideal generic series compensator.

is its maximum. Naturally, if the sum of the compensation voltage and the source voltage V_S is on the circle, the magnitude of V_{SI} may be smaller or larger than the magnitude of V_S.

The compensation voltage V_C can be added to the V_S in a way that the resultant voltage V_{S1} has the same magnitude of V_S but with a phase shifted by an angle α. In this case, the series compensator can be called as a phase-shifter compensator, and the power flowing through the transmission line (see Fig. 28.6) is expressed below:

$$P_S = \frac{V^2}{X_L}\sin(\delta - \alpha) \tag{28.9}$$

Eq. (28.9) shows that transmitted power increases as the phase difference $(\delta - \alpha)$ reaches 90 degrees. However, its maximum value is the same as in the case of no compensation. The difference is that with this compensator, the system power angle, and angle difference between the two voltage sources at the terminals of the line can be controlled faster than the conventional way, that is, by controlling the synchronous generator.

In Fig. 28.7, voltage V_C may have any phase angle with respect to line current. Therefore, it may have to supply or absorb active power and control reactive power. As in the case of the shunt device, this feature must also be taken into account in the synthesis of the actual devices. As a first approximation, when the goal is to control active power flowing through the medium- or short-length transmission lines, compensator location seems to be a question of convenience.

Fig. 28.8 summarizes the active power transfer characteristics in a transmission line as a function of the power angle, δ, as shown in Figs. 28.1 and 28.2, for the cases of the line without compensation, line with series or shunt reactive power compensation, and line with phase-shift compensation (generic series compensation). These characteristics are drawn on the assumption that the source voltages V_S and V_R (see Fig. 28.2) have the same magnitude. A 50% series compensation ($s = 0.5$) as defined in Eq. (28.4) presents a significant increase in the line power transfer capability.

As shown in Fig. 28.8, in general, series compensation is the best choice for increasing power transfer capability. The phase-shifter compensator is important to connect two systems with excessive or uncontrollable phase difference. It does not increase power transfer capability significantly; however, it may allow the adjustment of large or highly variable phase differences. The shunt compensator does not increase power transfer capability in a significant way in its normal operating region, where the angle δ is naturally below 90 degrees and in general around or less than 30 degrees. The great importance of the shunt compensator is the increase in the stability margin, as explained in Fig. 28.9.

Fig. 28.9 shows the power transfer characteristics $(P_\delta \times \delta)$ of a transmission line, which is first assumed to be transmitting power P_{S0} at phase angle δ_0. If a problem happens in the line (e.g., a fault), the turbine that drives the generator cannot change its mechanical power input immediately even if there

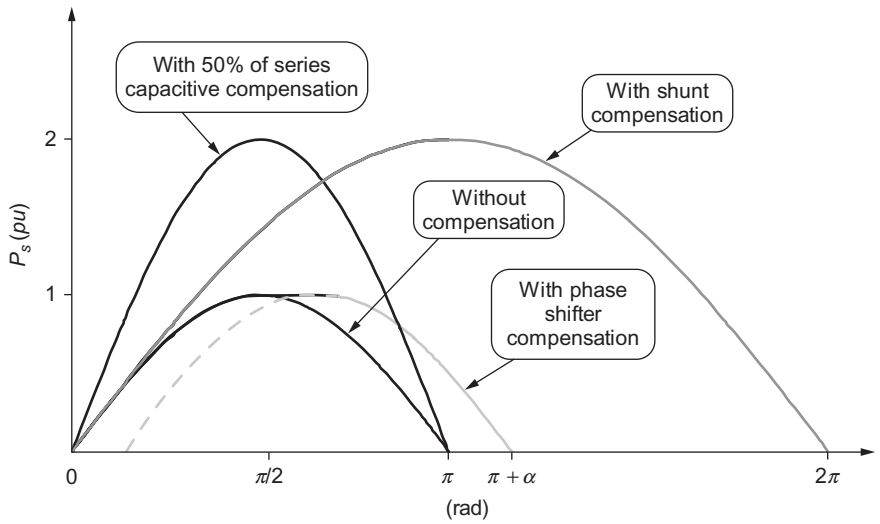


FIG. 28.8 Power transfer characteristics for the case of shunt, series, phase shift, and no compensation.

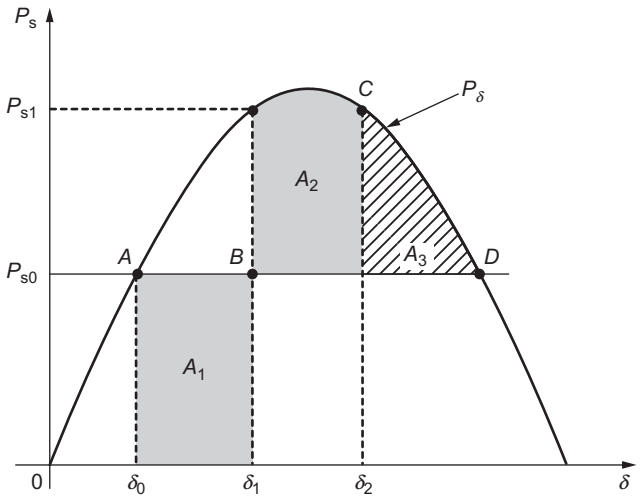


FIG. 28.9 Stability margin characteristics—stable situation.

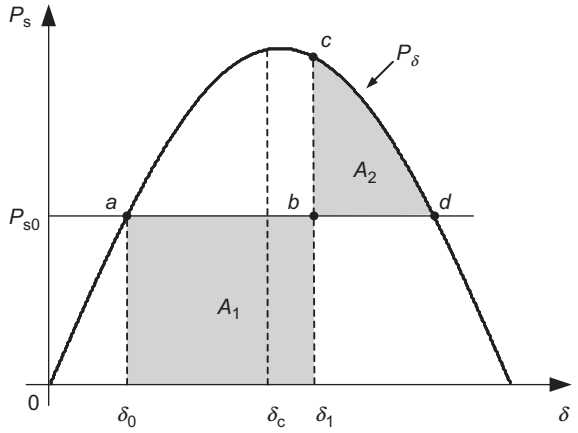


FIG. 28.10 Stability margin characteristics—unstable situation.

is no power transmission for a short time. This situation accelerates the generator, increasing its frequency and leading to an increase of the phase angle δ to δ_1. If the line restarts operation at the instant corresponding to this phase angle δ_1, the transmitted power will be P_{S1}, which is larger than P_{S0} and decelerates the turbine or generator. The area A_1 corresponds to the energy that accelerated the turbine. As the frequency gets higher than the rated frequency at (P_{S1}, δ_1), the phase angle will increase up to δ_2, where the area A_2 is equal to the area A_1. If the area given by the A_2 plus A_3 is larger than A_1, the system is said to be dynamically stable. On the contrary, if it is not possible to have an area A_2 equal to A_1, the system is said to be unstable. An unstable situation is shown in Fig. 28.10 in which the system is the same as in Fig. 28.9 but assuming a longer interval with no power transmission. In this case, the turbine or generator accelerates more than that in Fig. 28.9, and the phase angle δ increases above its critical value δ_c, which is slightly less than 90 degrees reaching δ_1. Therefore, the area below the $Px\delta$ curve to decelerate the system is not enough leading to an unstable system because A_2 is smaller than A_1 and the frequency does not return to its original value.

Looking at Fig. 28.8, it is possible to see that depending on the operating point, all three compensation methods increase the stability margin as the area under the curve of transmitted power $P\delta$ versus phase angle δ is increased. The ideal shunt compensator is the one that most increases this area, and thus, it is said to be the best option to increase the stability margin.

28.4 Synthesis of FACTS Controllers

It has been stated that the synthesis of the compensators presented in Sections 28.2 and 28.3 can be achieved with thyristors or self-commutated switches. Each type of switches (thyristor or self-commutated) leads to controllers with different operating principles and synthesis concepts, and hence, they should be discussed separately. Terms and definitions for most of the FACTS controllers are given in Ref. [10].

Thyristor-based FACTS controllers use line or natural commutation together with large passive energy storage elements (capacitors or reactors). On the other hand, controllers based on self-commutating switches use gate-controlled commutation. In general, it is said that the first generation of FACTS devices is based on conventional line-commutated thyristors, and the subsequent generations are based on gate-controlled devices or self-commutated switches. The most important FACTS controllers based on thyristors and self-commutating controllers are presented in the following sections.

28.4.1 Thyristor-Based FACTS Controllers

28.4.1.1 Thyristor-Controlled Reactor

The most used thyristor-based FACTS controller is the thyristor-controlled reactor (TCR) as shown in Fig. 28.11A. This is a shunt compensator that produces an equivalent continuous variable inductive reactance by using phase-angle control. Fig. 28.11B shows the voltage and current waveforms of the TCR. The current is controlled by the firing angle α; the magnitude of the fundamental current component can be larger or smaller depending on the angle α, which can vary from 90 to 180 degrees measured from the zero crossing of the voltage. At $\alpha = 90$ degrees, the reactor is fully inserted in the circuit, and for $\alpha = 180$ degrees, the reactor is completely out of the circuit. Fig. 28.12 shows the equivalent admittance of the TCR as function of the firing angle α. Naturally, this admittance is always inductive.

28.4.1.2 Thyristor-Switched Capacitor

Fig. 28.13 shows the thyristor-switched capacitor (TSC). The word "controlled" used in the case of the reactor is substituted by "switched" because the thyristor is turned on only when zero-voltage switching (ZVS) condition is possible. This means that the voltage across the thyristor terminals has to be zero at

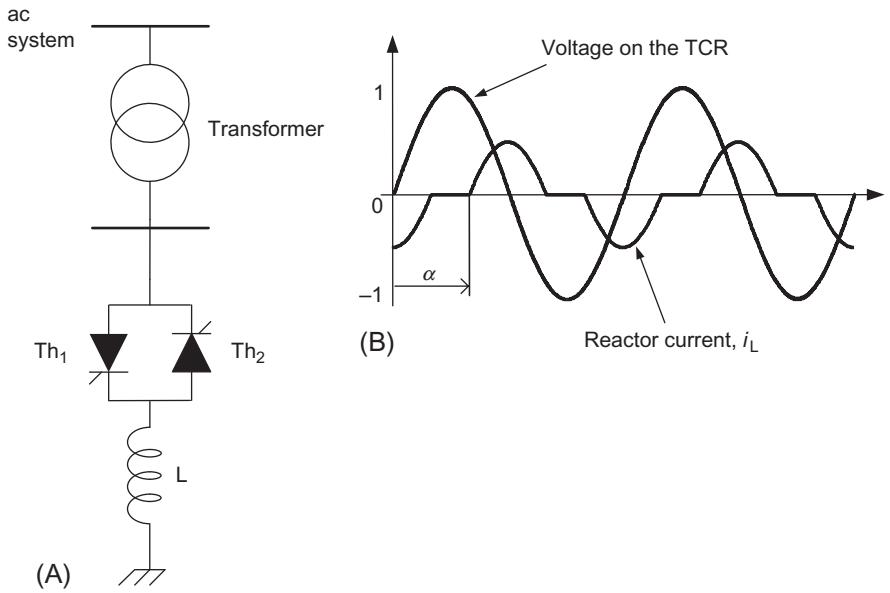


FIG. 28.11 (A) TCR and (B) its voltage and current waveforms.

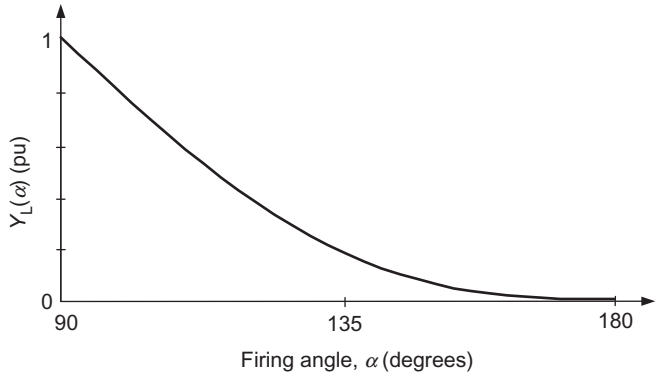


FIG. 28.12 Equivalent admittance of a TCR as a function of the firing angle α.

the turn-on instant. In practical cases, it may be slightly positive because thyristors need positive anode-cathode voltages to be triggered (positive anode-cathode voltage during turn-on); however, if this voltage is too high, it can produce a large current spike that can damage the thyristors. Therefore, due to this switching characteristic, the thyristors can only connect the capacitor to the grid or disconnect it. Consequently, only step-like control is possible, and a continuous control is not possible. The capacitor connection to or disconnection from the grid is normally performed at very low frequencies, and the harmonics, when they appear, are not a serious concern.

28.4.1.3 Static Var Compensator

The use of the TCR shown in Fig. 28.11 or the TSC shown in Fig. 28.13 allows only continuous inductive compensation or discontinuous capacitive compensation. However, in most applications, it is desirable to have continuous capacitive or inductive compensation. The static var compensator (SVC)

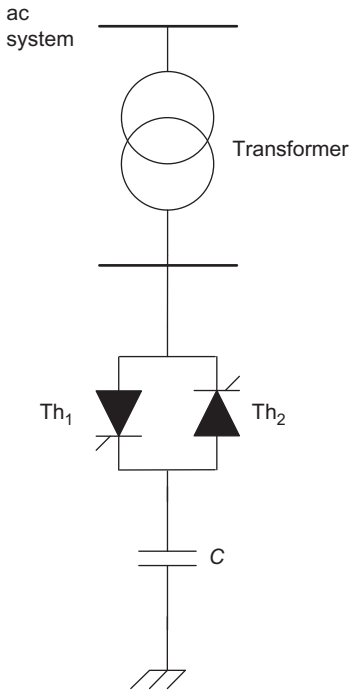


FIG. 28.13 Thyristor-switched capacitor (TSC).

is generally designed to operate in both inductive and capacitive continuous compensation [11,12]. It may be used for reactive power compensation for either voltage regulation or power factor correction. The basic three-phase SVC scheme is comprised of a three-phase TCR parallel connected to a capacitor bank. The TCR serves as the controller basis for the conventional SVC.

Fig. 28.14 shows a single-line diagram of an SVC, where the TCRs are Δ connected and the capacitors are Y connected. The

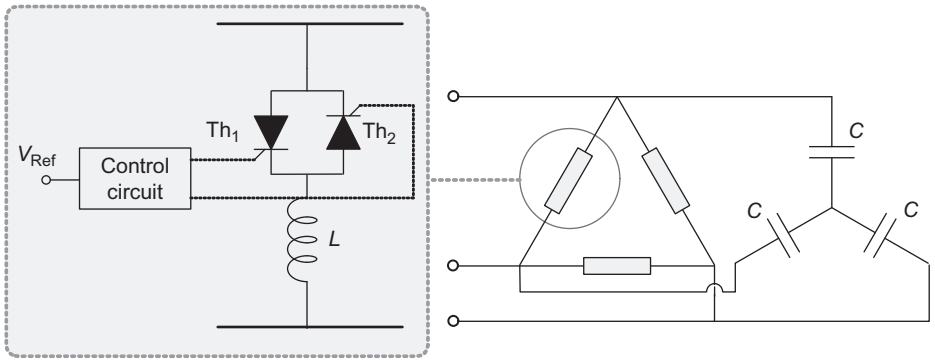


FIG. 28.14 Six-pulse SVC.

circuit does not show the filters that are normally needed due to the switching-generated harmonics. In some cases, the capacitor bank can be a fixed capacitor parallel connected to a TSC in order to get more flexibility in terms of control range.

The capacitance of the SVC is calculated in such a way as to generate the maximum capacitive reactive power that it has to control. This condition is achieved when the thyristors are turned off ($\alpha = 180$ degrees). On the other hand, the maximum reactive power of the TCR inductor has to be greater than the reactive power of the capacitor bank. In this way, the SVC can control the reactive power from capacitive to inductive. The maximum inductive reactive power is given for the case when the thyristors are turned on at minimum firing angle ($\alpha = 90$ degrees). The SVC can control reactive power from maximum capacitive for $\alpha = 180$ degrees to maximum inductive for $\alpha = 90$ degrees. Thus, the SVC represents an adjustable fundamental frequency susceptance to the ac network, controlled by the firing angle of the TCR thyristors (90 degrees $< \alpha <$ 180 degrees).

The SVC is well known, and many examples of successful applications can be found around the world.

Due to the once-per-cycle thyristor firing with phase-angle control, current with low-order harmonic components appears and Y-Δ transformers and passive filters may be needed to eliminate part of them. Three sets of TCRs connected in the Δ side of Y-Δ transformers form a conventional six-pulse TCR. To minimize harmonic generation, it is common to have two sets of transformers connected in Y-Δ and Δ-Δ with the TCR connected in the Δ side forming a 12-pulse TCR.

28.4.1.4 Thyristor-Switched Series Capacitor

Fig. 28.15 shows the thyristor-switched series capacitor (TSSC). In this controller, the thyristors should be kept untriggered so as to connect the capacitors in series with the transmission line. If the thyristors are turned on, the capacitor is bypassed. Thyristors must be turned on at a zero-voltage condition (ZVS), as it occurs in the case of the TSC, to avoid current spikes in the switches. An example of an application based on this concept is presented in Ref. [13].

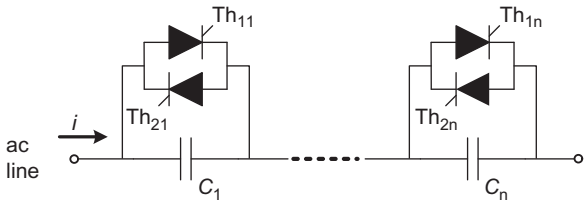


FIG. 28.15 Thyristor-switched series capacitors (TSSC).

This compensation system has the advantage of being very simple. However, it does not allow continuous control. If the connection or disconnection of the capacitors is to be made at sporadic switching, it can be said that no harmonic problem occurs. Depending on the frequency the thyristors are switched, harmonic or subharmonics may appear. In this arrangement, it is interesting to choose a number of capacitors in such a way that many different combinations can be achieved. For example, if the total number of capacitors is three, they could have impedance proportional to 1, 2, and 3. Therefore, by combining these values, it is possible to obtain equivalent capacitive impedance proportional to 1, 2, 3, 4, 5, and 6.

28.4.1.5 Thyristor-Controlled Series Capacitor

Fig. 28.16 shows the thyristor-controlled series capacitor (TCSC). In this figure, the transmission line and the voltage

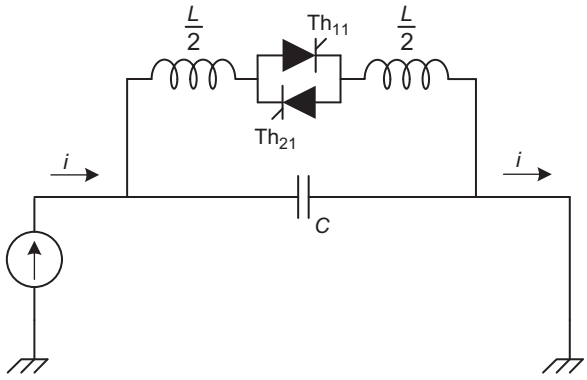


FIG. 28.16 Thyristor-controlled series capacitors (TCSC).

sources at its ends are represented by a current source because this is the actual behavior of most of the transmission system. This compensator is also based on the TCR that was first developed for shunt connection. When the TCR is used connected in series with the line, it has to be always connected in parallel with a capacitor because it is not possible to control the current if the equivalent of the transmission line and the sources is a current source. This circuit is similar to the conventional SVC with the difference that the TCSC is connected in series with the line. In this compensator, the equivalent value of the series connected reactor can be continuously controlled by adjusting the firing angle of the thyristors. As a consequence, this device presents a continuously controllable series capacitor. Various practical systems based on this concept are under operation around the world [13–15]. This device has been used for power flow control and power oscillation damping.

Fig. 28.17 presents the current and voltage waveforms in the TCSC, showing that although there is a large amount of harmonics in the capacitor and reactor currents, capacitor voltage is almost sinusoidal. In actual applications, these harmonics are not a serious concern, and they are filtered by the capacitor itself and by the transmission line impedance.

Fig. 28.18 shows the equivalent impedance of the TCSC as a function of the firing angle α. This figure shows that this controller has both capacitive and inductive characteristic regions divided by a resonant region. In the example shown in this figure, the resonance happens for α around 145 degrees. In normal operation, the TCSC is controlled in the capacitive compensation region where its impedance varies from its minimum value Z_{min} for firing angle $\alpha = 180$ degrees and its maximum safe value Z_{max} for α around 150 degrees. Operation with α close to the resonance region is not safe. This device can operate also in the inductive region, but in this case, normally, it is used only when $\alpha = 90$ degrees to decrease power transfer capability of the transmission line.

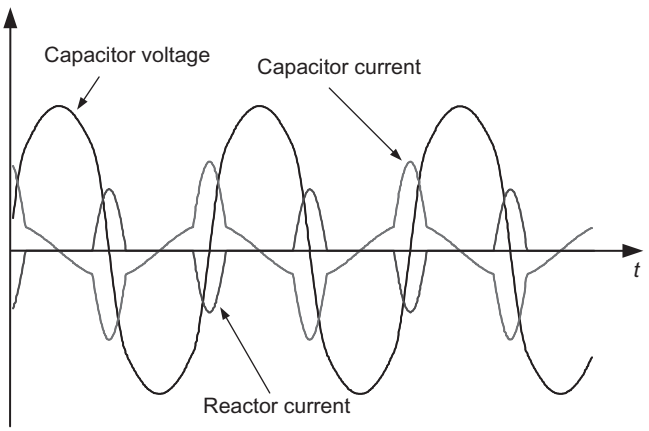


FIG. 28.17 TCSC voltage and current waveforms.

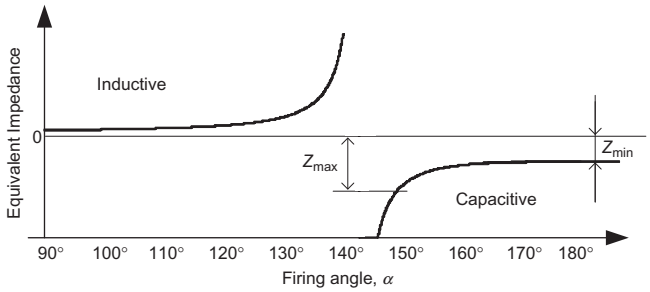


FIG. 28.18 TCSC equivalent reactance.

28.4.1.6 Thyristor-Controlled Phase Angle Regulator

The thyristor-controlled phase-angle regulator (TCPAR), shown in Fig. 28.19 as an example, may improve considerably the controllability of a utility of power transmission system. In this figure, only the control of phase "a" is detailed. The series voltage generated in phase "a" comes from three secondary windings of a transformer whose primary side is connected between phases "b" and "c." Each of the three secondary windings can be connected in series with the line through the thyristors' switching. The thyristors are connected in antiparallel, forming bidirectional naturally commutated switches. By turning on a set of thyristors, a voltage whose magnitude can be controlled by phase control is connected in series with the transmission line. The number of secondary windings is chosen as to decrease harmonic content of the series compensation voltage (Fig. 28.17).

The TCPAR in Fig. 28.19 has some peculiarities that should be pointed out. One of them is that active power can only flow from the shunt to the series windings. The compensation voltage phasor, as shown in Fig. 28.20, has a limited range of

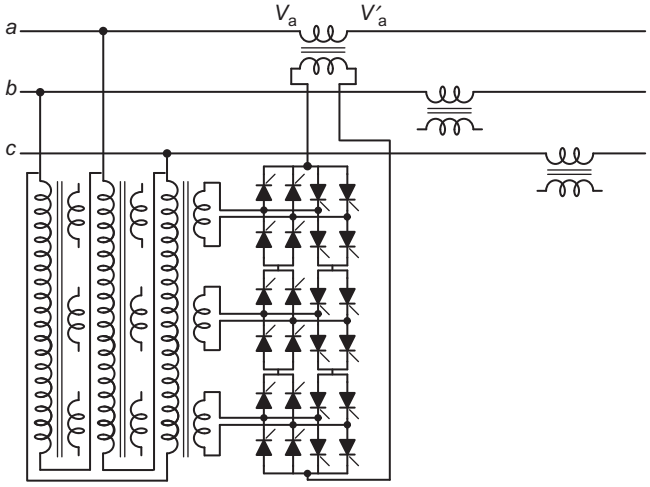


FIG. 28.19 Thyristor-controlled phase-angle regulator (TCPAR).

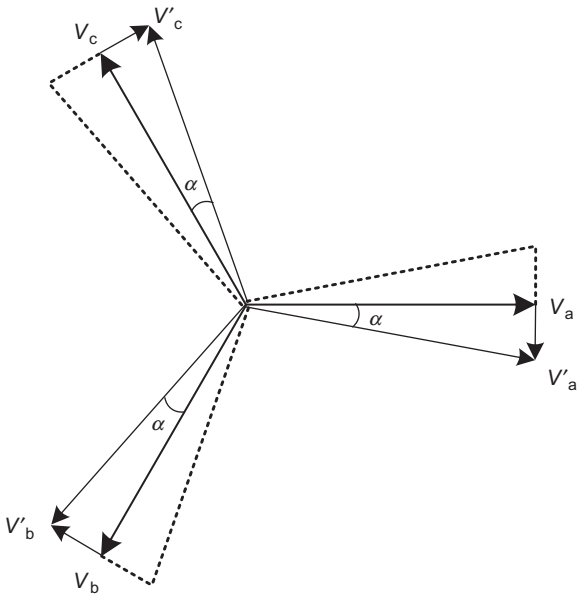


FIG. 28.20 Phasor diagram of the TCPAR in Fig. 28.19.

variation; in the case of phase "a," its locus is along a line orthogonal to V_a because the injected voltage is in phase with the voltage $(V_b - V_c)$. As a consequence, it is not possible for the TCPAR to generate a compensating voltage phasor whose locus is a circle, as shown in Fig. 28.7, for the case of an ideal generic series compensator.

Other configuration of phase shifters can be found in the literature, for example [16,17].

28.4.2 FACTS Controllers Based on Self-Commutated Switches

There are various different types of FACTS controllers based on self-commutated switches, and the names used here are in accordance with the names published in Ref. [10]. Some of them are newer controllers and are not in that reference. In this case, the name used is the same as it appears in the literature. In Ref. [2], it is possible to find most of the details of FACTS controllers.

The development of high-power self-commutated devices has led to the development of high-power voltage source converters (VSC), such as the six-pulse two-level VSC shown in Fig. 28.21A [4] or the three-level neutral point clamped VSC shown in Fig. 28.21B [18]. In the figures, the generic switches could be IGBTs, IGCTs, or other self-commutating switches or even the recently developed SiC switches, with an antiparallel connected diode. This set of self-commutated switch and antiparallel diode operates with a unidirectional voltage-blocking capability and a bidirectional current flow. In contrast, the current source converters (CSC) used in HVDC transmission systems use switches (thyristors) operating with unidirectional current flow and bidirectional voltage-blocking capabilities.

In a conventional VSC, for industrial applications, a voltage source is connected at the converter dc side. However, in the case that only reactive power has to be controlled, the dc voltage source may be replaced by a capacitor. If active power has to be absorbed or generated by the compensator, an energy storage system has to be connected at the dc side of the VSC.

In practical applications, small reactors (L) are necessary to connect the VSC to the ac network. This is necessary to avoid current peaks during switching transients. In most cases, these reactors are the leakage inductance of the coupling transformers.

28.4.2.1 Static Synchronous Compensator (STATCOM)

The first high-rating STATCOM started operation in 1991 [19] in Japan and uses three single-phase VSCs to form one

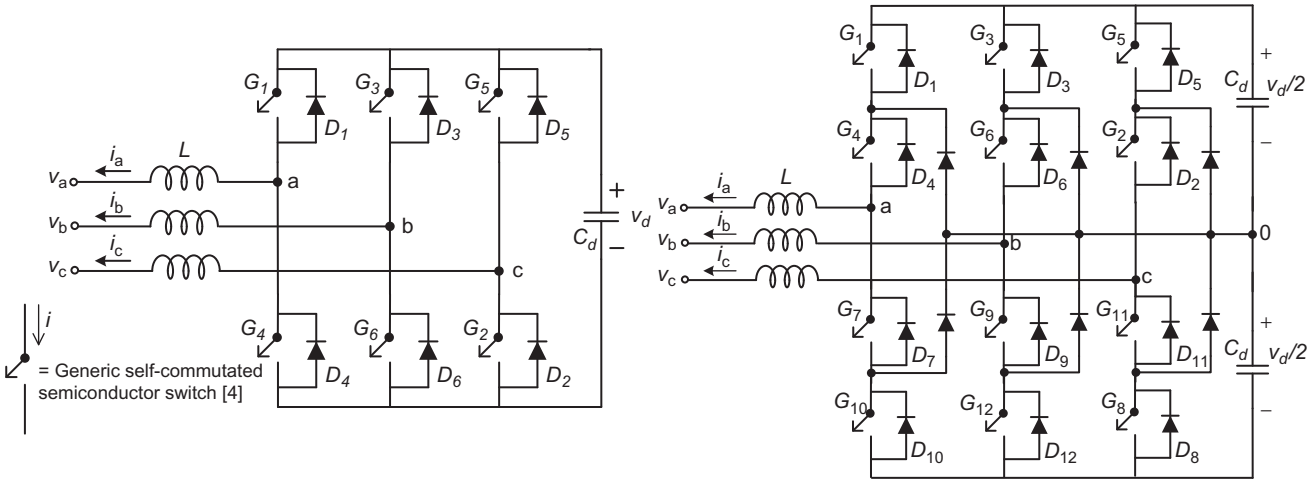


FIG. 28.21 (A) Basic six-pulse VSC two-level var compensator and (B) basic three-level var compensator.

three-phase, six-pulse, 10 MVA converter. To guarantee low losses, the switching frequency is equal to the line frequency, and a total of eight sets of three-phase converters are used to form a 48-pulse converter. All the converters have a common dc capacitor in their dc side. In the ac side, the converters are connected in series through a zigzag transformer to eliminate low-frequency voltage harmonics. The device with compensation capability of 80 MVA was developed to increase the transient stability margin of the system, and it has allowed a 20% increase of the transmitted power above the previous stability limit. Since it was developed for improving transient stability margin, it normally operates in standby mode without reactive compensation and, consequently, low losses. During transient situation, this STATCOM operates for a short time until the system is stable.

The development of the first high-power (±100 Mvar) STATCOM in the United States was reported in Ref. [20]. It is based on eight sets of three-phase bridge converters, similar to that shown in Fig. 28.21A; it was developed for reactive power control, so it can operate continuously with acceptable losses. The switching frequency is equal to line frequency, and the number of pulses is 48; therefore, the output voltage waveform is almost sinusoidal, and harmonic filters are not used in both cases referred in Refs. [19,20].

Basic switching control techniques

In FACTS applications, the power ratings of the converters are in the range of some MW to hundreds of MW, and the switching frequency is lower than the switching frequency used in industrial application converters to avoid excessive switching losses. However, there are various switching control types. The most known so far are as follows:

- Multipulse converters switched at line frequency, as in Refs. [19,20]
- Pulse-width modulation (PWM) with harmonic elimination technique [21]
- Sinusoidal PWM [7]
- Cascade converters [22], including the multilevel modular converter (MMC) [23]

Multipulse converters switched at line frequency

The multipulse converter was the first choice for STATCOM application because it presents low losses and low harmonic content [19,20]. Fig. 28.22 shows a 24-pulse converter based on three-phase, two-level six-pulse converters. In this case, the zigzag transformers are connected in such a way as to produce phase differences of 15, 30, 45, and 60 degrees. With this arrangement, the resulting output voltage and its harmonic spectrum are as shown in Fig. 28.23. The first two harmonic components are the twenty-third- and twenty-fifth-order harmonics. Fig. 28.24 shows the voltage waveform for a 48-pulse converter and its respective harmonic spectrum. In this case, the first two harmonic components are the forty-seventh-

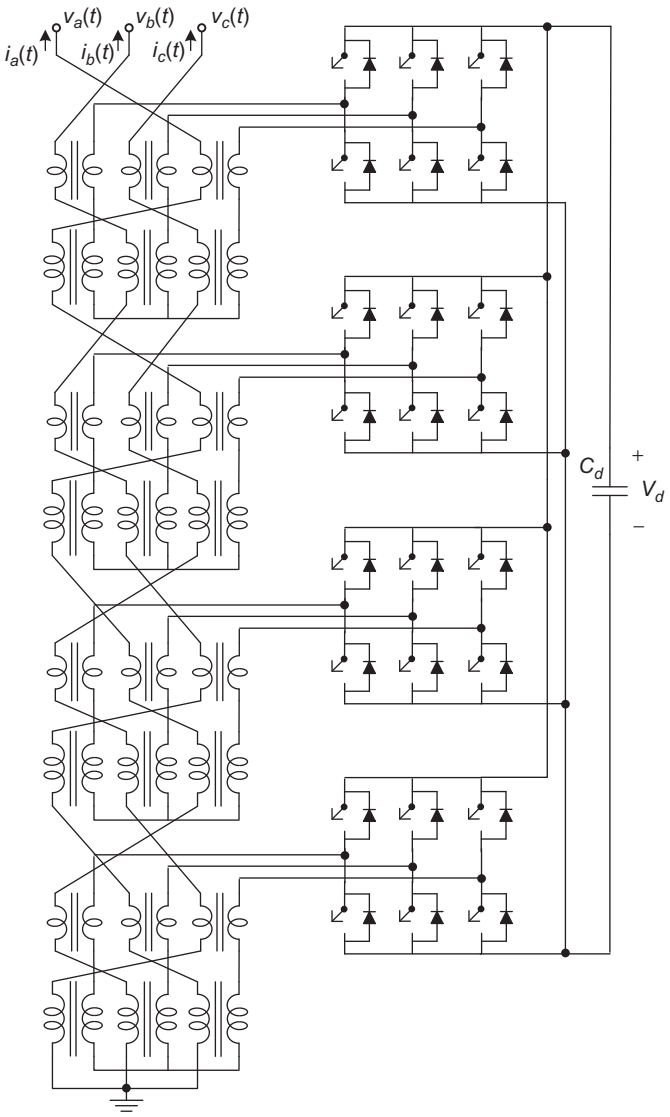


FIG. 28.22 Six-pulse 2-level VSC-based 24-pulse static var compensator (STATCOM).

and forty-ninth-order harmonics. The total harmonic distortions (THD) for the 24-pulse and 48-pulse converters are 7% and 3.3%, respectively. These converters can also be built by using three-level converters. However, one drawback of the multipulse converter is the complexity, weight, and cost of the transformers, which have to operate with high harmonic content in their voltage and various different turns ratio.

PWM with harmonic elimination technique

One way to avoid the complexity of the multipulse converters is to use PWM with harmonic elimination technique [21]. With this approach, it is possible to use relatively low switching frequency and, consequently, have low switching losses. The PWM modulation is obtained by off-line calculation of the switches at "on" and "off" instants in order to eliminate the low-frequency harmonics. Fig. 28.25A shows an example of

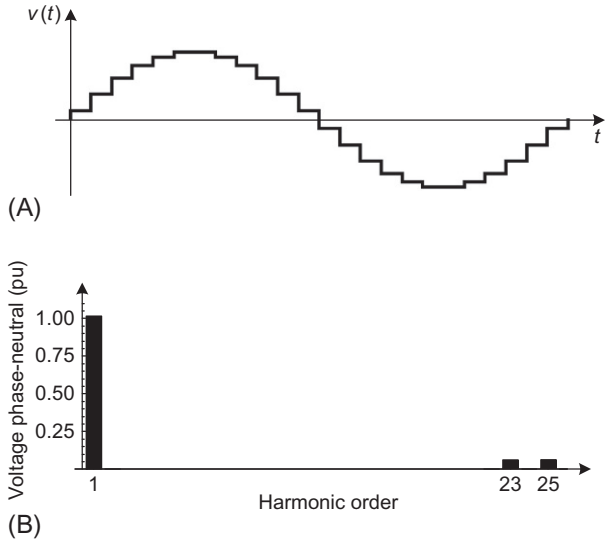


FIG. 28.23 (A) 24-pulse converter voltage waveform and (B) its harmonic spectrum.

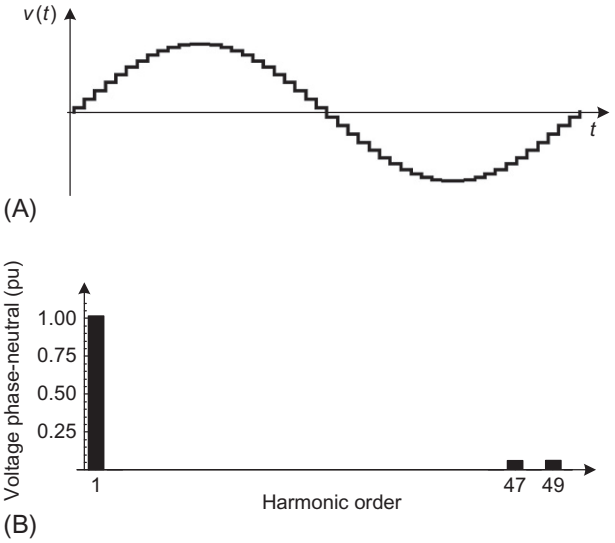


FIG. 28.24 (A) 48-pulse converter voltage waveform and (B) its harmonic spectrum.

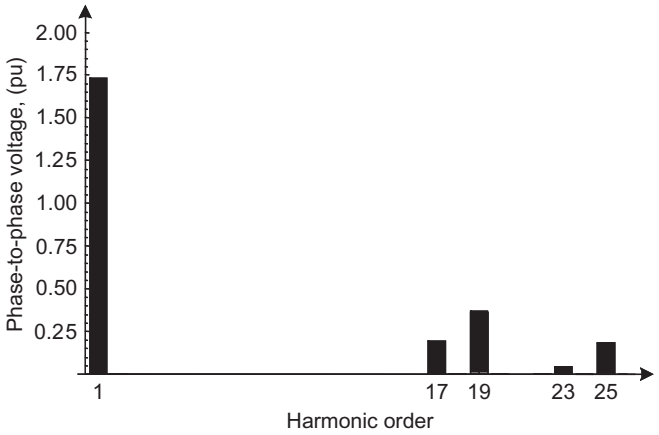


FIG. 28.26 Line voltage harmonic spectrum for the voltage waveform in Fig. 28.25A.

voltage waveform with "on" and "off" instants calculated in such a way as to eliminate the fifth-, seventh-, eleventh-, and thirteenth-order harmonics. This voltage corresponds to the voltage between one phase of the converter and the negative terminal of the dc side. Fig. 28.25B shows the control angle as a function of the modulation index m_a. Fig. 28.26 shows the harmonic spectrum for the phase-to-phase voltage waveform corresponding to that shown in Fig. 28.25A. Here, it is considered that the rms value of the fundamental component of the voltage in Fig. 28.25 is equal to unity. In Fig. 28.26, the magnitude of the fundamental component is equal to $\sqrt{3}$ pu. The higher-order harmonics in the voltage waveform can be eliminated by a relatively small passive filter, so the voltage and the current at the converter terminals are practically harmonic-free; therefore, the transformer that connects a PWM-controlled STATCOM to the grid may be a conventional transformer designed for sinusoidal operation.

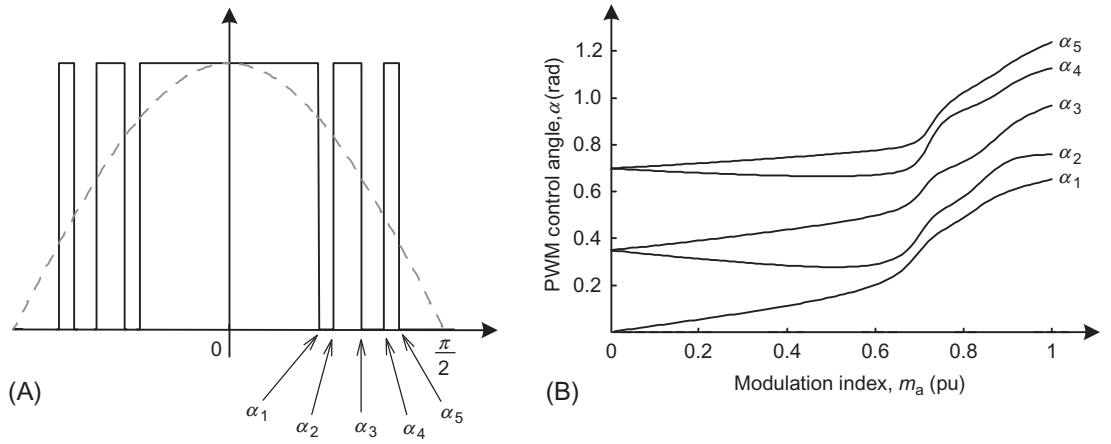


FIG. 28.25 (A) Example of one-phase voltage with the harmonic elimination technique and (B) the control angle as function of the modulation index.

Sinusoidal PWM

The sinusoidal PWM control technique is possibly the simplest to implement and can be synthesized by comparing a sinusoidal reference voltage with a triangular carrier [4]. This switching control method needs a relatively high switching frequency, which is in the range of 1–2 kHz and consequently produces higher switching losses than multipulse STATCOM. The harmonic content at low frequencies is negligible; however, there is a relatively high harmonic content at the switching frequency, which is eliminated by a passive filter.

Cascade converter

The basic cascade converter [22] topology is shown in Fig. 28.27. Only two single-phase full-bridge converters are shown, the first and the *n*th. However, in actual application, several of them are connected in series and switched at line frequency. The resulting voltage waveform can be similar to the multipulse converter waveform with the advantage that there is no need of transformers to sum up the converter output voltage. Due to the line frequency switching, the switching losses are very low. The resulting voltage waveform can be almost sinusoidal depending on the number of series converters, and the transformer used to connect them to the grid can be a conventional sinusoidal waveform transformer, if necessary. The need to have one dc capacitor for each single-phase converter has two consequences: the number of capacitors is equal to the number of single-phase converters, and the capacitance of each capacitor has to be much higher than three-phase converters. This is because the instantaneous power in each single-phase converter has a large oscillating component at double of the line frequency, and it would force a large voltage ripple in the capacitors if they were small.

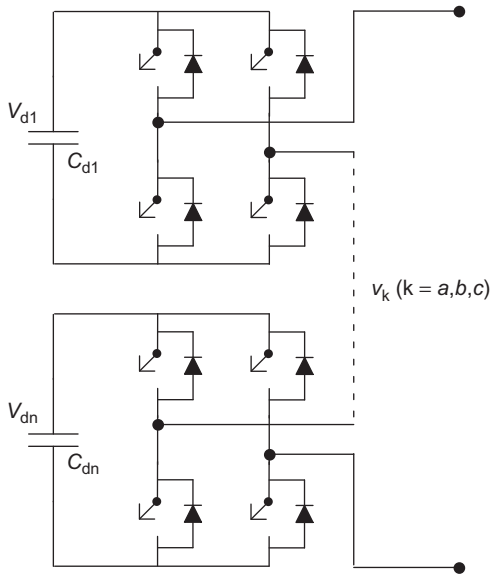


FIG. 28.27 Cascade converter basic topology.

Multilevel modular converter: The MMC is an emerging topology for high-power and high-voltage VSC application [23]; it is suitable for either HVDC transmission or FACTS applications [24,25]. For very high-power applications, an MMC is also an alternative, and potentially preferable, to a multilevel converter [26]. The MMC is being presented as the preferred potential candidate for VSC-HVDC system applications [27]. Features like modularity and capability of a multimodule VSC to handle high power or high voltage indicate that a MMC may also be an option to high-power STATCOM and other FACTS compensator such as SSSC, UPFC, or IPFC.

Fig. 28.28 shows the basic topology of a three-phase MMC. Each leg is comprised of *n* submodules, which are composed of two self-commutated switches and a storage capacitor. Depending on the application, a full-bridge submodule might be necessary instead of the half bridge shown in this figure. A semi-full-bridge submodule topology is an alternative option for blocking short-circuit current in the dc link of the converter [28]. The submodule can be seen as a voltage source with two possible stages 0 or V_C where V_C is the voltage over the submodule capacitor. Thus, each arm can be understood as a controllable voltage with *n* possible voltage steps, and the higher the number of submodules, the more approximated sine waveform can be achieved at the ac side. The main advantages of the MMC are low switching losses, low *dv/dt* over individual switch, modularity, reconfigurable design, and increased energy storage [26]. Beyond that, the MMC can also be directly connected to the power system, that is, without any power transformer [29], which can reduce the overall substation footprint and cost, resulting in a compact-area HVDC substation.

STATCOM control techniques

The control of reactive power in the STATCOM is done by controlling its terminal voltage. Fig. 28.29 shows a simplified circuit in which the ac grid is represented by a voltage source V_S behind an impedance jX_L and the STATCOM is represented by its fundamental voltage component V_I. Fig. 28.30A shows the case when the ac grid phasor voltage V_S is in phase with the STATCOM voltage V_I and both have the same magnitude. In this case, the line current I_L is zero. Fig. 28.30B shows the case when V_S is little larger than V_I. In this case, the line current I_L, which lags the impedance voltage V_L by 90 degrees, is also lagging the ac grid phasor voltage V_S, and therefore, the STATCOM produces an inductive reactive power. On the other hand, Fig. 28.30C shows the case when V_S is little smaller than V_I. Hence, the line current I_L, which lags the voltage V_L by 90 degrees, leads the voltage V_S, and therefore, the STATCOM produces a capacitive reactive power. In summary, the STATCOM reactive power can be controlled if the magnitude of its V_I voltage is controlled, assuming that it is in phase with V_S:

- If $|V_S|$ is equal to $|V_I|$, there is no reactive power and no active power in the STATCOM.

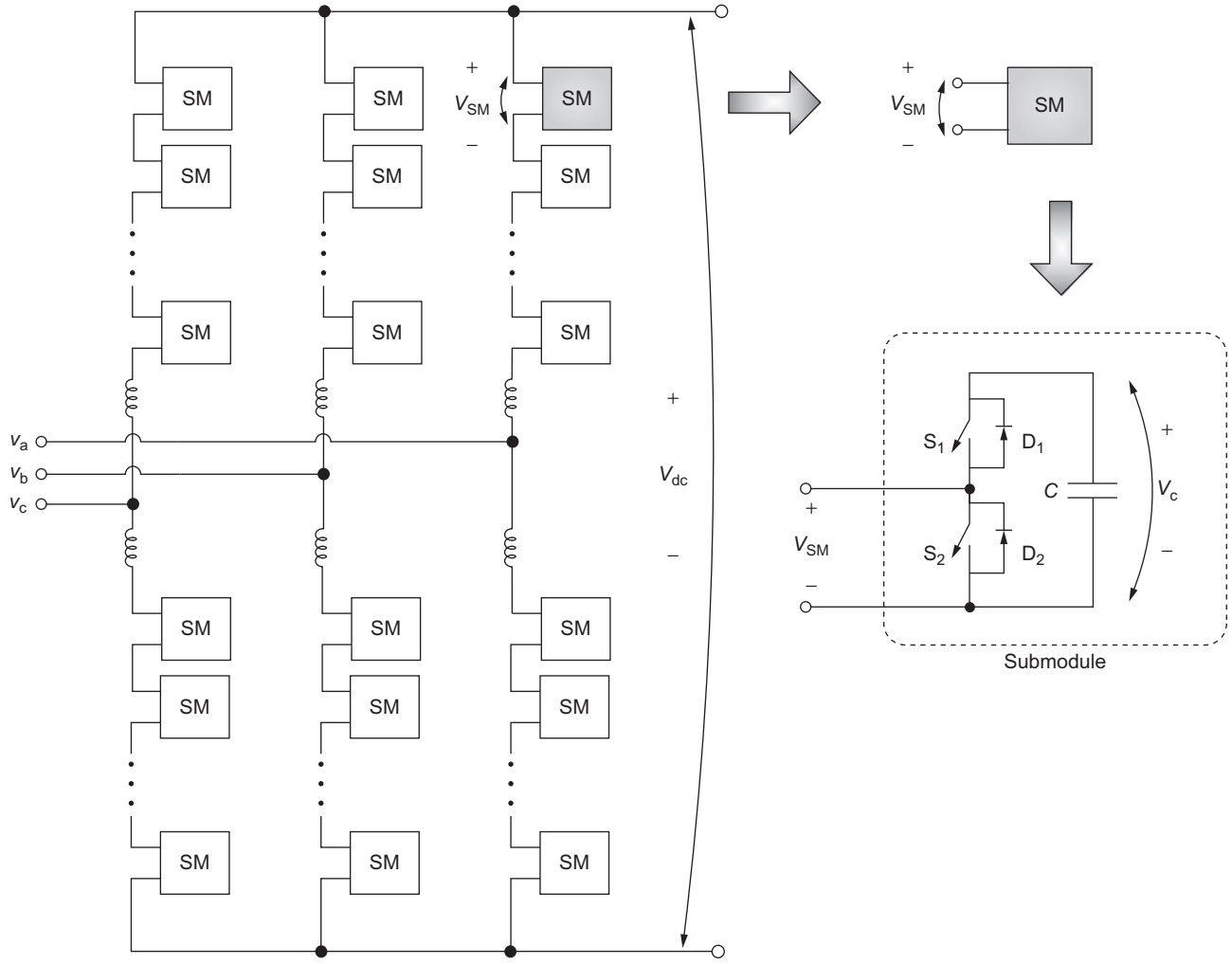


FIG. 28.28 Modular multilevel converter topology.

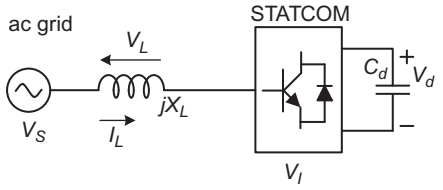


FIG. 28.29 Simplified circuit for the ac grid and the STATCOM.

- If $|V_S|$ is larger than $|V_I|$, the STATCOM reactive power is inductive.
- If $|V_S|$ is smaller than $|V_I|$, the STATCOM reactive power is capacitive.

Therefore, the reactive power control in a STATCOM is a problem of how to control the magnitude of its voltage V_I. There are two basic principles: (*i*) in the case of multipulse converters, the output voltage magnitude can only be controlled by controlling the dc-side voltage that is the dc capacitor voltage, and (*ii*) in the case of PWM control, the dc capacitor voltage can be kept constant, and the voltage can be controlled by PWM controller.

Fig. 28.31A shows the phasor diagram for the case when a phase difference δ between V_S and V_I is positive. The resulting line current is in such a way that produces an active power flowing into the converter, charging the dc capacitor. Fig. 28.31B shows the phasor diagram for a negative phase angle δ. In this case, the dc capacitor is discharged. Therefore, by controlling the phase angle δ, it is possible to control the dc capacitor voltage.

In general, STATCOM based on multipulse converter without PWM has to control its voltage by charging or discharging the dc capacitor, and this voltage has to be variable. On the other hand, STATCOM based on a PWM-controlled converter has to control dc-side capacitor voltage only to maintain it constant. In both cases, the principle shown in Fig. 28.31 is valid.

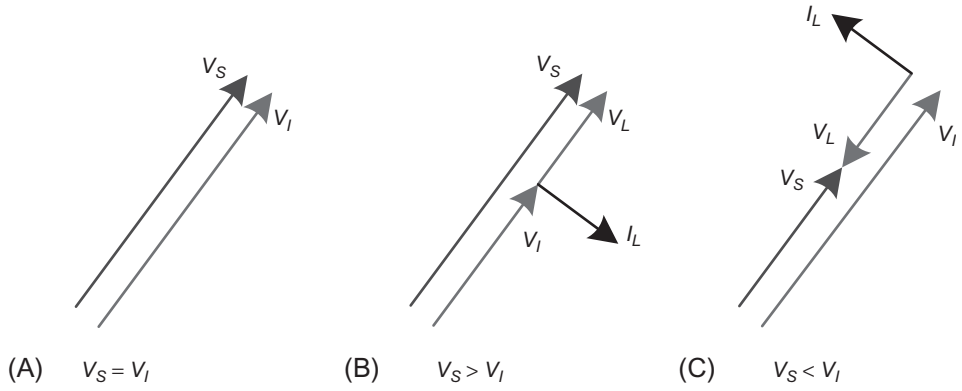


FIG. 28.30 Reactive power control in a STATCOM.

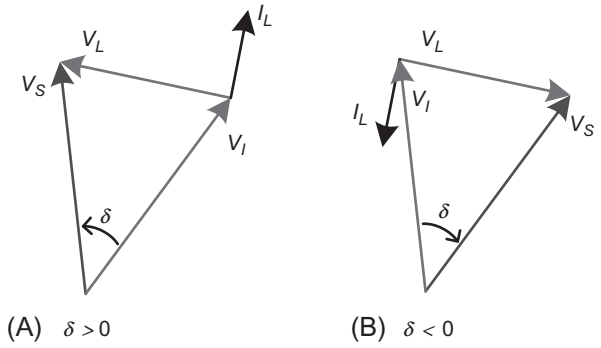


FIG. 28.31 Active power control in a STATCOM.

The STATCOM control technique presented previously illustrates the basic scalar control concepts. However, this compensator can be also controlled by a vector technique [30].

Fig. 28.32 shows a basic control structure for the STATCOM. In this diagram, the vector control technique is implemented in dq synchronous reference frame. This technique is called voltage-oriented control (VOC), in which the grid voltage vector is aligned with the d-axis through the phase-locked loop (PLL) block. This means that the q-axis component of the grid voltage, in steady state, is zero.

The dc-link and grid voltages are controlled through the d- and q-axes, respectively. For the dc voltage control, the voltage across the capacitor is sensed by Hall effect sensor and compared with its reference value. For the grid voltage control, the voltage at the PCC is sensed by Hall effect sensor too, and these signals are transformed to *dq* components in synchronous reference frame. The next step is to compute the aggregate value for this quantity. The aggregate value is an instantaneous quantity, and it results from the square root of the sum of the squared instantaneous values of currents or voltages. This means that the aggregate value is a constant if and only if the voltages (or currents) in all phases are perfectly sinusoidal and balanced [31,32]. The LPF block is a low-pass filter to eliminate any oscillating components in the signal of the aggregate value. Error signals are generated and are input in proportional-integral (PI) controllers, for both cases, as shown in Fig. 28.32, and the current references are generated. From

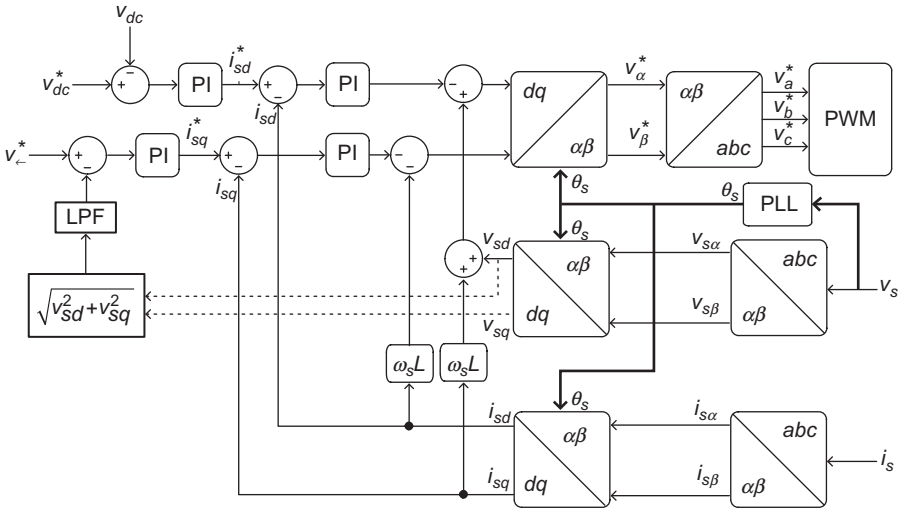


FIG. 28.32 Block diagram of STATCOM based on voltage-oriented control (VOC).

these, reference currents are in *dq* synchronous reference frame. In the inner control loop, the current references are compared with measured values of these same variables. Thus, error signals resulting from this operation excite PI controllers that generate voltage references in the controllers' outputs. Nevertheless, these values must be compensated to avoid coupling between *d*- and *q*-axes [33–35].

Another detail, for this diagram, is that there is an intermediate transformation block from abc to αβ instead of the direct transformation abc-dq, because dc values can be present in αβ component signals caused by the acquisition and/or signal conditioning systems or even by the modulation system, in some cases. Thus, they can be eliminated through the installation of high-pass filters (not present in the figure) just after those intermediate blocks, which would not be possible in the case of direct transformation from abc to dq.

Another way to control the STATCOM is by using the instantaneous power theory [36,37], where only the imaginary power is controlled.

STATCOM DC side capacitor

Theoretically, the dc-side capacitor of a STATCOM based on three-phase converters operating in a balanced system and controlling only the reactive power could have a capacitance equal to zero farad, once the three-phase instantaneous reactive power does not contribute to the energy transfer between the dc and ac side [38]. However, in actual STATCOM, a finite capacitor has to be used with the objective of keeping constant or controlled dc voltage as it tends to vary due to the converter switching. One parameter commonly used in synchronous machine is the inertia constant *H* defined by

$$H = \frac{J\omega^2/2}{S} \tag{28.10}$$

where *J* and ω are the rotor moment of inertia and angular speed and *S* is the machine apparent power. A similar parameter for the STATCOM, H_{ST}, can be defined by

$$H_{ST} = \frac{CV_d^2/2}{S} \tag{28.11}$$

where *C* and V_d are the dc capacitance and its voltage, respectively, and *S* is the STATCOM apparent power.

In both cases, the constants *H* and H_{ST} are values in time units corresponding to the relation of the amount of energy stored in the rotor inertia, or in the capacitor, and the machine, or STATCOM, apparent power, respectively. In the case of synchronous machines, the value of *H* is in the range of few seconds (generally, in the range of 1–3 s), and in the case of the STATCOM, H_{ST} value is in the range of milliseconds or below (0.5–50 ms) if only reactive power is to be controlled. These numbers show that the STATCOM based on three-phase converters and designed only for reactive power control (which is the general case) has almost no stored energy in its dc capacitor. On the other hand, STATCOM based on single-phase converters without a common dc link may have larger capacitors as in the case of cascade converters due to the power oscillations at double of the line frequency.

There are STATCOM (in some cases with different names) that are designed for operation with unbalanced loads. In this case, the dc capacitor has to be also much larger than in the case of balanced systems to avoid large voltage ripple on the dc voltage due to power oscillations at twice the line frequency, which appears naturally in unbalanced systems [33,39] or unbalanced voltages [34] or system with flicker problem [35,40]. In this case, the STATCOM compensates reactive power and the instantaneous oscillating active power due to the negative sequence current components. In fact, this is an extension of the shunt active power filter application where the goal is the current harmonic compensation, which includes negative sequence currents even at the fundamental frequency. If subharmonics are present, the device is able to filter them out as well.

STATCOM with energy storage

In general, the STATCOM is designed for reactive power compensation, and it does not need large energy storage elements. However, there are some applications where it may be interesting to have some energy stored in the dc side, for example, to compensate for active power for a short time. In these applications, the dc-side capacitor has to be substituted by a voltage source energy storage device like a battery [41] or a double-layer capacitor (super capacitor). Another possibility is to store energy in superconducting magnetic energy storage (SMES) systems [42,43]. A natural solution for the use of the superconducting reactor would be the connection to the ac grid through a current source converter (CSC) instead of the voltage source converter. However, this has not been the case found in the literature. Fig. 28.33 shows a block diagram of a typical STATCOM/SMES system, where the SMES is

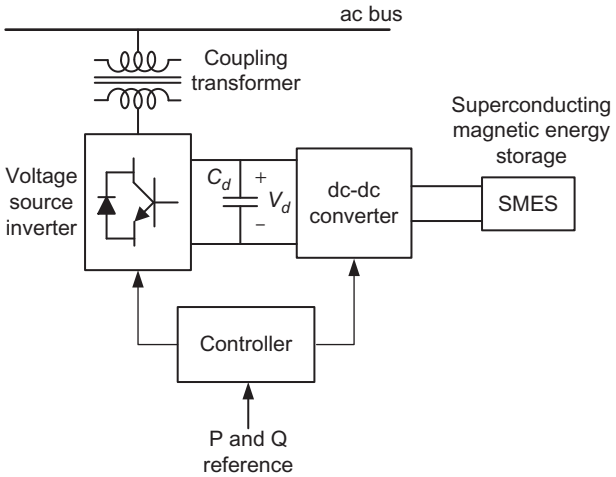


FIG. 28.33 STATCOM with SMES.

connected to the dc side of the STATCOM through a dc-dc converter, which converts the direct current in the superconductor magnet to dc voltage in the STATCOM dc side and vice versa. This STATCOM can control reactive power continuously and active power for a short time, normally up to few seconds, depending on the amount of energy stored in the superconducting magnet.

Comparison between SVC and STATCOM

Fig. 28.34A shows the steady-state volt-ampere characteristics for the SVC shown in Fig. 28.14, whereas Fig. 28.34B shows the same characteristics for a STATCOM. For operation at rated voltage, both devices can present similar characteristics in terms of control range. However, current compensation capability of SVC for lower voltages becomes smaller, whereas in the STATCOM, it does not change significantly for voltages lower than rated value (but approximately above 0.2 pu). This is explained by the fact that the SVC is based on impedance control, whereas the STATCOM is based on current controlled voltage source control. Therefore, in the SVC, the current decreases with a corresponding voltage decrease, whereas in the STATCOM, the current capability of the converters depends only on the switching device used, so the maximum current can be kept unchanged even for a low voltage condition. This is an important characteristic, especially in applications where the voltage may drop (as in most cases), where the STATCOM presents a better performance.

28.4.2.2 Adjustable Speed Synchronous Condenser (ASSC)

The adjustable speed synchronous condenser is not exactly a FACTS compensator, as it contains an electric machine. However, it may be an interesting shunt device to compensate reactive power continuously and relatively large amounts of active power for a short time. The basic topology of this compensator is shown in Fig. 28.35. It is based on a double-fed machine with a conventional three-phase winding in the stator and a three-phase winding in the rotor. The latter is supplied by a three-phase converter connected back-to-back to a second converter, which is connected to the grid.

This configuration allows the generation of a rotating magnetic flux in the rotor, which depends on the rotor converter frequency. When the machine is rotating at synchronous speed, the rotor converter operates at zero frequency and the magnetic flux in the rotor is stationary with respect to the rotor itself. In this case, the compensator operates as a conventional synchronous condenser.

However, when the rotor speed is lower or higher than the synchronous speed (normally during transients), the rotor converter generates a field current with the necessary frequency to keep the stator and rotor fluxes synchronized—if the synchronous frequency is 60 Hz and the rotor is running, for instance, at 58 Hz, the rotor converter has to supply voltage or current at 2 Hz so as to synchronize the fluxes. Naturally, it would be more interesting to use field-oriented control [44] instead of scalar control to get a better performance.

This hybrid compensator may supply energy to the ac system, if rotor speed is decreased. This machine is designed to have relatively large rotor inertia so as to present a large inertia constant (which may be in the range of more than 10 s). It is also called adjustable speed rotary condenser [45]. Operation at speeds higher than the synchronous speed is also possible, if it is necessary to absorb energy from the grid.

One of the advantages of this device is that a compensator with power in the range of 400 MVA may be synthesized with power electronics converter rated at a small fraction of this power and with a large capability to supply both active (for a few seconds) and reactive power (continuously) [45].

28.4.2.3 Static Synchronous Series Compensator

In contrast to the STATCOM, which is a shunt FACTS compensator, it is possible to build a converter-based compensator for series compensation. Fig. 28.36 shows the basic diagram of a static synchronous series compensator (SSSC) based on voltage

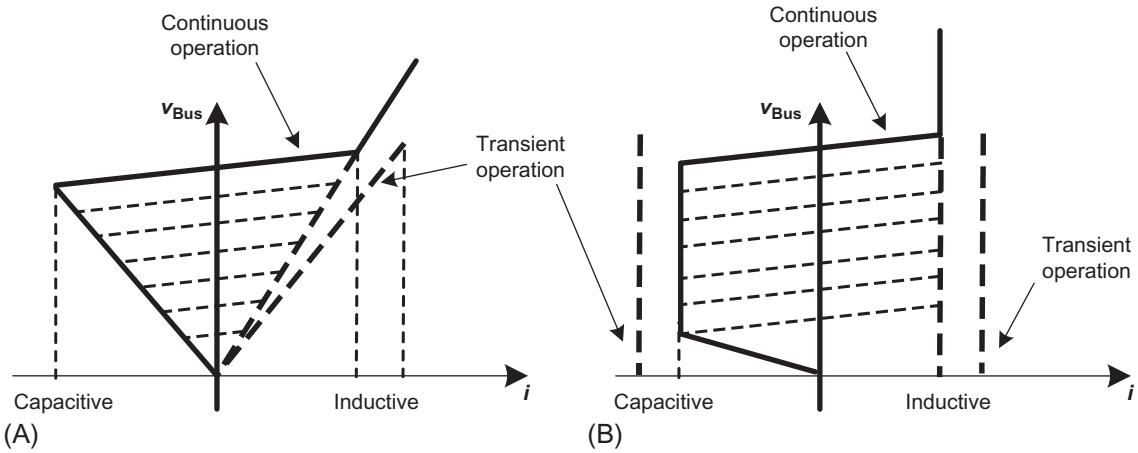


FIG. 28.34 Comparison between volt-ampere characteristics of (A) SVC and (B) STATCOM.

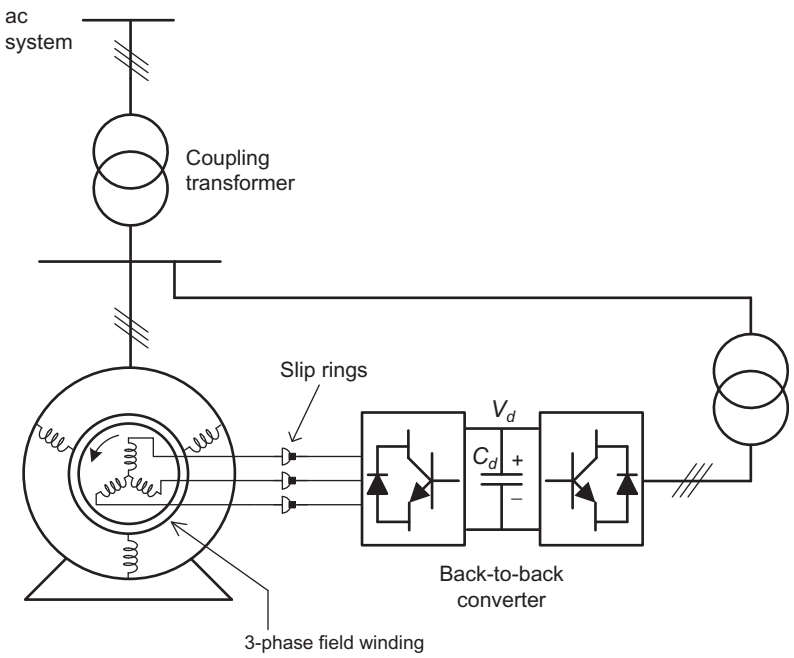


FIG. 28.35 Adjustable speed synchronous condenser (ASSC).

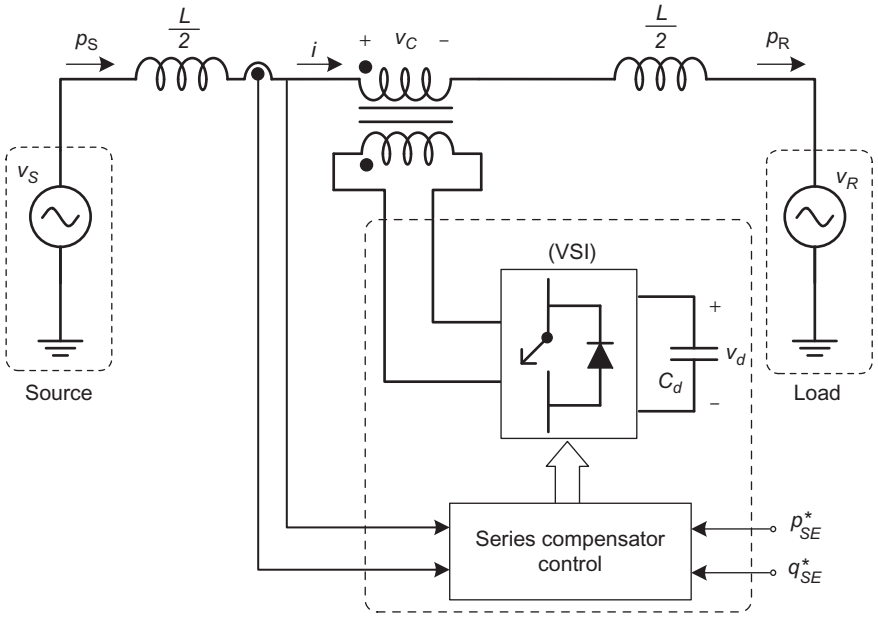


FIG. 28.36 Static synchronous series compensator (SSSC).

source converter (VSC) with a capacitor in its dc side and connected in series with the transmission line through a transformer [46]. The inputs to the SSSC controller shown in this figure are the line current and voltage and the active and reactive power references p^*_{SE} and q^*_{SE}, respectively. In general, only reactive power is compensated, and in this case, the active power reference p^*_{SE} is zero and q^*_{SE} is chosen so as to control power flow. Naturally, in the case of power flow control, it is necessary to have another control loop for this purpose and this is not shown in the figure.

One should note that if current is flowing in the transmission line, the SSSC controls reactive power by generating voltage v_C in quadrature with the line current. The device then shows capacitive or inductive equivalent impedance by increasing or decreasing the power flow, respectively. The compensation characteristic is as shown in Fig. 28.8, for the case of series

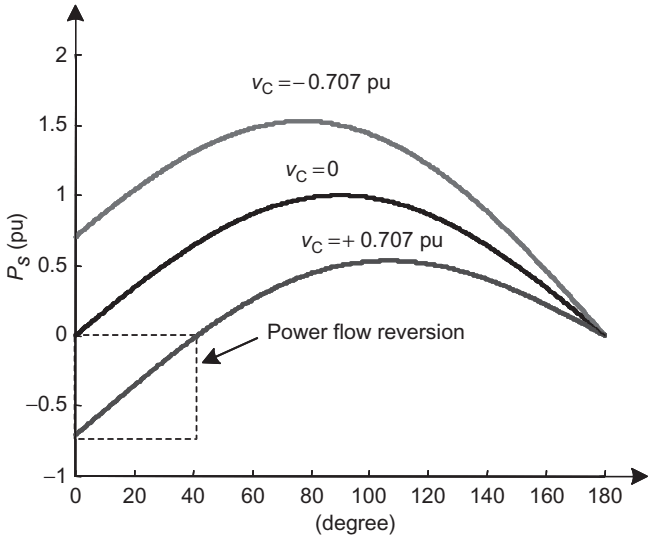


FIG. 28.37 Power flow characteristics for voltage-controlled SSSC.

compensation where the transmitted power is always positive for $0 < \delta < 180$ degrees. That is, with reactive power control, it is only possible to transmit in one direction. However, if instead of controlling q^*_{SE}, voltage v_C is controlled, it is possible to have power flow reversion. Fig. 28.37 shows the power flow characteristics of a transmission line with an SSSC using constant voltage control. The voltage is in quadrature with the current, and its magnitude is kept constant. The figure shows that it is possible to have power flow reversion for small values of δ with a constant compensation voltage v_C.

It should be noted that the discussion presented with respect to the converters topologies and controllers for the case of the STATCOM is also valid for the case of the SSSC. The SSSC can be used for power flow control and for power oscillation damping as well.

28.4.2.4 Gate-Controlled Series Capacitor

Fig. 28.16 shows the TCSC, which is basically a TCR in parallel with a capacitor and both connected in series with a transmission line. The combination is effective in continuously controlling the equivalent capacitive reactance presented to the system, mainly for power flow control and power oscillation damping purposes. It was also pointed out that the device has the disadvantage of a resonant condition due to the parallel association of capacitor and TCR (see Fig. 28.18).

In [47], the continuously regulated series capacitor using GTO thyristors to directly control capacitor voltage is presented. Fig. 28.38 shows this new device that is called gate-controlled series capacitor (GCSC) [48], hereafter renamed as the gate-controlled series capacitor (GCSC) because it may also be built using other self-commutated switches such as IGBTs or IGCTs.

The GCSC circuit consists of a capacitor and a pair of self-commutated switches in antiparallel connection. As the

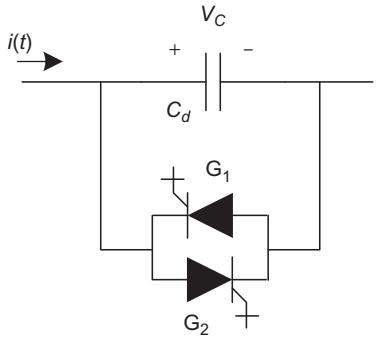


FIG. 28.38 Gate-controlled series capacitor.

switches operate under ac voltage, they must be able to block both direct and reverse voltages and allow current control in both directions.

Fig. 28.39 shows the voltage and current waveforms for the GCSC, where the current in the transmission line is assumed to be sinusoidal. If the switches are kept turned on, the capacitor is bypassed and does not present any compensation effect. If they are kept off, the capacitor is fully inserted in the line. On the other hand, if the switches are conducting and are turned off at a given blocking angle γ counted from the zero crossings of the line current, the capacitor voltage v_C appears as a result of the integration of the line current passing through it. The next time the capacitor voltage crosses zero, the switches are turned on again, to be turned off at the next turn-off angle γ. With this switching control sequence, it must be clear that the switches always switch at zero voltage. This is an interesting feature for the series connection of the switches under high-voltage operation [49].

The GCSC has some advantages when compared with the TCSC—the blocking angle can be continuously varied, which in turn varies the fundamental component of the voltage v_C. Also, it can be smaller than the TCSC [50]. Moreover, the dynamic response of the GCSC is generally better than that of the TCSC [51].

The impedance of the GCSC at the fundamental frequency, as a function of the blocking angle γ, is shown in Fig. 28.40.

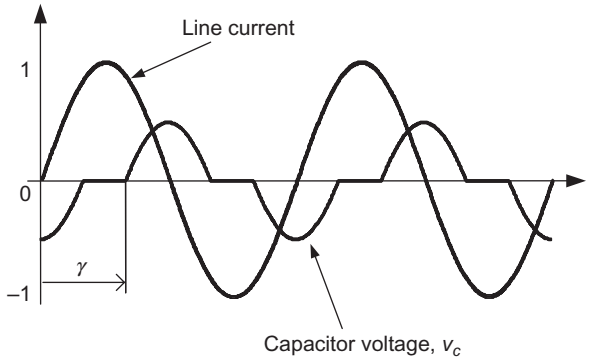


FIG. 28.39 GCSC voltage and current waveforms.

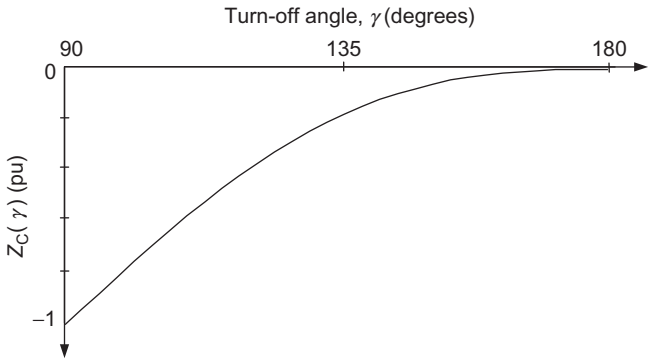


FIG. 28.40 GCSC equivalent fundamental impedance.

A blocking angle of 90 degrees means the capacitor is fully inserted in the circuit, whereas a value of 180 degrees corresponds to a situation where the capacitor is bypassed and no compensation occurs.

28.4.2.5 Unified Power Flow Controller

The unified power flow controller (UPFC) is a more complete transmission line compensator [52], shown as a simplified block diagram in Fig. 28.41. This device can be understood as a STATCOM and an SSSC with a common dc link. The energy storing capacity of the DC capacitor is generally small, and so the shunt converter has to drain (or inject) active power from the grid in exactly the same amount as the active power being injected (or drained) by the series converter. If this is not followed, the dc-link voltage may increase or decrease with respect to the rated voltage, depending on the net power being absorbed or delivered by both converters. On the other hand, the reactive power in the shunt or series converter can be controlled independently, giving a great flexibility to the power flow control.

The phasor diagram in Fig. 28.42 shows that the UPFC can be controlled in such a way as to produce any voltage phasor in series with the transmission line that fits inside the dashed-line

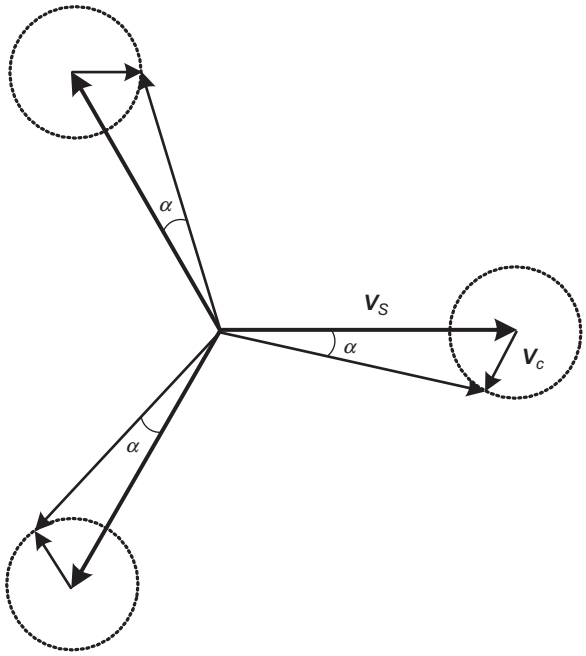


FIG. 28.42 Phasor diagram for a system with a UPFC.

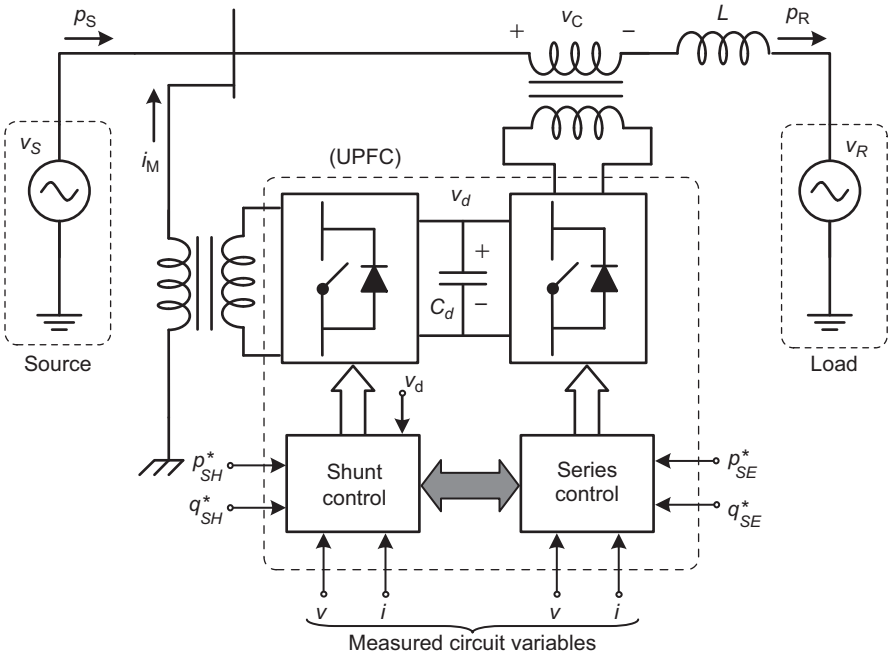


FIG. 28.41 UPFC block diagram.

circle on top of the phase voltage phasors. The maximum radius of the circle is limited by the voltage limitation of the series converter. The fact that the locus of v_c is a circle is one of the greatest advantages of the UPFC when compared with the thyristor-based phase shifter. If the UPFC presents capacitive or inductive reactive power in parallel with the system, the magnitude of voltage V_S is increased or decreased, respectively. This extra characteristic increases the locus of the series voltage v_c. Of course, this effect is only possible if an inductive impedance is present in series with the voltage source V_S, which is normally the case.

The shunt compensator of the UPFC is normally used with two objectives. The first is to control the reactive power in the point of connection, therefore controlling the voltage at this point. The second is to control active power in such a way as to control the dc-link voltage. The control technique to be used can be similar to the one used in STATCOM. The series compensator can be controlled in the same way as the SSSC, with the difference that in this case, it may control active and reactive power. Naturally, the active power control in the series compensator would change the capacitor voltage that should be controlled by the shunt compensator.

The UPFC can also be used to regulate directly the voltage in distribution feeder or transmission line. In the case that the UPFC is based on single-phase converter units (UPFC-1ϕ) [53,54], it can control unbalanced voltage. This application is named as direct voltage control (DVC) [55], and it is a promising solution for power quality issues in distribution grid with high penetration of intermittent generation sources, such as wind or solar power. Since this grid has a resistive characteristic, the indirect voltage control, based on shunt reactive compensator, could be ineffective [56]. Moreover, the use of single-phase converters permits the direct voltage control even under unbalanced operation, and each phase voltage can be controlled independently to balance the grid voltage.

Fig. 28.43 shows the basic line diagram of the UPFC based on single-phase back-to-back VSC unit for phase *a*. In each phase, one converter (VSC 1a) is shunt connected to the grid through a transformer (T_{sh}), and the other converter (VSC 2a) is directly connected in series at the point that voltage should be controlled (PCC). In Fig. 28.43, each VSC is connected in series with the secondary windings of the grid transformer (T_{grid}), avoiding a coupling transformer. The series converter of each UPFC 1ϕ is controlled to synthesize a compensation voltage (V_{comp}) to keep the PCC voltage regulated at a reference value, that is,

$$\dot{V}_{PCC_j} = \dot{V}_{T2_j} + \dot{V}_{comp_j} \tag{28.12}$$

where $\dot{V}_{T2_j}$ ($j = a, b, c$) is the phasor of voltage phase "j" in secondary wind of the transformer and $\dot{V}_{comp_j}$ is the phasor of the compensation voltage synthetized by the series VSC connected to phase "j." The compensation voltage can be represented as

$$\dot{V}_{comp_j} = \dot{k}\,\dot{V}_{2_j} \tag{28.13}$$

where $\dot{k}$ is the complex compensation factor, which means that both the magnitude and the phase of the compensation voltage can be controlled independently in each phase. This feature is suitable for grids with unbalanced voltage issues. If only the magnitude of the voltage in each phase should be compensated, the compensation factor is a real number, which means that the compensation voltage, $\dot{V}_{comp_j}$, is in phase to the secondary phase voltage of the grid transformer, $\dot{V}_{T2_j}$, and a simple control strategy can be applied as shown in Fig. 28.44. This figure shows the control block diagram of the series VSC for direct voltage magnitude compensation for one phase. The rms value of the PCC phase voltage ($V_{PCC\,rms_j}$) is compared with the reference value ($V_{rms\ ref}$); the output error is processed by a PI controller, generating the compensation voltage magnitude. This signal is multiplied by a sinusoidal signal, sin(θ_{PLL}), in phase with secondary phase voltage of the grid transformer, $\dot{V}_{T2_j}$, obtained from the synchronizing circuit (phase locked loop (PLL)).

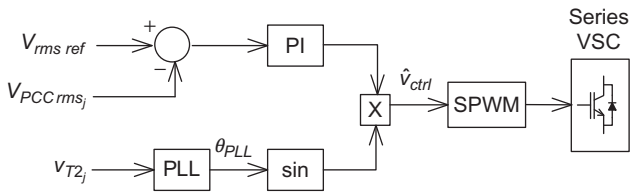


FIG. 28.44 Voltage control block diagram for the series VSC (magnitude compensation only).

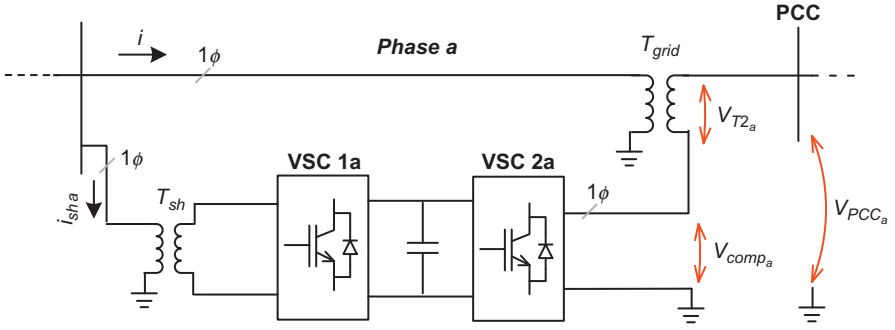


FIG. 28.43 Direct voltage control using UPFC 1ϕ units.

28.4.2.6 Interline Power Flow Controller

The interline power flow controller (IPFC) [53] is a UPFC-derived device with the objective of controlling power flow between two lines instead of one line as in the UPFC. Fig. 28.45 shows a basic block diagram of an IPFC with two converters to control the power flow in lines 1 and 2. The minimum number of converters connected back-to-back is two, but there may be more. Each converter should be connected in series with a different transmission line and should control power flow in this line with the following conditions:

- The reactive power control can be totally independent in each converter.
- The active power flowing into or out of each converter has to be coordinated in such a way that the dc-link voltage is kept controlled.

The dc-link voltage control can be achieved in a similar way as in the case of the UPFC. In this case, one of the series converters can control the compensation voltage freely, and it may produce active power flowing into or from the dc link, which would charge or discharge the dc-link capacitor. Therefore, the other converter has to be controlled to regulate this dc voltage. If there are n converters with n greater than two, $(n-1)$ converters can absorb or generate active power, whereas one converter has to control the dc-link voltage. Anyway, all n converters can control reactive power freely. For instance, this concept allows the control of the power flow in n lines, and it is possible to transfer active power from one line to another to balance power flow in n parallel transmission lines.

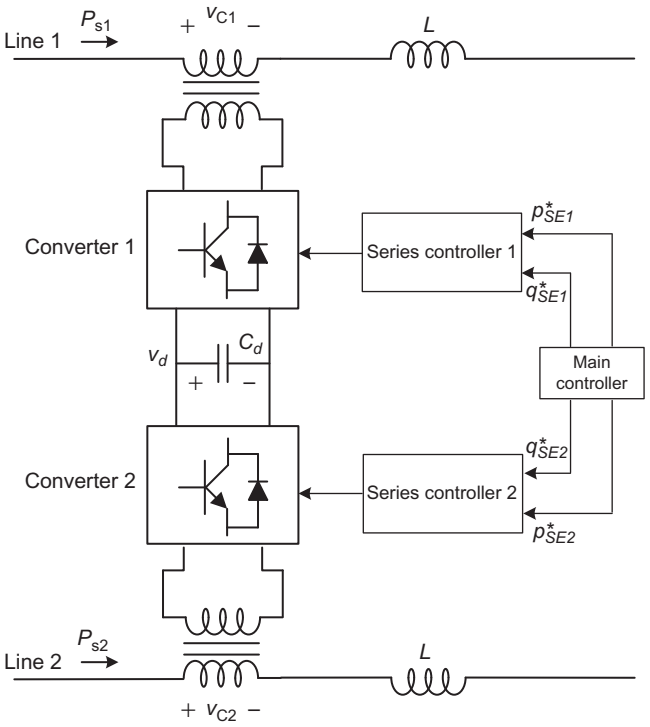


FIG. 28.45 Block diagram of IPFC with two converters.

28.4.2.7 Convertible Static Converter

Following the IPFC, a more generic concept is the convertible static converter (CSC) [57,58], which is based on the connection of a voltage source converter in various different topologies. Considering one simple case of two transmission lines and two converters with apparent power each equals to S, it is possible to have the following topologies:

- Two converters connected in shunt operating as a STATCOM rated at $2S$ apparent power
- Two converters connected in series with one transmission line forming an SSSC with $2S$ apparent power
- One converter connected in shunt and the other in series forming a UPFC
- One converter connected in series with one line and the other connected in series with the other line forming an IPFC

Other topologies are possible depending on how the converters are connected in the system. The basic control of each converter depends on how it is being used if, as a STATCOM, SSSC, UPFC, or IPFC.

28.5 Ancillary Services

Ancillary services are essential for grid reliability, including these services that can facilitate wind farms obtaining connection permits in some countries. Thus, taking advantage of the current scenario with high penetration of wind turbines in the distribution and transmission systems in several regions throughout the world, more and more, these services are being incorporated into the modern wind farms. These services include voltage and reactive power support, frequency-active power control, and fault ride through capability. This is all possible thanks to the ability of modern wind turbines to make use of FACTS controller features. Nowadays, most of wind farms are based on doubly fed induction generator (DFIG) or permanent magnet synchronous generator (PMSG). However, solar photovoltaic power plants can also contribute to these services, since they are connected to the grid via power inverters [59]. So, photovoltaic and wind turbine power plants can contribute to increase the reliability of distribution and transmission systems, as indicated in Fig. 28.46.

Modern grid codes define a range of technical requirements that generation power plants must fulfill. For example, it is very common in the voltage support through reactive current injection during fault operation and the voltage support of the power system in normal operation through the

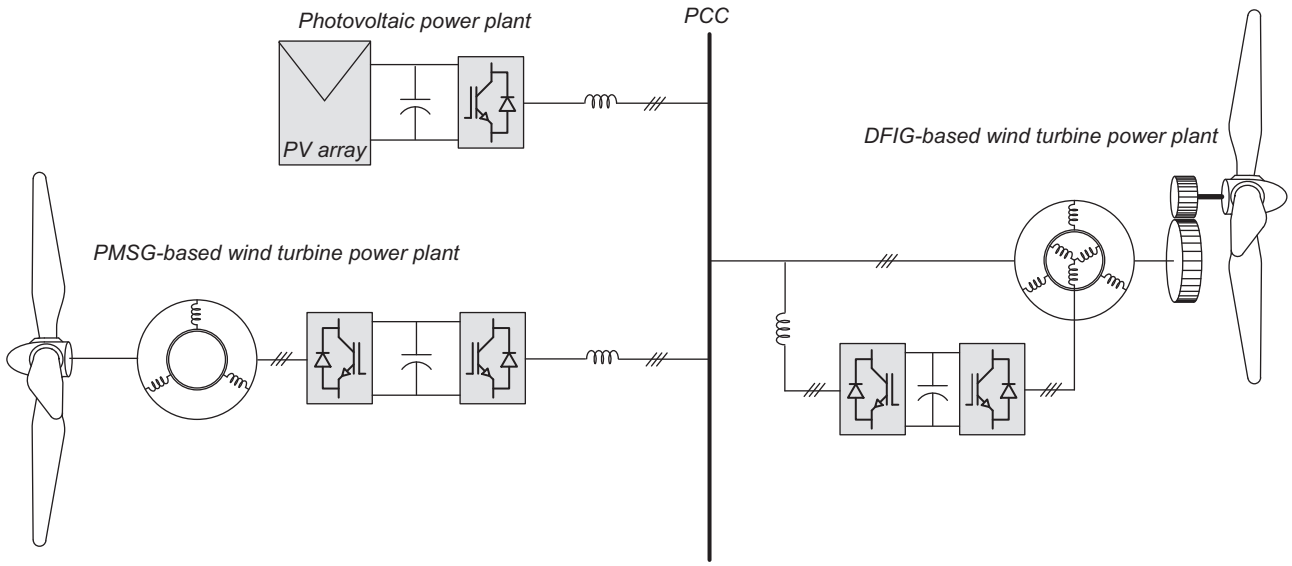


FIG. 28.46 Photovoltaic and wind turbine power plants connected to the grid.

reactive power control. Advanced control designs associated with power electronics converters are responsible to provide these ancillary services [59,60].

Wind turbines connected to the grid through a static power converter can provide an adequate inertial response to the system. The idea behind that is that the converter control system ensures a resistant torque to the wind turbine shaft during a frequency disturbance to extract energy. Thus, the behavior of synchronous generator with large inertia can be emulated [61–65].

Generally, a photovoltaic power plant has no energy storage; therefore, it cannot emulate an inertia, so it cannot contribute by itself to increasing the inertia of the system. Unless it uses other components like a flywheel or a battery to allow this service [61].

References

[1] N.G. Hingorani, Power electronics in electric utilities: role of power electronics in future power systems, Proc. IEEE 76 (4) (1988) 481–482.

[2] N.G. Hingorani, L. Gyugyi, Understanding Facts—Concepts and Technology of Flexible AC Transmission Systems, IEEE Press, New York, 1999.

[3] E.W. Kimbark, Direct Current Transmission, Wiley-Interscience, New York, 1971.

[4] N. Mohan, T.M. Undeland, W.P. Robins, Power Electronics—Converters, Applications and Design, John Wiley & Sons, Inc., New York, 2003.

[5] M.H. Rashid, Power Electronics, Circuits, Devices, and Applications, third ed., Prentice Hall, 2003.

[6] J. Rabkowski, D. Peftitsis, H.P. Nee, Silicon carbide power transistors: a new era in power electronics is initiated, IEEE Ind. Electron. Mag. 6 (2) (2012) 17–26, http://dx.doi.org/10.1109/MIE.2012.2193291.

[7] B.K. Bose, Power Electronics and Motor Drives: Advances and Trends, Elsevier Inc, 2006.

[8] A. Yazdani, R. Iravani, Voltage-Sourced Converters in Power Systems, Wiley-IEEE Press, 2010.

[9] L. Gyugyi, Emerging Practices in Technology: Solid-State Synchronous Voltage Sources for Dynamic Compensation and Real Time Control AC Transmission Lines, IEEE Standards Press, 1993.

[10] A.A. Edris, R. Adapa, M.H. Baker, L. Bhomann, K. Clark, K. Habashi, L. Gyugyi, J. Lemay, A.S. Mehraban, A.K. Myers, J. Reeve, F. Sener, D. R. Togerson, R.R. Wood, Proposed terms and definitions for flexible AC transmission systems (FACTS), IEEE Trans. Power Del. 12 (4) (2002) 1848–1853.

[11] C. Wei-Nan, C.-J. Wu, Developing static reactive power compensators in a power system simulator for power education, IEEE Trans. Power Syst. 10 (4) (1995) 1734–1741.

[12] T. Hasegawa, Y. Aoshima, T. Sato, Development of 60 MVA SVC (static var compensator) using large capacity 8 kV and 3.5 kA thyristors, in: IEEE Power Converter Conference—PCC-Nagaoka, 1997, pp. 725–730.

[13] A.J.F. Deri, B.J. Ware, R.A. Byron, A.S. Mehraban, M. Chamia, P. Halvarsson, L. Ängquist, Improving transmission system performance using controlled series capacitors, in: Cigré Joint Session 14/37/38-07, Paris, France, 1992.

[14] N. Christl, R. Hedin, K. Sadek, P. Lützelberger, P.E. Krause, S. M. McKenna, A.H. Montoya, D. Torgerson, Advanced series compensation (ASC) with thyristor controlled impedance, in: Cigré Joint Session 14/37/38-05, Paris, France, 1992.

[15] C. Gama, Brazilian north–south interconnection control application and operating experience with a TCSC, in: IEEE—PES Summer Meeting, vol. 2, 1999, pp. 1103–1108.

[16] K. Xing, G.L. Kusic, Damping sub-synchronous resonance by phase shifters, IEEE Trans. Energy Conver. 4 (3) (1989) 344–350.

[17] S. Nyati, M. Eitzmann, J. Kappenman, D. VanHouse, N. Mohan, A. Edris, Design issues for a single core transformer thyristor controlled phase-angel regulator, IEEE Trans. Power Del. 10 (4) (1995) 2013–2019.

[18] D.G. Holmes, T.A. Lipo, Pulse Width Modulation for Power Converters: Principles and Practice, Wiley-IEEE Press, 2003.
[19] S. Mori, K. Matsuno, M. Takeda, M. Seto, Development of a large static var generator using self-commutated inverters for improving power system stability, IEEE Trans. Power Del. 8 (1) (1993) 371–377.
[20] C. Schauder, M. Gernhardt, E. Stacey, T. Lemak, L. Gyugyi, T. W. Cease, A. Edris, Development of a /spl plusmn/100 Mvar static condenser for voltage control of transmission system, IEEE Trans. Power Del. 10 (3) (1995) 1486–1496.
[21] G. Reed, J. Paserba, T. Croasdaile, M. Takeda, Y. Hamasaki, T. Aritsuka, N. Morishima, S. Jochi, et al., The VELCO STATCOM based transmission system project, in: IEEE Power Engineering Society Winter Meeting, 2001, vol. 3, 2001, pp. 1109–1114.
[22] C. Qian, M.L. Crow, A cascade converter-based STATCOM with energy storage, in: IEEE PES Winter Meeting, vol. 1, 2002, pp. 544–549.
[23] A. Lesnicar, R. Marquardt, An innovative modular multilevel converter topology suitable for a wide power range, in: IEEE Power Tech Conference Proceedings, Bologna, 23–26 June, vol. 3, 2003, p. 6.
[24] J. Dorn, H. Huang, D. Retzmann, Novel voltage-sourced converters for HVDC and FACTS applications, in: Cigré Symposium, Osaka, Japan, 2008.
[25] H. Huang, Multilevel voltage-sourced converters for HVDC and FACTS applications, in: Cigré SC B4 Colloquium, Bergen and Ullensvang, Norway, 2009.
[26] D. Soto, T. Green, A comparison of high-power converter topologies for the implementation of FACTS controllers, IEEE Trans. Ind. Electron. 49 (5) (2002) 1072–1080.
[27] J. Kuang, B. Ooi, Series connected voltage-source converter modules for force-commutated SVC and DC-transmission, IEEE Trans. Power Del. 9 (2) (1994) 977–983.
[28] Ferreira, J.R.B.L., Direct Current Transmission Based on Modular Multilevel Converter, PhD. Thesis, (in Portuguese), Federal University of Rio de Janeiro, Rio de Janeiro, 2014.
[29] S. Allebrod, R. Hamerski, R. Marquardt, New transformerless, scalable modular multilevel converters for HVDC-transmission, in: IEEE Power Electronics Specialists Conference, 2008, PESC 2008, 2008, pp. 174–179.
[30] C. Schauder, H. Mehta, Vector analysis and control of advanced static var compensators, IEE Proc. Gener. Transm. Distrib. 140 (4) (1993) 299–306.
[31] Buchholz, F., Das Begriffsystem Rechtleistung. Wirkleistung, totale Blindleistung. Selbstverlag München, 1950.
[32] M. Depenbrock, The FBD-method, a generally applicable tool for analyzing power relations, IEEE Trans. Power Syst. 8 (2) (1993) 381–387.
[33] M. Takeda, et al., Development of an SVG series for voltage control over three-phase unbalance caused by railway load, in: Proc. International Power Electronics Conference—IPEC-Yokohama'95, Yokohama, Japan, 1995, pp. 603–608.
[34] C. Hochgraf, R.H. Lasseter, STATCOM controls for operation with unbalanced voltages, IEEE Trans. Power Del. 13 (2) (1998) 538–544.
[35] G.F. Reed, J.E. Greaf, T. Matsumoto, Y. Yonehata, M. Takeda, T. Aritsuka, Y. Hamasaki, F. Ojima, A.P. Sidell, R.E. Chervus, C.K. Nebecker, Application of a 5 MVA, 4.16 kV D-STATCOM system for voltage flicker compensation at Seattle iron and metals, in: IEEE Power Engineering Society Summer Meeting 2000, vol. 3, 2000, pp. 1605–1611.
[36] H. Akagi, Y. Kanazawa, A. Nabae, Instantaneous reactive power compensators comprising switching devices without energy storage components, IEEE Trans. Ind. Appl. IA-20 (3) (1984) 625–630.
[37] E.H. Watanabe, R.M. Stephan, M. Aredes, New concepts of instantaneous active and reactive power for three phase system and generic loads, IEEE Trans. Power Del. 8 (2) (1993) 697–703.
[38] H. Akagi, E.H. Watanabe, M. Aredes, Instantaneous Power Theory and Application to Power Conditioning, Wiley-IEEE Press, 2007.
[39] F. Ichikawa, et al., Operating experience of a 50 MVA self-commutated SVC at the Shin–Shimano Substation, in: Proc. International Power Electronics Conference—IPEC-Yokohama'95, Yokohama, Japan, 1995, pp. 597–602.
[40] C. Schauder, STATCOM for compensation of large electric arc furnace installations, in: IEEE Power Engineering Society Summer Meeting 1999, vol. 2, 1999, pp. 1109–1112.
[41] C. Shen, Z. Yang, M.L. Crow, S. Atcitty, Control of STATCOM with energy storage device, in: IEEE Power Engineering Society Winter Meeting 2000, vol. 4, 2000, pp. 2722–2728.
[42] A.B. Arsoy, Y. Liu, P.F. Ribeiro, F. Wang, STATCOM-SMES, IEEE Ind. Appl. Mag. 9 (2) (2003) 21–28.
[43] M.G. Molina, P.E. Mercado, E.H. Watanabe, Dynamic performance of a static synchronous compensator with superconducting magnetic energy storage, in: IEEE Power Electronics Specialist Conference—PESC'2005, 2005, pp. 224–230.
[44] W. Leonhard, Control of Electrical Drives, third ed., Springer, 2001.
[45] H. Akagi, The state-of-the-art of power electronics in Japan, IEEE Trans. Power Electron. 13 (2) (1998) 345–356.
[46] L. Gyugyi, C.D. Schauder, K.S. Kalyan, Static synchronous series compensator: a solid-state approach to the series compensation of transmission lines, IEEE Trans. Power Del. 12 (1) (1997) 406–417.
[47] G.G. Karady, T.H. Ortmeyer, B.R. Pilvelait, D. Maratukulam, Continuous regulated series capacitor, IEEE Trans. Power Del. 8 (3) (1993) 1348–1354.
[48] L.F.W. de Souza, E.H. Watanabe, M. Aredes, GTO controlled series capacitors: multi-module and multi-pulse arrangements, IEEE Trans. Power Del. 15 (2) (2000) 725–731.
[49] E.H. Watanabe, M. Aredes, L.F.W. de Souza, M.D. Bellar, Series connection of power switches for very high-power applications and zero voltage switching, IEEE Trans. Power Electron. 15 (1) (2000) 44–50.
[50] L.F.W. de Souza, E.H. Watanabe, J.E.R. Alves, L.A.S. Pilotto, Thyristor and gate controlled series capacitors: comparison of components rating, in: IEEE Power Engineering Society General Meeting, Toronto, Canada, 2003, pp. 2542–2547.
[51] S. Banerjee, J.K. Chatterjee, S.C. Triphathy, Application of magnetic energy storage unit as continuous VAR controller, IEEE Trans. Energy Conver. 5 (1) (1990) 39–45.
[52] L. Gyugyi, Unified power-flow control concept for flexible AC transmission systems, IEE Proc. C 139 (4) (1992) 323–331.
[53] S.L. Silva Lima, UPFC for Voltage Control. PhD. Thesis, (in Portuguese), Federal University of Rio de Janeiro, Rio de Janeiro, 2013.
[54] S.L. Silva Lima, R.F.S. Dias, E.H. Watanabe, Direct voltage control in grids with intermittent sources using UPFC, Power Electron. Mag. SOBRAEP 19 (3) (2014) 260–267.
[55] W.S.J.P. da Costa, W. Kruschel, P. Zacharias, Power electronics for voltage control in distribution networks, in: 16th Kassel Symposium on Energy Systems Technology, 2011, pp. 1–15.
[56] D. Geibel, T. Degner, B. Engel, J.P. da Costa, W. Kruschel, T. Reimann, T. Blo, B. Sahan, P. Zacharias, Active intelligent

distribution networks coordinated voltage regulation methods for networks with high share of decentralised generation, in: 2012 CIRED Workshop, Lisbon, 2012, pp. 1–4.
[57] A.A. Edris, S. Zelinger, L. Gyugyi, L.J. Kovalsky, Squeezing more power from the grid, IEEE Power Eng. Rev. 22 (6) (2002) 4–6.
[58] E. Uzunovic, B. Fardanesh, L. Hopkins, B. Shperling, S. Zelingher, A. Schuff, NYPA convertible static compensator (CSC) application phase I: STATCOM, in: IEEE—PES Transmission and Distribution Conference and Exposition, 2, 2001, pp. 1139–1143.
[59] I.D. Margaris, A.D. Hansen, P. Sørensen, N.D. Hatziargyriou, Illustration of modern wind turbine ancillary services, Energies 3 (6) (2010) 1290–1302.
[60] A. Zertek, G. Verbic, M. Pantos, A novel strategy for variable-speed wind turbines' participation in primary frequency control. IEEE Trans. Sustain. Energy 3 (4) (2012) 791–799, http://dx.doi.org/10.1109/TSTE.2012.2199773.
[61] G. Revel, A.E. Leon, D.M. Alonso, J.L. Moiola, Dynamics and stability analysis of a power system with a PMSG-based wind farm performing ancillary services, IEEE Trans. Circ. Syst. I: Reg. Papers 61 (7) (2014) 2182–2193, http://dx.doi.org/10.1109/TCSI.2014.2298281.
[62] E. Ela, et al., Effective ancillary services market designs on high wind power penetration systems, in: 2012 IEEE Power and Energy Society General Meeting, 2012.
[63] J. MacDowell, S. Dutta, M. Richwine, S. Achilles, N. Miller, Serving the future: advanced wind generation technology supports ancillary services, IEEE Power Energy Mag. 13 (6) (2015) 22–30, http://dx.doi.org/10.1109/MPE.2015.2461331.
[64] F. Baccino, F. Conte, S. Grillo, S. Massucco, F. Silvestro, An optimal model-based control technique to improve wind farm participation to frequency regulation, IEEE Trans. Sustain. Energy 6 (3) (2015) 993–1003, http://dx.doi.org/10.1109/TSTE.2014.2327243.
[65] L. Ruttledge, D. Flynn, Emulated inertial response from wind turbines: gain scheduling and resource coordination, IEEE Trans. Power Syst. 31 (5) (2016) 3747–3755, http://dx.doi.org/10.1109/TPWRS.2015.2493058.

Further Reading

[66] L. Gyugyi, C.D. Schauder, K.S. Kalyan, The interline power flow controller concept: a new approach to power flow management in transmission systems, IEEE Trans. Power Del. 14 (3) (1999) 1115–1123.
[67] B.R. Andersen, L. Xu, P.J. Horton, P. Cartwright, Topologies for VSC transmission, Power Eng. J. 16 (3) (2002) 142–150.
[68] N. Flourentzou, V.G. Agelidis, G.D. Demetriades, VSC-based HVDC power transmission systems: an overview, IEEE Trans. Power Electron. 24 (3) (2009) 592–602.
[69] M.P. Bahrman, B.K. Johnson, The ABCs of HVDC transmission technologies, IEEE Power Energy Mag. 5 (2) (2007) 32–44.
[70] J.A. Baroudi, V. Dinavahi, A.M. Knight, A review of power converter topologies for wind generators, Renew. Energy 32 (14) (2007) 2369–2385.

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Section V

Motor Drive

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29

Drive Types and Specifications

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29.1 An Overview

29.1.1 Introduction

In every industry, there are industrial processes of some form, which require adjustments for either normal operation or optimum performance. Such adjustments are usually accomplished with a variable speed drive (VSD) system. They are an important part of automation. They help to optimize the process, reduce investment costs, energy consumption, and energy cost.

There are three basic types of VSD systems: electric drives, hydraulic drives, and finally mechanical drives. This chapter focuses mainly on electric drives.

A typical electric VSD system consists of three basic components: the electric motor, the power converter, and the control system, as illustrated in Fig. 29.1. The electric motor is connected directly or indirectly (through gears) to the load. The power converter controls the power flow from an AC supply (often via a supply transformer) to the motor by appropriate control of power semiconductor switches (part of the power converter).

With recent advances of power semiconductor and converter topologies, electric VSDs are witnessing a revolution in applications including computer peripheral drives, machine tools and robotic drives, test benches, fan pumps and compressors, paper mill drives, automation, traction and ship propulsion, and cement mill and rolling mill drives.

For a proper control system, the VSD system variables, both mechanical and electric, are required for control and protection. Signals are usually derived from sensors, whose outputs are very much dependent on the control strategy employed and the functionality required.

This chapter introduces electric VSDs and briefly describes their benefits. It examines their classifications from different perspectives. Their specification requirement to meet

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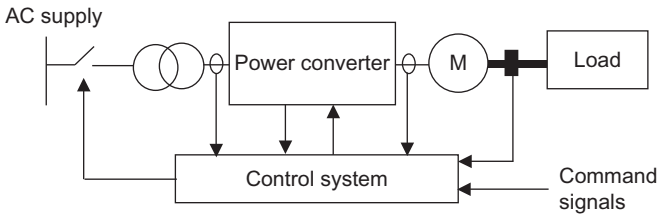


FIGURE 29.1 VSD schematic diagram.

applications of different industries is briefly outlined. Various VSD topologies have been carefully examined and compared with each other. A selection of modern VSD applications are examined and briefly commented upon.

29.1.2 Historical Review

In order to appreciate electric VSDs, significant dates in the evolution of electric drives are summarized in Table 29.1 [1].

The increased popularity of electric VSD systems, witnessed in recent years, may be explained by the many advantages a VSD can offer. Such advantages include operation at speeds significantly different from the synchronous speed, energy saving, reduced mechanical shock, improved process performance, improved efficiency, reduced mechanical wear, increased plant life, reduced total ownership costs, reduced system fault levels, and reduced AC disturbances in certain applications. Furthermore, modern electric drives are equipped with many features, including serial communication, remote control, diagnostics, and trip history. In the low-voltage low-power arena, packaged electric drives are becoming a commodity product. The disadvantages of such a system are also recognized. They include the need for extra space to accommodate the equipment, cooling, capital cost, noise, and power system harmonic effects. The following is a brief review of some of the benefits and drawbacks of VSDs.

TABLE 29.1 Historical review

Year	Key advancement
1886	The birth of the electric variable speed drive system represented by Ward-Leonard system
1889	The invention of squirrel cage induction motor
1890	The slip-ring induction motor drive—speed control via rotor resistance control
1904	Kramer drives—introduce a DC link between the slip rings and the AC supply
1911	Variable speed system based on induction motor with a commutator on the rotor
1923	Ignitron made controlled rectification possible
1928	The invention of thyratron and grid-controlled mercury-arc rectifiers
1930	DC-to-AC power inversion
1931	AC-to-AC power conversion by cycloconverters
1950	Silicon-based power switches
1960	Thyristors (SCRs) became available, and variable speed drives began
1961	Back-to-back reversing DC drive introduced
1960s	Power semiconductor voltage and current ratings grew and performance characteristics improved
1970	The concept of packaging industrial drives was introduced
1972	First integrated motors with DC converter
1973	Isolated thyristors packages
1970s	The principle of vector control (field-oriented control) evolved
1983	Plastic molding made their first significant impact on VSDs
1985	Direct torque control as a concept
1990	Integrated power modules
1992	A new packaging trend emerged
1996	Universal drives (a general purpose open-loop vector drive, a closed-loop flux vector drive, and a servo drive)
1998	Complete AC/AC integral converter up to 15 kW
1998	Medium-voltage pulse-width-modulated voltage-source inverter drives—became a commercial product

29.1.3 Advantages of VSD

The author suggests that VSDs benefit most industrial processes with some form of drive. The challenge has often been how to quantify these benefits. The energy saving potential of VSD can be easily quantified, particularly for fan and pump drive applications.

29.1.3.1 Energy Saving

Electric VSD provides savings in two ways: (a) directly by consuming less energy and (b) indirectly by improving the product quality. The latter is often more difficult to quantify.

Direct energy saving is possible only with centrifugal loads such as centrifugal pumps and fans. Such loads are often run at fixed speeds. Traditionally, an automatic valve, or some other mechanical means, is used to vary fluid flow rates in pumps. However, if a VSD is used, then the motor speeds can be controlled electronically to obtain a desired flow rate and can result in significant energy savings.

On the basis of the laws of affinity for centrifugal loads,

- the volume of flow is directly proportional to speed,
- pressure is proportional to the square of the speed,
- input power is proportional to the cube of the speed.

The affinity law states that the power consumption is proportional to the cube of the motor speed. This implies that if the speed is halved, then the power consumption is reduced to one-eighth. So, energy savings occur as the requirement for volume decreases. If, for example, a cooling system calls for operation at 50% airflow volume, it requires only 12.5% of the power needed to run the system at 100% volume. Because power requirements decrease faster than the reduction in volume, there is a potential for significant energy reduction at lower volume.

Generally, centrifugal pumps and fans are sized to handle peak volume requirements that typically occur for short periods. As a result, centrifugal pumps and fans mostly operate at reduced volumes.

Opening or closing of a damper allows the airflow of fans to be controlled. Restricting the airflow causes the motor to work hard even with a low throughput.

With a VSD, the speed of the fan can be reduced, thus giving the opportunity to reduce energy consumption. Adjusting the speed of the motor regulates the airflow. The control can be achieved by monitoring humidity, temperature, flow, etc. The lower the required throughput, the greater the energy saved.

It has been estimated that the payback period of a 50 kW fan or pump VSD equipment operating 2000 h/year is 1.9 years for operation at 75% speed and 1.23 years for 50% speed. It has been assumed that the cost of the VSD is £5.5 k and the cost of power is £0.05/kW.

29.1.3.2 Improved Process Control

Using VSDs to improve process control results in more efficient operating systems. The throughput rates of most industrial processes are functions of many variables. For example, throughput in continuous metal annealing depends on, among other factors, the material characteristics, the cross-sectional area of the material being processed, and the temperature of one or more heat zones. If constant speed motors are used to run conveyors on the line, it must either run without material during the time required to change the temperature in a heat zone or produce scrap during this period. Both choices waste energy or material.

With VSDs, however, the time needed to change speed is significantly less than the time it takes to change heat-zone temperature. By adjusting the material flow continuously to match the heat-zone conditions, a production line can operate continuously. The results are less energy use and less scrap metal.

29.1.3.3 Reduced Mechanical Stress (Soft Starts)

Starting a motor on line power increases stress on the mechanical system, for example, belts and chains. Direct on-line start-up of an induction motor is always associated with high inrush current with poor power factor.

VSD can improve the operating conditions for a system by giving a smooth, controlled start and by saving some energy during starting and running. Smoother start-up operation will prolong life and reduce maintenance, but it is difficult to do more than make an estimate of the cost advantages of these. The benefits of soft start, inherent in VSD, are that it eliminates the uncontrolled inrush of current that occurs when stationary motor is connected to full line voltage, and also the inevitable suddenly applied high start-up torque. Benefits are that the power wasted by current inrush is eliminated and that the life of the motor and the driven machine are prolonged by the gentle, progressive application of torque.

29.1.3.4 Improved Electrical System Power Factors

When a diode supply bridge is used for rectification, electric VSDs operate at near-unity power factor over the whole speed range (the supply delivers mostly real power). When a fully controlled thyristor supply bridge is used (as in DC, cyclo, and current source drives), the power factor starts at around 0.9 at full speed and proportionately worsens as speed declines due to front-end thyristors (typically 0.45 at 50% speed and 0.2 at 25% speed).

Modern pulse-width modulated (PWM) drives convert the three phases AC line voltage to a fixed-level DC voltage. They do this regardless of inverter output speed and power. The PWM inverters, therefore, provide a constant power factor regardless of the power factor of the load machine and the controller installation configuration, for example, by adding a reactor or output filter between the VSD and the motor.

29.1.4 Disadvantages of VSD

The cost of VSD is generally space, cooling, and capital cost. Some of the drawbacks are the following:

- Acoustic noise
- Motor derating
- Supply harmonics

The PWM voltage-source inverter (VSI) drives, equipped with fast-switching devices, add other possible problems such as (a) premature motor insulation failures, (b) bearing/earth current, and (c) electromagnetic compatibility (EMC).

29.1.4.1 Acoustic Noise

In some installations, placing a VSD on a motor increases the motor's acoustic noise level. The noise occurs when the drive's nonsinusoidal (current and voltage) waveforms produce vibration in the motor's laminations. The nonsinusoidal current and voltage waveforms produced by the VSD are the result of the transistor switching frequency and modulation in the DC-to-AC inverter. The switching frequency, fixed or variable, determines the audible motor noise. In general, the higher the carrier frequency, the closer the output waveform is to a pure sine wave. One method of reducing audible motor noise is full-spectrum switching (random switching frequency). The VSD manufacturers accomplish full-spectrum switching by an algorithm within the VSD controller. The motor performance is optimized by evaluating motor characteristics, including motor current, voltage, and the desired output frequency. The resulting frequency band, though audible to humans, produces a family of tones across a wide frequency band. So, the perceived motor noise is considerably less than it would be with a single switching frequency.

Motor noise may not present a problem. Relevant factors include motor locations and the amount of noise produced by other equipment. Traditionally, motor noise level is reduced by adding an LC filter between the VSD and the motor, that is, reducing the high-frequency component of the motor voltage waveform. Modern PWM inverter drives run at very high switching frequency and with random switching frequency thus reducing the noise level too. Various methods have been proposed to reduce the magnetically generated noise, which is radiated from inverter-fed induction motors.

29.1.4.2 Motor Heating

Most motor manufacturers design their products according to NEMA standards to operate on utility-supplied power. Designers base their motors' heating characteristics and cooling methods on power supplied at fixed voltage and frequency.

For many drive applications, particularly those requiring relatively low power, inverters with a high switching speed can produce variable voltage and variable frequency with little significant harmonic content. With these, either standard or high-efficiency induction motors can be used with little or no motor derating. However, the inverters used in larger drives have limits on switching rate that cause their output voltages to contain substantial harmonics of orders 5, 7, 11, 13, and so on. These, in turn, cause harmonic currents and additional heating (copper and iron losses) in the stator and rotor windings. These harmonic currents are limited mainly by the leakage inductance. For simple six-step inverters, the additional power losses, particularly those in the rotor, may require derating of the motor by 10%–15%.

Existing constant speed drives often have an oversized induction motor. These can usually be converted to variable speed operation using the original induction motor. Most of the subsequent operation will be at lower load and lower loss than that for which the motor was designed.

Modern PWM-VSI drives produce a voltage wave with negligible lower-order harmonics. The wave consists of pulses formed by switching at relatively high frequency between the positive and negative sides of the DC link voltage supply. With larger motors that operate from AC supplies up to 6600 V, the rapid rate of change of the voltage applied to the winding may cause deterioration and failure in the insulation on the entry turns of standard motors.

On self-ventilated (fan-cooled) motors, reducing the motor shaft speed decreases the available cooling airflow. Operating a motor at full torque and reduced speed results in inadequate airflow. This consequently results in increased motor insulation temperature. This potentially can be damaging and can reduce the life of the motor's insulation or cause the motor to fail. One potential solution is to add a constant speed, separately driven cooling fan to the motor. This approach ensures adequate stator cooling over the whole speed range. However, the rotor will run hotter than designed as internal airflow remains a function of speed. As there are no windings in the rotor, insulation failure is not an issue, but bearings may run hotter and require more frequent lubrication.

Fan-cooled motors with centrifugal loads present less of a problem. Pumps and fans, for example, do not require full torque at reduced speeds. So, in these cases, there is less thermal stress on motors at reduced speeds. Centrifugal load does not cause the motor to exceed thermal limits defined by the insulation system.

29.1.4.3 Supply Harmonics

Current and voltage harmonics in the AC supply are created by VSD (as a nonlinear load) connected on the power distribution system. Such harmonics pollute the electric plant, which could cause problems if harmonic level increases beyond a certain level. The effect of harmonics can be overheating of transformers, cables, motors, generators, and capacitors connected to the same power supply with the devices generating the harmonics.

The IEEE 519 recommends practices and requirements for harmonic control in electric power systems. The philosophy of such regulations is to limit the harmonics injection from customers so that they will not cause unacceptable voltage distortion levels for normal system characteristics and to limit the overall total harmonic distortion of the system voltage supplied by the utility.

In order to reduce supply harmonics that are generated by VSDs equipped with a 6-pulse diode bridge rectifier, VSD equipment manufacturers adopt various techniques. Table 29.2 summarizes the most common methods and their advantages and disadvantages [2].

Ref. [2] quantifies the cost of these options as a percentage of the cost of a basic system with 6-pulse diode bridge. For low-power VSDs, the cost of a drive with a line reactor is estimated to be 120% of that without. A VSD with a 12-pulse diode bridge with a polygon transformer is 200% while for a double-wound transformer is 210%. The most expensive solution is that with active front end, estimated at 250%.

For 6-pulse converter, $n6p \pm 1$ (5, 7, 11, 13, 17, 19, etc) order harmonics are generated. To minimize the effects on the supply network, recommendations are laid down by IEEE 519 as to the acceptable harmonic limits. For higher drive powers, therefore, either harmonic filtering or use of a higher converter pulse number is necessary. It is generally true that the use of a higher pulse number is the cheaper alternative. Ref. [2] also quantifies the harmonic levels generated by each of the above method; refer to Table 29.3 for a direct comparison.

29.2 Drives Requirements and Specifications

29.2.1 General Market Requirements

Some of the most common requirements of VSDs are high reliability, low initial and running costs, high efficiency across speed range, compactness, satisfactory steady-state and dynamic performance, compliance with applicable national and international standards (e.g., EMC, shock, and vibration), durability, high availability, ease of maintenance, and repairs.

The order and priority of such requirements may vary from one application to another and from one industry to another.

TABLE 29.2 Techniques used to reduce supply harmonics

Topology	Advantage	Disadvantage
6-Pulse bridge with a choke	• Least expensive—low cost • Known technology • Simple to apply	• Bulky • Too large a value can reduce available torque • Only applies to the drive • Least effective method of filtering
12-Pulse bridge	• Eliminates the 5, 7, 17, and 19 harmonics • Known technology • Simple to apply	• Bulky and expensive • Only applies to the drive • A lot of 12-pulse drives on one site will shift the problem to the eleventh and thirteenth harmonics
6-Pulse, fully controlled active front end	• Comprehensive filtering for the drive • Cancels all low-order harmonics	• Very expensive • Not widely available • New technology
Harmonic filters	• Filters the installation • Reduces the harmonics at the point of common coupling • Least expensive filter to install	• Needs a site survey • Only sized to the existing load
Active filter	• Intelligent filter • Extremely efficient • Can be used globally or locally • More than one device can be installed on the same supply	• Very expensive

TABLE 29.3 Supply harmonics for different supply bridge configurations

Harmonic order number	Fifth (%)	Seventh (%)	Eleventh (%)	Thirteenth (%)	Seventeenth (%)	Nineteenth (%)
6-Pulse	54	36	10	6.7	7	5
6-Pulse with inductor	30	12	9	6	4	4
12-Pulse with polygon transformer	11	6	6	5	2	1
12-Pulse with double-wound transformer	4	3	8	5	1	1
24-Pulse 250% cost	4	3	1	1	1	1
Active front end	3	3	3	0	2	2

For example, for low-performance drives such as fans and pumps, the initial cost and efficiencies are paramount, as the main reason for employing VSDs is energy saving. However, in other industries such as marine, the compactness of the equipment (high volumetric power densities) is a priority requirement due to shortage in space. In such environments, direct raw water cooling is the preferred choice as water is plentiful, and forced water cooling results in a more compact drive solution.

In critical VSD applications, such as military marine propulsion, reliability, availability, and physical size are very critical requirements. Cost is relatively less critical. However, achieving these requirements adds to the cost of the basic drive unit. Series and parallel redundancy of components enable the VSD equipment to continue operation even with failed components. These are usually repaired during regular maintenance. In other critical applications (such as hot mill strips or subsea drives), the cost of drive failures could be many times more expensive than the drive itself. For example, accessing a drive down on the seabed, many kilometers below the seawater level, could be very difficult.

This section identifies the VSD requirements in various drive applications in different industries.

29.2.1.1 The Mining Industry

The majority of early-generation large mine winders are DC drives. Modern plants and retrofits generally employ cycloconverters with AC motors. However, small mine winders (below 1 MW) tend to remain DC.

The main requirements are the following:

- High reliability and availability
- Fully regenerative
- Small number requiring single-quadrant operation
- High range of speeds
- High starting torque required
- High torque required continuously during slow-speed running
- Low-torque ripple required
- Low supply harmonics
- Low audible noise emissions
- Flameproof packaging

29.2.1.2 The Marine Industry

The requirements of this industry are the following:

- Initial purchase price
- Reliability
- Ease of maintenance, that is, minimum component count and simple design
- Size and weight of equipment
- Transformerless, water-cooled VSD equipment is always preferred

Other desirable features include the following:

- A requirement for the integration of power management functions
- High volumetric power density (the smallest possible)
- Remote diagnostics, to allow faultfinding by experts onshore in critical situations

Drive powers are commonly in the range of 0.75–5.8 MW for thrusters and 6–24 MW for propulsion. The evolution in the commercial market is toward powers from 1 to 10 MW for propulsion. Higher powers are required for naval applications. The package drive efficiency must be equal to or better than 96%. Noise and harmonics problems are to be considered when using PWM inverters. The supply side harmonics produced must be capable of being filtered. Above 1 MW, power converters are usually equipped with a 12-pulse supply bridge, given today's technology.

Two-quadrant operation is required in general; hence, a diode supply bridge is adequate. Occasional requirement for crash stops forces the use of dynamic brake chopper. DC bus can be advantageous for supply to wharf loading equipment, but the drive power ranges are such that commercially available products already adequately serve this application.

The use of standard AC machines is desirable; however, if motors matched to the inverter prove to be cheaper, their use could be preferred. Low-noise emission (acoustic and electromagnetic) is very important. There is no requirement for high torque at low speed. Programming and expanded input and output capabilities are required to avoid the need for additional programmable logic control (PLC).

29.2.1.3 The Process Industries

The main requirements of this market are the following:

- Initial purchase price (long-term cost of ownership does not generally influence purchasing decision)
- Efficiency in continuous processes
- Reliability
- Ease of maintenance
- Bypass facility

The industry preference is for air-cooled drives. It is perceived that air-cooled drives are less costly than their water-cooled equivalents. Customers often have the belief that water and electricity does not mix well and are wary of problems with leaks. The exception is the offshore industry where equipment size is paramount, and therefore, water cooling is standard. In general, there is no perceived requirement for space saving in majority of process plants. The desirable features often requested by customers are ease of maintenance and good diagnostic facilities.

The market requirement is for cost-effective, stand-alone drives at various power levels from a fraction of a kW up to 30 MW. The use of standard AC machines is desirable. However, if nonstandard but simpler and cheaper machines can be offered, an advantage could be gained:

- Two-quadrant operation for fans, pumps, and compressors.
- Four-quadrant operation for some test benches.
- Control must allow additional functions such as temperature protection, motor bearing temperature, and flow and pressure control.
- There is no requirement, in general, for field weakening.
- The harmonics produced by the drive, imposed on the power system, should not require a harmonic filter. Harmonics must be minimized.

In the low-voltage (LV) arena, the PWM-VSI is dominating the market. In the medium-voltage (MV) arena, there are a number of viable drive solutions—load-commutated inverters (LCIs) and cycloconverters. However, there is a developing market for MV PWM-VSI drives.

29.2.1.4 The Metal Industries

The requirements of this industry are the following:

- Reliability—high availability.
- Efficiency of the equipment—long-term costs of ownership.
- Low maintenance costs—this has been a key factor in the move from DC to AC.
- Power supply system distortion—more onerous regulations from the supply authorities.
- Initial purchase cost—very competitive market and large drive costs have a big impact on total project costs.
- Confidence in the supplier and their solution.

The following is a list of desirable features:

- Programmable system drives with powerful programming tools.
- Preference for air-cooled stacks but water-cooled is acceptable if a water-to-air heat exchanger is used.
- Powerful maintenance and diagnostic tools.
- Low EMC noise signature.
- Ability to interface to existing automation system via network, fieldbus, or serial link.
- Physical size of equipment is often not an important consideration.
- Fire protection systems integral to drive equipment.

The main market concerns are (a) EMC regulations, (b) effects on motor insulation of higher voltage levels, and (c) cooling with "dirty" mill water is not acceptable. The maintenance of deionized water circuits is a big issue.

29.2.2 Drive Specifications

Failure to properly specify an electric VSD can result in a conflict between the equipment's supplier and the end user. Often, the cost can be delayed project completion and/or the loss of revenue.

In order to avoid such a problem, requirement specifications should reflect the operating and environmental conditions (Table 29.4). The equipment supplier and the customer need to work as partners and cooperate from the beginning of the project until successful commissioning and hand over. It is advisable that the end user procures the complete drive system, including system engineering, commissioning, and engineering support, from one competent supplier.

It is one of the first priorities to identify applicable national and international standards on issues related to EMC, harmonics, safety, noise, and smoke emissions during faults, dust, and vibration. Overspecifying the requirements could often result in a more expensive solution than necessary. Underspecifying the requirements result in poor performance and disappointment.

As far as the end user is concerned, they need to specify the drive interfaces—the AC input voltage, shaft mechanical power, and shaft speed. The torque and current are calculated from these. Frequency and power factor depend on the choice of motor.

For a high-power drive, it is always recommended to carry out a "harmonic survey." Such a survey will reveal the existing level of harmonics and quantify the impact of the new drive on the harmonic levels.

TABLE 29.4 Typical example of VSD specifications

Variable	Specification
Application	Dynamometer application for a test bench
Motor type	Induction motor
Duty cycle	Continuous at full rating. 150% overload for 1 min every 60 min
Power rating	100 kW
Supply voltage	690 V ± 5%
Supply frequency	50 ± 0.05 Hz
Speed range	1000:1
Accuracy	0.1%
Min/max speed	0/1500 rpm
Torque dynamic response	<10 ms from 100% positive torque to 100% negative torque
Power factor	>96% lagging at all speeds
Efficiency	>98% at full load
Performance	Fully regenerative Full torque at zero speed
Ambient temperature	0–40°C
Supply harmonics	G5/3, IEEE519
Life expectancy	>5 years
MTBF	>50,000 h
MTTR	<2 h
IP rating	IP45
IEEE 519	IEEE recommended practices and requirements for harmonic control in electric power systems
IEC 60146	Semiconductor converters. Specifications of basic requirements
IEC 61800	Adjustable speed electric power drives systems

29.3 Drive Classifications and Characteristics

Table 29.5 illustrates the most commonly used classifications of electric VSDs. In this section, particular emphases will be given to classification by applications and by converter types.

Other classifications, not listed in Table 29.5, include the following:

- Working voltage: low voltage <690 V or medium voltage (MV) 2.4–11 kV
- Current type: unipolar or bipolar drive
- Mechanical coupling: direct (via a gearbox) or indirect mechanical coupling
- Packaging: integral motors as opposed to separate motor inverter
- Movement: rotary movement, vertical, or linear
- Drive configuration: stand-alone system and DC link bus
- Speed: high speed and low speed
- Regeneration mode: regenerative or nonregenerative
- Cooling method: direct and indirect air and direct water (raw water and deionized water)

Section 29.2 deals with the subject of drives requirement and specification from applications point of view, while Section 29.5 deals with drive topologies from the point of view of motor classifications.

29.3.1 Classification by Applications

Under this classification, there are four main groups:

- Appliances (white goods)
- General purpose drives
- System drives
- Servo drives

Table 29.6 describes the main features of these groups and lists typical applications.

TABLE 29.5 Classifications of electric VSD

By application	By devices	By converter	By motors	By industry	By rating
• Appliances	• Thyristor	• AC/DC (chopper)	• DC	• Power generation	• Fraction kW power <1 kW
• Low performance (2Q) ($1 < P < 5$ kW)	• Transistor	• AC/AC direct (cyclo- and matrix converter)	• Induction motor (squirrel cage and wound rotor)	• Metal	• Low power
• High performance (4Q)	• Gate turn-off thyristor (GTO)				
• Integrated gate-commutated thyristor (IGCT) power < 500 kW	• AC/AC via a DC link voltage source	• Synchronous motor	• Petrochemical	• Medium	
• Servo	• Insulated-gate bipolar transistor (IGBT)	• AC/AC via a DC link current source	• *Special motors*: SRM, BDCM, stepper, actuators, linear motor	• Process industry	• High power 1–50 MW
• MOSFET				• Mining • Marine	

TABLE 29.6 Classification of electric VSD by application

Type of drive	Appliances	General purpose	System	Servo
Performance	Low	Low	High	Very high
Power rating	Very low	Whole range	Whole range	Low
Motor	Universal and induction motor. Recently, PM and SRM are being used	DC motor, induction motor, and synchronous motor	DC motors, induction motors, and synchronous motors	DC motors, brushless DC motors, induction motor, stepper motors, and actuators
Converter	Simple, low cost	AC and DC drives with open-loop controller	PWM drives with DC bus, cycloconverter, good quality control with closed-loop control, and needs encoder or an observer	DC drive, AC drive, and special motor drives. Tendency toward brushless DC motors
Typical industry	Home	Process	Metal	Automation
Feature	Mass production, low cost, price-sensitive, and very low power	Nonregenerative, cost-sensitive, low or no overload, low start-up, low performance, and stand-alone	Accuracy with encoders $\lll 0.1\%$ in steady state and dynamic, good precision and linearity of I/O and control, flexible with operation capability, and setup and configuration communication and feedback	Closed loop, PM motor, >1000 Hz torque response, precise and rapid response, and frequent full speed reversal high precision and linearity of I/Os
Applications	Home appliances, for example, washing machines, dishwasher, temple dryers, and freezers	Fans, pumps, compressors, mixers, and simple elevator	Test benches, winders, sectional process line, elevator, cranes, and hoists	Positioning, pick and place, robotics, coordinate control, and machine tools

29.3.2 Classification by Type of Power Device

The silicon-controlled rectifier (SCR), also known as the thyristor, is the oldest controllable solid-state power device and still the most widely used power device for MV—AC voltages between 2.4 and 11 kV—high-power drive applications. Such devices are available at high voltages and currents, but the maximum switching frequency is limited and requires a complex commutation circuit for VSI drive. The SCRs are therefore most popular in applications where natural commutation is possible (e.g., cycloconverters and LCI current source converters).

The gate turn-off thyristor (GTO) has made PWM-VSI drives viable in LV drive applications. The traction industry was one of the first to benefit from such a device on a large scale.

Complex gate drive and limited switching performance, combined with the need for a snubber circuit, limited this device to high-performance applications where the SCR-based drives could not give the required performance.

The main power devices available in the market can be divided into two groups as shown in Table 29.7.

Bipolar-/MOSFET-type transistors have witnessed significant popularity in the late 1980s; however, they have been replaced by the IGBT that combines the characteristics of both devices—the current handling capability of the bipolar transistor and the ease of drive of the MOSFET.

Traction inverters are designed for DC link voltages between 650 V DC and 3 kV DC with ratings up to 3 MW. The first generation of widely used traction inverter equipment was GTO-based, while the latest generation is almost exclusively IGBT-based. Conversion to IGBT has enabled a 30%–50% reduction in cost, weight, and volume of the equipment.

Early attempts to use GTOs in MV applications failed because of their high cost, snubber requirements, and associated snubber energy loss, which is proportional to the square of the supply voltage. Energy-recovery circuitry enables recovery of most of the snubber energy but adds to the cost and complexity of the converter. With high-voltage IGBT and IGCT, MV PWM-VSI has become commercially available with supply voltage up to 6.6 kV and power rating in excess of 19 MW.

29.3.3 Classification by the Type of Converter

The power converter is capable of changing both its output voltage magnitude and frequency. However, in many applications, these two functions are combined into a single converter by the use of the appropriate switching function, for example, PWM. By appropriate control of the stator frequency of AC machines, the speed of rotation of the magnetic field in the machine's air gap and thus output speed of the mechanical drive shaft can be adjusted. As the magnetic flux density in the machine must be kept constant under normal operation, the ratio of motor voltage over stator frequency must be kept constant.

The input power of the majority of VSD systems is obtained from sources with constant frequency (e.g., AC supply grid or AC generator). In order to achieve a variable-frequency output energy, an AC/AC converter is needed. Some converters achieve direct power conversion from AC/AC without an intermediate step (e.g., cycloconverters and matrix converters). Other converters require DC link (as current source or voltage source).

In all AC VSDs, the direction of shaft rotation is reversed by simply changing the phase rotation of the inverter through the sequence of driving the switches.

29.3.3.1 DC Static Converter

This drive employs the simplest static converter. It is easily configured to be a regenerative drive with a wide speed range. Table 29.8 summarizes its key features.

High torque is available throughout the speed range with excellent dynamic performance. Unfortunately, the motor requires regular maintenance, and the top speed often is a limiting factor. Commutator voltage is limited to around 1000 V, and this limits the maximum power available. The continuous stall torque rating is very limited due to the motor's commutator.

29.3.3.2 Direct AC/AC Converters

Cyclo-converter

A typical cycloconverter comprises the equivalent of three anti-parallel 6-pulse bridges (for regenerative converter) whose output may be operated in all four quadrants with natural commutation. The main features of cycloconverters are listed in Table 29.8. This type of drive is best suited for high-performance high-power >2 MW drives where the maximum motor frequency is <33% of the mains frequency.

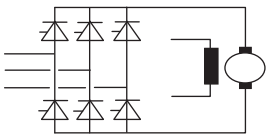
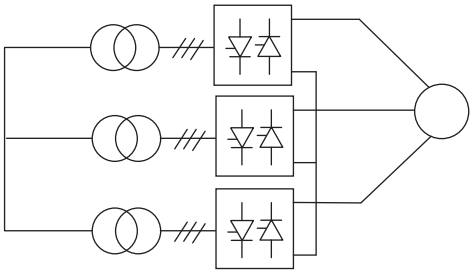
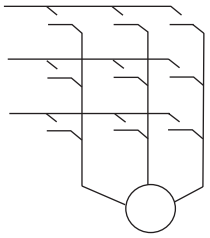
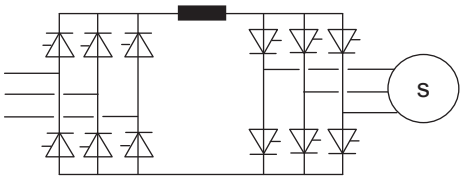
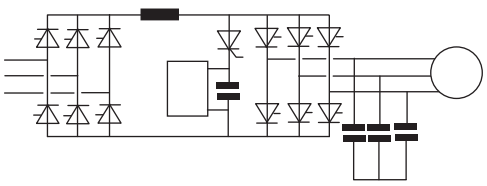
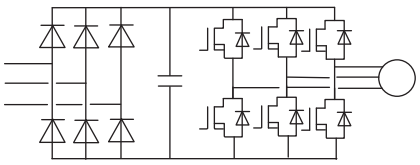
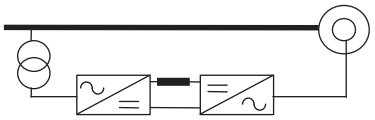
Matrix-converter

The force-commutated cycloconverter (better known as a matrix converter) represents possibly the most advanced state of the art at present, enabling a good input and output current waveform and eliminating the DC link components with very

TABLE 29.7 Power devices used in the VSD converters

Group 1: thyristors	Group 2: transistors
This group covers devices having a four-layer, three-junction monolithic structure. They are characterized by low conduction losses and high surge and current-carrying capabilities. They operate as an on/off switch. The most popular types of devices listed under this group	Switches listed under this group are basically three-layer two-junction structure devices, which operate in switching and linear modes. They are best recognized for ruggedness of their turn-off capabilities
• Silicon-controlled rectifier (SCR) • Gate turn-off thyristor (GTO) • MOSFET-controlled thyristor (MCT) • Field-controlled thyristor (FCT) • Emitter-switched thyristor (EST) • MOS turn-Off thyristor (MTO) • Integrated gate-commutated thyristor (IGCT)	• Bipolar junction transistor (BJT) • Darlington transistor • MOSFET • Injection-enhanced gate transistor (IEGT) • Carrier stored trench-gate bipolar transistor (CSTBT) • Insulated-gate bipolar transistor (IGBT)

TABLE 29.8 Converter topologies

Converter	Schematic	Features
(a) Controlled rectifier		• DC motor • Fully controlled SCR converter • Controlled DC voltage • Simple converter topology • Power factor is a function of speed
(b) Cyclo		• Induction motor and synchronous motor • Direct AC/AC power conversion • 3 × 6-pulse SCR-based fully controlled converters—APT for fully regenerative • Natural commutation • Low supply harmonics, 18-pulse • Power factor is a function of speed
(c) Matrix		• Squirrel-cage induction motor • Synchronous motor • Direct AC/AC power conversion • Forced commutated, reverse conducting switches • Four-quadrant operation inherent PWM in/PWM out • Controlled power factor
(d) LCI		• Synchronous motor • Simple converter arrangement • Power factor is a function of speed • Load-commutated SCRs • Synchronous motor requires excitation • Suffer from torque pulsation at low speeds
(e) FCI		• Squirrel-cage induction motor • Similar to LCI • Requires output capacitors for commutation • Requires a diverter commutation circuit for commutation at low speeds • Torque pulsation and resonance
(f) VSI		• Synchronous and squirrel-cage induction motors • 6-pulse diode front end • Good power factor across speed range • DC link voltage source • PWM output voltage
(g) Kramer		• Wound-rotor induction motor with slip rings • Small energy recovery converter • Any type of converter may be used between slip ring and AC input

little limitation in input-to-output frequency ratio. This type of converter is still at its early stages of development. The main advantage of this drive is the ability to convert AC fixed-frequency supply input to AC output without DC bus. It is ideal for integrated motor drives with relatively low power ratings. Major drawbacks include (a) the increased level of silicon employed (bidirectional switches), (b) its output voltage is always less than its input voltage, and (c) complexity of commutation and protection.

Matrix converters provide direct AC/AC power conversion without an intermediate DC link and the associated reactive components. They have substantial benefits for integrated drives as outlined below:

- Reduced volume due to the absence of DC link components.
- Ability to operate at the higher thermal limit imposed by the power devices.
- Reduced harmonic input current compared with diode bridge.
- Ability to regenerate into the supply without dumping heat in dynamic braking resistors.
- Matrix converters have not been commercially exploited because of voltage ratio limitation, device count, and difficulties with current commutation control and circuit protection.

29.3.3.3 Current Source Inverter

The output of this inverter is rectangular blocks of current from the motor bridge supplied from a supply converter whose output is kept at constant current by a DC link reactor and current servo. This type of inverter is typically based on fast thyristors.

Load commutated inverter

Natural commutations of thyristors are usually achieved with synchronous machines at speeds >10%. Natural commutation is induced as a result of the presence of the motor's electromotive force (EMF); this is called load commutation hence the drives' other name of LCI. At low speeds, the motor voltage is too low to give motor bridge commutations. This is achieved by using the supply converter. Induction-motor LCI drives can be supplied by adding a large capacitor on the motor terminals.

The LCI drive covers a wider speed range (up to 10,000 rpm) with power rating up to 100 MW. It gives full load torque throughout the speed range with moderate dynamic performance. Its simple converter design combined with a maintenance-free motor design (both induction and synchronous) has increased the popularity of these drives. It is still a popular solution for high-power drives (e.g., conveyors, pumps, fans, compressors, and marine propulsion).

The LCI drive has limited performance at low speeds. It also suffers from torque pulsation at 6 and 12 times the motor's frequency and beat frequencies. Critical speeds can excite mechanical resonance. Its AC power factor varies with speed. Torque pulsations can be reduced in 12-pulse systems if required.

Forced commutated inverter

Externally commutated current source converters with an induction motor are also a viable solution. To compensate for the inductive component in the motor current, a bank of capacitors are usually used at the motor terminals. The capacitor current is proportional to the motor voltage and frequency. Load commutation at high speed where the compensation current is high enough. Forced commutation at lower speed where the capacitive current is too low for compensation. Forced commutation is achieved using various techniques. The one shown above is based on DC link diverter that consists of a GTO, loading equipment in parallel with the diverting/compensating capacitor. Modern drives employ forced commutated devices, such as reverse-blocking GTOs and IGCTs.

29.3.3.4 Slip Power Recovery (Kramer)

In this type of converter, which is described in Table 29.8, the rotor current of a slip-ring wound-rotor induction motor is rectified and the power then reconverted to AC at fixed frequency and fed back into the supply network. For traditional designs, the low-frequency slip-ring currents are rectified with a diode bridge, and the DC power is then inverted into AC power at mains frequency.

The traditional designs had poor AC mains dip immunity, high torque pulsation, and high levels of low-frequency AC supply harmonics. The latest generation of this type of drive is called the rotor drive and uses PWM-VSI inverters for the rotor and AC supply bridges.

This keeps sine-wave currents in the AC rotor circuits, and the drive has many advantages over traditional circuits including the following:

- No torque pulsation
- Low AC harmonics
- Very high immunity to AC supply dips
- Very cost-effective if a limited speed range is required but still requires a separate starter
- Inherent ability to run at rated speed without electronic circuits
- Converter cost reduced by 2:1 if it uses the ± speed ability to give a speed range

29.3.3.5 PWM-VSI Converter

The availability of power electronic switches with turn-off capability; for example, FETs, BJTs, IGBTs, and GTOs have currently favored drives with voltage-fed PWM converters on induction.

The PWM-VSI drives offer the highest possible performance of all VSDs; refer to Table 29.9. Recent improvements

TABLE 29.9 Drive features

	DC drive			AC drive		
Type	DC	Cyclo	CSI (FCI)	CSI (LCI)	Kramer	PWM-VSI
Motor type	• DC motor	• Induction and synchronous motors	• Induction motor	• Synchronous motor	• Slip-ring wound-rotor induction motor	• Induction or synchronous
Power • Speed range • Accuracy • Maximum speed	• Up to 10 MW • 1000:1 • 0.01% • Limited by motor capability	• 2–30 MW • 1000:1 • ±0.01% • 1000 rpm	• 1–10 MW • 10:1 • ±1% • 6000 rpm	• 1–100 MW • 10:1 • ±0.01% • 10,000 rpm	• 0.5–50 MW • 0.8:1.2 • 0.1% • <1200 rpm	• 0.5–2 MW • 1000:1 • 0.01% • 10,000 rpm
Performance	• High torque over speed range • High dynamic performance	• High torque over speed range • High dynamic performance	• Poor dynamic response • Low starting torque	• High torque over speed range • Reasonable dynamic performance	• High torque over speed range • High dynamic performance	• High torque over speed range • High dynamic performance
Advantages	• Simple regenerative	• High stall torque (induction) • Inherently regenerative • Robust motors • Low maintenance motor • High overload capacity	• Standard robust maintenance-free motor • Minimal derating	• Simple • Inherently regenerative • Maintenance-free motor	• Regenerative (new) • Robust • Slip ring wound rotor • High overload capacity	• Good power factor • Tolerant to supply dips • Standard robust maintenance-free motor • Minimal derating
Disadvantages	• Stall torque rating • Motor maintenance • Custom motor design	• Motor custom design • Low AC supply power factor	• Complex • Poor dynamic performance • Torque pulsation and resonance	• Motor custom design • Torque pulsation	• Complex • Motor custom design	• Complex • Expensive • Regeneration at extra cost
Applications	• Mill drives (ball and sag) • Marine propulsion • Mine winders • Process lines • Conveyors	• Mill drives (ball and sag) • Marine propulsion • Mine winders • Conveyors	• Pumps, fans, and compressors • Soft starter	• Pumps, fans, and compressors • Soft starter • Marine propulsion • Conveyors • Mill drives	• Pumps, fans, and compressors • Power generation • Mills (ball and sag)	• Process lines • Paper machines • Traction

in switching technology and the use of microcontrollers have greatly advanced this type of drive. The inverters are now able to operate with an infinite speed range. The supply power factor is always near unity. Additional hardware is easily added if there is a requirement to regenerate power back into the mains supply. Motor ripple current is related to the switching frequency, and in large drives, the motor may be derated by <3%.

29.3.3.6 Comparison

Table 29.9 summarizes the main features of all types of converter drives discussed above and assesses their merits and drawbacks. It also illustrates typical applications.

29.4 Load Profiles and Characteristics

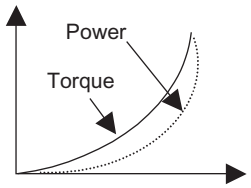
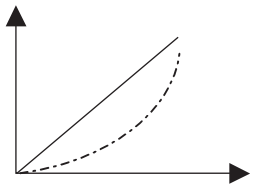
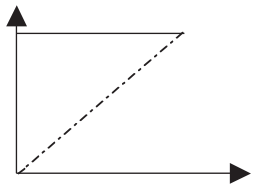
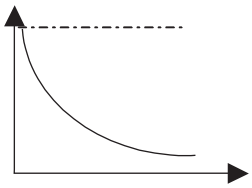
The way the drive performs is very much dependent on the load characteristics. Here are four load characteristics described.

29.4.1 Load Profile Types

In the literature, four different load profiles have been described, for example, Ref. [3] (Table 29.10). These are the following:

1. Torque proportional to the square of the shaft speed (variable torque)
2. Torque linearly proportional to speed (linear torque)

TABLE 29.10 Load characteristics

Type I	Type II	Type III	Type IV
• $T=f(n^2)$ • $P=f(n^3)$ • Low start-up torque • Best suited for energy saving • Torque-speed curve is required when specifying a drive • Axial and centrifugal pumps • Axial and centrifugal ventilators • Screw and centrifugal compressors • Centrifugal mixers • Agitators	• $T=f(n)$ • $P=f(n^2)$ • Information about process is needed (e.g., density, consistency, viscosity, and temperature) • Mixers • Stirrers	• $T=$ constant • $P=f(n)$ • At start-up, the torque may be higher than nominal. Examples are static friction with conveyor belts. Vertical and horizontal forces need to be taken into consideration for inclined conveyors • Extrusions, draw benches • Paper and printing continuous machines • Volumetric gear pumps/pistons pumps, etc. • Piston compressors • Conveyor machines • Lift machines	• $T=f(1/n)$ • $P=$ constant • Mostly dominated by DC drives but modern PWM-VSI is taking over. Certain loads such as winding and reeling machinery require closed-loop controls • Lift machine • Reciprocating rolling mill • Winding machines • Lathes • Winders • Reelers • Wire drawers • Web-feed printing machines
			

3. Torque independent of speed (constant torque)
4. Torque inversely proportional to speed (inverse torque)

29.4.2 Motor Drive Duty

29.4.2.1 Duty Cycle

The size of the driven motors is generally chosen for continuous operation at rated output, yet a considerable proportion of motor drives is used for duties other than continuous. As the output attainable under such deviating conditions may differ from the continuous rating, fairly accurate specification of the duty is an important prerequisite for proper planning. There is hardly a limit to the number of possible duty types.

In high-performance applications, such as traction and robotics, the load and speed demands vary with time. During acceleration of traction equipment, a higher start-up torque (typically twice the nominal torque) is required; this is usually followed by cruising and deceleration intervals. As the torque varies with time so does the motor current (and motor flux linkage level). The electric, magnetic, and thermal loading of the motor and the electric and thermal loading of the power electronics converter are definite constraints in a drive specification.

Table Table 29.11 categorizes operating duties into eight major types (Ref. [4]).

29.4.2.2 Mean Output

Variation of the required motor output during the periods of loaded operation is among the most frequent deviations from the duty types defined in Table Table 29.11. In such cases, the load (defined as current or torque) is represented by the mean load. This represents the root-mean-square (RMS) value, calculated from the load versus time characteristics. The maximum torque must not exceed 80% of the breakdown torque of an induction motor.

If the ratio of the peak torque to the minimum power requirements is greater than 2:1, the error associated with using the RMS output becomes excessive, and the mean current has to be used instead. No such mean value approximation is possible with duty type S2, which therefore necessitates special inquiry.

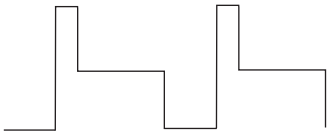
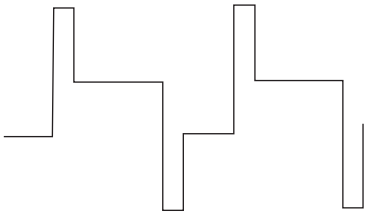
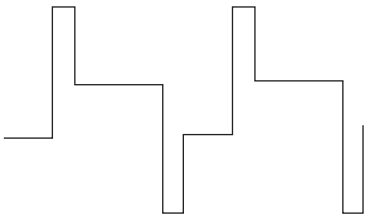
Careful assessment of duty types S2–S8 reveals that there exist two distinct groups:

1. Duties S2, S3, and S6 permit uprating of motors relative to the output permissible in continuous running duty (S1).
2. Duties S4, S5, S7, and S8 requiring derating relative to the output permissible in continuous running duty (S1).

29.4.2.3 Thermal Cycling

The drive duty cycle also affects the reliability and the life expectancy of power devices. Repetitive load cyclic duty results in additional thermal stresses on power devices. Frequent acceleration and deceleration of drives results in repetitive junction temperature rise and falls at the cyclic duty. The life expectancy of devices is often determined by the maximum allowed number of cycles for a given power device junction temperature rise.

TABLE 29.11 Definition of load cyclic duties—VDE0530, in accordance with IEC 34-1

Duty type	Representation	Description
S1: Continuous running duty		Operation at constant load of sufficient duration for the thermal equilibrium to be reached. Specify by indicating "S1" and required output
S2: Short-time duty		Operation at constant load during a given time, less than required to reach thermal equilibrium, followed by a rest and deenergized period of sufficient duration to reestablish machine temperatures within 2°C of the coolant
S3: Intermittent periodic duty with a high start-up torque		A sequence of identical duty cycles, each including a period of operation at constant load and a rest and deenergized period. In this duty type, the cycle is such that the starting current does not significantly affect the temperature rise
S4: Intermittent periodic with a high start-up torque		A sequence of identical duty cycles, each cycle including a significant period of starting, a period of operation at constant load, and a rest and deenergized period
S5: Intermittent periodic duty with high start-up torque and electric braking		A sequence of identical cycles, each cycle consisting of a period of starting, a period of operation at constant load, a period of rapid electric braking, and a rest and deenergized period
S6: Continuous-operation periodic duty		A sequence of identical duty cycles, each cycle consisting of a period of operation at constant load and a period of operation at no load. There is no rest and deenergized period
S7: Continuous-operation periodic duty with high start-up torque and electric braking		A sequence of identical duty cycles, each cycle consisting of a period of starting, a period of operation at constant load, and a period of electric braking. There is no rest and deenergized period
S8: Continuous-operation periodic duty with related load/speed changes		A sequence of identical duty cycles, each cycle consisting of a period of operation at constant load corresponding to a predetermined speed of rotation, followed by one or more periods of operation at other constant loads corresponding to different speeds of rotation. There is no rest and deenergized period

Although this is true for all types of power devices, it is more critical for IGBTs where wire bonds and solder layers are used.

In modern IGBT-based converter design, the maximum junction temperature rise of the IGBTs is limited to a level, which ensures a conservative number of thermal cycles over the lifetime of the drive. Typical junction temperature rise is 30°C for a repetitive cyclic duty (e.g., steel mill) and 40°C for nonrepetitive cyclic duty (e.g., fan pumps).

29.4.2.4 Multiquadrant Operation

Fully regenerative electric VSDs offer a rapid regenerative dynamic braking in both forward and reverse directions. Operation in motoring implies that torque and speed are in the same direction (QI, III). In regenerative braking, the torque is opposite to the speed direction (QII and IV), and the electric power flow in the motor is reversed. (See Fig. 29.2.)

Positive power flow of electric energy means that electric power is drawn from the power supply via the power

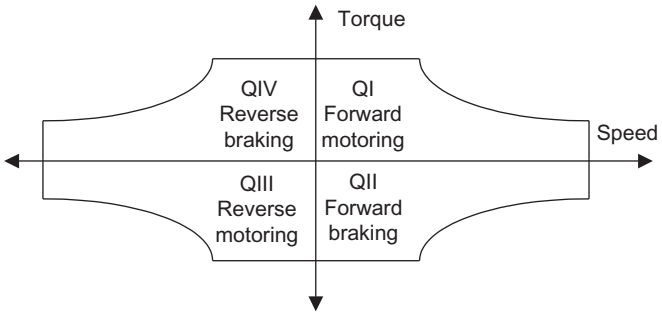


FIGURE 29.2 Operating regions of electric VSD.

electronics converter by the motor, while negative power flow refers to electric power delivered by the motor in the generator mode to the power electronics converter. This could be regenerated back to the supply or dissipated as a heat in the dynamic brake dissipative mechanism.

For regenerative drive, the power electronics converter has to be designed to be able to handle bidirectional power flow. In low and medium power converter (say <500 kW) with slow dynamic braking demands, the generated power during the braking period is interchanged with the strong filter capacitor of power electronics converter, or DC (dynamic) braking is used.

29.4.2.5 Dynamic Braking Energy

There exist two types of energy stored in VSD, which need to be dealt with during dynamic braking:

- *Inertia or kinetic energy loads*: Typically moving (rotating or linear) machines. These would decelerate naturally to rest. Braking can speed up the process cycle for the sake of productivity.
- *Mass or potential energy loads*: Typically hoists or lifts—which would run on or even accelerate. Braking must apply full power to maintain constant speed while the load is lowered.

The drive losses, mechanical resistance, and the transmission efficiency, work in favor of deceleration, reducing the braking power demand. The energy regenerated by potential energy loads depends on maximum power and both the overrun time and the decelerating time.

The braking time and the duty cycle time are decided by the requirements of the process system, but note particularly the effect of varying the braking duty cycle time and the deceleration time.

For DC injection braking, the kinetic energy of the motor-load system is converted to heat in the motor rotor. For fast and frequent generator braking, the power electronics converter has to handle the generated power either by a controlled dynamic brake chopper (with braking resistor) or through bidirectional power flow. The power losses in the converter can assist in dynamic braking.

For a fast speed response, modern VSDs may develop a maximum transient torque up to the base speed and maximum transient power up to a maximum speed, provided that both the motor and the power electronics converter can handle these powers. For a 200 kW dynamometer drive application, a rapid change of torque from full positive torque to full negative torque is required in <10 ms.

29.5 VSD Topologies

In this section, drive topologies are classified according to the motor they employ. Various publications dealt with this subject, for example, Refs. [3,5]. The most common motors are illustrated in Fig. 29.3.

29.5.1 DC Motor Drives

Until recently, the DC motor drive was the most commonly used type of electric VSD, with only very few exceptions, and is the least expensive. The mechanical commutator is an electromechanical DC-to-AC bidirectional power flow power converter, as the currents in the rotor armature coils are AC while the brush current is DC. The DC drive is well-known, well proved, and widely applied; yet, its popularity is in relative decline due to the emergence of the more robust, lower cost squirrel-cage induction motor drive.

Unfortunately, the mechanical commutator though not bad in terms of losses and power density has serious commutation current and speed limits and thus limits the power per unit to 1–2 MW at 1000 rpm and may not be accepted at all in chemically aggressive or explosion-prone environments. The application of the DC drive has been restricted to hazardous areas due to the very limited availability of flameproof DC machines. Commutator and brush maintenance is difficult in such

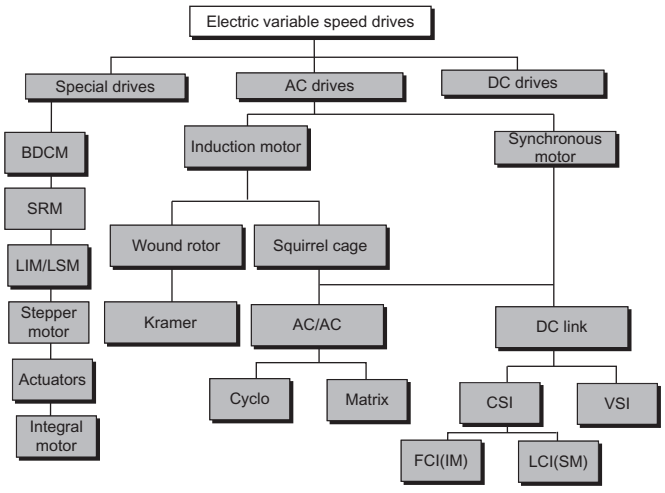


FIGURE 29.3 Classification of electric VSD.

environments. Furthermore, continuous sparking at the brushes is virtually inevitable at full load output.

Due to the inherent ease of speed control of the separately excited DC machine, DC drives found popularity in early electric drive applications, by varying the applied armature voltage. This variable armature voltage is simply generated by phase-controlled rectification, and this technique has now almost entirely replaced the Ward-Leonard systems previously used.

The AC/DC converter offers a variable DC voltage, which is capable of four-quadrant operation (positive and negative DC voltage and DC current output). Permanent magnet-excited brushed motors have been used in numerous applications for some time, particularly in nonregenerative drive applications.

Motor output torque is approximately proportional to armature current, and motor speed is approximately proportional to converter output voltage. Speed control by sensing armature voltage is therefore feasible giving an accuracy of around 5%.

Provided the motor excitation is kept constant, the DC drive power factor is proportional to motor speed. Since most pumps, compressors, and fans demand a torque proportional to the square of speed, constant excitation systems are used and so the above relationship applies.

A typical power factor, at maximum rated speed for a DC drive, is 0.85. This relationship applies to many other types of electric drives.

If a slow dynamic response is satisfactory, regeneration to the mains supply is achieved either by reversing the motor field or armature connection. Alternatively, regeneration with faster response is achieved by connecting another thyristor bridge in antiparallel with the main bridge. In this case, fast response is possible with changeover time of <15 ms between full torque motoring to full torque regenerating. The 6-pulse drive configuration is acceptable for powers up to 1 MW. This limitation arises not from any semiconductor device limitation but is due to AC line current harmonics the converter generates.

A force-commutated or "chopper" converter for DC motors uses the principle of variable mark-space control using a thyristor or transistor solid-state switch. With a diode front-end converter, a fixed, smoother DC supply is derived from the mains by uncontrolled rectification and rapidly applied, removed, and reapplied to the machine for adjustable intervals, thus applying a variable mean DC voltage to the DC motor; refer to Fig. 29.4B.

This type of DC drive has the advantage of high (near unity) power factor at all motor speeds and much reduced harmonic spectrum.

29.5.2 Induction Motor Drive

29.5.2.1 Squirrel Cage Induction Motor

Squirrel-cage induction motors are simpler in structure than DC motors and are most commonly used in the VSD industry. They are robust and reliable. They require little maintenance and are available at very competitive prices. They can be designed with totally enclosed motors to operate in dirty and explosive environments. Their initial cost is substantially less than that of commutator motors, and their efficiency is comparable. All these features make them attractive for use in industrial drives.

The three-stator windings develop a rotating magnetic flux rotating at synchronous speed. This speed depends on the motor pole number and supply frequency: the rotating flux intersects the rotor windings and induces an EMF in the rotor winding, which in turn results in circulating current. The rotor currents produce a second magnetic flux, which interacts with the stator flux to produce torque to accelerate the machine. As the rotor accelerates, the induced rotor voltage falls in magnitude and frequency until an equilibrium speed is reached. At this point, the induced rotor current is sufficient to produce the torque demanded by the load. The rotor speed is slightly lower than the synchronous speed by the slip frequency, typically 3%.

In order to ensure constant excitation of the machine, and to maximize torque production up to the base speed, the ratio of stator voltage to frequency needs to be kept approximately constant.

Induction motor drive has three distinct operating regions:

(a) *Constant torque*: The inverter voltage is controlled up to a maximum value limited by the supply voltage. As the motor speed and the voltage are increased in proportion, constant V/F, the rated flux linkage is maintained up to the base speed. Values of torque up to the maximum value can be produced at speeds up to about this base value. The maximum available torque is proportional to the square of the flux linkage. Typically, the induction

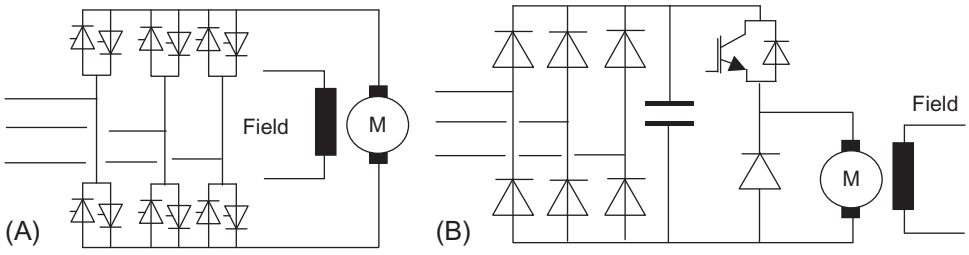


FIGURE 29.4 DC drive: (A) with fully controlled antiparallel supply bridge and (B) diode rectifier with DC chopper.

motor is designed to provide a continuous torque rating of about 40%–50% of its maximum torque.

(b) *Constant power*: For higher speed, the frequency of the inverter can be increased, but the supply voltage has to be kept constant at the maximum value available in the supply. This causes the stator flux linkage to decrease in inverse proportion to the frequency. Constant power can be achieved up to the speed at which the peak torque available from the motor is just sufficient to reach the constant power curve. A constant power speed range of 2–2.5 can usually be achieved. Within this range, the motor frequency is increased until at maximum speed.

(c) *Machine limit (pullout torque)*: Once the machine limit has been reached, the torque falls off in proportion to the square of motor frequency. Operation at the higher end of this speed range may not be feasible as the motor power factor worsens. This in turn results in a higher stator current than the rated value. The motor heating may be excessive unless the duty factor is low.

Induction motors are used in applications requiring fast and precise control of torque, speed, and shaft position.

The control method widely used in this type of application is known as vector control, a transient response at least equivalent to that of a commutator motor can be achieved.

The voltage, current, and flux linkage variables in this circuit are space vectors from which the instantaneous values of the phase quantities can be obtained by projecting the space vector on three radial axes displaced 120 degrees from each other. The real and imaginary components of the space vectors are separated, resulting in separate direct and quadrature axis equivalent circuits but with equal parameters in the two axes.

Changes in the rotor flux linkage can be made to occur only relatively slowly because of the large value of the magnetizing inductance of the induction motor. Vector control is based on keeping the magnitude of the instantaneous magnetizing current space vector constant so that the rotor flux linkage remains constant. The motor is supplied from an inverter that provides an instantaneously controlled set of phase currents that combine to form the space vector, which is controlled to have constant magnitude to maintain constant rotor flux linkage. The second component is a space vector, which is in space quadrature with the instantaneous magnetizing current space vector. This component is instantaneously controlled to be proportional to the demand torque.

To the extent that the inverter can supply instantaneous stator currents meeting these two requirements, the motor is capable of responding without time delay to a demand for torque. This feature, combined with the relatively low inertia of the induction motor rotor, makes this drive attractive for high-performance control systems.

Vector control requires a means of measuring or estimating the instantaneous magnitude and angle of the space vector of the rotor flux linkage. Direct measurement is generally not feasible. Rapid advances are being made in devising control configurations that use measured electric terminal values for estimation.

29.5.2.2 Slip-Ring (Wound-rotor) Induction Motor Drive

Wound-rotor induction motors with three rotor slip rings have been used in adjustable speed drives for many years. In an induction motor, torque is equal to the power crossing the air gap divided by the synchronous mechanical speed. In early slip-ring induction motor drives, power was transferred through the motor to be dissipated in external resistances, connected to the slip-ring terminals of the rotor. This resulted in an inefficient drive over most of the speed ranges. More modern slip-ring drives use an inverter to recover the power from the rotor circuit, feeding it back to the supply system.

The speed of slip-ring induction motor can be controlled by the following:

- Stator frequency control as with a cage rotor machine.
- Rotor frequency control.
- Rotor resistance control.
- Slip energy recovery (Kramer system). For capital cost reasons, the last two are commonly used.

Addition of rotor resistance especially for starting large induction motors is well-known. The basic effect produced by adding rotor resistance is to alter the speed at which maximum motor torque is developed. Unfortunately, power dissipation as heat in the rotor resistance bank takes place; earlier means to overcome this shortcoming were to convert the rotor power to DC and feed a DC motor on the same shaft. The rotor slip energy, when running at reduced speed, is therefore reconverted to mechanical power. This is the "Kramer" system. The disadvantages of this approach were the extra maintenance and capital costs.

The static Kramer system overcomes these shortcomings by replacing the DC machine with a line-commutated inverter that returns the slip energy directly to the AC line, either directly (on lower power systems) or via a transformer. A key advantage of the Kramer drive system is that the slip-energy recovery equipment (DC machines or static inverter) needs only be rated for a fraction of the maximum motor rating. This is true when a small speed range is required and provided that a separate means is provided of starting the motor. This is because the motor rotor current is proportional to torque and the rotor voltage inversely proportional to speed.

Naturally, if the slip-energy recovery network can be rated to withstand full rotor voltage (developed at standstill), a controlled speed range of zero to maximum could be achieved. However, this is generally only feasible on smaller motors (below 2000 kW) where the rotor voltage is sufficiently low for an economic inverter package. Secondly, if a full speed range is needed, the slip-energy recovery network has to be

rated at full motor power, so static Kramer drives become uneconomic for wide speed ranges. The overall system power factor would be very low for a wide speed range system.

For the above reasons, Kramer drives are very suitable for high-power drives (>200 kW) where a small speed range is required. Pump and fan drives present therefore good economic applications. Kramer drives have also been used for low-speed-range endurance dynos using the recovery system to control torque of induction generator. As with all line-commutated converters and inverters, current harmonics are produced, and these can be reduced to acceptable values. However, as the slip-energy recovery network is only power-rated in direct proportion to the speed reduction required (assuming constant load torque), the magnitudes of the harmonic currents generated are proportionally less than with drives where the solid-state converters have to handle the whole drive power. Harmonics of the rotor rectifiers are transmitted through the rotor and appear as noninteger harmonics in the main supply.

The main disadvantages of the slip-ring induction motor drive are (a) the increased cost of the motor in comparison with a squirrel cage, (b) the need for slip-ring maintenance, (c) difficulty in operating in hazardous environments, (d) the need for switchable start-up resistors, and (e) the poor power factor compared with other types of drive.

29.5.3 Synchronous Motor Drives

To understand the way the synchronous machine operates, let us assume that the induction motor were to rotate at the synchronous speed by an external means. Under this condition, the frequency and magnitude of the rotor currents would become zero. If an external DC power supply were connected to the rotor winding, then the rotor would become polarized in a similar way to a permanent magnet. The rotor would pull into step with the air-gap-rotating magnetic field, generated by the stator but lagging it by a small constant angle referred to as the load angle. The load angle is proportional to the torque applied to the shaft, and the rotor keeps rotating at synchronous speed, provided that the DC supply is maintained to the rotor field winding. The magnetic flux produced by the rotor winding intersects the stator windings and generates a back EMF, which makes the synchronous motor significantly different from the induction motor.

As with the induction motor drive, the requirement is to keep the ratio V/F constant (i.e., varies both the stator frequency and applied voltages in proportion to the desired motor speed).

The supply bridge converter is phase-controlled generating an adjustable DC current in the DC link choke. To generate maximum torque from the synchronous motor, this current is switched into the motor stator windings at the correct phase position with respect to rotor angular position as detected by the position sensor by the inverter bridge. When running above about 10% speed, the back EMF generated by the synchronous motor is sufficient to commutate the current into the next arm of the inverter bridge. So, as this type of inverter is machine (motor)-commutated, the inverter configuration is merely that of a conventional DC drive. The complexity, expense, and limited power capability of the force-commutated circuitry is therefore avoided.

The motor back EMF is insufficient for thyristor commutation at low speeds. The technique here, therefore, is to rapidly phase back the supply converter bridge to reduce the DC link current to zero and after a short delay (to ensure that all thyristors in the machine bridge are turned off) reapply DC current when the correct thyristor trigger pattern has been reestablished. As the motor speed and thus back EMF increase to a value sufficient for machine commutation, changeover to continuous DC link current operation is effected.

During the starting mode, the correct inverter bridge firing instant is determined by rotor position sensor, which is mounted on the motor shaft whose angular position is detected by opto or magnetic probes. When in the machine-commutated mode, sensing of stator voltage is used. To develop maximum torque in the low speed or pulsed mode, angular rotor position sensing is necessary. However, if less than full load torque availability at low speed can be tolerated, the inverter system can be set to produce a low fixed frequency in the pulsed mode. This frequency is then increased, as motor rotation is detected (either in steps or on a preset ramp rate) until sufficient back EMF is generated to facilitate changeover to the voltage-sensing mode.

As previously stated, the key advantage of this type of drive is that all thyristor devices are line- or machine-commutated. Expensive and complex forced commutation circuitry is avoided, and fast turn-off thyristors are unnecessary. Inverter systems of this type can therefore be built at very high powers, up to 100 MW. Also, as a result of avoiding force commutation, converter efficiency is high.

The thyristors in the machine inverter bridge must be triggered at such an angle to give sufficient time for commutation from one device to the next. This results in the synchronous motor operating at a high leading power factor of around 0.85. However, as far as the mains supply is concerned, the total drive has the characteristics of a DC drive where power factor is proportional to speed.

Another important characteristic of this type of drive is that it is inherently reversible and regenerative. For regenerative operation, the inverter bridge is triggered in the fully advanced position, so in effect, it becomes a plain diode bridge. A DC output voltage, approximately proportional to motor speed, is therefore generated at the DC side of the supply converter bridge. This converter bridge is now triggered in the regenerative mode thus returning power to the supply system. Reversing operation is achieved by altering the sequence in which the thyristors in the inverter bridge are triggered.

This type of drive is widely applied over a wide power range as it embodies an efficient brushless motor and relatively simple

and efficient converter. At lower powers, say below 30 kW, permanent-magnet synchronous motors are more common.

Unlike the induction motor, the synchronous type requires two types of converter: the first for main power conversion while the second is low power for field excitation. The field converter feeds the rotor exciter winding through slip rings and brushes, or alternatively, a brushless exciter can be used. A coordinated control of the two converters provides for active power and reactive power control and for efficient wide speed range control in high-power applications.

For high-power applications, synchronous motors are preferred because of the ability to control reactive power flow through appropriate control of excitation. Synchronous motors tend to have wider speed range and higher efficiency. However, synchronous motors are generally more expensive than induction motors.

With modern high-power PWM-VSI drives, synchronous motor can be driven for same inverter with vector control methods.

29.5.4 Special Motors

Motors under this category employ power electronics converters for normal operation. Generally, this type of motor has a large number of phases in order to limit torque pulsation and self-start from any rotor initial position. This is a new breed of motors, which can be fed through a unipolar or bipolar current. Also they have singly salient or doubly salient magnetic structures with or without permanent magnets on the rotor.

29.5.4.1 Brushless DC Motor Drive

This type of machine has a similar construction to a standard synchronous machine, but the rotor magnetic field is produced by permanent magnet material. A position sensor is used to ensure synchronism between the rotor position and the stator magnetomotive force (MMF) via drive signals to the inverter. The use of new magnet materials characterized by high coercive force levels has reduced magnet sizes and largely overcome the demagnetization problem. The absence of the field copper losses improves the machine efficiency.

As the permanent magnet is the source for excitation, the brushless DC motor (BDCM) can be viewed as a constant flux motor. A limited amount of flux weakening can be achieved by increasing the load angle of the stator current. Achieving a useful constant power range is not usually practical with this type of motor. A large demagnetizing component of stator current would be required to produce a significant reduction in magnet flux, and this would increase the stator loss substantially.

The required base torque determines the motor size, and the losses are essentially independent of the number of stator turns. At speeds up to the base speed of the constant power range, the efficiency of the motor is essentially the same as for one designed for rated voltage at base speed. For operation above base speed, the stator current from the inverter is reduced in inverse proportion to the speed. This mode of operation in the high-speed range reduces the dominant stator winding losses relative to a machine in which the flux is reduced and the current kept constant. The losses in the inverter are, however, increased due to its higher current rating. For an electric road vehicle that must carry its energy store, the net energy saving may be sufficiently valuable to overcome the additional cost of the larger inverter. A further advantage of this approach is that, if the DC supply to the inverter is lost, the open-circuit voltage applied to the inverter switches will be within their normal ratings.

The BDCM has higher volumetric power density compared with other types of motors (induction or synchronous). They are particularly suited for the high values of acceleration required in drives (e.g., machine tools). They are often operated with high acceleration for a short time followed by a longer period of low torque. At such low values of load factor, the cooling capability is frequently not a limitation. The major interest is in obtaining the maximum acceleration from the motor. The short-term stator current of a BDCM is limited to the value required for magnet protection. These values of acceleration are significantly higher than that can be achieved with either induction or DC motors of similar maximum torque rating.

29.5.4.2 Switched Reluctance Motor Drive

This motor can be regarded as a special case of a salient synchronous machine in which the field MMF is zero and the torque is produced by reluctance or saliency action only. The rotor has no winding. The switched reluctance motor (SRM) drive needs an inverter whose frequency is locked to the shaft speed, but since the torque is linearly proportional to the square of the stator current, the use of unidirectional current involves little sacrifice in performance.

Generally, the use of position sensors in the SRM and BDCM is something of a disadvantage in both cases. The SRM does not require permanent magnets, which can cost and may involve demagnetization risks and limit top speeds due to centrifugal forces. The SRM hence has a simpler construction and is more robust. However, the need to magnetize the motor from the AC side adds to inverter costs and may increase peak current levels significantly, hence raising stator copper losses.

Switched-reluctance synchronous motors have a cylindrical stator with three AC windings and a solid rotor (without any winding) with a moderate orthogonal axis magnetic saliency up to 4 (6) to 1. High magnetic saliency is obtained with multiple flux barriers. The conventional SRMs are to some extent (up to 100 kW) used in low-dynamics VSDs with open-loop speed control, as the speed does not decrease with load. Consequently, the control is simpler than with induction motors.

The main drawback of the conventional SRD is the low motor power factor and the relatively poor torque density, which leads to a higher kVA rating of the power converter ($\sim$20%). The main advantage of the synchronous reluctance motor over the induction motor of similar rating is the higher

efficiency. Compared with the squirrel-cage induction motor, the rotor loss is small or negligible in synchronous reluctance machines. If the saliency ratio is sufficient to produce a power factor equal to that of the induction motor, the stator winding loss will be the same. Also, the stator iron losses will be similar for the two motors.

The reluctance motor is capable of operation in the constant power mode of operation. As for all AC drives, when the supply voltage limit is reached above the base speed, the flux linkage is reduced in inverse proportion to the shaft speed, and the torque is inversely proportional to speed squared.

29.5.4.3 Linear Motors

There are applications in which linear motion, as opposed to rotational, is required. A linear machine has the same operating principles as those applied to all other rotating machines. The PWM-VSI converters and motor control principles discussed in this chapter are also applicable to this type of motor.

There are two types of linear motors:

- LIM—linear induction motor
- LSM—linear synchronous motor with permanent magnetic excitation

The LSM type has the following advantages over the LIM:

- Better power factor
- More responsive control
- Higher efficiency

The disadvantages of LSM are the following:

- Very accurate position feedback is required.
- The use of PM—expensive and heavy.

Transport, material handling, and extrusion processes are a few examples in which linear motors have successfully been employed.

29.5.4.4 Stepper Motors

Stepper motors are either built in a similar manner to BDCM, with permanent magnets embedded in or bonded to the rotor or a rotor with no magnets. The latter type is made of a ferrite magnetic material, and its circumference is cut to form a number of slots, forming teeth lengthwise to the rotor axis.

Torque production can be based on (a) magnetic reluctance (as in SRM), (b) magnetic attraction (as in BDCM), or (c) both magnetic reluctance and attraction.

Stepper drives do not offer dynamic speed control, and the main action is to accelerate at full torque to full speed, maintain the speed, and decelerate at full torque. In comparison with the reluctance-type stepper motor, the permanent magnet type offers greater torque for a given speed, particularly at start and low speeds.

Most drives incorporate controllers with connections for a communications link for supervisory control by PLC, hard-wiring connectors for analog/digital inputs and outputs, and some are equipped with software for communications with a computer or handheld keypad. Table 29.12 lists typical options.

Unlike above motor drives, the stepper motor can achieve precise position control without the need for any external feedback.

29.5.4.5 Actuators

Actuators are widely used in industry, primarily for positioning tasks. Their designs are based on all sorts of force-producing principles. Ref. [7] describes several types of direct drive electric actuators, including (a) the DC actuator (moving coil type), (b) induction actuators, (c) synchronous actuators (moving magnet DC type), (d) reluctance actuators, and (e) inductor actuators (polarized reluctance type).

Electric actuators are used increasingly in control systems and automated electromechanical equipment. Typical specification factors include range of motion, type of motion (linear

TABLE 29.12 Control features for servo and stepper motor drives (Ref. [6])

Control features	Servo drive	Stepper drive
Acceleration/deceleration time	Adjustable	Accelerate at maximum torque, time is dependent on maximum torque and inertia
Maximum speed	Part of the motor specification	Part of the motor specification
Speed control	Permit a range of speed settings	Not necessarily available
Torque control	Many offer speed and torque control	Always operate at maximum torque
Auto-tuning	A feature of some servo drive	Not applicable
Reversing	Commonly available by digital control signal	Commonly available by digital control signal
Zero speed clamp	Applies full torque to hold the position constant	Applies full torque to hold the position constant
Dynamic braking	Controlled deceleration, may require dissipative brake resistor	Usually standard
Regenerative braking	Dedicated circuit for controlled braking	Not applicable
Travel limits	Definition of travel limits in the forward and reverse directions	Standard
Jog or inch	Digital command to "jog" one step (with defined distance)	Optional feature
Closed-loop configuration	Most drives accept external signals for closed-loop control	Most drives accept external signals for closed-loop control
Programming functions	Many drives incorporate programming functions as in PLCs, reset all functions to default states, return to a home position, enable or disable repetition or a preset sequence, select a particular set of control inputs, increased or decreased speed, change the torque boost, etc.	

or rotary and stepwise or continuous), resolution needs, speed of response, environmental conditions, supply conditions, allowable electromagnetic noise emission level, need for integrated position and velocity sensors, maintenance needs, eligibility, cost, peak, and continuous torque.

The main demands of industry for high-performance systems are the following:

(a) A convenient supply and low power consumption
(b) Reliability and robustness
(c) Low initial cost and maintenance
(d) Fast response
(e) Linear "torque-excitation" characteristics

29.5.4.6 Integrated Motors

The integral motor consists of a standard AC motor with an integrated frequency inverter and EMC filter. It is robust and specified for reliable operation and often designed to handle rough working conditions, including ambient temperature −25°C to −40°C and dusty, corrosive, and humid environments (enclosure IP55). This type of drive uses a standard induction motor with the AC/AC converter integrated in the motor frame often as a separate converter box mounted directly above the motor frame in place of the terminal box. The power popularity of this type of drive is limited to 0.5–7.5 kW.

This type of motor offers the following advantages:

- Save space by eliminating the need for a separate controller
- Reduce installed costs because cabling between motor and converter is eliminated
- Eliminate motor problems caused by high voltage transient due to output cable capacitance
- Minimize EMC due to high dV/dt

The integrated drive includes most features including start, stop, forward, reverse, speed and torque controls, and controlled acceleration and deceleration.

29.6 PWM-VSI DRIVE

In recent years, the popularity of PWM-VSI has increased beyond recognition. Its dynamic performance and controllability is better than the DC drive. Its power range has extended to areas dominated for years by traditional solutions such as the cycloconverter and LCI drives.

29.6.1 Drive Comparison

Table 29.13 shows a direct comparison between the cycloconverter, LCI, and PWM-VSI drives. The DC drive and the slip-power recovery converter type are not listed because AC drives have already replaced DC drives in most applications due to low maintenance and better reliability of AC motors. Slip recovery is only suitable for applications with a limited speed range and requires a slip-ring wound rotor.

TABLE 29.13 Drive comparison

Control features	Cyclo	LCI	PWM-VSI	Matrix
Speed	Limited	Wide	Wide	Wide
Dynamic response	Excellent	Good	Excellent	Excellent
Torque pulsation	Low	High	Very low	Very good
Power factor at low speed	Poor	Poor	Very good	Very good
Stability	Good	Moderate	Very good	Very good
Motor	Custom	Custom	Standard	Standard[a]
Regeneration	Inherent	Inherent	Needs extra hardware	Inherent
Volumetric power density	Moderate	Good	Very good	Excellent

[a]The AC output voltage of the matrix converter is always less than the input voltage—derating is expected, or a larger frame size is required.

In comparison with the cycloconverter and LCI current-source converter drives, the PWM-VSI drive offers the following advantages:

- Excellent dynamic response
- Smooth torque/speed control over full speed range (0–200 Hz)
- High volumetric power density
- Ride through of dips in supply voltage
- Use of standard motors (squirrel-cage induction motor or synchronous motor)
- Improved AC supply power factor over full speed range
- Reduced cabling and transformer size and cost in comparison with cycloconverters
- No significant torque pulsation
- Lower noise level
- Low maintenance

29.6.2 Medium Voltage PWM-VSI

The maximum power rating of LV VSD is limited by practical current ratings of power components such as motor, cable, and transformer (typically 1500 A), giving a limit of about 2 MVA at 600 V. At this rating, motor manufacturers always prefer an MV machine design—significant saving and improved thermal performance of power components can be achieved by operating at medium voltages instead of low voltages. Many VSD applications will benefit from the availability of economic MV alternatives.

When adequately rated high blocking voltage devices are available, a simple two-level inverter or alternatively three-level neutral-point clamp (NPC) has always been the choice to meet required output voltages. These topologies offer a simple and cost-effective solution.

Series connection of power devices is the traditional solution for high-power high-voltage thyristor-based drives. This approach is perceived to be complex with fast-switching IGBTs because of simultaneous switching and correct static and dynamic voltage sharing of series devices.

The "multilevel" inverter drive is seen to offer a better solution for high-power, high-voltage inverter drive. The output waveform is high quality, even at very high modulation frequencies, which inherently results in lower harmonic content in the output voltage waveform (less losses, less torque pulsation, and lower insulation voltage stresses).

Ref. [8] and Fig. 29.5 categorize MV converter topologies as follows:

(A) Series-connected two level (SC2L)
(B) Three-level neutral-point clamp (3LNPC)
(C) Multilevel: diode-clamped multilevel (DCML) and capacitor-clamped multilevel (CCML)
(D) Isolated series H-bridge (ISHB) (Table 29.14)

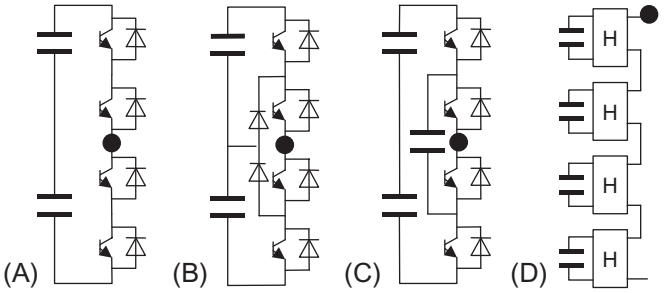


FIGURE 29.5 MV stack topologies.

29.6.3 Control Strategies

Several control techniques can be found in the VSD industry; refer to Fig. 29.6. These are the following:

- Open-loop inverter with fixed V/Hz control
- Open-loop inverter with flux vector control

TABLE 29.14 Comparison between different MV converter stack topologies

Topologies	Advantages	Disadvantages
Two-level with series devices (SC2L)	• Simple and proved technology • Same converter design over supply voltage range • Standard fully developed PWM control • Provision for series redundancy of power switches per inverter phase arm ($n+1$)	• Static and dynamic voltage sharing of series devices • High dV/dt due to synchronous commutation of series devices • High switching frequency harmonic content in inverter output voltage
Three-level NPC (3LNPC)	• Well proved • Reduced harmonic content • Better utilization of switches • Reduced dV/dt (half the SC2L equivalent)	• Series redundancy is difficult to achieve • More complex PWM control is needed than two level • Requires extra clamping diodes • Requires split DC link • Requires midpoint voltage balance control • Even number of power devices per arm is always needed • Switches require snubbers
Diode-clamped multilevel (DCML)	• Reduced harmonic contents • Reduced dV/dt	• Series redundancy is very difficult to achieve • Very complex PWM control is needed • Requires many steering diodes • Requires split DC link • Requires voltage balance control of split DC link capacitors • Uneven current stresses on power devices • Requires snubbers
Capacitor-clamped multilevel (CCML)	• This configuration has all the advantages of a multilevel converter plus simpler arrangement, modular building block • Less components • Snubberless operation is possible • Easier capacitor voltage balance than 3LNPC	• Possible parasitic resonance between decoupling capacitors • Complex to provide series redundancy • More complex PWM control strategy than for two level • Voltage redistribution of capacitors during supply voltage surges • Too many capacitors (bulky stack design and poor capacitor utilization at high ratings) • Complex converter arrangement (for low stray inductance) • Inverter rating is limited by the load current flowing through the capacitors
Series-connected isolated H-bridges (ISHB)	• Modular design of the converter power modules • The basic building block is based on a DC supply bridge, decoupling capacitor, and an H-bridge arrangement • In the AC supply, the combined diode bridge rectifiers act like a multipulse bridge (18p for four level and 24p for five level), reducing harmonic injection into the AC supply. • Its output has very low harmonic contents in spite of the low switching frequency	• Employs a special (bulky and expensive) transformer • Complex to achieve series redundancy • Different supply transformer designs are required for applications operating at different AC line voltages • Power pulsation for poor power factor loading • Poor utilization of capacitors • Not suitable for common DC bus applications • Dynamic braking is difficult

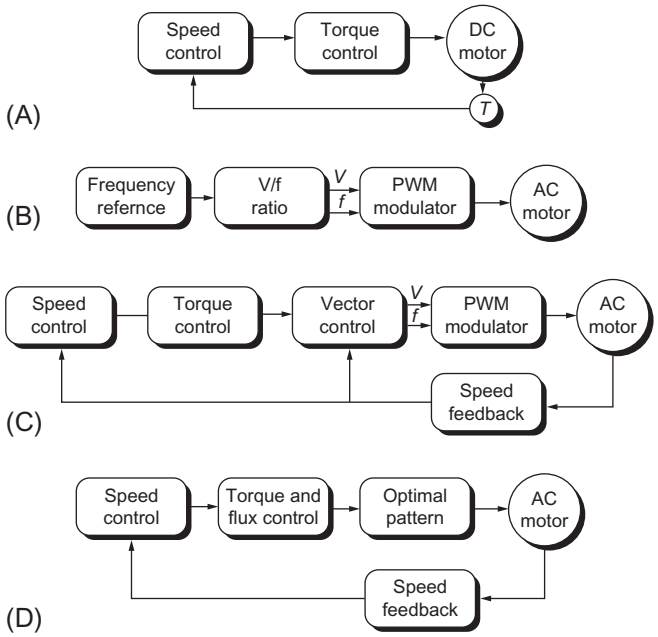


FIGURE 29.6 Electric drive control techniques. (A) DC drive, (B) frequency control (PWM scalar control), (C) flux vector control (field-oriented control), and (D) direct torque control.

- Closed-loop inverter with flux vector control (induction motor)

Table 29.15 summarizes the main features, advantages, and disadvantages of each technique.

29.6.4 Communication in VSDs

The use of a high-speed advanced digital communication (fieldbus) to build industrial automation system for real-time control or simply for data logging has become well established in modern industries. Digital communication resulted in replacing wiring looms with a digital serial network; this resulted in a lower cost installation and a more reliable solution. Over the last few years, many industrial fieldbuses emerged, and end users, system integrators, and original equipment manufacturers (OEMs) chose the optimum system for their applications.

A fieldbus is a digital communication system that allows a control system to exchange data with remote sensors, actuators, and drives using a single communication link. The major benefits seen are (a) reduced installation and cabling cost and better overall immunity of the system. Both factors result in a more reliable operation and reduced maintenance costs.

There exist two main types of network:

(a) Centralized network—requires a network master controller, typically a PLC. The master device is entirely responsible for controlling communications over the network, while the slave devices tend to be "dumb" devices with no local intelligence.
(b) Decentralized network—which requires some local intelligence at each node but no overall master device. This is ideal for real-time application environment, as all nodes are effectively running in parallel.

Most modern VSDs are equipped with hardware and software, which enable local and remote communication with plant

TABLE 29.15 Comparison between various control methods used in VSD

Drive type	DC drive		AC drive	
Control method	• Field oriented	• Frequency control	• Flux vector control	• Direct torque control
Features	• Field orientation via mechanical commutator • Controlling variables are armature current and field current • Torque control is direct • Typical response 10–20 ms	• Voltage and frequency control • Simulation of variable speed drive using modulator • Flux provided with a constant *V*/*F* ratio • Open-loop drive • Load dictate torque level • Typical torque dynamic response 100 ms	• Field-oriented control—similar to DC drive • Motor electric characteristics are modeled (observer) • Closed-loop drive • Torque controlled indirectly • Typical torque dynamic response 10–20 ms	• Use advance control theory • Controlled variables are magnetizing flux and motor control • Typical torque dynamic response is <5 ms
Advantages	• Accurate and fast torque control • High dynamic speed response • Simple to control	• Low cost • No feedback devices are required • Simple	• Good torque response • Accurate speed control • Full torque at zero speed • Performance approaching DC drive	• Simple • No feedback requirements • No need for an observer
Disadvantages	• Reduced motor reliability • Regular maintenance • Motor costly to purchase • Needs encoder for feedback	• Field orientation not used • Motor status ignored • Torque is not controllable • Delaying modulator used	• Feedback is needed • Costly • Modulator is needed	

automated system via a fieldbus system. The most popular fieldbuses are Profibus, Interbus, Ctnet, Sercos, Worldfib, and DeviceNet.

29.6.5 PWM Techniques

Different PWM techniques have been employed in PWM-VSD converters. Fig. 29.7 identifies the most commonly used techniques.

29.6.6 Impact of PWM Waveform

29.6.6.1 PWM Voltage Waveform

Fast switching of IGBTs (typically <1 μs) results in high *dV/dt*, typically 3–5 kV/μs, and possible voltage overshoot at turn-off that can last for a few microseconds. The fast rate of rise/fall of voltage combined with high peak voltage at the turn-off results in a premature failure of motors and EMC. Refs. [9–11] deal with the effect of PWM waveforms of VSD.

The following is a brief summary of the effect of the unfiltered waveforms.

29.6.6.2 Effect on Motor

- Premature insulation failure due to partial discharge as a result of peak voltage, high *dV/dt*, and high frequency.
- Motor shaft voltage that forces current into the shaft bearing, leading to early bearing failure.
- Motor stray capacitance (between windings and earthed frame) leads to earth-current flow caused by high *dV/dt*.
- High *dV/dt* creates nonuniform distribution of voltage across the winding, with high voltage drop across the first few turns and consequential failures.
- In a large motor, voltage differential on the frame is likely to develop in spite of protective earthing of the motor. More than one earthing point is needed.

29.6.6.3 Effect on Cables

- Voltage-doubling effect at the rising/falling edges of voltage waveform due to wave propagation in long cables [9].
- Earth-current flows in cable stray capacitance due to *dV/dt*.
- Restriction on cable type used and earthing methods employed.
- Cable type (armored, screen, and multicore).
- Likelihood of cross talk with other surrounding cables running in parallel.
- For PWM drives, the cost of cabling is likely to be significant due to special requirements of cables and termination methods employed.

29.6.6.4 Effect on EMC/Insulation/Earthing

- Inductive and capacitive couplings between live components and earth result in common-mode and differential-mode noise. This could lead to malfunctioning of nearby sensitive equipment.
- The voltage to earth applied on drive components pulsates at the switching frequency, adding voltage stresses (worst at low speeds and low modulation index). This poses

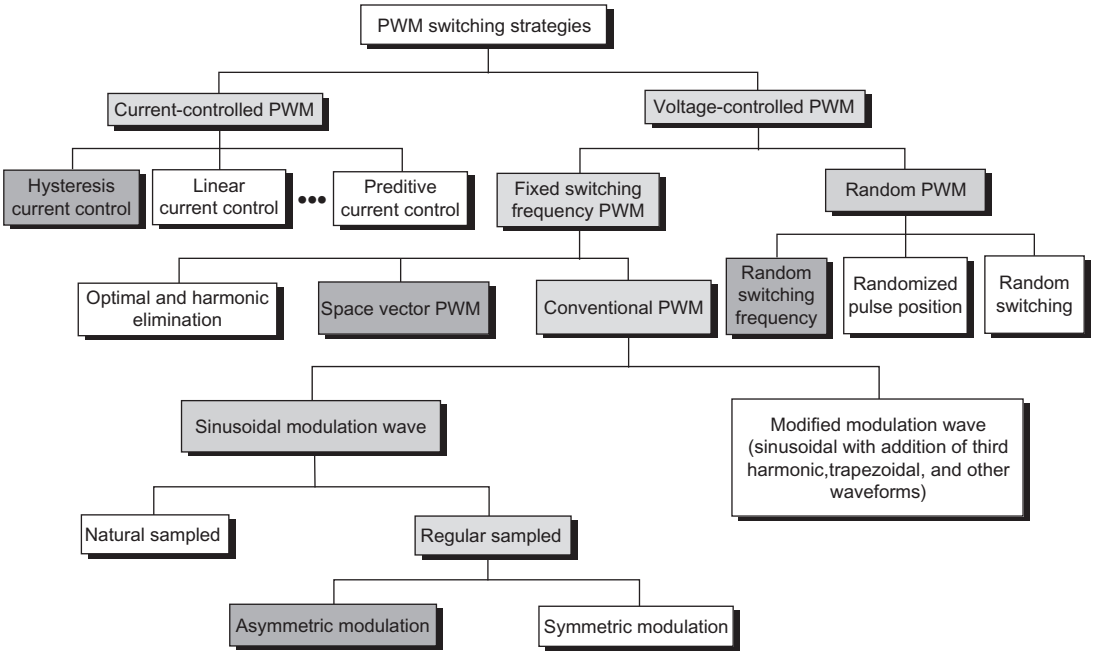


FIGURE 29.7 Classifications of PWM techniques.

additional insulation requirements on main power components (motor, cable, output filter, and transformer).
- A fourth wire may be required between the motor frame and the converter virtual earth so that a low impedance path is provided for the motor earth current.
- Strict rules must be observed when cabling and earthing.

29.6.6.5 Motor Insulation

High peak voltages can be experienced at the motor terminals especially when long cable is employed (10–100 m depending on the size of motor). This is usually caused by voltage-doubling phenomena of a transmission line with unequal line and load impedance. Motor line voltage can reach twice the DC link voltage with long cables.

Fast voltage rise times of 5000 V/μs can be measured at the motor terminals. Under this condition, the motor insulation becomes stressed and can lead to a premature breakdown of a standard motor insulation. When motor fails due to insulation stress caused by high peak voltage and fast voltage rise times, failure occurs in the first turn as phase-to-phase short or phase-to-stator short. The highest voltage is normally seen by the first turn of the winding.

Standard motor capabilities, established by the National Electrical Manufacturers Association (NEMA) and expressed in the MG-I standard (part 30), indicate that standard NEMA type B motors can withstand 1000 V peak at a minimum rise time of 2 μs (500 V/μs). Ref. [10] describes the effect of PWM inverter waveform on motor insulation in more detail.

Partial discharge

The phenomena that starts deterioration of the motor insulation is called partial discharge (PD). When electric stresses in insulation voids exceed the breakdown voltage of the air, a partial discharge occurs. Successive PDs destroy the insulation slowly.

Voltage strength between phase to phase and phase to frame

Both NEMA and IEC are proposing (a) maximum 1000 V at rise time <2 μs and (b) a maximum rate of rise of 500 V/μs. It is believed that low-voltage standard motors can withstand a lot larger voltage stresses than specified by NEMA and IEC, possibly up to 1300 V, almost regardless of the rise time.

Voltage strength between turn to turn

In low-voltage AC motors, the conductor insulation is designed for 245 V RMS (350 V peak). The insulation strength is however higher depending on the impregnation method.

29.6.6.6 Bearing Current

Bearing current and shaft voltages under 50/60 Hz sine-wave operation has been recognized since 1924. The bearing impedance characteristics largely determine the resulting bearing current that will flow for a given shaft voltage [11].

The rotating machines have three basic sources of shaft voltage. These are the following:

- Electromagnetic induction from the stator winding to the rotor shaft (due to small asymmetries of the magnetic field in the air gap that is inherent in a practical machine design). The design limit is <1 V RMS.
- Electrostatic coupled from internal sources: such as voltage in motors where rotor charge accumulation may occur (belt-driven coupling and ionized air passing over rotor fan blades).
- Electrostatic coupled from external sources such as PWM inverter. The presence of high *dV/dt* across the stator neutral to frame ground causes a portion of the voltage to ground due to capacitor divider action. The presence of PWM-related voltage components is undesirable and leads to a premature bearing failure.
- The fundamental cause of the shaft voltage is magnetic asymmetry between the stator and the rotor or possibly a phase shift of the motor voltage waveform. System ground may also contribute to this condition through unbalance system voltage.
- NEMA-500 recommends the consideration of insulated bearing for motor frame of certain sizes.

29.6.6.7 Electromagnetic Compatibility

The main sources of electromagnetic emission of PWM-VSI drives are described in [12] as follows:

AC/DC converter: Supply harmonics caused by supply bridge rectifier (from 100 Hz to 2.5 kHz): as already explained, the input bridge circuit with an SCR or diode bridge is a source of supply harmonics in the input current.

DC/AC inverter: Harmonics caused by the switching of the inverter bridge (from 3 kHz to 20 MHz): the inverter bridge uses fast-switching devices to create PWM voltage output. The inverter is a source of a wide band of frequencies, typically extending from the basic switching frequency (usually several kilohertz) to the radio high-frequency bands at 20 MHz. The radio frequency current spreads out into both the supply and motor connections. An EMC filter is often used to limit the spread of high-frequency harmonics into the supply.

Control electronics: The control circuit employs a microprocessor with clock frequency of several megahertz, typically 20 MHz. The clock wave produces frequencies, which are multiple of 20 MHz up to 300 MHz (Table 29.16).

29.6.7 Techniques Used to Reduce the Effect of PMP Voltage Waveform

29.6.7.1 Output Line Reactor

A reactor increases the rise time, but the benefit of its connection may be negated as follows:

- Beneficial connection if cable length is short enough for reflections to be superimposed within rise time, that is,

TABLE 29.16 An overview of techniques used as a counter measure to EMI

Effect	Frequency range (f)	Counter measure	
		At source	At load
Mains	$\leq$100 Hz	• Avoid circulating currents	• Balanced signal circuits • Avoid earth loops in signal paths • Screening (electric field only)
Mains harmonics	$100 < f \leq 2.5$ kHz	• Line and/or DC link reactor on rectifiers. • Higher pulse number rectifier (e.g., 12, 18, or 24) • Low impedance supply • Harmonic filters	• Balanced signal circuits • Avoid earth loops in signal paths • Filtering
Intermediate	$2.5 < f \leq 150$ kHz	• Filters	• Filtering • Screening • Balanced signal circuits
Low frequency	150 kHz $< f \leq$ 30 MHz	• Filters—one per apparatus • Cable screening	• Filtering • Screening
High frequency	30 MHz $< f \leq$ 1 GHz	• Screening • Internal filtering	• Screening

if rise time is increased beyond critical value of cable length.
- Harmful connection if cable length is too long; the reactor may have negligible effect on peak voltage (theoretically, its presence is insignificant in this case) or ringing period, but it will increase the duration of each overshoot, thus increasing the probability of partial discharge.

Adding a series line reactor between the motor and inverter is not as simple as illustrated above because the reactor adds or adjusts other resonant modes where the reactor rings with lumped capacitance. These resonant modes are pure transmission line modes and can double voltage. Some line inductance helps short-circuit protection. If earth current is limited by other means, then the coupled reactors may be helpful.

29.6.7.2 Sine-Wave Filter

This mechanism filters the PWM carrier frequency; thus, the converter output voltages are sinusoidal. This type of filter is best suited for low-performance drives and/or retrofit applications (old or standard motors). Ref. [13] and Table 29.17 illustrate the filtering options for high-power VSDs.

Employing a filter at the inverter output has some practical consequences:

- Cost and weight of filter
- Filter power losses and voltage drop
- A small derating of power switches due to circulating current between filter L, C, and DC link capacitor
- Reduced torque response due to time delay in the filter, sine-wave type
- Potential oscillations that have to be electronically dampened
- Potential induction motor self-excitation

29.6.7.3 PWM (dV/dt) Filter

This reduces the dV/dt seen by the motor to a level, which does not compromise the motor or EMC. It is ideal for high-performance drives with custom-built motors.

29.6.7.4 RC Filter at Motor Terminals

A simple RC network is used at the motor terminal; the capacitor would represent a short circuit for the high-frequency components (sharp dV/dt). Wave reflection will not happen if the resistor value is similar to the cable characteristic impedance. Resistor losses are generally small, as current flow will only occur at the rising and falling edges of the PWM waveform.

29.6.7.5 Common Mode Reactor

The presence of capacitive current due to the high dV/dt can be improved by employing a common-mode reactor. It is well established that such a choke is not effective to reduce the RMS and mean values of the leakage current but only effective to reduce the peak value. The presence of such a choke in the circuit increases the inductance and resistance of the zero sequence impedance.

29.6.8 Supply Front-End for PWM-VSI Drives

There are many types of PWM voltage-source drive depending on the supply front-end type and regenerative technique employed (Table 29.18):

(i) PWM-VSI with a diode supply front end
(ii) As above but with a dynamic brake chopper
(iii) Fully controlled thyristor front end
(iv) As above but with a dynamic brake chopper
(v) Fully controlled antiparallel thyristor supply bridge
(vi) PWM supply front end

TABLE 29.17 Filtering options for PWM-VSI drives (Ref. [13])

Option	No filter	*dV/dt* filter	Sine-wave filter
Motor *dV/dt*	High	Acceptable	Low
Motor insulation	Must be increased	Normal	Normal
EMC ground noise	Very high	Low	Very low
PWM carrier at motor	100%	100%	Very low
Motor audible noise	Higher	Decreased a little	Minimum
Motor derating	Approx. 13%	Approx. 3%	0%
Torque response	Fast	Fast	Suits most applications
Motor cost	Typically +10% cost	Normally no extra cost	No extra cost
Conclusions	Impractical	Suitable only for high dynamic torque response	Best choice for most drives

The use of a higher pulse number than 6-pulse would necessitate the use of a supply transformer. This is always considered to be an unnecessary "evil" because of additional cost, losses, and the need for extra space to accommodate this component. For MV applications, this is considered to be a necessity for isolation and protection.

29.6.8.1 Regenerative Braking

Several techniques are usually used for regenerative braking.

A simple diode front-end supply bridge will operate in two quadrants (positive and negative speeds). There is no regenerative power capability as any regeneration of power would result in an increase in the DC link voltage, and the drive will trip on overvoltage.

If a small amount of regeneration is required, during stopping, or speed reversal, then a dynamic brake chopper may be used. This is a simple chopper with a dynamic brake resistor. The size of the resistor is very much dependent on the regenerative brake energy, its magnitude, and repetition rate.

Full power regeneration is possible by employing a fully controlled antiparallel thyristor front end. This is similar to that used on DC drives or cycloconverters.

A more modern approach is to use pulse converter front end (fully controlled bridge). This is a four-quadrant converter with the ability to control the power factor and the DC link. Such an option necessitates the use of a precharge circuit for the DC link and smoothing inductance on the AC side.

For fully regenerative drives, the supply needs to be receptive.

By using a PWM rectifier as a primary converter in this composite structure, both the problems of regeneration and line current distortion are successfully solved—with the penalty of having a much more complicated converter structure and control system.

With the modern PWM-VSI VSD controller, the supply bridge can be fully controlled. Such an option offers the following benefits:

- Fully regenerative drive
- Unity power factor all time
- Sine-wave input voltage and current
- Can operate with controlled power factor (e.g., leading power factor)

TABLE 29.18 Types of supply front-end bridges of PWM-VSI drives

Type	Power device	Motor speed reversal	Regenerative capability	Regenerative with AC supply loss	Comment
I	Diode	Yes	No	No	• Good power factor across speed range • Needs precharge circuit • The lack of protection
II	Diode	Yes	Dissipative	Yes	• Ditto
III	SCR	Yes	No	No	• Power factor is function of speed • Fully controlled DC link • Phase back when (a) supply voltage rises, (b) fault on DC bus side • Needs gate drivers for SCRs
IV	SCR	Yes	Dissipative	Yes	• Ditto
V	SCR	Yes	Regenerative into supply	No	• Ditto
VI	Forced commutated devices (e.g., IGBT/IGCT)	Yes	Regenerative into supply	No	• Can operate with controlled power factor (unity, lagging, leading) • High-frequency harmonics • DC link voltage higher than the crest of the supply voltage • Fully controlled DC link, even during a supply dip • Output voltage equals to input voltage • Requires a precharge circuit

- Can operate as an active filter while supplying power to the load. Possible elimination of low-order supply harmonics (fifth and seventh)
- Output voltage equals the input voltage

29.7 Applications

29.7.1 VSD Applications

Table 29.19 summarizes main industries and applications.

Present solution of drives and electric drive application examples from various industries have been described in this section.

29.7.2 Applications by Industry

29.7.2.1 Deep Mining

Ref. [14] lists various high-power MV VSI inverter drive applications for the mining industry. In deep mine conveyor belt applications, a PWM-VSI drive offers significant advantages over other conventional alternatives. The following benefits have been identified for deep mine conveyor belts applications:

- Improved drive starting and stopping
- Improved reliability
- Matching belt speed to production
- Easier belt inspection
- Reduced belt wear and increased belt life
- Lower specification belt material may be used
- Low speed running to reduce coal removal by windage
- Manpower saving—less coal spillage
- Unity power factor with low harmonic content
- Reduced AC supplies disturbances

For hoist applications, the PWM-VSI drives can also be used to replace DC and cycloconverter drives for mine hoist applications. The benefits are the following:

- Improved drive control, with 100% continuous stall torque available with induction motors
- Reduced AC supplies disturbances
- Very unlikely to need reactive MVAR correction even at high ratings
- Improved immunity to AC supplies dips

The use of electrically coupled mine hoist systems has many advantages especially for deep mines and set to become an essential feature of many new mine shaft systems. The circuit is shown in Fig. 29.8.

The power flows naturally from motor 1 to motor 2 such that at the point of balance, the AC supply current is virtually zero and at near-unity power factor.

This technology is the natural successor to the DC electrically coupled winders and totally solves the poor AC power factor that would result if twin drive cyclo motors were used.

29.7.2.2 Industrial Processes

In this industry, there are a number of viable drive solutions available for the major market power ranges, from LCIs to FCI. However, there is a developing market for MV variable speed drives. The PWM-VSI using new high-power IGBTs or IGCTs appears to be the best solution for the future. Benefits include better power factor, no limit on frequency, and higher voltages.

PWM-VSI converter cost is likely to be higher than equivalent other well-established technologies (e.g., LCI). Hence, the

TABLE 29.19 Application analysis of VSDs

Industry	Current drive topology	Preferences	Applications
Power generation	Direct on line (DOL) Soft start CSI3	• 6.6–11 kV	Boiler feed pump, start-up converter, coal mills
Petrochemical	LCI DOL CSI3	• Air-cooled, stand-alone • Induction motors up to 10 MW • Synchronous above 10 MW	Petrochemical and derivatives, gas liquefaction, pipelines and storage, oil on/offshore and pipelines
Mining	Cycloconverters	• Low maintenance • Reliability • Low power supply distortion	Mine winders, conveyor belts, coal mills, ventilation fans, underground machinery
Stand-alone and process industries		• Low cost • Efficiency • Ease of repair and maintenance	Water and sewage pumps, wind mills, material handling (extruders), test benches, paper and plastic machines
Metals	Mill drives—cycloconverters	• Air-cooled • High dynamic performance • Low maintenance motor	Hot mills, medium section mills, finishing section mills, cold mills
Marine	LCI cycloconverters	• Small size • Low maintenance • Water-cooled	Warships, drilling vessels (mono hulls), chemical tankers, shuttle tankers, cruise liners, icebreakers, semisubmersibles, fishing vessels, cable layers, floating exploration rigs, ferries, research vessels, container vessels

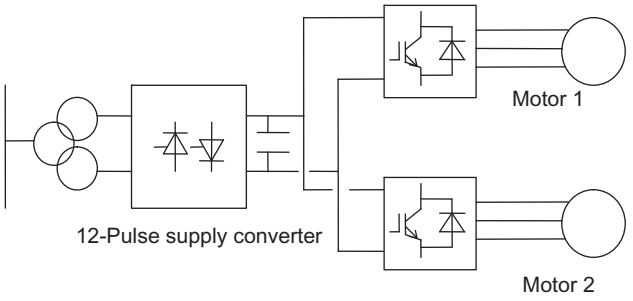


FIGURE 29.8 PWM-VSI electrically coupled mine hoist drive.

flexibility in choice of motors and improved control must be exploited. The advantage of offering an MV solution may prove significant. Possible means of reducing motor costs are the following:

1. Higher frequencies are achievable, allowing the use of high-speed motors and gearboxes.
2. Higher pole number machines can be used, giving a cost saving.
3. Better power factor over the speed range giving power supply saving.
4. Induction motors with rotors adapted for use with VSDs can be used with resultant cost savings over standard DOL, fixed speed motors.
5. Higher voltages and smaller conductors.
6. However, at low powers, the relative cost of the machines is less significant versus the cost of the converters. Hence, the viability of this technology in this market requires close examination.

The cycloconverter drive with a synchronous motor is used when four-quadrant operation is required. Particularly for high power rating with high torque at low speed and at standstill but with a rather low maximum speed are drive requirements. Gearless cement mill drives were the first applications of cycloconverters. The mill tube is driven from low-speed wraparound motor with a high number of poles.

29.7.2.3 Metal Industry

The majority of installed hot mill drives are cycloconverters. A few LCI drives have been used, but applications are limited for such technology on mill main drives. Most early-generation plants are equipped with DC drives. The trend is to replace DC with AC.

Direct current drive applications were universally used in the first generation of rolling mills. The market for new mills requiring this technology is declining as the steel industry moves to AC as a preference. On early-generation mills where motors are retained, DC drives are likely to be required. Customers in their inquiries, some requesting AC alternatives, are still requesting DC drive solutions.

DC drives are probably still the most economic for the power range of 750–1500 kW. The number of manufacturers however, producing DC motors, is declining, particularly in the case of large DC motor manufacture. The lower price of DC solutions is offset by the advantage of the use of AC motors in AC solutions, making AC the more popular choice.

Current-source inverter LCI can be applied to roughing stands of rod and bar mills. Technical limitations include the risk of torque pulsation and a minimum drive output frequency of 8 Hz.

Cycloconverter is the solution most often used. However, it is relatively expensive compared with alternative technology. Major cost penalties arise from supply transformers, cabling, and bridge configuration. In some cases, active power supply compensation equipment may be required, taking the costs even higher. Cycloconverter solutions will still be cost-effective for medium-to-high power, low-speed, low-frequency (say below 21 Hz maximum operating frequency) applications. This would include hot reversing mills, with direct drive, for the primary rolling processes, albeit a declining application area, and possibly for direct-drive, low-speed, high-torque roller-table applications. Technical limitations include limited output frequency (typically 29 Hz for 12-pulse at 60 Hz supplies), which can necessitate the use of two-pole motors to reach application speeds.

The high-power PWM-VSI using new power devices (IGBT/IGCT) appears to be the best solution for the future. Benefits include better power factor, no limit on frequency, and higher voltages. Potentially, either the two-level or the multilevel solution will meet the market requirements.

In some applications, like coilers/uncoilers, the system is composed of several drives, which have different power cycles; when some drives are furnishing power, others are braking. A common DC bus system will allow that the energy fed from drives operating in the regenerative braking mode will be utilized by other drives connected to the same DC bus but operating in the motoring mode. The supply bridge, that is, rectifier, feeding the DC bus system will only be rated for the total system power.

The benefits of the DC bus systems include the following:

- Good operating power factor
- Low harmonics (lowest when using 12-pulse or 18-pulse front ends)
- Possibility of energy transfer on the common DC link solutions (reducing front-end converter and transformer sizes with attendant energy saving, possibility of using kinetic energy to allow controlled stopping)

29.7.2.4 Marine and Offshore

Drive powers are commonly in the range of 0.75–5.8 W for thrusters and 6–24 MW for propulsion. The evolution in the commercial market is toward powers from 1 to 10 MW for propulsion. Higher powers are required for naval applications with package drive efficiency better than 96%.

The PWM inverters at these powers would allow the use of induction machines, rather than the more expensive

synchronous alternatives required for LCI drive. This could give savings in the price of the motor.

Current source inverter (CSI) drive LCI is used for all applications except for icebreakers where cycloconverter drives are used. The PWM (voltage source) inverter using new force-commutated drive appears to be the best solution for the future. Benefits include better power factor, no limit on frequency, and higher voltages. Many icebreakers and some other ships are equipped with diesel-generator-fed cycloconverter synchronous motors with power ratings up to about 20 MW per unit.

29.7.3 Examples of Modern VSD Systems

29.7.3.1 Integrated Power System for All Electric Ship

This is a full-scale main propulsion drive for the US Navy [15]. It consists of a main propulsion 19 MW induction motor drive system. The power converter consists of three 6-pulse rectifier stages, three 6 kV DC links, and 15 IGBT-based H-bridges feeding a 15-phase induction motor (Fig. 29.9).

This drive demonstrates the potential of modern power electronics over more traditional solutions such as cycloconverter and LCI. The volumetric power density of the new converter is reported to be 905 kW/m^3, compared with 455 kW/m^3 for cyclo and 313 kW/m^3 for LCI.

29.7.3.2 Subsea Separation and Injection System

This is a full-scale pilot plant developed to increase recovery and improve the economics of offshore oil and gas fields. The system comprises several VSD units, typically 500 kW oil pump, 1 MW multiphase booster and 1–2.5 MW water injection drive unit, and such a system is called "SUBSIS" [16]. The main task for such a system is to separate the bulk water from the well stream and treat it either for discharge into the sea or reinjection into the reservoir.

This system employs subsea-based rotating machinery for pumping, boosting, and compression. The subsea electric power distribution system (SEPDIS) is an innovative and cost-effective subsea processing (Fig. 29.10). The pump motors are mounted in a pressurized vessel and positioned on the seabed. Ref. [16] identifies the benefits of subsea drives as follows:

- 3%–6% increase in oil and gas recovery
- Improved pipeline transportation conditions by removing water from the well stream
- Reduced environmental impact due to lower energy consumption and reduction in chemicals used to inhibit corrosion
- Reduced size and cost of new platforms
- Cost-effective development of marginal fuels through reuse of existing infrastructure

29.7.3.3 Shaft-Generator for Marine Application

During cruising at sea, up to 3.5 MW of electric power is extracted from the ship's main diesel engine/propeller shaft (90,000 hp per ship) via a salient pole shaft generator, which is fitted to the main propeller shaft. The converter output voltage (set at 60 Hz) is stepped up to 6.6 kV [17].

The converter is based on 24-pulse converter (LCI) technology, which is traditionally used as main ship propulsion. The shaft generator output frequency varied between 14 and 25.7 Hz; six-phase generator and the output stage are configured as 24-pulse, via a step-up transformer. At the output, a passive LC filter is employed, with a synchronous condenser started by a pony motor.

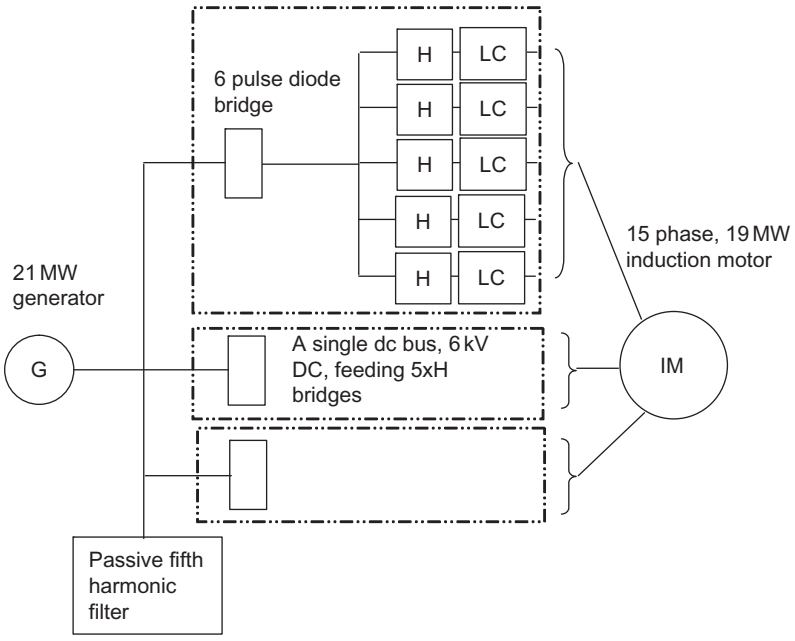


FIGURE 29.9 Schematic diagram of the IPS drive system [15].

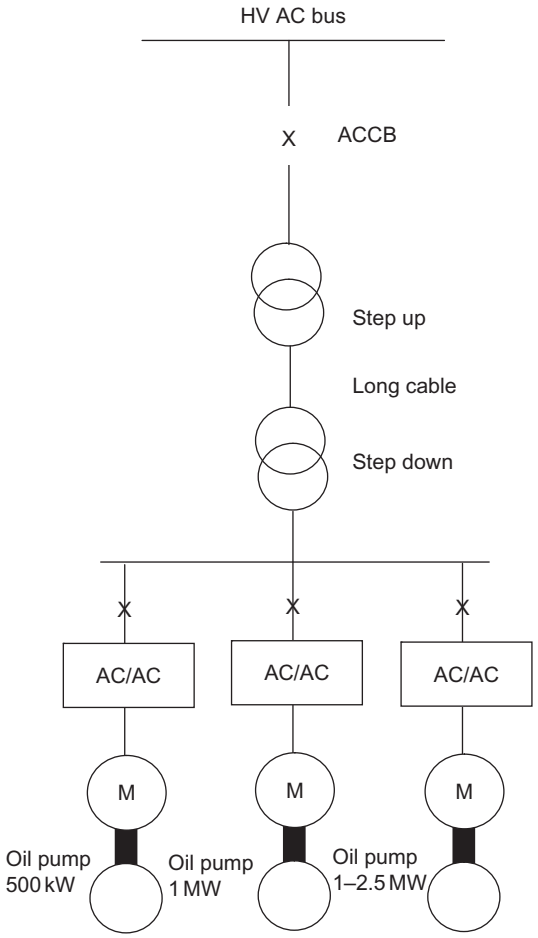


FIGURE 29.10 Schematic diagram of SEPDIS.

This type of application is likely to significantly benefit from the higher volumetric power density of the PWM-VSI with fully controlled front-end. Such a system will eliminate the need for a passive filter at the output stage and use a standard three-phase generator.

The same technology is also applicable to high-speed generators and windmill energy. The ability of the active front end to sustain fixed DC link voltage over a relatively wide shaft speed range results in a very good control of the output voltage, irrespective of the shaft speed.

In wind power plants, the optimal efficiency of the wind turbine depends on the speed when the wind conditions change. It is, therefore, advantageous to vary the speed of the generator and link it via a frequency converter to the AC system.

For high-speed generators, driven by diesel engine or gas turbine, the fully controlled converters enable direct power conversion from AC high frequency (hundreds of Hz) to fixed power frequency (50/60) Hz fixed output voltage. The magnitude of the output voltage is kept constant irrespective of speed variation of the generator (Fig. 29.11).

29.7.3.4 Linear Motor Drive for Roller Coaster

This drive involves a fully regenerative PWM-VSI. The supply front end is made of antiparallel thyristor front end, while the machine bridge is based on PWM IGBT VSI. "Superman" has been developed for Six Flags California at Magic Mountain. The inverter output frequency is 0–230 Hz and 525 V AC RMS. The power rating is 1.8 MW. The duty cycle is 1.8 MW for 7 s, followed by 16 s at zero power, and 1.3 MW for 5 s and a stop period of 32 s. This ride involves acceleration at 4.5 g, speed and free fall (6.5 s of weightlessness, during which a height of 415 ft is achieved [18]).

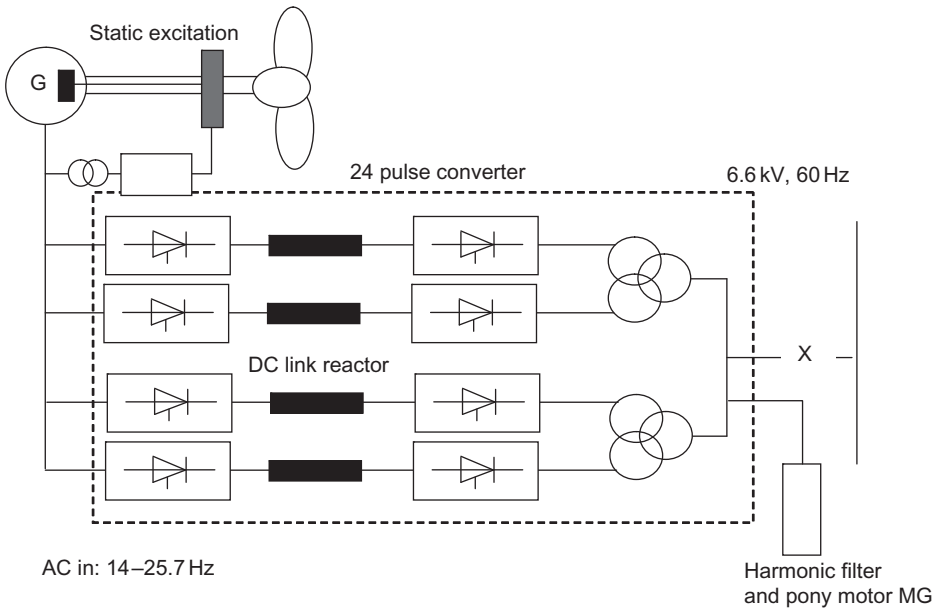


FIGURE 29.11 Schematic diagram of shaft generator.

The same concept employed in this application could be used for aeroplane launcher on aircraft carriers, instead of the conventional catapult.

29.8 Summary

The benefits of VSD are there to be quantified, and energy saving has been the prime reason for employing a VSD in standalone drive applications. Other benefits such as improved process control or increase life expectancy are often difficult to quantify in real terms.

There is a large selection of VSD systems to meet a wide range of applications. In the low and medium power, the induction motor and PWM-VSI are supreme. At higher power ratings, MV PWM-VSIs are gaining popularity, but LCI and cycloconverter drives would remain key technologies with very high power applications.

Modern drives are becoming more available at competitive prices with good reliability record. However, there are concerns with regard to the impact of fast switching on the motor and the environment.

To ensure successful implementation of a VSD system, both the supplier and end users need to work in partnership. Ideally, one competent supplier should supply the full drive package, with some after-sale service support. Understanding the nature of the load plays an important role in specifying the power rating of VSD correctly to meet performance requirements and required life expectancy.

New areas of VSD applications are emerging as the power electronics advances and become more reliable at affordable prices. Packaged drives up to several hundred kWs are becoming a commodity product, and end users do not need to involve a third party during specification, installation, and commissioning. Integrated motors are likely to increase their popularity, possibly with new types of power converters, for example, matrix.

References

[1] W. Dury, Electrical variable speed drives mature consumable or radical infant, Power Eng. J. 13 (2) (1999) 65–78. IEE, London.
[2] Guide to Harmonics with AC drives. ABB Technical Guide No. 6.
[3] B.K. Bose, Power Electronics and Variable Frequency Drives: Technology and Applications, IEEE Press, Piscataway, NJ, 1997.
[4] Siemens, Complete Guide Series to Variable Speed Drives, Knowledge of Motor Duty—Key to Proper Planning of Drives, 3.6.
[5] P.J. Hobbs, Electrical variable speed drives saves energy, in: Conference on Development in Variable Speed Drives for Fluid Machinery, ImechE, 1981. C101/81.
[6] A.W. Richmond, Apprentice Engineers' Handbook No. 2, Servos and Steppers, Drives and Controls Publication, Kamtech Publishing Ltd, Croydon, Surrey.
[7] Y. Shakweh, Aspects of Limited Motion Actuators and Sub-kW Unipolar Drives (Ph.D. thesis), London University, 1989.
[8] Y. Shakweh, E. Lewis, Assessment of MV converter stack topologies, in: Power Electronics Specialist Conference, 1999.
[9] A. von Jouanne, et al., Application issues for PWM adjustable speed AC motor drives, IEEE Ind. Appl. Mag. (1998) 10–18.
[10] L. Manz, Motor insulation system quality for IGBT drives, IEEE Ind. Appl. Mag. 3 (1997) 51–55.
[11] S. Chen, T.A. Lipo, Circulating type motor bearing current in inverter drives, IEEE Ind. Appl. Mag. (1998) 32–38.
[12] C. Hargis, Electro-Magnetic Compatibility—A Basic Guide for Power Engineers, Control Techniques Technical Publications, Powys.
[13] Y. Shakweh, P. Aufleger, Multi-megawatts, medium voltage, PWM voltage source sine-wave converter for industrial drive applications, in: Power Electronics & Variable Speed Drives Conference (PEVD'98), UK, London, 21–23 September, 1998.
[14] Y. Shakweh, E.A. Lewis, A. Gent, High-power drives for mining applications, in: Minmech 98, South Africa, September, 1998.
[15] A. Crane, T.J. McCoy, EMC design for a 19 MW PWM motor drive, in: IEEE Industry Applications Society Annual Meeting'99, Vol. 3, 1999, pp. 1590–1995.
[16] R. Stromquist, S. Gustafson, SUBSIS—World's First Separation and Injection System, ABB Review, 6/1998.
[17] B. Clegg, et al., The Application of Drives and Generator Technology to a Modern Container Ship, IEE, PEVD98, London, UK.
[18] N.J. Elliott, Novel application of a linear synchronous motor drive, in: IEE Colloquium on "Update on New Power Electronics Techniques", IEE, London, May 23, 1997.

Further Reading

[1] Y. Shakweh, Power devices for MV PWM VSI converters, Power Eng. J. (1999). IEE, UK.
[2] A.W. Richmond, A Practical Engineer's handbook, Industrial Electric Drives, Drives & Controls Publications, Kamtech Publishing Ltd, Croydon, Surrey, UK, 2015.
[3] Direct Torque Control, ABB Technical Guide No. 1.

30

Motor Drives

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30.1 Introduction

The widespread proliferation of power electronics and ancillary control circuits into motor control systems in the past several decades have led to a situation where motor drives, which process about two-thirds of the world's electric power into mechanical power, are on the threshold of processing all of this power via power electronics. The days of driving motors directly from the fixed ac or dc mains via mechanical adjustments are truly over. Table 30.1 indicates application areas where various types of power electronic converter-driven motor drives are routinely used.

The widespread incorporation of power, control, and signal electronics in motor drives has meant that processes can now be driven much more efficiently with a much greater degree of flexibility than previously possible. Of course, certain processes are more favorable to certain types of motors, because of the more favorable match between their characteristics. Historically, this situation was brought about by the demands of the industry. Increasingly, however, power electronic devices and control hardware are easily tailoring the rigid characteristics of the motor (when driven from a fixed dc or ac supply source) to the requirements of the load. Development of novel forms of machines and control techniques therefore has not abated, as recent trends would indicate.

It should be expected that just as power electronics equipment has tremendous variety, depending on the power level of the application, motors also come in many different types, depending on the requirements of application and power level. Often, the choice of a motor and its power electronic drive circuit for application is forced by these realities, and the application engineer therefore needs to have a good understanding of the application, the available motor types, and the suitable power electronic converter and its control techniques. Table 30.1 gives a rough guide of combinations of suitable motors and power electronic converters for a few typical applications.

For many years, the brushed dc motor had been the natural choice for applications requiring high dynamic performance. Drives of up to several hundred kilowatts have used this type of motor. In contrast, the induction motor was considered for low-performance, adjustable-speed applications at low and medium power levels. At very high power levels, the slip-ring induction motor or the synchronous motor drive was the natural choice. These boundaries are increasingly becoming blurred, especially at the lower power levels, especially for AC motor drives.

Another factor for motor drives was the consideration for servo performance. The ever-increasing demand for greater productivity or throughput and higher quality of most of the industrial products that we use in our everyday lives means that all aspects of dynamic response and accuracy of motor drives have to be increased. Issues of energy efficiency and harmonic proliferation into the supply grid are also increasingly affecting the choices for motor-drive circuitry.

A typical motor-drive system is expected to have some of the system blocks indicated in Fig. 30.1. The load may be a conveyor system, a traction system, the rolls of a mill drive, the cutting tool of a numerically controlled machine tool, the compressor of an air conditioner, a ship propulsion system, a control valve for a boiler, a robotic arm, and so on. The power electronic converter block may use diodes, metal oxide semiconductor field-effect transistors (MOSFETS), gate turnoff thyristors (GTOs), insulated gate bipolar transistors (IGBTs), or thyristors. The controllers may consist of several control loops, for regulating voltage, current, torque, flux, speed, position, tension, or other desirable conditions of the load. Each of these may have their limiting features purposely placed in order to protect the motor, the converter, or the load. The input

TABLE 30.1 Typical motor, converter, and application guides

Motor	Type of converter	Type of control	Applications
Brushed dc motor	Thyristor ac-dc converter	Phase control, with inner current loop	Process rolling mills, winders, locomotives, large cranes, extruders, and elevators
	GTO/IGBT/MOSFET chopper	Pulse-width modulator (PWM) control with inner current loop	Drives for transportation, machine tools, and office equipment
Induction motor (cage)	Back-back thyristor	Phase control	Pumps and compressors
	IGBT/GTO inverter/ cycloconverter	PWM *V-f* control	General-purpose industrial drive such as for cranes, pumps, fans, elevators, material transport and handling, extruders, and subway trains
	IGBT/GTO	Vector control	High-performance ac drives in transportation, motion control, and automation
Induction motor (slip ring)	Thyristor ac-dc converter	Phase control with dc-link current loop	Large pumps, fans, and cement kilns
Synchronous motor (excited)	Thyristor ac-dc converter	DC-link current loop	Large pumps, fans, blowers, compressors, and rolling mills
Synchronous motor (PM)	IGBT/MOSFET inverter	PWM current control	High-performance ac servo drives for office equipment, machine tools, automotive traction drives and motion control

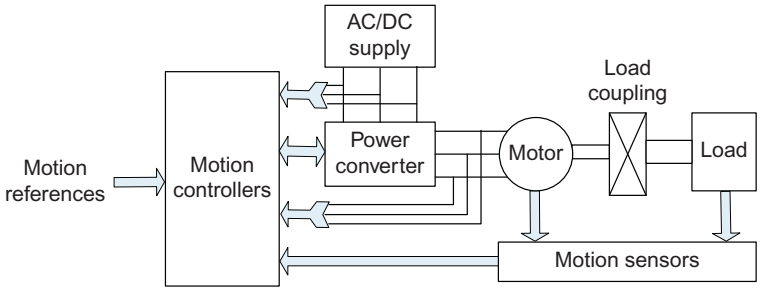


FIG. 30.1 Block diagram of a typical motor-drive system.

commands and the limiting values to these controllers would normally come from the supervisory control systems that produce the required references for a drive. This supervisory control system is normally more concerned with the overall operation of the process rather than the drive.

Consequently, a vast array of choices and technologies exist for a motor-drive application. Against this background, this chapter gives a brief description of the dominant forms of motor drives in current usage. The interested reader is expected to consult further reading material listed at the end of this chapter for more detailed coverage.

30.2 DC Motor Drives

30.2.1 Introduction

Direct-current motors are extensively used in variable-speed drives and position-control systems where good dynamic response and steady-state performance are required. Examples are in robotic drives, printers, machine tools, process rolling mills, paper and textile industries, and many others. Control of a dc motor, especially of the separately excited type, is very straightforward, mainly because of the incorporation of the commutator within the motor. The commutator brush allows the motor-developed torque to be proportional to the armature current if the field current is held constant. Classical control theories are then easily applied to the design of the torque and other motion loops of a drive system.

The mechanical commutator limits the maximum applicable voltage to about 1500 V and the maximum power capacity to a few hundred kilowatts. Series or parallel combinations of more than one motor are used, when dc motors are applied in applications that handle larger loads. The maximum armature current and its rate of change are also limited by the commutator.

30.2.2 DC Motor Representation and Characteristics

The dc motor has two separate sources of fluxes that interact to develop torque. These are the field and the armature circuits. Because of the commutator action, the developed torque is given by

$$T = Ki_f i_a \tag{30.1}$$

where i_f and i_a are the field and the armature currents, respectively, and K is a constant relating motor dimensions and parameters of the magnetic circuits.

The dynamic and the steady-state responses of the motor and load are given by

$$\text{Dynamic} \qquad \text{Steady} - \text{state}$$

$$v_a = R_a i_a + L_a \frac{di_a}{dt} + e \qquad V_a = R_a I_a + E \tag{30.2}$$

$$v_f = R_f i_f + L_f \frac{di_f}{dt} \qquad V_f = R_f I_f \tag{30.3}$$

$$e = Ki_f \omega \qquad E = KI_f \omega \tag{30.4}$$

$$T = J\frac{d\omega}{dt} + D\omega + T_L \qquad T = J\omega + T_L \tag{30.5}$$

where J, D and T_L are the moment of inertia, damping factor, and load torque, respectively, referred to the motor, and the subscripts a and f refer to the armature and field circuits, respectively. R, L, I, and E refer to resistance, inductance, current, and back emf of the motor in associated circuits referred by the subscripts.

Small servo-type dc motors normally have permanent-magnet (PM) excitation for the field, whereas larger size motors tend to have separate field supply, V_f, for excitation. The separately excited dc motors represented in Fig. 30.2A have fixed field excitation, and these motors are very easy to control via the armature current control, which are easily designed using classical linear control theory. Thyristor ac-dc converters with phase-angle control are popular for the larger size motors, whereas the duty-cycle-controlled pulse-width-modulated switching dc-dc converters are popular for servo-motor drives. The series-excited dc motor has its field circuit in series with the armature circuit as shown in Fig. 30.2B. Such a connection gives high torque at a low speed and low torque at a high

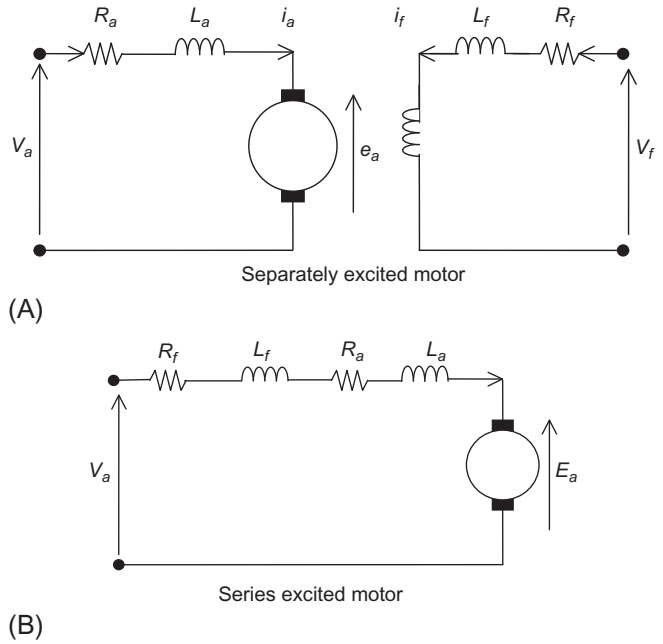


FIG. 30.2 Representation of the separately excited and series-excited motor circuits: (A) separately excited dc motor circuit and (B) series-excited dc motor circuit.

speed—a pseudo constant-power-like characteristic that may match traction-type loads well.

Torque-speed characteristics of the separately excited and series-excited dc motors are indicated in Fig. 30.3A and B, respectively. The speed of the separately excited dc motor drops with load, the net drop being about 5%–10% of the base speed at full load. The voltage drop across the armature resistance and the armature reaction are responsible for this. Operation of the motor above the base speed at which the armature voltage reaches for the rated field excitation is by means of field

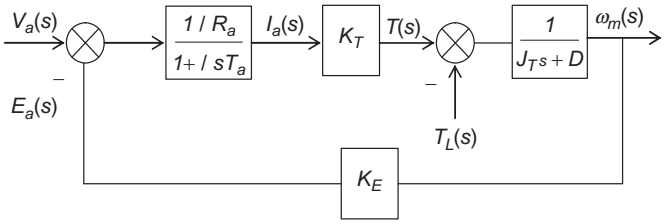


FIG. 30.4 Transfer characteristic block diagram of a separately excited motor.

weakening, whereby the field current is reduced in order to increase speed beyond the base speed. The armature voltage is now maintained at the rated value actively, by overriding the field control if required. Note that the range of field control is limited because of the magnetic nonlinearity of the field circuit and the problem of good commutation at weak field. Usually, the top speed is limited to about three times the base speed. Note also that field weakening results in reduced torque production per ampere of armature current. Depending on the type of load, the armature current, and speed change as dictated by Eqs. (30.1)–(30.5).

For the separately excited dc motor, assuming that the field excitation is held constant, the transfer characteristic between the shaft speed and the applied voltage to the armature can be expressed as indicated in the block diagram of Fig. 30.4. If we ignore the load torque T_L, the transfer characteristic is given by

$$\frac{\omega_m}{V_a} = \frac{K_T}{(sL_a + R_a)(Js + D) + K_E K_T} \tag{30.6}$$

the characteristic roots of which are given by

$$\left(s + \frac{1}{T_a}\right)\left(s + \frac{D}{J}\right) + \frac{1}{T_a T_m} = 0 \tag{30.7}$$

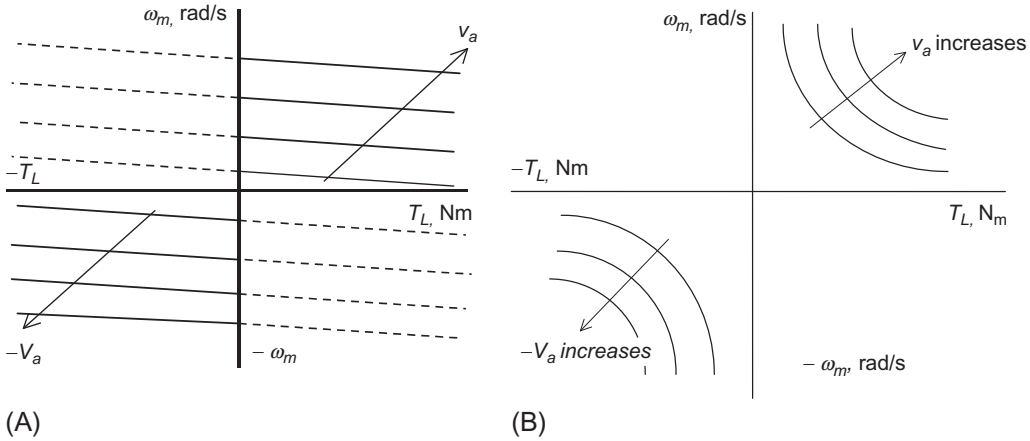


FIG. 30.3 Torque-speed characteristics of the (A) separately excited and (B) series-excited motors.

If we compare this with a standard second-order system, the undamped natural frequency and damping factor are given by

$$\omega_n = \sqrt{\frac{1}{T_a}\left(\frac{1}{T_m} + \frac{D}{J}\right)} \tag{30.8}$$

and

$$\sigma = \xi\omega_n = \frac{1}{2}\left[\frac{1}{T_a} + \frac{D}{J}\right] \tag{30.9}$$

where T_m = mechanical time constant = $\frac{R_a J}{K_E K_T}$ in which $K_E = Ki_f = K_T$ in SI units and T_a = electric time constant = $\frac{L_a}{R_a}$.

The speed response of the motor around an operating speed to the application of load torque on the shaft is given by

$$\frac{\Delta\omega_m}{\Delta T_L} = \frac{1 + sT_a}{(1 + sT_a)(Js + D) + \frac{K_E K_T}{R_a}} \tag{30.10}$$

30.2.3 Converters for DC Drives

Depending on the application requirements, the power converter for a dc motor may be chosen from a number of topologies. For example, a half-controlled thyristor converter or a single-quadrant pulse-width-modulated (PWM) switching converter may be adequate for a drive that does not require controlled deceleration with regenerative braking. On the other hand, a full four-quadrant thyristor or transistor converter for the armature circuit and a two-quadrant converter for the field circuit may be required for a high-performance drive with a wide speed range.

The frequency at which the power converter is switched, for example, 100 Hz for a single-phase thyristor bridge converter supplied from a 50 Hz ac source (or 300 Hz for a three-phase thyristor bridge converter), 20 kHz for a PWM MOSFET H-bridge converter, and so on, has a profound effect on the dynamics achievable with a motor drive. Low-power switching devices tend to have faster switching capability than high-power devices. This is convenient for low-power motors since these are normally required to be operated with high dynamic response and accuracy.

30.2.3.1 Thyristor Converter Drive

Consider the dc drive of Fig. 30.5 for which the armature supply voltage v_a to the motor is given by

$$v_a = \frac{2V_{\max}}{\pi}\cos\alpha \tag{30.11}$$

where V_{max} is the peak value of the line-line ac supply voltage to the converter and α is the firing angle. The dc output voltage v_a is controllable via the firing angle α, which in turn, is controlled by the control voltage e_c as the input to the firing control circuit (FCC). The FCC is synchronized with the mains ac supply and drives individual thyristors in the ac-dc converter according to the desired firing angle. Depending on the load and the speed of operation, the conduction of the current may become discontinuous as indicated in Fig. 30.6A. When this happens, the converter output voltage does not change with the control voltage as proportionately as with the continuous conduction. The motor speed now drops much more with the load as indicated by Fig. 30.6B. The consequent loss of gain of the converter may have to be avoided or compensated if good control over speed is desired.

The output voltage of the simple, two-pulse ac-dc converter of Fig. 30.5 is rich in ripples of frequency nf, where n is an even integer starting with two and f is the frequency of the ac supply. Such low-frequency ripple may derate the motor considerably. Converters with higher pulse number, such as the 6- or 12-pulse converters deliver much smoother output voltage and may be desirable for more demanding applications.

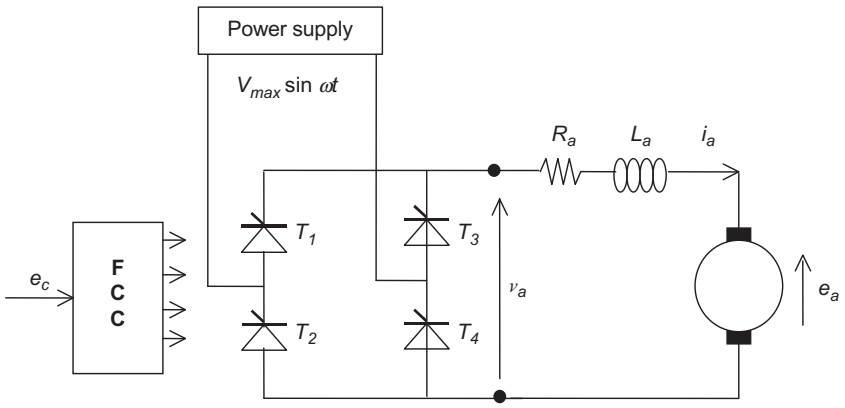


FIG. 30.5 A two-quadrant single-phase thyristor bridge converter drive.

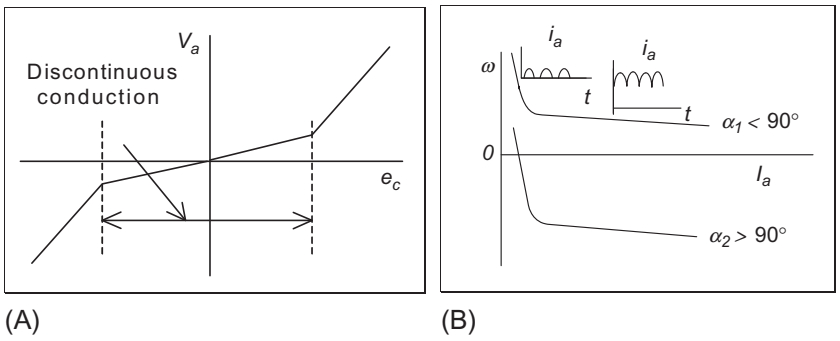


FIG. 30.6 Converter output voltage and motor torque-speed characteristic with discontinuous conduction.

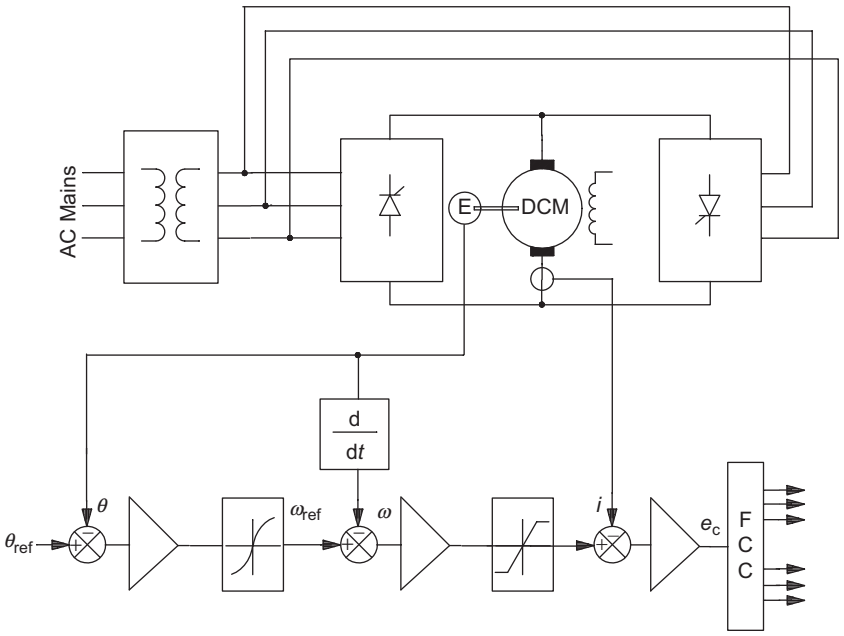


FIG. 30.7 Bidirectional speed- and position-control system with a back-to-back (dual) thyristor converter.

A high-performance dc drive for a rolling mill drive may consist of such converter circuits connected for bidirectional operation of the drive, as indicated in Fig. 30.7. The interfacing of the FCC to other motion-control loops, such as speed and position controllers, for the desired motion is also indicated

Two fully controlled bridge ac-dc converter circuits are used back-to-back from the same ac supply. One is for forward, and the other is for reverse driving of the motor. Since each is a two-quadrant converter, either may be used for regenerative braking of the motor. For this mode of operation, the braking converter, which operates in the inversion mode, sinks the motor current aided by the back emf of the motor. The energy of the overhauling decelerating motor now returns to the ac source.

It may be noted that the braking converter may be used to maintain the braking current at the maximum allowable level right down to zero speed. A complete acceleration-deceleration cycle of such a drive is indicated in Fig. 30.8. During braking, the firing angle is maintained at an appropriate value at all times so that the controlled and predictable deceleration takes place at all times.

The innermost control loop indicated in Fig. 30.7 is for torque, which translates to an armature current loop for a dc drive. Speed- and position-control loops are usually designed as hierarchical control loops. Operation of each loop is sufficiently decoupled from each other so that each stage can be designed in isolation and operated with its special limiting features.

30.2.3.2 PWM Switching Converter Drive

Pulse-width-modulated switching converters have traditionally been referred to as choppers in many traction and forklift-type drives. These are essentially PWM dc-dc converters operating from rectified dc or battery mains. These converters can also operate in one, two, or four quadrants, offering a few choices to meet application requirements. Servo-drive systems normally use the full four-quadrant converter of Fig. 30.9 that allows the bidirectional driving and regenerative braking capabilities.

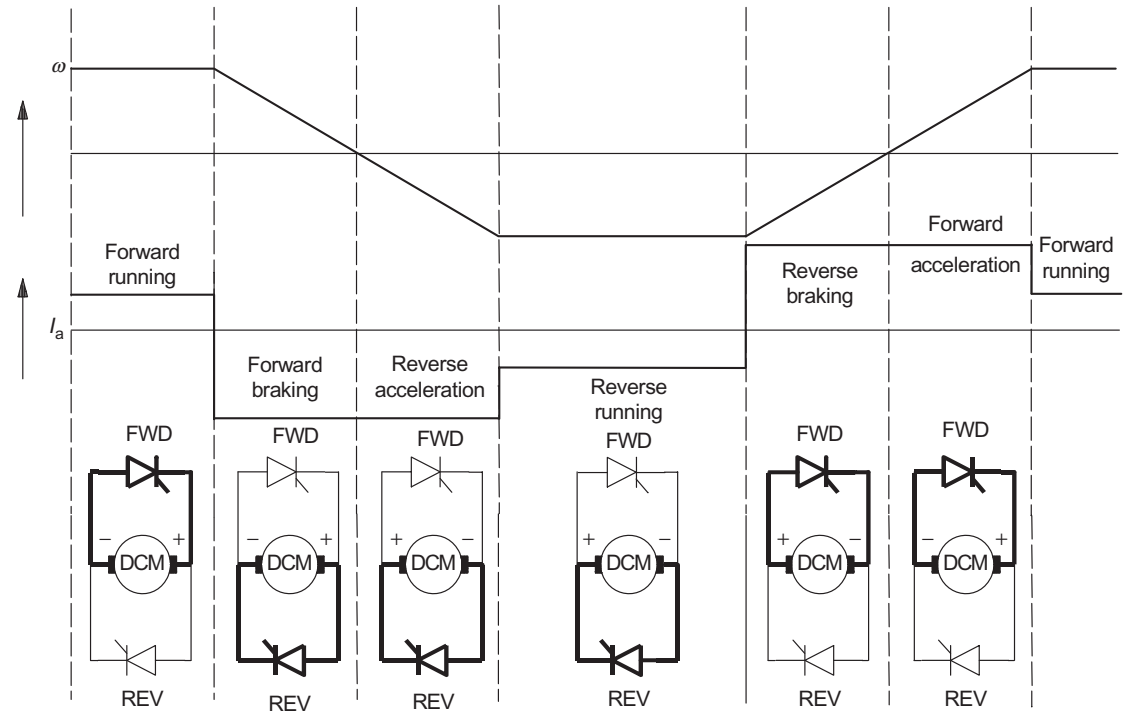


FIG. 30.8 Converter conduction and operating duty of a bidirectional drive.

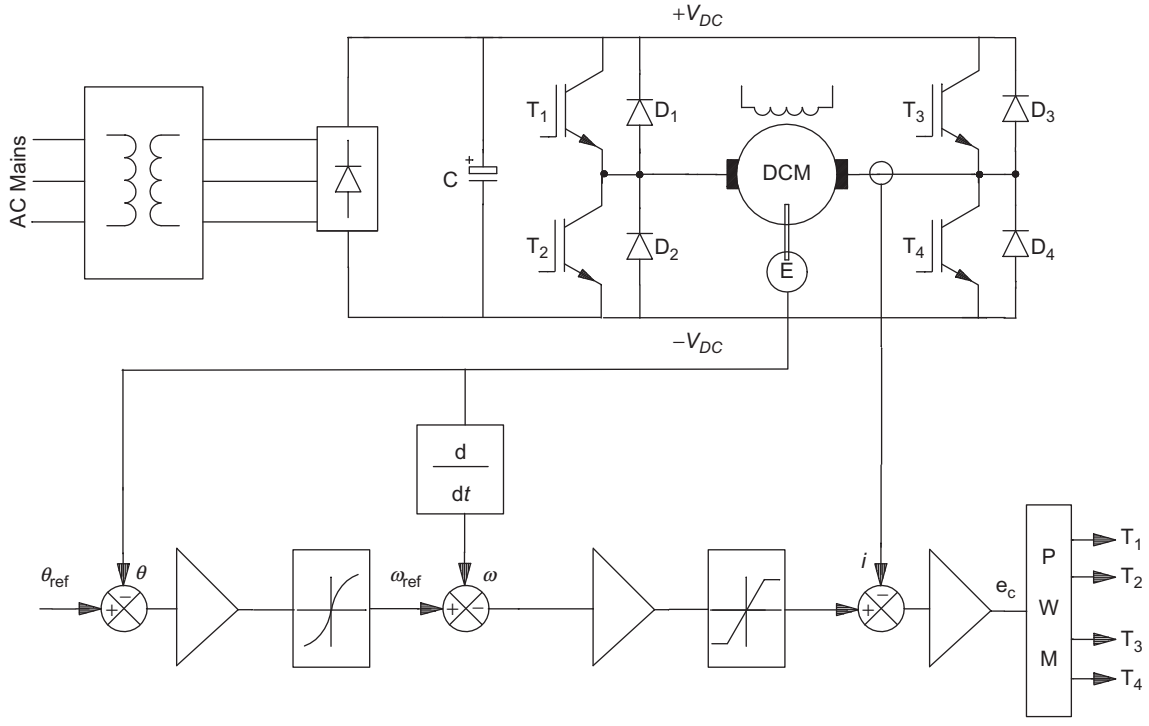


FIG. 30.9 Bidirectional speed- and position-control system with a PWM transistor bridge drive.

For forward driving, the transistors T_1 and T_4 and diode D_2 are used as a buck converter that supplies a variable voltage, v_a, to the armature given by

$$v_a = \delta V_{DC} \tag{30.12}$$

where V_{DC} is the dc supply voltage to the converter and δ is the duty cycle of the transistor T_1.

The duty cycle δ is defined as the duration of the ON-time of the modulating (switching transistor) as a fraction of the switching period. The switching frequency is normally dictated

by the application and the type of switching devices selected for the application.

During regenerative braking in the forward direction, transistors T_2 and diode D_4 are used as a boost converter that regulates the braking current through the motor by automatically adjusting the duty cycle of T_2. The energy of the overhauling motor now returns to the dc supply through the diode D_1, aided by the motor back emf and the dc supply. Again, note that the braking converter, comprising T_2 and D_1, may be used to maintain the regenerative braking current at the maximum allowable level right down to zero speed.

Fig. 30.10 shows a typical acceleration-deceleration cycle of such a drive under the action of the control loops indicated in Fig. 30.9.

Four-quadrant PWM converter drives such as that in Fig. 30.10 are widely used for motion-control equipment in the automation industry. Because of the significant development of power switching devices, switching frequencies of 10–20 kHz are easily attainable. At such frequencies, virtually, no derating of the motor is necessary.

In order to satisfy the requirements of a drive application, simpler versions of the drive circuits indicated in Figs. 30.7 and 30.9 may be used. For instance, for a unidirectional drive, half of the converter circuits indicated earlier may be used. Further simplification of the drive circuit is possible, if regenerative braking is not required.

30.2.4 Drive System Integration

A complete drive system has a torque controller (armature current controller for a dc drive) as its innermost loop, followed by a speed controller as indicated in Fig. 30.11.

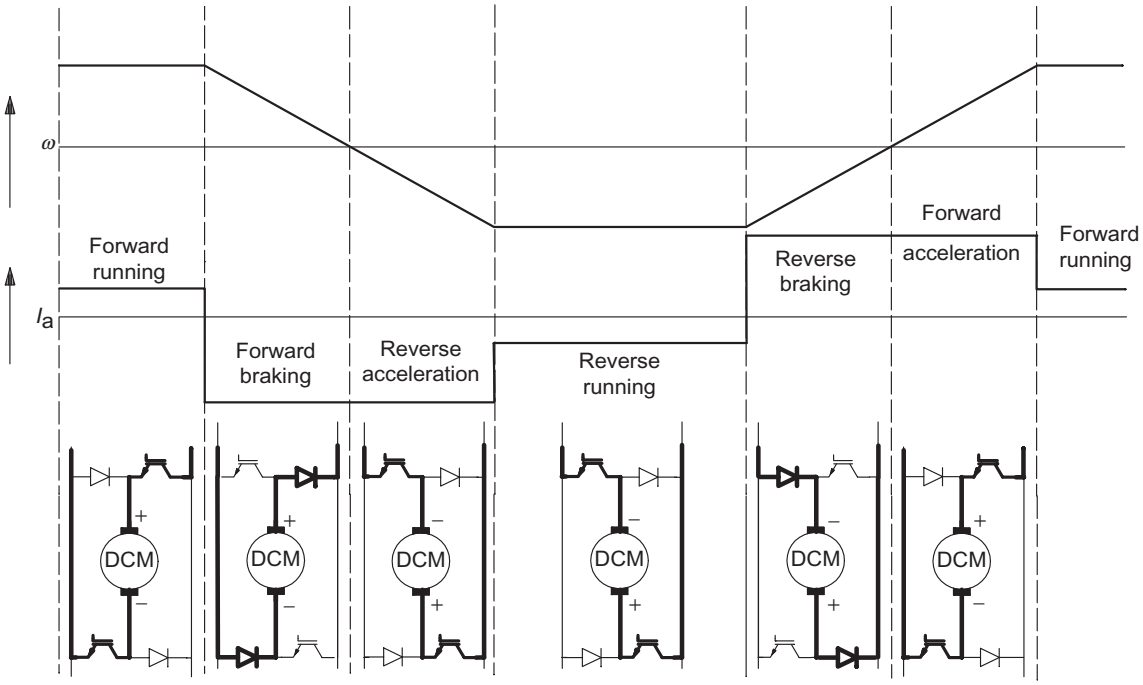


FIG. 30.10 Converter conduction and operating duty with a PWM bridge transistor drive.

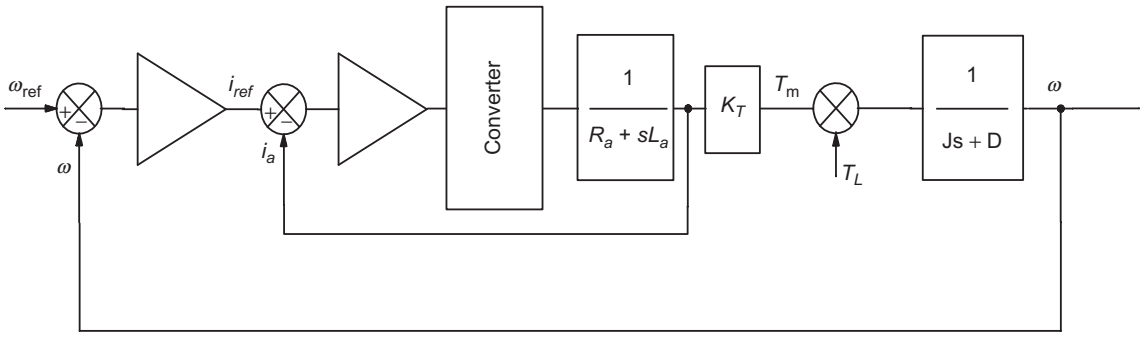


FIG. 30.11 Structure of a closed-loop speed-control system with a dc drive.

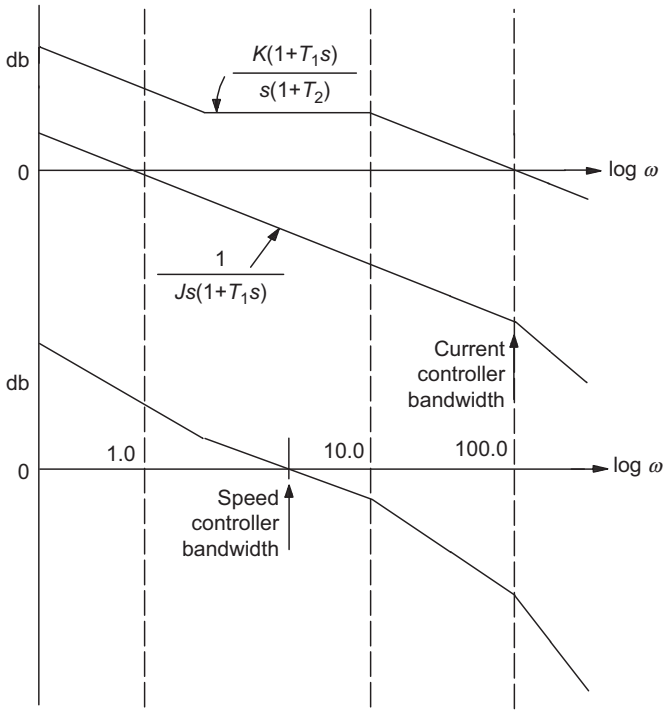


FIG. 30.12 Typical current and speed-control-loop designs for the system of Fig. 30.11.

The inner current loop is often regulated with a proportional-plus-integral (PI)-type controller of high gain. The rest of the inner loop consists of the converter, the motor armature, which is essentially an R-L circuit with the armature back emf as disturbance and the current sensor. The current sensor is typically an isolated circuit, such as a Hall sensor or a direct-current transformer (DCT). A well-designed torque (armature current) loop behaves essentially as a first-order lag system. Together with the mechanical inertia load, this loop can be indicated as the middle Bode plot of Fig. 30.12, in which $1/T_1$ represents the current-controlled system bandwidth. (Note that the damping factor D and the load torque T_L indicated in Fig. 30.11 have been neglected in this description for simplicity.) The current loop is normally designed by analyzing the block diagram of Fig. 30.11, the converter and the PI controller for the current loop using Bode analysis or other control system design tools.

The next step is usually the design of the speed controller. The 0 db intercept of $1/Js(1+T_is)$ is normally too low. Again, if a PI controller is selected for the speed loop, its Bode plot is superimposed on the current-controlled system as indicated in Fig. 30.12 to obtain the desired speed-control bandwidth.

30.2.5 Converter-DC Drive System Considerations

Several operational factors need to be considered in applying a dc drive. Some of the important ones are as follows:

1. The armature current may be rich in harmonics. This is particularly true for thyristor converters. The feedback of these current ripples into the FCC may cause overloading of individual switches and tripping. Adequate filtering is necessary to avoid such problems.
2. Since the converter is switched at regular intervals while the current controller operates continuously, current overshoot may occur because of the delay in the FCC. The current controller gains must be limited to limit this overshoot.
3. The switching frequency of the converter should be selected according to the desired motor-current ripple, supply input current harmonics, and the dynamic performance of the drive.
4. Ripple in the speed-sensor output limits the performance of the speed controller. Analog tachogenerator output is particularly noisy and defines the upper limit of the speed-control bandwidth. Digital speed sensors, such as encoders and resolvers, alleviate this limit significantly.

30.3 Induction Motor Drives

30.3.1 Introduction

The ac induction motor is by far the most widely used motor in the industry. Traditionally, it has been used in constant and variable-speed drive applications that do not cater for fast dynamic processes. Because of the recent development of several new control technologies, such as vector and direct torque controls, this situation is changing rapidly. The underlying reason for this is the fact that the cage induction motor is much cheaper and more rugged than its competitor, the dc motor, in such applications. This section starts with the induction motor drives that are based on the steady-state equivalent circuit of the motor, followed by vector-controlled drives that are based on its dynamic model.

30.3.2 Steady-State Representation

The traditional methods of variable-speed drives are based on the equivalent circuit representation of the motor referred to the stator, as shown in Fig. 30.13.

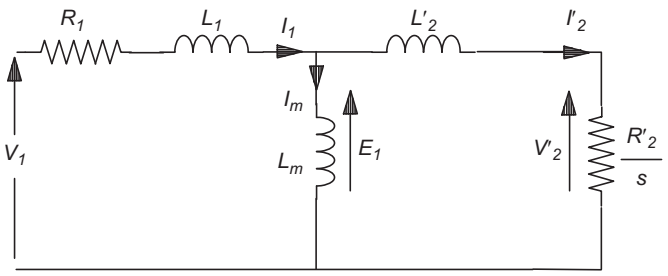


FIG. 30.13 Steady-state equivalent circuit of an induction motor.

From this representation, the following power relationships in terms of motor parameters and the rotor slip can be found:

$$\text{Power in the rotor circuit, } P_2 = 3I_2'^2\frac{R'_2}{s} = \frac{3sR'_2E_1^2}{R_2'^2+(s\omega_1L'_2)^2} \tag{30.13}$$

$$\text{Output power, } P_o = P_2 - 3I_2'^2R'_2 = (1-s)P_2 = \omega_0 T = \frac{(1-s)\omega_1}{p}T \tag{30.14}$$

where

$$\text{slip, } s = \frac{\omega_1-\omega_r}{\omega_1} = \frac{\omega_1 - p\omega_o}{\omega_1}$$
$$p = \text{number of polepairs}$$
$$\omega_o = \frac{2\pi N}{60}\text{ rad/s; } N \text{ is the rotor speed in rev/min,}$$
$$\omega_r = \text{rotor speed in electrical rad/s,} \tag{30.15}$$

and

$\omega_1 = 2\pi f_1$ rad/s (electrical), f_1 being the supply frequency.

$$\text{The developed torque, } T = \frac{P_2}{\omega_1/p}\text{Nm} \tag{30.16}$$

The slip frequency, sf_1, is the frequency of the rotor current and the air-gap voltage E_1 is given by

$$E_1 = \omega_1 L_m I_m = \omega_1 \lambda_m \tag{30.17}$$

where λ_m is the stator flux linkage due to the air-gap flux. If the stator impedance is negligible compared with E_1, which is true when f_1 is near the rated frequency f_o,

$$V_1 \approx E_1 = 2\pi f_1 \lambda_m \tag{30.18}$$

and

$$T = \frac{3p}{\omega_1}\frac{sR'_2V_1^2}{R_2'^2+(s\omega_1L'_2)^2} = \frac{3p}{\omega_1}\frac{sR'_2(2\pi f_1)^2\lambda_m^2}{R_2'^2+(s\omega_1L'_2)^2} \tag{30.19}$$

30.3.3 Characteristics and Methods of Control

The above analysis suggests several speed-control methods. The following are the widely used methods:

1. Stator voltage control
2. Slip power control
3. Variable-voltage, variable-frequency (*V-f*) control
4. Variable-current, variable-frequency (*I-f*) control

These methods are sometimes called *scalar controls* to distinguish them from *vector controls*, which are described in Section 30.3.4. The torque-speed characteristics of the motor differ significantly under different types of control, as will be evident in the following sections.

30.3.3.1 Stator Voltage Control

In this method of control, back-to-back thyristors are used to supply the motor with variable ac voltage, as indicated in the converter circuit diagram of Fig. 30.14A.

The analysis of Section 30.3.1 implies that the developed torque varies inversely as the square of the input root-mean-square (RMS) voltage to the motor, as indicated in Fig. 30.14B. This makes such a drive suitable for fan- and impeller-type loads for which the torque demand rises faster with speed. For other type of loads, the suitable speed range is very limited. Motors with high rotor resistance may offer an extended speed range. It should be noted that this type of drive with back-to-back thyristors with the firing-angle control suffers from poor power and harmonic distortion factors when operated at a low speed.

If unbalanced operation is acceptable, the thyristors in one or two supply lines to the motor may be bypassed. This offers the

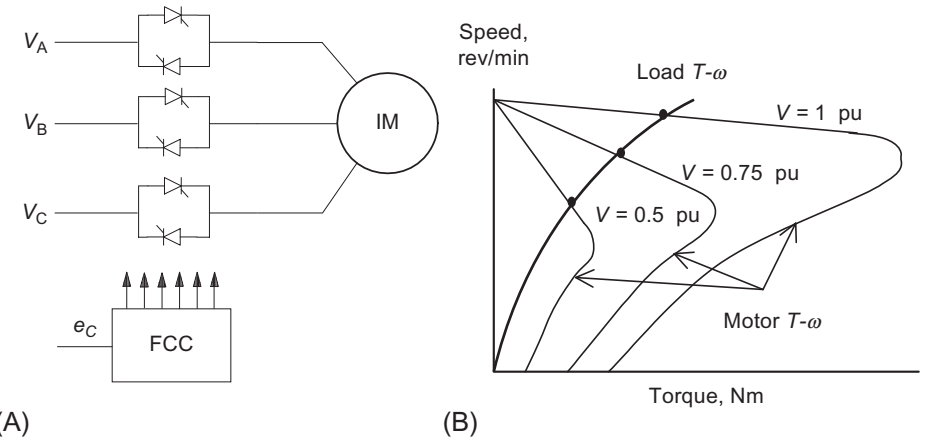


FIG. 30.14 (A) Stator voltage controller and (B) motor and load torque-speed characteristics under voltage control.

possibility of dynamic braking or plugging, desirable in some applications.

30.3.3.2 Slip Power Control

Variable-speed, three-phase, wound-rotor (or slip-ring) induction motor drives with slip power control may take several forms. In a passive scheme, the rotor power is rectified and dissipated in a liquid resistor or in a multitapped resistor that may be adjustable and forced cooled. In a more popular scheme, which is widely used in medium- to large-capacity pumping installations, the rectified rotor power is returned to the ac mains by a thyristor converter operating in a naturally commutated inversion mode. This static Scherbius scheme is indicated in Fig. 30.15. In this scheme, the rotor terminals are connected to a three-phase diode bridge that rectifies the rotor voltage. This rotor output is then inverted into mains frequency ac by a fully controlled thyristor converter operating from the same mains as the motor stator.

The converter in the rotor circuit handles only the rotor slip power, so that the cost of the power converter circuit can be much less than that of an equivalent inverter drive, albeit at the cost of the more expensive motor. The dc-link current, smoothed by a reactor, may be regulated by controlling the firing angle of the converter in order to maintain the developed torque at the level required by the load. The current controller (CC) and speed controller (SC) are also indicated in Fig. 30.15. The current controller output determines the converter firing angle α from the firing control circuit (FCC).

From the equivalent circuit of Fig. 30.13 and ignoring the stator impedance, the RMS voltage per phase in the rotor circuit is given by

$$V_R = \frac{V_s}{n}\frac{\omega_r}{\omega_s} = \frac{V_s}{n}\frac{s\omega_s}{\omega_s} = \frac{V_s s}{n} \tag{30.20}$$

where ω_s and ω_r are the angular frequencies of the voltages in the stator and rotor circuits, respectively, and n is the ratio of the equivalent stator to rotor turns. The dc-link voltage at the rectifier terminals of the rotor, v_d is given by

$$v_d = \frac{3\sqrt{6}V_R}{\pi}$$

Assuming that the transformer interposed between the inverter output and the ac supply has the same turns ratio n as the effective stator-to-rotor turns of the motor,

$$v_d = -\frac{3\sqrt{6}}{\pi}\frac{V_s}{n}\cos\alpha \tag{30.21}$$

The negative sign arises because the thyristor converter develops negative dc voltage in the inverter mode of operation. The dc-link inductor is mainly to ensure continuous current through the converter so that the expression (30.21) holds

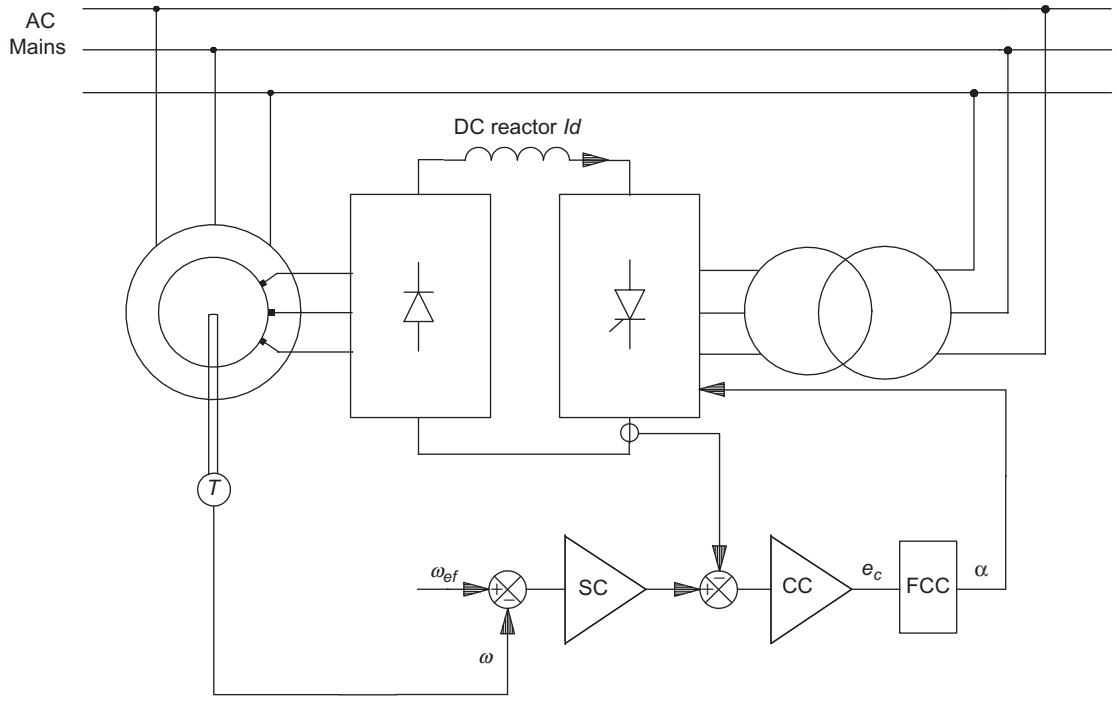


FIG. 30.15 The static Scherbius drive scheme of slip power control.

for all conditions of operation. Combining the preceding three equations gives

$$s\omega_s = -\omega_s \cos\alpha \text{ so that, } s = -n\cos\alpha$$

and the rotor speed

$$\omega_o = \frac{1}{p}(1-s)\omega_s = \frac{1}{p}\omega_s(1+n\cos\alpha) \text{ rad/s} \qquad (30.22)$$

Thus, the motor speed can be controlled by adjusting the firing angle α. By varying α between 180° and 90°, the speed of the motor can be varied from zero to full speed, respectively. For a motor with low rotor resistance and with the assumptions taken earlier, it can be shown that the developed torque of the motor is given by

$$T = 3p\frac{V_s}{\omega_s} i_d \approx 3p\lambda_m i_d \text{ Nm} \qquad (30.23)$$

where i_d is the dc-link current. Thus, the inner torque-control loop of a variable-speed drive using the Scherbius scheme normally employs a dc-link current loop as the innermost torque loop. Fig. 30.16 shows the transient responses of the dc-link, rotor, and stator currents of such a drive when the motor is accelerated between two speeds.

The drive is normally started with a short-time-rated liquid resistor, and the thyristor speed controller is started when the drive reaches a certain speed.

By replacing the diode rectifier of Fig. 30.16 with another thyristor bridge, power can be made to flow to and from the rotor circuit, allowing the motor to operate at higher than synchronous speed, as is used for grid-connected generator operation in wind power conversion. For very large drives, a cycloconverter may also be used in the rotor circuit with direct conversion of frequency between the ac supply and the rotor and driving the motor above and below synchronous speed.

30.3.3.3 Variable-Voltage, Variable-Frequency (V–f) Control

SPWM inverter drive

When an induction motor is driven from an ideal ac voltage source, its normal operating speed is less than 5% below the synchronous speed, which is determined by the ac source frequency and the number of motor poles. With a sinusoidally modulated (SPWM) inverter, indicated in Fig. 30.17, the supply frequency to the motor can be easily adjusted for variable speed. Eq. (30.18) implies that, if rated air-gap flux is to be maintained at its rated value at all speeds, the supply voltage V_1 to the motor should be varied in proportion to the frequency f_1, when the voltage drop across the stator resistance can considered to be negligible. The block diagram of Fig. 30.18A shows how the frequency f_1 and the output voltage V_1 of the SPWM inverter are proportionately adjusted with the speed reference. The speed reference signal is normally passed through a filter that only allows a gradual change in the frequency f_1. This type of control is widely referred to as the *V-f* inverter drive. Control of the stator input voltage V_1 as a function of the frequency f_1 is readily arranged within the inverter by modulating the switches $T_1 - T_6$. At a low speed, however, where the input voltage V_1 is low, most of the input voltage may drop across the stator impedance, leading to a reduction in air-gap flux and loss of torque.

Compensation for the stator resistance drop, as indicated in Fig. 30.18B, is often employed. However, if the motor becomes lightly loaded at a low speed, the air-gap flux may exceed the rated value, causing the motor to overheat.

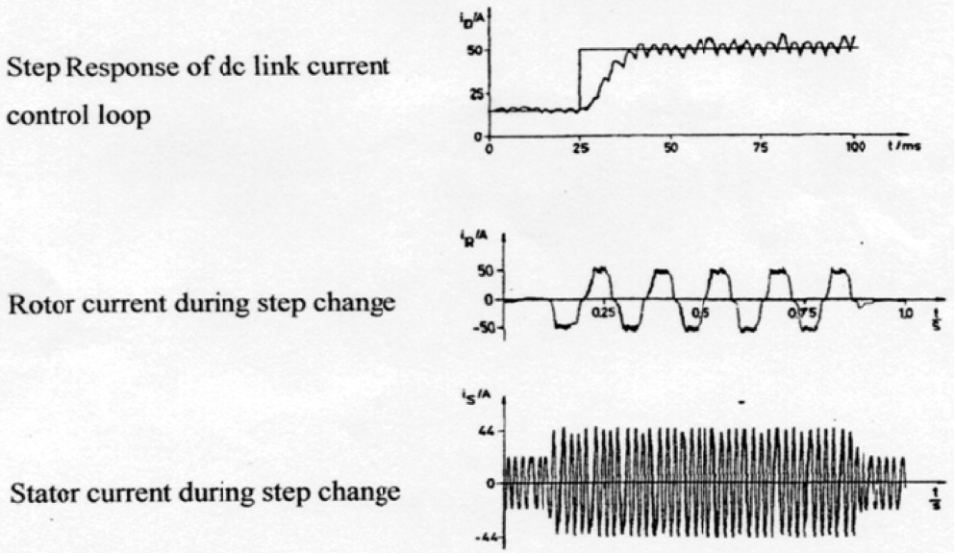


FIG. 30.16 Transient responses of a slip power-controlled drive under acceleration.

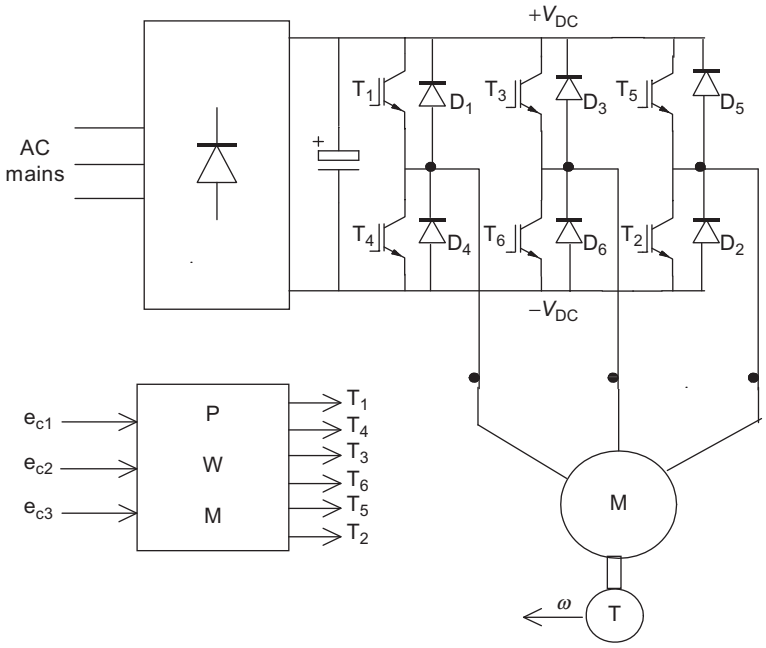


FIG. 30.17 *V-f* drive with SPWM inverter.

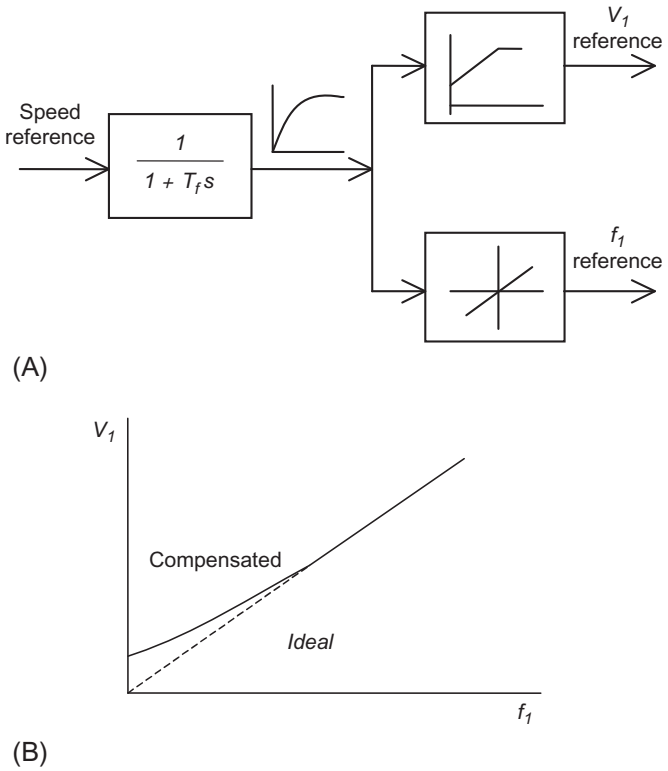


FIG. 30.18 (A) Input reference filter and voltage and frequency reference generation for the *V-f* inverter drive and (B) voltage compensation at a low speed.

From the equivalent circuit of Fig. 30.13 and neglecting the rotor leakage inductance, the developed torque T and the rotor current I'_2 are given by

$$I_2 = \frac{E_1 s\omega_1}{R'_2\omega_1} = \frac{\lambda_m}{R'_2} s\omega_1 A \tag{30.24}$$

and

$$T = 3p\frac{R'_2}{\omega_r} I'^2_2 Nm \tag{30.25}$$

where s ω_1 is the slip frequency, which is also the frequency of the voltages and currents in the rotor. Eq. (30.24) implies that by limiting the slip s, the rotor current can be limited, which in turn limits the developed torque Eq. (30.25). Consequently, a slip-limited drive is also a torque-limited drive. Note that this is true only in the steady state. A speed-control system with such a slip limiter is shown in Fig. 30.19. In this scheme, the motor speed is sensed and added to a limited speed error (or limited slip speed) to obtain the frequency (or speed reference for the V-f drive).

Many applications of the V-f controller, however, are open-loop schemes, in which any demanded variation in V_1 is passed through a ramp limiter (or filter) so that sudden changes in the slip speed ω_r are precluded, thereby allowing the motor to follow the change in the supply frequency without exceeding the rotor current and torque limits.

From the foregoing analyses, it is obvious that the V-f inverter drive essentially operates in all four quadrants, with rotor speed dropping slightly with the load and developing full torque at the same slip speed at all speeds. This assumes that the stator input voltage is properly compensated, so that the motor is operated with constant (or rated) air-gap flux at all speed. The motor can be operated above the base speed by keeping the input voltage V_1 constant, while increasing the stator frequency above base frequency in order to run the motor at speeds higher than the base speed. The air-gap flux and hence the maximum developed torque now fall with speed, leading to constant-power-type characteristic. Fig. 30.20 depicts the $T-\omega$ characteristics of such a voltage- and frequency-controlled drive for various operating frequencies. In this figure, the $T-\omega$ characteristic for base speed has been drawn in full, indicating the maximum developed torque T_{max} and the rated torque. Below base speed, the V_1-f_1 ratio is maintained to keep the air-gap flux constant. Above base speed, V_1 is kept constant, while f_1 increases with speed, thus weakening the air-gap flux. Forward driving in quadrant 1 takes place with the inverter output voltage sequence of $a-b-c$, whereas reverse driving in quadrant 3 takes place with the sequence $a-b-c$. Regenerative braking while forward driving takes place by adjusting the input frequency f_1 in such a way that

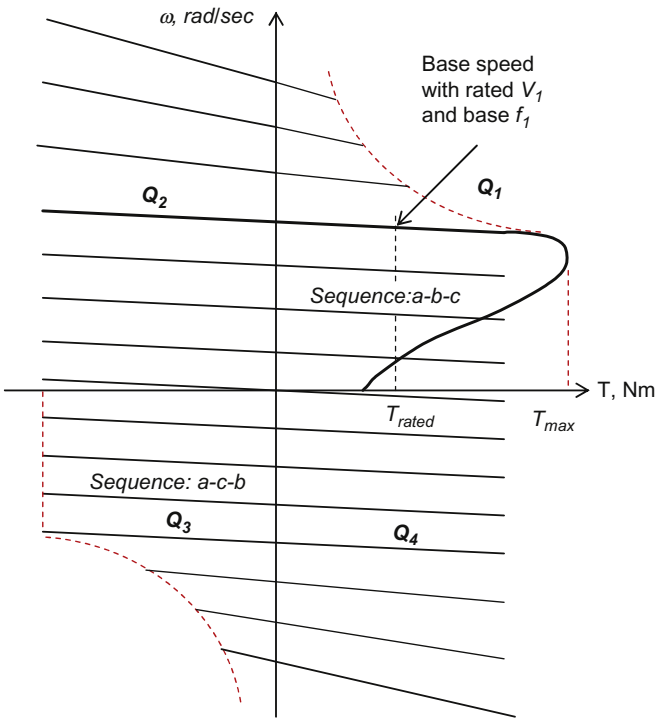


FIG. 30.20 Typical $T-\omega$ characteristics of V-f drive with the input frequency f_1 and voltage V_1 below and above base speed.

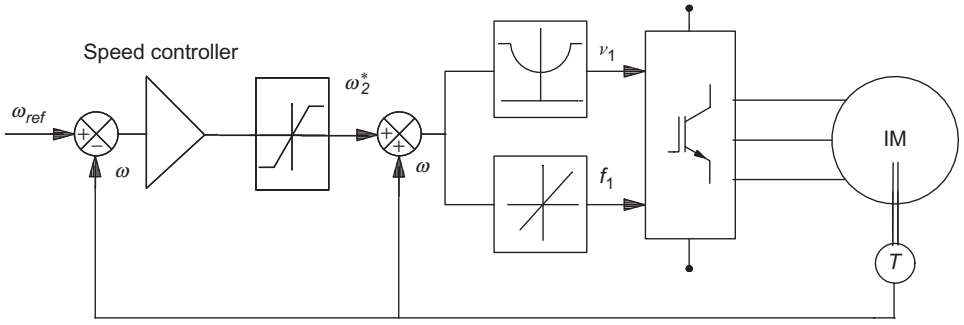


FIG. 30.19 Closed-loop speed controller with an inner slip loop.

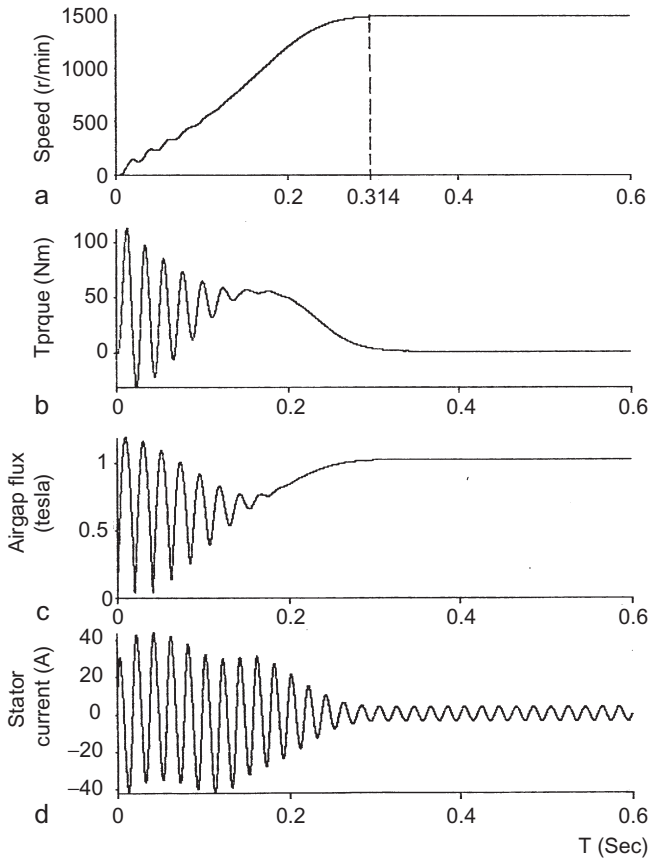


FIG. 30.21 Transient response of torque, speed, current, and air-gap flux during acceleration from standstill using a *V-f* inverter drive.

the motor operates in quadrant 2 (quadrant 4 for reverse braking) with the desired braking characteristic.

Note that the characteristics in Fig. 30.20 are based on the steady-state equivalent circuit model of the motor. Such a drive suffers from the poor torque response during transient operation because of time-dependent interactions between the stator and rotor fluxes. Fig. 30.21 indicates the machine air-gap flux during acceleration with *V-f* control obtained from a dynamic model. Clearly, the air-gap flux does not remain constant during the dynamic operation.

Cycloconverter drive

For large-capacity induction motor drives, the variable-frequency supply at variable voltage is effectively obtained from a cycloconverter in which a back-to-back thyristor converter pairs are used, one for each phase of the motor, as indicated in Fig. 30.22. Each thyristor block in this figure represents a fully controlled thyristor ac-dc converter. The maximum output frequency of such a converter can be as high as about 40% of the supply frequency. In view of the large number of thyristor switches required, cycloconverter drives are suitable for large-capacity but low-speed applications.

30.3.3.4 Variable Current–Variable Frequency (*I–f*) Control

In this scheme, medium- to large-capacity induction motors are driven from a variable but stiff current supply that may be obtained from a thyristor converter and a dc-link inductor as indicated in Fig. 30.23. The frequency of the current supply to the motor is adjusted by a thyristor converter with auxiliary diodes and capacitors. The diodes in each inverter leg and the capacitors across them are needed for turning off the thyristors when current is to be commutated from one to the next in sequence. The motor-current waveforms are normally six-step, or quasi-square, as indicated in Fig. 30.24. The switching states of the inverter thyristors are also indicated in this figure. The motor voltage waveforms are determined by the load. These waveforms are more nearly sinusoidal than the current waveforms.

The thyristor converter supplying the quasi-square current waveforms to the motor has firing-angle control, in order to regulate the dc-link current to the inverter. The dynamics of the dc-link current control is such that this current may be considered to be constant during the time the inverter switches commutate the dc-link current from one switch to the next.

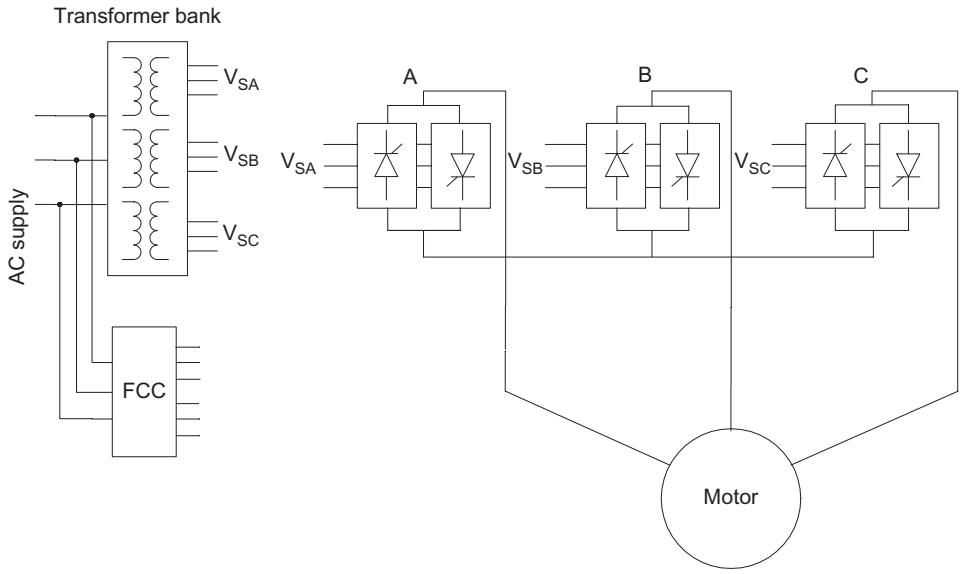


FIG. 30.22 *V-f* drive with cycloconverter drive.

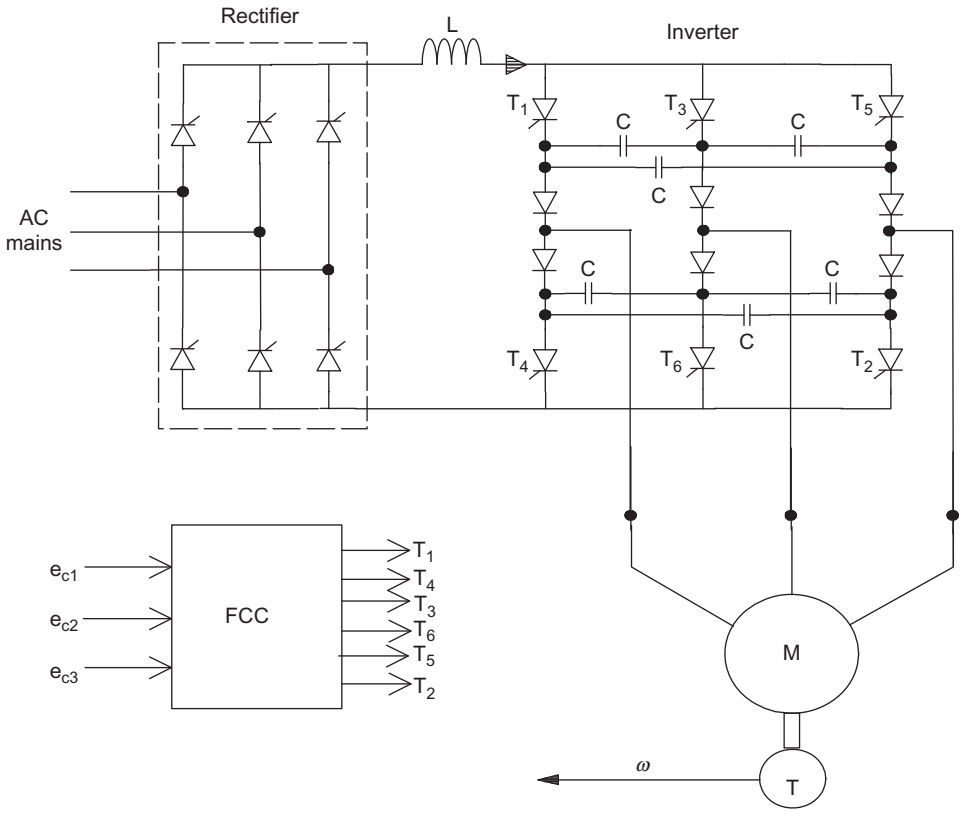


FIG. 30.23 DC-link current-source thyristor inverter drive.

Such a current-source drive offers four-quadrant operation, with independent control of the dc-link current and output frequency. One drawback is that the motor voltage waveforms have voltage spikes due to commutation.

From the analysis of Section 30.3.2, if the higher order harmonics of the current waveforms in Fig. 30.24 are neglected and it is assumed that the motor voltage and current waveforms are sinusoidal, the magnetizing current I_m in Fig. 30.13 can be kept constant (for constant air-gap flux operation) if the RMS value of the stator supply current I_1 is defined according to Eq. (30.26). This relationship is also shown in graphic form in Fig. 30.25.

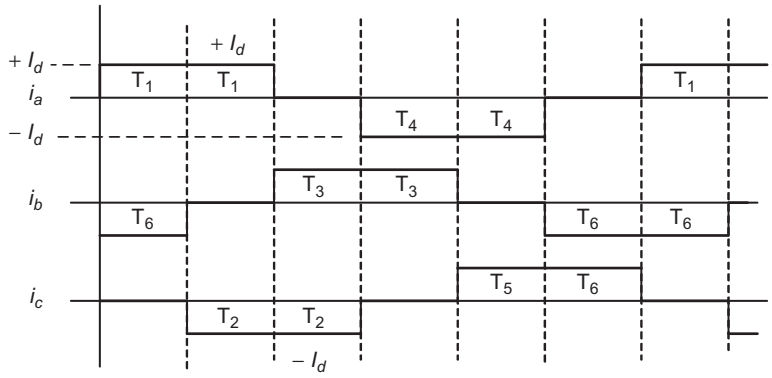


FIG. 30.24 Motor-current waveforms and the thyristor switching states for a current-source drive.

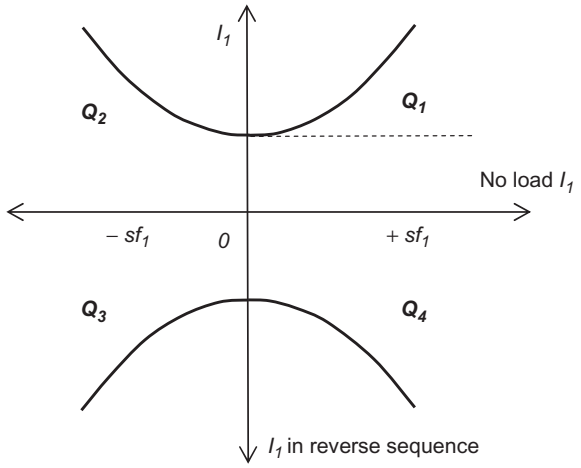


FIG. 30.25 Stator current versus rotor (slip) frequency for constant air-gap flux operation.

$$I_m = I_1 \left[\frac{R_2'^2 + \left(2\pi f_1 s L_2'\right)^2}{R_2'^2 + 2\pi f_1 \left(L_2' + L_m\right)^2} \right]^{1/2} = \text{constant} \qquad (30.26)$$

The control scheme for variable-speed operation with a current-source drive is indicated in the block diagram of Fig. 30.26. The speed reference defines the stator current reference according to Eq. (30.26), and the frequency reference is obtained by adding the rotor frequency to the actual speed of the motor. The inverter drive may consist of the thyristor current source and the inverter of Fig. 30.23 or a diode rectifier supplied SPWM transistor inverter of Fig. 30.17 with independent current regulators, one for each phase.

The dynamic performance of such current-controlled induction motor drives is not very satisfactory, just as for the voltage-source inverters. Furthermore, the current-source inverter drive cannot normally be operated open loop, like the *V-f* inverter drive. For high dynamic performance, vector-controlled drives are becoming popular.

30.3.4 Vector Controls

The foregoing scalar control methods are only suitable for adjustable-speed applications in which the load speed or position is not controlled like in a servo system. Instantaneous frequency control with a view to control motor speed or position cannot be defined, and therefore, instantaneous torque control cannot be addressed by scalar control methods. Vector control technique allows a squirrel-cage induction motor to be driven with high dynamic performance, comparable with that of a dc motor. In vector control, machine dynamic model rather than steady-state model (on which scalar controllers are based on) is used to design the controller. For this, the controller needs to know the rotor speed (in the indirect method) or the air-gap flux vector (in the direct method) accurately, using sensors.

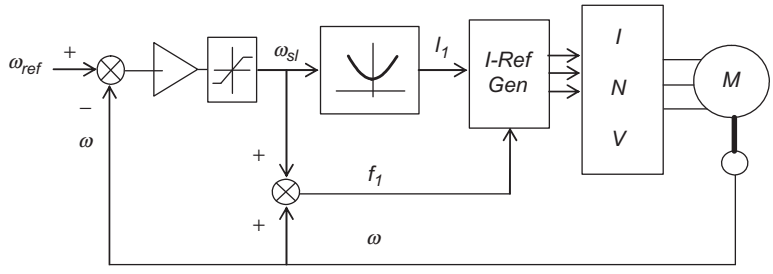


FIG. 30.26 Variable-current/variable-frequency inverter drive scheme.

The latter method is not practical because of the requirement of attaching air-gap flux sensors. The indirect method, which is being widely accepted in recent years, requires the controller to be matched with the motor being driven. This is because the controller also needs to know some rotor parameter(s), which may vary according to the conditions of operation, continuously.

30.3.4.1 Basic Principles

The methods of vector control are based on the dynamic equivalent circuit of the induction motor. There are at least three fluxes (rotor, air gap, and stator) and three currents or mmfs (stator, rotor, and magnetizing) in an induction motor. For high dynamic response, interactions among current, fluxes, and speed, must be taken into account in determining appropriate control strategies. These interactions are understood only via the dynamic model of the motor.

All fluxes rotate at synchronous speed. The three-phase currents create mmfs (stator and rotor) that also rotate at synchronous speed. Vector control aligns axes of an mmf and a flux orthogonally at all times. It is easier to align the stator current mmf orthogonally to the rotor flux.

Any three-phase sinusoidal set of quantities in the stator can be transformed to an orthogonal reference frame by

$$\begin{bmatrix} f_{\alpha s} \\ f_{\beta s} \\ f_o \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta - \frac{4\pi}{3}\right) \\ \sin\theta & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta - \frac{4\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} f_{as} \\ f_{bs} \\ f_{cs} \end{bmatrix} \tag{30.27}$$

where θ is the angle of the orthogonal set $\alpha-\beta-0$ with respect to any arbitrary reference. If the $\alpha-\beta-0$ axes are stationary and the α-axis is aligned with the stator α-axis, then $\theta = 0$ at all times. Thus,

$$\begin{bmatrix} f_{\alpha s} \\ f_{\beta s} \\ f_{os} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} f_{as} \\ f_{bs} \\ f_{cs} \end{bmatrix} \tag{30.28}$$

If the orthogonal set of reference rotates at the synchronous speed ω_1, its angular position at any instant is given by

$$\theta = \int_0^t \omega_1 t + \theta_o \tag{30.29}$$

The orthogonal set is then referred to as $d-q-0$ axes. The three-phase rotor variables, transformed to the synchronously rotating frame, are

$$\begin{bmatrix} f_{dr} \\ f_{qr} \\ f_o \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\omega_e-\omega_r)t & \cos\left((\omega_e-\omega_r)t - \frac{2\pi}{3}\right) & \cos\left((\omega_e-\omega_r)t - \frac{4\pi}{3}\right) \\ \sin(\omega_e-\omega_r)t & \sin\left((\omega_e-\omega_r)t - \frac{2\pi}{3}\right) & \sin\left((\omega_e-\omega_r)t - \frac{4\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \times \begin{bmatrix} f_{ar} \\ f_{br} \\ f_{cr} \end{bmatrix} \tag{30.30}$$

It should be noted that the difference $\omega_e - \omega_r$ is the relative speed between the synchronously rotating reference frame and the frame attached to the rotor. This difference is also the slip frequency, ω_{sl}, which is the frequency of the rotor variables. By applying these transformations, voltage equations of the motor in the synchronously rotating frame reduce to

$$\begin{bmatrix} v_{qs} \\ v_{ds} \\ v_{qr} \\ v_{dr} \end{bmatrix} = \begin{bmatrix} R_s + pL_s & \omega_e L_s & pL_m & \omega_e L_m \\ -\omega_e L_s & R_s + pL_s & -\omega_e L_m & pL_m \\ pL_m & (\omega_e-\omega_r)L_m & R_r + pL_r & (\omega_e-\omega_r)L_r \\ -(\omega_e-\omega_r) & pL_m & -(\omega_e-\omega_r)L_r & R_r + pL_r \end{bmatrix} \times \begin{bmatrix} i_{qs} \\ i_{ds} \\ i_{qr} \\ i_{dr} \end{bmatrix} \tag{30.31}$$

where the speed of the reference frame, ω_e, is equal to ω_1 and $L_s = L_{ls} + L_m$, $L_r = L_{lr} + L_m$.

Subscripts l and m stand for leakage and magnetizing, respectively, and p represents the differential operator d/dt, not the number of pole pairs. The equivalent circuits of the motor in this reference frame are indicated in Fig. 30.27A and B.

The stator flux linkage equations are

$$\lambda_{qs} = L_{ls} i_{qs} + L_m\left(i_{qs} + i_{qr}\right) = L_s i_{qs} + L_m i_{qr} \tag{30.32}$$

$$\lambda_{ds} = L_{ls} i_{ds} + L_m\left(i_{ds} + i_{dr}\right) = L_s i_{ds} + L_m i_{dr} \tag{30.33}$$

$$\hat{\lambda}_s = \sqrt{\left(\lambda_{qs}^2 + \lambda_{ds}^2\right)} \tag{30.34}$$

The rotor flux linkages are given by

$$\lambda_{qr} = L_{lr} i_{qr} + L_m\left(i_{qs} + i_{qr}\right) = L_r i_{qr} + L_m i_{qs} \tag{30.35}$$

$$\lambda_{dr} = L_{lr} i_{dr} + L_m\left(i_{ds} + i_{dr}\right) = L_r i_{dr} + L_m i_{ds} \tag{30.36}$$

$$\hat{\lambda}_r = \sqrt{\left(\lambda_{qr}^2 + \lambda_{dr}^2\right)} \tag{30.37}$$

The air-gap flux linkages are given by

$$\lambda_{mq} = L_m\left(i_{qs} + i_{qr}\right) \tag{30.38}$$

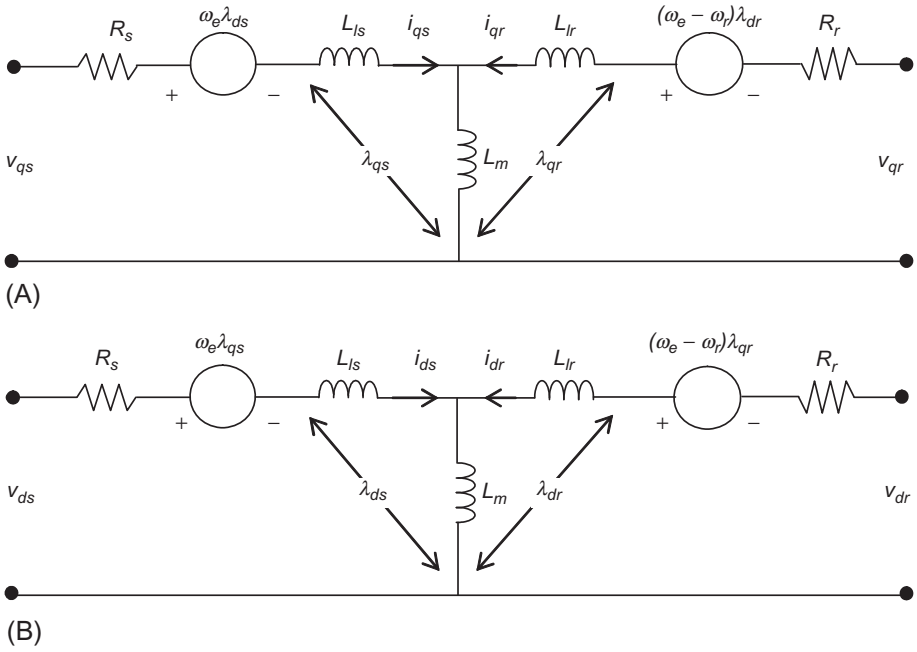


FIG. 30.27 Motor dynamic equivalent circuits in the synchronously rotating: (A) q- and (B) d-axes.

$$\lambda_{md} = L_m(i_{ds} + i_{dr}) \tag{30.39}$$

$$\hat{\lambda}_m = \sqrt{\left(\lambda_{mqs}^2 + \lambda_{mds}^2\right)} \tag{30.40}$$

The torque developed by the motor is given by

$$T = \frac{3p}{2}\left[\lambda_{ds} i_{qs} - \lambda_{qs} i_{ds}\right] \tag{30.41}$$

where p is the number of pole pairs.

From Eq. (30.31), the rotor voltage equations are

$$v_{qr} = 0 = L_m \frac{di_{qs}}{dt} + (\omega_e - \omega_r) L_m i_{ds} + \left(R_r i_r + L_r \frac{di_{qr}}{dt}\right) + (\omega_e - \omega_r) L_r i_d r \tag{30.42}$$

$$v_{dr} = 0 = L_m \frac{di_{ds}}{dt} + (\omega_e - \omega_r) L_m i_{qs} + \left(R_r i_r + L_r \frac{di_{dr}}{dt}\right) + (\omega_e - \omega_r) L_r i_{qr} \tag{30.43}$$

Using Eqs. (30.35) and (30.36),

$$\frac{d\lambda_{qr}}{dt} + R_r i_{qr} + (\omega_e - \omega_r)\lambda_{dr} = 0 \tag{30.44}$$

$$\text{and} \quad \frac{d\lambda_{dr}}{dt} + R_r i_{dr} + (\omega_e - \omega_r)\lambda_{qr} = 0 \tag{30.45}$$

Also from Eqs. (30.35) and (30.36),

$$i_{qr} = \frac{1}{L_r}\lambda_{qr} - \frac{L_m}{L_r} i_{qs} \tag{30.46}$$

$$i_{dr} = \frac{1}{L_r}\lambda_{dr} - \frac{L_m}{L_r} i_{ds} \tag{30.47}$$

The rotor currents i_{qr} and i_{dr} can be eliminated from Eqs. (30.44) and (30.45) by using Eqs. (30.46) and (30.47). Thus,

$$\frac{d\lambda_{qr}}{dt} + \frac{L_r}{R_r}\lambda_{qr} - \frac{L_m}{L_r} R_r i_{qs} + (\omega_e - \omega_r)\lambda_{dr} = 0 \tag{30.48}$$

$$\frac{d\lambda_{dr}}{dt} + \frac{R_r}{L_r}\lambda_{dr} - \frac{L_m}{L_r} R_r i_{ds} + (\omega_e - \omega_r)\lambda_{qr} = 0 \tag{30.49}$$

The elimination of transients in rotor flux and the coupling between the two axes occurs when

$$\lambda_{qr} = 0 \quad \text{and} \quad \hat{\lambda}_r = \lambda_{dr} \tag{30.50}$$

The rotor flux should also remain constant so that

$$\frac{d\lambda_{dr}}{dt} = 0 = \frac{d\lambda_{qr}}{dt} \tag{30.51}$$

From Eq. (30.48) to Eq. (30.51),

$$\omega_e - \omega_r = \omega_{sl} = \frac{L_m R_r}{\hat{\lambda}_r L_r} i_{qs} \tag{30.52}$$

$$\text{and} \quad \frac{L_r}{R_r}\frac{d\hat{\lambda}_r}{dt} + \hat{\lambda}_r = L_m i_{ds} \tag{30.53}$$

Substituting the expressions for i_{qr} and i_{dr} into Eqs. (30.35) and (30.36),

$$\lambda_{qs} = \left(L_s - \frac{L_m^2}{L_r}\right) i_{qs} + \frac{L_m}{L_r}\lambda_{qr} \tag{30.54}$$

$$\lambda_{ds} = \left(L_s - \frac{L_m^2}{L_r}\right) i_{ds} + \frac{L_m}{L_r}\lambda_{dr} \tag{30.55}$$

Substituting λ_{qs} and λ_{ds} from Eqs. (30.54) and (30.55) into the torque equation of Eq. (30.41),

$$T = \frac{3P}{2}\frac{L_m}{L_r}\left(\lambda_{dr} i_{qs} - \lambda_{qr} i_{ds}\right) = \frac{3P}{2}\frac{L_m}{L_r}\hat{\lambda}_r i_{qs} \tag{30.56}$$

It is clear from Eq. (30.53) that the rotor flux $\hat{\lambda}_{dr}$ is determined by i_{ds}, subject to a time delay T_r, which is the rotor time constant (L_r/R_r). The current i_{qs}, according to Eq. (30.56), controls the developed torque T without delay. Currents i_{ds} and i_{qs} are orthogonal to each other and are called the flux- and torque-producing currents, respectively. This correspondence between the flux- and torque-producing currents is subject to maintaining the conditions in Eqs. (30.50) and (30.51). Normally, i_{ds} would remain fixed for operation up to the base speed. Thereafter, it is reduced in order to weaken the rotor flux so that the motor may be driven with a constant-power-like characteristic.

Based on how the rotor flux is detected and regulated, two methods of control are available. One is the more popular indirect rotor-flux-oriented control (IFOC) method, and the other is the direct vector control method; both are described hereafter.

30.3.4.2 Indirect Rotor Flux Oriented (IFOC) Vector Control

In the indirect scheme, the relationship between the slip frequency and current i_{qs} given by Eq. (30.52) is used to relate the compensated speed error $\omega_1 - \omega_r$ to i_{qs}. The i_{qs}, in turn, is used to develop to the demanded torque T^* according to the Eq. (30.56). The rotor flux is maintained at the base value for operation below speed, and it may be reduced to a lower value for field weakening above base speed. The orthogonal relationship between the torque-producing stator current i_{qs} and the flux-producing stator current i_{ds} is maintained at all times by generating the stator current references in the synchronously rotating dq reference frame, using sine and cosine functions of angle θ_1. This angle is obtained as indicated in Fig. 30.28.

The compensated speed error produces the current reference i_{qs}^* according to Eq. (30.56). The current reference i_{qs}^* also gives the slip speed ω_{sl} according to Eq. (30.53). The slip speed ω_{sl} is added to the rotor speed ω, to obtain the stator frequency ω_1. This frequency is integrated with respect to time to produce the required angle θ_1 of the stator mmf relative to the rotor flux vector. This angle is used to transform the stator currents to the dq reference frame. Two independent current controllers are used to regulate the i_q and i_d currents to their reference values. The compensated i_q and i_d errors are then inverse transformed into the stator $a-b-c$ reference frame for obtaining switching signals for the inverter via PWM or hysteresis comparators.

It is clear that this scheme uses a feedforward scheme, or a machine model, in which the current reference for i_{qs} is also

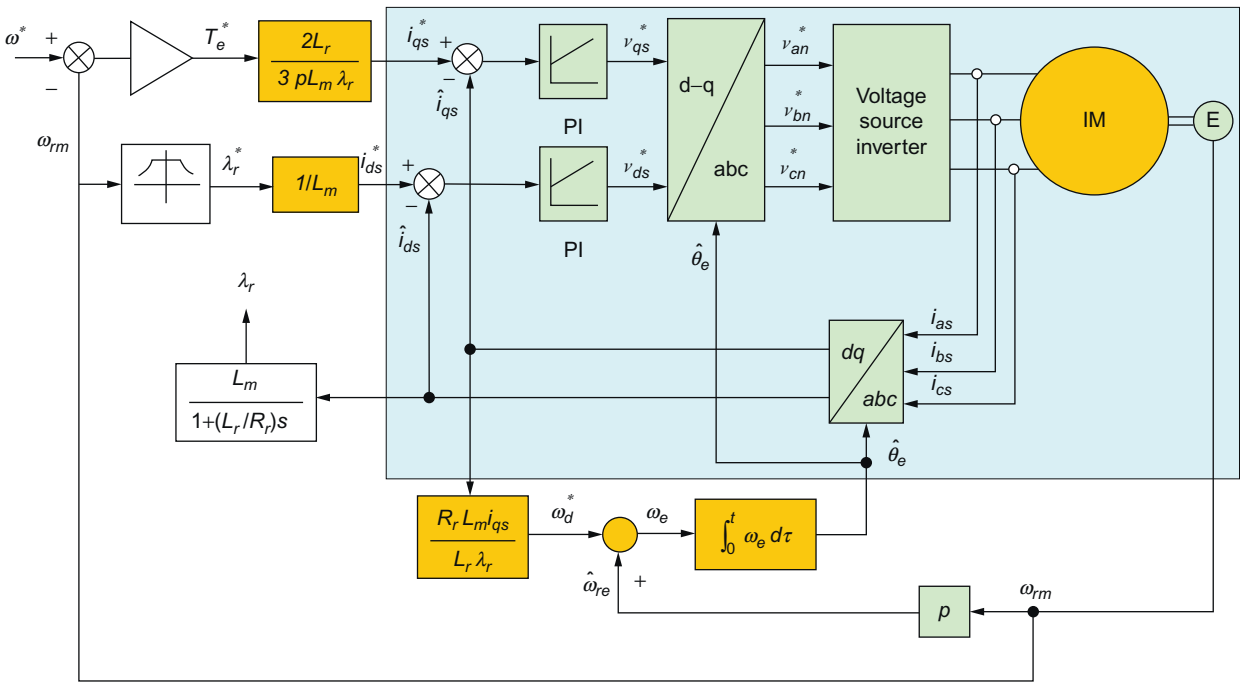


FIG. 30.28 Indirect rotor flux oriented vector control scheme.

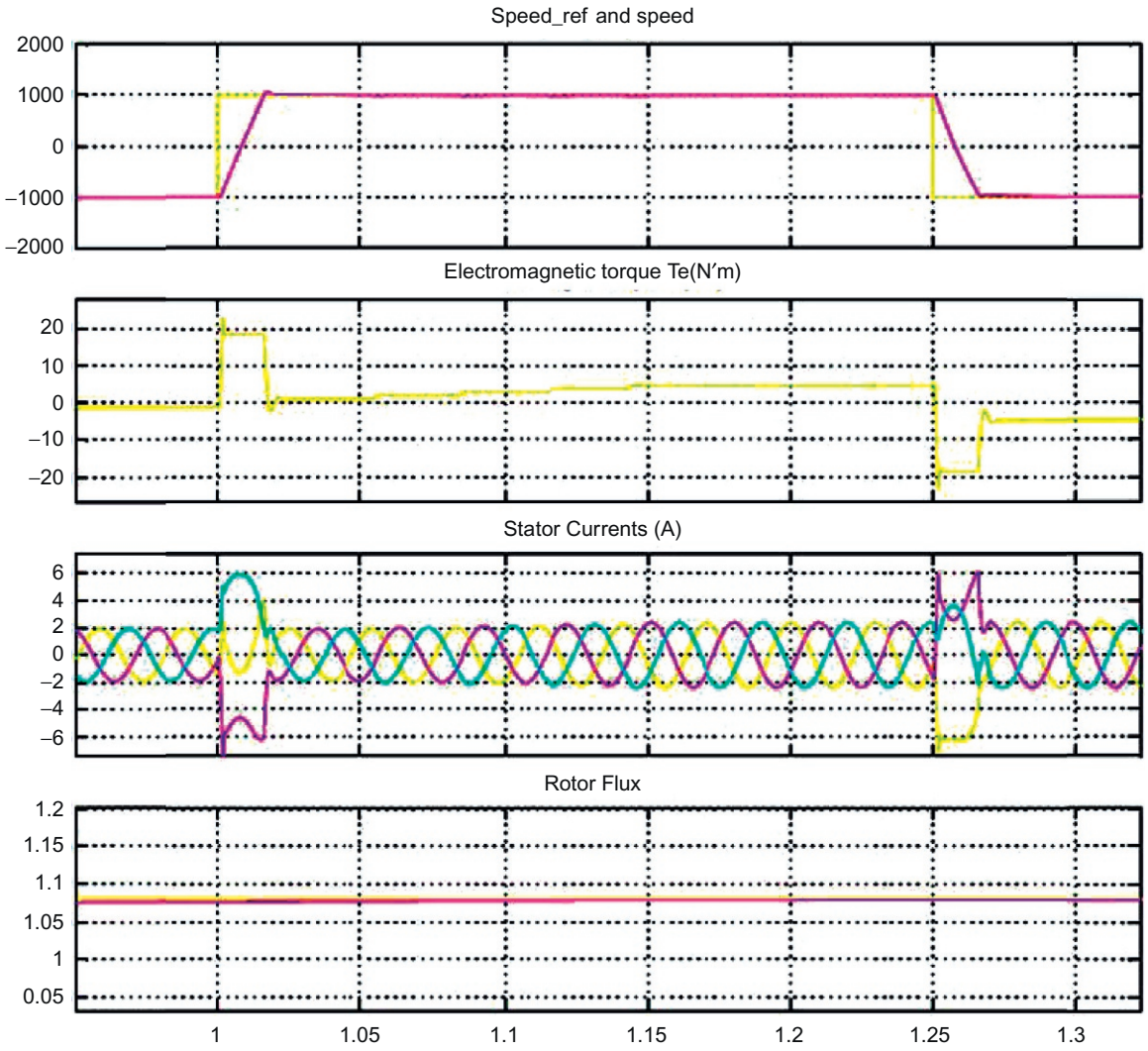


FIG. 30.29 Speed and current responses of an induction motor drive under the IFOC scheme of Fig. 30.28.

determined by the rotor time constant T_r. This is also indicated in Fig. 30.28. The rotor time constant T_r cannot be expected to remain constant for all conditions of operation. Its considerable variation with operating conditions means that the slip speed ω_{sl}, which directly affects the developed torque and the rotor flux vector position, may vary widely. Many rotor time-constant identification schemes have been developed in recent years to overcome the problem.

The mandatory requirement for a rotor-speed sensor is also a significant drawback, because its presence reduces the reliability of the IFOC drive. Consequently, sensorless schemes of identifying the rotor flux position have also drawn considerable interest in recent years.

Fig. 30.29 shows the transient response of an induction motor under the IFOC drive scheme of Fig. 30.28. In this case, the drive accelerates a large inertia load from standstill to the base speed of 1500 rev/min. It is clear that the overcurrent transients of Fig. 30.21 are eliminated, while the motor accelerates under a constant torque (implied by the constant rate at which the speed increases) and settles at the final speed with little over- or undershoot in speed. Clearly, rotor and air-gap fluxes remain constant at all times.

30.3.4.3 Direct Vector Control with Airgap Flux Sensing

In the direct scheme, use is made of the air-gap flux linkages in the stator d- and q-axes, which are then compensated for the respective leakage fluxes in order to determine the rotor flux linkages in the stator reference frame. The air-gap flux linkages are measured by installing quadrature flux sensors in the air gap, as indicated in Fig. 30.30.

By returning to Eqs. (30.32)–(30.40) in the stator reference frame and using some simplifications, it can be shown that

$$\lambda_{qr}^{s} = \frac{L_r}{L_m}\lambda_{qm}^{s} - L_{lr} i_{qs}^{s} \tag{30.57}$$

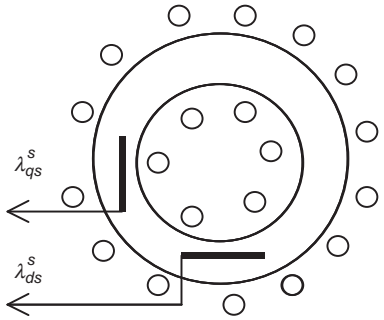


FIG. 30.30 Quadrature sensors for air-gap flux for direct vector control.

$$\lambda_{dr}^{s} = \frac{L_r}{L_m}\lambda_{dm}^{s} - L_{lr} i_{ds}^{s} \tag{30.58}$$

where the superscript s stands for the stator reference frame. Since the rotor flux rotates at a synchronous speed with respect to the stator reference frame, the angle θ_1 used for the coordinate transformations in Fig. 30.27 can be obtained from

$$\cos\theta_1 = \frac{\lambda_{dr}^{s}}{\hat{\lambda}_r} \tag{30.59}$$

$$\text{and} \quad \sin\theta_1 = \frac{\lambda_{qr}^{s}}{\hat{\lambda}_r} \tag{30.60}$$

where $|\hat{\lambda}_r| = \sqrt{\left(\lambda_{dr}^{2}\right)^2 + \left(\lambda_{qr}^{s}\right)^2}$.

The control of torque via i_{qs} and the rotor flux via i_{ds}, subject to satisfying conditions (30.50) and (30.51), remain as indicated in Fig. 30.28, according to the basic principle of vector control.

The requirement of air-gap flux sensors is rather restrictive. Such fittings also reduce reliability. Even though this method of control offers better low-speed performance than the IFOC, this restriction has practically precluded the adoption of this scheme. In an alternative method, the d- and q-axes stator flux linkages of the motor may be computed from integrating the stator input voltages.

30.4 Synchronous Motor Drives

30.4.1 Introduction

Variable-speed synchronous motors have been widely used in very large-capacity (> MW) pumping and centrifuge-type applications using naturally commutated current-source thyristor converters. At the low-power end, the current-source SPWM inverter-driven synchronous motors have become very popular in recent years in the form of permanent-magnet brushless dc and ac synchronous motor drives in servo-type applications. There are certain features of three-phase synchronous motors that have allowed them, especially the lower capacity motors, to be controlled with high dynamic performance using cheaper control hardware than is required for the induction motor of similar capacity. Since the average speed of the synchronous motor is precisely related to the supply frequency, which can be precisely controlled, multimotor drives with a fixed speed ratio among them are also good candidates for synchronous motor drives. This section begins with the performance of the variable-speed nonsalient-pole and salient-pole synchronous motor drive using the steady-state equivalent circuit followed by the dynamics of the vector-controlled synchronous motor drive.

30.4.2 Steady-State Equivalent-Circuit Representation of the Motor

Some of the operating characteristics of variable-frequency voltage- and current-source-driven synchronous motors can be readily obtained from their steady-state equivalent representation, as was the case with the scalar controls of induction motor drives. Assuming balanced, sinusoidal distribution of stator and rotor mmfs and a uniform air-gap (nonsalient-pole motor), the per-phase equivalent circuit of Fig. 30.31 represents the motor at a constant speed.

The representation in Fig. 30.31 is in terms of the RMS voltage V applied to the motor phase winding that consists of the phase resistance R, the synchronous reactance X_s (in Ω/phase), and the per-phase induced voltage E_f. The back emf E_f develops

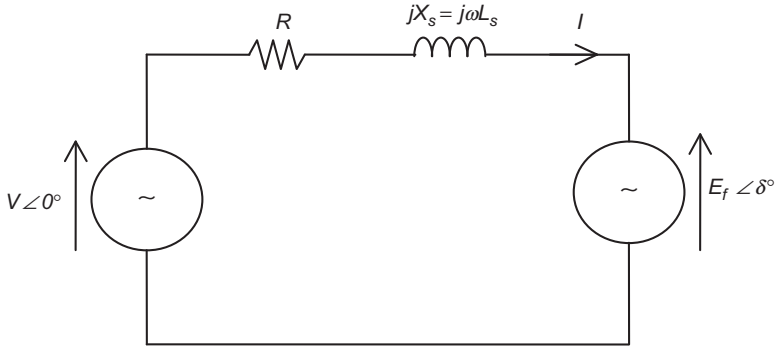


FIG. 30.31 Equivalent circuit of a nonsalient-pole motor.

in the stator phase winding as a result of rotor excitation supplied from an external dc source via slip rings or by permanent magnets in the rotor. The phasor E_f has an arbitrary phase angle δ with respect to the input voltage V. This is the load angle of the motor.

Unlike the induction motor, a synchronous motor may derive part or all of its excitation from the rotor via rotor excitation. For small synchronous motors that are used in the brushless dc and ac servo applications, this excitation is derived from permanent magnets in the rotor. This is readily and economically obtained with the modern permanent magnets, thus dispensing with the slip-ring-brush assembly. The i^2R losses in the rotor windings with the external excitation are also eliminated. These magnets also allow considerable reduction in space requirement for the rotor excitation. For large synchronous motors, this excitation is supplied more economically from an external dc source via slip rings or via an exciter.

The phasor diagrams of Fig. 30.32 may be used to analyze characteristics of the nonsalient-pole synchronous motor drive. Since the rotor magnetic field may be such that the motor may develop a back emf that is smaller or larger than the ac supply voltage to the stator windings, the motor may accordingly be underexcited or overexcited, respectively. The overexcited motor will normally operate at a leading power factor, as is the case in Fig. 30.32B. This is desirable in high-power applications.

In the phasor diagrams of Fig. 30.32C, the stator current I has been resolved into two components I_d and I_q, which are current phasors responsible for developing mmfs in the rotor d- and q-axes. These representations are in the stator reference frame, and hence are sinusoidal quantities at the frequency of the stator supply.

If the voltage drop across the stator resistance is neglected, which may be acceptable when the stator frequency is near the base frequency or higher, the developed torque T of the motor can be found from the phasor relationships of Fig. 30.32. Thus

$$T = \frac{3}{\omega_r}\frac{EV}{X_s}\sin\delta = \frac{3P}{\omega}\frac{EV}{\omega L_s}\sin\delta = \frac{3PK_\phi}{L_s}\frac{V}{\omega}\sin\delta \text{ Nm} \qquad (30.61)$$

for the nonsalient-pole motor (also for the sine wave PM ac motor with rotor magnets at the surface of the rotor) and

$$T = \frac{3P}{\omega_r}\left[\frac{EV}{\omega L_d}\sin\delta + \frac{V^2}{2}\left(\frac{L_d - L_q}{\omega L_d L_q}\right)\sin 2\delta\right] = 3P\left[\frac{K_\phi}{L_d}\frac{V}{\omega}\sin\delta + \frac{V^2}{2\omega^2}\left(\frac{L_d - L_q}{L_d L_q}\right)\sin 2\delta\right] \text{ Nm} \qquad (30.62)$$

for the salient-pole motor (also for the interior-magnet motor in which the rotor magnets are buried inside the rotor). Here, the flux constant of the motor, K_ϕ, is the ratio of the RMS value of the phase voltage E_f induced in the stator only due to the rotor excitation and speed. Note that for a given rotor excitation, the ratio $K_\phi = E_f/\omega$ remains constant at all speed.

30.4.3 Performance with Voltage-Source Inverter Drive

Eqs. (30.61) and (30.62) imply that if the motor is driven from a voltage-source supply and if the input voltage to frequency ratio, V-f, is kept constant, the motor will develop the same maximum torque at all speeds. For the nonsalient-pole motor, this maximum torque will occur for a load angle $\delta = 90°$. For the salient-pole motor, this will occur for a load angle, which is also influenced by the relative values of L_d and L_q.

At a low speed, where the supply voltage V is small, the voltage drop in the stator resistance may become significant compared with E_f. This may lead to a significant drop in the maximum available torque, as given by the torque Eqs. (30.63) and (30.64), which are derived from the phasor diagrams of Fig. 30.32. The stator per-phase resistance R is now included in the analysis. The developed torque is then given by

$$T = \frac{3PE_{fo}V_1}{\omega_o}\frac{\lambda X_{so}\sin\delta + R\left(\cos\delta - \dfrac{\lambda E_{fo}}{V_1}\right)}{R^2 + (\lambda X_{so})^2} \text{ Nm} \qquad (30.63)$$

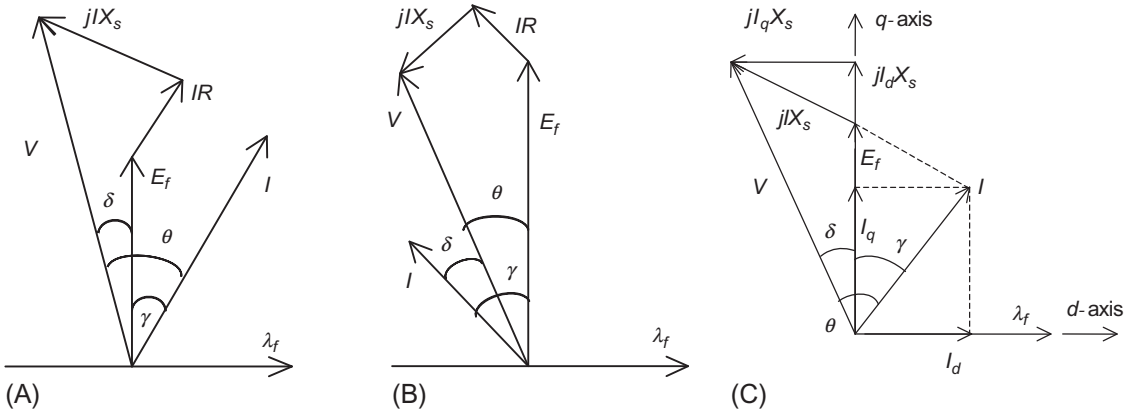


FIG. 30.32 Phasor diagrams of synchronous motors: (A) underexcited nonsalient-pole motor, (B) overexcited nonsalient-pole motor, and (C) underexcited salient-pole motor.

for the nonsalient-pole motor and

$$T = \frac{3P}{\omega_o}\left[\frac{\frac{V_1^2}{\lambda}R + VE_{fo}\lambda X_{qo}\sin\delta + \frac{V^2}{2}\left(X_{do} - X_{qo}\right)\sin 2\delta - VRE_{fo}\cos\delta}{R^2 + \lambda^2 X_d X_q}\right] \text{Nm} \tag{30.64}$$

for the salient-pole motor where the subscript o refers to the base quantities and λ refers to the per unit input frequency f_1/f_0.

Eqs. (30.63) and (30.64) indicate that the maximum torque that the motor can develop diminishes at a low speed because of the voltage drop across the stator resistance R. This drop in maximum available torque at a low speed can be avoided by boosting the input voltage at a low speed, as indicated in Fig. 30.33A. This voltage boosting is similar to the IR compensation applied to a variable-frequency induction motor drive.

Fig. 30.33 indicates an open-loop V-f inverter drive scheme, similar to the scheme for an induction motor drive in which the RMS stator input voltage is made proportional to frequency. The speed reference is passed through a first-order filter, as shown in Fig. 30.33A, so that a large and abrupt change in the input frequency command to the inverter is avoided. The filtered speed reference is translated into a proportional frequency reference f_1. The voltage reference V_1 is also proportional to frequency reference but with a zero frequency bias. The variable RMS input voltage V_1 to the motor may be obtained from an inverter by SPWM methods or from a cycloconverter with phase-angle control.

The available input voltage V_1 is normally limited by the available dc-link voltage to the inverter or the ac supply voltage to a cycloconverter. This limit is normally arranged to occur at base speed. Above this speed, the stator flux drops leading to field weakening and constant-power-like operation, as indicated in Fig. 30.33B. In some control scheme, the maximum load angle δ is not allowed to exceed a certain limiting value δ_{max}. By selecting δ_{max}, constant-power operation at various power levels is possible.

30.4.4 Characteristics Under Current-Source Inverter (CSI) Drive

A CSI-driven synchronous motor drive generally gives higher dynamic response. It also gives better reliability because of the automatic current-limiting feature. In a variable-speed application, the synchronous motor is normally driven from a stiff current source. A rotor-position sensor is used to place the phase current phasor I of each phase at a suitable angle with respect to the back-emf phasor (E_f) of the same phase. The rotor-position sensor is thus mandatory.

Two converter schemes have generally been used. In one scheme, as indicated in Fig. 30.34, a large dc-link reactor

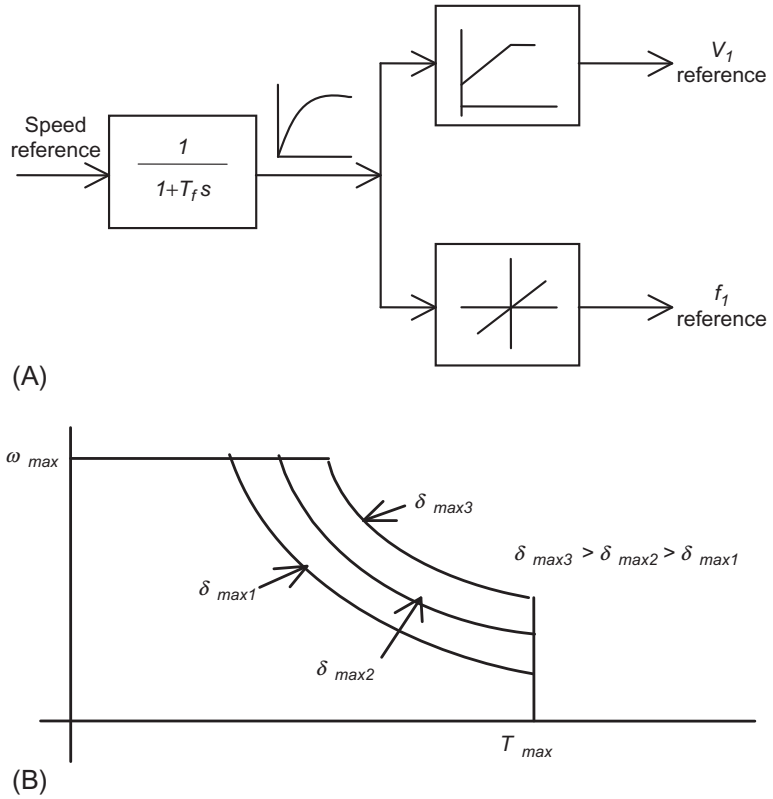


FIG. 30.33 (A) V-f controller for an open-loop inverter drive and (B) $T-\omega$ characteristics with a limited maximum δ for constant-power operation.

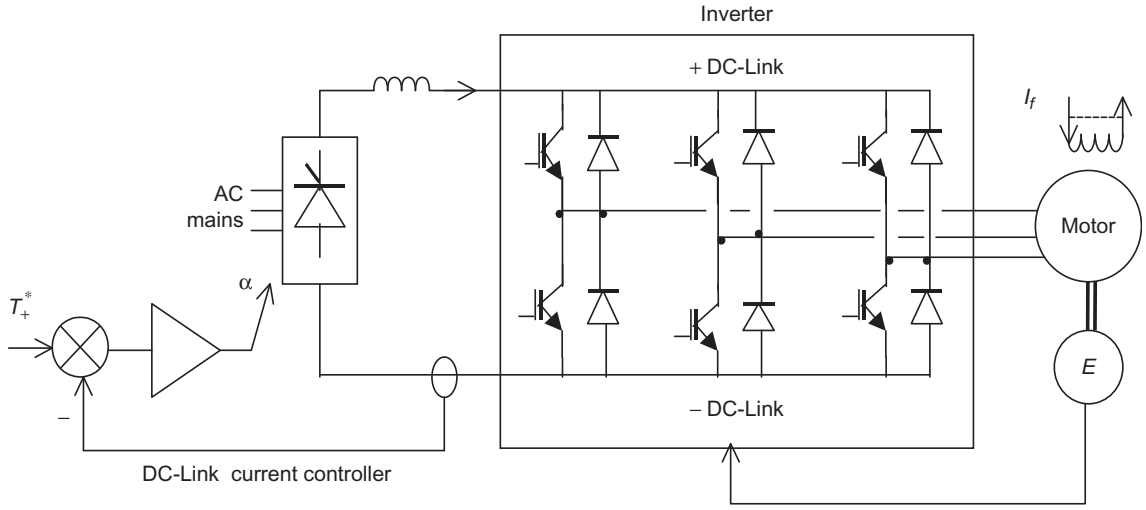


FIG. 30.34 Schematic of a current-source inverter (CSI)-driven synchronous motor.

(inductor) makes the current source to the inverter stiff. The scheme is suitable for large synchronous motors for which thyristor switches are used in the inverter. A current loop may also be established by sensing the dc-link current and by using a closed-loop current controller that continuously regulates the firing angle of the controllable rectifier in order to supply the inverter with the desired dc-link current. It can be shown that the motor-developed torque is proportional to the level of the dc-link current.

The inverter drives the motor with quasi-square-wave current waveforms as indicated in Fig. 30.35. The current waveforms are switched according to the measured rotor-position information, such that the current waveform in each phase has a fixed angular displacement, γ, with respect to the induced emf of the corresponding phase. Because of this, the drive is sometimes referred to as self-controlled. The angular displacement of these current waveforms (or their fundamental components) with the respective back-emf waveforms is

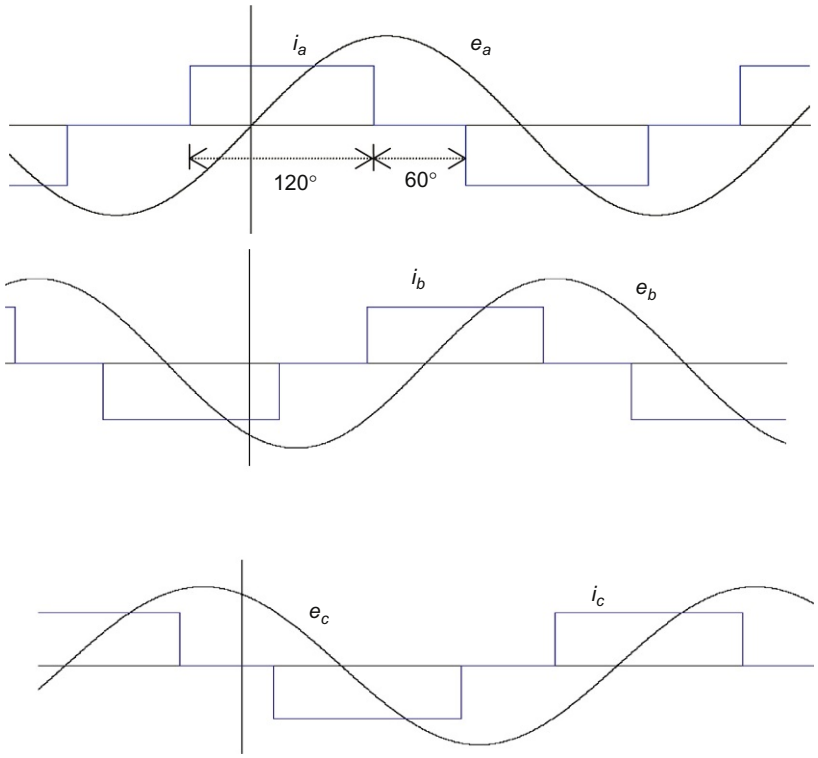


FIG. 30.35 Current waveforms in the dc-link current-source-driven motor.

indicated in Fig. 30.35. Because of the large dc-link inductor, the phase currents may be considered to remain essentially constant between the switching intervals. The quasi-square current waveforms contain many harmonics, and are responsible for large torque pulsations that may become troublesome at a low speed.

In the foregoing scheme, the motor can be reversed easily by reversing the sequence of switching of the inverter. It can also be braked regeneratively by increasing the firing angle of the input rectifier beyond 90° while maintaining the dc-link current at the desired braking level until braking is no longer required. The rectifier now returns the energy of the overhauling load to the ac mains regeneratively.

In another scheme, which is preferred for lower capacity drives for which higher dynamic response is frequently sought, phase currents are regulated within the inverter. The inverter typically employs gate turnoff switches, such as the IGBT, and pulse-width modulation techniques, as indicated in Fig. 30.36. Motor currents are sensed and used to close independent current controllers for each phase. Normally, two current controllers suffice for a balanced star-connected motor. Three-phase sinusoidal ac currents are supplied to the motor, the amplitude and phase angle of which can be independently controlled as required. The references for the current controllers are obtained from a three-phase current reference generator that is addressed by the feedback of the rotor position. The rotor position is continuously measured by a high-resolution encoder. In this way, the current references and hence the actual stator currents are synchronized to the rotor.

30.4.5 Brushless DC Operation of the CSI-Driven Motor

The torque characteristic of the CSI drive scheme of the foregoing section can be easily analyzed using the phasor diagrams shown earlier, if the harmonics in the motor-current waveform are neglected or if the motor-current waveforms are indeed sinusoidal as in the second scheme described earlier. In the following analysis, it is assumed that the supply current waveforms are sinusoidal. It is also assumed that the phase angle of these current sources with respect to the induced voltage in each phase can be arbitrarily chosen.

The phase back-emf and the current waveforms and the phasor diagram of the nonsalient-pole motor are shown in Fig. 30.37. The phase angle γ between the E_f and I phasors and the RMS value (or amplitude) of I are determined according to the desired torque and power factor considerations. The developed torque is found from the phasor diagram to be

$$T = \frac{3E_f I\cos\gamma}{\omega_r} = K\phi I\cos\gamma \text{ Nm} \tag{30.65}$$

If the angle $\gamma = 0°$ is chosen, the familiar dc-motor-like torque characteristic is obtained. It should be noted from the

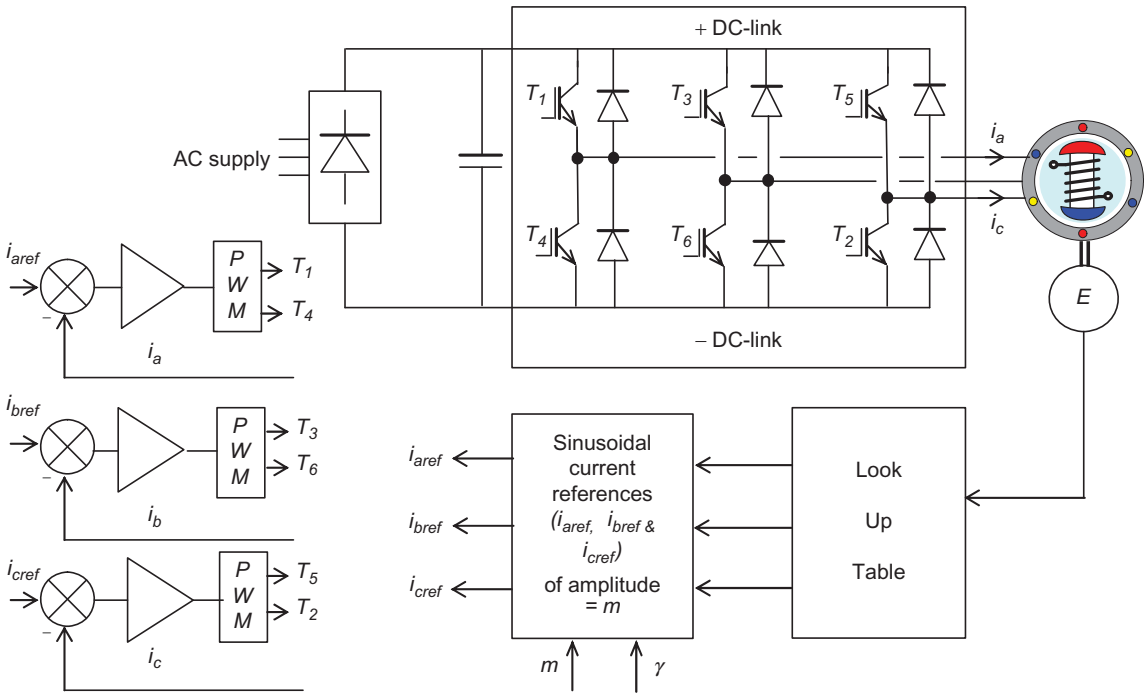


FIG. 30.36 Control scheme of the PWM current-source drive.

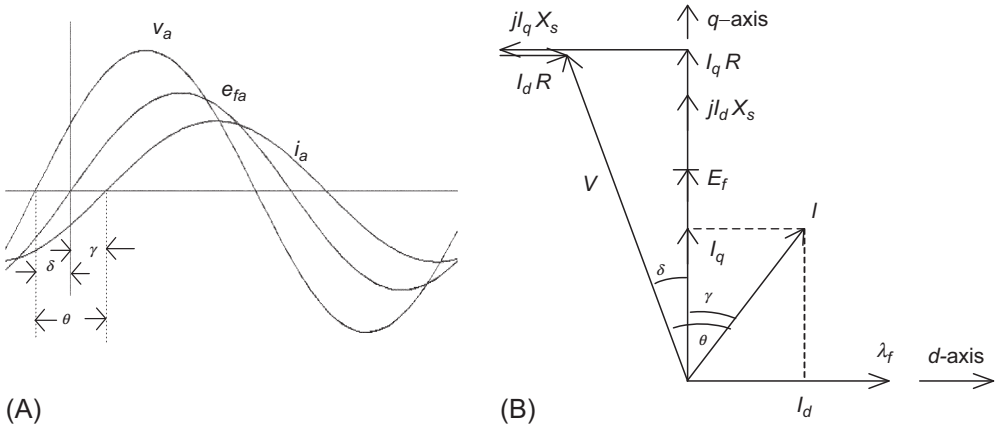


FIG. 30.37 Phasor relationships of CSI-driven motor: (A) back-emf and current waveforms and (B) the phasor diagram.

foregoing that the developed torque at any speed is independent of R since a high-gain (stiff) current-source drive is used. Note also that the ratio E_f/ω at any operating speed is proportional to the amplitude of the stator flux linkage, λ_f, due to rotor excitation. For fixed rotor excitation, this ratio is a constant.

Eq. (30.65) indicates that the developed torque of a nonsalient-pole synchronous motor can be controlled by controlling the amplitude of the rotor field (field control), or more conveniently, by controlling the amplitude of the stator phase current. The highest torque per ampere characteristic is achieved when $\gamma = 0°$. Note that the operation with a fixed γ angle is key to this dc-motor-like torque characteristic.

30.4.5.1 Operation with Field Weakening

If the stator impedance drop is neglected, the maximum E_f is largely determined by the dc-link voltage and $E_f = K\lambda_f\omega$ implies that speed ω can be increased by decreasing λ_f. Consequently, the operation above base speed is normally achieved with field weakening. In this speed range, because of the limited dc-link voltage, the rotor field must be weakened; otherwise, the amplitude of the phase-induced emf will exceed the dc-link voltage, and current control will not be effective. Field weakening is a means of keeping this voltage at the rated level for speeds higher than the base speed.

The flux linkage due to the rotor excitation, λ_f, can be adjusted when a variable rotor supply is available. This may also be achieved by demagnetizing the rotor mmf by using the mmf produced by the stator currents. For motors with permanent-magnet excitation, the latter is the only means of weakening the λ_f. Referring to the phasor diagram of Fig. 30.38, if I is made to lead E_f, the d-axis component of I, that is, I_d, will lead E_f by 90°. The mmf due to I_d then opposes the rotor d-axis mmf. The net rotor flux linkage along the q-axis is then given by

$$\lambda_f' = \lambda_f + L_d I_d \tag{30.66}$$

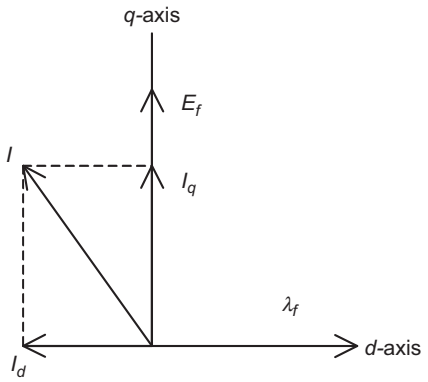


FIG. 30.38 Field weakening using stator mmf.

where I_d is negative when I leads E_f. If the air gap is small, the d-axis component of the armature current may reduce the rotor flux to the required extent.

30.4.6 Operating Modes

A synchronous motor may be driven with a view to achieving various operating characteristics, such as power factor compensation, maximum torque per ampere characteristic, and field weakening. The power factor at which a synchronous motor operates is an important issue, especially for a large drive. A large angle θ between the input voltage and current phasors of the motor results in a poor overall power factor. The operation of the synchronous motor with stator current waveforms with a certain phase angle with respect to the respective phase back-emf waveforms allows interesting power-factor compensation possibilities. Consider the following three cases.

30.4.6.1 Case 1: Operation with *I* Lagging E_f

In this case, the motor is underexcited and I lags E_f, by an angle γ, as indicated in Fig. 30.39. The overall power factor in this case

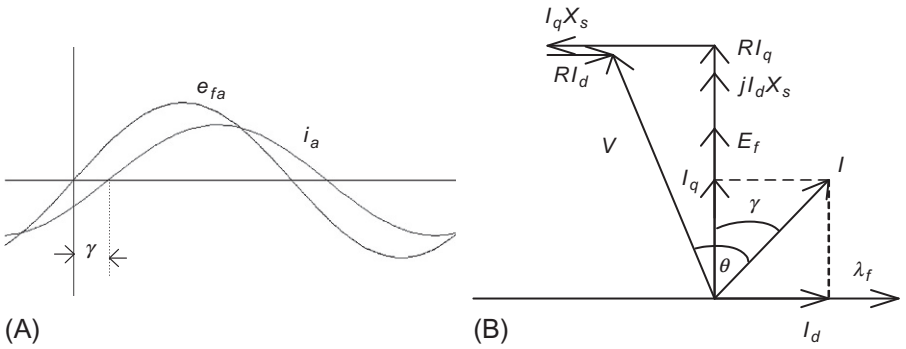


FIG. 30.39 (A) Phase back-emf and current waveforms and (B) the phasor diagram with I lagging E_f.

is lagging, since I lags V by an angle θ. The power-factor angle θ is larger than γ. Note that I_d now magnetizes the rotor field.

30.4.6.2 Case 2: I is in phase with E_f; Maximum Torque per Ampere Operation ($\gamma = 0°$)

If $\gamma = 0°$ is used, the motor input current i_a is in phase with the back emf e_a, as indicated in the waveforms of Fig. 30.40A. From Eq. (30.65), the developed torque is given by

$$T = K\phi I \tag{30.67}$$

Thus, for a fixed rotor excitation, the developed torque is the highest that can be achieved per ampere of stator current I. In other words, if $\gamma = 0°$ is chosen, the drive operates with its maximum torque per ampere characteristic. From the phasor diagram of Fig. 30.40B, it is clear that the input current I phasor now lags the voltage V phasor at the motor terminals (see the phasor diagram in the figure). Note that the level of E_f that is determined by the level of excitation also determines the angle θ to some extent. Clearly, when maximum-torque-per-ampere characteristic is required, a power factor less than unity has to be accepted.

30.4.6.3 Case 3: Operation with I Leading E_f

If I is chosen to lead E_f, the overall power factor can be higher, including unity, as is indicated in Fig. 30.41. Note that the

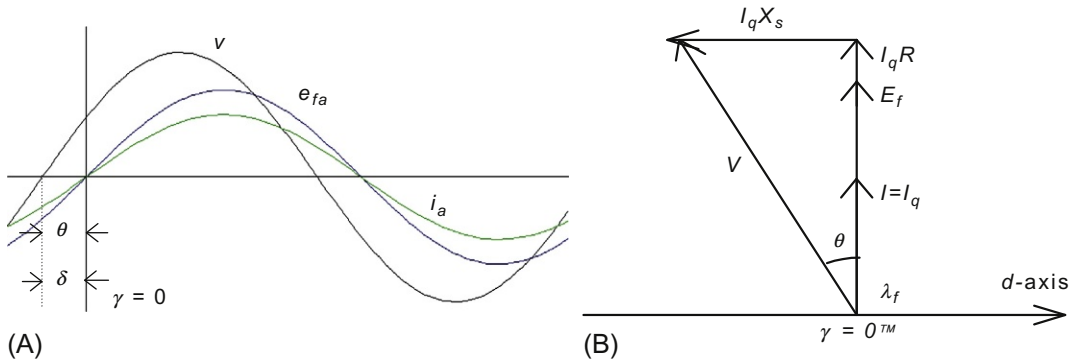


FIG. 30.40 (A) Phase back-emf and current waveforms and (B) phasor diagram for I in phase with E_f.

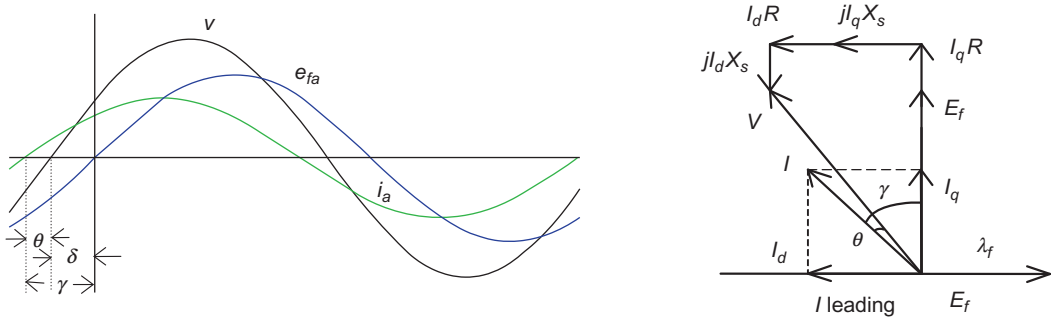


FIG. 30.41 Back-emf and current waveforms and phasor diagram for I leading E_f.

motor now operates with less than maximum torque per ampere characteristic. Note also that the d-axis component of I now tends to demagnetize the rotor and that the operation with field weakening is implied.

With a CSI-driven motor, the amplitude and the angle of the phase current relative to the back emf can be selected according to one of the desirable operating characteristics mentioned above. Additionally, other operational limits such as the inverter/motor-current limit, the maximum stator voltage limit, and the maximum power limit can also be addressed. The amplitude of the stator current I clearly determines the developed torque of the motor. Consequently, the error of the speed controller is used to determine the amplitude of I. The overall control system with an inner torque loop can be described by Fig. 30.42.

30.4.7 Vector Control

Controls described in foregoing sections were based on the steady-state equivalent circuit of the motor. Even though the torque Eq. (30.65) for a current-source drive evokes vector-control-like relationships, they do not address the dynamics of the current controls as is possible in an orthogonal reference frame. Using an orthogonal set of reference attached to the rotor, a simple set of decoupled, dc-motor-like torque-control relationships is readily obtained. Following the transformation technique used in Section 30.3.4, the stator voltage equations of a synchronous motor with fixed rotor excitation in the rotor reference frame are

$$\begin{bmatrix} v_q \\ v_d \end{bmatrix} = \begin{bmatrix} R+pL_q & \omega L_d \\ -\omega L_q & R+pL_d \end{bmatrix} \begin{bmatrix} i_q \\ i_d \end{bmatrix} + \begin{bmatrix} \omega\lambda_f \\ 0 \end{bmatrix} \tag{30.68}$$

$$T = \frac{3}{2}P\left(\lambda_f i_q + \left(L_d - L_q\right) i_d i_q\right) \tag{30.69}$$

where all the quantities in lower case represent instantaneous quantities in the rotor dq-frame. The λ_f is the flux linkage per phase due to the rotor excitation, ω is the electric angular velocity in radians per second, and P is the number of pole pairs. Here, p is the time derivative operator d/dt. Assuming the magnetic linearity, the stator flux linkages are

$$\begin{aligned} \lambda_d &= L_d i_d + \lambda_f \\ \lambda_q &= L_q i_q \end{aligned} \tag{30.70}$$

Note that the Eq. (30.68) can be written down directly from Eq. (30.31), taking into account the fixed rotor excitation so that the third and fourth rows and columns of Eq. (30.31) may be dropped. Since the reference frame now rotates at the speed of the rotor, $\omega_e = \omega$. The induced back emf due to the fixed rotor excitation occurs in the rotor q-axis and is included in Eq. (30.68), as a separate term. Similarly, the torque expression of Eq. (30.69) may also be written down from Eq. (30.41), using the flux linkages of Eq. (30.70).

Eqs. (30.67)–(30.69) are for a salient-pole motor for which $L_d \neq L_q$. For a nonsalient-pole motor, L_d is equal to L_q, and the developed torque is proportional to i_q only. In either case, the inner torque loop consist of two separate current loops: one for i_d and the other for i_q, as indicated in Fig. 30.43. The i_q current loop generally derives its reference signal from the output of the speed controller and constitutes the inner torque loop. The reference for the i_d current loop is normally specified by the extent of field weakening for which a negative i_d reference is used. Otherwise, the d-axis current is maintained at zero. Note that for large synchronous motors with variable external excitation, field weakening is normally applied through adjustment of the rotor excitation, using a spillover signal from the output of the speed controller.

From Eq. (30.68), it is clear that the couplings of q- and d-axis voltages exist through the d- and q-axis currents, respectively, and the back emf. During dynamic operation, such coupling effects become undesirable. The coupling effects of d- and q-axis currents and the back emf into q- and d-axis voltages, respectively, can be removed by the feedforward terms shown

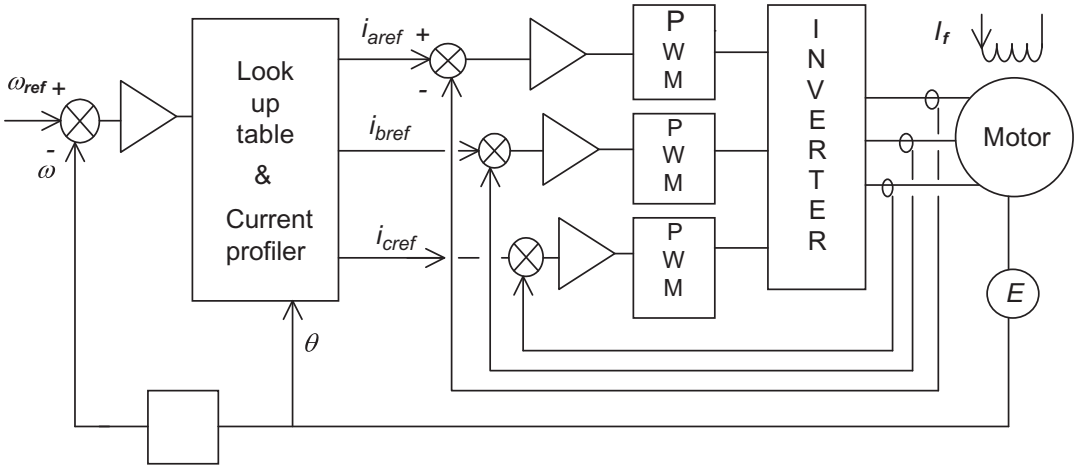


FIG. 30.42 Structure of a speed-control system with a CSI-driven synchronous motor.

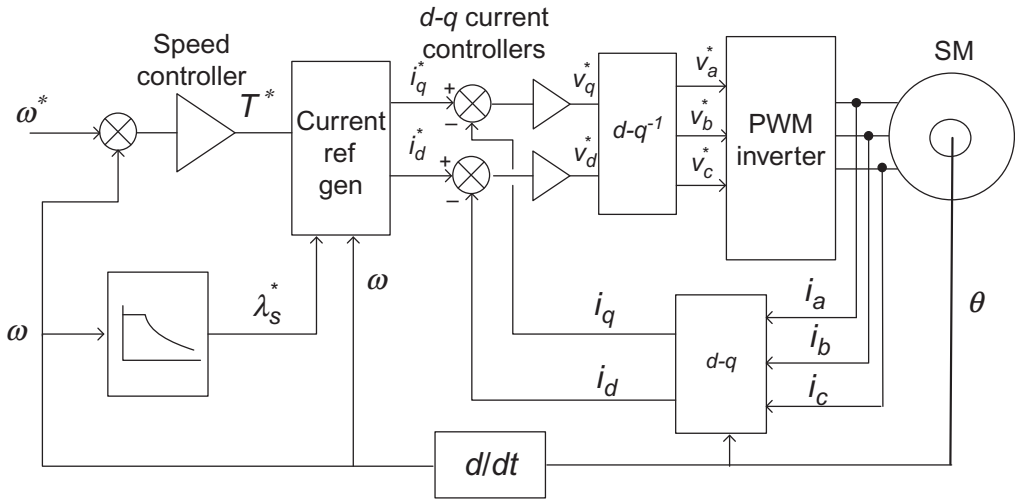


FIG. 30.43 Inner torque loop of a vector-controlled synchronous motor drive.

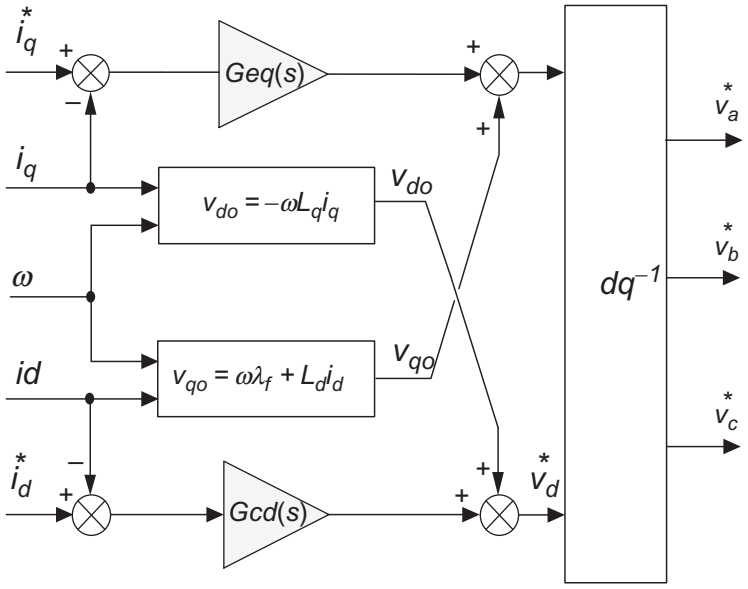


FIG. 30.44 The *d*- and *q*-axis decoupling compensation.

in the shaded part of the block the diagram of Fig. 30.44, which also shows the two current-control loops. The two outputs v_d^* and v_q^* from the decoupled current controllers are transformed to the stator reference frame before being subjected to pulse-width modulators or hysteresis comparators. Note that the current references i_d^* and i_q^* are obtained with due regard for the desired operating and limiting conditions as described in Section 30.4.5.

Under this type of control, which is exercised in the rotor reference frame, the *d*- and *q*-axis currents are separately regulated. The purpose of the *q*-axis current controller is primarily to control the developed torque, especially for the nonsalient-pole motor. For this motor, the *d*-axis current is normally maintained at zero, when the motor is operated below the base speed. The *d*-axis current may be used to weaken the air-gap flux so that the motor operates with a constant-power-like characteristic. It should be noted that the field weakening may also be carried out more directly by adjusting the rotor excitation current by using a spillover signal from the speed controller, when the base speed is exceeded.

The dynamic response of the drive under the vector control scheme indicated in Fig. 30.44 is the highest possible with a CSI drive. It should also be noted that the *dq* currents in the rotor reference frame vary only the mechanical dynamics of the rotor. In fact, they are dc quantities when the motor runs at a constant speed. Consequently, the following error (or lag)

associated with tracking a sinusoidally time-varying current reference, which is the case when current control is exercised in the stator $a-b-c$ reference frame, can be reduced easily by using an integral-type current controllers.

30.5 Permanent-Magnet Synchronous Motor Drives

30.5.1 Introduction

Since the introduction of samarium cobalt and neodymium-iron-boron magnetic materials in the 1970s and 1980s, respectively, synchronous motors with permanent-magnet excitation in the rotor have been displacing the dc motor in many high-performance applications. The trend is more noticeable in applications requiring high-performance motors of up to a few kilowatts. In low- to medium-power applications, the superior dynamics, smaller size, and higher efficiency of motors with PM excitation in the rotor, compared with all other motors, are well-known.

The arrangement just mentioned is very similar to a conventional synchronous motor. This is particularly so when the stator windings and the rotor mmf are sinusoidally distributed. Several rotor configurations of the PM synchronous motor have been developed, of which the important ones are indicated in Figs. 30.45–30.47.

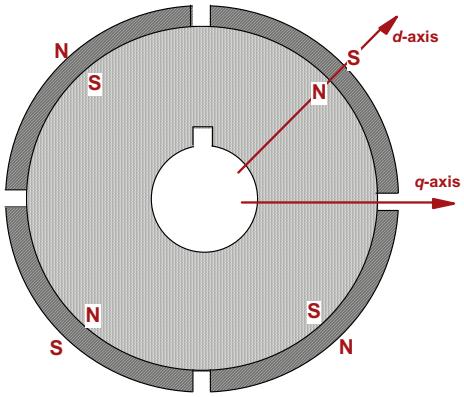


FIG. 30.45 Schematic of the cross section of a surface-magnet synchronous motor.

30.5.2 The Surface-Magnet Synchronous Motor with Trapezoidal Back Emf Waveform

The surface-magnet motor comes with the rotor magnets glued onto the surface of the rotor. An additional stainless steel (i.e., nonmagnetic) cylindrical shell may be used to cover the rotor in order to keep the magnets in place against centrifugal force in high-speed applications. Since the relative permeability of the magnetic material is very close to unity, the effective air gap is uniform and large. Because the air gap includes the magnet thickness, it is long. Consequently, the synchronous

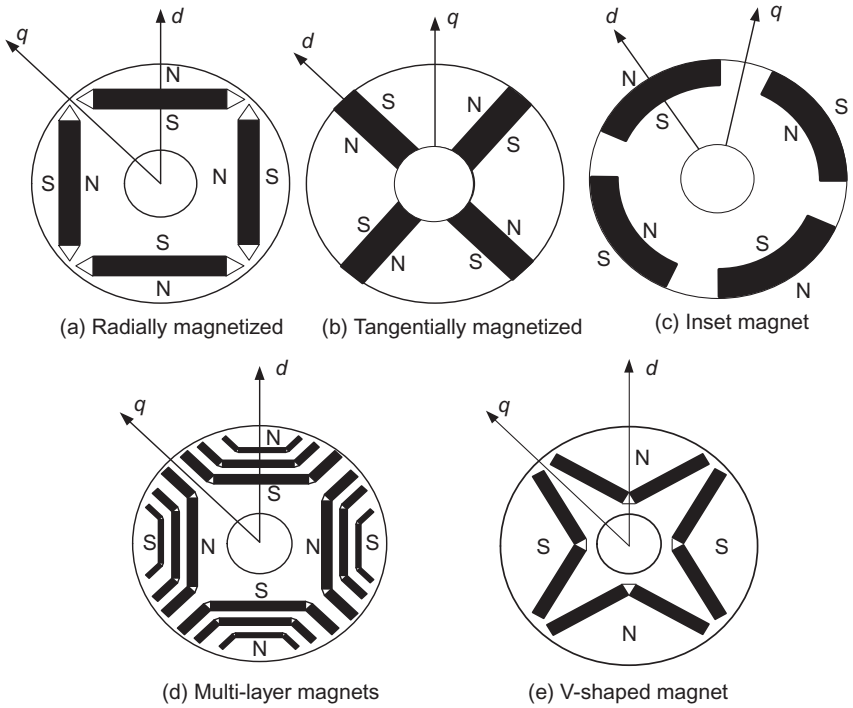


FIG. 30.46 Schematic of the rotor cross section of an interior-magnet motor.

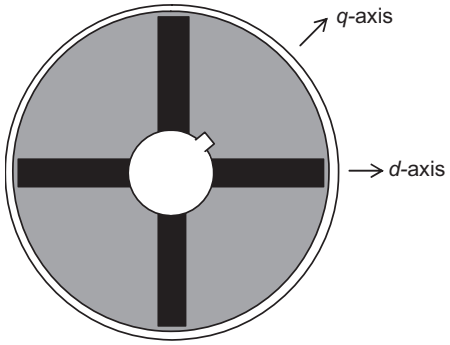


FIG. 30.47 Schematic of the rotor cross section of a circumferential-magnet motor.

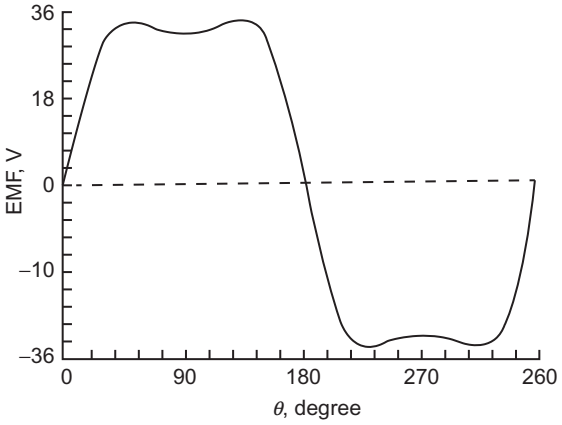


FIG. 30.48 Back emf of a trapezoidal waveform motor.

inductances along the rotor d- and q-axes, as indicated in Fig. 30.45, are equal and small (i.e., $L_d = L_q = L_s$). The armature reaction in this type of motor is small.

The three-phase winding in the stator has uniformly distributed windings. The span of the magnets are selected in such a way that the back emf induced in the stator windings are trapezoidal with nearly 120° of constant amplitude in each half cycle. Such a motor, often called a brushless dc (BLDC) motor because of its similarity to the inside-out conventional brushed PM DC motor, develops a trapezoidal back-emf waveform as indicated in Fig. 30.48, when it is driven at a constant speed. The back-emf waveforms have flattops for nearly 120° in each half cycle followed by 60° of transition from positive to negative polarity of voltage and vice versa. These motors are very suitable for variable-speed applications such as spindle drives in machine-tool and disk drives.

30.5.2.1 Control of the Trapezoidal-wave Motor

Neglecting higher-order harmonic terms, the back emf in the motor phases may be as indicated in Fig. 30.49. Each back emf has a constant amplitude (or flattop) for 120° (electric) followed by 60° of transition in each half cycle. The developed torque at any instant is given by

$$T = \frac{e_{an} i_a + e_{bn} i_b + e_{cn} i_c}{\omega} \text{ Nm} \tag{30.71}$$

It is readily seen that the ideal current waveform in each phase needs to be a quasi-square waveform of 120° of conduction angle in each half cycle. The conduction of current in each

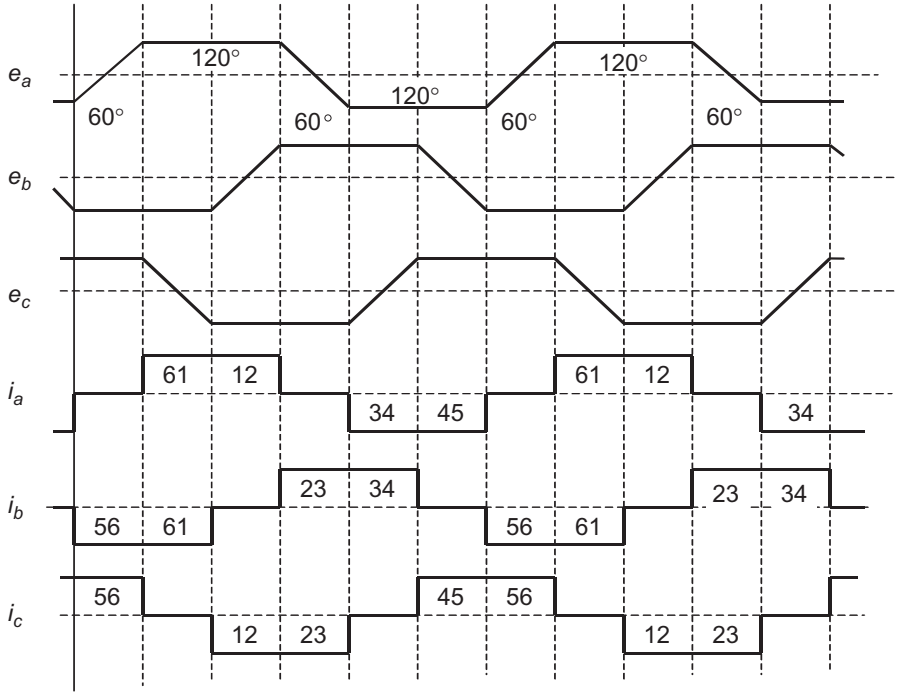


FIG. 30.49 Back-emf and current waveforms and on-states of transistor switches in the trapezoidal waveform motor.

phase winding coincides with the flat part of the back-emf waveforms, which guarantees that the developed torque, that is, $\left(\sum_{x=a}^{c}\frac{e_{xn}\cdot i_{xn}}{\omega_r}\right)$, is constant or ripple-free at all times. With such quasi-square current waveforms, a simple set of six opto-couplers or Hall-effect sensors would be required to drive the six inverter switches indicated in Fig. 30.36. The output current waveforms for the three-phase inverter and the switching devices that conduct during the six switching intervals per cycle are also indicated in Fig. 30.49. Since only six discrete outputs per electric cycle are required from the rotor-position sensors, the requirement of a high-resolution position sensor is dispensed with. Continuous current control for each phase of the motor, by hysteresis or PWM control, to regulate the amplitude of the motor current in each phase is normally employed. The operation of the BLDC motor drive is further described in detail in Section 30.6.

Even though careful electromagnetic design is employed in order to have perfect trapezoidal back-emf waveforms as indicated in Fig. 30.49, the back-emf waveforms in a practical brushless dc motor exhibit some harmonics, as indicated in Fig. 30.48. If ripples in the back-emf waveforms are significant, then torque ripples will also exist when the motor is driven with quasi-square phase current waveforms. These ripples may become troublesome when the motor is operated at a low speed, when the motor load inertia may not filter out the torque ripples adequately.

A second source of torque ripple in the permanent-magnet brushless dc (PM BLDC) motor is from the commutation of current in the inverter. Since the actual phase currents cannot have the abrupt rise and fall times as indicated in Fig. 30.49, torque spikes, one for each switching, may exist.

Even though the PM BLDC motor does not have sinusoidal back emf and inductance variations with rotor angle, the analysis of Section 30.4 in terms of the fundamental quantities will often suffice. The switching of the inverter using the six rotor-position sensors guarantees that the current waveform in each phase always remains in synchronism with the back emf of the respective phase. Since the quasi-square phase current waveform in each phase coincides with the flat part of the back-emf waveform of the same phase, the angle γ is clearly zero for such operation. Thus, considering fundamental quantities, the motor back emf and the torque characteristics can be expressed by

$$E = K_E\omega \text{ V} \tag{30.72}$$

$$T = K_T I\cos\gamma = K_T I \text{ Nm} \tag{30.73}$$

where K_E and K_T are equal in consistent units. Note that E and I are now RMS values of the fundamental components of these quantities.

30.5.2.2 Sensorless Operation of the PM BLDC Motor

In spindle and other variable-speed drive applications, where the lowest speed of operation is not less than a few hundred revolutions per minute, it is possible to obtain the switching signals for the inverter from the motor back emf, thus dispensing with rotor-position sensors. The method consists of integrating the back-emf waveforms, which are the same as the applied phase voltage if the other voltage drops are neglected, and comparing the integrated outputs with a fixed reference. These comparator outputs determine the switching signals for inverter. It may be noted that the amplitude of the back-emf waveforms is proportional to the operating speed, so that the frequency of the comparator outputs increases automatically with speed. In other words, the angle γ and the current waveform relative to the back-emf waveform in each phase remains the same regardless of the operating speed. Integrated circuits are available from several suppliers that perform this task of sensorless BLDC operation satisfactorily, covering a reasonable speed range.

30.5.3 The PM Synchronous Motor with Sinewave Back Emf Waveforms

The PM sine-wave motor, which may also have magnets on the rotor surface or buried inside the rotor (as in the interior-magnet motor of Fig. 30.46), typically has sinusoidally distributed windings. The air-gap flux distribution produced by the rotor magnets is also sinusoidal, arranged through magnet and rotor flux barrier shaping. Consequently, the back-emf waveform of each phase when running at a constant speed is also a sinusoidal waveform, as indicated in Fig. 30.50, when the motor is driven at a constant speed.

It should be noted, however, that with magnets mounted on the rotor surface, the effective air gap is large and uniform so that $L_d = L_q = L_s$. Because of the large equivalent air gap, these inductances are also small, and consequently, the armature reaction is small. As a result, this motor essentially operates with fixed excitation, and there is hardly any scope for altering the operating power factor or the rotor mmf, once the motor and its drive voltage and current ratings have been selected.

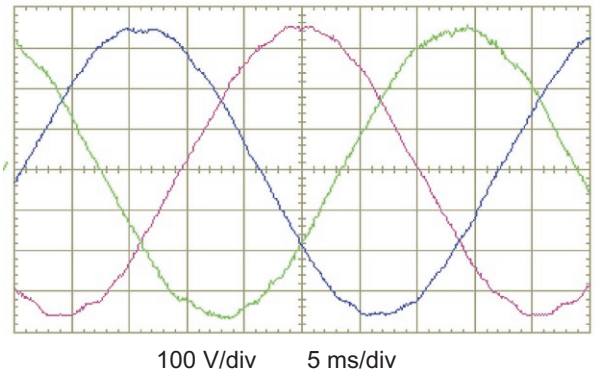


FIG. 30.50 Back-emf waveforms of a sine-wave PM motor. Speed = 1815 rev/min.

The interior permanent-magnet synchronous motor (IPMSM), which comes with magnets buried inside the rotor as indicated in Figs. 30.46, has an easier magnetization path along the rotor q-axis, so that $L_q > L_d$. The small air gap implies that the inductances L_d and L_q may not be small and hence may allow considerable scope for field weakening.

If the sine-wave motor is supplied from an PWM inverter, the analyses and vector diagrams of PM sine-wave motor are similar to those in Section 30.4 for the nonsalient-pole and salient-pole synchronous motor drives. The surface-magnet motor is more akin to the nonsalient-pole motor, since $L_d = L_q = L_s$, whereas the interior-magnet motor is more akin to the salient-pole motor because of the d- and q-axis inductances being unequal. Thus, the equations in Section 30.4 will apply equally well for this motor, both in the steady state and dynamically and for both voltage- and current-source supply.

30.5.3.1 Control of the PM Sinewave Motor

The sinusoidal back-emf waveforms imply that the three-phase motor must be supplied with a sinusoidal three-phase current if a dc-motor-like (or vector-control-like) torque characteristic is desired, as was found in Section 30.4. For such operation, the phase currents must also be synchronized with the respective phase back-emf waveforms, in other words, with the rotor dq- reference frame. This implies the operation with a specified γ angle. Two implementations are possible.

In one scheme, the stator currents are regulated in the stator reference frame, and the stator current references are produced with reference to the rotor position, as indicated in Fig. 30.51. The rotor position θ is continuously sensed and used to produce three sinusoidal current references of unit amplitude. The phase angle γ of the references relative to the respective back-emf waveforms is usually derived from the speed controller, which defines the field-weakening regime of the drive. The operating power factor of the drive may also be addressed using the γ angle control, as explained in Section 30.4.5. The amplitudes of these references are then multiplied by the error of the speed controller in order to produce the desired torque reference. In this way, both the RMS value I of the phase current and its angle γ with respect to E_f can be adjusted independently (which is equivalent to independent dq-axis current control). Three PWM current controllers are indicated, but two suffice for a balanced motor. Other types of current controllers, such as hysteresis controllers, may also be used.

In the second scheme, the motor currents are first transformed into the rotor dq-reference frame using continuous rotor-position feedback, and the measured rotor d- and q-axis currents are then regulated in the rotor reference frame, as indicated in Fig. 30.52. The main advantage of regulating the stator currents in the rotor reference frame, compared with the stator reference frame as in the first scheme, is that current references now vary more slowly and hence suffer from lower tracking error. At constant speed, the stator current references are in fact dc quantities as opposed to ac quantities, and hence, the inevitable tracking errors of the former scheme are easily removed by an integral-type controller. The other advantage is that the current references may now include feedforward decoupling so as to remove the cross coupling of the d- and q-axis variables as shown in the motor representation of Fig. 30.52. The latter scheme is currently preferred, since it allows more direct control of the currents in the rotor reference frame.

It should be noted that continuous transformations to and from rotor dq-axes are required; hence, the rotor-position sensor is a mandatory requirement. Rotor-position sensors of 10- to 12-bit accuracy are normally required. This is generally viewed as a weakness for this type of drive.

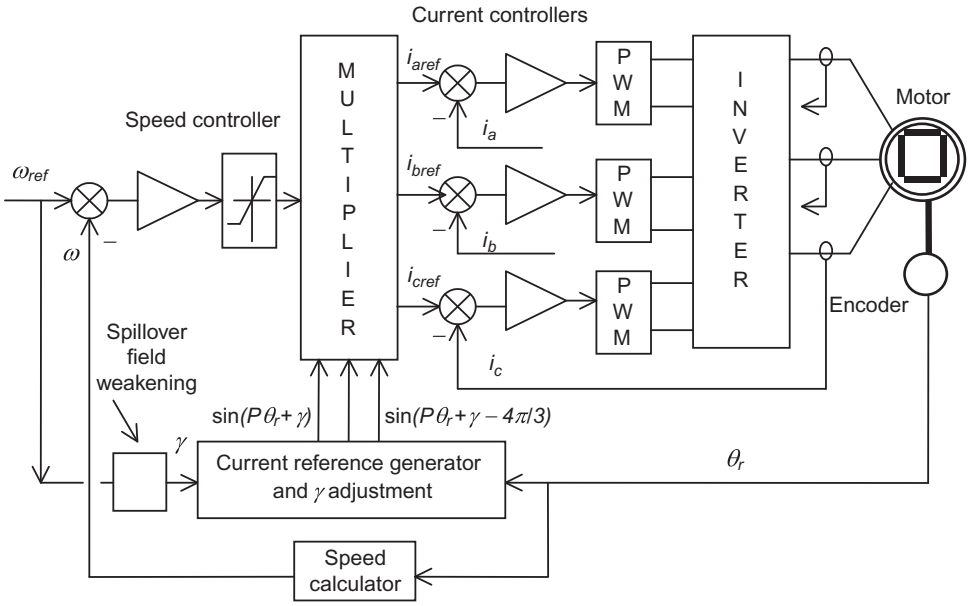


FIG. 30.51 Speed-controlled drive with the inner torque loop via current control in the stator reference frame.

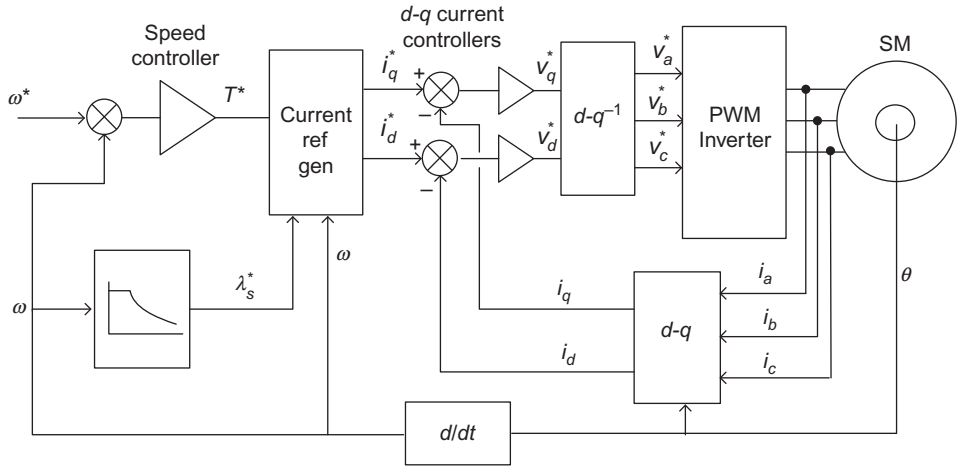


FIG. 30.52 Block diagram of a current-controlled drive.

The general torque relationship of a sine-wave motor supplied from a current-source SPWM inverter is given by Eq. (30.69) that is rewritten here:

$$T = \frac{3}{2}P\left(\lambda_f i_q + \left(L_d - L_q\right) i_d i_q\right) \tag{30.74}$$

Precise control of the developed torque control requires that both i_d and i_q be actively controlled in order to regulate it to the level determined by the error of the speed controller. For the surface-magnet synchronous motor, the large effective air gap means that $L_d \approx L_q$, so that i_d should be maintained at zero level. This implies that the i_d current reference in Fig. 30.52 should be kept zero. For the interior-magnet motor, $L_q > L_d$, so that i_d and i_q have to be controlled simultaneously to develop the desired torque. A few modes of operation are possible.

30.5.3.2 Operating Modes

Operation with maximum torque per ampere (MTPA) characteristic

In this mode of control, the developed torque T per ampere of stator current is the highest for a given rotor excitation. The combination of i_d and i_q that develops the maximum torque per ampere of stator current is indicated in Fig. 30.53. The reference signal for the inner torque loop normally determines the i_q reference, while the i_d reference is given by

$$i_d = \frac{\lambda_f}{2\left(L_q - L_d\right)} - \sqrt{\frac{\lambda_f^2}{4\left(L_q - L_d\right)^2} + i_q^2} \tag{30.75}$$

It should be noted that with $i_d = 0$, this mode of operation is achieved for the surface-magnet motor.

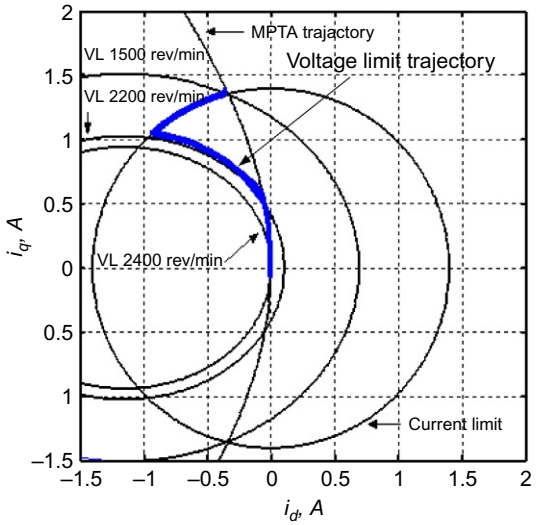


FIG. 30.53 $i_d - i_q$ Trajectories for the maximum torque per ampere characteristic and for maximum voltage and current limits of an interior PM motor.

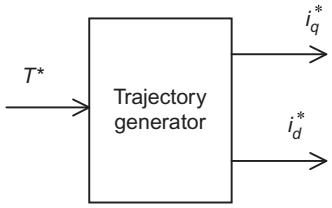


FIG. 30.54 i_d and i_q Trajectory generation satisfying the desired operating modes.

Operation with voltage and current limits

The maximum current limit of the motor/inverter, I_{smax}, is normally imposed by setting appropriate limits on i_d and i_q such that

$$i_d^2 + i_q^2 \leq I_{\text{smax}}^2 \tag{30.76}$$

Eq. (30.75) defines a circle around the origin of the $i_d - i_q$ plane.

The available dc-link voltage to the inverter places an upper limit of the motor phase voltage, V_{smax}, given by

$$V^2 = V_d^2 + V_q^2 \leq V_{\text{max}}^2 \tag{30.77}$$

$$\left(L_q i_q\right)^2 + \left(L_d i_d + \lambda_f\right)^2 \leq \left(\frac{V_{am}}{\omega}\right)^2 \tag{30.78}$$

where the stator voltages v_d and v_q are expressed in the rotor reference frame, as in Eq. (30.68). Eq. (30.78) is obtained from the voltage equation of Eq. (30.68) when the phase resistance R is neglected. Eq. (30.78) defines elliptical trajectories that contract as speed increases. All the three modes of operation are included in Fig. 30.53.

Operation with field weakening

This mode of operation is normally required for operating the motor above the base speed. A constant-power characteristic is normally desired over the full field-weakening range. For a given rotor excitation of λ_f and developed power of P_0, the developed torque T and the net rotor flux linkage required for constant-power operation can be determined. From this, the limiting values for i_d and i_q, which further constrain the allowable $i_d - i_q$ trajectory is also indicated in Fig. 30.53, can be determined.

The operating modes described in the preceding section are normally included in a trajectory controller that generates the references for i_d and i_q continuously, as indicated in Fig. 30.54.

30.6 Permanent-Magnet Brushless DC Motor Drives

30.6.1 Machine Background

Anyone studying electric machines would be aware that the classical synchronous machine offers the possibility of the very highest efficiencies. These machines have the current-carrying conductors in the stationary part; therefore, there is no need to transfer high power through a brush system. The field is provided on the rotating part either by an electromagnet, which does require some very low-power brushes, or, at best, by a permanent magnet with no power requirements at all.

This is clearly better than the traditional dc machine with high-power brushes and rotating conductors, with those conductors having a very poor path for heat to get away under overload conditions. You might ask, "why did we use so many of them?" It was of course because the dc machine offered the ability to control the speed fully and easily, which the synchronous machine, when running from the mains at a fixed frequency, was definitely not capable of. Thus, for example, all electric trains and trams built up to the 1980s, many of them still in service, use brushed dc motors. Low-cost, high-energy-density, and rare-earth PM materials available since 1984 changed this scene fundamentally.

The induction machine, the work horse of industry, is quite efficient, but because of the need to carry magnetizing current in the stator and load current and the existence of slip, it cannot be as good as the synchronous machine. It also innately has a very limited speed range.

All this changed with the advent of inexpensive, reliable power electronics. Quite suddenly, power electronics engineers had the ability to vary both the frequency and the amplitude of an ac supply and thus to provide the holy grail of variable-speed ac motors. This was first applied to induction machines, with the simplest form of open-loop control. The complexity of control for synchronous machines added substantially to the cost and was not so appealing. Today, the thought of putting a digital signal processor (DSP) or a microcontroller in a small motor controller is no longer as daunting as it was 10 years ago, so the distinction between the complexity of a controller for induction machines and synchronous machines has almost disappeared.

While power electronics radically changed our attitudes to electric machine design and operation, there was a second very important development that arrived on the scene at almost the same time: the appearance of very powerful rare-earth permanent-magnet materials.

The first rare-earth magnet material was samarium cobalt, used in very special applications such as space and defense, but it was then and still is very expensive. Neodymium-iron-boron (Nd-Fe-B) came next with even higher energy product. Energy product is a measure used to quantify the effectiveness of magnets. Nd-Fe-B began expensively but has continued to drop in price at a spectacular rate and recently became cheaper than ferrites in term of dollars per unit of energy product.

Thus, all the machines discussed here are permanent-magnet (PM) machines, in general using Nd-Fe-B magnets.

30.6.1.1 Clarifying Torque Versus Speed Control

As is well understood, given a fixed magnetic flux level, the magnitude of the current in a motor determines the magnitude of the torque out of the machine. In a general application if a torque is set, the speed is determined by the load. This is what happens when driving an automobile. The throttle or accelerator varies the torque. The speed can be very slow or very high for the same foot position, depending on the road conditions and vehicle motion history, even if the vehicle is in the same gear. This principle of torque control rather than speed control is fundamental to the operation of electric machines. When speed control is required in PMBDCMs, it is usual to implement torque control, with an extra outside control loop, like a cruise control in an automobile, to use the torque control to deliver speed control. So from here on, the discussion will describe torque control for the variable-speed motor.

30.6.1.2 Permanent-Magnet AC Machines

There are two quite different types of permanent-magnet ac machines, actually looking very similar in their physical realization but dramatically different in their electric characteristics and in the way in which they are controlled.

Permanent-magnet synchronous machines

These are simple extensions of the classical synchronous machine, where all of the voltages and currents are designed to be sinusoidal functions of time, as they are in the synchronous machine when used as a supply generator. These machines are known as permanent-magnet synchronous machines (PMSMs) or brushless ac machines and are discussed elsewhere in this book. While the application of sinusoidal waveforms everywhere is comforting to many and does result in less acoustic noise, less "stray losses," etc., there is in general a requirement to know the exact rotor angular position at every instant of time, with an accuracy in the order of one degree. This knowledge is then used to shape the current waveforms to be sure that they are in phase with the back emf of the windings. While much research is going on to run these machines without position sensors, the reality in the workplace today is that you need to include a relatively expensive shaft position encoder with your PMSM, if you wish to control it electronically.

Permanent-magnet brushless DC machines

A very much simpler possibility has emerged, which also gives the benefits of smooth torque and rapid controllability. This results in smaller minimum machine size, yielding maximum machine power density.

For this variant, the current waveforms and the back-emf waveforms are trapezoidal rather than sinusoidal. In this case, the machine is known as a permanent-magnet brushless dc machine (PMBDCM), with waveforms as shown in Fig. 30.55.

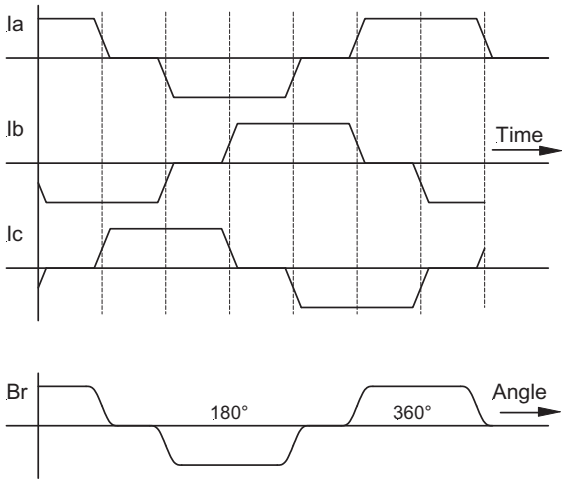


FIG. 30.55 Phase currents as functions of time and the flux density on the surface of the rotor as a function of angular position for a typical PMBDCM.

30.6.1.3 Brief Tutorial on Electric Machine Operation

The operation of electric machines can be explained in a variety of ways. Two possible and different methods are by the following:

1. Using an understanding of the interaction of magnetic fields and the tendency of magnetic fields to align. This tendency to align is what provides the force that makes a compass needle swing around, until it aligns with the earth's magnetic field.
2. Using the physical principle that "a current-carrying conductor in a magnetic field has a force exerted on it." This force is commonly known as the Lorentz force.

The difference between the two explanations is that the first method gives better "physical pictures." However, when one gets a little more serious, wanting to put in numbers, the force equations, while not greatly more difficult, are a little more challenging as they involve vector cross products.

With the second method, once the principle is accepted, there is a particularly simple scalar version of the force equation that very rapidly and simply gives numeric answers. The directions of the force, current, and motion are all orthogonal, that is, at right angles and a formal exposition would again use a vector cross product. However, provided the rules learned in high school science are applied, the scalar version, $F = BLI$ can be used, where F is the force in newtons, B is the flux density in tesla, L is the length of the conductor in meters, and I is the current in amperes.

Let us try both the methods, on the simple machine of Fig. 30.56.

The rotor is a magnet with a north and a south pole, and there is a coil of wire in the slots in the stator. Current is shown

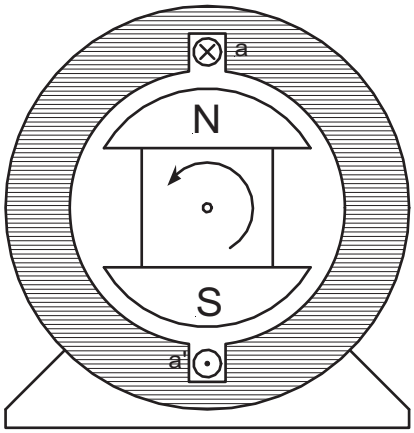


FIG. 30.56 A simple motor with a single coil in the stator and a permanent-magnet rotor.

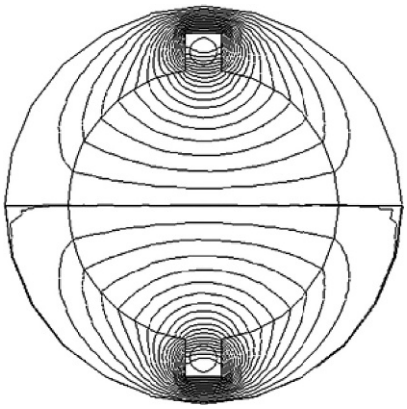


FIG. 30.57 A computer generated magnetic field for current in the windings and a stator made of electric steel.

going into the conductor called a at the top of the stator and coming out of the conductor called **a**′ at the bottom. To simulate a real machine more closely, one should imagine putting a one-turn "coil" of wire into the slot, with a connection made at the back of the machine to connect the top wire to the bottom, so that by applying a positive voltage to the top wire and a negative voltage to the end of the coil (the bottom wire), current will flow in at the top and out at the bottom as discussed previously.

Method 1. If the current is put into the top and comes out of the bottom as marked, then according to the right-hand rule (if you forget, then look at the Institution of Electrical and Electronic Engineers (IEEE) logo), magnetic flux will be forced to go through the center of the coil from right to the left, creating a north pole on the left. The flux will then double back through the iron frame of the motor to arrive back at the south pole on the right.

Fig. 30.57 shows a computer-generated magnetic field plot. This was produced using finite element analysis and modeling the stator as electric steel, the volume in the center as air and injecting current into the coil.

If the permanent-magnet rotor is then put inside the stator of Fig. 30.57, the rotor will align by rotating 90° counterclockwise.

Method 2. In this case, looking at Fig. 30.58, the conductor **a** will be immersed in a quite dense field produced by the magnets, with the flux lines going up the page in the rotor, across the air gap into the steel of the stator, heading down the stator to jump back across the lower air gap to return to the south pole. If a current is directed into the upper conductor and out of the bottom as before, it will produce force. Applying the direction rules associated with the Lorentz force, the force on the conductor will be to the right at the top and to the left at the bottom. Invoking Newton's third law, that action and reaction are equal and opposite, it is clear that if the wire is fixed, as it is, then there will be a force on the rotor to the left at the top and to the right at the bottom; thus, the rotor will move counterclockwise as before.

30.6.2 Electronic Commutation

If the rotor of Fig. 30.58 moves, then to keep it rotating in the same direction, sooner or later, the current in the conductors

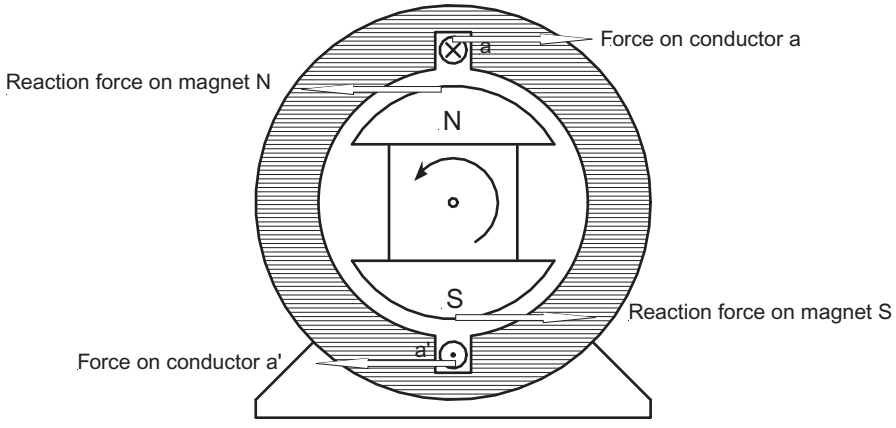


FIG. 30.58 Lorentz forces on conductor and rotor of a simple machine.

must be reversed. The time at which that needs to be done is when the rotor has moved to an almost aligned position, so it is not really a matter of time but a matter of rotor position. Since the rotor is a permanent magnet, it is a very simple matter to determine at least where the physical pole edges are using simple, reliable, and inexpensive Hall-effect (HE) sensors. These are small semiconductor devices that respond to magnetic flux density. (There are many ways to sense the position of the rotor; however, the remainder of this exposition will stay with the HE sensor for simplicity.)

A very simple motor, relying on the inertia of the rotor for continuous rotation, could have a control circuit that sensed when the rotor magnet was horizontal and then reversed the current in **aa**′ of Fig. 30.58.

The traditional "H-" bridge switching circuit shown in Fig. 30.59 does that very effectively. Switch drive logic must ensure that either S1 and S4 are on, or S2 and S3 are on and never S1 and S2 simultaneously or S3 and S4 simultaneously. This simultaneous operation would provide a short circuit. When this happens due to errors in the switch drive signal it is called "shoot through." There are generally important parts of the switch drive signal logic, discussed later, which try to make this impossible in normal operation.

In real motors, the permanent-magnet rotor field does not change instantaneously from north to south as the rotor rotates, so there would be reasonably large angles over which the torque could not be effectively produced. Also, more coils are put in so that the space of the machine frame is used more efficiently.

The use of three "phases," as in Fig. 30.60, is very common. There are many things that balance naturally in a three-phase system, and it is the simplest system with which it is possible to develop constant and unidirectional torque at all times and positions.

A very common method has developed, known as "six-step switching." In this system, three phases are used. They are connected in star, and there is a space between each of the magnet poles on the rotor, and the two phases are activated at any one time, the third "resting" as the space between the magnet poles passes over it.

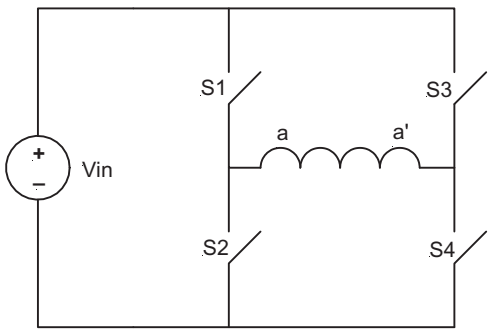


FIG. 30.59 An "H-" bridge circuit that can reverse the current through aa′, as drawn with mechanical switches.

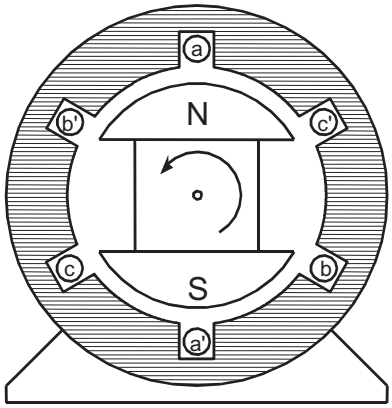


FIG. 30.60 The physical layout of a three-phase PMBDCM.

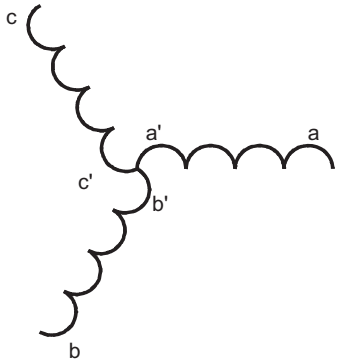


FIG. 30.61 The schematic connection of the windings shown in Fig. 30.60.

While the motor in Fig. 30.60 looks just like a three-phase synchronous machine, its operation is rather different.

As stated above, the windings are invariably star connected, as shown in Fig. 30.61.

30.6.2.1 Six Step Switching Explained

Consider the coil **aa**′, as shown in Fig. 30.60 and also diagrammatically in Fig. 30.61. Current driven into the **a** terminal, coming out of the **a**′ terminal, will produce, as discussed before, flux from left to right, as shown here.



Obviously if the current direction in **aa**′ is reversed, the flux will be



Similarly if current is driven into **b** and out of **b**′, flux will result



And if it is reversed,



Finally, if current is driven into **c** and out of **c′**, flux will result

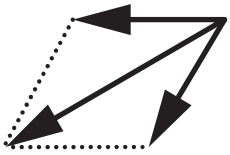


And if it is reversed,



The permanent-magnet rotor would tend to align with the flux arrow shown in each of the states above, as discussed under machine operation, Method 1.

Now, if the motor is wired in star as shown in Fig. 30.61 and a steady current is driven into **a** and out of **b**, the first and the fourth cases above occur at the same time. They add to produce a resultant,



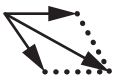
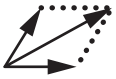
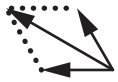
and the rotor will tend to align with this resultant.

The Hall-effect sensors are positioned so that just as the rotor gets to within 60° of being aligned, another arrangement of the windings is energized, and the field jumps forward another 60°, so the rotor is 120° away from being aligned. The rotor is always an average of 90° away from its desired position!

If a controller has input power from positive and negative of a dc supply and outputs to the terminals **a**, **b**, and **c** only, then the sequence of connections shown in Table 30.2 will produce the resultant flux directions as shown, providing continuous rotation.

The switching of Table 30.2 is simply achieved by a variant of the "H" bridge, as shown in Fig. 30.62. This process of switching current into different windings is called commutation and is the equivalent of the sliding brush contacts in a traditional brushed dc machine.

TABLE 30.2 The sequence of connections that results in counterclockwise continuous rotation of the rotor of the PMBDCM of Fig. 30.60

When rotor gets to this position, connections are made as at right	Terminal a	Terminal b	Terminal c	Flux directions
	Current in	Current out	Zero	
	Zero	Current out	Current in	
	Current out	Zero	Current in	
	Current out	Current in	Zero	
	Zero	Current in	Current out	
	Current in	Zero	Current out	

30.6.3 Current/Torque Control

You may have noted that the discussion has been about current in the windings rather than the voltage across them. In very simple small brushless DC machines, like the one in the muffin fan in your computer power supply, voltages are connected directly to the windings. For these small motors, the resistance of the windings is relatively high, and this helps limit the actual current that flows and swamps inductive effects.

There is an extra difficulty that must be addressed with high-performance, high-efficiency, well-made machines, and it adds another layer to the control of the motor. Such machines can easily be designed with very low resistance windings. It is not uncommon to have windings for a 200 V machine at the 20 kw level with the winding resistances less than 0.1Ω.

When starting or at a low speed, the current in a winding is limited only by the very low resistance, and for the machine above by Ohm's law, $I = E/R$ would result in more than 2000 A.

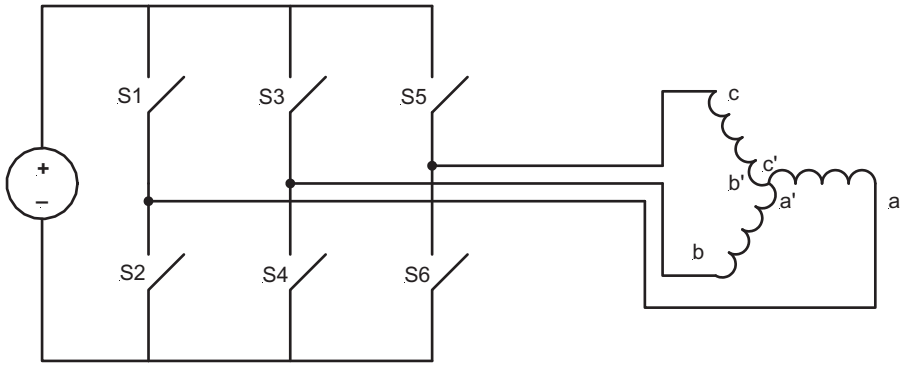


FIG. 30.62 The switching circuit used for commutation of a PMBDCM.

The most common requirement for a steady current in the windings is to provide a steady torque. There is always a back emf generated in the windings whenever the motor is rotating, which is proportional to speed and subtracts from the applied voltage. Thus, currents cannot be determined just by terminal voltage. The winding does however have inductance. Whenever the copper conductors are put in coils in an iron structure, particularly if there are low reluctance magnetic paths with only small air gaps, the creation of quite large inductances cannot be avoided. These are used to very good effect.

The nature of inductance is that when a voltage is applied to an inductor, instantaneous current does not result; rather, the current begins to increase and ramps up in a quite controlled fashion. If the voltage across the inductor is reversed, the current does not immediately reverse; rather, it ramps down, will go through zero, and reverses if the reversed voltage is left there long enough. However, if the voltage is alternated by switching rapidly, as can be done with power electronics, the current can be controlled to ramp-up and ramp-down either side of a desired current, staying within any determined tolerance of that desired current.

Figure 30.63 looks very much like the simple "H-" bridge commutation circuit but is performing a very different function. It is controlling the current amplitude to stay within a desired band. If S1 and S4 are turned on then the current will begin to increase from left to right in the winding. The current sensor in the circuit detects when the current reaches a value of half the hysteresis band of the comparator above the desired current level and initiates turnoff of S1 and S4 and turn-on of S2 and S3. (If they were all turned off at once, the inductive nature of the circuit would produce very high voltages that would cause arcing in mechanical switches or breakdown and failure of semiconductor switches; see later.) The current then begins to reduce. It reduces a small amount, down to half the hysteresis band of the comparator below the desired current level and then the switches reverse again. Thus, a desired current level is achieved, with an arbitrarily small triangular ripple superimposed, as shown in Fig. 30.64.

The general process of controlling by switching a voltage fully on or fully off at a high speed is called pulse-width modulation (PWM), and the specific method of current control

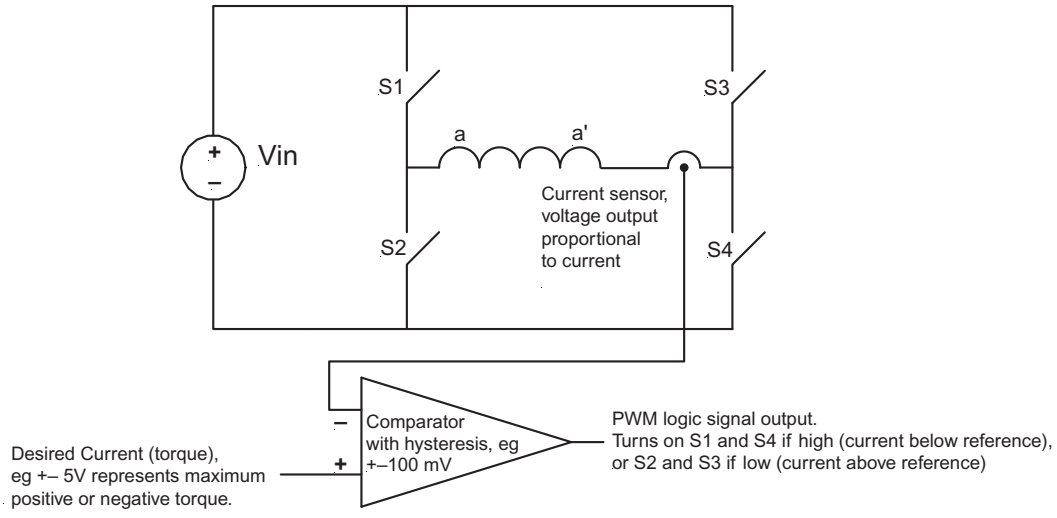


FIG. 30.63 Hysteresis band current control using pulse-width modulation (PWM).

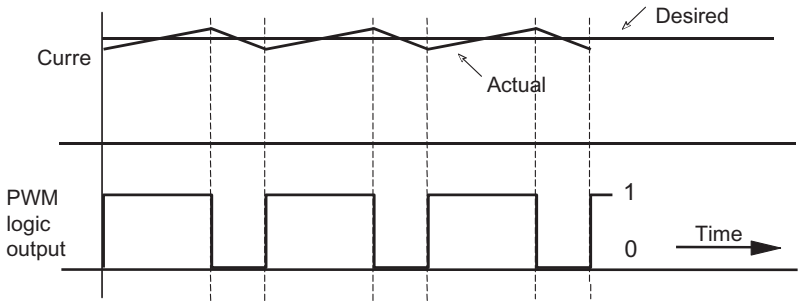


FIG. 30.64 Hysteresis band current control and PWM waveforms.

achieved above with PWM is called hysteresis band current control (HBCC).

Of course, to keep this current ripple small, the switching may need to be very fast, but with the modern semiconductor switches, there is no great problem up to 100 kHz for small machines and typically above 15 kHz for acoustic noise reasons, for machines rated up to several hundred kilowatts.

A perceived "drawback" of HBCC is that the switching frequency is determined by the circuit inductance, the width of hysteresis band, the back emf, and the applied voltage, ranging very widely in normal operation. It is not difficult, but it is a little more complicated, to use a fixed frequency, and a linear analog of the current error to modify the pulse width of the PWM signal.

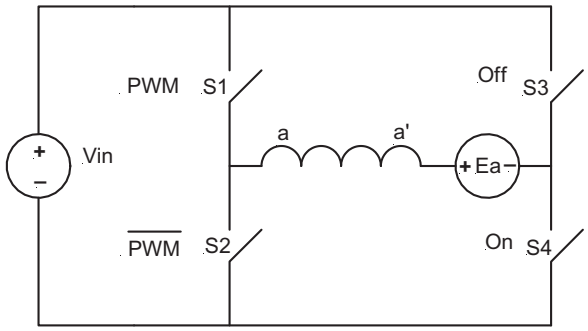


FIG. 30.65 H-bridge switching with one switch steadily on and a back emf.

30.6.3.1 Switching Losses

There is a practical limit to how often semiconductor switches can be operated. At every change of state, if the switch is carrying current as it is opened, then as the voltage rises across the switch and the current through it falls, there is a short pulse of power dissipated in the switch. Similarly, as the switch is closed, the voltage will take some time to fall and the current will take some time to rise, again producing a pulse of power dissipation. This loss is called switching loss. Fairly obviously, it will represent a power loss proportional to the switching frequency, and so the switching frequency is generally set as low as it can be without impinging on the effective operation of the circuit. "Effective operation" might well include criteria for acoustic noise and levels of vibration.

30.6.3.2 High Efficiency Method of Managing the Switching in the H Bridge

A very common way to control the current with the smallest number of switching transitions is to combine HBCC with, for example, alternating only S1 and S2 in Fig. 30.65 leaving S4 on all the time, on the understanding that there will be a back emf in the winding and the current can still be increased or decreased as desired.

Thus, when the motor is rotating and the back emf is somewhere between zero and the rail voltage, alternating two switches rather than four will still allow current control in the coil, using, for example, HBCC, exactly as before.

This is a very common control scheme and will need some extra logic to reverse the direction of rotation of the motor, either by turning S4 off and S3 on continuously or by swapping the control signals to the left and right "legs." For full-servo operation, normal H-bridge switching can be used, and the logic is slightly different, but not significantly more complicated. However, following the discussion above, the switching losses will be higher.

30.6.3.3 Combining Commutation and PWM Current Control

The real breakthrough is that one set of six switches can be used for both PWM and commutation. That is the clever part and also the confusing part when one first tries to understand what is going on.

Thus, in a controller, there are two control loops. The first is an inner current loop switching at, for example, 15 kHz to control carefully and exactly the current in two of the coils. Then, at a much lower rate, for example, at 50 times/s at 3000 rpm, the two coils doing the work are changed according to Table 30.2, controlled by an outer commutation loop, using information from the Hall-effect shaft position sensors.

A complete controller is shown in the block diagram form in Fig. 30.66. Various aspects of this block diagram will now be examined and explained in detail.

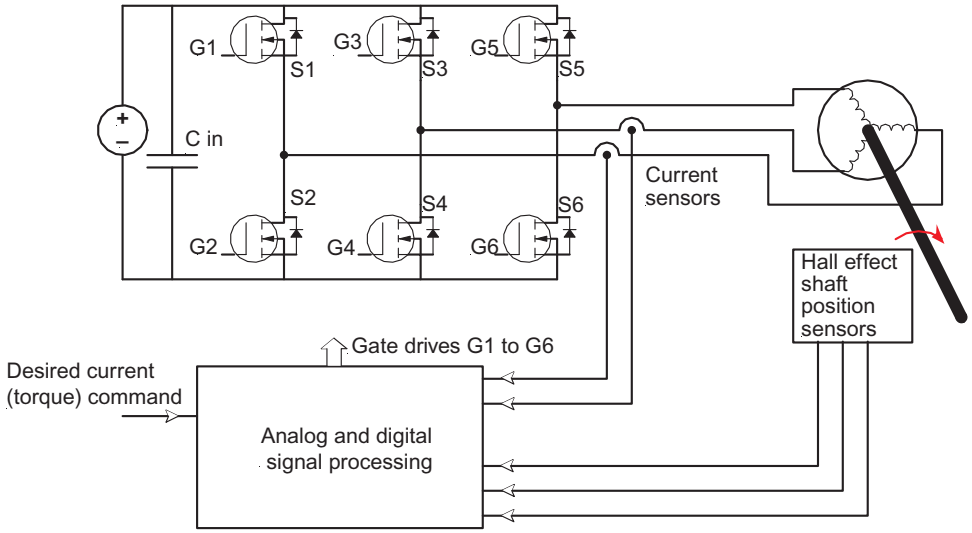


FIG. 30.66 A complete controller showing the two feedback paths, one for the position sensors and one for the current sensors.

Hardware details—semiconductor switches

The three most likely semiconductor switches for a six-step controller are the bipolar junction transistor (BJT), the metal oxide silicon field-effect transistor (MOSFET), and the insulated gate bipolar transistor (IGBT). Older controllers used BJTs; however, contemporary controllers tend to use MOSFETs for lower voltages and powers and IGBTs for higher voltages and powers. Both of these devices are controlled by a gate signal and will turn-on when the voltage of the gate above the source or emitter is greater than a threshold, which is typically about 5 V. Use of about 10 V is common. The devices are thus off when the gate voltage below the threshold. Systems typically use zero volts for the off state. The controller of Fig. 30.66 shows MOSFETs used for the six switches.

The trick is that the voltage at terminal **a**, also S1's source, is either ground or the positive potential of the battery, depending on which switches are on. Driving S2, S4, and S6 is easy since the MOSFET sources are all at the potential of the negative rail, and the lower gate drive signals are referred to this rail.

There is a range of dedicated integrated circuits that can drive the switches S1, S3, and S5 and that use a "charge pump" principle to generate the drive signal and the drive power internally, all related to the MOSFET source potential. Various approaches to this technical challenge of providing a floating gate drive are commonly discussed under the generic heading of "high-side drives."

For the most sophisticated drives, transformer coupling is used to provide a tiny power supply especially for the isolated gate drive and send the control signals either through an optocoupler or a separate transformer coupling. The high-side drive problems here are exactly the same as those encountered in the traditional buck converter or in drives for induction motors and PMSMs.

Dead time and flyback diodes

Two issues have been mentioned above that must be addressed when using high-speed electronic switches in inductive circuits.

The first, in Section 30.6.2 "Electronic Commutation," was that care should be taken to ensure that the upper and lower switches in the same "leg," (e.g., S1 and S2) are never turned on at the same time. If the controller attempts to turn one off and the other on at the same instant and switch turnoff is slower than turn-on (as it is with BJTs and IGBTs), then a short circuit will result for a brief time. The bus capacitor is usually very large to provide ripple current (see later) and usually of very high quality being fabricated especially for power electronic applications and can easily provide thousands of amperes for a few microseconds, which is enough to destroy the semiconductor switches.

The second issue, discussed in Section 30.6.3 "Current/Torque control," is that one cannot turn off both switches in a leg at the same time, even for a few nanoseconds, since the voltages resulting from attempting to interrupt current in an inductor will cause avalanche breakdown and failure of the semiconductors. This sounds like quite a dilemma.

There is actually a very simple and effective solution. At any transition, the control circuitry ensures that the active switches are all turned off before any switch is turned on, usually for a few microseconds. This is known as "dead time," and its provision is an essential part of most of the dedicated integrated circuits in use. Then, a "flyback"/"freewheel" diode is put in antiparallel with each semiconductor switch, and this provides the current path during dead time. These diodes are shown in Fig. 30.66.

The diode has a little more loss than the switch, since the diode forward drop is more than the switch drop. This is significant in a low-voltage controller. However, as stated above,

for a low-voltage controller, MOSFETs are the device of choice. They have a lesser known property, that when gated on, they can carry current in both directions. Intriguingly, the "on" state resistance is lower in reverse than in the forward direction! Thus, for low-voltage controllers, when the switch forward drop represents a significant contribution to losses, the MOSFET is turned on after dead time for both the current directions. Thus, the higher loss in the diode is only for a few microseconds.

It is not difficult to produce from the PWM signal an "I up" logic signal that is used to cause the current to increase and an "I down" logic signal used to decrease it, with the timing as shown in Fig. 30.67. The function can be executed in sequential logic, or with the simple analog timing circuits.

A. Semiconductor Detail

In MOSFETs and most IGBTs, there is a diode already within the device; it is unavoidable and results from the fabrication processes. In modern power semiconductors, this intrinsic diode is optimized to be a good switching diode. The serious designer, however, will check the specifications for reverse recovery of this diode, since in highly optimized controller designs, reverse recovery losses in the intrinsic diode can be significant and are very difficult to control. In low-voltage controllers, you can put a Schottky diode in parallel with the intrinsic body diode. The Schottky diode, with its lower forward voltage drop, will tend to take the current and has no reverse recovery problems, but the current must commutate to it from the semiconductor die, and the inductance of the connections is critical.

B. The Smoothing Capacitor on the Input to the Controller

This is a substantial capacitor, often very expensive, (it is shown in Fig. 30.66 as C in), and its design is quite challenging. The issue of smoothing is quite serious. If there are high frequencies or sudden current changes in the leads from the dc supply to the controller, they will radiate electromagnetic energy. Good design will limit the length of conductors in which the current is changing rapidly. Thus, a very large capacitor is placed physically as close to the positive bus of the switches as possible, aiming to have a steady current in the longer conductors from the dc supply, up to the capacitor. When the motor is running at, say, half speed and providing large torques, a very high level of ripple current is carried by this capacitor. Kirchhoff's current law (KCL) must be applied at node A, as shown in Fig. 30.68. Good capacitors have a ripple current maximum buried away in their specification sheet. It turns out that in general, the size of the capacitor in a given design has very little to do with how much voltage ripple you can tolerate at the bus but rather is determined by the ability to carry the ripple current without the capacitor heating up and failing. It has been known that the small electrolytics in prototype controllers mysteriously explode. On searching, it is found that they are in parallel with the main capacitor and quite close to it, so they carry a lot of ripple current, then heat up and explode!

30.6.4 The Signal Processing for Producing Switch Drive Signals from Hall Effect Sensors and Current Sensors

30.6.4.1 Operation of the Hall Sensors

The flux density directly under a magnet pole can be anywhere from 500 to 800 mT with Nd-Fe-B magnets. Hall-effect (HE) sensors with a digital output, called Hall-effect switches, change state at very close to zero flux density. Thus, they will change state when the north and south poles are equidistant from

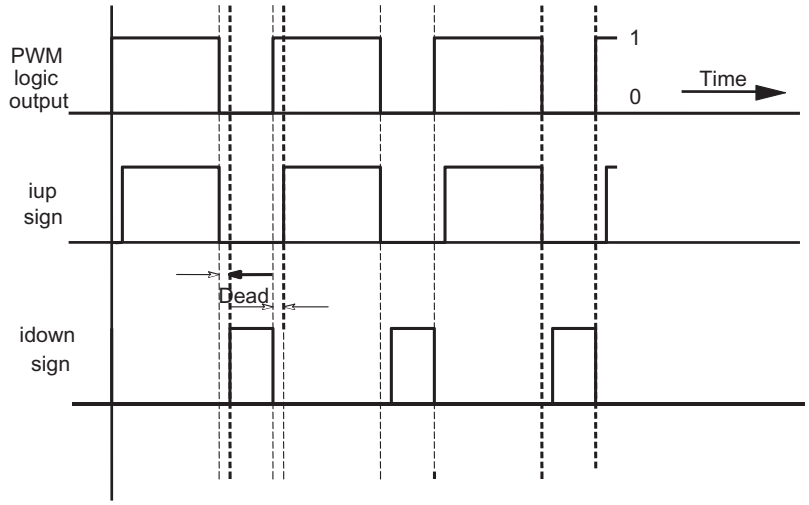


FIG. 30.67 Dead time introduced into the PWM logic signal, for switch drive.

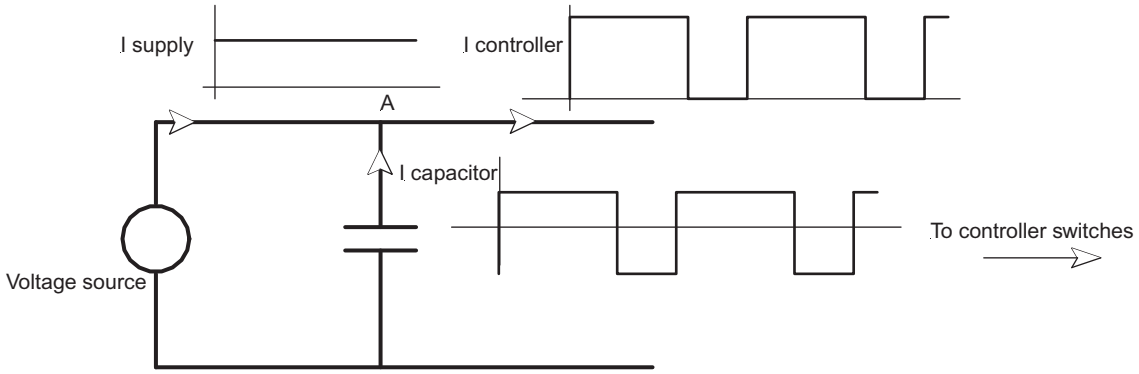


FIG. 30.68 Kirchhoff's current law at node A.

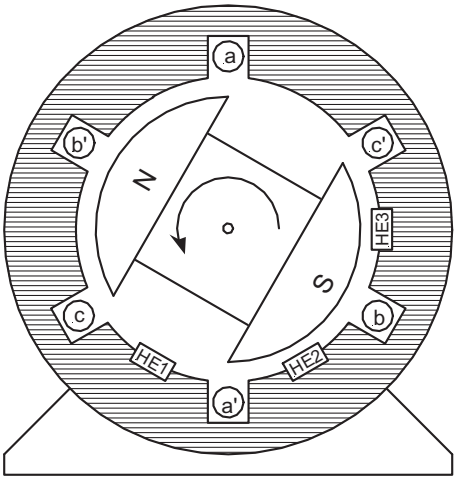


FIG. 30.69 Possible Hall-effect switch positions in a three-phase machine.

TABLE 30.3 Hall-effect switch outputs for rotor positions as shown, HE switches placed as in Fig. 30.69

When the center of the rotor north pole is in this sector	HE1 outputs	HE2 outputs	HE3 outputs
	1	0	0
	1	1	0
	1	1	1
	0	1	1
	0	0	1
	0	0	0

them, so that, for example, in Fig. 30.69, the switch HE1 is just changing state with the rotor as shown.

In practice, a motor designer needs to consider what magnetomotive force comes from the current in the windings that might result in flux that would trip the HE sensor at a slightly different time. If you follow all the above logic about six-step switching, you will see that you only need the magnet poles to have a span of a bit more than 120°. Using 180° magnet poles can add considerably to the cost and have an impact on such things as cogging torque. Actual designs often add extra "sense" magnets to cover 180° just at the circumferential strip where the HE switches are located, adding minimally to the magnet mass and ensuring good and accurate triggering.

However, if the switches operate as above, then Table 30.3 will result for the HE switches located as shown in Fig. 30.69.

30.6.4.2 Sensing the Current in the Motor Windings

Fig. 30.66 shows two current sensors. In the most sophisticated systems, there are two current sensors, one in each of the two motor phases. The current sensing is done at the winding and isolated either with a HE sensor in a soft ferromagnetic magnetic core surrounding the conductor (commercial items are available) or by using a resistive shunt sensor and some accurate analog signal isolation/coupling through transformers or optocouplers. The isolation is necessary since the potential at points **a**, **b**, and **c** is either the dc bus voltage or zero, depending on which switches are on, so that any current measure such as the small voltage across a shunt is superimposed on these very

large voltage changes. This is a very similar problem to that for the high-side gate drives discussed earlier. The current in the third winding is determined by the algebraic application of KCL, given the other two readings.

Simple controllers sometimes avoid the complexities of isolated current measurement and instead measure the current in the return negative supply, for example, from the bottom of the three lower switches to the bottom of the supply smoothing capacitor. This arrangement senses current when an upper and a lower switch is on, but not when the current is being carried in flyback diodes or by two lower switches. While it is inexpensive, it does not provide fully accurate control. The system works because the current should be decreasing when a measure is not available, heading toward zero, so switch or system failure due to overcurrent should not occur.

30.6.4.3 Management of Current Sensing

The controller must select the right current to increase or decrease, dependent on rotor position. The following convention is adopted. Positive current provides torque in the counterclockwise direction and therefore goes into winding **a**, **b**, or **c**.

All systems are capable of regeneration, which implies that negative torque can be commanded (without reversing the direction of rotation) to make the machine operate as a generator, developing retarding torque.

Thus, for the above sequence of sector determinations, referring back to Table 30.2, the output of current sensors should be directed to the current controller as shown in Table 30.4.

The addition and negation required can be carried out with the standard operational amplifier circuitry. The three required analog measures are then fed to a three to one analog multiplexer, gated from the HE switch signals suitably processed in combinational logic. The resulting single analog output is fed to the current comparator.

30.6.4.4 Distribution of Control Signals to the Switches

Given that the dead time is introduced elsewhere in sequential logic, or with timing circuits, it is a simple matter to develop the combinational logic for directing, or steering, the switching signals to the right switches. A typical scheme for a specific controller is shown in Table 30.5.

It is usual also to include some shutdown logic from dedicated protection circuits, for example, sensing overcurrent, overbus voltage, undervoltage for gate drive, and overtemperature both in the motor and in the controller power stage. For simplicity, this is not shown in the table.

TABLE 30.4 Current sensors to use as input to the current controller, for each of the six rotor-position sectors

Hall-effect switch outputs (HE1, HE2, and HE3)	Monitor current as read by
100	Negative of (sensor a + sensor b)
110	Negative of (sensor a + sensor b)
111	Sensor b
011	Sensor b
001	Sensor a
000	Sensor a

TABLE 30.5 Distribution of control signals to the switches using "high-efficiency method of managing the switching in the H bridge"

HE states (1,2,3)	S1	S2	S3	S4	S5	S6
100	I up	I down	0	1	0	0
011	0	0	0	1	I up	I down
001	0	1	0	0	I up	I down
000	0	1	I up	I down	0	0
100	0	0	I up	I down	0	1
110	I up	I down	0	0	0	1

30.6.5 Summary

30.6.5.1 What is Discussed in the Above

The physical principles of the operation of a PMBDCM have been discussed that lead to the development of the necessary parts of a power electronic controller. One specific type of current control, hysteresis band current control was explained in detail, and one specific type of switch logic pattern was developed. The exposition has included many of the issues that can cause difficulties for controller designers if they are not careful.

30.6.5.2 What is Not Discussed in the Above

Many PMBDCMs have more than one pair of poles. The arguments above can all be extended to higher pole count machines, by taking any mention of degrees to be electrical degrees rather than mechanical degrees. The controller discussed in detail only manages one direction of rotation. It is an excellent exercise and straightforward, but not trivial, to repeat the above steps, preparing the tables for clockwise rotation of the simple machine discussed above. Then, following the discussion in the first part of Section 30.6.3 "Current/Torque Control", about H-bridge switching, prepare the logic tables again for full bidirectional control, using the I up and I down logic signals exactly as above but applying them to both "legs" determined by the rotor position. Only one form of current sensing was discussed in detail. There are many simpler schemes in use that do not have quite the flexibility and accuracy of the above but that can suit certain applications. Similarly, there are other forms of current control such as the constant-frequency linear method briefly discussed. Shaft position sensors take many forms. Adherence to the HE sensor was for simplicity and to reinforce the magnetic field aspects of the machine operation.

30.7 Servo Drives

30.7.1 Introduction

Servo drives are motor drives that operate with high dynamic response. Historically, servo drives have implied motion-control systems in which sophisticated motor design, drive, and control techniques have been employed to obtain very much shorter positioning times than is possible with conventional drive systems. Examples are in machine-tool drives, robotic actuators, and computer disk drives. The power range for these drives has typically been in the range of a few kilowatts or less. This range has steadily increased in recent years as a result of advances in magnetic materials, machine design, power and signal electronic devices, and sensors.

Apart from the fast positioning times, "high dynamic response" also means that the drive operates with the following:

1. Very smooth torque up to a very low speed
2. Very high reliability and little maintenance
3. Immunity from load disturbances

The last of the foregoing items is brought about by robust and intelligent control algorithms; the first two items are brought about by innovative and often costly motor and controller designs. As a result of these, the cost of a servo-motor drive is usually much higher than the equivalent power-rated industrial drives.

The distinctions just mentioned may be easily recognized by noting, for example, that the drives that bring material to a mill may not require high performance, but the drives that take part in shaping, milling, or reducing the material should have high dynamic response in order to increase throughput and meet the accuracy requirements of the final product.

30.7.2 Servo Drive Performance Criteria

The performance of a servo drive can be expressed in terms of a number or factors such as servo bandwidth, accuracy, percentage regulation, and stiffness. While servo bandwidth indicates the ability of the drive to track a moving or cyclic reference, the percentage regulation and stiffness stipulate the drive's static holding performance for speed or position, in the face of disturbances from the load and in the supply conditions. The servo bandwidth, specified as a frequency in hertz or radian per second, is often found from the system frequency response plot, such as the Bode diagram.

The percentage regulation of a speed-controlled system often refers to the percentage change in speed from no load to full load. In a type-zero system, this figure will have a finite value. Many systems are type zero, albeit with a high gain so that the regulation is acceptably low. For such systems, the regulation is often necessary for operational reasons. In some applications, zero percentage error is required, which calls for type 1 or integral-type control system.

The servo stiffness is similar to the percentage error mentioned earlier, but it applies mainly for the position servo. It specifies the deflection of the load from its reference position, when full load torque is applied. It is usually the slope of the deflection versus the applied load torque in rad/Nm around the reference position.

30.7.3 Servo Motors, Shaft Sensors, and Coupling

Servo drives use motors that allow the desired goals of high dynamic response to be achieved. The important parameters/attributes of a servo motor are as follows:

1. High torque-to-inertia ratio
2. High torque-to-volume ratio
3. Low inductance of the motor windings
4. Low cogging torque at a low speed
5. Efficient heat dissipation
6. Low coefficient of shaft compliance
7. Direct-coupled, high-resolution, shaft-mounted sensors for position and speed

High torque-to-inertia ratio allows fast acceleration or deceleration of the drive when motion references are changed. This is often achieved through innovative low-inertia rotor design and low inductance in the stator winding. One example of a dc servo motor is the pancake-printed armature dc motor with no iron in the rotor, as indicated in Fig. 30.70. The rotor is sandwiched between axially mounted stator poles. The commutator is also on the printed armature. Another example is the disk rotor stepping motor, also without iron in the rotor, as indicated in Fig. 30.71.

The PM ac synchronous motors with modern high-energy-density magnets in the rotor, as described in Section 30.6, are also examples where the motor designer strives to minimize the rotor inertia. Modern permanent magnets allow the required air-gap flux to be developed with a much reduced volume of the magnets, consequently reducing the diameter of the rotor.



FIG. 30.70 Pancake armature of a dc servo motor. Courtesy—printed Motors Ltd., the United Kingdom.

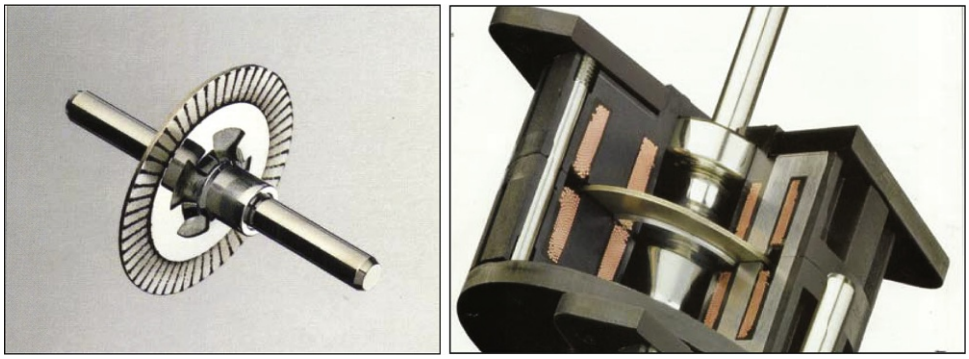


FIG. 30.71 A disk rotor stepping motor with ironless rotor for low inertia and inductance. Courtesy—Escap Motors.

It is well-known that the moment of inertia of a motor increases as the fourth power of its outer radius!

Another benefit of the modern permanent-magnet material is that the motor volume is also reduced. Servo motors often have to be located in a very confined space, and this reduction in volume is an important attribute.

The ironless designs mentioned earlier bring other benefits in the form of reduced inductance and cogging torque. Brushed pancake ironless motors are available with armature inductance as low as 100 μH.

From Section 30.2.2, the mechanical and electric time constants of a brushed dc motor are given by

$$\tau_m = \text{mechanical time constant} = \frac{R_a J}{K_E K_T} s$$

$$\text{and} \quad \tau_a = \text{electrical time constant} = \frac{L_a}{R_a} s.$$

It is well-known that for the highest load acceleration, the load inertia referred to the motor should be equal to the rotor inertia. Thus, in a matched system, the total inertia the motor accelerates is twice its own inertia. In other words, the motor inertia should also be minimized.

For a good servo motor, the ratio between the mechanical and the electric time constants is often of the order of five or more. This allows the speed and the current-control loops to be decoupled and noninteracting. The electric time constant of a motor determines how quickly the motor current may be changed and hence how quickly the torque can be changed. As also mentioned in Section 30.2, drives with a reasonable dynamic performance should have an inner torque loop. This torque loop is built around current loops, for the armature, for the brushed dc motor, or for the *d*- and *q*-axis currents for the induction and synchronous motor drives. Having a low inductance in the winding allows these currents to be followed dynamically changing current or the torque references with higher accuracy and bandwidth.

The cogging torque, if appreciable, causes the rotor to have preferential positions. As a result, the position accuracy of the motor may suffer. Another problem is the ripple in speed as the motor is operated at a low speed. At a high speed, these ripples due to cogging torque may be filtered out by the motor inertia; however, the extra loss due to cogging remains. The ironless or toothless rotor obviously produce very small cogging torque because of the absence of preferential paths for the air-gap flux to establish through the rotor iron of the brushed dc motor. The surface-magnet synchronous motor also has this feature. The interior-magnet motor normally has skewed stator slots to avoid the production of cogging torque.

Servo motors often operate with frequent start-and-stop duty, with the fastest allowable acceleration and deceleration during which the motor current is allowed to reach about 2–3 times the continuously rated current. The increased I^2R loss in such duty must be dissipated. This calls for adequate cooling measures to be incorporated in the motor housing. With such operation, it is sometimes possible to excite the mechanical resonance due to shaft compliance. This is avoided through proper arrangement of the shaft position/speed sensor and the coupling between the motor and the sensor. A belt-driven speed sensor may be acceptable for an industrial drive; however, for servo applications, a rigid, direct-coupled sensor mounted as close as possible to the motor armature is preferable. Additionally, the speed sensor is also required to have negligible noise. Speed signal from analog tachogenerators, which were used for speed sensing until recently, invariably needed to be filtered to remove the cyclic ripple/noise that existed. Such filtering often limits the maximum speed-control bandwidth of a drive.

30.7.4 The Inner Current/Torque Loop

The inner current loops in a servo-motor drive play a more important role than just limiting the current in case of overload. These loops operate continuously to regulate the motor-developed torque so as to meet the load demand, and for meeting the speed trajectory specified by the motion controller. Motor drives of high dynamic response currently employ PWM current sources. These sources use MOSFET or IGBT switching devices that allow the modulator to be operated with a switching frequency between 10 and 25 kHz. At these

frequencies, the inherent switching delay, which is equivalent to half of the PWM switching period, is made rather small for the bandwidth of the torque-control loop. The bandwidth of the current-control loops closely represents the bandwidth of the torque control. This is because the motor-developed torque generally is proportional to these currents. Servo drives up to a few kilowatts presently have torque-/current-control-loop bandwidths in excess of 1 kHz.

For higher power, fast-response drives, such as those used in the metal-processing industries, thyristor converters have been used for many years. The switching frequencies of these converters are rather low, being some multiple of the mains frequency, according to the converter chosen. Fortunately, the larger mechanical time constant of the larger power motor and the nature of the applications have allowed the 300 Hz (360 Hz in the United States) switch frequency of the three-phase thyristor bridge converter to be used satisfactorily in many applications requiring high dynamic response. The growing availability of faster and higher power IGBT devices is continually enhancing the dynamic performance of larger drives.

Fast-response, inner torque-control loops have in recent years been extended to ac induction and synchronous motors. These motors were hitherto considered only for industrial drives. The vector methods described in Sections 30.3 and 30.4, which employ inner quadrature axis current controllers in the synchronous (for the induction motor) or the rotor (for the synchronous motor) reference frame, have transformed the prospects of ac motor drives in servo applications.

Because of the fast dynamic response requirement of servo drives, the servo motor is nearly always driven with the maximum torque per ampere (MTPA) characteristic. Field weakening is normally not used. In other words, field control either directly for a brushed dc motor or a synchronous motor or indirectly through armature reaction (i.e., through i_d current control) for induction, or PM ac synchronous motors is not used for field weakening. It is nevertheless used for regulating the field at the desired level. Field weakening are mainly used for drives where the operation at higher than base speed with constant-power characteristic is desirable.

30.7.5 Sensors for Servo Drives

Servo drives require high-bandwidth current sensors for the inner torque loop and high-accuracy, noise-free speed and position sensors for the outer loops. The current sensor is often a Hall device with an amplifier, which can have bandwidths as high as 100 kHz. The inner current loop both limits and continuously regulates the motor current in all operating modes of the drive, including acceleration and deceleration. About 2–3 times, the continuous rated current of the motor is tolerated during acceleration and deceleration. This entails limiting the speed controller output to the level corresponding to the current sensor output for the limiting values of motor currents.

The current-sensor output has to be filtered to adequately remove the switching frequency noise. Otherwise, certain switching devices in converter may be overloaded. This task is more important for the thyristor converters for dc drives for which the switching frequency is rather low. This filtering of the current-sensor output limits the bandwidth of the current-control system, that is, the inner torque-control loop.

Performance of servo-motor drives depends critically on the noise and accuracy of the speed and position sensors. Synchro resolvers with 12-bit or higher digital accuracy were used in many servo-drive systems until recently. The advent of cheaper incremental and absolute optical encoders has altered this situation completely. These digital sensors are actually position sensors. The speed information is derived from positions measured by discrete differentiation. Such differentiation is not feasible with analog position sensors, because of the noise.

Analog tachogenerators are also avoided for speed servo systems. This is because of the tachogenerator ripples inherent in the sensor.

Modern discrete position sensors provide for virtually noise-free speed and position sensing. This allows very fast dynamic response to be achieved if the switching frequency of the converter allows it.

30.7.6 Servo Control-Loop Design Issues

30.7.6.1 Typical Controllers

Proportional controller

A proportional controller provides for a straight gain to amplify the error signal. It has no discriminatory properties. With the input and feed-resistance values indicated in Fig. 30.72, the total gain of the controller is $(K+1)$.

$$\text{For this controller,} \quad v_c = (K+1)(\theta_i - \theta) \tag{30.79}$$

Transient velocity feedback controller

It is well-known that a following error will exist in the preceding system when a moving or ramp reference is tracked. If a rate feedback, such as the speed feedback in a position-control system, is used to damp the system, this error is further increased.

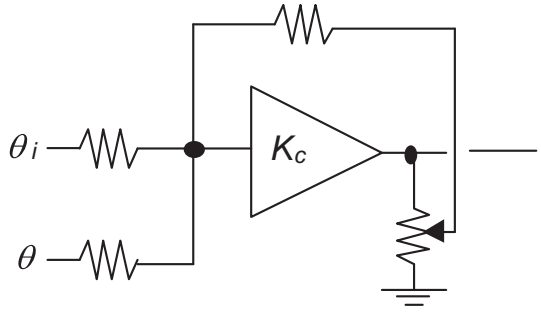


FIG. 30.72 Proportional controller.

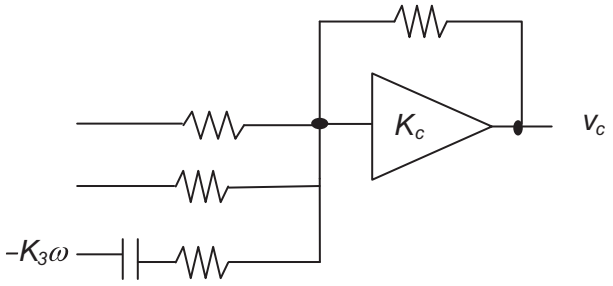


FIG. 30.73 Transient velocity feedback controller.

To overcome this following error due to velocity feedback, transient velocity feedback can be used as indicated in Fig. 30.73.

The speed (velocity) signal is passed through an RC circuit at the input of the amplifier circuit. An input current occurs only when the speed signal changes. In the steady state, the capacitor is fully charged, so that no following error in the steady state due to the velocity feedback can exist.

In the steady state when the velocities are equal, the output may lag or lead depending on the relative values of R_1 and R_2. It can be shown that in the absence of frictional load torque, as is often the case in servo applications, no following error is introduced if $R_1 = R_2$.

Integral controller

In the transient-velocity and error-rate feedback schemes, the following error will exist if viscous friction and load torque are present. If such loads are present, the system gain has to be infinity to have a zero error. Very large gains will make any physical systems unstable, unless bandwidth limitations exist. One way to employ infinite gain in the steady state is to use an integrator. This amplifies the steady-state error until it is eliminated.

Normally, a proportional plus integral (PI) action is used. A derivative term is normally not used in the control system of a drive system, since the drive feedback signals are very noisy. Instead, derivative signals are obtained through sensors such as tachogenerators. The structure of a PI controller is indicated in Fig. 30.74.

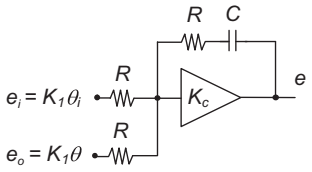


FIG. 30.74 Integral controller.

It can be shown that there will be no steady-state error even in the presence of frictional or other load torque.

Many types of more complex controllers are available, such as the variable structure controller. Drives with fuzzy controllers have also been in the marketplace for some years.

The controller circuits just described are usually implemented in analog circuits using operational amplifiers. Digital implementations are also being gradually introduced using the embedded microcontrollers and digital signal processors.

30.7.6.2 Simplified Drive Representations and Control

Consider the block diagram of Fig. 30.75 in which the individual elements (blocks) are represented in terms of their transfer functions in terms of the Laplace operators.

Here, $G_A(s)$, $G_C(s)$, $G_L(s)$, $H_T(s)$, and $H_F(s)$ represent the transfer functions of the power converter plus the motor, the controller, the load, the sensor (of speed in this example), and the filter following the sensor, respectively. The reference input for speed and the feedback signal are connected to a summing junction of an operational amplifier through resistors R_i and R_f, respectively.

The preceding system can be simplified to that shown in Fig. 30.76 and further to that in Fig. 30.77.

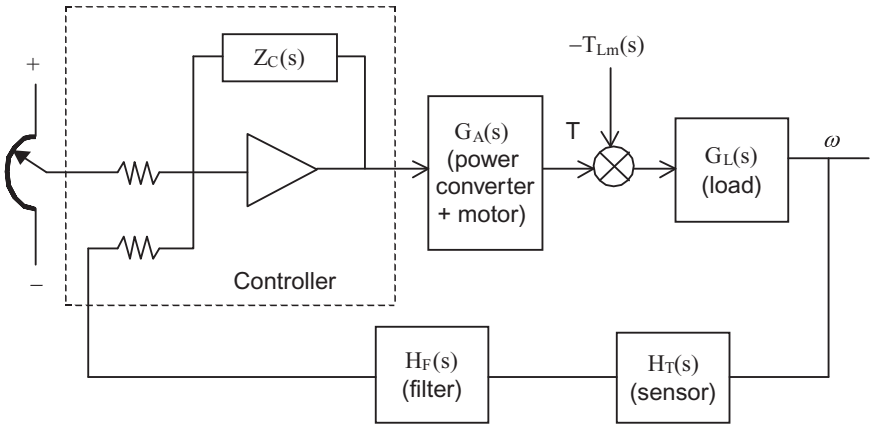


FIG. 30.75 Block diagram of a speed-control system.

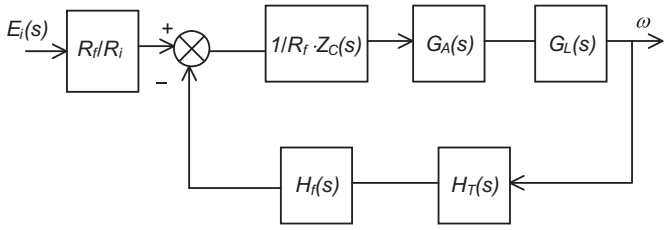


FIG. 30.76 Simplified representation of Fig. 30.75.

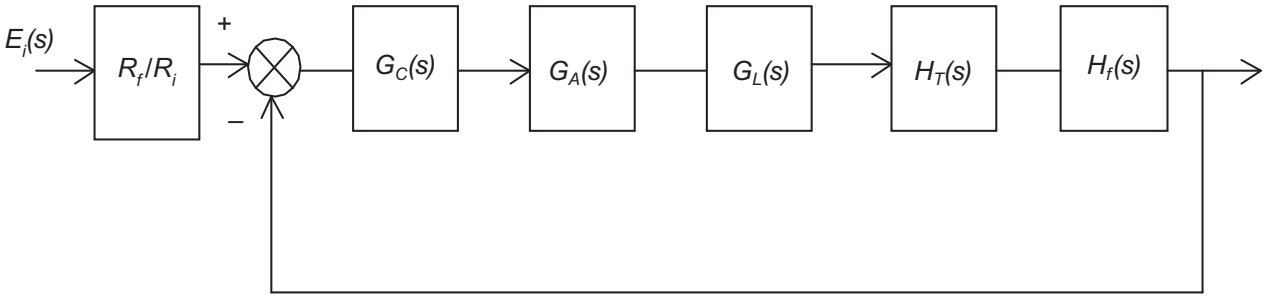


FIG. 30.77 Further simplified representation of Fig. 30.75.

In general, if the individual control blocks are approximated as first-order systems and are mutually decoupled, meaning that each block operates in a frequency band that is far outside the frequency bands of all other blocks, then the foregoing systems can be represented by a transfer function of the form

$$G_1(s) = \frac{K}{(1+sT_1)(1+sT_2)(1+sT_3)(1+sT_4)\cdots} \tag{30.80}$$

When T_3 and T_4 are much smaller time constants than T_1 and T_2, the preceding may be approximated by

$$G_1(s) \approx \frac{K}{(1+sT_1)(1+sT_2)(1+sT_s)} \tag{30.81}$$

where $T_s = T_3 + T_4 + \cdots$. A dc-motor speed-control system with current and speed sensors falls in this category. For such a system, there exist two dominant time constants (poles).

For such a system, a proportional plus integral controller is of the form

$$G_c(s) = \frac{(1+s\tau_1)(1+s\tau_2)}{s\tau_0(1+s\tau_{F1})(1+s\tau_{F2})} \tag{30.82}$$

One optimization criterion (Kessler's) stipulates that $\tau_1 \approx T_1$, $\tau_2 \approx T_2$, and $\tau_o \approx 2KT_s$. With this stipulation, the transfer function of the complete system is given by

$$G(s) = G_1(s)G_c(s) = \frac{1}{2sT_s(1+T_s)} \tag{30.83}$$

and

$$\frac{V(s)}{V_i(s)} = \frac{G}{1+G} = \frac{1}{1+2sT_s+2s^2T_s} \tag{30.84}$$

Note that the two filter time constants τ_{F1} and τ_{F2} are included in $G_c(s)$ for the sake of its realizability. These can be relegated to frequencies far higher than the range of interest and can be ignored for further analysis of the system. For an unit step input of V_i, the output V is given by

$$v(t) = 1 - \sqrt{2}e^{-1/2T_s}\sin\left(\frac{t}{2T_s} + \frac{\pi}{4}\right) \quad \text{for} \quad t \geq 0. \tag{30.85}$$

A typical output is indicated in Fig. 30.78.

If the transfer function $G_1(s)$ has one dominant time constant $T_1(s)$, as for the field current control of a dc motor, a suitable controller is the form

$$G_c(s) = \frac{(1+sT_1)}{s\tau_0(1+sT_F)} \tag{30.86}$$

In some cases, the transfer function $G_1(s)$ is of the form

$$G_1(s) = \frac{K}{sT_1(1+sT_2)(1+sT_s)} \tag{30.87}$$

where T_s is the sum of a number of short-time constants, associated with sensors, switching frequency, and so on. The

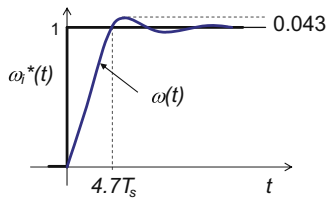


FIG. 30.78 Response of the optimized system of Fig. 30.75.

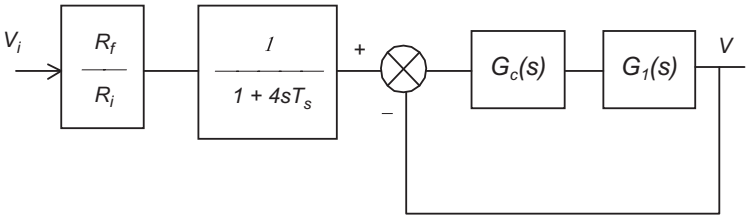


FIG. 30.79 Block diagram representation of a drive with one dominant time constant.

current controller of the dc motor with back emf has such a characteristic. A suitable PI controller for this system is

$$G_c(s) = \frac{(1+s\tau_1)(1+s\tau_2)}{s\tau_0(1+s\tau_{F1})(1+s\tau_{F2})} \tag{30.88}$$

For this system, Kessler's optimization criterion stipulates that

$$\tau_1 = 4T_s, \tau_2 = T_2, \text{ and } \tau_0 = \frac{8KT_s}{T_1}$$

The transfer function of the complete system is then

$$\frac{V(s)}{V_i(s)} = \frac{1+4sT_s}{1+4sT_s+8s^2T_s^2+8s^3T_s^3} \tag{30.89}$$

The peak overshoot of this system to a unit step unit is usually unacceptable, as indicated by the response of Fig. 30.79. This overshoot is usually reduced by inserting a first-order filter in the reference circuit. The filter network and the responses are given in Fig. 30.80.

30.8 Stepper Motor Drives

30.8.1 Introduction

A stepper motor is a positioning device that increments its shaft position in direct proportion to the number of current pulses supplied to its windings. A digital positioning system without any position or speed feedback is thus easily implemented at a much lower cost than with the other types of motors, simply by delivering a counted number of switching signals to the motor. Typically, a 200 steps-per-revolution stepper motor with 5% stepping accuracy will be equivalent to a dc motor with a 12-bit (or 4000 counts/rev) encoder plus the closed-loop speed and position controllers for obtaining similar positioning resolution. This advantage, however, is obtained at a cost of increased complexity of the drive circuits. A disadvantage of the motor is perhaps its inability to reach an absolute position, since the final position reached is only relative to its arbitrary initial position. Nevertheless, the true digital nature of this motor makes it a very suitable candidate for digital positioning systems in many manufacturing, automation, and indexing systems.

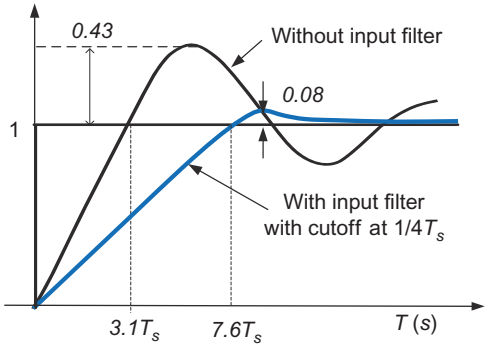


FIG. 30.80 Optimized response of the system of Fig. 30.79.

The working principle of stepper motors is based on the tendency of the rotor to align with the position where the stator flux becomes maximum (i.e., seeking of the minimum-reluctance position, also called the detent position). The rotor and the stator are both toothed structures, and the stator normally has more than two windings to step the rotor in the desired direction when they are energized in certain combinations with current. Some motors additionally have permanent magnets embedded in the rotor that accentuate an already existing, zero-excitation detent torque. These motors hold their positions even when the stator excitations are removed completely, a feature desirable for some applications.

In addition to the point-to-point stepping action, these motors can also be operated at high slewing speed, simply by increasing the pulsing rate of phase currents. Since the motor is inherently a synchronous actuator, the pulsing rate has to be increased and decreased properly, so that the rotor may follow it. At the end of a complete run, the motor always stops at the desired incremental position or angle without any accumulated error. The only error that may be encountered is mainly due to the machining accuracy of the teeth in the stator and rotor. This error is of the order of about 5% of one step position/angle, and it is nonaccumulative.

30.8.2 Motor Types and Characteristics

30.8.2.1 Single-Stack Variable-reluctance Stepper Motor

Single-stack motors are normally of the variable-reluctance type with no excitation in the rotor. The cross section of a three-phase motor with two stator poles/phase and four rotor poles is indicated in Fig. 30.81. The motor can be stepped clock or anticlockwise by energizing the phase winding in the ABCA

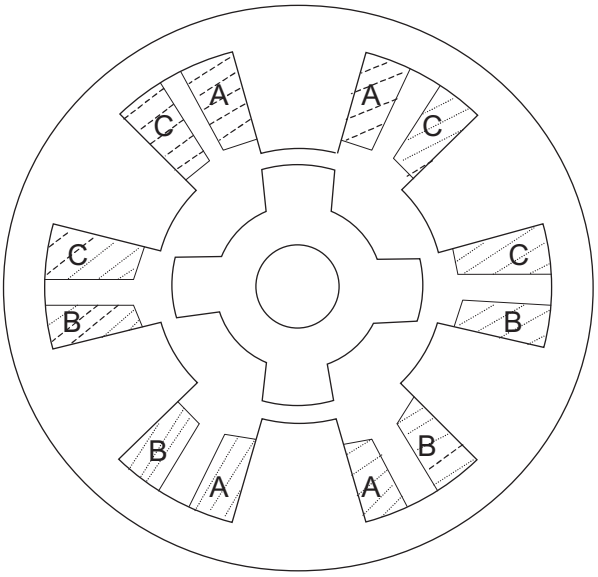


FIG. 30.81 Cross section of a single-stack variable-reluctance stepper motor.

or ACBA sequence, respectively. The step angle, that is, the angle moved by the rotor for each change in excitation sequence, of the motor is given by

$$\theta_s = \frac{360}{NP} \text{ degrees} \tag{30.90}$$

where N is the number of phases in the stator and P is the number of poles in the stator. Single-stack motors typically have larger step angles than other types because of limitations of space for the windings. The step angle of these motor tend to be larger than the multistack and hybrid stepper motors.

For each excited winding, the motor develops a torque angle ($T-\theta$) characteristic as indicated in Fig. 30.82. Note that there are two equilibrium positions of the rotor, namely, X and Y, where the motor develops zero torque.

The position X is referred to as the stable detent position, around which the rotor develops a restoring torque when displaced. The restoring torque increases as the rotor is moved from its detent position, becoming a maximum T_{max} on either side of this position. The slope of the $T-\theta$ characteristic around this detent position and the maximum torque, both of which depend on the level of excitation, indicate how far the rotor will be displaced under load torque. This means that the level of excitation also affects the position holding accuracy of the motor.

The motor may also be excited in the sequence: AB-BC-CA or AB-CA-BC for forward and reverse stepping, respectively. The two-phases-on scheme develops more torque around the detent positions at the expense of twice the resistive losses.

Yet, another excitation scheme is AB-B-BC-C-CA-A-AB for forward stepping and AB-A-AC-C-BC-B-AB for reverse stepping. In this scheme, the step size is halved as opposed to the full-step size of the previous sequences. Two different levels of torque are produced for alternate detent positions. However, the reduced step size and the more damped nature of each step may outweigh this disadvantage.

30.8.2.2 Multi Stack Variable-Reluctance Stepping Motor

In a multistack variable-reluctance motor, the stator windings are stacked along the shaft. Each stack section now has the same

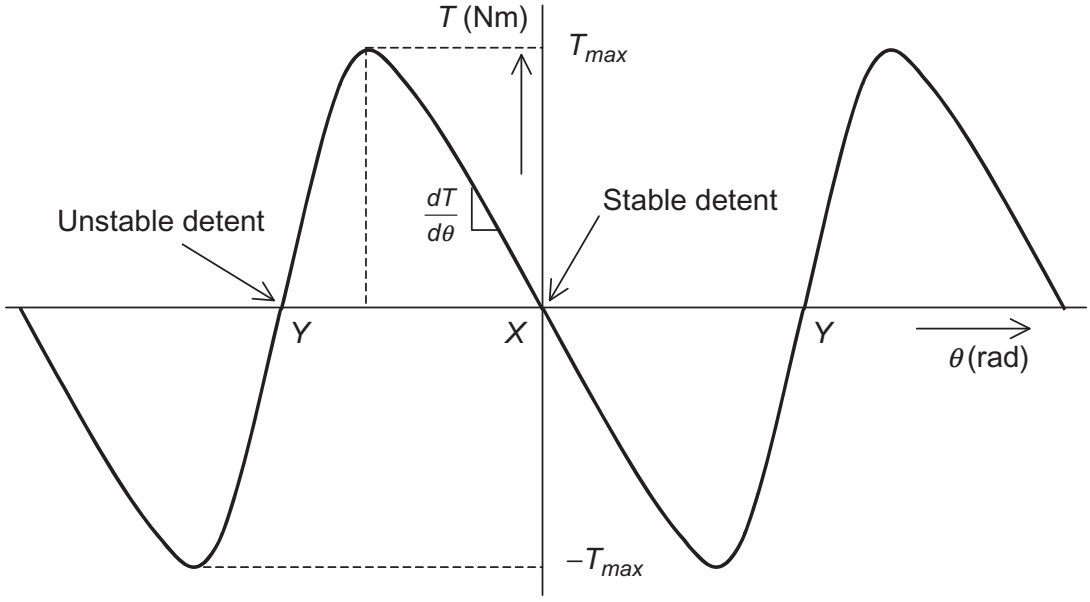


FIG. 30.82 Static torque characteristic of a stepper motor.

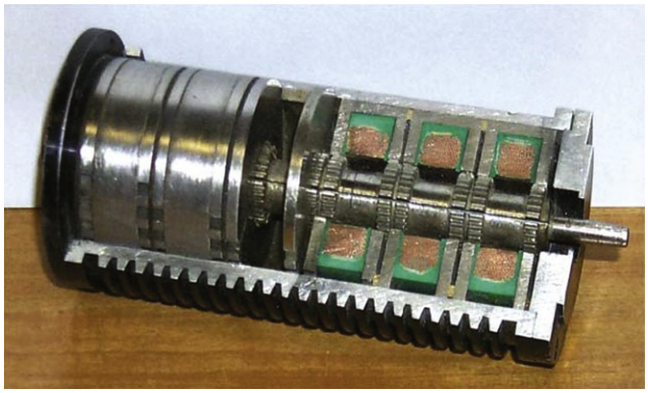


FIG. 30.83 Cutout view of a six-phase, multistack, and variable-reluctance stepper motor. Courtesy: Pratt Hydraulics, the United Kingdom.

number of poles in the stator and the rotor. Normally, each stator stack is staggered with respect to its neighbor by *one/Nth* of a pole pitch, where N is the number of stator/rotor phases or sections. The cutout view of Fig. 30.83 shows some internal details of a six-phase multistack motor, in which each stack has a phase winding between two rings, each with 32 stator and rotor poles. The step size of this motor is

$$\theta_s = \frac{360^\circ}{Np} = \frac{360^\circ}{6 \times 32} = 1.875^\circ \tag{30.91}$$

The excitation sequence of this motor is similar to the ones mentioned in Section 30.8.2.1, except that more excitation sequences are available. When a stator winding is energized, the rotor poles of that section tend to align with those defined by the stator excitation. The stator and rotor teeth in the other sections are not aligned. By changing the combination of excited phases to the next in sequence, the rotor is made to move by one step angle.

30.8.2.3 Hybrid Stepping Motor

A hybrid stepper motor has an axially oriented permanent magnet sandwiched between two sections of the stator and rotor, as indicated in Fig. 30.84. The magnetic flux distributes radially through the two stator and rotor sections, both of which are toothed, and axially through the back iron of the stator and the shaft. The stator has two-phase windings, each of which creates alternate polarities of magnetic poles in both sections of the stator. Stator windings are excited with bipolar currents, as opposed to the unipolar currents in the variable-reluctance motors of the two preceding sections. The magnetic flux produced by the stator windings not only is circumferential in each stator and rotor section but also crosses the air gap radially. It does not, however, pass through the rotor magnet. The two rotor sections are offset by half its tooth pitch.

The rotor magnet causes to the stator and rotor teeth to settle at the minimum reluctance position with a modest amount of

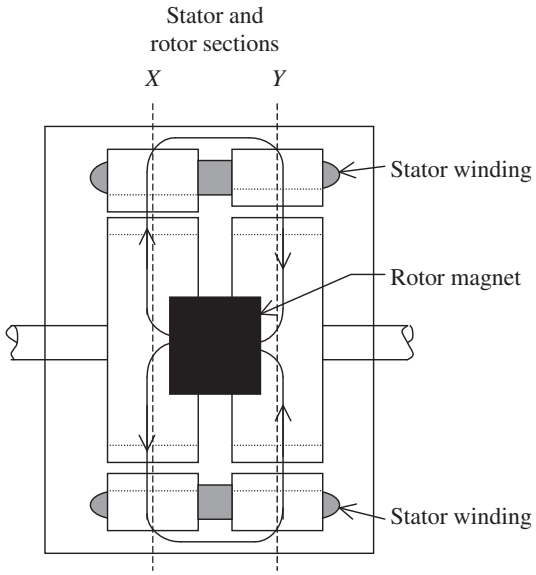


FIG. 30.84 Axial cross section of the hybrid motor.

detent torque to keep the rotor in position, when the stator windings are not energized. The rotor magnetic flux distributes outward through stator poles 3 and 7 in section X and inward through poles 1 and 5 in section Y, as shown in Fig. 30.85A and B. When the stator windings A and B (indicated as dark and faint shaded, respectively) are energized with positive and negative currents, respectively, the resulting stator flux also distributes through these same poles, so that the rotor then develops a much higher detent torque $(T-\theta)$ characteristic. The motor can be stepped forward or backward by energizing windings in sequence $A\overline{B} - AB - \overline{A}B - \overline{AB}$ or $A\overline{B} - \overline{AB} - \overline{A}B - A\overline{B}$ respectively, where the over bar indicates the polarity of currents in phases A and B.

The stepping angle of a hybrid stepper motor is given by

$$\theta_s = \frac{90^\circ}{P} \tag{30.92}$$

where P is the number of rotor poles.

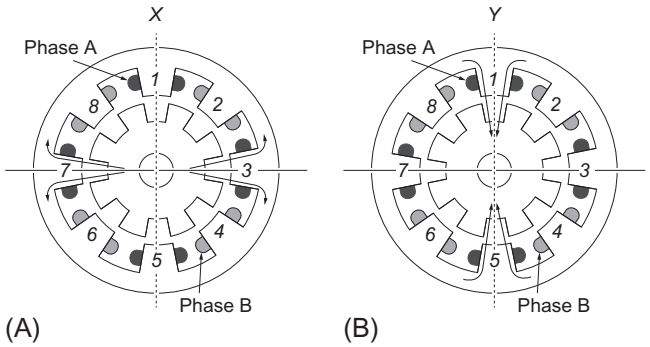


FIG. 30.85 Cross section of the hybrid motor: (A) section X and (B) section Y.

30.8.2.4 Permanent-Magnet Stepping Motor

Permanent-magnet stepper motors have alternate polarities of permanent magnets on the rotor surface, while the rotor iron, if it is used, has no teeth. In one type of construction, the rotor has no iron, and the stator consists of two windings that set up alternate poles when energized, just as in the case of the hybrid motor. The rotor consists of permanent magnets, alternately polarized, attached to the surface of a nonmagnetic disk, as shown in Fig. 30.86. The stator and rotor fluxes cross the air gap, one on either side of the disk, axially.

30.8.3 Mechanism of Torque Production

30.8.3.1 Variable-Reluctance Motor

If it is assumed that the current in the excited winding remains constant, the production of static torque of a variable-reluctance motor around a detent position is given by

$$T = \frac{dW_m}{d\theta} \tag{30.93}$$

This torque expression may also be expressed as in Eq. (30.94), when it is further assumed that the inductance of the excited winding at any given position remains constant for all currents:

$$T = \frac{1}{2} i^2 \frac{dL}{d\theta} \tag{30.94}$$

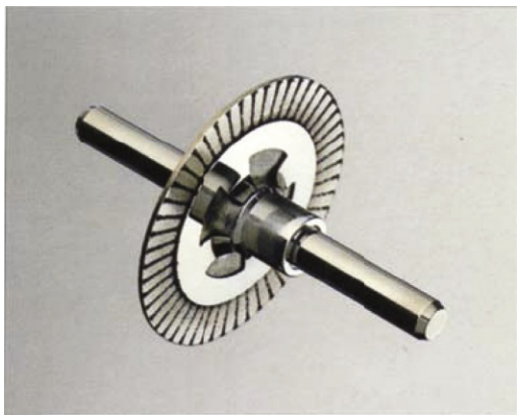


FIG. 30.86 Rotor of a PM stepper motor. Courtesy: Escap Motors.

The developed torque is due to the variation of inductance (or reluctance) with position. Note that the direction of current has no bearing on the developed torque. When the stator and rotor poles are perfectly aligned, as indicated in Fig. 30.87A, the inductance L changes little with a small change in θ. The developed torque is thus very small around this position, corresponding to the position X in Fig. 30.82. When the stator and rotor teeth are unaligned, as in Fig. 30.87B, L changes more significantly with θ, and the restoring torque becomes much larger. As θ increases, $dL/d\theta$ goes through a maximum, producing T_{max}. It should be noted that around a stable detent, L reduces as θ increases, so that the slope of the $T-\theta$ characteristic is negative at the origin. Beyond the position where T_{max} is developed, L increases as a result of the next set of rotor teeth coming under the stator teeth. This explains the drop in T_{max} and the positive slope of the $T-\theta$ characteristic in the region between where T_{max} is developed and Y in Fig. 30.82.

If stepper motors are operated in magnetically linear region where L remains constant with the current for a given angular position, the developed torque per unit volume is small. Because of this, steppers motors are normally driven far into saturation. Eq. (30.94) then does not represent the torque characteristic adequately.

For a saturated stepper motor, the calculation of the $T-\theta$ characteristic for any given current involves complex computation of stored energy, or coenergy, for each position of the rotor. This requires the magnetization characteristics of the motor for different levels of stator currents and rotor positions to be known. Reference [33] may be consulted for further reading on this.

30.8.3.2 Hybrid and PM Motors

In hybrid stepper motors, most of the developed torque is contributed by the variable-reluctance principle explained earlier. The rest is developed by the rotor magnet in striving to find the minimum-reluctance position. It should be noted that the alternate polarities of the magnetic poles created by each winding may be reversed by the direction of its current. Consequently, the polarity of the winding currents also determines the direction in which the developed torque increases positively around a detent position.

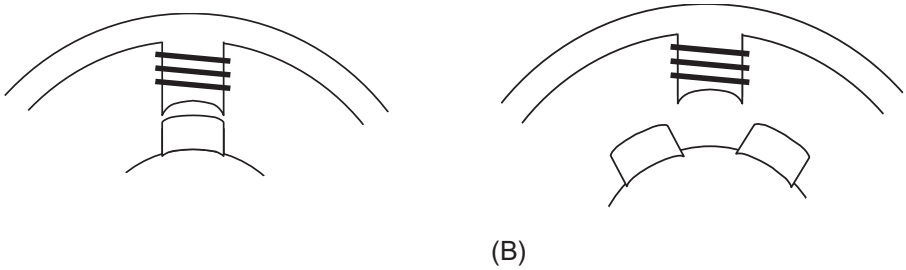


FIG. 30.87 Stator and rotor teeth alignment: (A) aligned position, $\theta = X$, and (B) unaligned position, $\theta = Y$.

30.8.4 Single- and Multi-Step Responses

When the rotor is at a detent position and phase currents are changed to a new value, the detent position is moved, and the rotor proceeds toward it and settles down at the new detent position. The movement of the rotor is influenced by the shape of the $T-\theta$ characteristic and the load friction. The rotor stepping is normally quite underdamped. The final positioning error is also determined largely by the load torque. For instance, if the $T-\theta$ characteristic is assumed to be a sinusoidal function of θ, the error in stepping is given by Eq. (30.95), where T_{max} is the peak of the $T-\theta$ characteristic and T_L is the load friction torque.

$$\theta_e = \left|\sin^{-1}(T_L/T_{\max})\right| \tag{30.95}$$

However, this error does not accumulate as further stepping is performed. If the phase currents are switched in succession, the rotor makes multiple steps. Typical single- and multistep responses are as indicated in Fig. 30.88

The maximum rate at which the rotor can be moved depends on several factors. The rise and fall times of the winding currents, which are largely determined by the electric parameters of the windings and the type of drive circuits used, and the combined inertia and friction parameters of the motor and load are important factors.

The discrete signals to step the motor in the forward or reverse direction are translated into current-switching signals for the drive circuits. This translator is a simple logical operation that is embedded in most of the integrated circuits available for driving stepper motors.

In many applications, the stepper motor is operated at far higher speeds than that it can start/stop from. The performance of a stepper motor at a high speed is normally given in terms of its pullout torque-speed ($T-\omega$) characteristic. This characteristic indicates the maximum average torque; the motor may develop while stepping continuously at a given rate. This torque is also largely determined by the parameters of the motor and its drive circuits. Fig. 30.89 indicates the typical shape of the pullout $T-\omega$ characteristic of a stepper motor drive.

At a low speed, the pullout torque is roughly equal to the average value of the positive half cycle of the $T-\theta$ waveforms of Fig. 30.82. At a high speed, the finite but fixed rise and fall

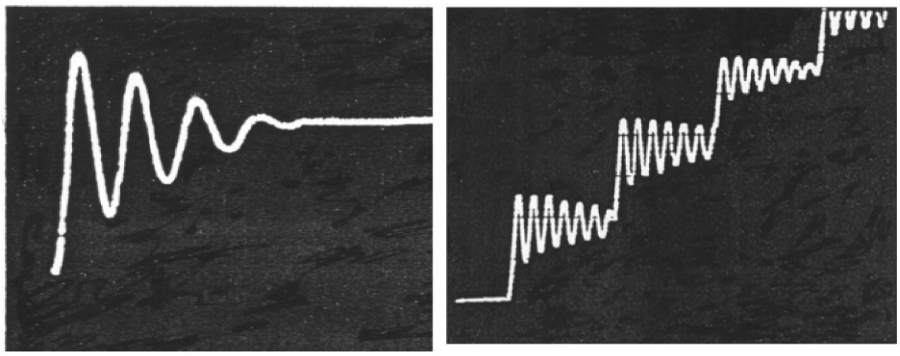


FIG. 30.88 Typical step responses of a stepper motor: (A) single-step response and (B) multistep response.

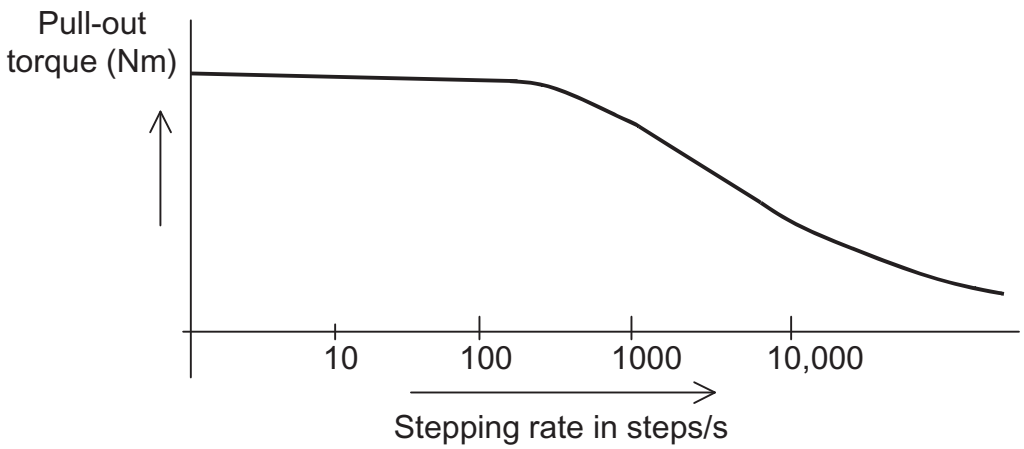


FIG. 30.89 Typical pullout torque characteristic of a stepper motor.

times of the currents and the back emf of the winding reduces the extent to which the windings are energized during each switching period. Consequently, the pullout torque of the motors falls as the stepping rate (speed) increases.

For operation at a high speed, the stepping rate is gradually increased and decreased from one speed to another. Without careful acceleration and deceleration to and from a high speed, the motor will not be able to follow the stepping commands and will lose its synchronism with the stepping pulses or winding excitations. The acceleration and deceleration rates of a stepper motor are also determined largely by the pullout torque characteristic.

Stepper motors are known to suffer from mechanically induced resonance and consequent misstepping when its switching rate falls within certain bands, which are largely determined by the way the developed torque varies with time, as the motor steps. Careful selection of stepping rate is normally employed to overcome the problem. Some shaft-mounted external damping measures may also be used when the stepping rate needs to be continuously varied, such as in the case of machine-tool profile following.

30.8.5 Drive Circuits

Two types of drive circuits are in general use for stepper motors. The unipolar drive is suitable for variable-reluctance stepper motors, for which the developed torque is determined by the level of current, not its polarity. For hybrid and permanent-magnet motors, the direction of current is also important, so that the bipolar drive circuits are more suitable.

30.8.5.1 Unipolar Drive Circuits

In its simplest form, the unipolar drive circuits, one for each winding, are as indicated in Fig. 30.90. The transistor (MOSFET) is turned on to energize the winding, with a current that is limited either by the winding resistance or by hysteresis or PWM current controllers. The freewheeling diode allows the

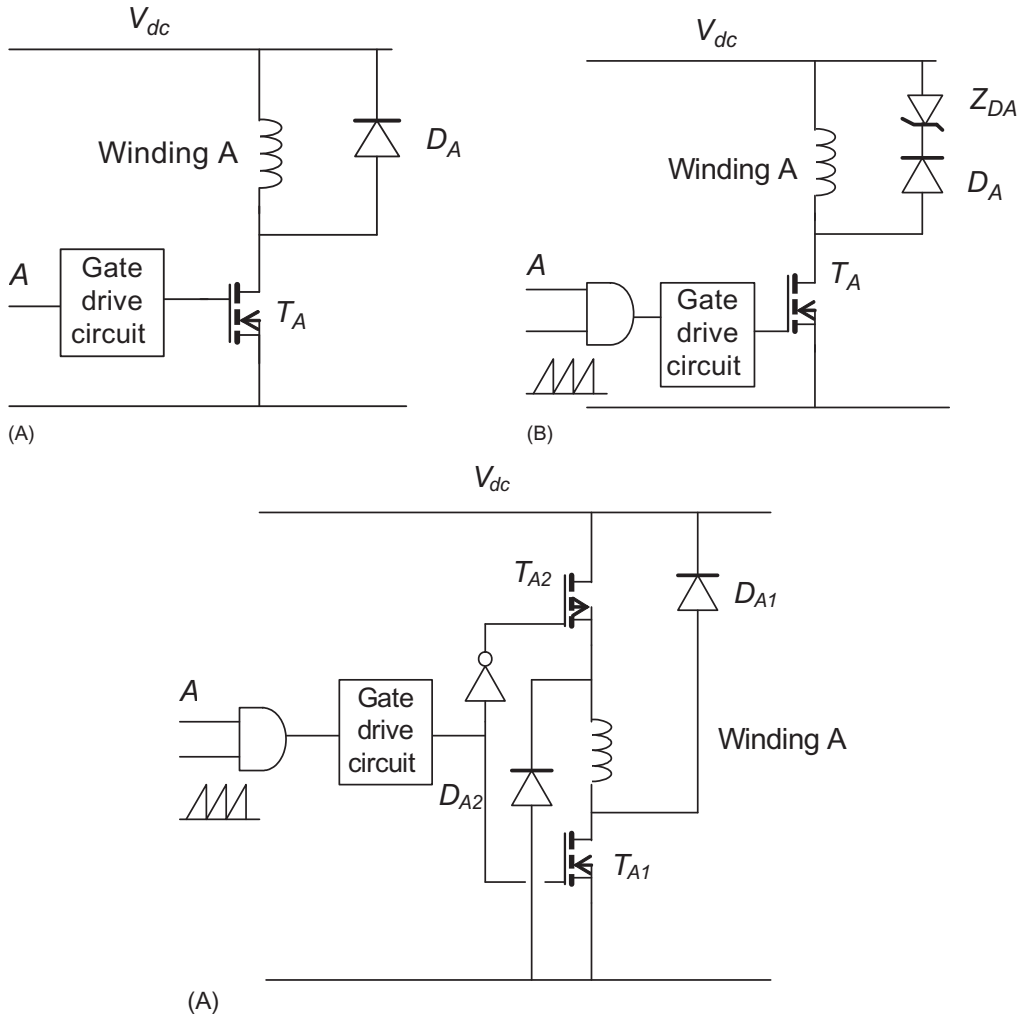


FIG. 30.90 Three commonly used unipolar drive circuits: (A) the basic unipolar drive, (B) unipolar drive with PWM current limiting and zener diode turnoff, and (C) unipolar drive with regenerative turnoff.

winding current a circulating path when the transistor is turned off.

The drive circuit of Fig. 30.90A is a basic one. A better drive circuit is shown in Fig. 30.90B, which includes a zener diode in the freewheeling path. A pulse-width modulator is also included in the gate driving circuit. The pulse-width modulator allows a higher dc supply voltage (typically 5–10 times the voltage for the resistance-limited drive) to be used, thereby reducing the rise time of current at switch on by 5–10 times. The zener diode allows a fast fall time for the current when the transistor is turned off by dissipating the trapped energy of the winding at switch-off faster. Yet another scheme is shown in Fig. 30.90C that allows the trapped energy of the winding at switch-off to be returned to the dc source when the transistor is turned off, rather than being dissipated in the winding or the freewheeling circuits. This circuit is by far the most efficient and at the same time gives the fastest possible rise and fall times for the winding currents.

30.8.5.2 Bipolar Drive Circuits

The bipolar drive allows the motor windings to be driven with bidirectional currents. The four-transistor bridge drive circuit of Fig. 30.91, one for each winding, is the most popular. The circuit can cater to the required rise and fall times of the winding by properly selecting the dc supply voltage V_{dc}, the pulse-width modulator, and the current controller gains.

Some hybrid and PM motors come with four windings, two for each phase. These may be connected in series or parallel, depending on the torque characteristics desired. In any case, only two drive circuits of the type indicated in Fig. 30.91 are required.

30.8.5.3 Drive Circuits for Bifilar Wound Motors

Hybrid stepping motors may also come with bifilar windings, which allow the simpler unipolar drive circuits to be used. These motors have two tightly coupled windings for each phase. Fig. 30.92 illustrates two bifilar windings on stator pole and their unipolar drives. The two windings on each pole have opposite sense, so that the magnetic polarity is reversed by simply switching the other winding. Since only unidirectional current is involved, the unipolar drive circuits of Fig. 30.90A or B may be used at a considerable savings in terms of the drive circuits. This benefit is, however, derived at the cost of extra winding space, and hence larger volume, for the same torque.

30.8.6 Micro Stepping

The drive sequences mentioned in Section 30.8.2 normally switch-rated current through the motor windings. These

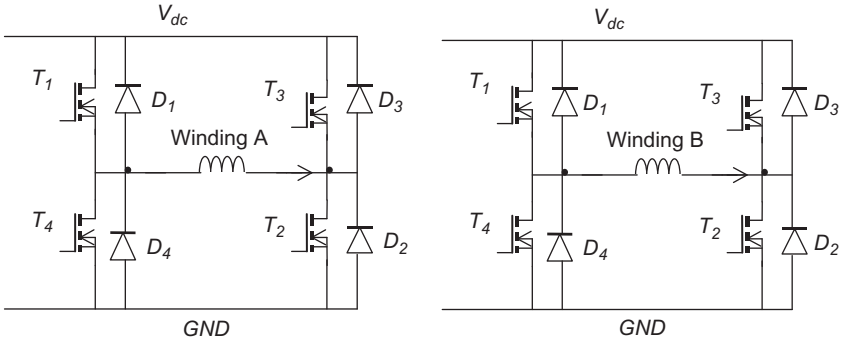


FIG. 30.91 Bipolar drive circuit (gate-drive circuits omitted).

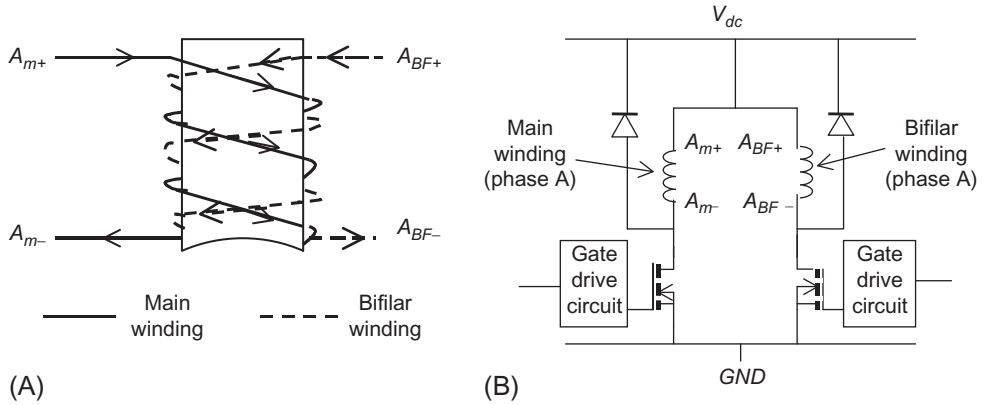


FIG. 30.92 Drive circuits for one phase of a bifilar-wound motor: (A) bifilar pole windings and (B) drive circuits.

produce regular step angles. The half-stepping operation also uses rated motor currents. Halving of the step angle is arranged mainly through the selection of the windings switched.

In microstepping, the regular step angle of the motor is subdivided further by a factor, typically from 10 to 100, by energizing the windings partially, with combinations of currents ranging from zero to full rated value in more than one windings simultaneously. This does not lead to any sacrifice of the developed torque, since the phase currents are so selected that the peak of total torque contributed by two partially energized windings is not lower than the peak detent torque T_{max} obtained in regular stepping.

The idea behind microstepping is readily understood when it is considered that by increasing the current in phase A of a two-phase hybrid in 10 equal steps to full value and decreasing the current in phase B in a similar manner, the motor step size may be divided by a factor of 10. If the closed-loop current controllers are added to the two drive circuits of Fig. 30.91 and distinct current references are obtained from a reference generator, a complete microstepping drive is realized.

In microstepping, the two current references must have values such that the motor does the following:

1. Develops the same T_{max} for every combination of winding currents
2. Develops the same torque slope, that is, $dt/d\theta$ at every microstepping detent position
3. Dissipates no more than the rated power loss (I^2R) for every combination of winding currents

The preceding conditions are necessary if the motor is to retain its static accuracy, maximum torque, and power dissipation characteristics.

The static torque characteristics (Fig. 30.92) of stepper motors are close to, but not exactly, sinusoidal functions of angle θ. The required current references for all windings of a stepper motor, including the variable-reluctance motor of three or more phases, can easily be calculated from the data of the $T-\theta$ characteristics of the motor for each phase for various currents and rotor positions. A typical set of $T-\theta$ data for a three-phase variable-reluctance motor is shown in Fig. 30.93.

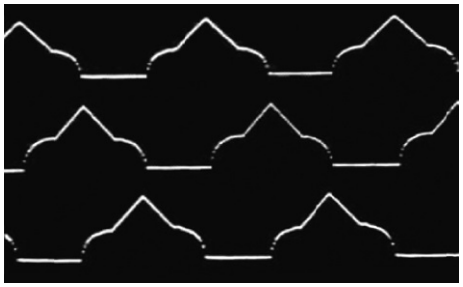


FIG. 30.94 Microstepping current references for the VR motor of Fig. 30.93. Stepping rate: 28,800 steps/s, $I = 6$ A (maximum).

The application of the three conditions mentioned earlier leads to a unique set of current references for each phase of the motor for each microstep. Fig. 30.94 shows the current references for this motor for microstepping.

In multi stepping operation, these microstepping current references have to be issued to the current controllers for each phase, at a rate determined by the commanded stepping rate.

Care has to be taken in designing the phase-current controllers so that the actual winding currents match the current references in both single- and multistepping operation up to the maximum stepping rate desired. Since the current references are time-varying, high-bandwidth current controllers are normally required to cover the desired speed range.

30.8.7 Open-Loop Acceleration–Deceleration Profiles

As mentioned in Section 30.8.4, many applications require the stepper motors to be driven far above the stepping rates to and from which the motor can start and stop abruptly without losing or gaining any step. This calls for carefully designed acceleration-deceleration profiles that the stepping pulse rate must not exceed.

The number of steps the motor is to be stepped and its direction are normally under the control of the motion controller. Once this reference is known, a digital timer/counter circuit

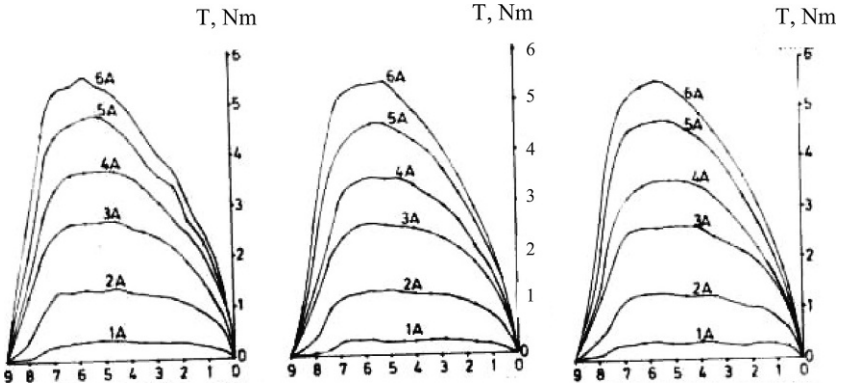


FIG. 30.93 $T-\theta$ characteristics of a three-phase variable-reluctance motor.

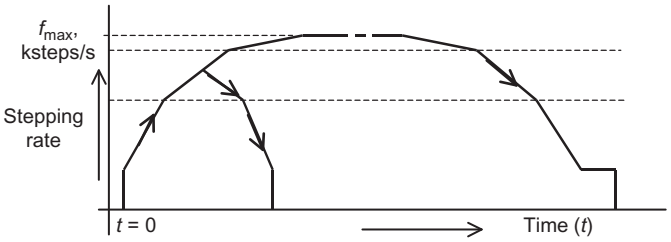


FIG. 30.95 Typical acceleration-deceleration profiles.

can be used in the controller to progressively adjust the time between the stepping pulses such that a prescribed acceleration-deceleration profile, as indicated in Fig. 30.95, is followed. The timer/counter and the pulsing sequence controller (the translator) need to be managed in real time to execute the motion-control task at hand.

The fastest acceleration-deceleration profile, a stepper motor is capable of is largely determined by its pullout $(T-\omega)$ characteristic, which in turn is determined by the motor winding parameters and the drive circuit. An optimized stepping profile to and from the top speed may have a number of segments as indicated in Fig. 30.95. These profiles are easily computed from the pullout $(T-\omega)$ characteristic by integrating the dynamic torque balance equation of the drive. For a large positioning angle, the entire profile, including some constant speed running at the top speed, may be used. For short-positioning angles, only part of the profile may be traversed. In general, a single-segment acceleration-deceleration profile is used in commercial stepper motor controllers, so as to avoid a great deal of real-time number crunching by the profile controller.

The overall stepper motor controller thus consists of the blocks depicted in Fig. 30.96.

30.9 Switched-Reluctance Motor Drives

30.9.1 Introduction

The switched-reluctance (SR) motor is a doubly salient electric machine with salient-poles on both the stator and rotor. The machine is operated by switching current pulses to each stator winding on and off in a continuous switching sequence. The rotor poles have no excitation. Fig. 30.97 shows the physical topology of a typical SR motor. The diagram illustrates a motor with eight salient stator poles (numbered A1–D2) and six

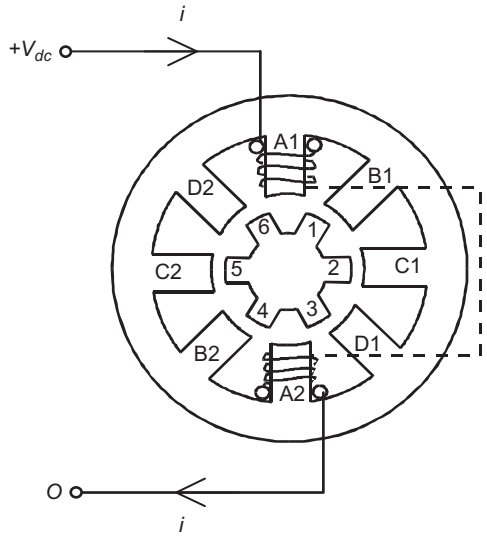


FIG. 30.97 Four-phase SR motor topology.

salient rotor poles (numbered 1–6). Although many combinations of the number of stator and rotor poles are possible, this particular type has found widespread use.

The phase windings on the stator of the SR motor consist of concentrated windings wrapped around the stator poles. In the conventional arrangement, each stator pole winding is connected with that of the diametrically opposite pole to form a stator phase. In Fig. 30.97, the connected stator pole pairs are indicated by the same prefix letter.

The general principle of operation of the SR motor is the same as all types of reluctance machines, that is, the stator and the rotor poles seek the minimum-reluctance position, so that the stator excited flux becomes maximum. Hence, when current flows in an SR motor stator phase and produces a magnetic field, the nearest rotor pole will tend to position itself with the direction of the developed magnetic field. This position, which is termed the *aligned position*, is reached when the rotor pole center axis is aligned with the stator pole center axis (assuming symmetrical poles). The aligned position also corresponds to the position of minimum reluctance and hence the position of maximum inductance.

It should be noted that the *unaligned* position is defined as the position when the *interpole axis*, or the axis of the center of the interpolar space in the rotor, is aligned with a stator pole axis.

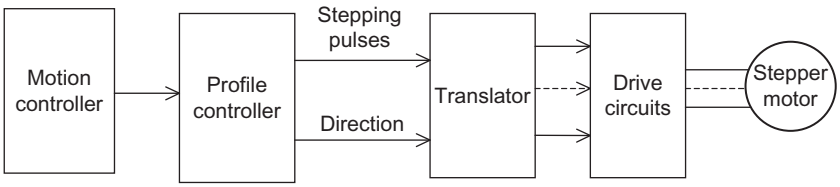


FIG. 30.96 Structure of an open-loop motion controller for a stepper motor.

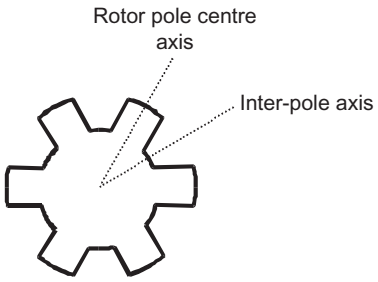


FIG. 30.98 Rotor pole axis positions.

This position corresponds to the position of minimum inductance. These rotor axis positions are illustrated in Fig. 30.98.

To achieve continuous rotation, the stator phase currents are switched on and off in each phase in a sequence according to the position of the rotor. Consider the motor schematic illustrated in Fig. 30.97. If coils A1 and A2 of phase A are excited and produce a magnetic field in a vertical direction, then poles 1 and 4 on the rotor will align themselves with the stator poles of phase A. If the coils of phase A now have their current switched off and coils B1 and B2 of phase B are now excited, then in a similar fashion, the rotor will move so that the poles 2 and 5 are aligned with stator poles B1 and B2. Exciting phases A, B, C, and D in sequence will produce rotor rotation in the counterclockwise direction.

From the preceding discussion, one may see that the switching on and off of excitation current to the motor phases is related to the rotor pole positions. This means that some form of position sensor is essential for the effective operation of the SR motor.

30.9.2 Advantages and Disadvantages of Switched-Reluctance Motors

The SR motor has a number of inherent advantages that makes it suitable for use in certain variable-speed drive applications. Nevertheless, the motor also has some inherent disadvantages that must be considered before choosing the motor for a particular application. In Table 30.6, the main advantages and disadvantages of the SR motor drive are summarized.

TABLE 30.6 Advantages and disadvantages of SR drives

Advantages	Disadvantages
Low-cost motor	Need for position measurement
Robust motor construction	Higher torque ripple than other machine types
Absence of brushes	Higher noise than other machine types
No motor short-circuit fault	Nonlinear and complex characteristics
No shoot-through faults	
Ability to operate with faulted phase	
High torque-to-inertia ratio	
Unidirectional currents	
High efficiency	

30.9.3 Switched-Reluctance Motor Variable-Speed Drive Applications

The main application for SR motors is in variable-speed drive systems. One application area has been general-purpose industrial drives where speed, acceleration, and torque control are desired. SR-motor-based industrial drives provide the advantages of a very wide range of operating speeds and high efficiency and robustness. Other applications of the SR drive include automotive applications, where the SR motor has advantages of robustness and fault tolerance. The SR motor in this application can also be easily controlled for acceleration, steady speed, and regenerative braking.

The SR motor is also well suited to aerospace applications where the ability to operate under faulted conditions and its suitability for operation under harsh environments are critical. Additionally, the very high-speed capability and high power density also make these motors well suited in the aerospace field. There are also many domestic appliances where cost is of primary concern. In these products, the SR motor can provide a low-cost solution for a brushless fully controllable motor drive. In addition, the motor can be used in battery-powered applications, where the motor-high efficiency and ability to use a dc supply are important.

30.9.4 SR Motor and Drive Design Options

The main components of the drive system are shown in Fig. 30.99. It is important to design the motor and drive together in an integrated manner. The main criteria that need to be considered in designing the components of the SR drive system will be discussed later. It will be seen that certain design choices, which may be advantageous for one component of the drive system, may bring about disadvantages in another component. This highlights the need for a careful, integrated system approach to be taken when designing the drive system.

30.9.4.1 Number of Motor Phases

There are many possibilities in choosing the number of stator phases and rotor poles in SR motors. The simplest SR motor may consist of only one phase; however, to operate the motor in four quadrants (motoring or generating in both forward and reverse directions), at least three phases are required. The most common configuration to date has been the four-phase SR motor, which has eight rotor poles and six stator poles, as was shown in Fig. 30.97.

30.9.4.2 Maximum Speed

The SR motor is capable of operating at very high speeds because of its robust rotor construction, and in most applications, the maximum speed is limited by the inverter switching speed and not limited by the motor itself. The maximum speed of the SR motor is itself normally greater than 15,000 rpm for a standard SR motor.

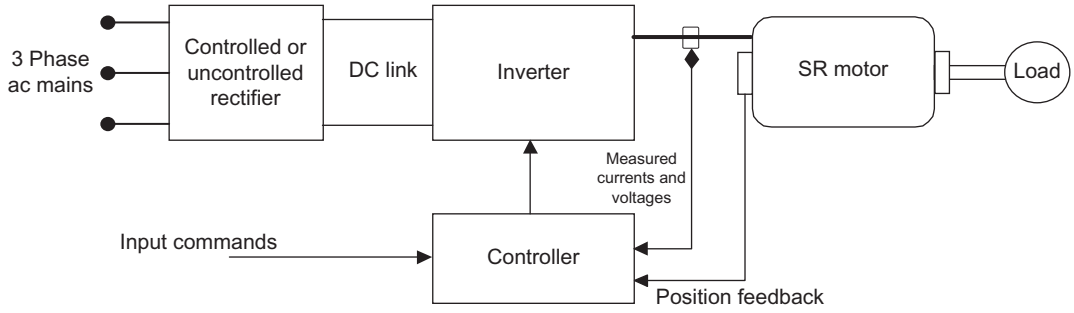


FIG. 30.99 Main components of an SR drive.

However, to determine the maximum drive speed, the controller and motor must be considered together. This is because the power-electronic device switching speed is directly proportional to the commutation frequency, which is in turn proportional to the motor speed. The maximum switching frequency of the power devices must therefore be taken into account in the SR drive design.

30.9.4.3 Number of Power Devices

In general, the number of switches per phase in SR motor drives will vary according to the inverter topology. A wide range of different SR drive circuits are available for SR drives, and these are detailed below. Circuits with only one switch per phase are possible; however, these have various disadvantages such as control restrictions, a need for extra windings, or higher switch voltages. However, with two switches per phase, the motor is fully controllable in four quadrants and has completely independent motor phase control. Therefore, the maximum number of power switches required for the motor operation is normally $2q$, where q is the number of phases.

30.9.4.4 Inverter Topology Types for SR Motors

As was mentioned, the torque produced in the SR motor is independent of the direction of current flow in each motor phase. This means the inverter is only required to supply unidirectional currents into the stator windings. The three major circuit topology types that have been used for each winding of SR motor drives are shown in Fig. 30.100. As indicated in this figure, these are commonly termed the *bifilar-*, *split-dc-supply-*, and *two-switch*-type inverter circuits.

In the circuits shown in Fig. 30.100, only one or two switching components per phase are required. Other circuit topology types that use shared components between the motor phases have limitations in control flexibility.

Bifilar type inverter circuit

In Fig. 30.100A, a drive circuit for a bifilar-wound SR motor is shown. The bifilar windings are closely coupled, with one winding being connected to a switching device, while the other is connected to a freewheeling diode. Current is increased in the winding when the switching device closes. At turnoff, the current transfers to the secondary winding through transformer action, and the inductive energy flows back into the supply via the freewheeling diode. If perfect coupling is assumed, then the voltage across the switching device will rise to twice the dc supply voltage during turnoff. However, in practice, this would be higher. This is because there will be some uncoupled inductance in the primary that will cause high induced voltages when the current in the winding collapses to zero. Thus, snubbing circuits would almost certainly be required to protect the switching components from overvoltage.

The advantage of the bifilar circuit is that it requires only one switching device per phase. However, with the advent of modern power electronic devices, which have both low cost and low losses, this advantage quickly disappears.

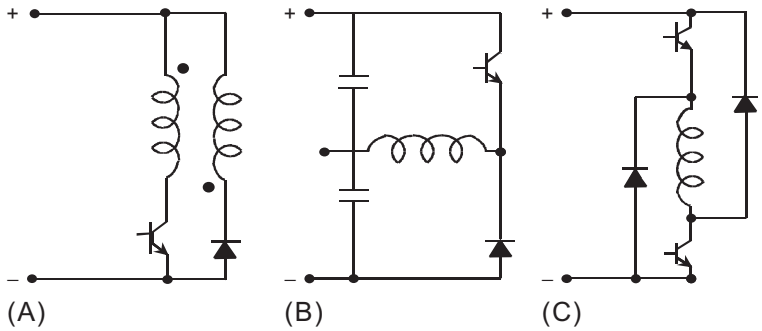


FIG. 30.100 Major SR inverter topology types: (A) bifilar type, (B) split-dc-supply type, and (C) two-switch type.

Split DC supply inverter circuit

The split-dc-supply-type inverter circuit is in Fig. 30.100B. As in the bifilar circuit, this configuration also uses only one switching device and one diode per phase. However, a center-tapped dc source is required. When the switching device is turned on, current increases in the phase winding because of the positive capacitor voltage being applied. At turnoff, the current is forced to flow through the diode and thus decays to zero more quickly because of the connection to the negative voltage. It is usual for the dc center tap to be implemented using a split capacitor in the dc-link. The voltages across each capacitor must remain balanced, which means that there can be no significant power-flow difference between the two capacitors.

Upon examination of the circuit, it can be seen that because of the split capacitor bank, only half the available dc voltage can be switched across the phase winding. Thus, for the same voltage across the motor phases that is supplied by the bifilar circuit described earlier, the dc supply voltage must be doubled with respect to the bifilar circuit supply. This means that the voltage rating of the devices would effectively be the same as in the bifilar circuit.

This is inherently inefficient. The configuration also has the need for balanced split capacitive components. In addition, it will be seen that the *soft-chopping* form of control described in Section 30.9.7 is not available in this drive.

Two-switch inverter circuit

The two-switch-inverter-type circuit, which is shown in Fig. 30.100C, uses two switching devices and two diodes per phase. Unlike the previous two circuits, three modes of operation are possible:

Mode 1—positive-phase voltage

A positive-phase voltage can be applied by turning both switching devices on. This will cause the current to increase in the phase winding.

Mode 2—zero-phase voltage

A zero-voltage loop can be imposed on the motor phases when one of the two switches is turned off while current is flowing through the phase winding. This results in current flow through a freewheeling loop consisting of one switching device and one diode, with no energy being supplied by or returned to the dc supply. The current will decay slowly because of the small resistance of the semiconductors and connections, which leads to small conduction losses. This mode of operation is used in soft-chopping control, as described in Section 30.9.7.

Mode 3—negative-phase voltage

When both switches in a motor phase leg are turned off, the third mode of operation occurs. In this mode, the motor phase current will transfer to both of the freewheeling diodes and return energy to the supply. When both of the diodes in the phase circuit are conducting, a negative voltage with amplitude equal to the dc supply voltage level is imposed on the phase windings.

In this circuit, the switching devices and diodes must be able to block the dc supply voltage amplitude when they are turned off, in addition to any switching transient voltages. However, because the circuit contains two devices in series, the blocking voltage is essentially half the value seen in the previous two circuit types for the same applied motor phase voltage amplitude. Another advantage of the two-switch inverter circuit is that it offers greater control flexibility with its three modes of voltage control.

A disadvantage of this inverter type, as compared with the bifilar and split dc supply types, is that it contains twice as many switching components per phase. However, with the current wide availability and economy of power semiconductors, in most applications, the advantages of the two-switch circuit outweigh the cost of an extra switching device per phase.

30.9.5 Operating Theory of the Switched-Reluctance Motor: Linear Model

If a linear magnetic circuit is assumed, the flux linkage is proportional to phase current for any rotor position θ. This is demonstrated in Fig. 30.101, where the magnetization curves for the linear SR motor for various rotor positions and currents are shown. In this linear case, the inductance L at any position θ, which is the slope of these curves, is *constant* and independent of current.

As the motor rotates, each stator phase undergoes a cyclic variation of inductance. As can be seen in Fig. 30.101, in the fully aligned position (when a rotor pole axis is directly aligned with the stator pole axis) the reluctance of the magnetic circuit through the stator and rotor poles will be at a minimum, and thus the inductance of the stator winding will be at a maximum. The opposite will occur in the fully unaligned position (when the rotor interpole axis is aligned with the stator pole). Thus, the inductance becomes a function of position only and is not related to the current level. If it is also assumed that mutual inductance between the phases is zero, then a typical inductance variation $L(\theta)$ with respect to the rotor position similar to that shown in Fig. 30.102 arises. Although this is an idealized inductance variation, it

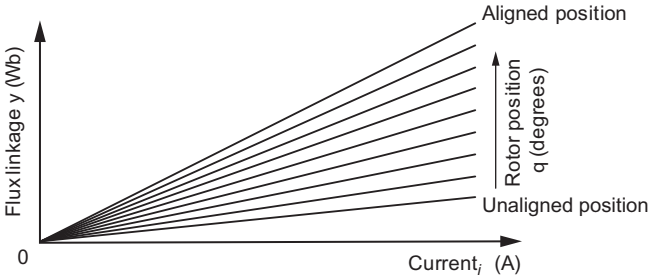


FIG. 30.101 Magnetization characteristics of linear SR motor.

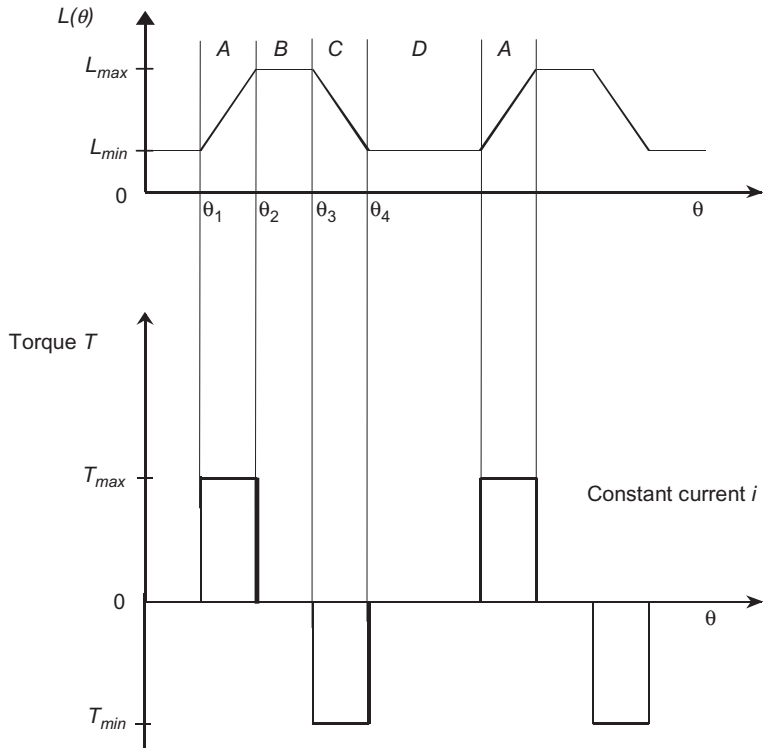


FIG. 30.102 Typical linear inductance variations and corresponding torque variations for constant phase current.

is helpful in the understanding of key operating principles of the machine. One should note that in the idealized inductance variation, there are sharp corners, which can only arise if flux fringing is completely ignored.

Four distinct regions can be identified in the plot of the linear inductance variation shown in Fig. 30.102. These distinct regions correspond to a range of rotor pole positions relative to the stator pole positions as described below:

Region A

This region begins at rotor angle θ_1, where the first edge of the rotor, with respect to the direction of rotation, just meets the first edge of the stator pole. The inductance will then rise in a linear fashion until the poles of the stator and rotor are completely overlapped at angle θ_2. At this point, the magnetic reluctance is at a minimum, and the phase inductance is at a maximum. These rotor positions are illustrated in Fig. 30.103A and B, for example, four-phase motor with rotor pole 1 approaching the stator pole of phase A.

Region B

This region spans from rotor positions θ_2 to θ_3. In this region, the inductance remains constant because the rotor pole is completely overlapped by the stator pole (i.e., the overlap area of the poles remains constant). At rotor angle θ_3, the edge of the rotor pole leaves the stator pole overlap region, and thus, the area of overlap will again begin to decrease. The position at which this occurs is illustrated in Fig. 30.103C.

Region C

When the rotor moves past θ_3, the rotor pole leading edge begins to leave the pole overlap region, and region C begins. At this point, the inductance begins to linearly decrease, until at θ_4, the rotor pole has completely left the stator pole face overlap region. At this point, the inductance is at its minimum once more. The rotor position at which the rotor pole has completely left the overlap is indicated in Fig. 30.103D.

Region D

In this region, the rotor and stator have no overlap, and thus, the inductance remains constant at the minimum level, until region A is reached once again.

It was mentioned earlier that when a stator phase is excited, the rotor poles will tend to move toward the maximum-inductance region. Thus, a motoring torque is produced when a stator phase is provided with a current pulse during the angles when the inductance is rising (assuming motoring rotation is in the direction of increasing θ in Fig. 30.102). This means that if positive torque is desired, excitation should be arranged such that the current flows between the appropriate rotor angles when the inductance is rising.

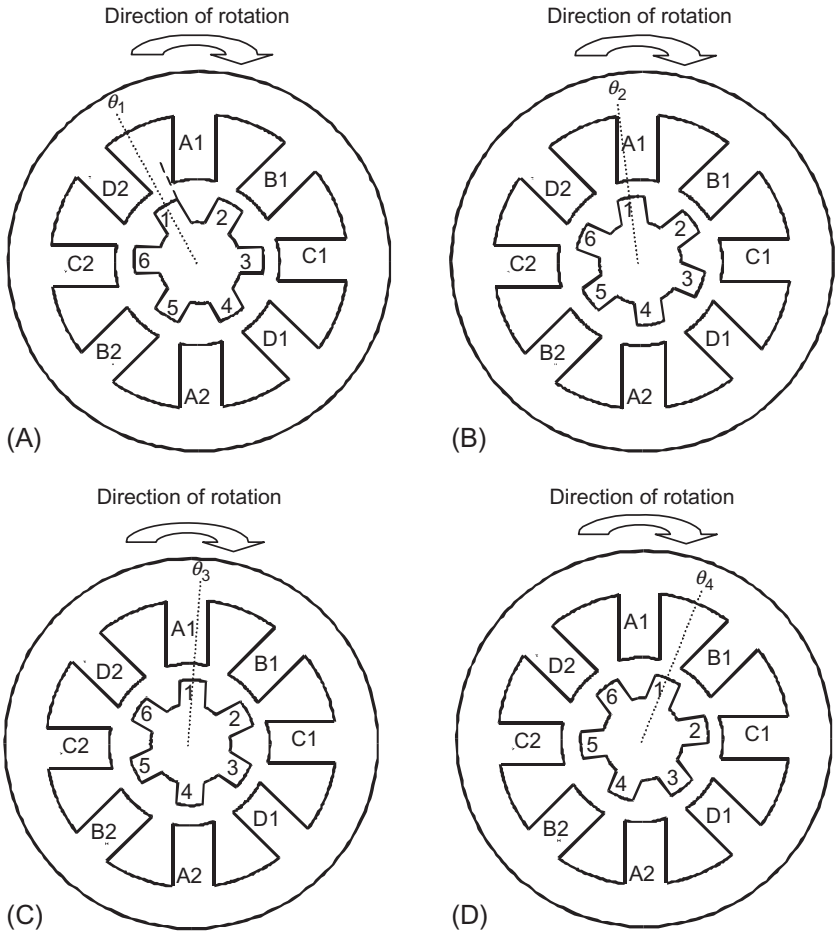


FIG. 30.103 Rotor pole 1 positions: (A) meeting edge of stator pole A, (B) overlapped by stator pole A, (C) edge of rotor pole leaving overlap region, and (D) rotor pole completely leaving overlap region. (Note that air-gap space is exaggerated for clarity.)

Conversely, if current flows during the decreasing inductance region, a negative torque would result. This is because the rotor will be attracted to the stator pole in such a way that it rotates in the opposite direction to the motoring rotation, or in other words, the rotor experiences a torque opposite to the direction of rotation.

It should be noted that this reluctance-machine torque always acts to decrease the reluctance. The direction of current flowing into the stator winding is irrelevant. This signifies that unidirectional current excitation is possible in the SR motor drive.

The variation of torque with rotor angle for a constant phase winding current is as shown in Fig. 30.102. It can be seen that the torque is constant in the increasing and decreasing inductance regions and is zero when the inductance remains constant.

The preceding physical explanation of the developed torque is also given by the familiar torque Eq. (30.96) for a variable-reluctance machine.

$$T = \frac{1}{2} i^2 \frac{dL(\theta)}{d\theta} \tag{30.96}$$

From Eq. (30.96), it is evident that the magnitude of the instantaneous torque developed in the SR motor is proportional to both i^2 and $dL/d\theta$. If the inductance is increasing with respect to the angle, and current flows in the phase winding, then the torque will be positive and the machine will operate in motoring mode. Hence, from Eq. (30.96), it can be seen that when the motor phase is excited during a rising inductance region, part of the energy from the supply is converted to mechanical energy to produce the torque, and another part is stored in the magnetic field. If the supply is turned off during this region, then any stored magnetic energy is partly converted to mechanical energy and partly returned to the supply.

However, a negative or braking torque will be developed by the motor if the inductance is decreasing with respect to the rotor angle and current flows in the phase winding. In this case, energy flows back to the supply from both the stored magnetic energy and the mechanical load, which acts as a generator.

It can also be seen from Eq. (30.96) that the sign (or direction) of the torque is independent of the direction of the current

and is only dependent on the sign of $dL/d\theta$. This explains the torque waveforms that were seen in Fig. 30.102, where for constant current (and constant $dL/d\theta$ magnitude), the magnitude of the torque was constant in the rising or decreasing inductance regions. However, it was seen that the torque changes from positive to negative according to the sign of $dL/d\theta$.

Hence, the ideal waveform for the production of motoring torque would be a square-wave pulse of current (with magnitude equal to the maximum possible supply current) flowing only during the increasing inductance period (Fig. 30.104). This current waveform is illustrated in Fig. 30.104B. However, in practice, this type of current waveform is difficult to produce in a motor phase. This is because the motor phase current is supplied from a finite dc voltage source, and thus, inductance of the stator phase winding would delay the rise and fall of current at the pulse edges. Instead, a more practical current waveform is normally used as is illustrated in Fig. 30.104C. It can be seen that in this waveform, the ideal square waveform is closely approximated by the use of hysteresis current control. At higher speeds, hysteresis current control can no longer be used and a current waveform similar to that shown in Fig. 30.104B is seen in the phase winding. These two types of practical current waveforms, which approximate the ideal square pulse waveform *(a) at low to medium speeds* and *(b) at high speeds*, will be discussed next.

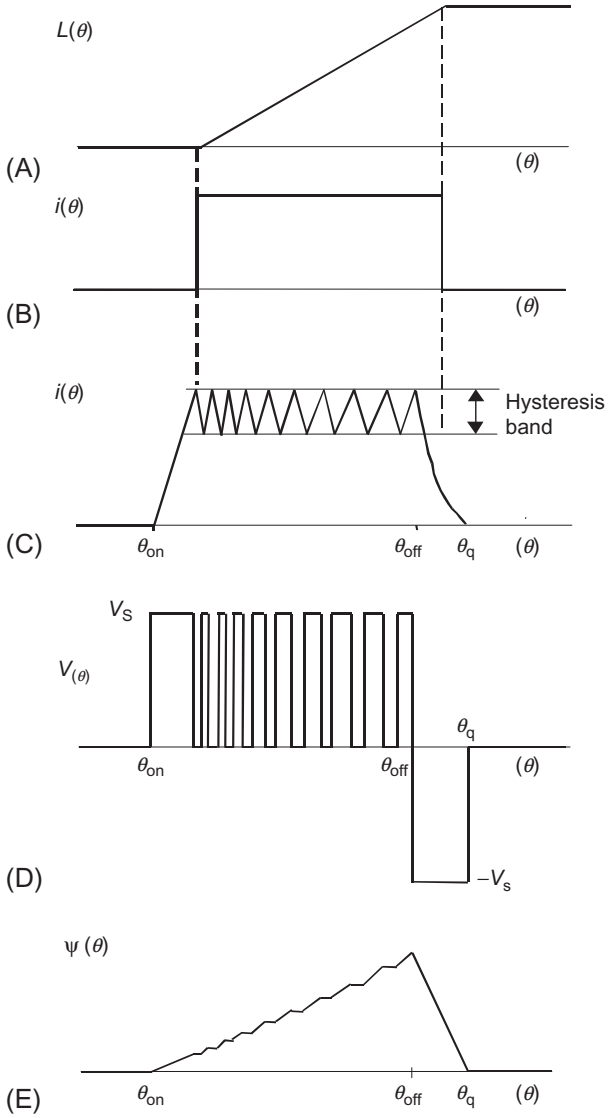


FIG. 30.104 (A) Linear phase inductance variation, (B) ideal square-wave phase current, (C) chopping-mode phase current, (D) chopping-mode phase voltage, and (E) flux linkage waveform corresponding to chopping-mode current.

30.9.5.1 Low to Medium-Speed Approximation to Square-pulse Current Waveform

At low to medium motor speeds, the ideal square-pulse current waveform is approximated in the practical motor drive using hysteresis current control, as is shown in Fig. 30.104C. The hysteresis method of controlling the current is termed the *chopping-mode control* method in SR motor drives. During the time of conduction (between the turn-on and turnoff angles), the current is maintained within the hysteresis band by the switching off and on of the phase voltage by the inverter when the phase current reaches the maximum and minimum hysteresis band. An example of the voltage waveform used for the hysteresis current control is shown Fig. 30.104D, where a constant inverter dc supply voltage of magnitude V_s is used. It can be seen that the switching frequency of the voltage waveform decreases as the angle increases. This is due to the fact that the phase inductance is linearly increasing with angle, which has the effect of increasing the current rise and fall time within the hysteresis band.

In the chopping-mode control method, the *turn-on region* is defined as the angle between the *turn-on angle* θ_{on} and the *turn-off angle* θ_{off} and is chosen to occur during the rising inductance region for motoring torque. In the practical chopping current waveform, the current turn-on angle θ_{on} is placed somewhat before the rising-inductance region. This is to ensure that the current can quickly rise to the maximum level in the minimum-inductance region before the rising-inductance, or torque-producing, region. Similarly, the turnoff angle θ_{off} is placed a little before the maximum-inductance region so that the current has time to decay before the negative-torque, or decreasing-inductance, region. The angle at which the current decays to zero after turnoff is labeled as θ_q in Fig. 30.104C.

30.9.5.2 High-Speed Approximation to Square-Pulse Current Waveform

The chopping-mode of operation cannot be used at higher speeds, as at these speeds, the hysteresis band current level will not be reached. This is because at high speeds, the back emf of the motor becomes equal to or larger than the voltage supply in the rising-inductance region (Fig. 30.105), which limits the increase of the motor phase current. In addition, the rise time of the current will correspond to an ever-increasing angle as the speed is increased. Eventually, at high speeds, the rise-time

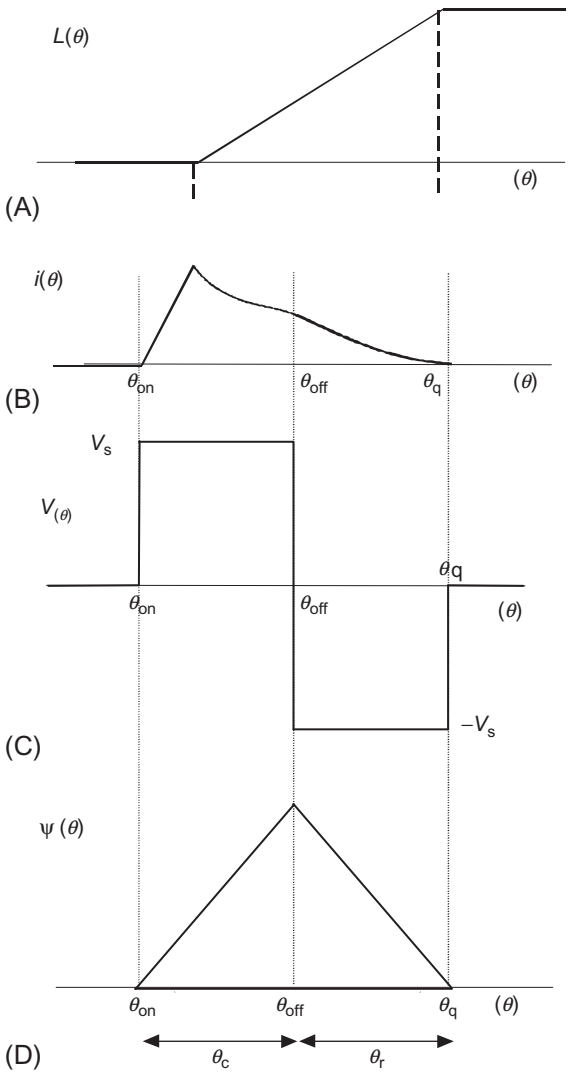


FIG. 30.105 (A) Linear phase inductance variation, (B) single-pulse mode phase current, (C) single-pulse mode phase voltage, and (D) flux linkage waveform corresponding to single-pulse mode current.

angle will be so large that the turnoff angle θ_{off} will be reached before the hysteresis current level has been exceeded. Thus, at high speeds, the current is switched on and off only once per cycle. In SR motor-drive control, this is called the *single-pulse mode* of operation. An example of the single-pulse mode current is illustrated in Fig. 30.105B.

In the single-pulse mode of operation, the inverter power switches turn-on at rotor angle θ_{on}, which places the dc voltage supply V_s across the phase winding, as is shown for the example single-pulse voltage waveform in Fig. 30.105C.

As for the chopping-mode case, in order to maximize torque, θ_{on} must usually be located prior to the rising-inductance region. This is so that, while the inductance is low, the current has a chance to rise rapidly to a substantial value before the torque-producing region begins and the motor back emf increases. At rotor angle θ_{off}, the power switches are turned off, and the phase will have a negative voltage (typically $-V_s$) thrown across it. The current will then decay until it becomes zero at rotor angle θ_q.

30.9.6 Operating Theory of the SR Motor (II): Magnetic Saturation and Nonlinear Model

In the linear model described earlier, it was assumed that the inductance of a phase winding is independent of current. However, in a real SR motor, significant saturation of the magnetic circuit normally occurs as the phase current increases, and thus, the phase inductance is related to both the phase current level and position. Because of the magnetic saturation effect, the actual phase inductances at a given rotor position can be reduced significantly compared with the inductance given by linear magnetization characteristics. In addition, the effect of magnetic saturation becomes larger as the motor current level increases.

The effects of saturation in an SR motor can be observed in a plot of its magnetization curves. This shows the relationship of flux linkage versus current, at rotor positions varying between the fully aligned and unaligned angles. A typical set of SR motor magnetization curves is shown in Fig. 30.106, where it can be seen that there is a nonlinear relationship between the flux linkage and current for each curve.

Due to the magnetic saturation effect discussed earlier, the instantaneous torque Eq. (30.96), which was derived assuming linear conditions, will not be generally valid for calculating the torque in SR motors. Therefore, for accurate calculations, the torque must take into account the dependence of phase inductance with current and position.

If one considers the phase-inductance saturation, the expression for instantaneous torque production of an SR motor phase can be written as

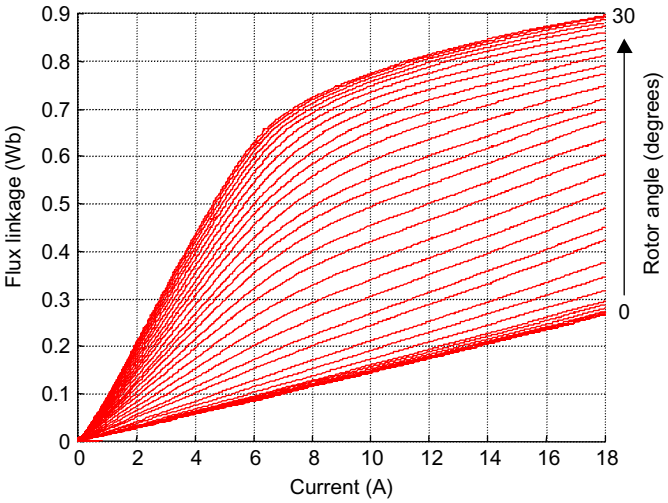


FIG. 30.106 Measured four-phase SR motor magnetization characteristics (each curve represents a constant rotor position).

$$T = \left[\frac{\partial W'}{\partial \theta}\right]_{i=constant} \tag{30.97}$$

where the coenergy W' is defined as

$$W' = \int_0^i \Psi di \tag{30.98}$$

30.9.7 Control Parameters of the SR Motor

A variety of performance characteristics can be obtained in the SR motor by controlling various parameters. These parameters include the chopping-mode control hysteresis level at low to medium speeds and the turn-on and turnoff angles θ_{on} and θ_{off} at all motor speeds. By controlling these parameters, it is possible to produce any desired characteristic such as constant torque, constant power, or some other particular characteristic in between.

As discussed in Section 30.9.5, two distinct modes of operation apply in the SR motor depending on the nature of the current waveform. These modes are the chopping-mode control, which can be used at low to medium motor speeds, and single-pulse mode of control, which is used at high speeds. Both of these modes of operation will be further detailed hereafter, with an explanation of the corresponding inverter switching operation.

30.9.7.1 Chopping-Mode Control

In the chopping-mode control region, the turn-on and turnoff angles are controlled together with the current level. As described in Section 30.9.5, the turn-on angle and turnoff angle are controlled, so that the current flows during the rising-inductance, or positive torque-producing, region. This normally means that the turn-on angle is placed shortly before the place where the rising-inductance angle begins and the turnoff angle is placed shortly before this region ends.

In the chopping mode, the current level is controlled to remain below the maximum allowable level. This involves switching the voltage across the phase on and off in such a manner that the current is maintained between some chosen upper and lower hysteresis current levels. An example of this form of current chopping control was shown in Fig. 30.104C.

The actual torque production of the motor in the chopping mode is set by the control turn-on and turnoff angles and the current hysteresis level. Within the chopping-mode of operation, two current hysteresis control schemes can be used. These are termed *soft* and *hard* chopping. Soft chopping can only be used in some circuit configurations, such as that shown in Fig. 30.107. For soft-chopping control, one switching device remains on during the entire conduction period, while the other is switched on and off to maintain the desired current level. This can be seen in Fig. 30.107A and B, where the two conduction modes during chopping are shown. When both switches are on, the phase winding receives the full positive supply, whereas when only one switching device is on, the phase experiences a zero-voltage freewheeling loop that will decrease the current.

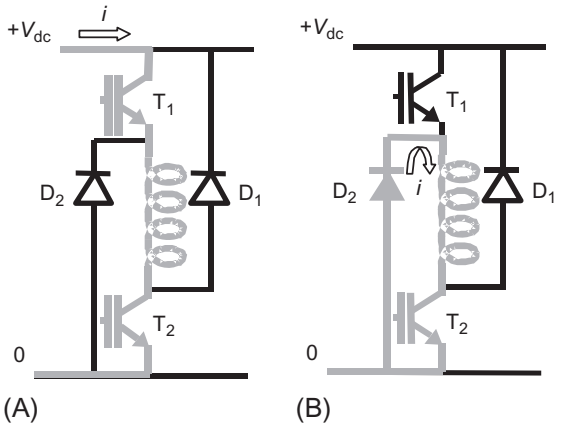


FIG. 30.107 Soft-chopping mode conduction paths: (A) both devices on: positive voltage applied to motor phase and (B) T1 turned off: zero voltage freewheeling loop applied to motor phase.

In the hard-chopping scheme, both devices are switched simultaneously and have the same switching state at all times. If both switching devices are turned on, the phase winding sees the full positive supply. To decrease the current, the full negative supply is applied by turning both devices off as shown in Fig. 30.108. In circuit configurations with fewer than two switches per phase, only hard chopping can be used.

Soft chopping is more advantageous than hard chopping. This is because of a smaller dc ripple current in the supply, which can substantially minimize the ripple-current rating of the dc-link capacitor and lower the hysteresis loss in the motor. It has also been found that the soft chopping lowers acoustic noise and electromagnetic radiation.

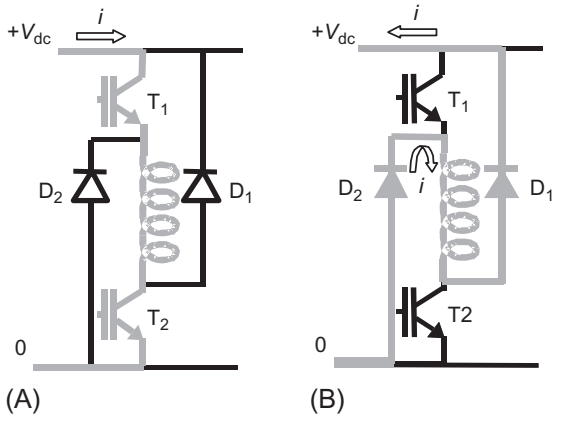


FIG. 30.108 Hard-chopping mode conduction paths: (A) both devices on: positive voltage applied to motor phase and (B) T1 and T2 turned off: negative voltage applied to motor phase.

30.9.7.2 Single-Pulse Mode Control

At higher speeds, the back emf of the SR motor eventually becomes greater than or equal to the supply voltage during the rising-inductance region. This means that even if a phase is excited, the current in the motor phase will not increase in the rising-inductance region. Therefore, at higher speeds, the turn-on angle must be placed before the beginning of the increasing inductance region, so that the phase current will have an adequate time to increase before the back emf becomes high.

In addition, the time available for the current to rise after turn-on becomes less and less as the speed of the motor increases. This is due to the fact that the available conduction time is lower for constant switching angles as the speed of rotation increases. This can be seen by considering that speed is the time rate of change of angle. Thus, as the speed increases, there will be a point when the current level never rises to the chopping level. At this point, the single-pulse mode of operation will come into effect and the current will decrease or remain constant throughout the increasing-inductance zone. An example of a single-pulse mode current waveform was seen in Fig. 30.105B.

As the current is not commutated in the single-pulse mode, the control in this mode consists only of controlling the on and off angles. The turn-on angle θ_{on} can be placed at some point in advance of the rising-inductance region where the phase inductance is low, so that the current can increase at a faster rate before the increasing-inductance region. The angle can be advanced up until maximum allowable current occurs at the peak of the waveform (this may even mean switching on in the previous decreasing-inductance zone). The actual control turn-on and turnoff angles for the single-pulse mode, for a given load torque and speed, can be determined by simulating the motor equations.

The speed at which a changeover between single-pulse and chopping-mode occurs is called the *base speed*. Base speed is defined as the highest speed at which the chopping mode can be maintained at the rated voltage and with fixed on and off angles. Below the base speed, the current increases during the rising-inductance region, unless it is maintained at the maximum or a lower level by chopping.

Therefore, it can be seen that at lower speeds that are below the base speed, the motor is controlled using chopping-mode control, whereas at speeds above the base speed, the single-pulse mode of control is used. In both the control modes, the control turn-on and turnoff angles are chosen so that the motor provides the required load torque.

30.9.8 Position Sensing

It can be seen from the preceding discussion that to control the SR motor satisfactorily, the motor phases are excited at the rotor angles determined by the control method. It is therefore essential to have knowledge of the rotor position. Furthermore, the rotor-angle information must be accurate and have high resolution to allow implementation of the more sophisticated nonlinear control schemes that can minimize torque ripple and optimize the motor performance.

This means that the performance of an SR drive depends on the accurate position sensing. The efficiency of the drive and its torque output can be greatly decreased by the inaccurate position sensing, and the corresponding inaccurate excitation angles. It has been demonstrated that at high motor speeds, an error of only 1° may decrease the torque production by almost 8% of the maximum torque output.

Traditionally, the rotor-position information has been measured using some form of mechanical angle transducer or encoder. The position-sensing requirements are in fact similar to those for brushless PM motors. However, although position sensing is required for the motor operation, the position-measurement sensors are often undesirable. The disadvantages of the electromechanical sensors include the following:

(a) The position sensors have a tendency to be unreliable because of environmental factors such as dust, high temperature, humidity, and vibration.
(b) The cost of the sensors rises with the position resolution. Hence, if high-performance control is required, an expensive high-resolution encoder needs to be employed.
(c) There is an additional manufacturing expense and inconvenience due to the sensor installation on the motor shaft. In addition, consideration must be given to maintenance of the motor because of the mechanical mounting of the sensors, which also adds to the design time and cost.
(d) Mechanical position sensors entail extra electric connections to the motor. This increases the quantity of electric wiring between the motor and the motor drive. This wire normally needs to be shielded from electromagnetic noise and thus further adds to the expense of the drive system.
(e) The allocation of space for the mounting of the position sensor may be a problem for small applications (such as for motors used in consumer products).

Hence, to overcome the problems induced by rotor-position transducers, researchers have developed a number of methods to eliminate the electromechanical sensor for deriving position information. This is achieved by indirectly determining the rotor position. Such methods are commonly termed *sensorless* rotor-position estimation methods. The term sensorless seems to imply that there are no sensors at all. However, there must be some form of sensor used to measure the rotor position. In fact, the term sensorless position estimation in reality implies that there are no additional sensors required to determine position apart from those that measure the motor electric parameters to control the motor. These are normally current- or voltage-measuring circuits.

Hence, all sensorless position estimation methods for the SR motor use some form of processing on electric waveforms of the motor windings. In essence, the major difference between sensorless position detection, and the electromechanical sensors mentioned above, is that there is no mechanical connection of the sensor to the motor shaft. Therefore, sensorless position detection involves electric measurements only.

30.10 Synchronous Reluctance Motor Drives

30.10.1 Introduction

In recent years, there has been a revival of interest in reluctance machines. Two main machines have been the focus of this interest: the switched-reluctance machine (SRM) and the synchronous reluctance machine (Syncrel). The SRM is a machine that does not have sine-wave spatial distributed windings, but instead has concentrated coils and a doubly salient rotor and stator structure. The operation of this machine is highly nonlinear in character, and normal ac machine modeling techniques cannot be applied in a straightforward manner to describe its operation. The SRM drive has been considered in detail in an earlier section.

The Syncrel, on the other hand, has conventional three-phase sinusoidally distributed windings on the stator. The word "synchronous" in the machine's name emphasizes the fact that the stator windings generate a spatial sinusoidally distributed magnetomotive force (mmf) in the air gap between the stator and the rotor and under steady-state conditions the rotor rotates in synchronism with this field. Therefore, the stator winding configuration of this machine is virtually exactly the same as that of the induction machine or the conventional synchronous machine. The major difference between the Syncrel and conventional synchronous and induction machines is in the rotor structure. In both the induction machine and the synchronous machine, there is a source of flux in the rotor itself. In the case of the induction machine, this flux is produced by currents resulting from an induction mechanism, and for the synchronous machine, there is a field winding wound on the rotor that is fed with the dc current to produce flux. The permanent-magnet synchronous machine replaces the wound field on the rotor with a permanent magnet. The Syncrel, on the other hand, does not have any source of flux on the rotor, but instead, the rotor is designed to distort the flux density distribution produced by the sinusoidally distributed mmf.

Sinusoidally wound reluctance machines were traditionally used in the fiber-spinning industry because of their synchronous nature. This made it simple to keep a large number of machines running at the same speed using just the frequency of the supply to the machines. These machines were direct-on-line-start machines. This was facilitated by the presence of an induction machine starting cage on the rotor. This cage was also essential to damp out oscillations in the rotor speed when running at synchronous speed. It should be pointed out that these machines are not considered to be Syncrels—*a Syncrel does not have an induction machine cage on the rotor*. A Syncrel is absolutely dependent on an intelligent inverter drive in order to start the machine and to stabilize it when running. The lack of a requirement for a starting cage means that the rotor design can be optimized for best torque and power performance.

The revival of interest in the Syncrel in the early 1980s was motivated by the development of low-cost microprocessors and reliable power electronics, coupled with the perception that the Syncrel may be more efficient and simpler to control in variable-speed applications compared with the induction machine. The control simplicity is achieved in practice, mainly because one does not have to locate the flux vector in order to implement vector control. The potential for improved efficiency and torque density compared with the induction machine is very much dependent on the rotor design. The Syncrel has the advantage over the switched-reluctance machine; in that it produces relatively smooth torque naturally, and it uses a conventional three-phase inverter. Therefore, inverter technology developed for the induction machine can be applied directly.

30.10.2 Basic Principles

Reluctance machines are one of the oldest electric machine structures, since they are based on the basic physical fact that a magnet attracts a piece of iron. In fact, Syncrel structures were being published in the early 1920s [1]. The essential idea behind the operation of all reluctance machines is that the windings of the machine produce magnetic poles that are used to attract the reluctance rotor. If the magnetic poles are moved around the periphery of the machine at the rate at which the rotor is moving, then sustained torque and rotation can be achieved.

A conceptual diagram of a Syncrel is shown in Fig. 30.109. In this figure, the rotor is represented as a simple "dumbbell"-type rotor. The axes of the three-phase sinusoidally distributed windings are indicated by the dashed lines. If these windings are being fed with currents, then a spatial sinusoidally distributed, mmf results. Because this mmf is sinusoidally distributed, it can be represented by a "space vector" (similar to sinusoidal time-varying quantities being represented by a time phasor). In Fig. 30.109, this resultant space vector is indicated by F, F_d, and F_q are the components of this vector that lie along the high-permeance and low-permeance axes of the machine, respectively.

If one considers the situation shown in Fig. 30.109, then the rotor would tend to rotate in the direction indicated. This rotation would continue until the high-permeance d_r axis (i.e., the least-reluctance axis) of the machine aligns with the mmf vector. When this alignment occurs, the flux produced by

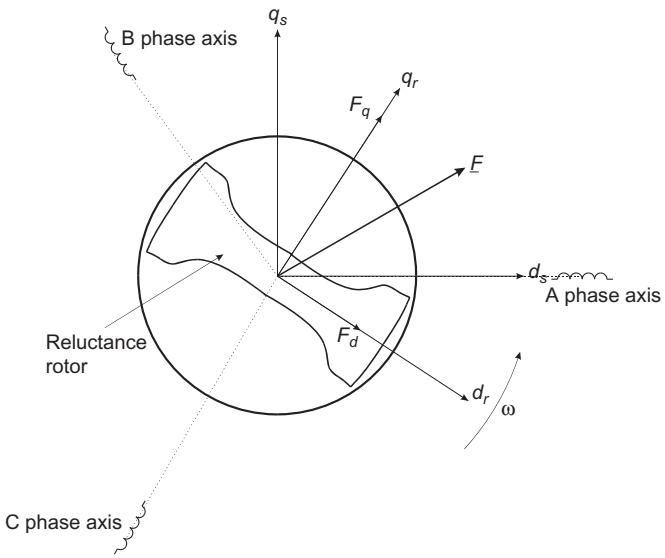


FIG. 30.109 Conceptual diagram of a synchronous reluctance machine.

the stator mmf vector would be maximized. If the vector F also rotates as the rotor rotates, then as mentioned previously, the angle between F and d_r will remain constant and the rotor will continue to chase the F vector, continuous rotation being the result.

One can ask even more fundamental questions such as "why does the rotor rotate to the position that maximizes the flux density?" This is essentially asking why a magnet attracts a piece of iron. To completely answer this question, one has to delve into the field of quantum physics, which is beyond the scope of this presentation. A less complicated explanation is based on the fact that the stator flux density tends to align the domains in the ferromagnetic rotor material, which produces an effect similar to having a current-carrying winding wrapped around the rotor. This effective current then interacts with the stator flux density to produce a force that has a component that is oriented radially around the periphery of the machine. It is this component that produces the torque on the rotor that causes the alignment with the stator mmf vector.

It was mentioned previously that in order to have a continuous motion, the mmf vector F must rotate at the same angular velocity as the rotor, so that the angle between the mmf vector and the d_r axis of the rotor is kept at a constant value. The rotation of the mmf vector is achieved by feeding the three-phase windings of the machine with time-varying currents. It can be shown that if these form a balanced 120° temporally phase-shifted set of sinusoidal currents, then the resultant mmf vector will rotate at a constant velocity related to the frequency of the input current waveforms and the number of pole pairs in the machine.

In order to get a more precise figure for the torque produced by a Syncrel, one has to develop techniques of modeling the machine. Because the Syncrel is a reluctance machine, the coenergy technique for developing the torque expressions can be used [2,3]. The coenergy technique is a very accurate way of determining the torque as it explicitly takes into account, the saturation nonlinearities in the iron of the machine. However, the technique does not lend itself to mathematical analysis and is not a good way of understanding the basic dynamic properties of the machine. The coenergy approach will not be pursued any further in this presentation.

30.10.3 Machine Structure

The essential difference between the Syncrel and, say, the induction machine is the design of the rotor. Most experimental Syncrel systems that have been built use the stator of an induction machine, including the same windings. The rotor designs can take on a number of different forms, from the very simple and basic dumbbell-shaped rotor (such as that sketched in Fig. 30.109) to more complex designs. Unfortunately, the designs that are simple to manufacture (such as the dumbbell design) do not give good performance; therefore, one is forced into more complex designs. The design of the rotor in a Syncrel is the key to whether it is economic to manufacture and has competitive performance with similar machines.

The design of Syncrel rotors fall into four main categories of increasing manufacturing complexity and performance: dumbbell or higher pole-number equivalent designs, flux-barrier designs, radially laminated flux-barrier designs, and axially laminated designs. The first two of these design methodologies are old and lead to designs with poor to modest performance. Therefore, they will not be considered any further. The latter two, however, lead to machine designs with performance comparable with that of the induction machine.

Figs. 30.110 and 30.111 show the cross section of a four-pole machine with a radial lamination flux barrier designed rotor and an axially laminated rotor. The radial lamination design allows the rotor to be built using similar techniques to standard radial laminations for other machines. The flux barriers can be punched for mass production, or wire-eroded for low production numbers. These laminations are simply stacked onto the shaft to form the rotor. The punched areas can be filled with plastic or epoxy materials for extra strength, if required. The iron bridges at the outside of the rotor are designed to saturate under normal flux levels and therefore do not adversely affect the performance of the machine. They are there to provide mechanical strength.

The axially laminated rotor is constructed with laminations running the length of the rotor (i.e., into the page on Fig. 30.111). In between the laminations, a nonmagnetic packing material is used. This can be aluminum or bronze, for example, but a nonconductive material such as slot insulation is better since eddy currents can be induced in conductive materials. The ratio of the steel laminations to nonmagnetic material is usually about 1:1. The axial laminations are all stacked on top of each other, and a nonmagnetic pole piece is bolted on top

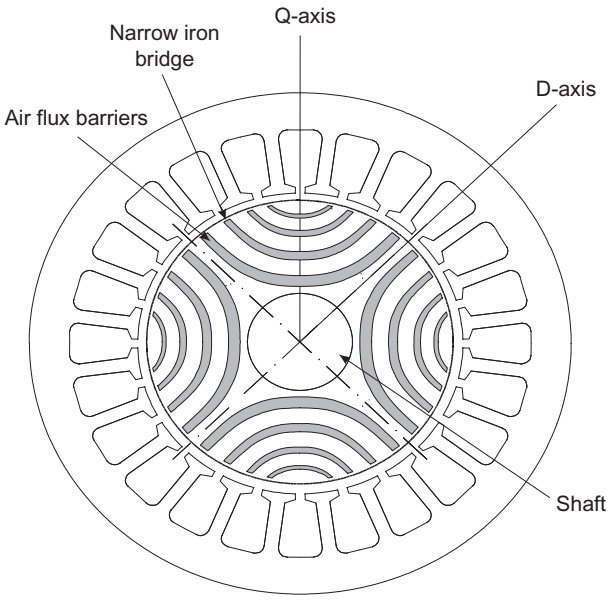


FIG. 30.110 Cross section of a radially laminated Syncrel.

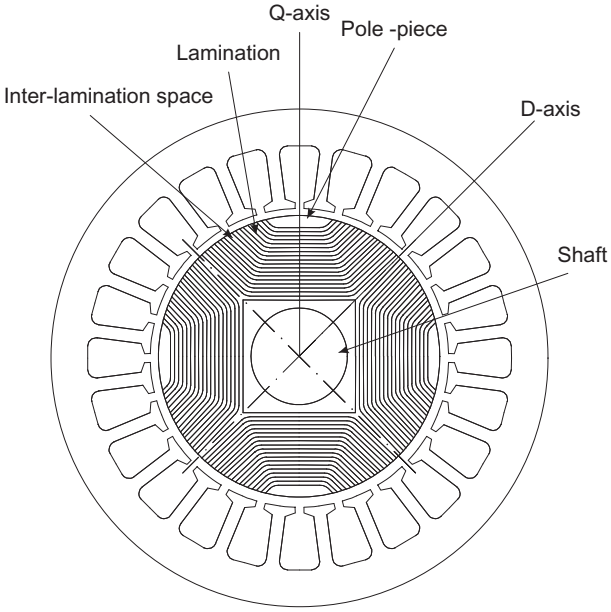


FIG. 30.111 Cross section of an axially laminated Syncrel.

of the stack to hold the laminations to the shaft. The strength of these bolts is usually the main limitation on the mechanical strength and hence the speed of rotation of this rotor. If more or thicker bolts are used to increase strength, the magnetic properties of the rotor are compromised because of the amount of lamination that has to be cut out to make room for them.

Radial- and axial-laminated rotors are usually limited to four-pole or higher machines because of the difficulty of accommodating the shaft in two-pole designs. An axially laminated two-pole rotor has been built with the shafts effectively bonded onto the end of the rotor. Another design was constructed of a block of alternating steel and bronze laminations, the whole structure being brazed together and the resultant stack then being machined into a round rotor and shafts (this rotor was used for high-speed generator applications).

Of the two rotor designs, the radially laminated one has the best potential for economic production. The axially laminated rotor in general gives the best performance, but the mass production difficulties with folding and assembling the laminations make its adoption by industry unlikely. On the other hand, improved designs for radially laminated rotors mean that they can now produce performance very close to that of the axial-laminated designs, and the ease of manufacture would indicate that these rotors are the future of Syncrel rotors.

30.10.4 Basic Mathematical Modeling

In order to give a more quantitative understanding of the machine, a basic mathematical dynamic model of the machine will be introduced.[1] This model will assume that the iron material in the machine does not saturate. This means that the flux density and flux linkage of the windings in the machine are linear functions of the currents in the machine.

To derive the electric dynamic model of a machine, one usually uses Faraday's flux linkage expressions. In the case of the Syncrel, the self and mutual flux linkage between the phases is obviously a function of the angular position of the rotor; therefore, one needs to have expressions for these inductances in terms of rotor position. The fundamental assumption used to make this mathematically tractable is that the inductances vary as a sinusoidal function of the rotor position.[2] The other major part of the modeling process is the conversion from a three-phase model to a two-phase model. This is a process that is carried out for most sinusoidally wound machines, since it allows a variety of machines to be represented by very similar models.

A further complication in this process is that the two-phase model is derived in a "rotating reference frame," as opposed to a stationary reference frame. Developing the equations in a rotating reference frame has the advantage that the normal sinusoidal currents feeding the machine are transformed into dc currents in the steady state, and the angular dependence of the machine's inductances disappear.

One way of heuristically understanding the effect of the rotating frame transformation is to imagine that we are observing the machine's behavior from the vantage point of the rotor. Because the sinusoidal flux density waveform is rotating around the machine in synchronism with the rotor, it appears

[1]Note that the model is not derived but instead just stated. The structure of the model will be heuristically explained.

[2]The sinusoidal variation of inductance with rotor position turns out to be very accurate because of the fact that the stator windings are sinusoidally wound. This forces the flux linkage to behave in a sinusoidal fashion.

from the rotor that the flux density is not changing with time—that is, it is a flux density created by dc currents flowing in a single sinusoidally distributed winding. This single sinusoidal winding is effectively rotating with the rotor. It should be noted that the transformation process of the fluxes, currents, voltages, and machine parameters to the two-phase rotating frame is an invertible process; therefore, one can apply the inverse transformation to ascertain what is happening in the original three-phase machine.

The models derived using the three-phase to two-phase transformations are known as *dq* models, the *d* and *q* referring to the two axes of the machine in the two-phase model (both stationary and rotating frame *dq* axes are shown in Fig. 30.109). The linear[3] *dq* equations for the Syncrel can be derived as [4]

$$v_d = Ri_d + L_d\frac{di_d}{dt} - \omega L_q i_q \tag{30.99}$$

$$v_q = Ri_q + L_q\frac{di_q}{dt} - \omega L_d i_d \tag{30.100}$$

where

$v_d i_d$ = the *d*-axis voltage and current,
$v_q i_q$ = the *q*-axis voltage and current,
L_d, L_q = the *d*- and *q*-axis inductances, respectively,
ω = the electric angular velocity of the rotor.

Thus far, we have concentrated on the electric dynamics of the machine. The other very important aspect is the torque produced by the machine. It is possible to derive the torque of the Syncrel using the principle of virtual work based on coenergy as

$$T_e = \frac{3}{2}p_p\left(L_d - L_q\right)i_d i_q \tag{30.101}$$

The 3/2 factor is to account for the fact that the two-phase machine produces two-thirds the torque of the three-phase machine.[4]

The only other remaining equation is the mechanical equation for the system

$$J\dot{\omega}_r + D\omega_r + T_F = T_e \tag{30.102}$$

where

$J \equiv$ the rotational inertia of the rotor/load,
$D \equiv$ the friction coefficient for the load,
$T_F \equiv$ the fixed load torque of the load,
$\omega_r \equiv$ the rotor mechanical angular velocity ($= \omega/p_p$).

[3]Linear refers to the fact that the equations are derived assuming that the iron circuit behaves linearly in relation to applied mmf and the flux produced.

[4]The 3/2 conversion factor is required if the transformations are power-variant transformations, as opposed to the power-invariant transformations. The power-variant transformations are the most common ones used because the single-phase machine parameters can be used directly in the resultant models, and the two-phase voltages and currents are identical in magnitude to their three-phase counterparts.

Remark Eq. (30.101) shows that the machine must be designed so that $L_d - L_q$ is as large as possible. This will maximize the torque that is produced by the machine for given d- and q-axis currents. To lower L_q, one must design the q-axis so that it has as much air obstructing the flow of flux as possible, and the d-axis must be designed so that it has as much iron as possible. In practice, these quantities cannot be varied independently.

Fig. 30.112 shows the equivalent circuit for the Syncrel corresponding to Eqs. (30.99) and (30.100). One can see that the dynamic equations for the Syncrel are intrinsically simple. In contrast, the induction machine electric equations consist of a set of four complex coupled differential equations.

30.10.5 Control Strategies and Important Parameters

The *dq* model captured in Eqs. (30.99)–(30.101) can be used to explain a number of control strategies for the Syncrel. It is beyond the scope of this section to present the derivation of these. The interested reader should consult references [4–6] cited at the end of this chapter.

One of the most common control strategies for any electric machine is to maximize the torque per ampere of input current. The following discussion should be considered in conjunction with Fig. 30.113, which shows the relationship of the various vectors in the machine to the $d_r q_r$- and $d_s q_s$-axes.

It turns out that one of the critical parameters for the control of the Syncrel is the angle of the resultant current vector in the machine in relation to the *d*-axis of the machine. It is possible to write the torque expression for the Syncrel in terms of this as

$$T_e = \frac{3}{2}p\left(L_d - L_q\right)|i|^2 \sin 2\delta \tag{30.103}$$

It is obvious that this expression is maximized for a given value of i if $\delta = \frac{\pi}{4}$. Therefore, one should control the currents so that δ stays at this angle, if maximum torque per ampere is desired.

Another control objective for the Syncrel is to maximize the power factor for the machine. This is important to minimize the kVA for the inverter. It can be shown that the current angle to maximize the power factor is [4]

$$\delta = \tan^{-1}\sqrt{\xi} \tag{30.104}$$

where $\xi = L_d/L_q$ (the inductance ratio).

Remark Eq. (30.104) indicates that ξ is the important parameter in relation to power factor. In order to obtain a power factor of 0.8, one requires an inductance ratio of approximately 10.

Finally, we shall consider another control objective—to maximize the rate of change of torque with a

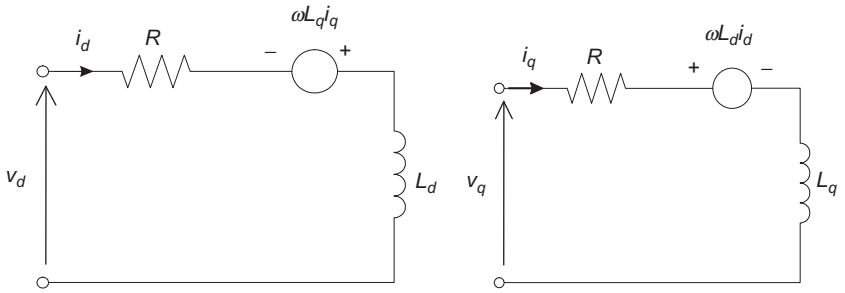


FIG. 30.112 Two-phase equivalent circuit of the Syncrel in a rotating frame.

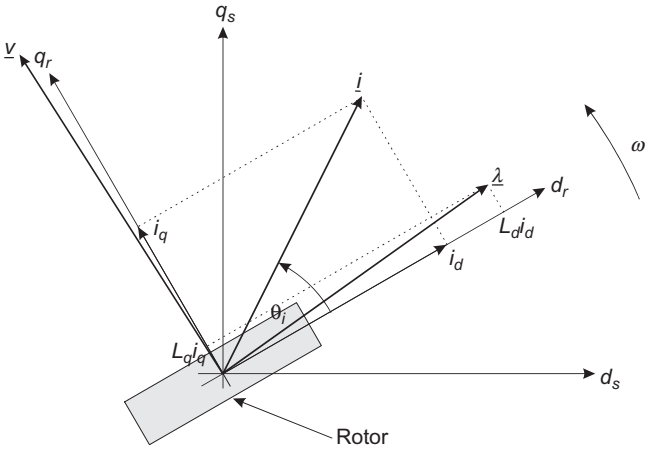


FIG. 30.113 Space phasor diagram of a Syncrel.

fixed-current-angle control strategy. In effect, this means that one is maximizing the rate of change of the currents in the machine for a given voltage applied to it. The analysis of this requirement results in [4]

$$\delta = \tan^{-1}\xi \tag{30.105}$$

Remark As with the maximum-power-factor case, ξ is the most important parameter in relation to the rate of change of torque. Because this control effectively optimizes the current into the machine for a given voltage and angular velocity, this angle also corresponds to that required to maximize the field-weakening range of the machine.

Other control strategies for the machine can be devised, as well as the current angles required to obtain the maximum power from the machine during field-weakening operation.

Remark If one carries out a thorough analysis of all the control properties of the Syncrel, then it emerges that all performance measures for the machine are enhanced by a large value of the ξ ratio.

30.10.6 Practical Considerations

The control strategies discussed in the previous section were all derived assuming that the machine does not exhibit saturation and there are no iron losses. The q-axis of the machine does not have any saturation, as the flux path on this axis is dominated by air. However, the d-axis of the machine does exhibit substantial saturation under operational flux levels, and this effect must be accounted for to optimize the drive performance.

The effect that saturation has on the ideal current angles is to increase them. This increase is most pronounced for the maximum torque per ampere control strategy, since this strategy results in a larger component of current in the d-axis, and consequently more saturation. Maximum power factor and maximum rate of change of torque are not affected as much. In order to get the correct current angle for maximum torque per ampere, a lookup table of the saturation characteristic of the machine must be stored in the controller, which is consulted in order to calculate the desired current angle [7].

It has been found that iron losses in the stator and the rotor also affect the optimal current angles. However, usually saturation effects dominate, and the effects of iron losses can be ignored.

30.10.7 A Syncrel Drive System

The basic structure of a variable-speed drive system based on using the Syncrel is shown in Fig. 30.114. Many components of this drive are very similar to those found in an induction machine drive system. One notable exception is the L_d lookup table block and the current reference generator. The L_d lookup stores the current versus d-axis inductance table for the machine, thereby allowing the inductance to be determined for various current levels. This table is also used to generate the incremental d-axis inductance. The inductance values generated from this table are used in the state feedback block and the torque estimator.

The state feedback block effectively generates an offset voltage to the PWM generator so that the voltage it produces is at least enough to counter the back emf. This technique effectively eliminates the back-emf disturbance from the current-control loops.

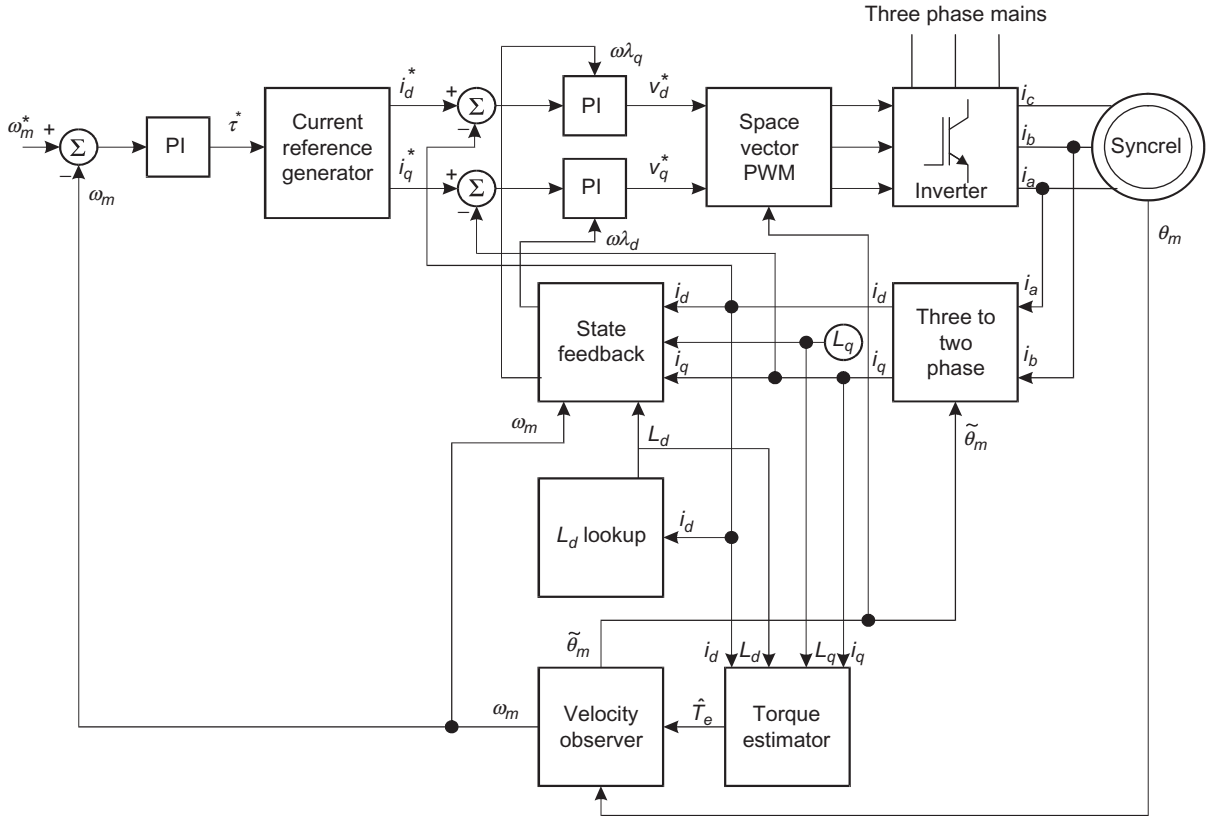


FIG. 30.114 Block diagram of a Syncrel drive system.

The current reference generator takes the desired torque as an input and generates the required *d*- and *q*-axis currents at the output. This block uses a lookup-table technique together with an inverse of the torque equation to generate these currents and takes into account the saturation characteristics of the machine.

The three-to-two-phase block converts the currents from a three-phase stationary frame to a two-phase rotating frame. This is a standard block in induction machine drives, and as with induction machine drives, this means that the Syncrel control algorithm is implemented in a rotating reference frame. The conversion from this frame back to the stationary frame occurs implicitly in the space vector PWM generator.

The Syncrel control algorithm is essentially a simplified vector controller, and consequently, the computational requirements are not high. This means that a Syncrel controller can be implemented on a modest microprocessor. As far as input and output hardware is concerned, the requirements are basically the same as those for an induction machine system—that is, sample two of the phase currents, the link voltage, and the rotor position.

30.10.8 Conclusion

The Syncrel-based drive system offers simplicity in control, excellent performance for variable-speed and position-control applications, good torque and power density, and efficiency that is more than competitive with that of the induction machine drive systems. To date, very few commercial drive systems are available using Syncrels, this being mainly due to the slow emergence of easy-to-manufacture rotors that give good performance and the conservatism of the motor-drive industry. One commercial application that has emerged is ac-servo applications, where the Syncrel offers low torque ripple (with appropriate rotor design) together with a small moment of inertia. Other applications under consideration are in the area of drives for electric vehicles and generators for flywheel energy storage systems. It remains to be seen whether the Syncrel can ever challenge the supremacy of the vector-controlled induction machine in mainstream industrial applications.

The interested reader who wishes to pursue Syncrel drives in more detail can find a good coverage of the control and motor design issues in [8].

Further Reading

DC Motor Drives

[1] G.K. Dubey, Power Semiconductor Controlled Drives, Prentice Hall, Englewood Cliffs, NJ, USA, 1989.
[2] W. Leonhard, Control of Electric Drives, Springer-Verlag, Berlin Heidelberg, Germany, 1996.
[3] V. Subrahmanyam, Electric Drives: Concepts and Applications, McGraw Hill, New York and London, 1994.
[4] M.A. El-Sharkawi, Fundamentals of Electric Drives, Thompson Learning, Boston, MA, USA, 2000.
[5] S.-K. Sul, Control of Electric Machine Drive Systems, Wiley & IEEE Press, New Jersey, USA, 2011.
[6] N. Mohan, Electric Drives, and Integrative Approach, MNPERE, Minneapolis, USA, 2003.

Induction Motor Drives

[7] W. Leonhard, Control of Electric Drives, Springer-Verlag, Berlin Hedelberg, Germany, 1996.
[8] B.K. Bose, Power Electronics and AC Drives, Prentice Hall, Englewood Cliffs, NJ, USA, 1987.
[9] J.M.D. Murphy, G.G. Turnbull, Power Electronic Control of AC Motors, Pergamon Press, Oxford, England, USA, 1988.
[10] D.W. Novotny, T.A. Lipo, Vector Control and Dynamics of Drives, Oxford Science Publications, Oxford, UK, 1996.
[11] P. Vas, Electrical Machines and Drives: A Space Vector Theory Approach, Clarendon Press, Oxford, UK/New York, USA, 1992.
[12] G.K. Dubey, Power Semiconductor Controlled Drives, Prentice Hall, Englewood Cliffs, NJ, USA, 1989.
[13] S.-K. Sul, Control of Electric Machine Drive Systems, Wiley & IEEE Press, New Jersey, USA, 2011.
[14] R.D. Donker, D.W.J. Pulle, A. Veltman, Advanced Electrical Drives, Springer, Berlin Heidelberg, Germany, 2011.

Synchronous Motor Drives

[15] W. Leonhard, Control of Electrical Drives, Springer-Verlag, Berlin Heidelberg, Germany, 1996.
[16] J.M.D. Murphy, G.G. Turnbull, Power Electronic Control of AC Drives, Pergamon Press, Oxford, England, USA, 1988.
[17] G.R. Slemon, Electric Machines and Drives, Addison-Wesley, New York, USA, 1992.
[18] W.W. Novotny, T.A. Lipo, Vector Control and Dynamics of AC Drives, Oxford Science Publications, Oxford, UK, 1996.
[19] S.-K. Sul, Control of Electric Machine Drive Systems, Wiley & IEEE Press, New Jersey, USA, 2011.
[20] R.D. Donker, D.W.J. Pulle, A. Veltman, Advanced Electrical Drives, Springer, Berlin Heidelberg, Germany, 2011.

Permanent-magnet Synchronous Motor Drives

[21] T.J.E. Miller, Brushless Permanent Magnet and Reluctance Motor Drives, Oxford Science Publications, Oxford, UK, 1989.
[22] "Performance and Design of Permanent Magnet AC Motor Drives", Tutorial course, IEEE Industry Application Society, 1989.
[23] R.M. Crowder, Electric Drives and Their Controls, Oxford Science Publications, Oxford, UK, 1995.
[24] L. Zhong, M.F. Rahman, K.W. Lim, Modelling and Experimental Studies of an Instantaneous Torque and Field Weakening Control Scheme for and Interior Permanent Magnet Synchronous Motor Drive, Journal on Mathematics and Computers in Simulation 46 (1998) 289–300.
[25] R.F. Schiferl, et al., Power Capability of Salient-pole Permanent-Magnet Synchronous Motors in Variable Speed drive Applications, IEEE Transactions on Industrial Applications 26 (1990) 115–123.

Permanent-magnet Brushless DC (BLDC) Motor Drives

[26] T.J.E. Miller, Brushless Permanent-magnet and Reluctance Motor Drives, Oxford University Press, Oxford, UK, 1989. For "square-wave brushless dc motors".
[27] T. Kenjo, S. Nagamori, Permanent-magnet and Brushless DC Motors, Oxford University Press, Oxford, UK, 1985. For "small machines used particularly in consumer electronics".
[28] D.C. Hanselman, Brushless Permanent-magnet Motor Design, Mc Graw Hill, USA, 1994. For "the possible range of controllers in the last chapter".
[29] Application notes from the various integrated circuit companies, particularly those that specialize in motor control.

Servo Drives

[30] G.W. Younkin, Industrial Servo Control Systems: Fundamentals and Applications, Marcel Dekker, New York, USA, 1996.
[31] B.C. Kuo, J. Tal, Incremental Motion Control 1: DC motors and systems, SRL Publishing, Champaign, USA, 1978.
[32] D. Shetty, R. Kolk, Mechatronics Systems Design, PWS Publishing, Boston, MA, USA, 1997.
[33] Fransua, R. Magureanu, Electric machines and Drive Systems, Technical Press, Oxford, 1984.

Stepper Motor Drives

[34] H.B. Ertan, A. Hughes, P.J. Lawrenson, Efficient numerical method for predicting the torque-displacement curve of saturated VR stepping motors, Proc. IEE 133 (Part B) (1980).
[35] T. Kenjo, A. Sugawara, Stepping Motors and Their Microprocessor Controls, Oxford University Press, Oxford, UK, 1994.
[36] P.P. Acarnley, Stepping Motors: A Guide to Modern Theory and Practice, IEE Control Engineering Series, Vol. 19, Peter Peregrinus, London, UK, 1982.
[37] Application Notes AN235, "Stepper Motor Driving," Discrete Semiconductor Handbook. SGS Thompson Microelectronics, 1995.
[38] M.F. Rahman, C.S. Chang, A.N. Poo, Approaches to ministepping step motor controllers and their accuracy considerations, IEEE Transactions on Industrial Electronics 32 (3) (1985).
[39] Proceedings of Symposium on Incremental Motion Controls Systems and Devices. 1972–1992. University of Illinois, Urbana-Champaign, IL.

Switched-reluctance Motor Drives

[40] J. R. Hendershot, "Application of SR drives", "IEEE Industry Application Society Tutorial on Switched Reluctance Drives", 60–90, 1990.
[41] P.J. Lawrenson, Switched reluctance motor drives, Electronics and Power (1983) 144–147.
[42] E. Richter, Switched reluctance machines for high performance operations in a harsh environment—a review paper, in: Int. Conf. Electrical machines (ICEM '90), Part 1, 18–24 August 1990, 1990.

[43] P.J. Lawrenson, Switched Reluctance Drives—A Fast Growing Technology, Electric Drives and Controls (1985).
[44] T.J.E. Miller, Switched Reluctance Motors and Their Control, Clarendon, Oxford, 1993.
[45] S.R. MacMinn, Control of the Switched Reluctance Machine, in: Switched reluctance drives tutorial, IEEE Industry Applications Society Conference, 25th Industry Application Society Annual Meeting, Seattle, 12 October 1990, 1990, pp. 36–59.
[46] A.D. Cheok, N. Ertugrul, High robustness of an sr motor angle estimation algorithm using fuzzy predictive filters and heuristic knowledge based rules, IEEE Trans. Ind. Electr. 46 (5) (1999) 904–916.

Synchronous Reluctance Motor Drives

[47] J. Kostko, Polyphase reaction synchronous motors, J. Amer. Inst. Elec. Eng. 42 (1923) 1162–1168.
[48] D. O'Kelly, S. Simmons, Introduction to Generalised Electrical Machine Theory, McGraw Hill, London, UK, 1968.
[49] D. Staton, W. Soong, T.J. Miller, Unified theory of torque production in switched reluctance motors, IEEE Trans. on Industry Applications IA-31 (1995) 329–337.
[50] R.E. Betz, Theoretical aspects of control of synchronous reluctance machines, IEE Proc. B 139 (1992) 355–364.
[51] T. Fukao Chiba, A closed-loop operation of super high speed reluctance motor for quick torque response, IEEE Trans. on Industry Applications IA-28 (1992) 600–606.
[52] M.G. Jovanovic, R.E. Betz, Theoretical aspects of the control of synchronous reluctance machine including saturation ad iron losses, in: Proceedings of IEEE-IAS Annual Meeting, Houston, October, 1992, 1992.
[53] M.G. Jovanovic, Sensorless Control of Synchronous Reluctance Machines, University of Newcastle, Australia, 1997. PhD thesis.
[54] I. Boldea, Reluctance Synchronous Machines and Drives, Clarendon Press, Gloucestershire, UK, 1996.

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31

Fundamentals of Power Electronics Controlled Electric Propulsion

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31.1 Introduction

After the energy-generating industries, transportation system is utilizing a big part of world's energy resources. Thus, it is responsible for a comparable share of environment pollutants caused by the combustion of fossil fuel (viz. petrol, diesel, and ethanol) [1]. A global transformation of transportation system for environment protection, energy conservation, energy-efficient system, and low-carbon emission will require significant improvement in the process of onboard energy production and its efficient consumption [2–4]. This technological transformation requires systematic development of fuel- and energy-efficient technologies in transportation sector.

31.1.1 Motivations for Vehicular Electrification

Conventional transportation system employs internal combustion engine (ICE)-based propulsion system, which uses petroleum products for propulsion. It is estimated that, at the present consumption rate, the current global petroleum resources will be used up within the next 50 years [4]. It has also raised growing concerns about environmental pollution and subsequent climate changes. For example, in the United States of America (USA), conventional transportation system accounts for 30% of total greenhouse gases (GHG) emission, causing significant global warming [3]. Moreover, it is projected that world population will increase from the existing 6 billion to around 10 billion in the next 50 years while the number of vehicles in operation is set to increase from 700 million to 2.5 billion [4].

With the projected growth of small cars and its CO_2 emissions, the importance of addressing fuel efficiency in road transport is significantly important on global environment, energy, and climate change agendas. Road transportation system is responsible for approximate 20% of global CO_2 emissions from fossil-fuel combustion, and in most countries, CO_2 emissions from transportation are growing at a faster rate than total CO_2 emissions [2,3]. Projections for road transport growth and car ownership for the next few decades as shown in Fig. 31.1 show that road transport will continue to dominate, despite the rapid growth in shipping and aviation sectors.

Significant fuel economy improvements and reduction in tailpipe emission in road transportation sector are required to stabilize and reduce greenhouse gas and CO_2 emissions. The United Nations Intergovernmental Panel on Climate

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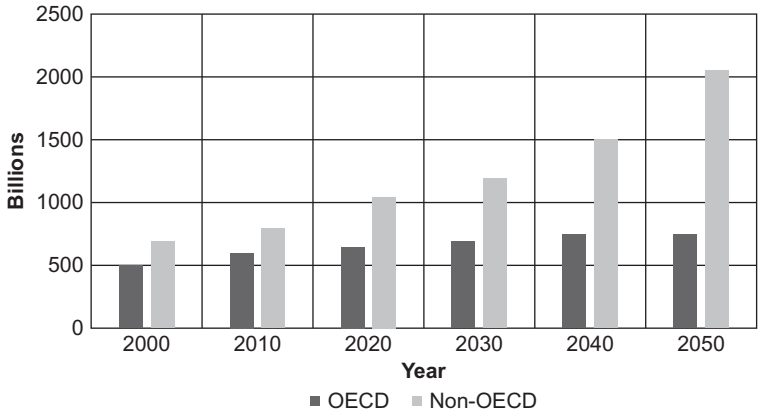


FIG. 31.1 Global growth in light-duty vehicles. Data from Mobility 2030: "Meeting the Challenges of Sustainability," World Business Council forSustainable Development (WBCSD) July 2004a and 2004b.

Change (IPCC) states that an ambitious 50%–80% reduction in global CO_2 emissions is required by 2050 (as compared with 2000 levels) in order to limit temperature rise to 2–2.4°C and stabilize atmospheric CO_2 concentration at 450 ppm, thus avoiding severe climate change [2,3]. Doubling the fuel efficiency of road vehicles is one of the most cost-effective and accessible measures toward achieving global stabilization of CO_2 emissions. However, the targets for both reduction of global CO_2 emission and improvement in fuel efficiency require that all countries should adopt cleaner technology on a large scale. Given this scenario, meeting the worldwide energy demand for the present and future transportation systems with the least impact on the environment is an important challenge in terms of technological and societal development.

In order to meet this challenge, novel concepts and innovations are being infused to make transportation systems more and more energy-efficient, reliable, and safe with zero or reduced emissions at an affordable cost. These novel concepts and innovations can be seen in terms of use of low-carbon fuel such as bioethanol or biodiesel, substitution of the petroleum energy by electric energy to drive vehicles, and hydrogen-based power generation. [4]. Majority of these innovations are solely relying on electrification of conventional vehicular technology and are grouped under the genre of electric vehicular technology (EVT). In EVT, ICE-based propulsion systems are being replaced by electric propulsion system (EPS), either partially or fully, to minimize fuel consumption and tailpipe emission. Vehicles that employ EVT can be broadly classified as follows [5–15]:

- Battery electric vehicles (BEVs)
- Hybrid electric vehicles (HEVs)
- Plug-in hybrid electric vehicles (PHEVs)
- Fuel-cell vehicles (FCVs)

BEVs are mainly the combination of energy storage system (ESS) and electric propulsion unit that together constitute the power to propel the wheels. Limited operating range and comparatively poor performance and limitation of storage system are the major concerns with BEVs. HEVs are the combination of BEVs and ICE vehicles to bring the advantages of both the vehicles together. Hybrid technologies can be used for almost all kinds of energy sources and engines. The additional electric and mechanical components make the HEVs more complex, bulkier, and costlier. PHEVs are the integration of EVs and HEVs to extend the degree of electrification and electric driving range of the vehicles to achieve the higher efficiency and reduced emission. However, infrastructures for charging stations are major concern. FCVs use hydrogen as fuel to produce electricity; therefore, they are basically emission-free.

31.1.2 Advancement of Electric Vehicular Technology

In the last decade, EVT is accelerated globally as competitor and sustainable alternatives of conventional ICE-based vehicles. Efforts and substantial resources are directed to meet market expectations for high-performance, energy-efficient, durable, safe, and affordable electrified vehicles [5]. The technological development and growth of EVT has taken on an accelerated pace on their road map to overcome the abovementioned issues associated with each of the electrified vehicles. Therefore, the dream of having commercially viable EVs/HEVs/FCVs/PHEVs is becoming a reality. EVs/HEVs are gradually commercializing and capturing the significant market space; PHEVs are ready to be commercialized, whereas FCVs are under development and yet to be commercialized [5–13]. The vision of vehicular electrification also includes generating electricity more and more from carbon-free and renewable energy sources such as wind, solar, hydro, fuel cell, and using them in transportation [12]. The next generation of electrified vehicles will therefore be integrated with electric power systems through EVs and PHEVs that will enable to implement grid-to-vehicle (G2V) and vehicle-to-grid (V2G) concept and will reduce environmental footprint significantly

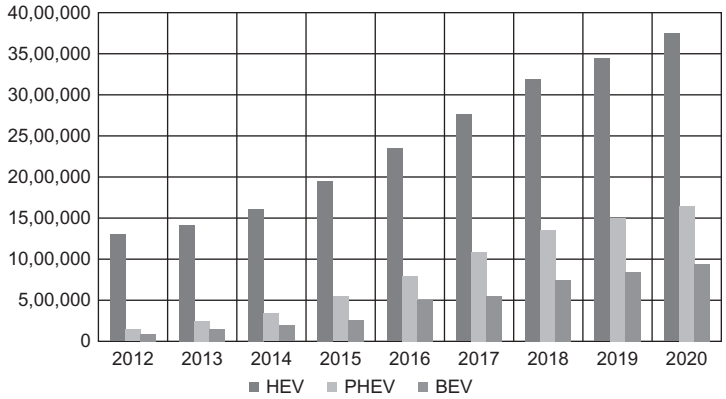


FIG. 31.2 Electrified vehicles sales worldwide. Data from https://www.navigantresearch.com/research/transportation-forecast-light-duty-vehicle/ (accessed 09.08.15).

[12–14]. The world-wise sales of BEVs, HEVs, and PHEVS are presented in Fig. 31.2.

In the last decade, successive development in vehicular electrification brought back the electrified vehicles specially HEVs in competition with ICE vehicles in terms of dynamic behavior, driving range, and practicability with added advantage of higher efficiency, reduced emission, and globally emerged as sustainable alternative of conventional ICE-based vehicles [5–10]. Therefore, at present, major attention has been focused on technological advancement and modernization of HEVs. Moreover, automobile industries are shifting toward more fuel-efficient, improved performance, higher degree of reliability, durability, safety, and added comforts. Thus, significant efforts and resources are being spent by leading car manufacturers and government to meet these market expectations at an affordable cost [16].

31.1.3 Hybridization of Energy System for EVT

In an EVT, the onboard energy sources are limited and acting as bottleneck of the technology [17]. However, it is essential that the power requirement of vehicle load should be met on board. It is impractical and very expensive to size a single-source energy system to offer continuous power with a capacity many times higher than the average power demand, just to meet momentary peaks in power needs. Therefore, adopting multiple energy sources on board that are specialized for the various segments within a vehicular power demand bandwidth becomes a viable solution [17]. The combination of storage system with high-energy-density specifications and storage system with high-power-density specifications provides sustainable solutions [18]. The task of a power and energy management system then is to properly coordinate the dynamics of the energy systems without compromising the vehicle's targeted performance [19].

In EPS, none of the available energy sources are capable enough to meet power and energy requirement of the vehicle for all driving profile [18]. In recent years, it has been observed that to fix the onboard energy demand of electrified vehicles, there is need to mix the energy sources. This encapsulates the idea that the solution to problem of meeting onboard energy demand is hybridization of diverse energy sources such as fossil fuel, solar, hydrogen, and portable source of electric energy like battery, ultracapacitor, and fuel cell.

As an alternative to onboard single-source energy system, hybridization of energy sources is considered as durable and sustainable energy system. HES is gaining more and more popularity in vehicular electrification due to their ability to provide high-power and high-energy-density systems. A well-designed HES offers features like reliability, durability, cleanliness, and efficient power processing operation compared with single-source energy system [17–20]. It provides optimum solution between availability and utilization of energy sources and offers good power-handling capability in steady-state operation and superior dynamic response during transient conditions.

31.1.4 Power Electronics for EVT

The integration of different components from different branches is a major challenge and is a growing concern in the road map of vehicular electrification. PECs and switches are playing a very significant role in incorporating different components and provide compatibility for proper coordination among them to meet vehicle's requirement in all driving profiles [21–25]. Advancement in power electronic devices is an enabling technology for the next generation of vehicles that offers smarter, efficient, cleaner, precise, environmentally friendly, and more flexible drive. The reasons for rapid acceleration in growth of vehicular power electronics as discussed in [23] are as follows:

- The new vehicle architecture integrated with power electronics makes the switching and fusing functions through single component with higher degree of reliability.

- Integrated of sensing technique with power electronic devices enables easy fault detections and diagnosis and makes system capable for fault-tolerant operation.
- PECs make on demand power conversion as per auxiliary load profile and for propulsion motor resembling the functions of adjustable speed drives.
- Voltage conversion for different voltage level especially in dual-voltage architecture and dc/ac and ac/dc conversion can be done using power electronics.
- Power electronics devices are used in the development of electronically controlled actuators and variable valves with high degree of precision and accuracy.
- Power electronics with modern digital signal controller provides very fast and high-power motion control of propulsion system by enabling high-power actuation and dynamics.

Power semiconductor devices constitute the heart of modern power electronic apparatus, and today's power electronic evolution has been possible primarily due to evolution in power electronic devices [21]. In the past few years, power device technology has made remarkable progress and grown in power rating and performance by an evolutionary process.

For EVT, there is a need of highly reliable, flexible, and fault-tolerant EPS. Suitable integration of ESS, power electronic converters (PECs), electric motors (EM), and electronic control unit (ECU) makes the EPS to compete against the conventional ICE-based vehicle [25]. The responsibility of integration of these components is well taken care by power electronic devices. A PEC, consisting of a matrix of power semiconductor switches and one or several passive components, helps to convert and control electric power from one form to another form at different voltage and current profile between ESSs and EMs according to the driving profile of the vehicle. PECs act as an interfacing medium for the hybridization of different energy sources like battery, ultracapacitor and fuel cell to match the onboard power and energy requirement. For vehicle acceleration, PECs take power from onboard energy system and supply power to the electric motor as per the demanded vehicle operation. On the other hand, PECs can also be used to utilize recovered energy during deceleration and regenerative braking to charge ESS. The electronic controllers composed of sensors, digital signal processors, and interfacing circuitry are used to generate the control signals for PECs [26].

Power electronics is an enabling technology for efficient electric power processing, which plays crucial role in shifting paradigm from conventional ICE vehicles to electrified vehicles [22,25]. The demand of electric power in vehicular application is growing rapidly as the mechanical components are being replaced by the electric and electronic components. It is expected that the power demand in electrified vehicle could reach 2–3 times of the current demand [23]. In order to accomplish the growing power demands of electrified vehicles in desired manner, integration of power electronic components with electric and mechanical loads of the vehicle becomes crucial [24]. The integration of PEC not only improves the overall performance and fuel economy but also reduces the emission as well as weight and size of the EPS.

31.2 Electric Vehicular Technology

The development process of the electrified vehicles is interesting, as the first battery-operated electric vehicle is invented in 1834 [8]. Due to the lack of technology, primarily for electrochemical storage units, the interest in EVs gradually diminished and ceased to receive any attention after 1920. In the early 1970s, circumstances changed in favor of the electrified vehicle concept due to the dramatic increase in petroleum prices, global awareness about environmental pollution, and stringent emission regulation [8]. The research on EVT is motivated by the argument that electric vehicles represent an economical and technically sustainable option for future transportation systems. Environmental impacts, escalating prices of petroleum fuels, emission restrictions, and the depletion of natural resources provide compelling impetus toward the development of more eco-friendly solutions. It represents one of the greatest challenges of today, a challenge that calls for sustainable advancements and development of EVT.

EVT, essentially, has two major components:

(1) Vehicle architecture and configuration
(2) Electric propulsion system that includes
   - energy storage system (ESS),
   - power electronic converter (PEC),
   - electric motor (EM),
   - electronic control unit (ECU).

There are plenty of review papers and literature that deal individually with topological architecture and configuration [4–15,27–29], energy source and storage systems [17–20,30–47], electric machines [21,48–62], power electronic converters [21–25,63–75], and power-flow management and control strategy [76,77]. This section discusses the architecture of HEVs that includes series, parallel, series-parallel, and complex HEV.

31.3 Classification of Electric Vehicular Technology [6]

The vehicular technology can be classified as ICE-based vehicles and EPS-based vehicles or electrified vehicles. Electrified vehicles that are driven by EPS either fully or partially further are classified as EVs, HEVs, PHEVs, and FCVs. In EVT, each vehicle has its own capability and limitation in terms of energy density, power density, emission rate, performance, fuel efficiency, size, weight, cost, and safety [4–10]. These factors are heavily governed by the particular vehicle architecture and

propulsion system configuration. Out of the several class of electrified vehicle mentioned above, HEV is the only option that has potential to compete the ICE vehicles in terms of performance. The major advantages of HEV are extended electric range of operation, good fuel economy, higher efficiency, and sufficient onboard power and better dynamic response. Different characteristic such as size versus distance characteristic is depicted in Fig. 31.3, whereas driving distance of some popular BEVs, HEVs, and PHEVs commercialized so far is given in Table 31.1 along with their associated benefits.

31.3.1 ICE Vehicles

A conventional ICE burns a high-energy-density petroleum fuel (gasoline/diesel) in its combustion chamber and produces power that can be utilized to propel the vehicle by means of

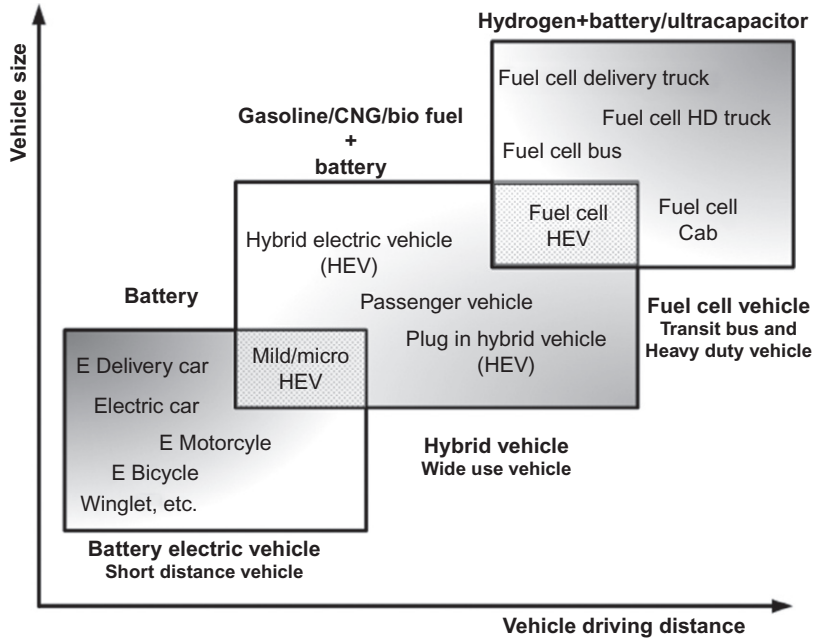


FIG. 31.3 Classification of EVs/HEVs/PHEVs/FCVs based on size versus distance. Based on www.toyota-global.com.

TABLE 31.1 Characteristic of different electrified vehicles

S.No	Car Model	Range (miles)	Top Speed (mph)	Charge Time (hrs)	Battery (kWh)	Rated output (HP)	Acceleration (0-60 mph)
Battery Electric Vehicle							
1	Smart Fortwo Electric	70-80	81	2.5	17.6	80	11.4 s
2	Ford Focus Electric	115	84	5.5 (240V)	33.5	143	9.9 s
3	Nissan Leaf	107	93	9.5	30	107	9.9 s
4	BMW i3	114	93	4	33	170	7 s
5	Kia Soul EV	132	90	4-5	27	109	10.8 s
Hybrid Electric Vehicle							
6	Toyota Prius Plus	640 25 on battery	103	2	8.8	121	10.5 s
7	BMW i8	310 23 on battery	155	2-3	7.1	357	4.2 s
8	Chevy Volt 2nd Generation	420 53 on battery	100	13 (120V)	18.4	84 (Engine) 74 (Motor)	9.2 s
9	Honda Accord Hybrid	758 On battery NA	112	NA	1.3	212	6.9 s
10	Volkswagon Jetta Hybrid	571.2 On battery NA	185	NA	1.1	170	7 s

* NA – Not Available

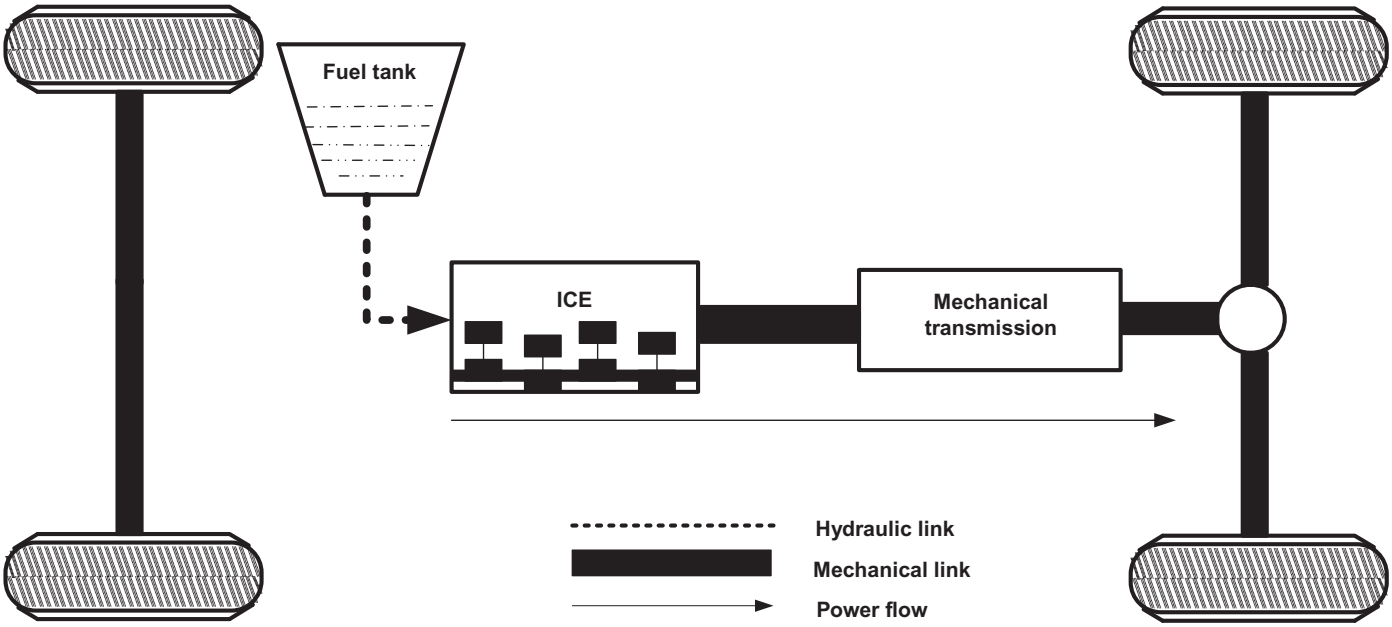


FIG. 31.4 Configuration of ICE-based vehicles [6].

mechanical transmission. An ICE-based power train is shown in Fig. 31.4. It consists of a fuel tank that provides onboard high-density-energy source, the internal combustion engine, and a mechanical transmission to transport the power from engine to wheel. The ICE vehicles score in driving distance because of the high energy density of liquid hydrocarbon fuels and dominate in recharging times as a refilling station takes minutes, compared with hours of battery charging time in electrified vehicles [6,29]. The main drawbacks of the conventional ICE vehicles are poor efficiency to convert the fuels into useful power and excessive tailpipe emission, which produces harmful impact on the environment. It has been proved that the maximum fuel conversion efficiency of conventional ICE-based vehicles is 25%–30% at best [6,7]. The main reason of inefficiency of ICE vehicles is the mismatch of engine power characteristic with the real load characteristic of the vehicles as shown in Fig. 31.5, poor efficiency of mechanical transmission and waste of kinetic energy during braking [29]. Although

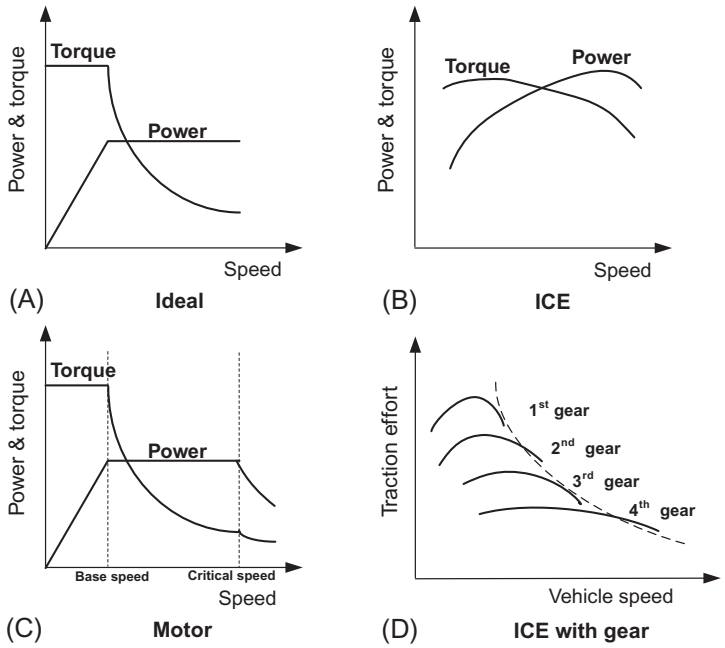


FIG. 31.5 (A) Ideal torque-speed characteristic for vehicles, (B) torque-speed characteristic of ICE, (C) torque-speed characteristic of electric motor, and (D) torque-speed characteristic of ICE with gear arrangement [29].

internal combustion engines have been used for more than a century, significant improvements in fuel economy, energy efficiency, and emission reduction have been achieved, and still, great research for optimization is going on.

31.3.2 Battery Electric Vehicles

New environmental concerns over the amount of pollutants released into the atmosphere by internal combustion engines (ICE), unstable petroleum prices in international market, and various emission regulations such as the California Air Resources Board (CARB) have mandated the concept of zero-emission vehicle (ZEV). This becomes a powerful motivation for the use of battery electric vehicles.

The concept of electric vehicles is based on electric drives that consist of the electric motor, power modulator, and onboard energy source and a controller. A simplified architecture of a BEV is shown in Fig. 31.6. A BEV has various advantages such as zero emission, high efficiency, independence of petroleum fuels, less noise, safe, and smooth operation. Moreover, while the maximum efficiency of the ICE vehicle can be 30%–35%, electric propulsion system drawing the power from battery can operate with a peak efficiency of 90% [4–8]. Also, electric vehicles have the capability to recover the waste energy through regenerative braking.

Apart from significantly large battery charging time, lower flexibility, and dynamic performance, an important limitation of BEV is its limited operating range per cycle of battery charge. For BEVs to compete against ICE vehicles, advanced energy sources and intelligent energy management system would play key roles.

31.3.3 Hybrid Electric Vehicles

A hybrid electric vehicle (HEV) is powered by the existing ICE technology and a suitable electric drive system. According to technical committee 69 (electric road vehicles) of the International Electrotechnical Commission, "a hybrid electric vehicle (HEV) is a vehicle in which at least one of the ESSs or converter can deliver electric energy." Conceptually, HEV uses two energy sources, namely, a fuel (like gasoline, diesel, and hydrogen) and stored energy (as in battery, ultracapacitor, and flywheel), to propel the wheel. The concept of HEV is to combine the EV and ICE vehicle so that better fuel utilization, good dynamic performance, and reduced tailpipe emission can be achieved, and their respective limitations can be overcome [6–9].

The major advantages of HEV are extended electric range of operation, good fuel economy, higher efficiency, and sufficient onboard power to meet the vehicles' demand in all driving profile. Combining automobile technology with electric technology adds complexity in controls and makes the system heavier and costly. Management and control of power flow from more than one energy sources to the load is a major concern and has to be treated in an optimized way so that better utilization of energy at predicted cost is achieved [6,10]. Fig. 31.7 shows the conceptual power-flow diagram of HEV.

To meet the desired load demand and to optimize the utilization of energy source(s), there are following possible operating modes to combine the two energy sources as illustrated in Fig. 31.7:

Mode I—Energy source A alone supplies power to the load.
Mode II—Energy source B alone supplies power to the load.

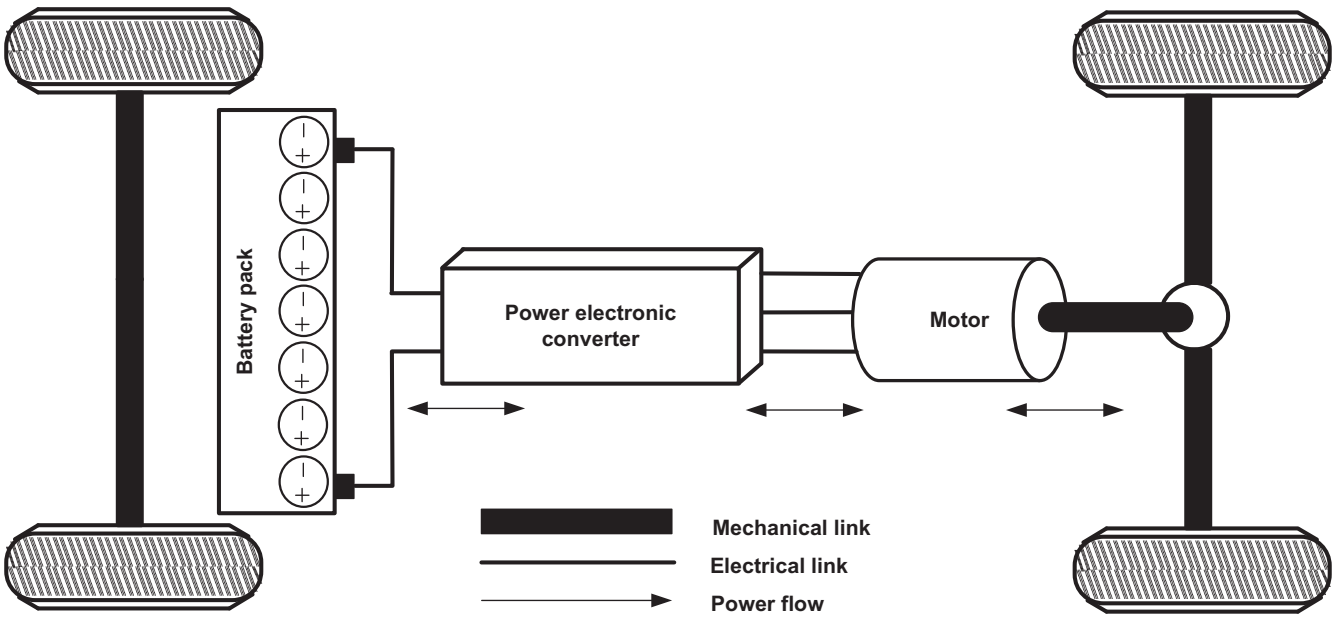


FIG. 31.6 Topological structure of BEVs [6].

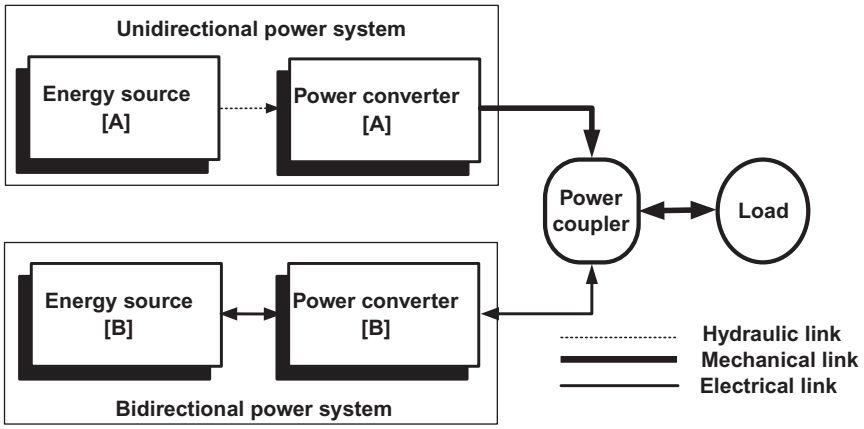


FIG. 31.7 Power flow in HEVs [78].

Mode III—Both energy sources A and B supply power to the load simultaneously.
Mode IV—Energy source B draws power from energy source A.
Mode V—Energy source B draws power from load at the time of braking (regenerative braking).
Mode VI—Energy source A supplies power to energy source B and the load simultaneously.
Mode VII—Energy source B draws power from energy source A and load simultaneously.
Mode VIII—Energy source A supplies power to energy source B, and energy source B supplies to the load.
Mode IX—Energy source A supplies power to load, and load supplies power to energy source B.

Energy source A could be gasoline/diesel/fuel cell, and power converter A is unidirectional in nature and converts chemical energy into mechanical energy. Energy source B could be a battery and/or ultracapacitor, and power converter B is bidirectional in nature and delivers electric output. Topological configuration of HEVs is based on energy utilization scheme of energy sources. In the automobile industry, development trends are toward mounting sophisticated electric systems and replacing various mechanical and hydraulic systems to provide more comfort and to increase safety [8].

HEVs are traditionally classified into four categories: series hybrids, parallel hybrids, series-parallel hybrids, and complex hybrids, where the entire configuration brings together the electric and mechanical power through various components.

31.3.3.1 Series Hybrid Electric Vehicles

A series hybrid is an HEV that has two energy sources empowering an electric motor that propels the vehicle. SHEVs are the simplest form of HEVs in which an ICE is mechanically coupled with an electric generator that, in turn, is connected to the electric motor and electrochemical battery pack through a power electronic converter as shown in Fig. 31.8. With the help of generator, mechanical power of ICE is transformed into electric power. The transformed electric power can be used to

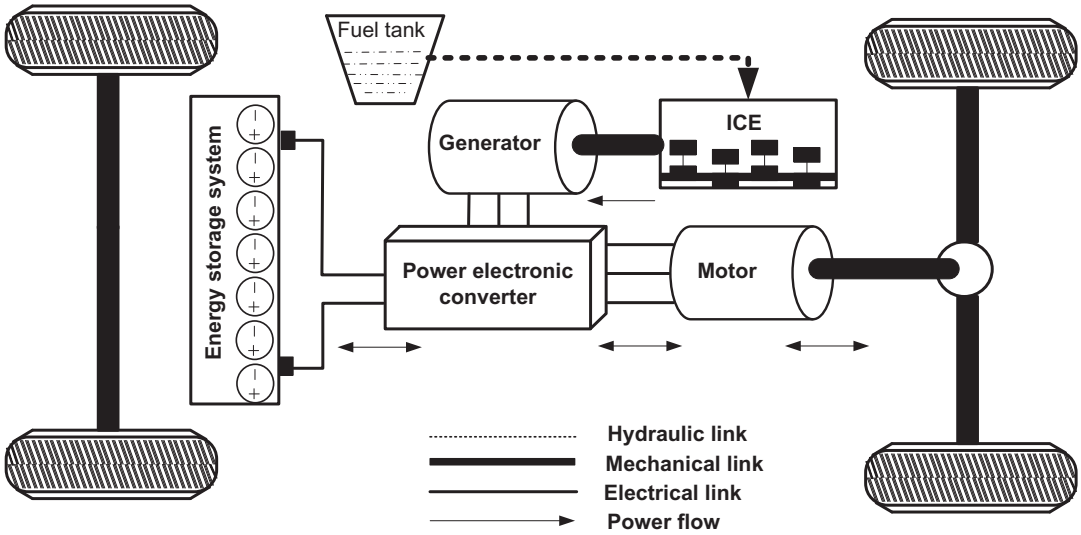


FIG. 31.8 Architecture of an SHEV [6].

charge the battery or can evade the battery to supply the electric motor to propel the vehicle, or both can happen simultaneously by means of power electronic converter [5,10]. The power flow from fuel tank to power electronic converter is unidirectional and from battery to electric motor is bidirectional.

Basically, it is ICE-based EVs where there is no mechanical link between ICE and wheel. The start/stop of ICE is controlled by the battery state of charge (SOC). When the battery reaches at a preset minimum SOC, the ICE starts in order to charge the battery. The ICE stops when the battery has reached a desirable maximum SOC. The control algorithm for the optimal operation of engine, having high efficiency and low fuel consumption, is selected such that the battery SOC should be maintained at around 65%–75% of full charge [9]. However, power transportation from energy sources to the wheel takes two stages of power conversion (mechanical to electric and electric to mechanical) and leads to increased energy losses and reduction in overall efficiency of the vehicle. All possible combinations (modes I–IX) of two energy sources are applicable for the SHEVs, but practically, only modes I–VI have been used so as to extend the life of battery [6]. The mechanical decoupling between the engine and wheels increases the degree of flexibility and reduces the complexity. Since the electric motor has the desired torque-speed characteristic, multigear mechanical transmission system can be eliminated. Simplified construction, control strategy, and reduced costs are the salient features for such a system. However, addition of generator and size of propulsion unit are two major concerns. The SHEVs are best suited for city driving where frequent "starts" and "stops" occur over a part of distance being traveled [5].

31.3.3.2 Parallel Architecture

In a parallel hybrid configuration, ICE and electric motor are connected in parallel to deliver power to the wheel as shown in Fig. 31.9. The powers from electric motor and ICE are pooled together with the help of mechanical coupling. However, the mechanical coupling adds to the complexity in control algorithm for the vehicle. The vehicle can be driven with the ICE, the electric motor, or both simultaneously, and therefore, it is possible to feed the desired amount of power at any given period of time [5–10]. In parallel HEV, except modes VII, VIII, and IX, all other modes (I–VI) can be used for better utilization of energy sources and reliable operation [6]. In this configuration, efforts are made to operate the electric motor alone at lower speed and ICE alone at higher speeds. Thus, at higher speed, ICE is operated at most efficient point, and hence, higher efficiency and better fuel consumption along with reduced tailpipe emission can be achieved. In case of acceleration or hill climbing, both the power sources are activated to fulfill the desired power demand. When ICE is working alone or in case of regenerative braking, the electric motor can operate as a generator to charge the battery.

As compared with series HEV, elimination of generator leads to single-stage power conversion that increases the efficiency and reduces the weight and cost of the vehicle. The parallel coupling of the power sources leaves space for further research and improvement of vehicle's performance. The major research efforts on parallel HEVs are focused on the implementation of continuously variable transmission (CVT) instead of a fixed-step transmission that gives the freedom to operate the ICE at its most efficient point at demanded torque [9].

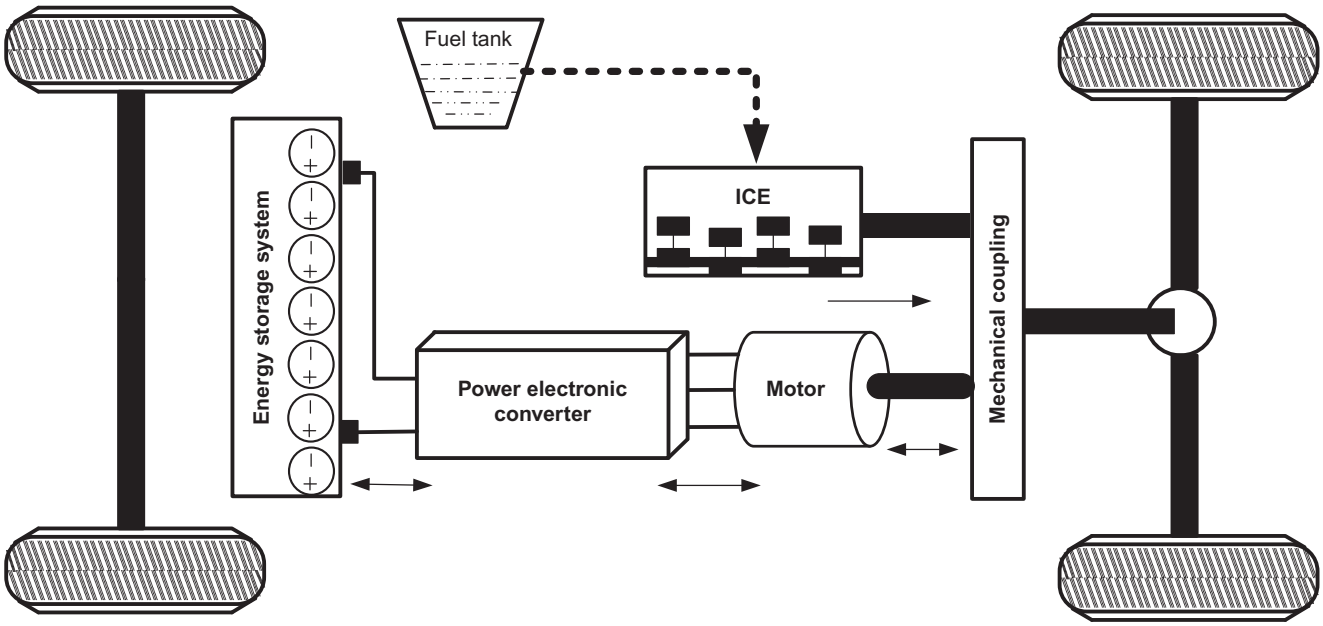


FIG. 31.9 Architecture of parallel HEV [6].

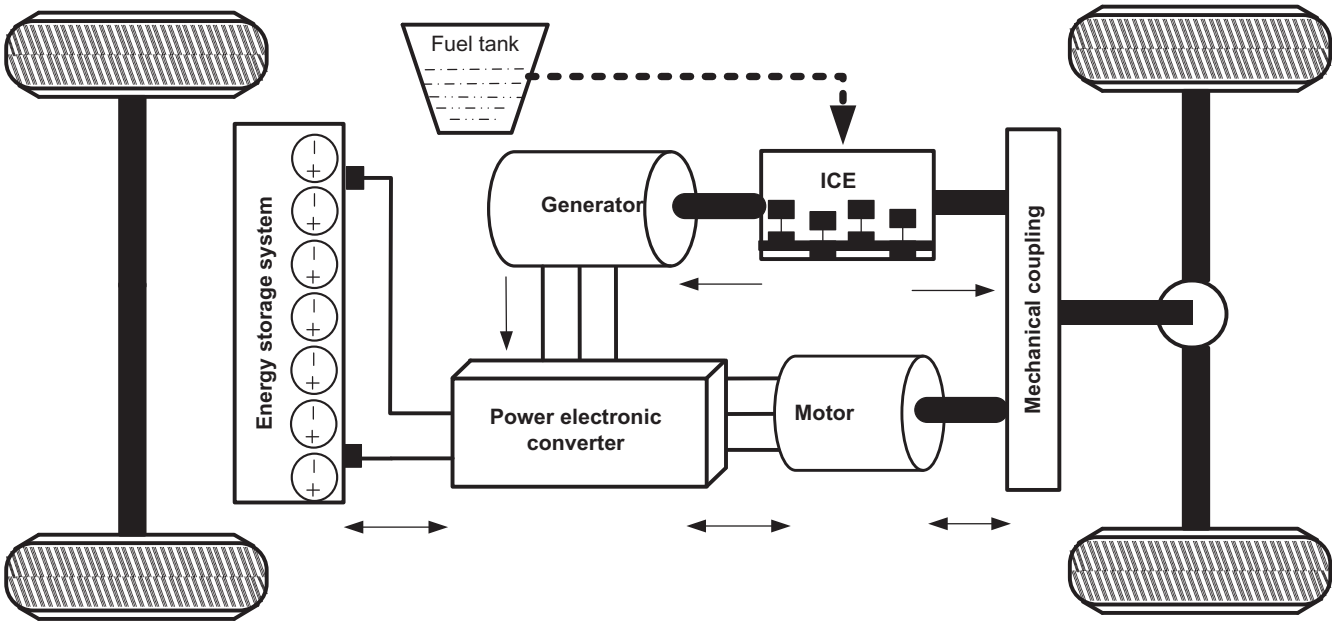


FIG. 31.10 Architecture of series-parallel HEVs [6].

31.3.3.3 Series Parallel Architecture

Series-parallel HEV is an integration of the series and parallel hybrids as shown in Fig. 31.10. The configuration introduces an additional mechanical link (unlike the series hybrid) and an additional generator (unlike the parallel hybrid) to facilitate the advantages of both configurations [4–10]. Among various possibilities in series-parallel hybrids, the general classification includes electric-intensive and engine-intensive. In electric-intensive configuration, electric motor is more dominating than the ICE. In engine-intensive configuration, ICE is more dominating than electric motor [10]. Accordingly, the dominating components are designed. The operating modes (start, normal driving, acceleration, deceleration, braking, and battery charging) of electric-intensive and ICE-intensive are almost the same except for the normal driving mode. In normal driving mode, efforts are made to operate the engine at its most efficient point. Therefore, in ICE-intensive configuration, the engine propels the wheels solely, and in electric-intensive configuration, the ICE can assist the electric motor to propel the wheels. Although the series-parallel hybrid vehicle incorporates the advantages of both the series and parallel hybrid, the use of additional electric and mechanical components (generator and planetary gear arrangement) adds to the complexity, weight, and costs.

31.3.3.4 Complex Hybrid System

All the configurations discussed previously are implemented for single-axle propulsion, for either the front or the rear wheel. A new hybrid scheme known as complex hybrid configuration is designed for dual-axle propulsion. In such an architecture, illustrated in Fig. 31.11, both the front and rear wheels propel the vehicle. In this configuration, the front-wheel and rear-wheel axles are decoupled from each other, and there is no mechanical link between them; hence, both the axles are driven independently [10]. In complex hybrid vehicle, the electric generator offers bidirectional power flow, whereas in case of series-parallel, it offers unidirectional power flow. However, both the configurations involve ICE, electric generator, and motor to propel the vehicle. The capability of complex hybrid system, to drive the wheels by either electric propulsion or hybrid propulsion or combination of both, offers additional flexibility and reliability. The front wheels are propelled by hybrid propulsion system, and rear wheels are propelled by electric propulsion system or vice versa. The operating modes for both the scheme are almost common, except when front wheels are propelled by hybrid system, all the wheels are driven; however, when front wheels are propelled by electric system, only front wheels are driven at starting [8–10]. A planetary gear arrangement is used to coupled ICE, front electric motor, and front axle altogether. Independent control of front and rear wheels provides smooth vehicle operation and flexibility in casing. This, however, increases complexity and costs. Also, regenerative braking in all four wheels can significantly improve efficiency of the system and hence fuel economy.

31.3.4 Plug-in Hybrid Electrical Vehicles

Plug-in hybrid electric vehicle is a transitional technology between BEVs and HEVs. The IEEE (board of directors, 2007) defines a PHEV as "any hybrid electric vehicle that contains at least (i) a battery storage system of 4 kWh or more, used to power the motion of the vehicle; (ii) a means of

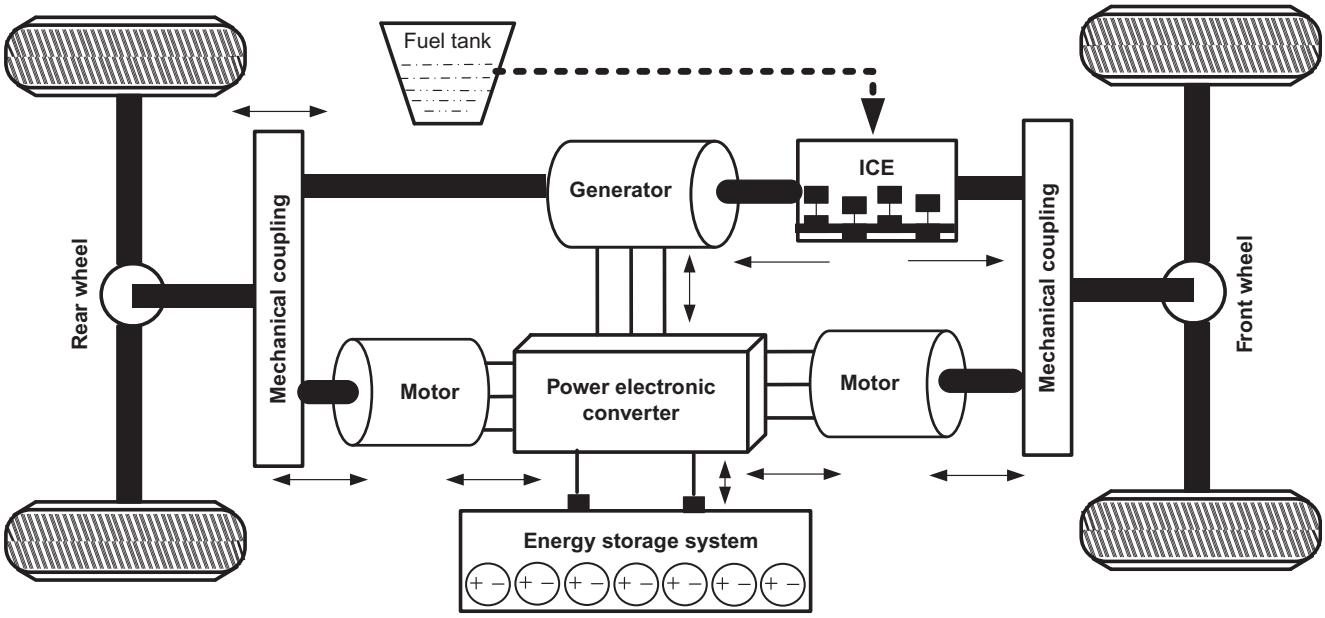


FIG. 31.11 Operating modes of complex HEVs [6].

recharging that battery system from an external source of electricity; and (iii) an ability to drive at least 10 mi in all-electric mode, and consume no gasoline" [15]. Conceptually, a PHEV is a HEV with large battery pack that can be recharged from the external source (utility grid or renewable source of energy) to extend the all-electric range (AER) of the vehicles as shown in Fig. 31.12.

In this vehicle, fuel tank and battery pack both can be recharged by external sources and are entirely different from hybrid vehicles that do not utilize any electric energy from the external sources or grid. When the battery pack is fully charged by external source, PHEV operates as EV with extended AER (30–60 km) and then switches to hybrid mode when battery reaches its predefined SOC or vehicle demands extra power for acceleration [13,14]. Moreover, not only PHEV has the capability to charge the battery pack from the grid, but also it will be able to supply the power to the grid, and hence, the vehicle-to-grid (V2G) concept is evolved [15]. The emerging technology of V2G must be bidirectional in nature so that grid can transfer power to the vehicle in charging mode, and vehicle delivers power to the grid in discharging mode at peak hours. All vehicles with V2G capability must meet the IEEE Standard 1547 for connecting to the utility.

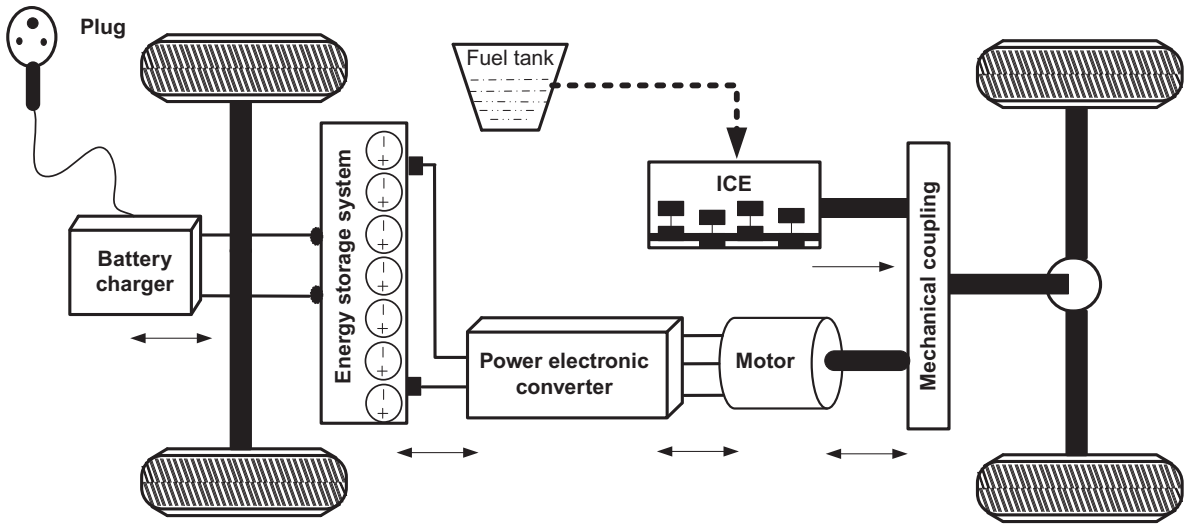


FIG. 31.12 Schematic diagram of PHEVs [6].

31.3.5 Fuel Cell Vehicles

In recent times, fuel-cell vehicle (FCV) is an upcoming technology, which involves automobile, electric, and chemical engineering. A fuel cell is a chemical engine that produces electricity from hydrogen, emitting only water as a by-product. The electricity produced is used for driving electric motor coupled with wheel of the vehicles. Fuel-cell technology offers the advantages of portable power supply. Unlike ICE, a fuel cell directly converts chemical energy into electric energy without internal combustion and pollution. In contrast to a battery, the fuel cell generates electric energy rather than storing it and continues to supply energy as long as fuel is fed [9].

Fuel-cell vehicles (FCVs) can be fueled with pure hydrogen gas stored on board in high-pressure tanks. They can also be fueled with hydrogen-rich fuels including methanol, natural gas, or even gasoline; these fuels must first be converted into hydrogen gas by an onboard device called a "reformer." This will add cost, complexity, and weight to the vehicle but will make the fuel distribution easier [28]. FCVs fueled with pure hydrogen emit no pollutants, only water and heat, while those using hydrogen-rich fuels and a reformer produce only small amounts of air pollutants. In addition, FCVs can be twice as efficient as similarly sized conventional vehicles and may also incorporate other advanced technologies to increase efficiency [9]. A conventional FCV system is shown in Fig. 31.13, where hydrogen-enriched fuel is first refined by the reformer to acquire pure hydrogen gas. This hydrogen gas is fed to fuel-cell stack where it directly meets oxygen of the atmosphere and undergoes a chemical reaction; consequently, electricity is produced. The output power of fuel-cell stack is processed by *PEC* to meet the power requirement of the EPS.

Since the power flow from the fuel cell to propulsion unit is unidirectional, to recover the braking energy by means of regenerative braking, storage medium such as battery and ultracapacitor can be included in the system. The storage unit stores energy and supplies to propulsion system at the time of acceleration to assist the fuel cell [27]. The integration of ICE and battery pack with fuel-cell system gives the concept of hybrid FCVs where all the configuration and advantages of HEVs can be utilized. With suitable power electronics arrangement, FCVs can also be operated as plug-in fuel-cell vehicles (PFCVs) where battery pack can be charged from grid or discharged to supply the grid [34]. Higher efficiency, reliability, and quieter operation with negligible emissions are some of the important features, which continue to attract the attention of researchers. As efforts are being directed to further improve the fuel-cell technology along with significant cost reduction, it has high potential to energize future automobile [8,9]. A fuel-cell system integrated with vehicular propulsion system must have the ability to compete against the ICE vehicles on cost, weight, onboard energy density, start-up, and transient response with the attainment of benefits such as zero emission and higher efficiency of the battery-operated vehicles.

Different types of electrified vehicles have their own capabilities and limitations in terms of emission rate, performance, fuel efficiency, durability, size, weight, cost, safety, and comfort. Among different types of electrified vehicles, HEV is the only one that currently has the potential to compete the ICE vehicle in terms of performance and all driving profiles and offers advantages like extended electric range of operation, good fuel economy, higher efficiency, sufficient onboard power, and better dynamic response [5–10]. However, integration of automobile technology with electric technology adds complexity in controls and makes the HEV system comparatively bulky and costly. At present, HEV technology is rated as a promising technology that is growing rapidly and capturing significant market space at a fast growth rate [7–9]. Plug-in HEVs are currently at the commercialization stage. To be commercially viable, they require good energy policies and infrastructure for charging stations in the near future [13–15]. The efficiency

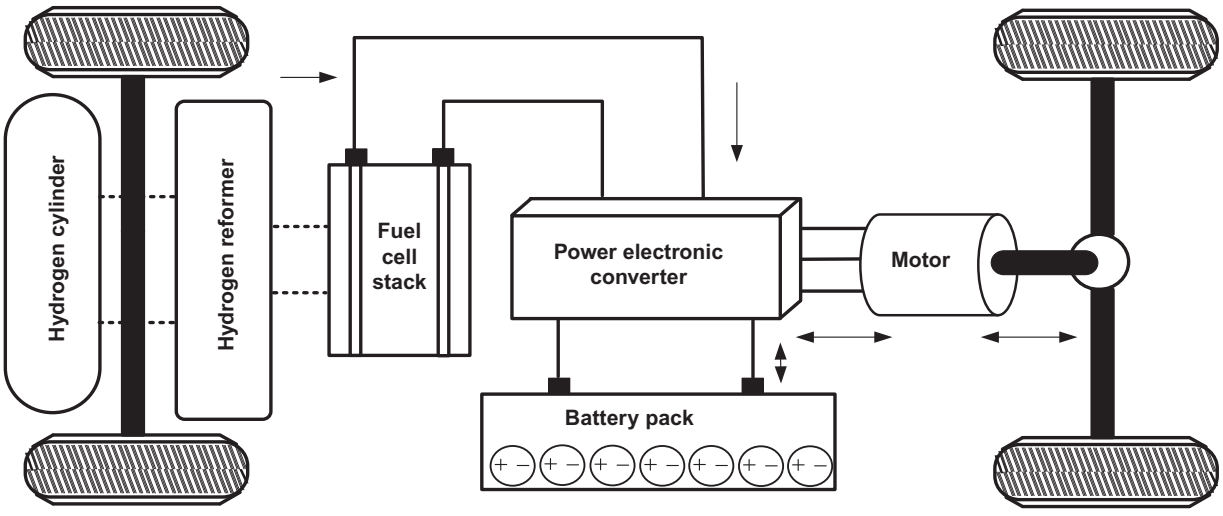


FIG. 31.13 Schematic diagram of FCVs [6].

analysis from well to wheels, the concept of V2G and G2V, and the impact of charging station on the grid are the major issues that are being researched for successful commercialization. On the other hand, fuel-cell vehicles, powered by hydrogen, are considered as the future of EVT [27,28]. The different characteristics and issues of ICEV and EVT presented in [8] are revised and summarized in Table 31.2.

31.4 Electrical Propulsion System

The sustainability of EVT is relying on maturity, which depends on technological advancement and development of its components such as ESS, PEC, electric motor, and ECU [29,78]. The ESS replaces the fuel tank and fulfills the energy requirement of the electric vehicular system.

TABLE 31.2 Different characteristics of ICEV/EV/HEV/PHEV/FCV [4]

Characteristic	Propulsion system	Energy storage	Energy source infrastructure	Advantages	Drawbacks	Important issues
ICE vehicles	■ ICE based drives	■ Fuel tank	■ Petroleum products with refueling station	■ Matured technology ■ Fully commercialized ■ Better performance ■ Simple operation ■ Reliable and durable	■ Less efficient ■ Poor fuel economy ■ Harmful emission ■ Comparatively ■ Bulky	■ Fuel economy ■ Harmful Emission ■ Highly dependency on petroleum products
EVs	■ EPS based drive	■ Battery ■ Ultra capacitor ■ Flywheel	■ Electrical energy with charging facilities	■ Energy efficient ■ Quite and Zero emission ■ Independency from petroleum products ■ Smooth operation ■ Commercialized	■ Limited driving range ■ Higher recharging time ■ Poor dynamic response	■ Size and weight of battery Pack ■ Vehicle performance ■ Infrastructure for charging station
Hybrid EVs	■ EPS and ICE based drive	■ Fuel tank ■ Battery ■ Ultra capacitor ■ Flywheel	■ Electrical power ■ Petroleum products with refueling station	■ Higher fuel economy ■ Very low emission ■ Long electric driving range ■ Reliable and durable ■ Commercialized	■ Costly and Bulky ■ Complex system ■ Complexity in control algorithm ■ Large component count	■ Power management of multi input source ■ Size and weight of battery Pack and ICE ■ Integration of components
Plug In HEVs	■ EPS and ICE based drive	■ Fuel tank ■ Battery ■ Ultra capacitor ■ Flywheel	■ Electrical power with charging station ■ Petroleum products with refueling station	■ Lower emission ■ Higher fuel efficient ■ Extended electric driving range ■ V2G or G2V capability ■ Partially commercialized	■ Higher complexity ■ Impact on grid ■ Higher initial cost ■ Sophisticated electronic circuitry ■ Battery technology	■ Size and weight of battery pack and ICE ■ Charging station infrastructure ■ Power flow control ■ Impact on grid
FCVs	■ EPS based drive	■ Fuel cell stack ■ Battery ■ Ultra capacitor	■ Hydrogen cylinder or Hydrogen enriched fuel ■ Hydrogen refueling station	■ Ultra low emission ■ Highly efficient ■ Independency from petroleum products ■ Competent driving range ■ Reliable and durable	■ High cost ■ Slow transient response ■ Not commercialized yet ■ Sophisticated ECU	■ Cost of fuel cell ■ Cycle life and reliability ■ Infrastructure for Hydrogen conditioning, storage and refilling system

Basically, ESS provides electric energy that has been processed and utilized by the other components of EPS. The electric motors transform the electric energy into mechanical energy or vice versa, as and when required. It converts electric energy of the ESS into mechanical energy to meet the power demands of the vehicle. The reversible process can also be achieved by regenerative braking, or electric energy can also be generated by electric motor to charge the ESS. The power electronic converters (PECs) are used to modulate power with suitable voltage and current between ESSs and electric motors. For vehicle acceleration, PECs supply required power to the electric motor to achieve the demanded operation. On the other hand, PECs can also be used to utilize the recovered energy of regenerative braking for the charging of ESS. The electronic controllers are composed of sensors, digital processors, and interfacing circuitry to generate the control signals for PECs and other electric and mechanical components.

In order to achieve the vision of sustainable EVT, electric propulsion system should address some important issues such as driving profile, weight and volume of vehicle, reliability and flexibility, packaging and installation, cooling system and maintenance, and all at affordable costs [16,79]. At present, the major challenges of EPS manufactures are to design and implement electric machines and power electronic converters that give better performance and can be more easily integrated for next-generation vehicles.

A functional block diagram of electric propulsion system, including the possible types of motors, computer-aided design methodologies, power converter devices/topologies, control hardware, software, and strategies, is shown in Fig. 31.14.

31.4.1 Energy Storage System

The strength of ESS is an important factor and plays vital role in vehicular electrification [17–20]. Basically, ESS constitutes the

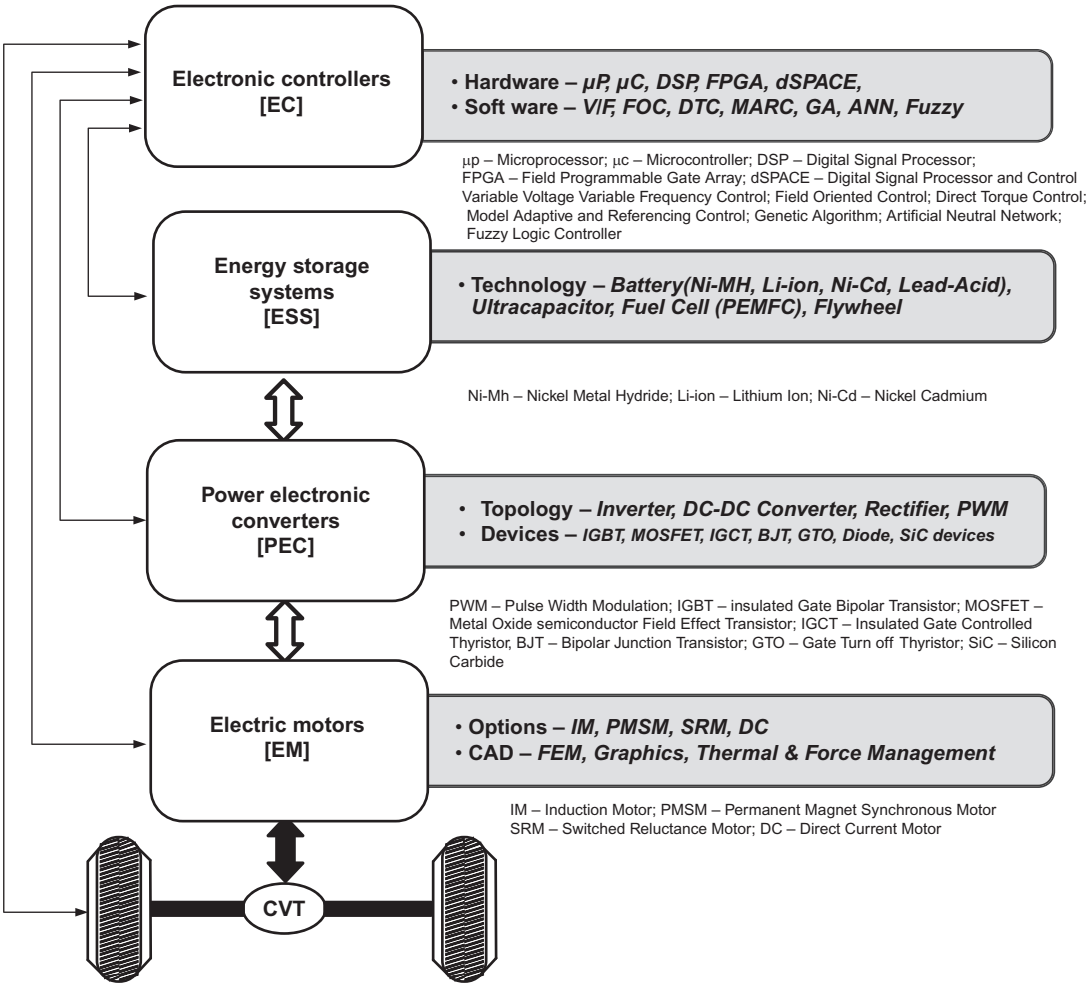


FIG. 31.14 Functional block diagram of electric propulsion system [4]. Modified from C.C. Chan, Y.S. Wong, Electric vehicles charge forward, IEEE Power Energy Mag. 2(6) (2004) 24–33.

source (fuel cell) and onboard energy storage devices that include battery, ultracapacitor, and flywheel. Battery and fuel cell both produce onboard electric energy by means of electrochemical energy conversion; however, a battery stores energy, whereas a fuel cell generates energy. Ultracapacitor relies on electrostatic principle to store energy, and therefore, it has capability to store high specific power rather than energy [18]. Use of flywheel is considered an optional technology for vehicle electrification due to weight and size considerations. The efficiency, fuel economy, and all-electric range (AER) of EVs/HEVs/PHEVs/FCVs are highly dependent on the onboard ESS of the vehicles. The ESS units must be sized so that they store sufficient energy (in kilowatt hours) and provide adequate peak power (in kilowatts) for the vehicle to have a specified acceleration performance and capability to meet appropriate driving cycles [8]. The major factors that affect the design of ESSs for vehicular application include energy density, power densities, life cycle, size, safety, maintenance, and recyclability at projected cost. The basic characteristics of specific power (W/Kg) versus specific energy (Wh/kg) of fuel cell, battery, ultracapacitor, and flywheel in comparison with petroleum-fuel-based ICE are shown in Fig. 31.15.

31.4.1.1 Battery

Battery converts chemical energy into electric energy and vice versa at the time of charging and discharging, respectively. The electrochemical battery is a combination of independent cells that possess all the electrochemical properties. Each cell is capable to store or deliver a significant amount of energy individually or in combination based on their connections [30]. High energy density, modularity, flexibility, and affordability are the factors that guide the battery technology on the road map of vehicle electrification [17]. In EVT, battery stores major onboard energy and contains high energy and power density to meet complete driving cycles of vehicle operation. The basic characteristics of battery for different vehicles are different. High-energy-density batteries are required for EVs, whereas high-power-density battery is required for HEVs and FCVs. For PHEVs, intermediate battery technology is required so that it can match the energy density of an EV battery and the power density of an HEV battery. However, batteries that fulfill the demand of PHEVs are yet to be designed specifically. A suitable battery type for EVT is the lithium-based battery such as lithium ion and lithium polymer and lead-acid and nickel-based battery such as Ni-Cd and Ni-MH [18,30–33].

Among these, lead-acid batteries are used for short-term use because of their low energy density. On the other hand, lithium- and nickel-based batteries are preferred for medium- and long-term use, respectively. However, Ni-Cd and Ni-MH battery technologies are matured, and their potential is fully explored. Therefore, significant improvement and cost reduction in these batteries in the coming years are least expected. The inherent advantages like high energy density, low weight, and low cost of lithium-based batteries invite attraction from automakers. In addition, the potential of lithium-based batteries is still not fully explored, and maturity level is yet to be achieved. Therefore, lithium-based batteries are considered as future's battery technology to power the electrified vehicles. The dominating characteristics and

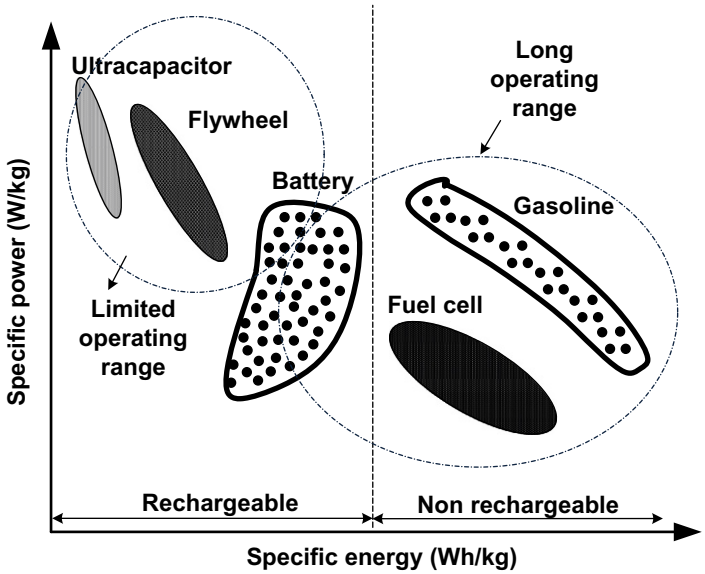


FIG. 31.15 Specific power versus specific energy characteristic for different ESS [8]. Reproduced with permission from C.C. Chan, The state of the art of electric, hybrid, and fuel cell vehicles, Proc. IEEE 95(4) (2007) 704–718.

TABLE 31.3 Characteristics of different battery technology [4]

Battery/parameters	Lithium-based		Nickel-based		
	Ion	Polymer	Ni-MH	Ni-Cd	Lead acid
Nominal cell voltage	3.6	3.0	1.2	1.2	2.0
Specific energy (Wh/kg)	35	100–200	60	40–60	35
Energy density (Wh/L)	70	150–350	220	60–100	70
Specific power (W/kg)	∼200	>200	130	140–220	∼200
Power density (W/L)	∼400	>350	475	220–350	∼400
Self-discharge (%/M)	4–8	∼1	30	10–20	4–8
Cycle life	500–1000	200–1000	300–500	300–700	250–500
Operating temp (°C)	From −20 to 60	From 0 to 60	From −20 to 60	From −40 to 60	From −20 to 60

comparison of different battery technologies available in [4] are given in Tables 31.3 and 31.4, respectively.

31.4.1.2 Ultracapacitor

Ultracapacitor is an electrochemical device that works on electrostatic principle to store energy; therefore, it can be charged/discharged hundreds or thousands of time without degrading the performance [34–36]. Basically, in ultracapacitor, porous carbon electrodes, which offer high surface area (1000 m^2gm^{-1}), are impregnated with electrolyte and small charge separation (10 Å) created by the dielectric separator between the electrodes as shown in Fig. 31.16. Appropriate modification in material selection and fabrication brought the ultracapacitor far away from conventional capacitor with very high capacitive (1000–5000 F) density [34]. Ultracapacitor stores energy higher than traditional capacitor but lower than battery, and hence, it can be used for applications, reserved for battery and capacitor.

The detailed comparison is given in Table 31.5. It offers high power density, long cycle life, and efficient operation. Since the rates of charge and discharge are determined by its physical properties, an ultracapacitor can release energy much faster (with more power) than a battery that relies on slow chemical reactions [34–36]. Ultracapacitors have been used for ICE-based vehicle tanks and submarines starting due to its ability of burst power delivery. In EVT, ultracapacitors can be used as primary energy devices for power delivery during starting, acceleration, and hill climbing and for recovery of braking energy during regenerative braking. The combination of ultracapacitor with a battery improves the energy performance of the former with greater energy storage capability of the latter [18]. It can downsize and extend the life of a battery, reducing maintenance and replacement costs. In future, it is expected that ultracapacitor can become a major dominating technology in vehicle electrification; however, desired energy density at reasonable weight and cost is a major concern.

The application of ultracapacitor in vehicle electrification is under development, and significant improvement has to be done for achieving maturity and commercialization in mass scale.

31.4.1.3 Fuel Cell

Recent technical advancements in fuel-cell technology have constructed the road map for its application in EVT as onboard energy source [40]. Significant advantages of a fuel cell are eco-friendly, simplicity, continuous power supply, durability, and silent operation along with strict confirmation to emission norms of vehicular systems. In fact, a fuel cell combines the best features of ICE (they can operate as long as fuel is supplied) and batteries (they can produce electricity directly from fuel, without combustion), thereby reducing emissions and noise and increasing the efficiency [41]. A fuel cell is an electrochemical device that uses hydrogen (H_2) as fuel and oxygen (O_2) from air to produce electricity with water and heat as by-products as shown in Fig. 31.17. To speed up the rate of these reactions, a catalyst such as platinum is used.

In a fuel cell, chemical energy of hydrogen is directly converted into electric power, thus eliminating the intermediate steps of converting fossil fuel to heat and then electric power that enhances efficiency comparatively. The specific energy of a fuel cell is as good as gasoline; however, its specific power is much lesser; therefore, the starting performances of fuel-cell vehicles are very poor. Consequently, to improve the power density and starting performance, battery or ultracapacitor can be used in conjunction with the fuel cell for vehicular application [41,42]. Therefore, it can be said that fuel cells and ultracapacitors are made for each other to lead perfect ESS for automotive. The types of fuel cell and their detailed comparison are presented in [43–45]. Among different fuel-cell technologies presented in [43–45], a PEM fuel cell is promising and is being used as energy source in fuel-cell vehicles. It offers easy start at low temperature, comparatively high power density, simple structure, small size, maintenance-free operation, and ability to operate in hostile environment [44].

TABLE 31.4 Comparison of different battery technologies [4]

Advantages ON / OVER		Lithium Based		Nickel Based		Lead Acid
		Ion	**Polymer**	**Nickel Metal Hydride Ni-MH**	**Nickel Metal Cadmium Ni-CD**	
Lithium based	**Ion**		▪ Gravimetric ▪ Energy density ▪ Design characteristics ▪ Safety ▪ Price	▪ Price ▪ Safety ▪ Discharge rate ▪ Recyclability	▪ Operating temperature ▪ Higher cyclability ▪ Price ▪ Safety ▪ Recyclability	▪ Higher cyclability ▪ Price ▪ Safety ▪ Recyclability
	Polymer	▪ Operating ▪ Temperature range ▪ Higher cyclability		▪ Volumetric energy density ▪ Higher cyclability ▪ Price	▪ Operating temperature ▪ Higher cyclability ▪ Price	▪ Higher cyclability ▪ Price
Nickel based	**Nickel Metal Hydride (NiMH)**	▪ Gravimetric energy density ▪ Volumetric energy density ▪ Operating ▪ temperature range ▪ Higher cyclability ▪ Voltage output ▪ Self discharge rate	▪ Gravimetric energy density ▪ Volumetric energy density ▪ Operating temperature range ▪ Self discharge rate ▪ Design characteristics		▪ Operating temperature ▪ Higher cyclability ▪ Self discharge rate ▪ Price	▪ Higher cyclability ▪ Voltage output ▪ Price
	Nickel Cadmium NiCd	▪ Gravimetric energy density ▪ Volumetric energy density ▪ Voltage output ▪ Self discharge rate	▪ Gravimetric energy density ▪ Volumetric energy density ▪ Self discharge rate ▪ Design characteristics	▪ Gravimetric energy density ▪ Volumetric energy density		▪ Higher cyclability ▪ Voltage output ▪ Price
Lead Acid		▪ Gravimetric energy density ▪ Volumetric energy density ▪ Voltage output ▪ Self discharge rate	▪ Gravimetric energy density ▪ Volumetric energy density ▪ Self discharge rate ▪ Design characteristics	▪ Gravimetric energy density ▪ Volumetric energy density ▪ Self discharge rate	▪ Gravimetric energy density ▪ Volumetric energy density ▪ Operating temperature ▪ Self discharge rate ▪ Reliability	
Absolute Advantages		▪ Gravimetric energy density ▪ Volumetric energy density ▪ Self discharge rate ▪ Voltage output	▪ Gravimetric energy density ▪ Volumetric energy density ▪ Self discharge rate ▪ Voltage output ▪ Design characteristics	▪ Volumetric energy density	▪ Operating temperature range ▪ Price	▪ Higher cyclability ▪ Price

Source: c. pilot "worldwide rechargeable battery 2007–11/report/pdf."

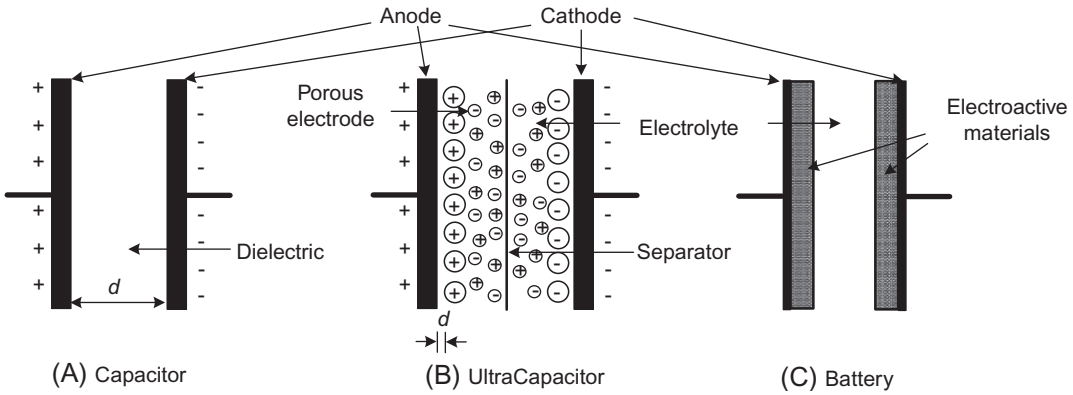


FIG. 31.16 Construction overview of (A) capacitor, (B) ultracapacitor, and (C) battery [78]. Reproduced with permission from L. Kumar, S. Jain, Electric propulsion system for electric vehicular technology: a review, Renew. Sust. Energ. Rev. 29 (2014) 924–940.

TABLE 31.5 Different characteristics of battery, capacitor, and ultracapacitor [78]

Characteristics	Battery	Ultracapacitor	Conventional capacitor
Charging time	1–5 h	0.3–30 s	10^{-3}–10^{-6} s
Discharging time	0.3–3 h	0.3–30 s	10^{-3}–10^{-6} s
Energy densities (Wh/kg)	10–100	1–10	<0.1
Power densities (W/kg)	<1000	<10,000	<100,000
Cycle life	1000–2000	>500,000	>500,000
Efficiency (%)	70–85	85–97	>95

31.4.1.4 Flywheel

A flywheel that stores and delivers mechanical energy in the form of rotational kinetic energy has been researched for many decades, but due to heavy weight and high cost, its implementation in vehicular system has been limited. Recent advancement in frictionless magnetic bearing, carbon-fiber composite materials, manufacturing technique, and sophisticated power electronic controllers has accelerated the development of flywheel energy storage system (FESS) [37]. The numerous features of advanced FESS such as higher power density, reliability, efficiency, and higher speed at reduced size made it a potential candidate for ESS in EVT [37–39]. The flywheel rim rotates in an evacuated containment that reduces frictional losses and ensures safety in case of failure.

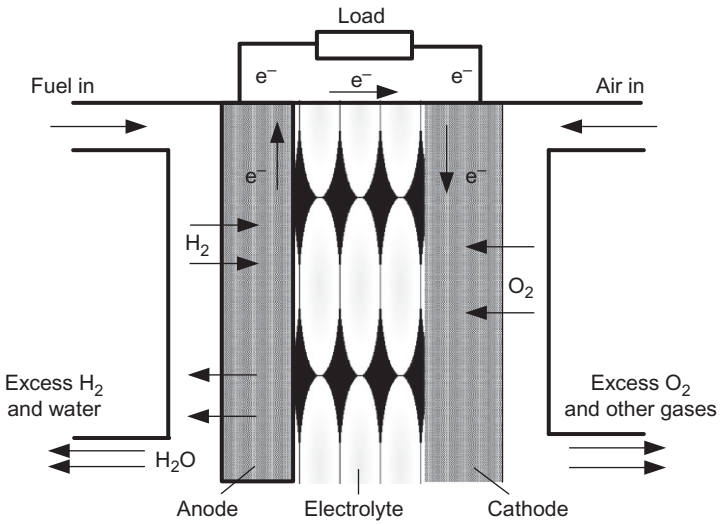


FIG. 31.17 Fuel-cell construction and operation [78].

A flywheel stores energy linear to its mass but square proportional to velocity from supply and delivers it to the load as per the requirements. The stored mechanical energy can be converted to electric energy or vice versa by means of integrated motor/generator set and PEC. Flywheel gets charged by speeding up as it accumulates mechanical energy and discharges by slowing down as it supplies mechanical energy to the EPS. The energy of regenerative braking can be recovered by charging the flywheel, which is further used for battery charging. Modern flywheels can store more energy and power than existing metal hydride or lead-acid batteries of similar weight and volume [38,39]. Unlike battery and ultracapacitor, flywheels are independent of in-depth discharge that improves its life cycle. It spins at a very high speed; therefore, safety, tensile strength of the material, and location of the placement of flywheel in EVT are prime concerns and need to be dealt with properly.

31.4.1.5 Hybrid Energy System

It can be concluded that not only the power and energy densities but also the voltage and current characteristics of different energy systems are different. Therefore, exclusive employment of one of the aforementioned energy sources cannot meet the energy and power demands of vehicle operation for all driving profiles. Compared to ultracapacitors and flywheel, a battery and a fuel cell have much higher specific energy but much lesser specific power as depicted in Table 31.6. Employment of such energy systems alone results higher cost, weight, and volume [46]. However, when these different energy systems are combined, an energy system with high power and high energy density can be obtained. Such kind of energy system is termed as hybrid energy system (HES), where batteries and a fuel cell supply the energy demand and the ultracapacitors and flywheel supply the power demand [46,47]. The combination of energy system can be chosen on the basis of vehicle design, operating profiles, and application. The prime concerns of hybrid energy system formation are their suitable integration, life expectancy, maintenance, cost, durability, and reliability.

TABLE 31.6 Comparison of different energy source and storage systems [78]

Characteristics	Battery	Ultracapacitor	Fuel cell	Flywheel
Mechanism	Chemical	Electrostatic	Chemical	Mechanical
Technology	Proved	Promising	Promising	Proved
Energy density	High	Low	Very high	Low
Power density	Low	Very high	Moderate	High
Charging time	Hours	Seconds	—	Minutes
Discharging time	Hours	Seconds	—	Minutes
Life	3–5 years	>10 years	10–20 k Hr	>20 years
Efficiency (%)	75–85	85–95	40–60	80–90
Issues	Disposal	Less	Very less	Very less

31.4.2 Electric Motor

In EVT, the electric motor needs to go through frequent starts and stops, high rate of acceleration, and deceleration, such as low-speed hill climbing and high-speed cruising along with different environmental and hostile conditions. Industrial motors, on the other hand, are usually operated at rated speed under common circumstances [16]. Thus, the electric motors used in EVT cannot be compared with motors being used for industrial processes. The electric motors used for EPS should be able to satisfy some basic characteristic for efficient operation. These characteristics are high torque for starting and low-speed hill climbing operation; high power density for acceleration and high-speed cruising for highway; high efficiency over wide torque and speed range; suitability for regenerative braking; overload capability during certain period of time; and controllability, high reliability, and robustness at affordable costs [48–50]. In addition, fault-tolerant capability, minimum torque ripple, temperature management, and low acoustic noise are other important issues for design consideration [21–24,63,64]. Suitability of electric motor in propulsion application should be strongly approved by torque-speed characteristic as discussed in [56] and illustrated in Fig. 31.18A. Moreover, the standard torque-speed characteristic of EPS is shown in Fig. 31.18B.

The choice of electric motor is the key factor in overall EPS design. A brief classification of the family of electric motor for EPS is summarized in Fig. 31.19. The commonly used electric motors for EPS include dc motor, induction motor, permanent-magnet (PM) motor, and switched reluctance (SR) motor [50–53]. Existing literature indicates that squirrel-cage rotor induction motors and PM motors are best suitable options. Also, SR motors are gaining more popularity and becoming reliable alternative for the future, while use of dc motors is declining gradually.

31.4.2.1 DC Motors

Traditionally, a dc motor has been used prominently for EPS due to its high starting torque and simple speed control. The torque-speed characteristics of dc motor exhibit good compliance for propulsion application; however, the inherent disadvantage of bulky construction, low efficiency, and the presence of mechanical commutators and brushes that aggravate maintenance requirements limit its use in light, high-speed, and maintenance-free vehicle application in hostile conditions [48–51]. Nevertheless, due to simple speed control and technical maturity, dc motors are prominent for low-power EPS. Technological advancements in power electronic converters and switches have helped to replace dc machines with commutatorless motors such as induction motors, PM motors, and SR motors. The commutatorless motors offer some tremendous advantages such as high power density, higher efficiency, and more reliable and maintenance-free operation with wide speed range over the dc motors.

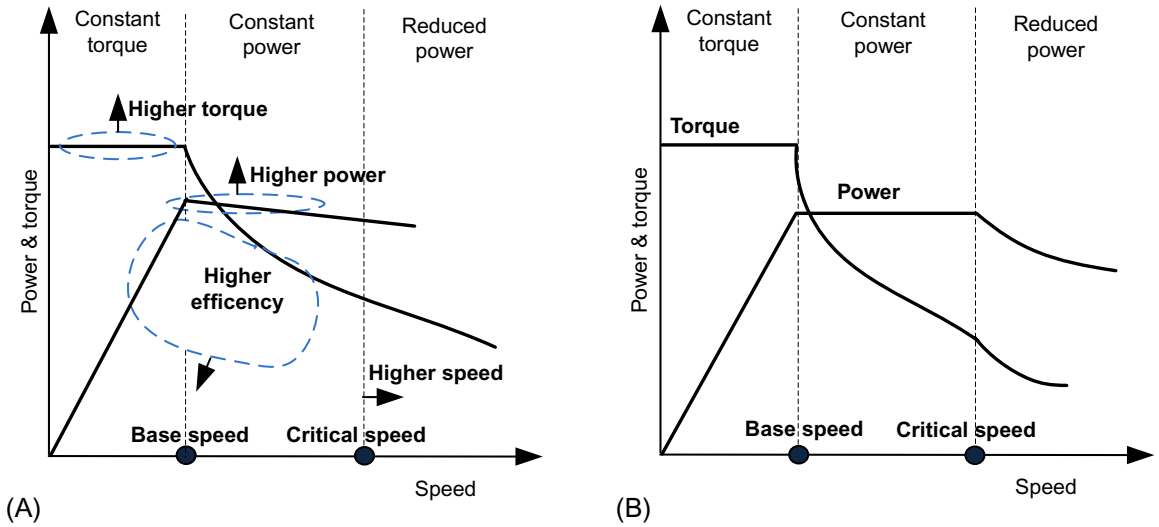


FIG. 31.18 Desired torque-speed characteristic of (A) vehicle propulsion system and (B) electric motors [56].

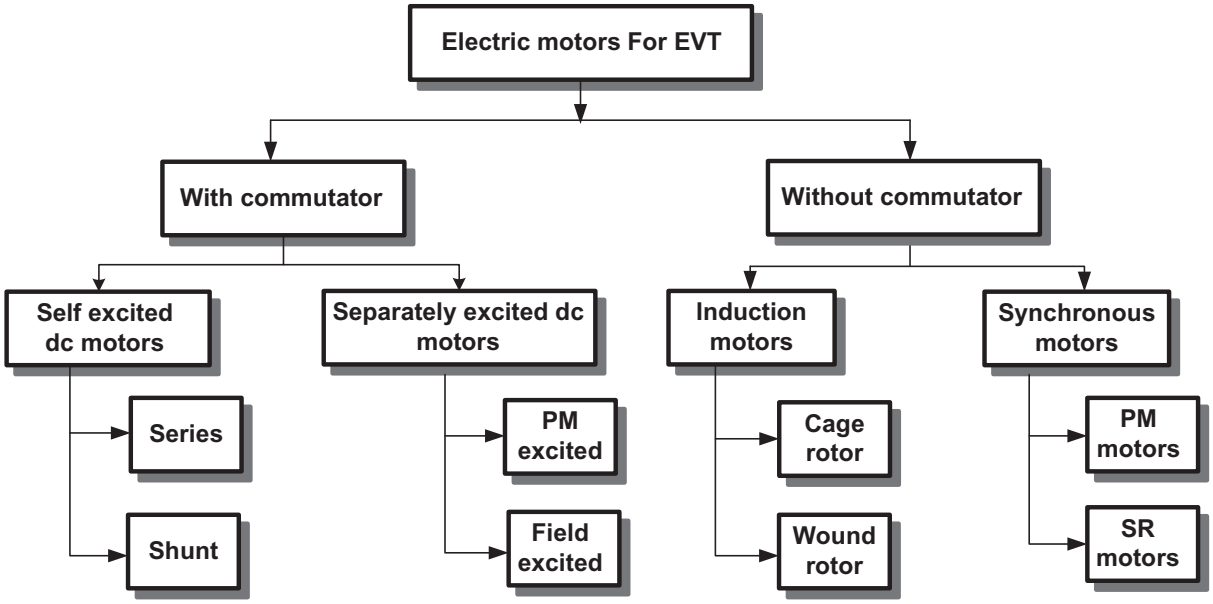


FIG. 31.19 Classification of electric motor for EPS.

31.4.2.2 Induction Motor

Induction motor (IM)-based propulsion systems are mature and are being extensively accepted as dominating candidate for EPS among various commutatorless motors. The numerous attractive features of IM are simplicity, high reliability, robustness, wide speed range, low maintenance, low torque ripple/noise, low cost, established power electronic converters, and ability to operate in hostile environment [48–53]. The behavior and performance characteristics of dc series motors can also be achieved with induction motor by employing well-matured field-oriented control (FOC) that provides decoupling of torque control from flux control [56]. The dynamic performance of IM can be further improved by applying either vector control or direct torque control (DTC) technique [57]. High-speed operation with extended constant power range of up to 4–5 times the base speed can be achieved by flux weakening, which is one of the desirable requirements for vehicle operation [56], although the high-speed operation and constant power range are limited by its pullout torque.

Apart from the various advantages, there are several disadvantages such as high losses, poor power factor, low efficiency, and low inverter usage. Moreover, its weight and volume are greater for the same power rating as compared with PM motors. These drawbacks of induction motor have been acting as speed bump in the race track. These limitations have been taken into account by the researchers. Efforts are being made to resolve these issues either at design level or by proposing new control schemes and/or converter topologies.

31.4.2.3 Permanent Magnet Motor

Among the available commutatorless motors, only permanent-magnet brushless motors have the capability to compete against the induction motors in EPS [48]. In recent times, PM motors are widely accepted by the leading vehicle manufacturers for designing the existing and upcoming EPS. Generally, PM motors are classified based on supply voltage and current as brushless dc and brushless ac. To maximize the torque density while keeping torque pulsation low, it is preferred to operate a PM machine in BLDC mode for trapezoidal back EMF waveform and in BLAC mode for sinusoidal back EMF waveform [58]. PM motors possess some inherent advantages: PMs excite the field that offers high power density and reduced weight and volume of the motor for a given power rating; due to reduced rotor losses, it offers highly efficient operation; compact packaging provides higher degree of reliability and maintenance-free operation; effective dissipation of heat into atmosphere enables efficient cooling [48–53]. Despite their numerous advantages, PM motors have some limitations such as short constant power region due to limited field weakening capability. In addition, control and management of back EMF at high speed increase size and ratings of PECs, and fault-tolerant capability is an issue. The extended speed range up to 3–4 times the base speed and enhanced efficiency of PM motors can be achieved by applying suitable control algorithms of power converters above the base speed [59]. Important design considerations for PM motors associated with fixed excitation for EPS include torque density, flux weakening capability, overload capability, stator iron losses, rotor eddy-current losses, and demagnetization withstanding capability.

The basic configurations of PM motors are classified based on the location of PMs. In conventional PM motors, PMs either are mounted on rotor surface or buried within the rotor. Surface-mounted PM (SPM) motors are widely used design and uses less magnet, whereas interior PM (IPM) motors use more magnets and offer higher air-gap flux density with higher degree of ruggedness [60]. Therefore, the interior PM motors are exceedingly being preferred for extended speed range and constant power operation over surface PM motors. In conventional PM motors, a compromise has to be made between low-speed torque capability and high-speed power capability. In order to overcome this problem, the concept of hybrid PM motor and field excitation technique has been adopted [49]. Conceptually, hybrid PM motor is either a combination of PM motor and reluctance motor or an inclusion of additional field winding that limits air-gap field. Thus, the hybrid PM motors enhance the overall operational efficiency and offer wide speed, constant power operation with more complex structures. Availability, cost, and supply issues with rare-earth PMs may affect their wide applications in EPS.

31.4.2.4 Switched Reluctance Motor

SR motor is gaining more and more attention for EPS in vehicular application. An SR motor offers tremendous potential for vehicular application especially for HEVs and FCVs [61,62]. The remarkable features of SR motors are the following: rotor without magnet and windings offers simple and robust construction that is desirable for very-high-speed and high-temperature operation; excellent torque-speed characteristics; fault-tolerant capability; and constant power region that can be extended up to 3–7 times, smooth and hazard-free operation [48–53]. Limitations of SR motors include high acoustic noise, vibrations, high torque ripple, complex control mechanism, and requirement of special converter topology. Although the cost of SR motors is relatively high, their mass production is expected to render them as cost-effective as induction motors. All the advantages are prominent for vehicular application, whereas the disadvantages are needed to be taken care properly to have feasible SR motor-based EPS.

Comparison of different motors based on desirable characteristic for EPS is shown in Table 31.7. The suitability of particular motor at particular characteristic is rated in the scale of 1–5 relatively. The point 5 indicates the higher attributes, whereas point 1 shows the poor attributes. This comparison is indicative and measured relatively on the basis of existing

TABLE 31.7 Comparative analysis of different electric motors used in EPS [78]

Characteristic	dc	IM	PMSM	SRM
Controllability	5	5	4	3
Size and weight	3	4	4.5	4
Robustness	3.5	5	4	4.5
Reliability	3	5	4	4.5
Power density	3	4	5	3.5
Efficiency	3	4	5	4.5
Speed range	2.5	4	5	5
Life time	3.5	5	4	4.5
Torque density	3	3.5	5	4
Technical maturity	5	4.5	4	3.5
Cost	3.5	5	3	4
Overload capability	3	4	4.5	4
Torque ripple/noise	3.5	4.5	4	3
Manufacturability	3	5	3	4
Improvability	2.5	3	4.5	5

TABLE 31.8 Power semiconductor devices for EPS [74]

Component	Semiconductor devices	Voltage rating (volt)	Current rating (amp)	Power rating (kW)	Switching frequency (kHz)
Inverter/rectifier for EPS	IGBTs/diodes	600–1200	100–600	20–100	5–30
dc/dc converter for EPS	IGBTs/diodes	600–1200	100–600	20–100	5–30
Inverter/rectifier for auxiliary loads	IGBTs/MOS-FET/ diodes	600–900	15–60	2–4	5–50
dc/dc converter for low-power loads	MOSFET/diodes	400–600	10–40	1–2	50–200

literature; however, it may vary with several factors like the design consideration of motor's type, placement of motor (in wheel or out of wheel), material used for magnet, core and laminations, relevant power electronics converter, and their control algorithms [21]. The main purpose of Table 31.7 is to bring out the motor technology with higher attributes to vehicular application.

31.4.3 Power Electronics Converters for EVT

For sustainable EVT, there is a need of highly reliable, flexible, and fault-tolerant electric power processing system on board to deliver high quality of power, as per vehicle demands [24]. At present, this responsibility has been taken care by the available PEC that includes dc/dc converters, rectifiers (dc/ac), inverters (ac/dc), and battery charger that is composed of ac/dc and dc/dc converters.

Individually or combination of these converters can be taken to serve the purpose of onboard power processing; however, operation of each PEC is entirely different from the other. Conceptually, PECs perform some of the critical tasks like ON/OFF switching of various actuators, valves, and equipments; power conditioning and voltage/current modulation to create compatibility among the sources; traction motors; and auxiliary loads like air conditioner, head lamp, power steering, power window, etc. [63]. PECs not only serve the purpose of converting electric power from one form to another (dc/dc and dc/ac) but also help to step up or step down the system voltage level on board.

These PECs are composed of power electronic devices that play significant role and are evolving rapidly. The selection of PEC devices for EV propulsion is generally based on the requirements of the voltage rating, current rating, switching frequency, power loss, and dynamic characteristic of the system [63]. The voltage rating depends on the battery nominal voltage, maximum voltage during charging, and regenerative braking. The current rating depends on the motor peak power rating and number of devices connected in parallel. Furthermore, the switching frequency should be high enough to reduce the noise, filter size, and EMI problem with good dynamic characteristics. The device protection, packaging, reliability, and cost should also be considered while choosing particular device. Among the available power devices, the GTO, BJT, MOSFET, IGBT, and MCT are particularly suitable for EV propulsion [38]. Some of their operating characteristics as presented in [74] are given in Table 31.8. At present, the most attractive and suitable device for EVT is IGBT, which possesses high-speed characteristics of a MOSFET with the high-conductivity characteristic of a BJT. In the near future, the wideband gap (WBG) devices like SiC and GaN will be the most favorable candidate for EPS because they provide high-temperature operation, high-power-handling capability, superior dynamic characteristic, low switching losses, and high reliability [74].

In the last decade, significant advancement in converter topologies dealing with battery charger, voltage-source inverter for motor drives, and bidirectional dc/dc converter for ESS integration has been made. Regardless of this topological advancement, still conventional PEC topologies are being used in modern electrified vehicles. Therefore, PECs for EVT can be broadly classified as shown in Fig. 31.20. The classification of the PECs is done based on their basic operation rather than topological advancement.

The current trends and future status of EM, PEC, and EPS based on essential characteristics of vehicle application are summarized in Table 31.9.

31.4.3.1 PEC Configuration for EPS

PECs are controlling, managing, and optimizing the power flow among energy sources and vehicle loads, and hence, they are considered as the heart of EPS, whereas EPS is the heart of EVT. The architecture of modern EPS for EVT with interconnection among electric power system, ESS, propulsion system, and control and protection system is shown in Fig. 31.21. The main elements for the power processing and conversion comprise an ac/dc charger, a bidirectional dc/dc converter, a dc/ac inverter, and a digital controller.

Charging from utility grid inevitably needs a battery charger with power factor correction (PFC). The bidirectional dc/dc converter with a proper charging-discharging profile is required to transfer energy between the ESS and the propulsion system [73]. The plug-in charger is usually composed of ac/dc rectifier and dc/dc converter. The bidirectional dc/dc converter is placed between the add-on battery and the high-voltage bus of the HEV. The digital controller is in charge of the control and monitoring of the ac/dc charger, bidirectional dc/dc

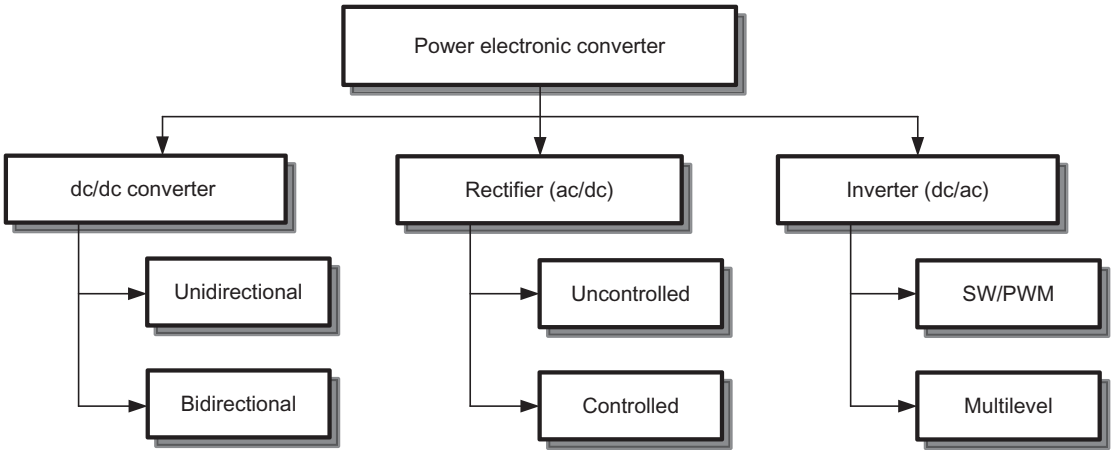


FIG. 31.20 Classification of power electronic converters.

TABLE 31.9 Present and future status of EM, PEC, and EPS [16]

Characteristic	Electric motors				Power electronic converter				Electric propulsion system			
	2010	2013	2015	2020	2010	2013	2015	2020	2010	2013	2015	2020
Power density (kW/L)	3.7	4.8	5	5.7	8.7	10.2	12	13.4	1.06	1.15	1.2	1.4
Specific power (kW/kg)	1.2	1.3	1.3	1.6	10.8	11.5	12	14.1	2.6	3.1	3.5	4.0
Efficiency (%)	90	91	92	93	91	92	94	97	90	91	93	95
Cost ($/kW)	11.1	9.5	7	4.7	7.9	6.5	5	3.3	19	16	12	8

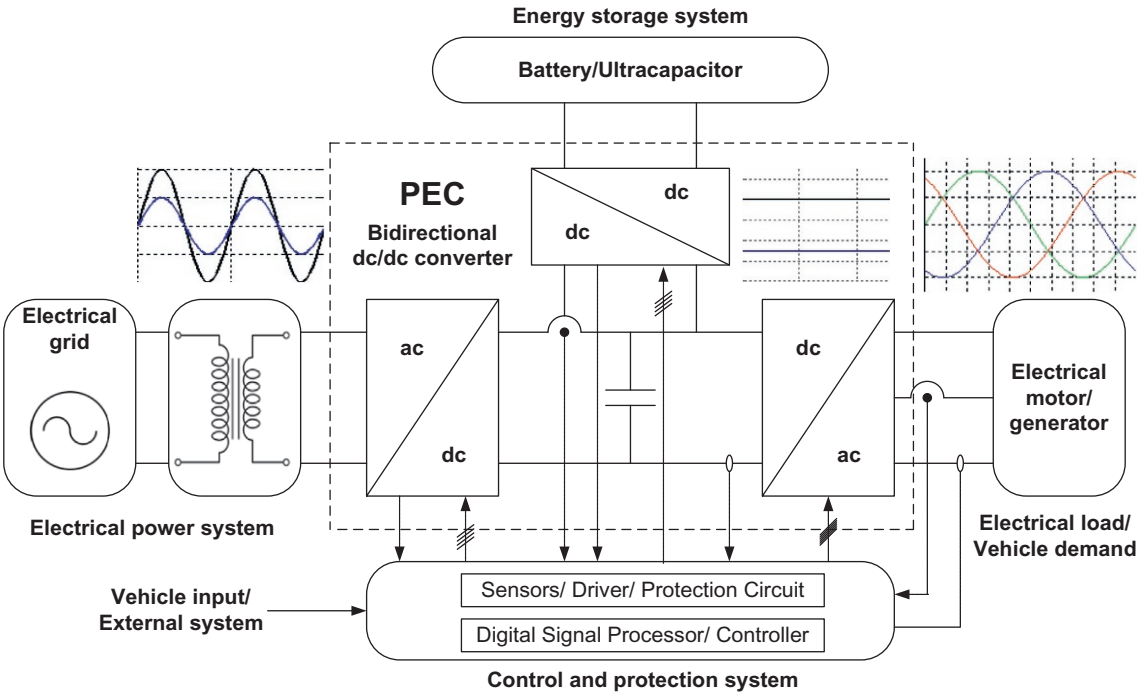


FIG. 31.21 Architecture of PECs in modern vehicular application.

converter, dc/ac inverter for propulsion, battery state of charge (SOC), and communication with external systems. Three voltage sources, that is, ac outlet voltage V_{ac}, battery voltage V_{batt}, and input to the propulsion inverter V_o, are shown in Fig. 31.21. These voltages are might be different from input/output voltage magnitude in each converter stage. This variation in voltage magnitude governs the operating modes and switching strategy of the converters under the supervision of digital controller.

The PECs contributing weight and volume of EPS are inverter, onboard charger, and bidirectional dc/dc converter. The main attention is being focused on bidirectional dc/dc converter for power-flow optimization [70]. Apart from dc/dc converter, innovative efforts are also directed toward inverters that drive the traction motors and supply the auxiliary loads of electrified vehicle in desired manner. The selection of inverter should be done based on the topology, power rating, type of motors, and the packaging methods [71]. Despite of significant topological advancement in multilevel inverters, as of now, the conventional two-level voltage-source PWM inverter is the most popular topology used in almost all the commercial electrified vehicles.

In EPS, two popular configurations are used to interface the ESS with propulsion inverter motor: (i) A high-voltage ESS is directly connected to propulsion inverter motor; (ii) a bidirectional dc/dc converter is placed between low-voltage ESS and propulsion inverter-motor drive [24]. In the first configuration, battery voltage level should match with propulsion inverter dc-link voltage level as shown in Fig. 31.22. This imposes certain constraints over the design and optimization of battery, inverter, and motor [24]. In the second configuration, a bidirectional dc/dc converter is placed between low-voltage ESS and high-voltage dc link of propulsion inverter motor as shown in Fig. 31.23. Inclusion of dc/dc converter increases overall component count but offers several advantages over the first configuration. It boosts voltage level of ESS to match the rated voltage of propulsion inverter dc link. It provides regulated bidirectional power flow between ESS and motor drive, which assists rapid acceleration and recovers energy to charge the battery during deceleration and regenerative braking. It not only offers significant reduction in weight, size, and cost of ESS but also gives space and flexibility in inverter control and motor design [24]. Another most important aspect of the inclusion of dc/dc converter is to recover the energy during regenerative braking that can be further utilized to recharge the battery or storage unit.

Addition of bidirectional dc/dc converter imposes certain disadvantages such as multistage power conversion, increased cost, power losses, integration, and control complexity. It also raises concern about size and cost of power switches and passive components. In addition, the reliability issues due to the integration of additional components must be taken into

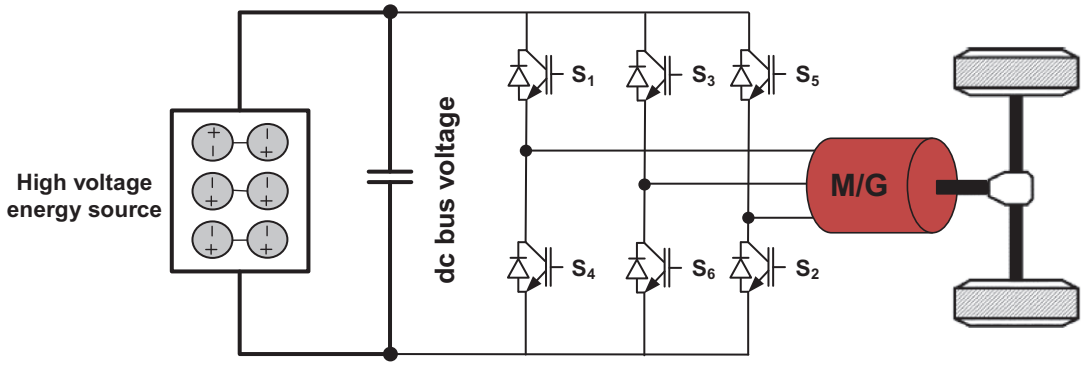


FIG. 31.22 Conventional battery-fed EPS.

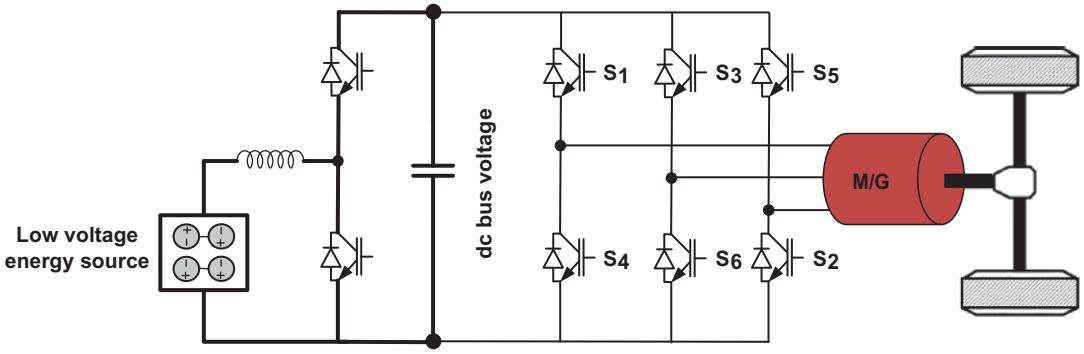


FIG. 31.23 Conventional bidirectional dc/dc converter-fed EPS.

account properly. However, the role of bidirectional dc/dc converter is very significant especially in terms of better utilization of onboard energy sources, power management, dynamic performance, flexibility, system optimization, and reduction of weight and cost [64].

31.4.3.2 PEC Configurations for Electrified Vehicle

PEC integration for EPS that completely replaces ICE-based propulsion system is shown in Fig. 31.24. In conventional configuration of EVs propulsion system, a battery bank is directly connected to propulsion inverter that converts dc voltage into three-phase variable ac voltage. This configuration is applicable to the system where battery bank is sufficiently large to match with the voltage of propulsion inverter-motor drives as discussed in previous section. In the second configuration of BEV propulsion system, a bidirectional dc/dc converter is connected in between battery bank and propulsion motor as shown in Fig. 31.24A. Inclusion of bidirectional dc/

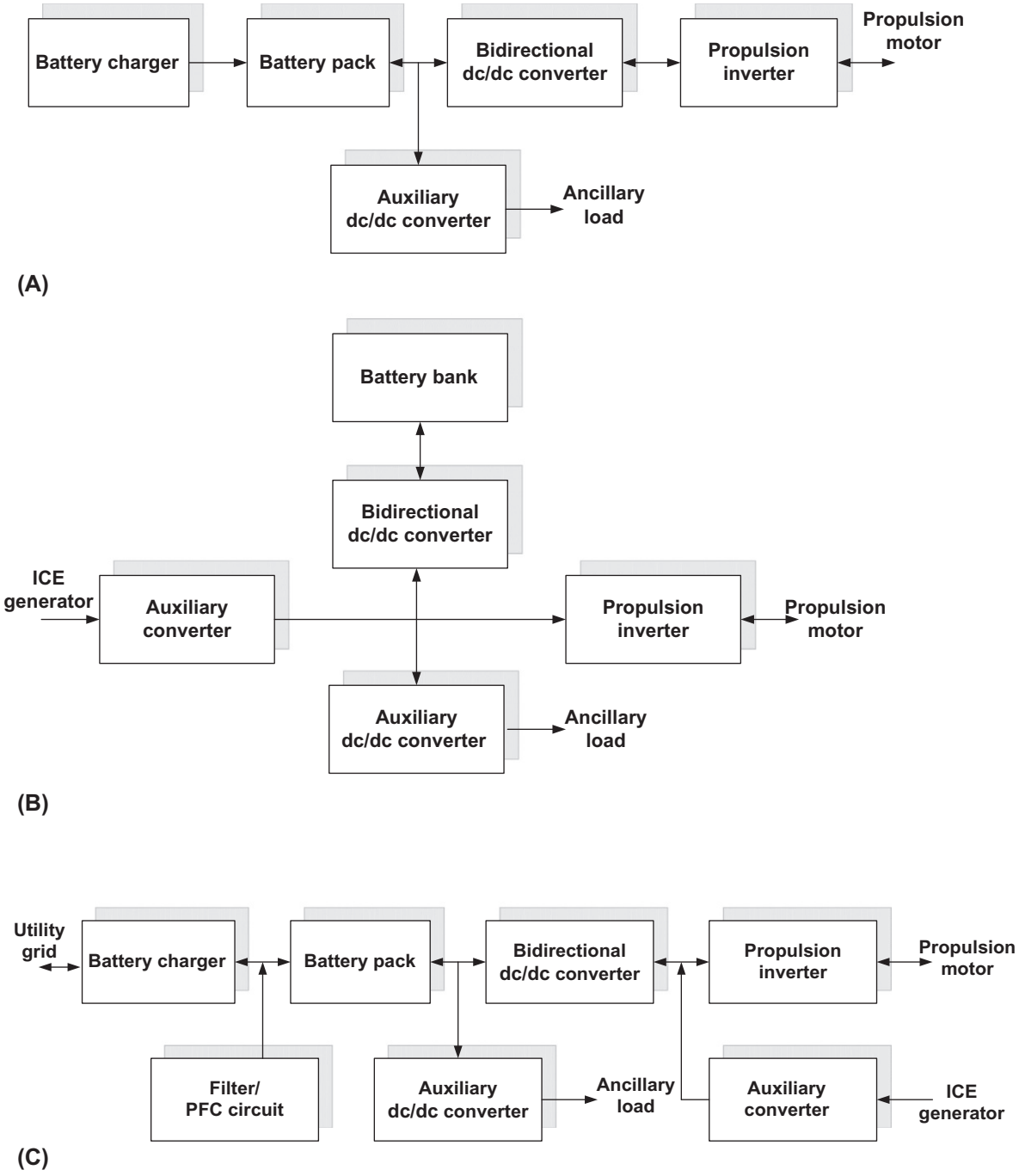


FIG. 31.24 Schematic diagrams of PECs for BEV, HEV, and plug-in HEV. (A) PEC configuration for BEVs, (B) PEC configuration for HEVs, and (C) PEC configuration for PHEVs.

dc converter increases flexibility and control in power flow and management from battery bank to propulsion inverter. It offers better utilization of battery bank and extends life of battery with controlled charging and discharging. It also helps to recover energy during regenerative braking. A battery charger is connected to battery bank to charge the battery from ac outlet. BEVs practically replace the ICE and the various mechanical systems with electric system.

It is well-established fact that the traditional rechargeable batteries are the main source of energy though they are heavy and expensive to replace and hence acting as a bottleneck of the BEV technology. In addition to traditional batteries like lead-acid, nickel-metal hydride (Ni-MH), and nickel-cadmium (Ni-Cd), there are advanced technologies like lithium-polymer (Li-polymer) and lithium-ion (Li-ion) batteries. Despite the popularity of these advanced batteries in portable electronic applications, they fail to keep same reputation for use in BEVs [22]. Consequently, the vehicle manufacturers are cutting down the production of BEV and shifting toward development on HEVs and FCVs.

The PEC for HEVs as shown in Fig. 31.24B consists of an ac/dc converter for converting the alternator ac output voltage into dc voltage for charging the batteries, an inverter for dc/ac conversion to power the propulsion motor, and a bidirectional dc/dc converter for charging the battery and maintaining bidirectional power flow. In addition to this, a low-voltage dc/dc converter is also connected to the battery bank to supply power to low-voltage ancillary loads of the vehicles. Furthermore, an electric air-conditioning unit, pump, and compressor units need an inverter and associated control systems [22].

The PEC configuration of plug-in HEV shown in Fig. 31.24C is similar to HEV with the charger facility to charge the battery bank from utility grid. The high-energy battery bank must be able to store enough electric energy from external charging and from regenerative braking and must be able to supply the stored electric energy to a propulsion inverter-motor system [23]. ac outlet charging should inevitably need a battery charger that is composed of a PFC-integrated ac-dc converter with a proper voltage-current profile for high-energy battery bank. A bidirectional dc-dc converter and charge-discharge profile is also necessary so as to transfer energy between the battery and the propulsion motor system as per requirement [23].

The main task of the fuel-cell propulsion system is converting the fuel-cell stack power output into a usable power for different electric and mechanical loads. Furthermore, the objective is to realize the full potential of the onboard fuel-cell stack by implementing efficient PEC in cost-effective manner. The primary power conversion would be used for three-phase ac output with variable voltage and variable frequency for the propulsion motor of the vehicle [80]. It is important to note that a high-peak-to-average power ratio is generally demanded from the PEC. If there is no ESS, the fuel-cell stack also needs to maintain the above critical power ratio to a maximum that increases size and volume of fuel-cell stack. Secondary power conversion is required for 12 or 42 V auxiliaries and for other loads such as air conditioning, pump, and power steering [80].

The different configuration of fuel-cell-based propulsion system for passenger car is shown in Fig. 31.25. The output voltage of the fuel-cell stack is first conditioned and processed to be compatible with the ESS voltage and propulsion motor using a dc/dc converter. The type of dc/dc converter depends on the voltage level of a fuel cell and ESS. A propulsion inverter is used to convert the dc voltage into modulating ac voltage at variable frequency to drive the propulsion motor under different torque

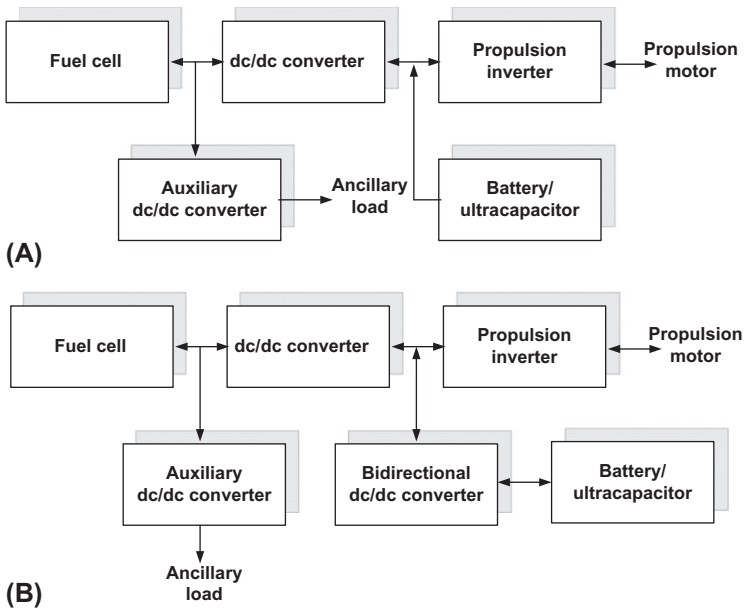


FIG. 31.25 PEC configuration for fuel-cell vehicles. (A) Parallel connected battery/ultracapacitor and (B) interfacing of battery and ultracapacitor through dc/dc converter.

and speed. The electronic controller unit (ECU) sends control signals to regulate the power output of the fuel cell, the dc/dc converter, and the dc/ac inverter based on the feedback signals of speed and torque and driver commands [80].

To begin with fuel-cell vehicle, a simplest configuration of a fuel cell is directly connected to propulsion motor through dc/ac converter. This configuration is applicable to the system only if the fuel-cell stack can produce a voltage level that is suitable for the propulsion inverter motor. However, this configuration is not preferred in general; hence, a unidirectional dc/dc boost converter is connected in between the fuel-cell stack and propulsion inverter as shown in Fig. 31.25A. The purpose of the dc/dc converter is to condition the fuel-cell power and raise the voltage level to match with the dc-link voltage. Typically, dc-link voltage in the range of 300–400 V is favorable for power levels up to about 100 kW [23]. A diode is connected in series with the output of the fuel-cell stack to prevent it from overload, getting short-circuited at output terminal, and to prevent current flowing back into fuel-cell stack [22]. Further, an additional low-voltage dc/dc buck converter is connected to supply the power to ancillary loads. Unlike the ICE-driven alternator, a fuel cell can produce power on board for different ancillary electric loads of vehicles that can eliminate the need of an alternator.

Fig. 31.25B shows the modification to system shown in Fig. 31.25A, with a low-voltage ESS connected through bidirectional dc-dc converter that performs the crucial task of power management and control. Generally, fuel cells are very efficient over particular load range but exhibit poor efficiency under light load condition and poor dynamic response during transient [24]. Therefore, integration of battery and ultracapacitor with a fuel cell makes it sustainable HES onboard for vehicular application. The ESS provides an input power to the propulsion inverter during warm-up time of the fuel cell. Once the fuel cell starts providing the required power, the ESS is disconnected, and the system can completely run on the fuel cell. The ESS system also provides power during transient conditions, to support the fuel cell, which improves the dynamic response and load leveling of overall system [80].

The fuel-cell propulsion system wins over ICE propulsion system on higher fuel conversion efficiency and fuel flexibility, emits practically no toxic pollutants, and reduces CO_2 emission drastically. However, a fuel-cell system designed for vehicular propulsion system should have weight, volume, power density, start-up, and a transient response similar to present-day ICE-based propulsion system [23].

31.4.3.3 PEC Configurations for ESS and HES

ESS whether battery and/or ultracapacitor is employed to reduce the cost and improve the performance of electrified vehicles [18]. The voltage level, *V-I* characteristics, and dynamic response of the ESS are normally different from the primary energy sources (ICE or fuel cell). Thus, a PEC needs to be incorporated to manage and control the power flow in overall vehicle system, which is a key component for achieving better fuel efficiency and dynamic performance [68,69]. For HES, storage element is an essential requirement to act as an energy buffer during transients in the system, to improve the dynamics of the overall system. Also, the storage element compensates the mismatch in power, between the source and load. Therefore, the choice of source combinations, such as battery/ultracapacitor or fuel cell/battery, fuel cell/ultracapacitor, and fuel cell/battery/ultracapacitor, is primarily governed by characteristics of the primary source and operating condition of the load [40,41].

In a fuel cell, the amount of power delivered depends on hydrogen pressure and slow chemical reaction results in poor dynamic response. Therefore, it should be combined with battery or ultracapacitor to achieve sustainable HES [40]. For example, a fuel cell and an ultracapacitor are combined together to constitute a portable HES that can meet different energy and power requirements as necessitated by different driving profiles of vehicle [41]. During acceleration, bulk amount of power has to be released to develop sufficient thrust. This responsibility can be well taken care by ultracapacitor as it can deliver power quickly. Similarly, a fuel cell can support to extend all-electric driving range of the vehicles, by supplying constant power, which in turn enhances durability and life span of the fuel-cell membrane [44].

In HEV, it is desired for the energy system to have high power density and high energy density to cater the sudden changes in the load demand [9]. Moreover, applications that require instantaneous power input and output delivery typically find batteries suffering from frequent charge and discharge cycle, which have an adverse effect on battery life. For such systems, it is crucial to have an additional storage system that is much better and robust in handling surge current. Here, the basic idea of HES is to combine battery and ultracapacitor to achieve a better performance than the latter system. Thus, an ideal source for EVT would be the combination of both the storage sources [18]. Also, the hybridization of battery and ultracapacitor offers much better utilization of energy recovered during regenerative braking.

HES demands suitable PEC to incorporate different energy sources and manages power flow among different sources and vehicle loads [18]. Therefore, investigation on PEC for HES is crucial task in EPS design for achieving optimal balance among efficiency, performance, durability, and reliability of system [63]. In HES, a dc/dc converter is the key constituent that provides compatible interfacing and integration of energy sources [64]. Beside output voltage regulation, a well-designed dc/dc converter can also control and manage power flow through different components. Therefore, selection and design considerations of dc/dc converters are important aspect in ESS. Apart from dc/dc converter, multiple-input dc/dc converter and multiphase interleaved converters are also employed for better energy diversification and utilization of the onboard HES [66,67]. Several topologies for HES configuration for EVT have been proposed in [68–70] to improve fuel efficiency

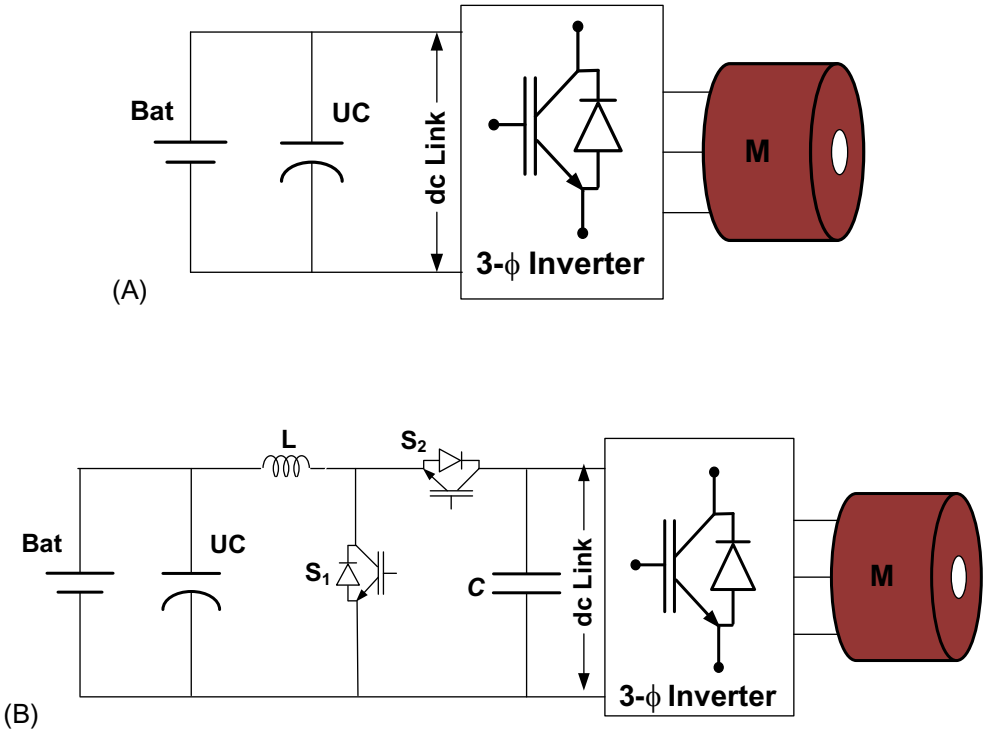


FIG. 31.26 Passive configurations of battery and ultracapacitor parallel with dc/dc converter. (A) Direct interfacing of battery and ultracapacitor and (B) interfacing of battery and ultracapacitor through dc/dc converter.

and dynamic performance that range from simple to complex circuits. On the basis of the use of dc/dc converter, HES can be classified into two categories: passive configuration and active configuration.

Passive configuration

Passive configuration [33] is the simplest method of combining battery and ultracapacitor (UC) bank together as shown in Fig. 31.26A, where battery and ultracapacitor are connected together in parallel without any dc/dc converters. In this method, since the two sources are connected in parallel, battery voltage, ultracapacitor voltage, and dc-link voltage should be maintained at the same level, and ultracapacitor essentially acts as filter. This configuration is easy to implement and eliminates need of expensive PEC and peripheral circuitry. However, major problem with this configuration is inefficient utilization of stored energy in ultracapacitor and battery.

To improve power flow and its proper utilization, a bidirectional dc/dc converter interfaces the parallel-connected ultracapacitor and battery with the dc link as shown in Fig. 31.26B. Despite wide voltage variation across ultracapacitor terminals, the dc-link voltage remains constant due to the regulation of the dc/dc converter. However, in this configuration, the battery voltage is always the same with the ultracapacitor voltage due to the lack of interfacing control between the battery and the ultracapacitor [18]. The battery current must charge the ultracapacitor and provide power to the load side as well.

Active configuration of battery/ultra capacitor

Conventional active methods use one or multiple full-size dc/dc converters to hybridize the battery and ultracapacitor to the dc link. In this case, full size refers to the fact that the dc/dc converter forms the sole path for the flow of energy in the device. The UC/battery configuration as shown in Fig. 31.27A proposed in [31] is the most studied and researched HES. By using a bidirectional dc/dc converter to interface the ultracapacitor, the voltage of ultracapacitor can be used in a wide range. However, the bidirectional converter needs to be of a larger size in order to handle the power of the ultracapacitor. The battery is connected directly to the dc link; as a result, the dc-link voltage cannot be varied. By swapping the positions of the battery and ultracapacitor in the ultracapacitor/battery configuration, we get the battery/ultracapacitor configuration as discussed in [68] and shown in Fig. 31.27B. In this configuration, the voltage of the battery can be maintained lower or higher than the ultracapacitor voltage. The ultracapacitor is connected in parallel with the dc link directly working as a low-pass filter. The control strategy applied to this configuration allows the dc-link voltage to vary within a range such that the ultracapacitor energy can be utilized more efficiently. However, in standard practice to achieve efficient HES, it is preferred that fast-response components are connected with high-power-density system whereas slow response devices are connected to high-energy-density system.

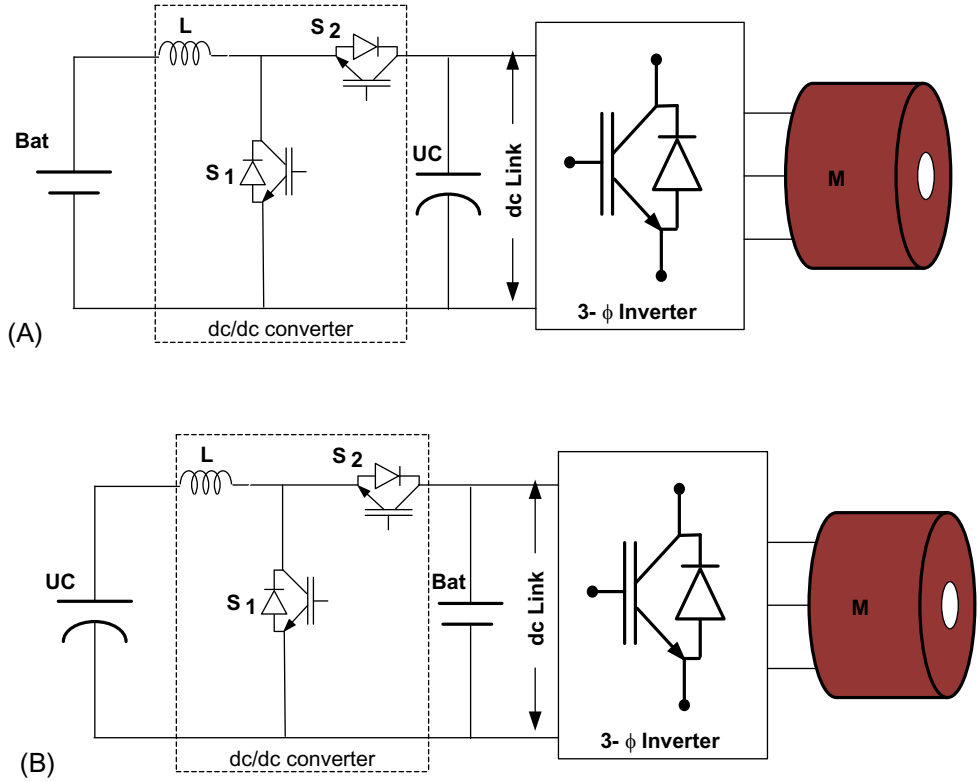


FIG. 31.27 Active configuration of battery and ultracapacitor. (A) Battery is connected through dc/dc converter. (B) Ultracapacitor is connected through dc/dc converter.

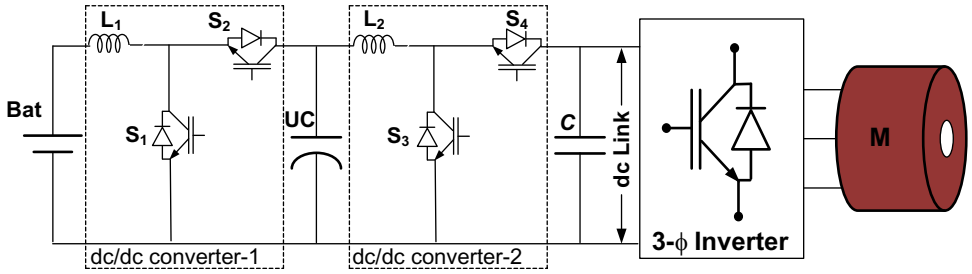


FIG. 31.28 Cascaded configuration of battery and ultracapacitor.

Cascaded configuration

To make a better working range of the ultracapacitor of the battery/ultracapacitor configuration, another bidirectional dc/dc converter is added between the ultracapacitor bank and the dc link, as shown in Fig. 31.28. This forms a cascaded configuration where two dc/dc converters are connected in series. In this configuration, a smaller size battery can be used with lower voltage level, which can be boosted up to a higher voltage level, to reduce the cost. In addition, the battery current can more efficiently be controlled compared with the passive configuration. Due to the existence of the boost converter, the battery current is smoothened, and the stress on the battery is reduced [18]. The battery supplies average power to the load, whereas the ultracapacitor delivers instantaneous power charge and gets charged quickly by recovering energy during regeneration. The drawback of this topology is that the battery can be charged neither by braking energy nor by the ultracapacitor due to the unidirectional boost converter [18]. However, the possibility of battery charging can be explored by replacing unidirectional dc/dc converter with a bidirectional dc/dc converter.

Parallel configuration

Instead of cascaded connection of the two converters, parallel configurations of battery/ultracapacitor are also used as shown in Fig. 31.29 proposed in [66]. The battery bank and the ultracapacitor are connected to the dc link in parallel through bidirectional dc/dc converter. In this configuration, both the battery and the ultracapacitor present a lower voltage level than the dc-link voltage. The voltage of the ultracapacitor can vary in a wide range so that capacitor is fully used. The voltages of the

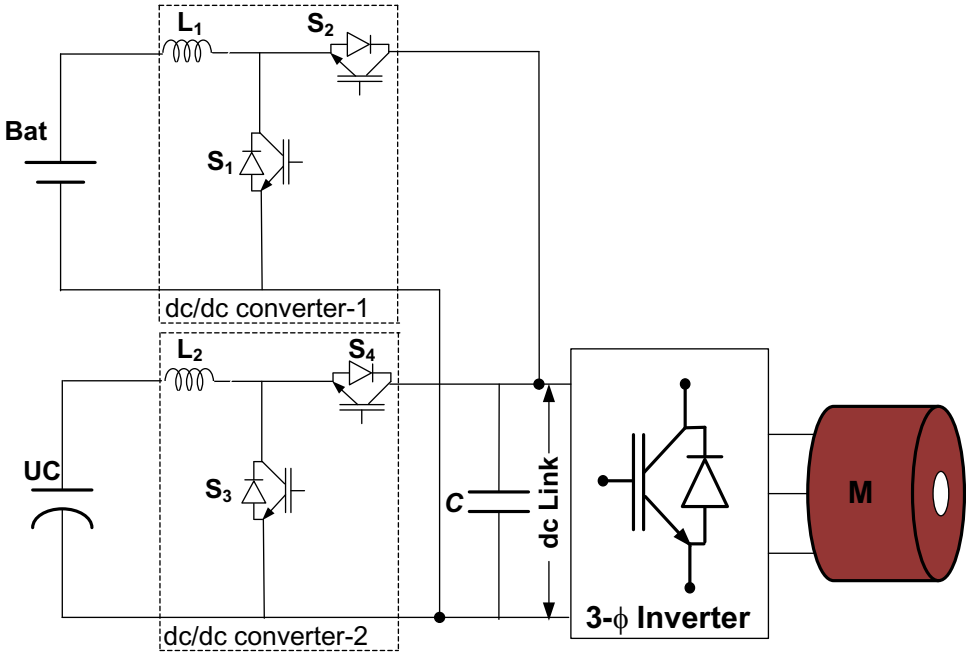


FIG. 31.29 Parallel configuration of battery and ultracapacitor.

battery and the ultracapacitor will be boosted up when the propulsion system demands power and bucked down under recharging conditions. Power-flow directions in/out of the battery and the ultracapacitor can separately be controlled, allowing flexibility for power management [18]. However, if two full-sized dc/dc converters are integrated in parallel, the cost, size, and complexity of control increase.

Multiple input configuration

As discussed in previous section, multiple-converter configuration is expensive because it requires two full-size bidirectional converters to interface both battery and ultracapacitor. Therefore, multiple-input converter (MIC) topologies [81–84] are proposed in order to reduce the cost of the overall system. The configurations of the MIC are shown in Figs. 31.30 and 31.31. MIC is a converter that can combine different energy sources with a single stage of power conversion. It offers simplicity, flexibility, and compact design and reduces the cost and control complexity of the system [82–84]. In the multiple-input bidirectional converter shown in Fig. 31.30, both the battery and the ultracapacitor are connected to one common inductor by parallel switches [81]. Each switch is paired with a diode, which is designed to avoid short circuit between the battery and the ultracapacitor. In parallel-connected switch, the higher-voltage-source cell will be dominating, which needs time multiplexing switching. The second approach is to form a pulsating voltage-source cell (PVSC) of the sources and connect these PVSC in series as shown in Fig. 31.31 and proposed in [82]. In series configuration of MIC, voltage magnitude of battery and ultracapacitor can be asymmetrical, and each of the sources can deliver power individually and simultaneously. Both input voltages are less than the dc-link voltage; thus, the

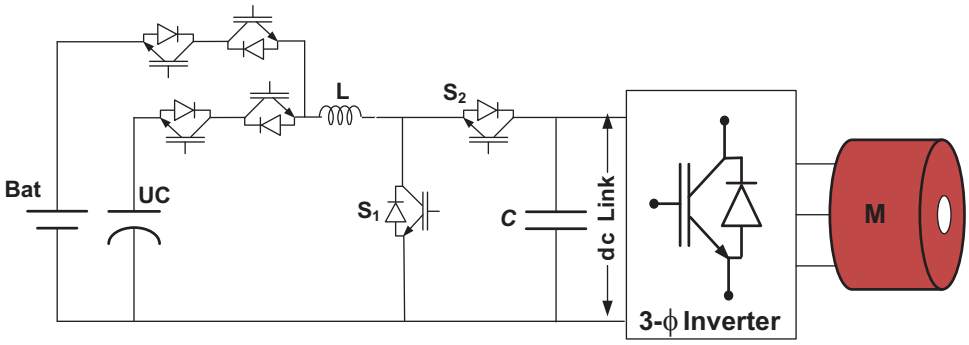


FIG. 31.30 Parallel configuration of multiple-input converters.

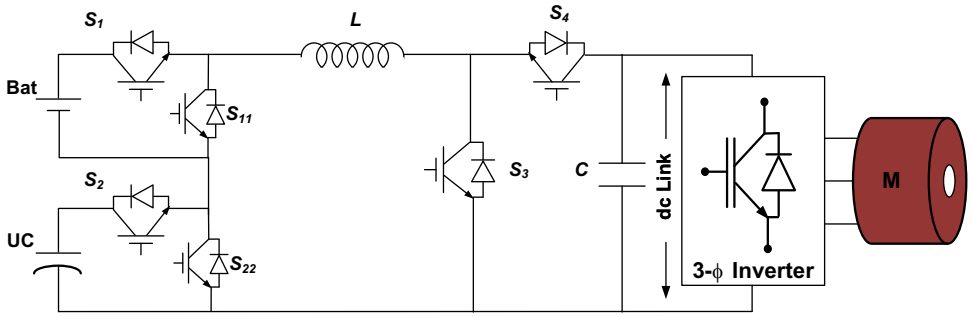


FIG. 31.31 Series configuration of multiple-input converter.

converter works in boost mode when input sources supply energy to drive load and in buck mode for recovering regenerative braking energy to recharge the battery and the ultracapacitor [81]. Only one inductor is needed, even if more inputs are added into the system. However, the controlling strategy and power-flow management of the system are relatively complex.

As discussed in parallel configuration, in HES, each energy source is connected together through separate single-input dc/dc converter (SIC), and their outputs are connected in parallel to a common dc bus as shown in Fig. 31.32. In conventional configuration paralleling, the whole system including energy sources offers good solution to obtain high degree of availability [76,83,84]. However, such configurations are costly, bulky, and relatively complex in design and reduce overall efficiency and flexibility and increase control complexity of the system. If costs and availability are being considered, then the single-input converters can be successfully replaced by a single multiple-input converter as shown in Fig. 31.33.

The conventional structure of interfacing multiple energy sources in multiple power stages can be successfully replaced by a single MIC that integrates multiple energy sources with a single stage of power conversion. In this structure, the system voltage is regulated, and the power flow among the energy sources, storage devices, and load can be controlled optimally and centrally. It eliminates the need for redundant power stages of the conventional structure and thus achieves reduced parts count [83]. MICs have advantages of easy power management, efficient thermal management, better utilization of available input sources, and centralized control compared with a conventional structure. The overall system efficiency is increased due to the reduction of the conversion stages, redundant passive elements, power switches, and hence their associated losses. The disadvantage of the MIC configuration is that the output stage of a MIC can act as a single point of failure. However, a MIC with modular component can compensate for this drawback by reducing the mean downtime (MDT) of the system [67].

In HEV, as shown in Fig. 31.34, where the combination of battery and ultracapacitor is preferred, battery supplies constant power, whereas additional power demand by the load during start-up and acceleration is delivered by the ultracapacitor while maintaining dc-link voltage constant. The amount of power drawn from the battery relies on the state of charge (SOC) of the battery; thus, for change in power drawn from the battery, power delivered by the ultracapacitors should also be changed.

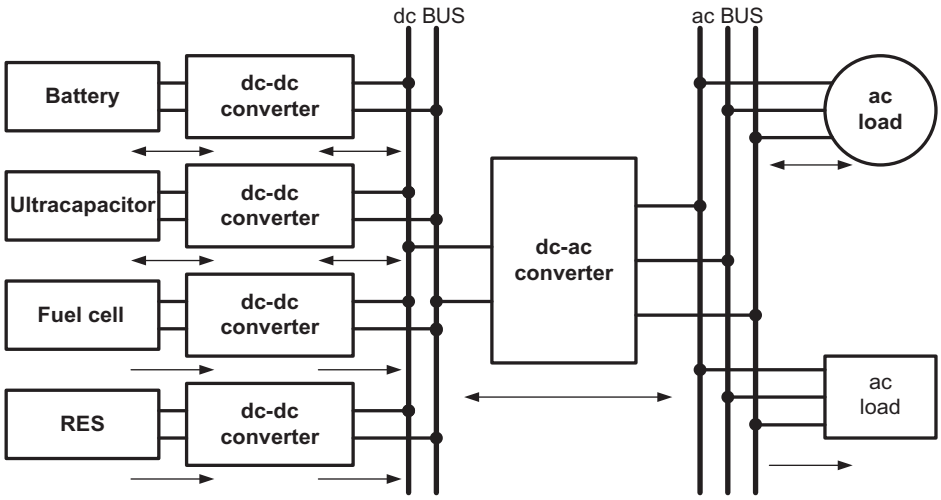


FIG. 31.32 Conventional hybrid energy system configuration with single-input dc/dc converter [83].

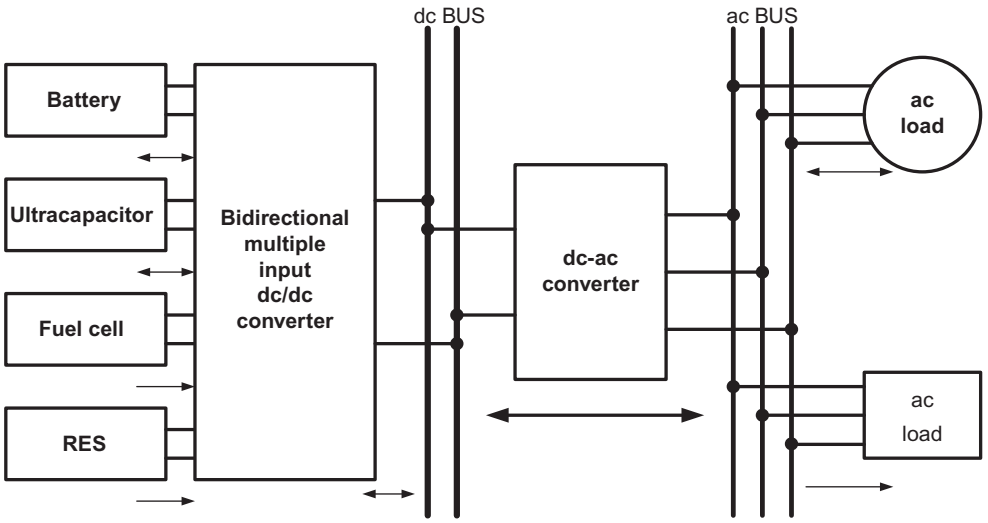


FIG. 31.33 Hybrid energy system configuration based on multiple-input dc/dc converter [83].

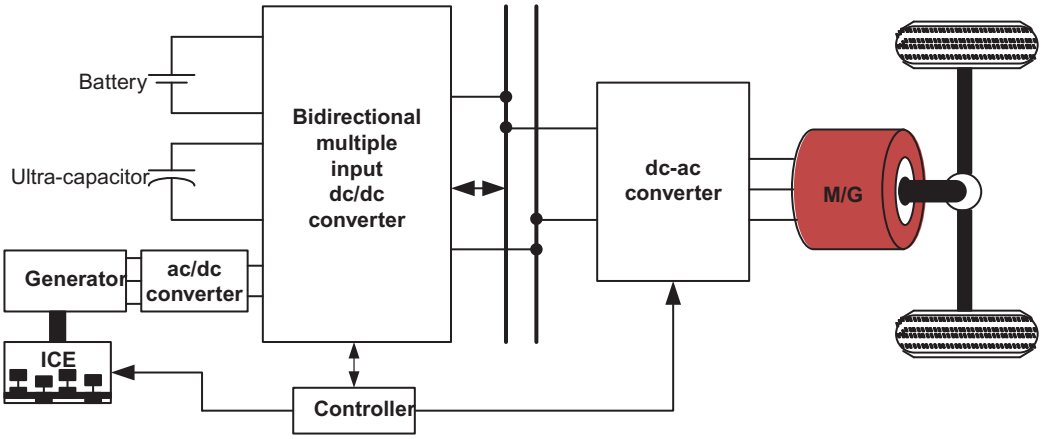


FIG. 31.34 Multiple-input converter-based hybrid electric vehicle.

Thus, effective power sharing can be achieved by MICs depending on the control strategies and operating mode. This modulation of power between battery and ultracapacitor is not possible in conventional structure because both the sources have to supply constant power to regulate the output dc-link voltage.

MIC structure has an explicit advantage over the conventional structure in terms of total component count and conversion stages used due to mutual sharing of system components. As a result, compact design and improved system efficiency can be achieved. Comparison of these two structures given in Table 31.10 shows that the MIC structure is promising alternatives in vehicular application to interface multiple sources on board.

TABLE 31.10 Comparison of SIC and MIC structure [83]

Characteristics	SIC structure	MIC structure
Common dc bus	Yes	No
Conversion step	Multiple	Single
Control scheme	Individual control	Centralized control
Power-flow management	Complicated and slow	Simple and fast
Transformer (isolated)	Multiple	Single multiwinding
Implementation effort	High	Low
Component count	High	Low
Flexibility	Low	High
Cost and volume	High	Low

31.4.3.4 PEC Configurations for Battery Charger

PEC configuration for battery chargers plays a critical role in the sustainable development of BEVs/PHEVs. The challenge of transforming BEVs/PHEVs from concept to reality is to make it safe, convenient, and affordable for consumers to charge batteries [63]. In order to improve convenience and increase charging efficiency, a number of charging schemes have been proposed as house charging, solar charging station, park and charge (PAC), move and charge (MAC), and regenerative

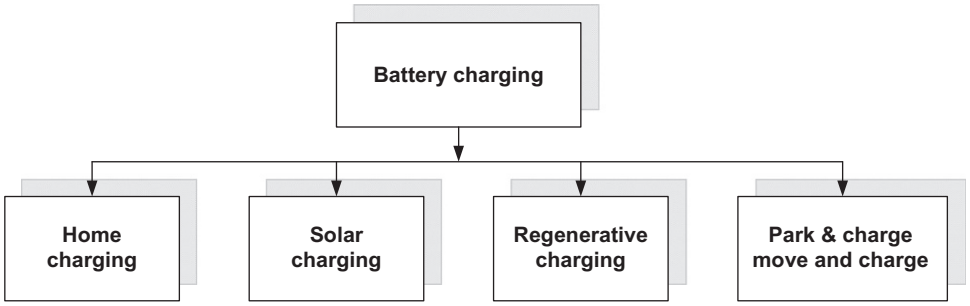


FIG. 31.35 Multiple options for charging of BEVs/PHEVs.

charging as shown in Fig. 31.35. A battery charger composed of several PECs should be reliable and efficient with high power delivery capacity at low cost and weight. Its operation depends on power electronics component, switching strategies, and control algorithms. A BEV/PHEV charger must ensure the operation at unity power factor or close to unity power factor to draw maximum amount of real power from utility grid with less distortion in current to minimize the power quality impact on grid. The battery charger should be designed according to IEEE-1547, SAE-J2894, and similar standards such that the amount of harmonic and dc current injected into the utility grid must be controlled within the preset limit.

A variety of PEC configurations and control methods have been developed as BEVs/PHEVs battery chargers, which includes single-stage and multistage power conversion. Single-stage conversion (ac/dc) configuration suffers with large low-frequency ripple in the output current, and hence, its application is limited to lead-acid batteries only. Conversely, multistage conversion configuration (ac-dc and dc-dc) inherently offers low-voltage ripple and relatively high power rating and hence is suitably adopted for lithium-ion and Ni-MH batteries, which are being used in PHEVs [43]. A simplified universal two-stage battery charger for BEVs/PHEVs is shown in Fig. 31.36. The input voltage is first filtered out and fed to the PFC integrated ac/dc converter. The rectified voltage is fed to a regulated intermediate dc-link bus. The dc/dc converter then converts dc-link voltage to a regulated output voltage for battery charging. The galvanic isolation is achieved at dc/dc conversion stage by using isolated dc/dc converter.

The availability of infrastructure for charging facility will help to reduce the size and capacity of onboard ESS, and consequently, cost and size will be reduced. Charging stations are classified as three types, on the basis of power-handling capacity, charging time, and location of charger installation. Type-I charging is the slowest method of charging, designed for home or business sites with readily available power outlet, and no additional infrastructure is required. It uses standard 120/230 V, 15 A single-phase charger outlet with standard J1772 connector [85]. In type-II charging, dedicated infrastructure and charging equipments are required, which be installed either on board or off-board to avoid redundancy in PEC. It charges battery with 240 V, 80 A single-phase or three-phase and offers fast charging compared with type-I charging. The BEVs/PHEVs owners are likely to prefer type-II charging technology due to its faster charging time and standardized vehicle-to-charger connection. Type-III charging is a commercialized fast charging method and offers the possibility of charging in less than 1.0 h. It can be installed in highway and city refueling points, analogous to conventional fuel stations. It typically operates with 480 V and requires an off-board charger to provide regulated power conversion. The SAE J1772 standard prescribes that type-I and type-II charging infrastructures should be installed on board, whereas type-III chargers should be mounted off-board. It is expected to use type-I and type-II charging stations to enable fast charging in public and private places with less impact on utility [86]. However, type-III charging can increase peak demand and has the potential to quickly overload local distribution system and equipment at peak

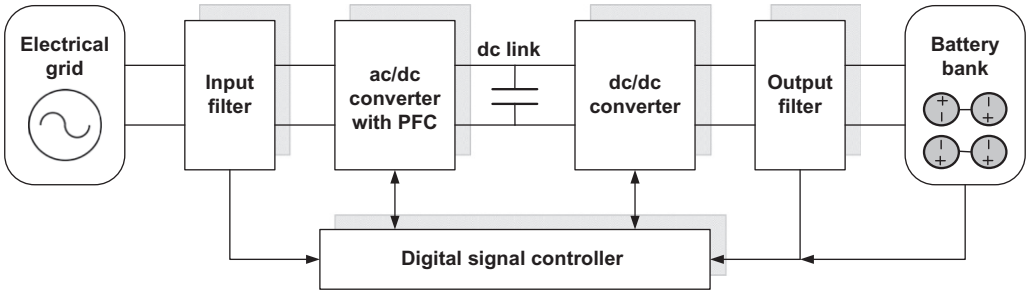


FIG. 31.36 Simplified diagram of universal battery charger.

TABLE 31.11 Charging types and power level [72]

Charging type	Charger location	Charger interface	Power rating (kW)	Charging time (h)	Vehicle technology
Type-I	Onboard	Home outlet	1.4 (12 A)	4–11	BEV (5–15 kWh)
	One-phase		1.9 (20 A)	11–36	PHEV (16–50 kWh)
Type-II	Onboard	Dedicated public or private outlet	8 (32 A)	1–4	BEV (5–15 kWh)
	One-phase		19.2 (80 A)	2–6	PHEV (16–30 kWh)
Type-III	Off-board	Dedicated commercial outlet	50	0.4–1	BEV (20–50 kWh)
	Three-phase		100	0.2–0.5	

times. The charging characteristics and infrastructure aspects for different type of charging methods are presented in [72] and are given in Table 31.11.

Battery chargers for BEVs/PHEVs can be classified as follows:

I. On-board and off-board charger
II. Unidirectional and bidirectional charger
III. Integrated charger
IV. Inductive charger

On-board and off-board charger

The onboard charger should be installed in the vehicle and designed for the slow charging rate, that is, it takes longer time to charge relatively. Due to limitation in available space in vehicle and payload, the onboard charger for BEVs/PHEVs should be light and compact in design. The advantage of onboard charger is that the battery can be charged at anyplace where there is electric outlet is available. An off-board battery charger is less constrained by size and weight and keeps redundancy in power electronic converters, which adds flexibility in the system. The onboard and off-board charger are usually implemented either with unidirectional or bidirectional power flow. Initially, the unidirectional charging should be the first step because it reduces power electronic component requirement, simplifies interconnection issues and control complexity, and reduces battery degradation [85]. These chargers typically use a diode bridge rectifier in conjunction with a power factor correction (PFC) and dc-dc converters [85].

Unidirectional and bidirectional charger

The classification of conventional unidirectional and bidirectional charger topology is shown in Fig. 31.37. The classification is made on the basis of operation of particular PEC topologies. A unidirectional PEC topology for a type-I battery charging system [87] is shown in Fig. 31.38. Simple control and operation of unidirectional chargers make it relatively unproblematic for a utility grid to manage heavily loaded distribution network to charge multiple BEVs at a time [88]. Battery charger with active front-end converter can control the supply current phase angle to deliver reactive power without discharging the battery. In unidirectional charging, it needs to optimize charging strategy to maximize the benefits and to minimize the impact on distribution system [87,88]. For high penetration of BEVs/PHEVs and active control of charging current, unidirectional chargers can meet practically all the objectives of the utility grid.

The conventional boost converter topology with PFC as battery charger is shown in Fig. 31.39 that is very popular configuration for unidirectional battery charging. A dedicated diode bridge rectifier is used to rectify the ac input voltage to dc that is further converted to dc followed by boost section. In this topology, the output ripple current, which is a difference between diode current and dc output current, is very high [89]. To

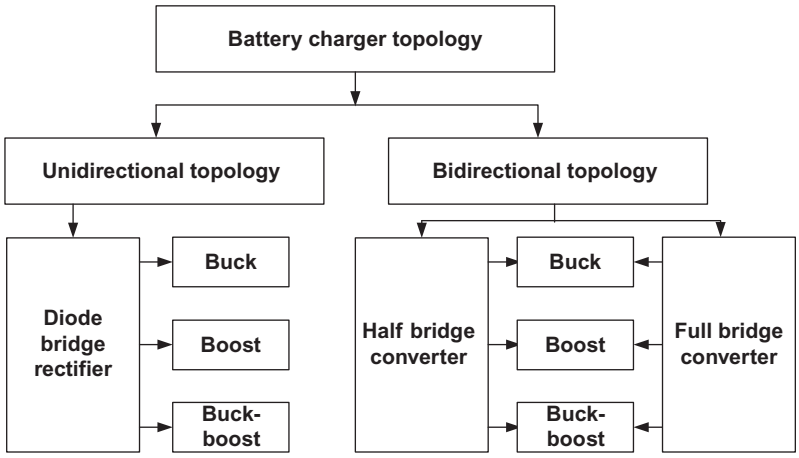


FIG. 31.37 Classification of conventional battery charger topology.

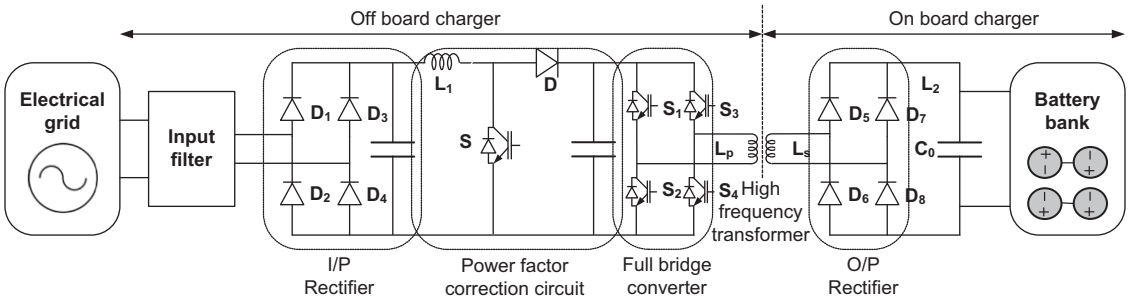


FIG. 31.38 Battery charger configuration for unidirectional power flow.

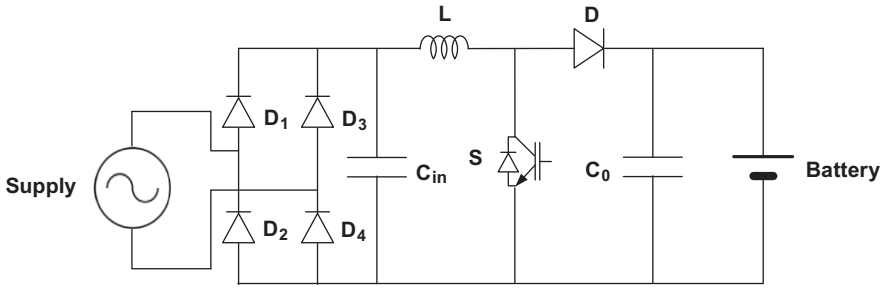


FIG. 31.39 Conventional single-switch PFC boost converter for battery charging.

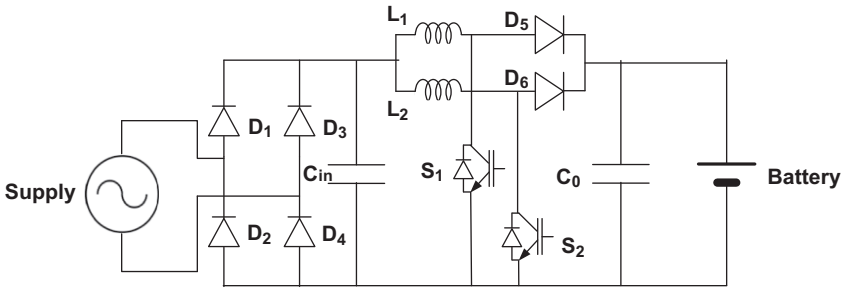


FIG. 31.40 Interleaved dc/dc boost converter for battery charging.

reduce the current ripple, the interleaved boost converter is presented as shown in Fig. 31.40. It consists of two boost converters in parallel operating 180 degrees out of phase [88,90]. The input current is the sum of the two input inductor currents that are out of phase and consequently cancel out each other, reducing the current ripple and stress across dc-link capacitor. The advantages of interleaved boost converter are parallel-connected switches that increase flexibility, switching out of 180 phase which increases the effective switch frequency and causes the reduction in filter size with lesser ripple content.

A bidirectional charging system supports grid-to-vehicle (G2V) and vehicle-to-grid (V2G) operation by injecting power to the grid and power stabilization with adequate power conversion [73,91,92]. A conventional bidirectional charger process supplies power in two stages. In the first stage, an active grid connected bidirectional ac/dc converter integrated with EMI filter and PFC is connected that enforces power factor to be close to unity. In the second stage a dc/dc converter is connected to regulate charging voltage and current [72]. In charging mode, charger should draw sinusoidal current with defined phase angle to control active and reactive power. In discharging mode, the charger should feed back power to the grid with sinusoidal current [91]. In ac/dc and dc/dc conversion, isolated and nonisolated converter topologies are used. An isolated bidirectional dual active bridge battery charger system is shown in Fig. 31.41 that offers high power density and fast control; however, the large number of component's count can add to cost [25].

The development of charger infrastructure with bidirectional power flow is growing rapidly; however, it imposes some serious challenges and issues such as reduction in battery life due to frequent charging and discharging, increased cost of charger, upgradation of existing distributed network, metering, and pricing [92]. Successful implementation of battery charger with bidirectional power flow needs to solve the abovementioned

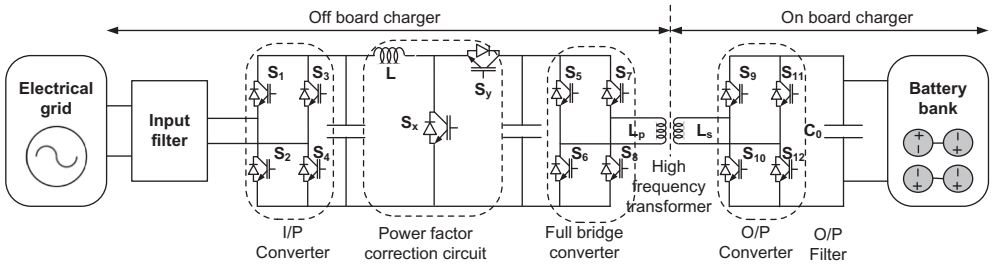


FIG. 31.41 Battery charger for EV/PHEV with bidirectional power flow.

issues. Also, it requires extensive safety measures and anti-islanding protection [92]. A unidirectional charger can be used for types I, II, and III charging; however, bidirectional chargers that are expected only for type-II charging system due to output power limit and cost target that are low and relatively high degree of freedom and flexibility in operation.

Integrated charger

At present, the onboard chargers face constraints on weight, volume cost, and space over specific power capacity of the battery. To overcome the abovementioned problems, charger configuration with integrated propulsion inverter-motor drive has been proposed [93,94]. The concept of integrated charger is feasible only if the vehicle is at rest. In an integrated charger, the propulsion inverter serves as a bidirectional ac/dc converter, and motor windings are used as filter inductors. Low cost, high-power-density bidirectional power flow, and fast charging with unity power factor are the advantages of the system. However, extra component requirement and control complexity are some of the challenges in its successful implementation. The schematic of a typical single-motor- and single-converter-based integrated charger system is shown in Fig. 31.42.

The classification of integrated charger topologies is done on the basis of the number of total converter and motor used such as one motor with a converter topology, one-motor and two-converter topology, and two-motor and two-converter topology [93–97]. A two-motor and two-converter integrated charger system is shown in Fig. 31.43 as discussed in [95]. In this system, main converter is used to drive the main motor, and auxiliary converter is used to drive the auxiliary motor during propulsion. During charging, two converters operated as ac/dc converter, and three-phase windings of the two motors act as filter inductor with neutral point connected to the grid [95,96]. The main converter recovers energy from main motor during regenerative braking for battery charging while maintaining the driving force for propulsion. The auxiliary converter coupled with auxiliary motor serves the purpose of starting of ICE and battery charging. This configuration of integrated charger is more popular for PHEVs. The inherent disadvantages of this integrated charger are the large number of extra components (twelve power switches, three contactors, and two motors) and control complexity.

A dual-inverter, single-motor integrated charger topology is shown in Fig. 31.44, where one motor with a double set of stator windings comprises two motor halves [97]. The working principle of this configuration is similar to two-motor and two-inverter configuration. However, in this configuration, elimination of one motor leads to reduction in cost and weight but still requires three contactors, 12 power switches, and a specially designed dual winding motor.

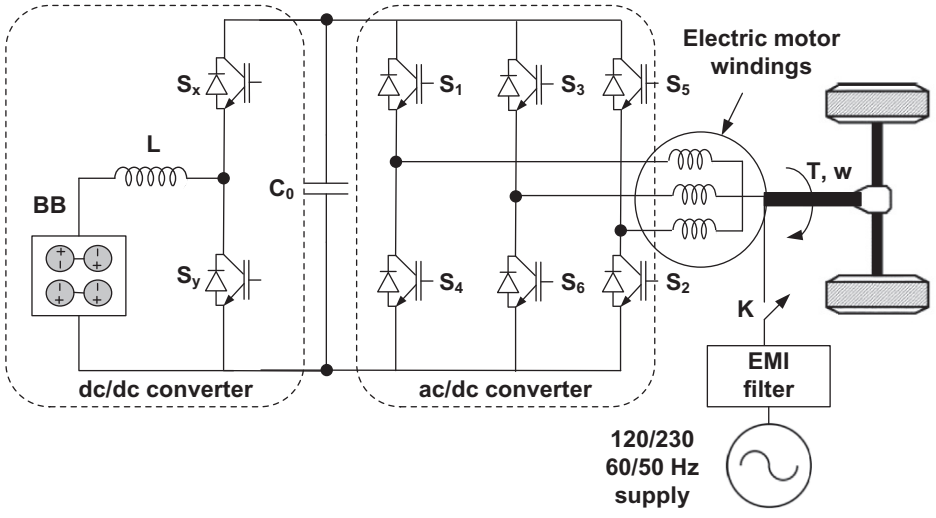


FIG. 31.42 Typical structure of integrated BEV charger.

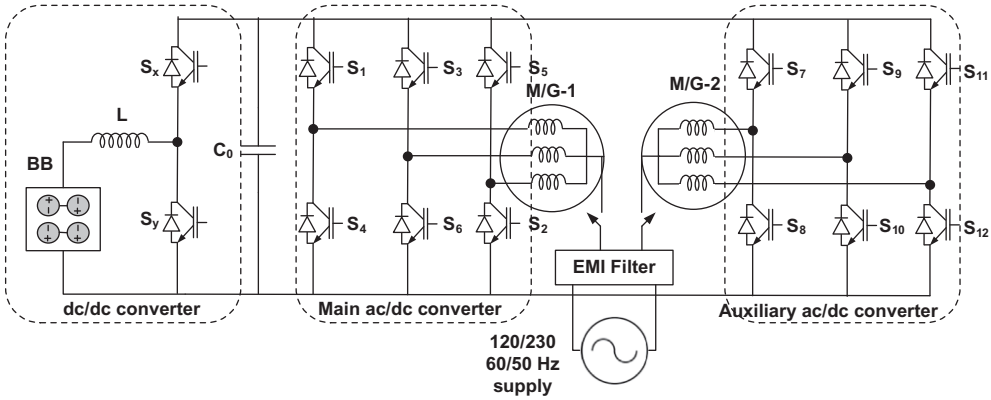


FIG. 31.43 Dual-motor dual-inverter integrated charger configuration.

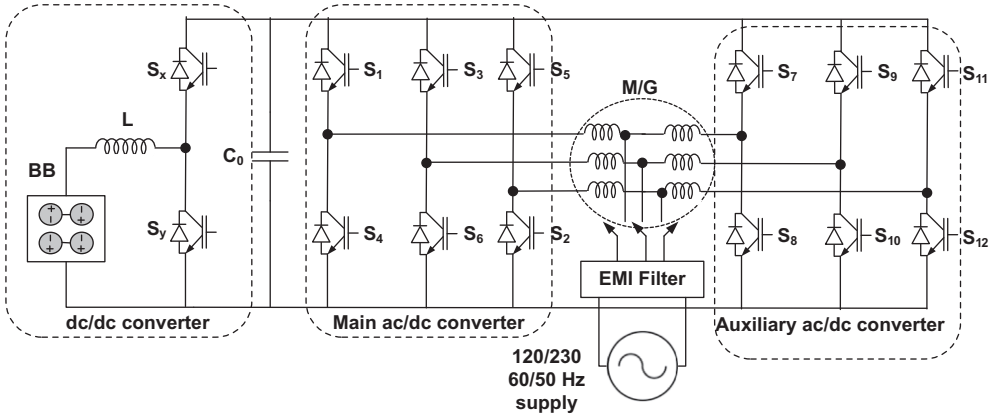


FIG. 31.44 Dual-inverter single-motor integrated charger configuration.

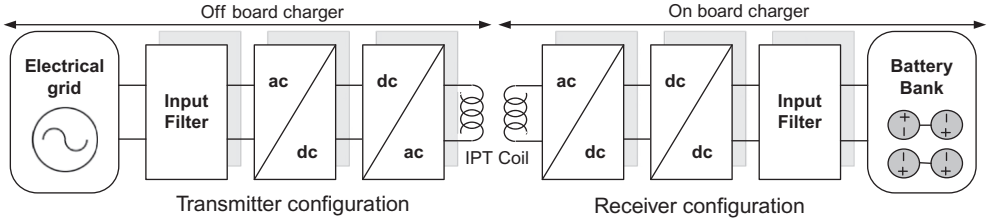


FIG. 31.45 Contactless, inductive, and wireless charging System.

Inductive charging

In conductive charging systems, battery bank is directly connected to the power outlet through charger connecting cable [98]. The standard charging port like domestic power outlets (type I and type II) or commercialized charging station (type II and type III) can be used for battery charging. However, in conductive charging, vehicles need to be parked and plugged into charging outlet.

As an alternative, inductive power charging concept has been introduced and mostly known as inductive power transfer (IPT). In IPT, the energy from power outlet is transferred to the onboard battery magnetically. The basic scheme of the IPT is illustrated in Fig. 31.45. The working principle of IPT is based on the magnetic coupling between two coils of a very-high-frequency transformer. The first coil of the transformer is mounted on the charger side, and the second coil is installed on the vehicle. Single-phase or three-phase ac supply of frequency 50–60 Hz is first rectified to dc, and then, this rectified dc is inverted to very-high-frequency ac within the charging station. This high-frequency power is transferred to the onboard battery through magnetically coupled primary and secondary coil. This high-frequency ac power received through vehicle side coil is converted to dc to charge the battery on board. The clear advantages of IPT are elimination of charger connectors, user convenience, and galvanic isolation. Also, it is possible to build charging strips on road, which enables

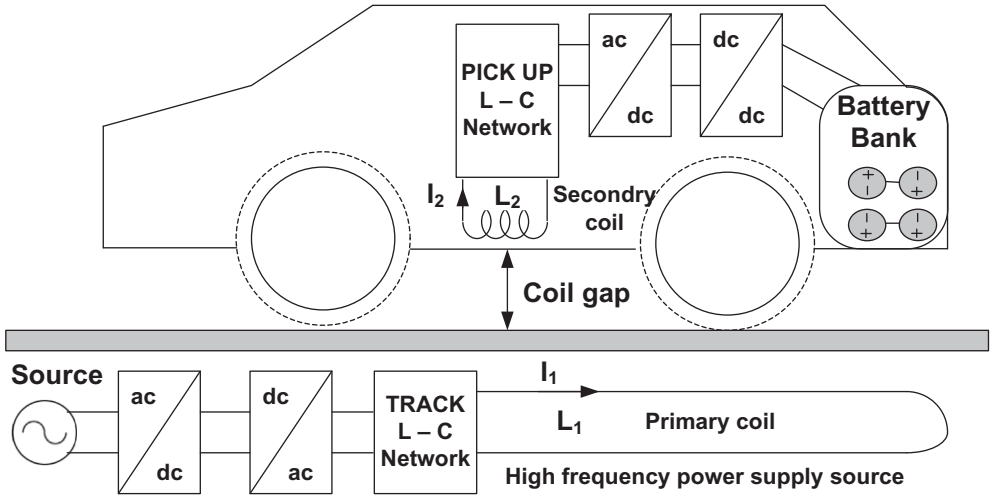


FIG. 31.46 Inductive coupling road bed BEV battery charger.

charging while driving as shown in Fig. 31.46. Relatively low power density and reduced efficiency, high control complexity, and manufacturing cost are some of the major disadvantages of this method [99–101].

31.5 Electronic Control Unit

The electronic control units (ECU) are designed to provide supervisory control of electric vehicular system [102]. It is a combination of dedicated system control software and electronic circuitry that includes interfacing hardware, sensing circuitry, driver and isolator circuitry, and communication buses. Basically, ECU is the integration of sophisticated electronic circuitry; dedicated digital controllers like microprocessors, microcontrollers, digital signal processors (DSP), and/or field programming gate array (FPGA); and modeling and simulation tools with autocode generation systems like MATLAB/Simulink, ADVISOR, PSAT, PSIM, SABER, SIMPLORER, and VTB, along with embedded software [26,102,103].

ECU provides the flexible multi-input/multi-output channels for communication among various components of the vehicular system. The controller synchronizes or coordinates with the components of EPS such as ESSS, PEC, electric motors along with ICE, transmission system, pilot commands, and operating modes of the vehicle. The ECU controls and maps the status of electric motor, ICE, and vehicle behavior based on a selection of system inputs. Standard pilot commands, such as braking and acceleration, are supplied as system input to the ECU from appropriate sensors and CAN buses. Based on system input and CAN bus information, certain mappings of different system components are performed to monitor their current status to select the vehicle's mode of operation [104,105]. The entire information is processed in digital controllers through programming, which performs the required calculation and converted into desired power and/or torque and/or speed commands for each wheel individually or simultaneously. The output of ECU that is driving signals for various components of the vehicle is communicated through CAN transmitter over different sections of vehicles. Not only the ECU is able to implement a variety of advanced vehicle control and dynamic algorithms, but also it monitors overall vehicle behaviors and observes the performance. The ECU is placed near to motor drives and engine; therefore, it should be designed such that it can bear temperature ranging from 80°C to 140°C and extreme vibrations that are a major challenge. A self-explanatory architecture of the ECU is shown in Fig. 31.47.

31.6 Power Management and Control Algorithm

In EVT, the control and management of power flow from multiple energy sources to power electronic converters and from converters to different vehicle loads is a major challenge. The technological advancement transforms the early ON/OFF control system to modern adaptive predictive control era that improves the overall performance of control system [106,107]. Dedicated efforts are being given for the development of appropriate control and energy management strategy that is very essential, specifically in HEV operation.

A control strategy is defined as an algorithm, which is a set of instructions or laws regulating the overall operation and power flow of the vehicular system. The algorithm can be considered as a black box that performs desired calculation on the basis of given information. Input information mainly contains measured data of vehicle's operating condition such as acceleration, braking, torque demand, traffic information, and driving profile. The output of the algorithms is a decision that commands

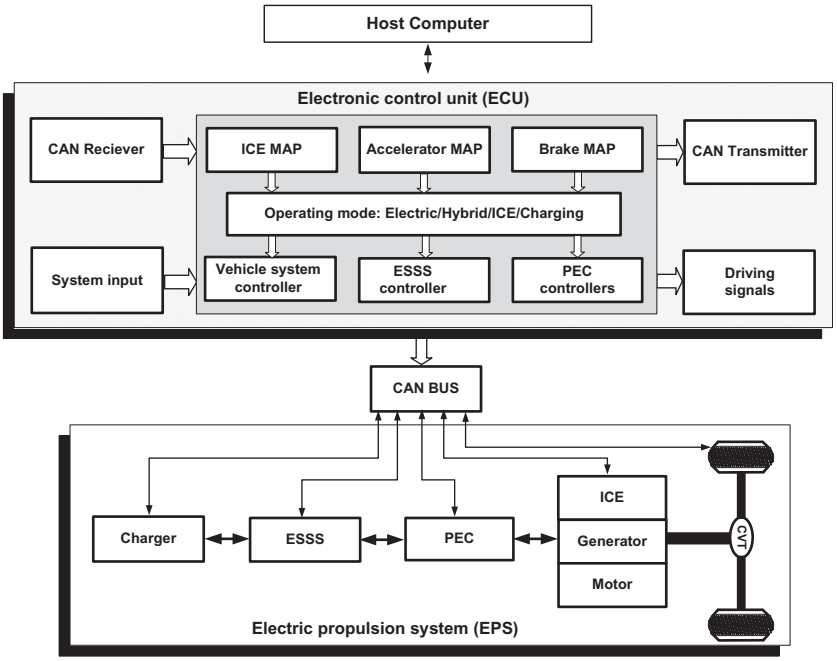


FIG. 31.47 Architecture of electronic controller in electrified vehicles [104].

the driver circuits to turn ON or OFF the vehicle's components or to modify their operating region toward optimization [106]. A properly developed control algorithm and management strategy should satisfy certain objectives such as vehicle power demand, monitoring of battery's state of charge, fuel economy, reduced emission, efficiency optimization, and smooth coordination between electric and mechanical components. Therefore, it becomes prime concern to adopt systematic process for power-flow control and optimization while designing the controllers and control algorithms.

Controllers are mainly classified into two groups based on their mathematical modeling strategy: (1) rule-based systems and (2) optimization-based systems [107]. The detailed classification of both the controllers is given in Fig. 31.48. Basically, rule-based controllers are designed to obtain maximum fuel economy and efficiency and reduced emission for predefined

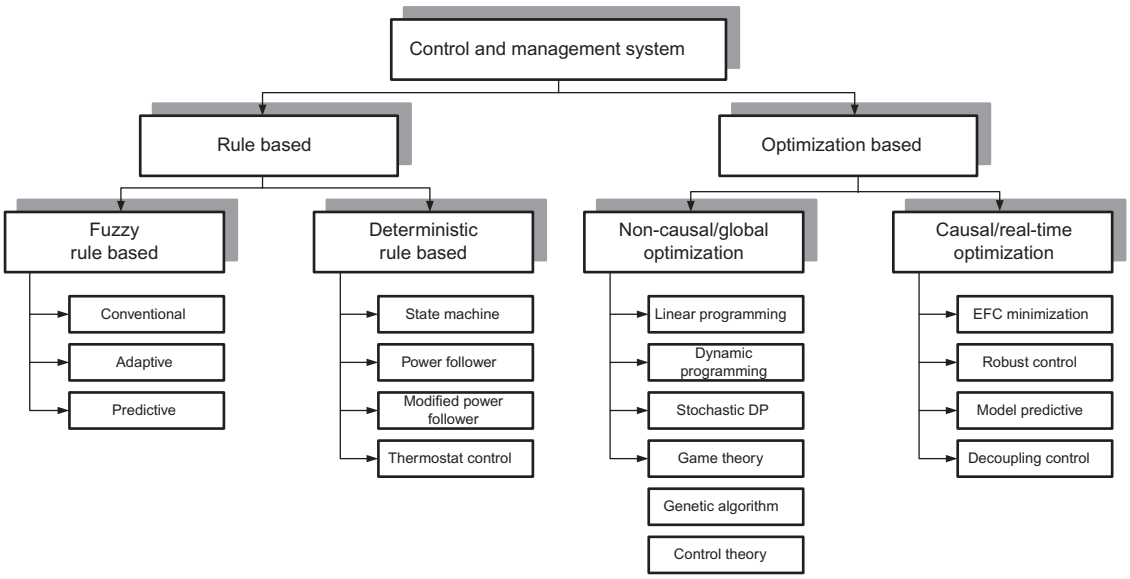


FIG. 31.48 Classification of control algorithms and power management techniques for EPS [107].

TABLE 31.12 Comparison between rule-based and optimization-based controllers

	Rule-based	Optimization-based
Implementation	Simple	Complex
Speed	Fast	Slow
Sensitivity	Low	High
Optimality	Approximate	Exact
Information needed	Less	More

driving profiles. Rule-based controllers are tuned based on sets of rules or criteria written on the basis of vehicle information. In this controller, state diagram and flow charts are commonly used for performance optimization of each component individually rather than cumulative. On the other hand, optimization-based controllers are designed to develop optimal control strategy for propulsion system by reducing the cost function. The cost function is derived based on the past and future information of driving profile, component parameters, and expected performance of the vehicles.

This controller is tuned for overall vehicular system optimization rather than component level. Both the controllers have their own pros and cons that are summarized in Table 31.12 and need to be addressed properly before implementing the algorithms. The global control strategy with real-time optimization has been the best proposed solution for HEV/PHEV so far [106].

31.7 Summary

Contemporary and futuristic global scenario of environmental, economical, and technological factors has accelerated the interest toward partial and/or complete electrification of vehicular technology. In this chapter, topological configuration of different vehicles has been presented with emphasis on EPS and its components to understand the fundamentals of EVT. The comprehensive review of the electrified vehicle architecture and EPS shows that EVT is a promising technology for sustainable future transportation system. At present, HEVs are dominating vehicle configurations, emerging rapidly and capturing the significant market space at very fast growth rate. Suitable energy policy and infrastructures for charging station will accelerate the commercialization of plug-in HEV very soon in the near future, and it will sustain for long time. FCVs are under development stage, and it will take time for their successful commercialization. FCV can be seen as the future of transportation system in long run.

The comprehensive review of EPS indicates that the recent modification in EPS due to technological advancement of its members, like ESS, PEC, EM, and ECU, makes EVT capable enough to compete against conventional ICE-based vehicular technology. Among all the components, PECs play crucial role as it bears the responsibility of compatible integration proper coordination among all the electric, mechanical, and electronic components on board. Also, the PEC controls and manages power flow from different energy sources and vehicle loads at appropriate voltage level and hence behaves as a heart of EPS in vehicle architecture. The integration and packaging of different components of EPS along with power electronic components are the challenging issues that need to be addressed properly so that weight, volume, and cost can be reduced significantly. For successive advancement of EPS, technical breakthroughs are necessary from device level to system level, so that improved performance, higher efficiency, longer driving distance, and higher degree of reliability can be achieved from electrified vehicles.

References

[1] D. Streimikiene, T. Baležentis, L. Baležentien, Comparative assessment of road transport technologies, Renew. Sustain. Energy Rev. 20 (2013) 611–618.
[2] Mobility 2030: "Meeting the Challenges of Sustainability", World Business Council for Sustainable Development (WBCSD) July 2004a and 2004b.
[3] International Energy Agency, Global EV outlook: Understanding the electric vehicle landscape to 2020. [Online]. Available: https://www.iea.org/publications/freepublications/publication/GlobalEVOutlook_2013.pdf, 2013.
[4] C.C. Chan, Y.S. Wong, Electric vehicles charge forward, IEEE Power Energy Mag. 2 (6) (2004) 24–33.
[5] A. Emadi, Transportation 2.0, IEEE Power Energy Mag. 9 (4) (2011) 18–29.
[6] Lalit Kumar, S. Jain, Development of Power Electronic Interface for Electric Propulsion System, PhD Dissertation, MANIT, Bhopal, India, 2016.
[7] S.S. Williamson, A. Emadi, Comparative assessment of hybrid electric and fuel cell vehicles based on comprehensive well-to-wheels efficiency analysis, IEEE Trans. Veh. Technol. 54 (3) (2005) 856–862.
[8] C.C. Chan, The state of the art of electric, hybrid, and fuel cell vehicles, Proc. IEEE 95 (4) (2007) 704–718.
[9] A. Emadi, K. Rajashekara, S.S. Williamson, S.M. Lukic, Topological overview of hybrid electric and fuel cell vehicular power system architectures and configurations, IEEE Trans. Veh. Technol. 54 (3) (2005) 763–770.
[10] K.T. Chau, Y.S. Wong, Overview of power management in hybrid electric vehicle, Energy Convers. Manag. 43 (2002) 1953–1968. Elsevier.
[11] R. Ghorbani, E. Bibeau, S. Filizadeh, On conversion of hybrid electric vehicles to plug-in, IEEE Trans. Veh. Technol. 59 (4) (2010) 2016–2020.
[12] D.P. Tuttle, R. Baldick, The evolution of plug-in electric vehicle-grid interactions, IEEE Trans. Smart Grid 3 (1) (2012) 500–505.
[13] S. Srinivasaraghavan, A. Khaligh, Time management, IEEE Power Energy Mag. 9 (4) (2011) 46–53.
[14] F. Nemry, G. Leduc, A. Muñoz, Plug-in Hybrid and Battery-Electric Vehicles: State of the Research and Development and Comparative Analysis of Energy and Cost Efficiency, JRC Technical Notes, European Communities, 2009.

[15] B. Kramer, S. Chakraborty, B. Kroposki, A review of plug-in vehicles and vehicle-to-grid capability, in: Industrial Electronics, 2008. IECON 2008. 34th Annual Conference of IEEE, 10–13 Nov, 2008, pp. 2278–2283.
[16] APEEM Annual Progress Report, http://www1.eere.energy.gov/vehiclesandfuels/pdfs (accessed 12.07.10).
[17] K.T. Chau, Y.S. Wong, C.C. Chan, An overview of energy sources for electric vehicle, Energy Convers. Manage. 40 (1999) 1953–1968. Elsevier.
[18] A. Khaligh, Z. Li, Battery, ultracapacitor, fuel cell, and hybrid energy storage systems for electric, hybrid electric, fuel cell, and plug-in hybrid electric vehicles: state of the art, IEEE Trans. Veh. Technol. 59 (6) (2010) 2806–2814.
[19] S.F. Tie, C.W. Tan, A review of energy sources and energy management system in electric vehicles, Renew. Sust. Energ. Rev. 20 (2013) 82–102.
[20] L. Sun, C.C. Chan, R. Liang, Q. Wang, State-of-art of energy system for new energy vehicles, in: Vehicle Power and Propulsion Conference, 2008. VPPC '08. IEEE, 3–5 Sept, 2008, pp. 1–8.
[21] B.K. Bose, Power electronics and motor drives recent progress and perspective, IEEE Trans. Ind. Electron. 56 (2) (2009) 581–588.
[22] A. Emadi, Y.J. Lee, K. Rajashekara, Power electronics and motor drives in electric, hybrid electric, and plug-in hybrid electric vehicles, IEEE Trans. Ind. Electron. 55 (6) (2008) 2237–2245.
[23] A. Emadi, S.S. Williamson, A. Khaligh, Power electronics intensive solutions for advanced electric, hybrid electric, and fuel cell vehicular power systems, IEEE Trans. Power Electron. 21 (3) (2006) 567–577.
[24] J.-S. Lai, D.J. Nelson, Energy management power converters in hybrid electric and fuel cell vehicles, Proc. IEEE 95 (4) (2007) 766–777.
[25] L. Kumar, K. Kumar Gupta, S. Jain, Power electronic interface for vehicular electrification, in: IEEE International Symposium on Industrial Electronics, 2013.
[26] B. Akin, S. Choi, H.A. Toliyat, DSP applications in electric and hybrid electric vehicles [in the spotlight], IEEE Trans. Sig. Process 29 (3) (2012) 136. 133.
[27] P. Thounthong, V. Chunkag, P. Sethakul, B. Davat, M. Hinaje, Comparative study of fuel-cell vehicle hybridization with battery or supercapacitor storage device, IEEE Trans. Veh. Technol. 58 (8) (2009) 3892–3904.
[28] J. Bernard, S. Delprat, F.N. Buchi, T.M. Guerra, Fuel-cell hybrid powertrain: toward minimization of hydrogen consumption, IEEE Trans. Veh. Technol. 58 (7) (2009) 3168–3176.
[29] C.C. Chan, K.T. Chau, Modern Electric Vehicle Technology, Oxford University Press, New York, 2001.
[30] M.S. Whittingham, History, evolution, and future status of energy storage, Proc. IEEE 100 (Special Centennial Issue) (2012) 1518–1534.
[31] M. Ortuzar, J. Moreno, J. Dixon, Ultra capacitor-based auxiliary energy system for an electric vehicle: Implementation and evaluation, IEEE Trans. Ind. Electron. 54 (4) (2007) 2147–2156.
[32] S. Lukic, Charging ahead, IEEE Ind. Electron. Mag. 2 (4) (2008) 22–31.
[33] S.M. Lukic, S.G. Wirasingha, F. Rodriguez, J. Cao, A. Emadi, Power management of an ultra-capacitor/battery hybrid energy storage system in an HEV, in: Proceedings of the IEEE Vehicular Power Propulsion Conference, Windsor, UK, 2006, pp. 1–6.
[34] A.F. Burke, Batteries and ultracapacitors for electric, hybrid, and fuel cell vehicles, Proc. IEEE 95 (4) (2007) 806–820.
[35] E. Bakhoum, New mega-farad ultracapacitors, IEEE Trans. Ultra. Ferroelect. Freq. Control 56 (1) (2009) 14–21.
[36] G. Zorpette, Super charged [ultracapacitors], IEEE Spectr. 42 (1) (2005) 32–37.
[37] R. Hebner, J. Beno, A. Walls, Flywheel batteries come around again, IEEE Spectr. 39 (4) (2002) 46–51.
[38] O. Briat, J.M. Vinassa, W. Lajnef, S. Azzopardi, E. Woirgard, Principle, design and experimental validation of a flywheel-battery hybrid source for heavy-duty electric vehicles, IET Electr. Power Appl. 1 (5) (2007) 665–674.
[39] R. Sebastián, R. Peña Alzola, Flywheel energy storage systems: review and simulation for an isolated wind power system, Renew. Sust. Energ. Rev. 16 (2012) 6803–6813.
[40] P. Mock, S.A. Schmid, Fuel cells for automotive powertrains—A techno-economic assessment, J. Power Sources 190 (1) (2009) 133–140.
[41] M.J. Riezenman, Fuel cells for the long haul, batteries for the spurts [electric vehicles], IEEE Spectr. 38 (1) (2001) 95–97.
[42] J. Bauman, M. Kazerani, A comparative study of fuel-cell-battery, fuel-cell-ultracapacitor, and fuel-cell-battery-ultracapacitor vehicles, IEEE Trans. Veh. Technol. 57 (2) (2008) 760–769.
[43] B. Sorensen, Hydrogen and Fuel Cells: Emerging Technologies and Applications, Academic Press, Elsevier, Oxford, UK, 2011. ISBN: 10:0-12-655281-2.
[44] S. Mekhilef, R. Saidur, A. Safari, Comparative study of different fuel cell technologies, Renew. Sust. Energ. Rev. 16 (2012) 981–989.
[45] A. Kirubakaran, S. Jain, R.K. Nema, A review on fuel cell technologies and power electronic interface, Renew. Sust. Energ. Rev. 13 (2009) 2430–2440.
[46] R.T. Doucette, M.D. McCulloch, A comparison of high-speed flywheels, batteries, and ultracapacitors on the bases of cost and fuel economy as the energy storage system in a fuel cell based hybrid electric vehicle, J. Power Sources 196 (3) (2011) 1163–1170.
[47] J.M. Miller, T. Bohn, T.J. Dougherty, U. Deshpande, Why hybridization of energy storage is essential for future hybrid, plug-in, and battery electric vehicles, in: Proceedings of the IEEE Energy Conversion Congress Exposition (ECCE), San Jose, CA, 2009, pp. 2614–2620.
[48] Z.Q. Zhu, D. Howe, Electrical machines and drives for electric, hybrid, and fuel cell vehicles, Proc. IEEE 95 (4) (2007) 746–765.
[49] M. Zeraoulia, M.E.H. Benbouzid, D. Diallo, Electric motor drive selection issues for HEV propulsion systems: a comparative study, IEEE Trans. Veh. Technol. 55 (6) (2006) 1756–1764.
[50] G. Nanda, N.C. Kar, A survey and comparison of characteristics of motor drives used in electric vehicles, in: Canadian Conference on Electrical and Computer Engineering, 2006. CCECE '06, 2006, pp. 811–814.
[51] N. Hashemnia, B. Asaei, Comparative study of using different electric motors in the electric vehicles, in: 18th International Conference on Electrical Machines, 2008. ICEM 2008, 2008, pp. 1–5.
[52] J.G.W. West, DC, induction, reluctance and PM motors for electric vehicles, in: IEE Colloquium on Motors and Drives for Battery Powered Propulsion, 1993. pp. 1/1–111.
[53] J. De Santiago, H. Bernhoff, B. Ekergård, S. Eriksson, S. Ferhatovic, R. Waters, M. Leijon, Electrical motor drivelines in commercial all-electric vehicles: a review, IEEE Trans. Veh. Technol. 61 (2) (2012) 475–484.

[54] Z.Q. Zhu, C.C. Chan, Electrical machine topologies and technologies for electric, hybrid, and fuel cell vehicles, in: IEEE Vehicle Power and Propulsion Conference, 2008. VPPC '08, 2008, pp. 1–6.
[55] R. Fessler, ORNL/TM-2011/73, Final Report on Assessment of Motor Technologies for Traction Drives of Hybrid and Electric Vehicles, published 10 March 2011.
[56] M. Ehsani, Y. Gao, J.M. Miller, Hybrid electric vehicles: architecture and motor drives, Proc. IEEE 95 (4) (2007) 719–728.
[57] T. Wang, et al., Design characteristics of the induction motor used for hybrid electric vehicle, IEEE Trans. Magn. 41 (1) (2005) 505–508.
[58] K.T. Chau, C.C. Chan, C. Liu, Overview of permanent-magnet brushless drives for electric and hybrid electric vehicles, IEEE Trans. Ind. Electron. 55 (6) (2008) 2246–2257.
[59] M.A. Rahman, Recent status on IPM traction drives for plug-in and hybrid electric vehicles, in: IEEE Power and Energy Society General Meeting, 2010, pp. 1–6.
[60] G. Pellegrino, A. Vagati, P. Guglielmi, B. Boazzo, Performance comparison between surface-mounted and interior pm motor drives for electric vehicle application, IEEE Trans. Ind. Electron. 59 (2) (2012) 803–811.
[61] K.M. Rahman, B. Fahimi, G. Suresh, A.V. Rajarathnam, M. Ehsani, Advantages of switched reluctance motor applications to EV and HEV: design and control issues, IEEE Trans. Ind. Electron. 36 (1) (2000) 111–121.
[62] B. Bilgin, A. Emadi, M. Krishnamurthy, Design considerations for switched reluctance machines with a higher number of rotor poles, IEEE Trans. Ind. Electron. 59 (10) (2012) 3745–3756.
[63] C.C. Chan, K.T. Chau, An overview of power electronics in electric vehicles, IEEE Trans. Ind. Electron. 44 (1) (1997) 3–13.
[64] D.M. Bellur, M.K. Kazimierczuk, DC-DC converters for electric vehicle applications, in: Electrical Insulation Conference and Electrical Manufacturing Expo, 2007, pp. 286–293.
[65] Y.-J. Lee, A. Khaligh, A. Emadi, Advanced integrated bidirectional AC/DC and DC/DC converter for plug-in hybrid electric vehicles, IEEE Trans. Veh. Technol. 58 (8) (2009) 3970–3980.
[66] L. Solero, A. Lidozzi, J.A. Pomilio, Design of multiple-input power converter for hybrid vehicles, IEEE Trans. Power Electron. 20 (5) (2005) 1007–1016.
[67] K.P. Yalamanchili, M. Ferdowsi, Review of multiple input DCDC converters for electric and hybrid vehicles, in: Proceedings of the IEEE Vehicle Power and Propulsion Conference, 2005, pp. 160–163.
[68] L. Gao, R.A. Dougal, S. Liu, Power enhancement of an actively controlled battery/ultracapacitor hybrid, IEEE Trans. Power Electron. 20 (1) (2005) 236–243.
[69] J. Cao, A. Emadi, A new battery/ultracapacitor hybrid energy storage system for electric, hybrid, and plug-in hybrid electric vehicles, IEEE Trans. Power Electron. 27 (1) (2012) 122–132.
[70] S. Lu, K.A. Corzine, M. Ferdowsi, A new battery/ultracapacitor energy storage system design and its motor drive integration for hybrid electric vehicles, IEEE Trans. Veh. Technol. 56 (4) (2007) 1516–1523.
[71] T.M. Jahns, V. Blasko, Recent advances in power electronics technology for industrial and traction machine drives, Proc. IEEE 89 (6) (2001) 963–975.
[72] M. Yilmaz, P.T. Krein, Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles, IEEE Trans. Power Electron. 28 (5) (2013) 2151–2169.
[73] Y.-J. Lee, A. Khaligh, A. Emadi, Advanced integrated bidirectional AC/DC and DC/DC converter for plug-in hybrid electric vehicles, IEEE Trans. Veh. Technol. 58 (8) (2009) 3970–3980.
[74] Z.J. Shen, I. Omura, Power semiconductor devices for hybrid, electric, and fuel cell vehicles, Proc. IEEE 95 (4) (2007) 778–789.
[75] H. Zhang, L.M. Tolbert, B. Ozpineci, Impact of SiC Devices on hybrid electric and plug-in hybrid electric vehicles, IEE J. Ind. Appl. 47 (2) (2011) 912–921.
[76] F. Musavi, M. Edington, W. Eberle, W.G. Dunford, Evaluation and efficiency comparison of front end AC-DC plug-in hybrid charger topologies, IEEE Trans. Smart Grid 3 (1) (2012) 413–421.
[77] SAE Electric Vehicle Inductive Coupling Recommended Practice, SAE 5-1773, 1995.
[78] L. Kumar, S. Jain, Electric propulsion system for electric vehicular technology: a review, Renew. Sust. Energ. Rev. 29 (2014) 924–940.
[79] https://www1.eere.energy.gov/vehiclesandfuels/pdfs/program/2013_apeem_report.pdf (accessed 27.07.13).
[80] L.E. Lesster, Fuel cell power electronics: managing a variable-voltage dc source in a fixed-voltage ac world, Fuel Cells Bull. 3 (25) (2000) 5–9.
[81] A. Khaligh, J. Cao, Y.-J. Lee, A multiple-input DC-DC converter topology, IEEE Trans. Power Electron. 24 (3) (2009) 862–868.
[82] L. Kumar, S. Jain, Multiple-input DC/DC converter topology for hybrid energy system, IET Power Electron. 6 (8) (2013) 1483–1501.
[83] H. Tao, A. Kotsopoulos, J. Duarte, M.A.M. Hendrix, Family of multiport bidirectional dc-dc converters, IEE Proc. Electric Power Appl. 153 (3) (2006) 451–458.
[84] W. Jiang, B. Fahimi, Multiport power electronic interface—concept, modeling, and design, IEEE Trans. Power Electron. 26 (7) (2011) 1890–1900.
[85] B. Singh, B.N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, D. P. Kothari, A review of three-phase improved power quality ac-dc converters, IEEE Trans. Ind. Electron. 51 (3) (2004) 641–660.
[86] C.B. Toepher, Charge! EVs power up for the long haul, IEEE Spectr. 35 (11) (1998) 41–47.
[87] G.Y. Choe, J.S. Kim, B.K. Lee, C.Y. Won, T.W. Lee, A bidirectional battery charger for electric vehicles using photovoltaic PCS systems, in: Proceedings of the IEEE Vehicular Power Propulsion Conference, 2010, pp. 1–6.
[88] M.A. Fasugba, P.T. Krein, Gaining vehicle-to-grid benefits with unidirectional electric and plug-in hybrid vehicle chargers, in: Proceedings of the IEEE Vehicular Power and Propulsion Conference, 2011, pp. 1–6.
[89] B. Singh, B.N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, D. P. Kothari, A review of single-phase improved power quality AC-DC converters, IEEE Trans. Ind. Electron. 50 (5) (2003) 962–981.
[90] D. Aggeler, F. Canales, H. Zelaya - De La Parra, A. Coccia, N. Butcher, O. Apeldoorn, Ultra-fast dc-charge infrastructures for EV-mobility and future smart grids, in: Proceedings of the IEEE Power Energy Society Innovative Smart Grid Technologies Conference Europe, 2010, pp. 1–8.
[91] Y. Du, S. Lukic, B. Jacobson, A. Huang, Review of high power isolated bi-directional DC-DC converters for PHEV/EV DC charging infrastructure, in: Proceedings of the IEEE Energy Conversion Congress and Exposition, 2011, pp. 553–560.
[92] S.B. Peterson, J.F. Whitacre, J. Apt, The economics of using plug-in hybrid electric vehicle battery packs for grid storage, J. Power Sources 195 (8) (2010) 2377–2384.

[93] W.E. Rippel, Integrated traction inverter and battery charger apparatus, U.S. Patent 4,920,475, 1990.
[94] S. Haghbin, K. Khan, S. Lundmark, M. Alaküla, O. Carlson, M. Leksell, O. Wallmark, Integrated chargers for EV's and PHEV's: Examples and new solutions, in: Proceedings of the International Conference on Electrical Machines, 2010, pp. 1–6.
[95] D.G. Woo, G.Y. Choe, J.S. Kim, B.K. Lee, J. Hur, G. B. Kang, Comparison of integrated battery chargers for plug-in electric vehicles: Topology and control, in: Proceedings of the Electric Machines and Drives Conference, 2011, pp. 1294–1299.
[96] L. Tang, G.J. Su, A low-cost, digitally-controlled charger for plug-in hybrid electric vehicles, in: Proceedings of the IEEE Energy Conversion Congress Expo, 2009, pp. 3923–3929.
[97] W. E. Rippel, A. G. Cocconi, Integrated motor drive and recharge system, U.S. Patent 5099186, 1992.
[98] SAE Electric Vehicle and Plug-in Hybrid Electric Vehicle Conductive Charge Coupler, SAE Standard J1772.
[99] G.A. Covic, J.T. Boys, H.G. Lu, A three-phase inductively coupled power transfer system, in: 1ST IEEE Conference on Industrial Electronics and Applications, Singapore, 2006, pp. 1–6.
[100] J.J. Huh, S.W. Lee, W.Y. Lee, G.H. Cho, C.T. Rim, Narrowwidth inductive power transfer system for online electrical vehicles, IEEE Trans. Power Electron. 26 (12) (2011) 3666–3679.
[101] H.L. Li, A.P. Hu, G.A. Covic, A direct ac-ac converter for inductive power-transfer systems, IEEE Trans. Power Electron. 27 (2) (2012) 661–668.
[102] K. Çağatay Bayindir, M. Ali Gözüküçük, A. Teke, A comprehensive overview of hybrid electric vehicle: powertrain configurations, powertrain control techniques and electronic control units, Energy Convers. Manag. 52 (2) (2011) 1305–1313, Elsevier.
[103] D.W. Gao, C. Mi, A. Emadi, Modeling and simulation of electric and hybrid vehicles, Proc. IEEE 95 (4) (2007) 729–745.
[104] www.proteanelectric.com (accessed 09.03.13).
[105] www.delphi.com (accessed 21.05.12).
[106] S.G. Wirasingha, A. Emadi, Classification and review of control strategies for plug-in hybrid electric vehicles, IEEE Trans. Veh. Technol. 60 (1) (2011) 111–122.
[107] F.R. Salmasi, Control strategies for hybrid electric vehicles: evolution, classification, comparison, and future trends, IEEE Trans. Veh. Technol. 56 (5) (2007) 2393–2404.

Further Reading

[108] M. Ehsani, K.M. Rahman, H.A. Toliyat, Propulsion system design of electric and hybrid vehicles, IEEE Trans. Ind. Electron. 44 (1) (1997) 19–27.

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Automotive Applications of Power Electronics

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32.1 Introduction

The modern automobile has an extensive electric system consisting of a large number of electric, electromechanical, and electronic loads that are central to vehicle operation, passenger safety, and comfort. Power electronics is playing an increasingly important role in automotive electric systems—conditioning the power generated by the alternator, processing it appropriately for the vehicle electric loads, and controlling the operation of these loads. Furthermore, power electronics is an enabling technology for a wide range of future loads with new features and functions. Such loads include electromagnetic engine valves, active suspension, controlled lighting, and electric propulsion.

This chapter discusses the application and design of power electronics in automobiles. Section 32.2 provides an overview of the architecture of the present automotive electric power system. The next section, Section 32.3, describes the environmental factors, such as voltage ranges, EMI/EMC requirements, and temperature, which strongly influence the design of automotive power electronics. Section 32.4 discusses a number of electric functions that are enabled by power electronics, while Section 32.5 addresses load control via multiplexed remote switching architectures that can be implemented with power electronic switching. Section 32.6 considers the application of power electronics in automotive electromechanical energy conversion, including power generation. Section 32.7 describes the potential evolution of automotive electric systems toward high- and dual-voltage systems and provides an overview of the likely requirements of power electronics in such systems. Finally, the application of power electronics in electric and hybrid electric vehicles (HEVs) is addressed in Section 32.8.

32.2 The Present Automotive Electrical Power System

Present-day automobiles can have over 200 individual electric loads, with average power requirements in excess of 800 W.

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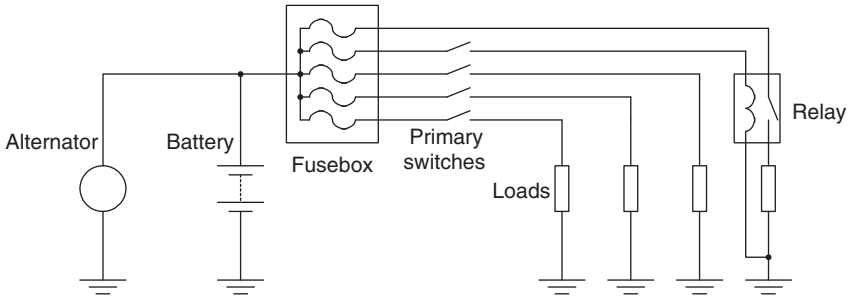


FIG. 32.1 The 12 V point-to-point automotive electric power system.

These include such functions as the headlamps, tail lamps, cabin lamps, starter, fuel pump, wiper, blower fan, fuel injector, transmission shift solenoids, horn, cigar lighter, seat heaters, engine control unit, cruise control, radio, and spark ignition. To power these loads, present-day internal-combustion-engine (ICE) automobiles use an electric power system similar to the one shown in Fig. 32.1. Power is generated by an engine-driven three-phase wound-field synchronous machine—a Lundell (claw-pole) alternator [1,2]. The ac voltage of this machine is rectified and the dc output regulated to about 14 V by an electronic regulator that controls the field current of the machine. The alternator provides power to the loads and charges a 12 V lead-acid battery. The battery provides the high power needed by such loads as the starter and supplies power when the engine is not running or when the demand for electric power exceeds the output power of the alternator. The battery also acts as a large capacitor and smoothes out the system voltage.

Power is distributed to the loads via fuses and point-to-point wiring. The fuses, located in one or more fuse boxes, protect the wires against overheating and fire in the case of a short circuit. Most of the loads are controlled directly by manually actuated mechanical switches. These primary switches are located in areas in easy reach of either the driver or the passengers, such as the dashboard, the door panels, and the ceiling. Some of the heavy loads, such as the starter, are switched indirectly via electromechanical relays.

32.3 System Environment

The challenging electric and environmental conditions found in the modern automobile have a strong impact on the design of automotive power electronic equipment. Important factors affecting the design of electronics for this application include static and transient voltage ranges, electromagnetic interference and compatibility requirements (EMI/EMC), mechanical vibration and shock, and temperature and other environmental conditions. This section briefly describes some of the factors that most strongly affect the design of power electronics for automotive applications. For more detailed guidelines on the design of electronics for automotive applications, the reader is referred to [1,3–16] and the documents cited therein, from which much of the information presented here is drawn.

32.3.1 Static Voltage Ranges

In most present-day automobiles, a Lundell-type alternator provides dc electric power with a lead-acid battery for energy storage and buffering. The nominal battery voltage is 12.6 V, which the alternator regulates to 14.2 V when the engine is on in order to maintain a high state of charge on the battery. In practice, the regulation voltage is adjusted for temperature to match the battery characteristics. For example, in Ref. [1], a 25°C regulation voltage of 14.5 V is specified with a −10 mV/°C adjustment. Under normal operating conditions, the bus voltage will be maintained in the range of 11–16 V [3]. Safety-critical equipment is typically expected to be operable even under battery discharge down to 9 V, and equipment operating during starting may see a bus voltage as low as 4.5–6 V under certain conditions.

In addition to the normal operating voltage range, a wider range of conditions is sometimes considered in the design of automotive electronics [3]. One possible condition is reverse-polarity battery installation, resulting in a bus voltage of approximately −12 V. Another static overvoltage condition can occur during jump starting from a 24 V system such as on a tow truck. Other static overvoltage conditions can occur due to failure of the alternator voltage regulator. This can result in a bus voltage as high as 18 V, followed by battery electrolyte boil-off, and a subsequent unregulated bus voltage as high as 130 V. Typically, it is not practical to design the electronics for operation under such an extreme fault condition, but it should be noted that such conditions can occur. Table 32.1 summarizes the range of static voltages that can be expected in the automotive electric system.

32.3.2 Transients and Electromagnetic Immunity

Power electronic circuits designed for automotive applications must exhibit electromagnetic compatibility, that is, the conducted and radiated emissions generated by the circuit must not interfere with other equipment on board the vehicle, and the circuit must exhibit immunity to radiated and conducted disturbances. The Society of Automotive Engineers (SAE) has laid out standards and recommended practices for the electromagnetic compatibility of automotive electronics in a set of technical reports [4]. These reports are listed in Table 32.2.

TABLE 32.1 Static voltage range for the automotive electric system [3]

Static voltage condition	Voltage
Nominal voltage with engine on	14.2 V
Nominal voltage with engine off	12.6 V
Maximum normal operating voltage	16 V
Minimum normal operating voltage	9 V
Minimum voltage during starting	4.5 V
Jump-start voltage	24 V
Reverse-battery voltage	−12 V
Maximum voltage with alternator-regulator failure followed by battery failure	130 V

Here, we will focus on two of the basic requirements of automotive power electronics, immunity to power lead transients and limitation of conducted emissions.

A major consideration in the design of an automotive power electronic system is its immunity to the transients that can appear on its power leads. A number of transient sources exist in the vehicle [5], and procedures for validating immunity to these transients have been established in documents such as SAE J1113/11 [4,6] and DIN 40389 [1]. Table 32.3 illustrates the transient test pulses specified in SAE J1113/11. Each test pulse corresponds to a different type of transient. The vehicle manufacturer determines which test pulses apply to a specific device.

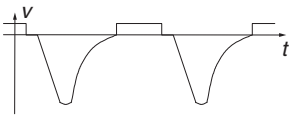
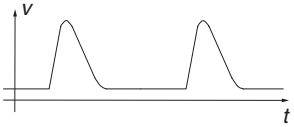
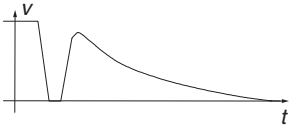
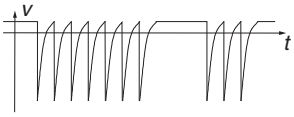
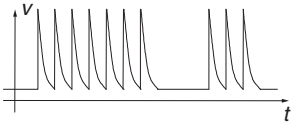
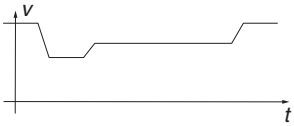
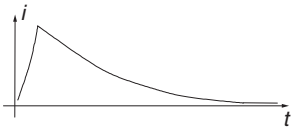
Transients occur when inductive loads such as solenoids, motors, and clutches are turned on and off. The transients can be especially severe when the bus is disconnected from the battery, as is the case for the accessory loads when the ignition is switched off. Test pulse 1 in Table 32.3 simulates the transient generated when an inductive load is disconnected from the battery and the device under test remains in parallel with it. When the inductive load is a dc motor, it may briefly act as a generator after disconnection. This transient is simulated by test pulse 2b. Test pulse 2a models the transient when current in an inductive element in series with the device under test is interrupted. Test pulses 3a and 3b model switching spikes that appear on the bus during normal operation. Test pulse 4 models the voltage transient that occurs on starting.

Perhaps, the best-known electric disturbance is the so-called load-dump transient that occurs when the alternator load current drops sharply and the battery is unable to properly buffer the change. This can occur when the battery becomes disconnected while drawing a large amount of current. To understand why a major transient can occur under this situation, consider that the Lundell alternator has a very large leakage reactance. The high commutating reactance interacting with the diode rectifier results in a high degree of load regulation, necessitating the use of a large back emf to source-rated current at high speed [7]. Back voltages as high as 120 V may be needed to generate rated current into a 14 V output at top speed. Analytic modeling of such systems is addressed in Ref. [8]. Two effects occur when the load on the alternator suddenly steps down. First, as the machine current drops, the energy in the alternator leakage reactances is immediately delivered to the alternator output, causing a voltage spike. The peak voltage reached depends on the electric system impedance and may be limited by suppression devices. Second, once the alternator current is reduced, the voltage drops across the leakage (commutating) reactances are reduced, and a much larger fraction of the machine back emf is impressed across the dc output. The proper output voltage is only reestablished as the voltage regulator reduces the field current appropriately. With conventional regulator circuits, this takes place on the time scale of the field-winding time constant (typically 100 ms) and results in a major transient event. In systems without centralized protection, a load dump can generate a transient with a peak voltage in excess of 100 V lasting hundreds of milliseconds. Test pulse 5 in Table 32.3 (expressed as a current waveform in parallel with an output resistance) is designed to simulate such a load-dump transient; other load-dump tests are even more severe [1,3].

TABLE 32.2 SAE J1113 electromagnetic compatibility technical reports

SAE specification	Type	Description
SAE J1113/1	Standard	Electromagnetic compatibility measurement procedures and limits, 60 Hz–18 GHz
SAE J1113/2	Standard	Conducted immunity, 30 Hz–250 kHz
SAE J1113/3	Standard	Conducted immunity, direct injection of RF power, 250 kHz–500 MHz
SAE J1113/4	Standard	Conducted immunity, bulk current injection method
SAE J1113/11	Standard	Conducted immunity to power lead transients
SAE J1113/12	Recommended practice	Electric interference by conduction and coupling—coupling clamp
SAE J1113/13	Recommended practice	Immunity to electrostatic discharge
SAE J1113/21	Information report	Electric disturbances by narrowband radiated electromagnetic energy—component test methods
SAE J1113/22	Standard	Immunity to radiated magnetic fields from power lines
SAE J1113/23	Recommended practice	Immunity to radiated electromagnetic fields, 10 kHz–200 MHz, strip-line method
SAE J1113/24		Immunity to radiated electromagnetic fields, 10 kHz–200 MHz, TEM cell method
SAE J1113/25	Standard	Immunity to radiated electromagnetic fields, 10 kHz–500 MHz, triplate-line method
SAE J1113/26	Recommended practice	Immunity to ac power line electric fields
SAE J1113/27	Recommended practice	Immunity to radiated electromagnetic fields, reverberation method
SAE J1113/41	Standard	Radiated and conducted emissions, 150 kHz–1000 MHz
SAE J1113/42	Standard	Conducted transient emissions

TABLE 32.3 Transient pulse waveforms specified in SAE J1113/11

Pulse	Shape	Maximum excursion	Source impedance	Duration and repetition rate
1		−100 V	10 Ω	$T_{pulse}=2$ ms 0.5 s < T_{rep} < 5 s
2a		100 V	10 Ω	$T_{pulse}=50$ μs 0.5 s < T_{rep} < 5 s
2b		10 V	0.5–3 Ω	$T_{pulse} \geq 200$ ms
3a		−150 V	50 Ω	$T_{pulse}=100$ ns $T_{rep}=100$ μs
3b		100 V	50 Ω	$T_{pulse}=100$ ns $T_{rep}=100$ μs
4		−7 V	0.01 Ω	$T_{pulse} \leq 20$ s
5		84 A	0.6 Ω	$\tau=115$ ms $T_{pulse} \sim 4\,\tau$

32.3.3 Electromagnetic Interference

Strict limits also exist for the amount of electromagnetic interference (EMI) that an automotive electronic component can generate. Limits for both conducted and radiated emissions are specified in SAE standards J1113/41 and J1113/42 [4,9,10]. Here, we will consider the conducted EMI specifications for power leads, since they directly impact the design of EMI filters for automotive power electronics. Meeting the conducted specifications is a major step toward achieving overall compliance.

The conducted EMI specifications in SAE J1113/41 limit the ripple that an electronic circuit can inject onto the voltage bus over the frequency range from 150 kHz to 108 MHz. The amount of ripple injected by a circuit usually depends on the bus impedance. To eliminate any variability due to this, EMI compliance testing is done using a line impedance stabilization network (LISN) between the bus and the device under test, as illustrated in Fig. 32.2. The LISN is also sometimes referred to as an artificial mains network (AN). Essentially, the LISN ensures that the equipment under test receives the proper dc voltage and current levels and also sees a controlled impedance for the ripple frequencies of interest. Fig. 32.3 shows the magnitude of the LISN output impedance for a low-impedance input source; the effective impedance is 50 Ω over most of the frequency range of interest. The 50 Ω termination impedance of the LISN is typically provided by the measurement equipment. The EMI specifications are stated in terms of the

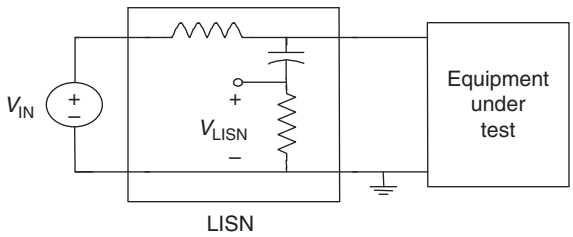


FIG. 32.2 Conducted EMI test setup with LISN. $L_{LISN}=5$ μH, $C_{LISN}=0.1$ μF, and $R_{LISN}=50$ Ω.

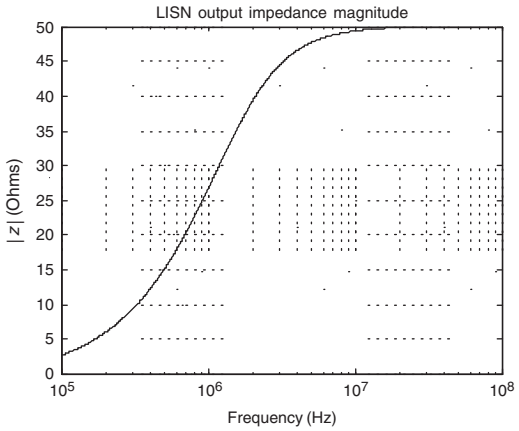


FIG. 32.3 The LISN output impedance magnitude for a low-impedance input source.

allowable voltage ripple (in dB μV) appearing across the 50-Ω LISN resistance as a function of frequency.

There are a wide range of other technical considerations for EMI testing, including the arrangement of the equipment over a ground plane and the types and settings of the measuring devices. One characteristic to consider is that the EMI measurements are done across frequency with a spectrum analyzer having a prespecified receiver bandwidth (RBW). For frequencies between 150 kHz and 30 MHz, the receiver bandwidth is 9 kHz, resulting in spectral components within 9 kHz of one another being lumped together for purposes of the test. A full test procedure is defined in the SAE specifications, beginning with narrowband measurements and moving to wideband measurements if necessary. Fig. 32.4 illustrates the narrowband conducted EMI limits for power leads in SAE J1113/41. It is interesting to note that for the commonly used class 5 limits, the allowable ripple current into the LISN at 150 kHz is less than 100 μA!

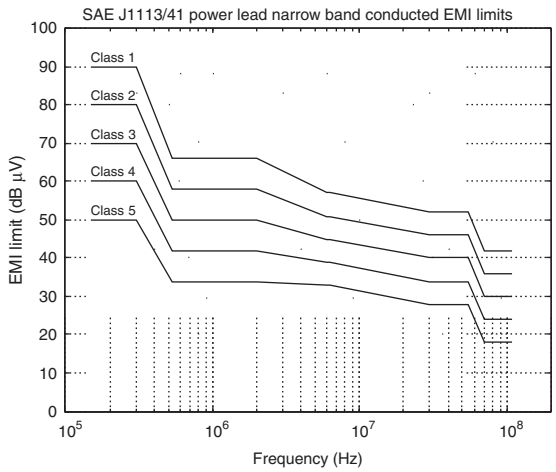


FIG. 32.4 SAE J1113/41 narrowband conducted EMI limits for power leads. The specification covers the frequency range from 150 kHz to 108 MHz.

As seen in the previous section, the transient disturbances generated by electric and electronic equipment are an important consideration in automotive applications. Because power electronic circuits typically contain switches and magnetic elements, they are potential sources for such transients, especially when powered from the switched ignition line. SAE J1113/42 specifies methods for testing and evaluating the transients generated by automotive electric components and proposes transient waveform limits for different severity levels. The equipment under test is set up in a configuration similar to that in Fig. 32.2 but with a switching device on one side or the other of the LISN, depending on the application. The equipment under test is then evaluated for transient behavior at turn-on, turnoff, and across its operating range. The voltage transients at the input of the equipment are measured and evaluated with respect to magnitude, duration, and rise and fall times. Specific limits for such transients are specified by the vehicle manufacturer, but SAE J1113/42 proposes a representative set of limits for four different transient severity levels.

Due to the tight conducted emission limits, input EMI filter design is an important consideration in automotive power electronics. Single- or multistage low-pass filters are typically used to attenuate converter ripple to acceptable levels [11–13]. When designing such filters, the parasitic behaviors of the filter components, such as capacitor equivalent series resistance and inductance and suitable filter damping, are important considerations [14]. One must also ensure that the filter design yields acceptable transients at switch on and off, and does not result in undesired dynamic interactions with the power circuit [13]. Attention to appropriate filter design, coupled with proper circuit layout, grounding, and shielding, goes a long way toward meeting electromagnetic interference specifications [14].

32.3.4 Environmental Considerations

The automobile is a very challenging environment for electronics. Environmental factors influencing the design of automotive electronics include temperature, humidity, mechanical shock, vibration, immersion, salt spray, and exposure to sand, gravel, oil, and other chemicals. In 1978, the SAE developed a recommended practice for electronic equipment design to address these environmental considerations [3,4]. This document, SAE J1211, provides quantitative information about the automotive environment to aid the designer in developing environmental design goals for electronic equipment. Here, we briefly summarize a few of the most important factors affecting the design of power electronics for automotive applications. For more detailed guidelines, the reader is referred to [3] and the documents cited therein.

Perhaps, the most challenging environmental characteristic is the extreme range of temperatures that can occur in the automobile. Table 32.4 summarizes some of the temperature

TABLE 32.4 Automotive temperature extremes by location [3]

Vehicle location	Min temp. (°C)	Max temp. (°C)
Exterior	−40	85
Chassis		
Isolated	−40	85
Near heat source	−40	121
Drivetrain high-temperature location	−40	177
Interior		
Floor	−40	85
Rear deck	−40	104
Instrument panel	−40	85
Instrument panel top	−40	177
Trunk	−40	85
Under hood		
Near radiator support structure	−40	100
Intake manifold	−40	121
Near alternator	−40	131
Exhaust manifold	−40	649
Dash panel (normal)	−40	121
Dash panel (extreme)	−40	141

extremes listed in SAE J1211 for different locations in the automobile. Ambient temperatures as low as −40°C may be found during operation, and storage temperatures as low as −50°C may be found for components shipped in unheated aircraft. Maximum ambient temperatures vary widely depending on vehicle location, even for small differences in position. Because ambient temperature has a strong impact on the design of a power electronic system, it is important to work closely with the vehicle manufacturer to establish temperature specifications for a particular application. For equipment that is air-cooled, one must also consider that the equipment may be operated at altitudes up to 12,000 ft above sea level. This results in low ambient pressure (down to 9 psia), which can reduce the heat transfer efficiency [3]. For equipment utilizing the radiator-cooling loop, maximum coolant temperatures in the range of 105–120°C at a pressure of 1.4 bar are possible [15].

In addition to the temperature extremes in the automobile, thermal cycling and shock are also important considerations due to their effect on component reliability. Thermal cycling refers to the cumulative effects of many transitions between temperature extremes, while thermal shock refers to rapid transitions between temperature extremes, as may happen when a component operating at high temperature is suddenly cooled by water splash. The damaging effects of thermal cycling and shock include failures caused by thermal expansion mismatches between materials. Test methods have been developed that are designed to expose such weaknesses [3,16]. The thermal environments in the automobile, including the temperature extremes, cycling, and shock, are challenging issues that must be addressed in the design of automotive power electronics.

A number of other important environmental factors exist in the automobile. Humidity levels as high as 98% at 38°C can exist in some areas of the automobile, and frost can occur in situations where the temperature drops rapidly. Salt atmosphere, spray, water splash, and immersion are also important factors for exterior, chassis, and underhood components. Failure mechanisms resulting from these factors include corrosion and circuit bridging. Dust, sand, and gravel bombardment can also be significant effects depending on equipment location. Mechanical vibration and shock are also important considerations in the design of automotive power electronic equipment. Details about the effects of these environmental factors, sample recorded data, and recommended test procedures can be found in Ref. [3].

32.4 Functions Enabled by Power Electronics

Over the past 20 years, power electronics has played a major role in the introduction of new functions such as the antilock braking system (ABS), traction control, and active suspension, as well as the electrification of existing functions such as the engine-cooling fan, in the automobile. This trend is expected to continue, as a large number of new features being considered for introduction into automobiles require power electronics. This section discusses some of the new functions that have been enabled by power electronics and some existing ones that benefit from it.

32.4.1 High Intensity Discharge Lamps

High-intensity discharge (HID) lamps have started to appear in automobiles as low-beam headlights and fog lights. The HID lamps offer higher luminous efficacy, higher reliability, longer life, and greater styling flexibility than the traditional halogen lamps [17,18]. The luminous efficacy of an HID lamp is over three times that of a halogen lamp, and its life is about 2000 h, compared with 300–700 h for a halogen lamp. Therefore, HID lamps provide substantially higher road illumination while consuming the same amount of electric power and, in most cases, should last the life of the automobile. The HID lamps also produce a whiter light than halogen lamps since their color spectrum is closer to that of the sun.

High-intensity discharge lamps do not have a filament. Instead, light is generated by discharging an arc through a pressurized mixture of mercury, xenon, and vaporized metal halides—mercury produces most of the light, the metal halides determine the color spectrum, and xenon helps reduce the start-up time of the lamp [17,19]. Unlike halogen lamps that can be powered directly from the 12 V electric system, HID lamps require power electronic ballasts for their operation. Initially, a high-voltage pulse of 10–30 kV is needed to ignite the arc between the electrodes, and a voltage of about 85 V is needed to sustain the arc [4.3]. Fig. 32.5 shows a simplified power electronic circuit that can be used to start and drive an HID lamp. A step-up dc-dc converter is used to boost the voltage from 12 V to the voltage needed for the steady-state

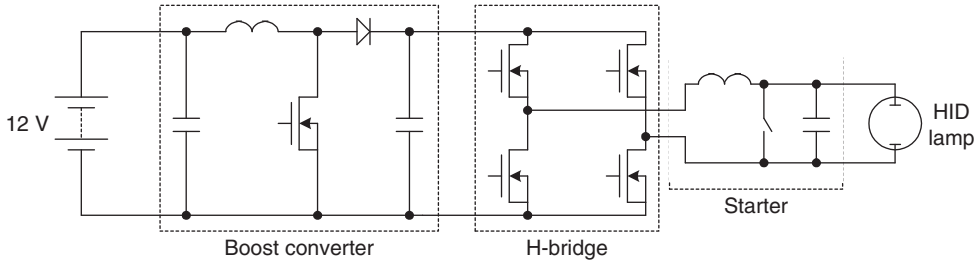


FIG. 32.5 Simplified power electronic circuit for an HID lamp ballast.

operation of the HID lamp. Any dc-dc converter that can step up the voltage, such as the boost or flyback converter, can be used for this application. An H-bridge is then used to create the ac voltage that drives the lamp in steady state. The circuit to initiate the arc can be as simple as a circuit that provides an inductive voltage kick, as shown in Fig. 32.5.

32.4.2 Pulse-Width Modulated Incandescent Lighting

Future automobiles may utilize a 42 V electric system in place of today's 14 V electric system (see Section 32.7). Because HID lamps are driven through a power electronic ballast, HID lighting systems operable from a 42 V bus can be easily developed. However, the high cost of HID lighting—as much as an order of magnitude more expensive than incandescent lighting—largely limits its usefulness to headlight applications. Incandescent lamps compatible with 42 V systems can also be implemented. However, because a much longer, thinner filament must be employed at the higher voltage, lamp lifetime suffers greatly. An alternative to this approach is to use pulse-width modulation to operate 12 V incandescent lamps from a 42 V bus [20].

In a pulse-width modulated (PWM) lighting system, a semiconductor switch is modulated to apply a periodic pulsed voltage to the lamp filament. Because of its resistive nature, the power delivered to the filament depends on the rms of the applied voltage waveform. The thermal mass of the system filters the power pulsations so that the filament temperature and light production are similar to that generated by a dc voltage with the same rms value. The PWM frequency is selected low enough to avoid lamp mechanical resonances and the need for EMI filtering while being high enough to limit visible flicker; PWM frequencies in the range of 90–250 Hz are typical [20].

Ideally, an 11.1% duty ratio is needed to generate 14 V rms across a lamp from a 42 V nominal voltage source. In practice, deviations from this duty ratio are needed to adjust for input voltage variations and device drops. In some proposed systems, multiple lamps are operated within a single lighting module with phase-staggered (interleaved) PWM waveforms to reduce the input rms current of the module.

Another issue with PWM lighting relates to start-up. Even with operation from a 12 V dc source, incandescent lamps have an inrush current that is 6–8 times higher than the steady-state value, because of how filament resistance changes with temperature; this inrush impacts lamp durability. The additional increase in peak inrush current due to operating from a 42 V source can be sufficient to cause destruction of the filament, even when using conventional PWM soft-start techniques (a ramping up of duty ratio). Means for limiting the peak inrush current—such as operating the controlling MOSFET in current-limiting mode during start-up—are needed to make practical use of PWM lighting control.

While PWM incandescent lighting technology is still in the early stages of development, it offers a number of promising advantages in future 42 V vehicles. These include low-cost adaptation of incandescent lighting to high-voltage systems; control of lighting intensity independent of bus voltage; ability to implement multiple intensities, flashing, dimming, etc. through PWM control; and the potential improvement of lamp durability through more precise inrush and operating control [20].

32.4.3 Piezoelectric Ultrasonic Actuators

Piezoelectric ultrasonic motors are being considered as actuators for window lifts, seat positioning, and head restraints in automobiles [21,22]. These motors work on the principle of converting piezoelectrically induced ultrasonic vibrations in an elastic body into unidirectional motion of a moving part. Unidirectional motion is achieved by allowing the vibrating body to make contact with the moving part only during a half cycle of its oscillation, and power is transferred from the vibrating body to the moving part through frictional contact. Ultrasonic motors have a number of attractive features, including high torque density, large holding torque even without input power, low speed without gears, quiet operation, no magnetic fields, and high dynamics [21,23]. These characteristics make ultrasonic motors an attractive alternative to electromagnetic motors for low-power high-torque applications.

Various types of ultrasonic motors have been developed. However, because of its compact design, the traveling-wave type is the most popular ultrasonic motor [24]. Fig. 32.6A shows the basic structure of such a motor. It consists of a metal stator and rotor, which are pushed against each other by a spring. The rotor is coated with a special lining material to increase friction and reduce wear at the contacting surfaces. A layer of piezoelectric material, such as lead zirconate titanate

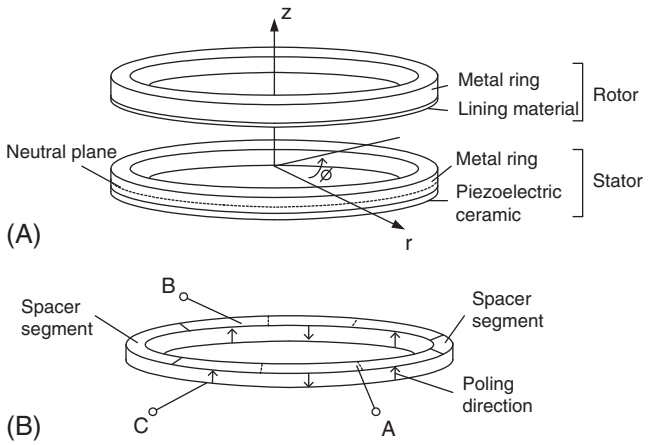


FIG. 32.6 (A) Basic structure of a traveling-wave piezoelectric ultrasonic motor and (B) structure of the piezoceramic ring and electrode for a four-wavelength motor. Arrows indicate direction of polarization. Dashed lines indicate segments etched in the electrode for poling but electrically connected during motor operation.

(PZT), is bonded to the underside of the stator. Silver electrodes are printed on both sides of the piezoceramic ring. The top electrode is segmented, and the piezoceramic is polarized as shown in Fig. 32.6B. The number of segments is twice the order of the excited vibration mode.

When a positive voltage is applied between terminals A and C, the downward-poled segment elongates, and the upward-poled segments contract. This causes the stator to undulate, waving down at the elongated section and up at the contracted one. When the polarity of the voltage is inverted, the undulations are also inverted. Hence, when an ac voltage is applied, a flexural standing wave is created in the stator. To get a large wave amplitude, the stator is driven at the resonance frequency of the flexural mode. An ac voltage between terminals B and C similarly produces another standing wave. However, because of the spacer segments in the piezoceramic ring, the second standing wave is 90 degrees spatially out of phase from the first one. If the two standing waves are excited by ac voltages that are out of phase in time by 90 degrees, a traveling wave is generated. As the traveling wave passes through a point along the neutral plane, that point simply exhibits axial (z-axis) motion. However, off-neutral plane points also have an azimuthal (ϕ-axis) component of motion. This azimuthal motion of the surface points propels the rotor. Ultrasonic motors require a power electronic drive. A power electronic circuit suitable for driving an ultrasonic motor is shown in Fig. 32.7. The two H-bridges are controlled to generate waveforms that are 90 degrees out of phase with each other.

32.4.4 Electromechanical Engine Valves

Electromagnetic actuators are finding increasing application in automotive systems. These actuators are more desirable than

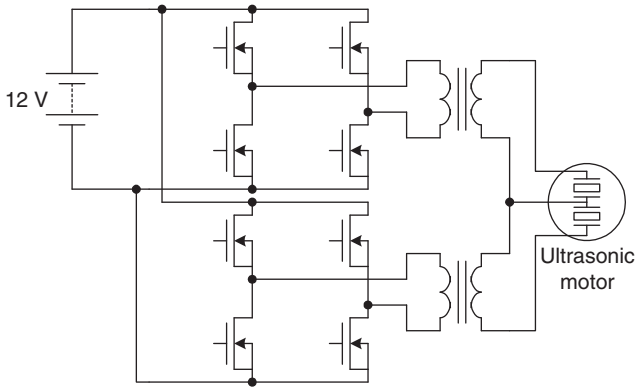


FIG. 32.7 Drive circuit for an ultrasonic motor.

the other types of actuators, such as the hydraulic and pneumatic actuators, because they can be more easily controlled by a microprocessor to provide more precise control. An application of electromagnetic actuators that is of particular interest is the replacement of the camshaft and tappet valve assembly by electromechanically driven engine valves [25]. The opening and closing of the intake and exhaust valves can be controlled to achieve optimum engine performance and improved fuel economy over a wide range of conditions determined by variables such as the speed, load, altitude, and temperature. The present cam system provides a valve profile that can give optimum engine performance and improved fuel economy only under certain conditions.

Two power electronic circuits suitable for driving the solenoids for valve actuation are shown in Fig. 32.8. The circuit of Fig. 32.8A is suitable for solenoids that require unidirectional currents through their coils, while the circuit of Fig. 32.8B is suitable for solenoids that require bidirectional currents through their coils.

32.4.5 Electric Air Conditioner

It is desirable to replace some of the engine-driven functions of a vehicle with electrically driven counterparts. The benefits of driving these functions electrically include the elimination of belts and pulleys, improved design and control due to independence from engine speed, and resulting increased efficiency and improved fuel economy. Furthermore, there is the opportunity for operation of the function in the engine-off condition.

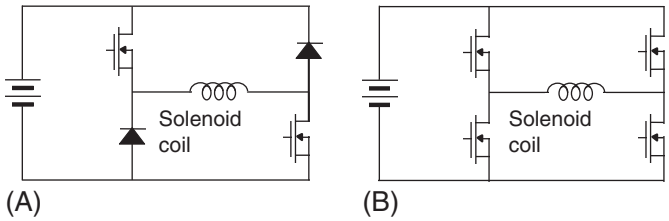


FIG. 32.8 Power electronic circuits for driving solenoids.

The air conditioner is an example of an engine-driven function that could benefit from electrification. The engine drives the compressor of the air conditioner. Consequently, the speed of the compressor varies over a wide range, and the compressor has to be oversized to provide the desired performance at engine idle. Also, since the compressor speed is dependent on the engine speed, excessive cooling occurs at highway speeds requiring the cool air to be blended with the hot air to keep the temperature at the desired level. Furthermore, shaft seals and rubber hoses can lead to the loss of refrigerant (CFC) and pose an environmental challenge.

In an electric air conditioner, an electric motor is used to drive the compressor [26]. The motor is usually a three-phase brushless dc motor driven by a three-phase MOSFET bridge. The speed of the compressor in an electric air conditioner is independent of the engine speed. As a result, the compressor does not have to be oversized, and excessive cooling does not occur. Also, shaft seals and hoses can be replaced with a hermetically sealed system. Another benefit of an electric air conditioner is the flexibility in its location, since it does not have to be driven by the engine.

32.4.6 Electric and Electrohydraulic Power Steering Systems

The hydraulic power steering system of a vehicle is another example of an engine-driven accessory. This system can be replaced with an electric power steering (EPS) system in which a brushless dc motor is used to provide the steering power assist [27]. The electric power steering system is more efficient than the hydraulic power steering system because, unlike the engine-driven hydraulic steering pump, which is driven by the engine all the time, the motor operates only on demand. Another system that can replace the hydraulic power steering system is the electrohydraulic power steering (EHPS) system. In this case, a brushless dc motor and inverter can be employed to drive the hydraulic steering pump. The ability of the EHPS system to drive the pump only on demand leads to energy savings of as much as 80% as compared with the conventional hydraulic system. Challenges in implementing EPS and EHPS systems include meeting the required levels of cost and reliability for this critical vehicle subsystem.

32.4.7 Motor Speed Control

Some of the motors used in a vehicle require variable speed control. Consider, as an example, the blower motor used to provide air flow to the passenger compartment. This motor is typically a permanent-magnet dc motor with a squirrel-cage fan. The speed of the motor is usually controlled by varying the resistance connected in series with the motor winding. This method of speed control leads to a significant power loss. A low-loss method of speed control employs semiconductor devices as shown in Fig. 32.9. In this case, the speed of the motor is controlled via PWM—that is, by switching the MOSFET on and off with different duty ratios for different speed settings. An input filter is needed to reduce the EMI generated by the switching of the MOSFET. This method of speed control is equivalent to supplying power to the motor through a variable-output dc-to-dc converter. The converter is located close to the motor, and no filter is required between the converter output and motor winding.

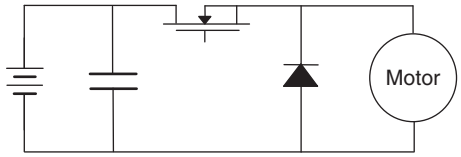


FIG. 32.9 Low-loss circuit to control the speed of a motor.

Another low-loss method that can be used to control the speed of a motor employs a three-phase brushless dc motor. The speed in this case is controlled by controlling the MOSFETs in the dc-to-three-phase-ac converter that drives the motor.

32.5 Multiplexed Load Control

Another emerging application of power electronics in automobiles is in the area of load control. In the conventional point-to-point wiring architecture, most of the loads are controlled directly by the primary mechanical switches, as shown in Fig. 32.1. In a point-to-point wiring architecture, each load has a dedicated wire connecting it to the fuse box via the primary switch. Consequently, fairly heavy wires have to be routed all over the vehicle, as illustrated in Fig. 32.10A. The situation is made worse when multiple switches control the same load, as is the case with power windows and power door locks. The complete harness of a 1994 C-class Mercedes-Benz that uses point-to-point wiring has about 1000 wires, with a total length of 2 km, over 300 connectors, and weighs 32 kg. The process of assembling the wiring harness is difficult and time-consuming, leading to high labor costs. Retrofitting, fault tracing, and repairing are time-consuming and expensive. The bulky harness also places constraints on the vehicle body design, and the large number of connectors compromises system reliability.

An alternative wiring technique is to control the loads remotely and multiplex the control signals over a communication bus, as shown in Fig. 32.10B and C. A control message is sent on the communication bus to switch a particular load on or off. This allows more flexibility in the layout of the power cables and could allow the preassembly of the harness to be more automated. Furthermore, with communication between the remote switches, it is practical to have a power management system than can turn off nonessential loads when there is a power shortage. One possibility is to group the remote switches

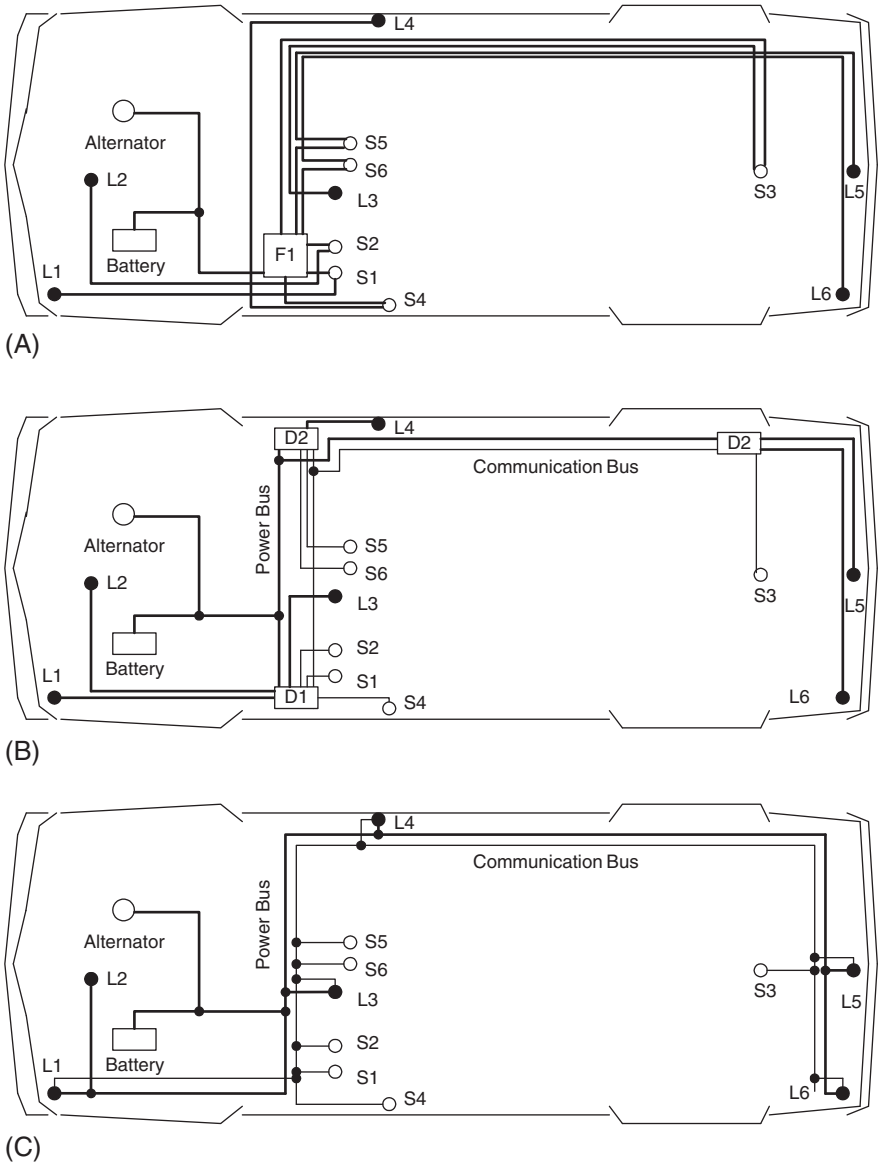


FIG. 32.10 Alternative control strategies illustrated for a simple automotive electric system with six loads (L1-6) and six primary switches (S1-6): (A) conventional direct switching architecture with a single fuse box (F1); (B) multiplexed remote switching architecture, with remote switches and transceivers in three distribution boxes (D1-3); and (C) multiplexed point-of-load switching with electronics integrated into the loads and the primary switches.

into strategically located distribution boxes, as shown in Fig. 32.10B. A power and a communication bus connect the distribution boxes. Another possibility is to integrate the remote switches with the load, that is, point-of-load switching, as shown in Fig. 32.10C. In Fig. 32.10B, the transceivers are also built into the distribution boxes, while in Fig. 32.10C, each load and primary switch has an integrated transceiver. The point-of-load switching topology is attractive because of its simplicity but raises cost and fusing challenges.

Multiplexed remote switching architectures have been under consideration since at least the early 1970s, when Ziomek investigated their application to various electric subsystems [28]. The initial interest was dampened by cost and reliability concerns and the nonavailability of appropriate remote switches. However, advances in semiconductor technology and rapid growth in the automotive electric system revived interest in multiplexed architectures. The SAE Multiplexing Standards Committee has partitioned automotive communications into three classes: class A for low-data-rate (1–10 kbit/s) communication for the control of body functions, such as headlamps, windshield wipers, and power windows; class B for medium-data-rate (10–100 kbit/s) parametric data exchange; and class C for high-data-rate (1 Mbit/s) real-time communication between safety-critical functions, such as between ABS sensors and brake actuators [29]. Although load control is categorized as class A, the lack of any widely accepted class A communication protocols has led to the application of class B and class C communication IC's to load control. Class B has

received the most attention due to the California Air Resources Board mandated requirement for onboard diagnostics (OBD II), and a large number of competing protocols, including the French vehicle area network (VAN), the ISO 9141, and the SAE J1850, have been developed [30]. Of these, the SAE J1850 is the most popular in the United States. Another popular protocol is the controller area network (CAN) developed by Bosch [31]. Although designed for class C with bit rates up to 1 Mbit/s, it is being applied for class A and class B applications due to the availability of inexpensive CAN ICs from a large number of semiconductor manufacturers.

Remote switching systems require remote power switches. An ideal remote switch must have a low on-state voltage, be easy to drive from a microcontroller, and incorporate current sensing. A low on-state voltage helps minimize the heat sinking requirements, while current sensing is needed for the circuit protection function to be incorporated into the switch. To withstand the harsh automotive environment, the switch must also be rugged. Furthermore, if PWM control is required for the load, the switch must have short turn-on and turnoff times and a high cycle life. The traditional means of remotely switching loads in an automobile is via electromechanical relays. Although relays offer the lowest voltage drop per unit cost, they require large drive current, are relatively large, are difficult to integrate with logic, and are not suitable for PWM applications [32–34]. Therefore, their use will be limited to very-high-current, non-PWM applications. The power levels of the individual loads in the automobile are too low for IGBTs and MCTs to be competitive. Bipolar transistors are also not very attractive because they are harder to drive than a MOS-gated device. Because of its fast switching speed, low voltage drop, relative immunity to thermal runaway, low drive requirements, and ease of integration with logic, the power MOSFET is the most attractive candidate for remote switching. Smart-power MOSFET devices with integrated logic interface and circuit protection have recently become available. Use of these devices for power electronic control of individual loads has become economically competitive in some subsystems and may be expected to become more so with the advent of higher-voltage electric systems.

The benefits of remote switching electric distribution systems have been demonstrated by Furuichi et al. [35]. The multiplexed architecture they implemented had 10 remote units (two power units with fuses, power drivers and signal inputs, five load control units with power drivers and signal inputs but no fuses, and three signal input units with only signal inputs). To increase system reliability, each power unit was connected to the battery via independently fused power cables. Although wiring cost decreased, the authors report an increase in overall system cost due to the additional cost of the remote units. Intel's CAN ICs with data rates of 20 kbit/s were used for the transmission and reception of control signals over an unshielded twisted-pair ring bus. Intelligent power MOSFETs were used as the remote switches, and fusing was done with minifuses. The results of their work are shown in Table 32.5.

TABLE 32.5 Comparison of a multiplexed and the conventional system, as reported by Furuichi et al. for a compact vehicle [35]

	Point-to-point	Multiplexed	Change (%)
Harness weight (kg)	14.0	9.8	−30
ECU weight (kg)	1.2	0.0	N/A
Remote unit weight (kg)	0.0	3.5	N/A
Total weight (kg)	15.2	13.3	−12.5
Number of wires	743	580	−21.9
Number of terminals	1195	915	−23.4
Number of splices	295	246	−16.6
Length of wire (m)	809	619	−23.5

In the multiplexed system, the function of nine electronic control units (ECUs) was integrated into the remote units.

Although weight of the wiring harness was reduced by 30%, the total system weight decreased by only 12.5% due to the added weight of the remote units.

32.6 Electromechanical Power Conversion

Power is generated in the automobile by an electric machine driven by the engine. In the early days of the automobile, the electric load was small, and a dc generator was used for this purpose. As the electric loads grew, the dc generator could not meet the growing demand of electric power and was displaced by a three-phase alternator and diode rectifier. Continuously increasing power and performance requirements are driving further evolution in automotive power generation and control and are motivating the introduction of power electronics and improved electric machines in automobiles. In addition to high-power alternators, future applications of electromechanical power conversion may include integrated starter/alternators and propulsion systems. This section describes some of the machine and power electronic technologies that are useful for meeting the increasing challenges in the automobile.

32.6.1 The Lundell Alternator

The Lundell or claw-pole alternator is a three-phase wound-field synchronous machine that is almost universally used for power generation in present-day vehicles [1]. As illustrated in Fig. 32.11, the rotor is made of a pair of stamped pole pieces (claw poles) fixed around a cylindrical field coil. The field winding is driven from the stator via a pair of slip rings and brushes and causes the two pole pieces to become opposing magnetic poles. A full-bridge diode rectifier is traditionally used at the machine output, and a fan mounted on the rotor is typically used to cool the whole assembly.

The dc output voltage of the alternator system is regulated by controlling the field current. A switching field regulator applies a pulse-width modulated voltage across the field. The

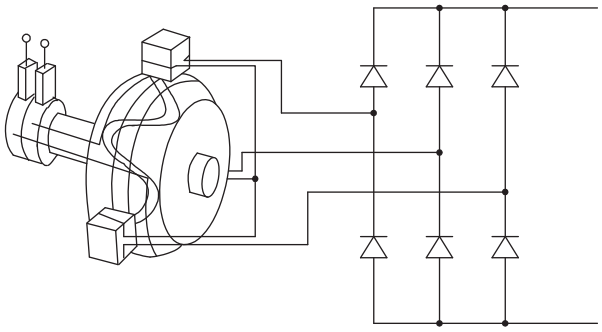


FIG. 32.11 Structure and circuitry of the conventional Lundell alternator.

steady-state field current is determined by the field-winding resistance and the average voltage applied by the regulator. Changes in the field current occur with an L/R field-winding time constant in the order of 100 ms or more. This long field-winding time constant and a large stator leakage reactance are the characteristic of this type of alternator and tend to dominate its performance.

The alternator is driven by means of a belt and is designed to operate over a wide speed ratio of about 10:1, though much of its operating lifetime is spent within a narrower 3:1 or 4:1 range. The gearing ratio provided by the belt is a design variable for the alternator; an alternator mechanical speed range from 1800 to 18,000 rpm for a 12-pole machine is typical.

A simple electric model for the Lundell alternator is shown in Fig. 32.12. The armature of the alternator is modeled as a Y-connected set of leakage inductances L_s and back voltages v_{sa}, v_{sb}, and v_{sc}. The fundamental electric frequency ω of the back emfs is one-half of the product of the number of machine poles p and the mechanical speed ω_m. The magnitude of the back emfs is proportional to the electric frequency and the field current. For the sinusoidal case, the line-to-neutral voltage back-emf magnitude can be calculated as

$$V_s = k\omega i_f \tag{32.1}$$

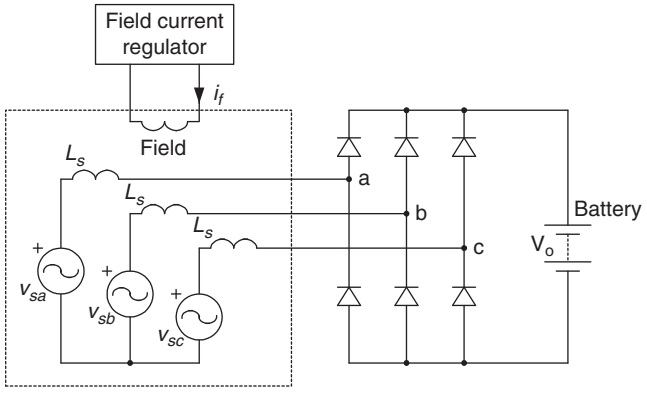


FIG. 32.12 A simple Lundell alternator model.

where k is the machine constant and i_f is the field current. The diode bridge feeds a constant voltage V_o representing the battery and other loads. This simple model captures many of the important characteristics of the Lundell alternator while remaining analytically tractable. Other effects, such as stator resistance, mutual coupling, magnetic saturation, and waveform harmonic content, can be incorporated into this model at the expense of simplicity. The constant-voltage battery load on the alternator makes the analysis of this system different from the classic case of a diode rectifier with a current-source load. Nevertheless, with reasonable approximations, the behavior of this system can be described analytically [8]. Using the results presented in Ref. [8], alternator output power versus operating point can be calculated as

$$P_o = \frac{3V_o\sqrt{V_s^2 - \left(4V_o^2/\pi^2\right)}}{\pi\omega L_s} \tag{32.2}$$

where V_o is the output voltage, V_s is the back-emf magnitude, ω is the electric frequency, and L_s is the armature leakage inductance. Extensions of Eq. (32.2) that also include the effect of the stator resistance are given in Ref. [8].

As can be inferred from Eq. (32.2), alternator output power varies with speed and is maximized when the back-emf magnitude of the machine is substantially larger than the output voltage. In a typical Lundell alternator, back voltages in excess of 80 V may be necessary to source-rated current into a 14 V output at high speed. Furthermore, as can be seen from Eq. (32.2), the armature leakage reactance limits the output power capability of the alternator. These characteristics are a result of the fact that significant voltage drops occur across the leakage reactances when current is drawn from the machine. These drops increase with speed and current and cause the alternator to exhibit significant drop in output voltage with increasing current. Thus, an appropriate dc-side model for a Lundell alternator is a large open-circuit voltage (related to the back-emf magnitude) in series with a large current- and speed-dependent output impedance. This characteristic, coupled with the long field time constant, is the source of the undesirable load-dump transient characteristic of the Lundell alternator. In this transient, the large open-circuit voltage is transiently impressed across the alternator output when the load is suddenly reduced.

The efficiency of the conventional Lundell alternator is relatively poor. Typical efficiency values are in the order of 40%–60%, depending on the operating point [1,36,37]. At low and medium speeds, losses tend to be dominated by stator copper losses. Iron losses become dominant only at very high speeds [1].

32.6.2 Advanced Lundell Alternator Design Techniques

The conventional diode-rectified Lundell alternator, though inefficient, has so far met vehicle electric power requirements

in a cost-effective manner. However, continuing increase in electric power demand and growing interest in improved fuel economy is pushing the limits of conventional Lundell alternator technology. This section describes some established and emerging technologies that can be used to improve the performance of the Lundell alternator.

32.6.2.1 Third-harmonic Booster Diodes

One widely used approach for improving the high-speed output power capability of Lundell alternators is the introduction of third-harmonic booster diodes [1]. In this technique, the neutral point of the Y-connected stator winding is coupled to the output via a fourth diode leg, as illustrated in Fig. 32.13. While the fundamental components of the line-to-neutral back voltages are displaced by 120 degrees in phase, any third-harmonic components will be exactly in phase. As a result, third-harmonic energy can be drawn from the alternator and transferred to the output by inducing and rectifying common-mode third-harmonic currents through the three windings. The booster diodes provide a means for achieving this. At high speed, the combination of the third-harmonic voltages at the main rectifier bridge (at nodes a, b, and c in Fig. 32.13), combined with the third harmonic of the back voltages, is large enough to forward bias the booster diodes and deliver third-harmonic energy to the output. In systems with significant (e.g., 10%) third-harmonic voltage content, up to 10% additional output power can be delivered at high speed. Additional power is not achieved at low speed or in cases where the third harmonic of the back voltage is small.

32.6.2.2 Lundell Alternator With Permanent Magnets

The structure of the rotor of the claw-pole alternator is such that the leakage flux is high. This reduces the output current capability of the alternator. The leakage flux can be reduced by placing permanent magnets on the pole faces or in the spaces between the adjacent poles of the rotor. This modification allows the alternator to deliver more output current. Placing the magnets in the spaces between adjacent poles is a better approach because it is simpler to implement and leads to a higher output current at engine idle [38].

32.6.2.3 Twin-rotor Lundell Alternator

The maximum power capability of the Lundell alternator is limited in part by the limit on its length-to-diameter ratio imposed by mechanical stresses on the stamped pole pieces. This prevents the Lundell alternator from being arbitrarily scaled up in size. The power capability of conventional designs is probably limited to 3 kW, which is likely to be unacceptable in the foreseeable future [39]. One way to retain the cost-effectiveness of the claw-pole alternator while achieving higher output power is to place two claw-pole rotors back-to-back on a common shaft inside a common stator [40]. This effectively increases the length of the claw-pole alternator without changing its diameter. This design allows higher power alternators to be built while retaining most of the cost benefits of the claw-pole design.

32.6.2.4 Power Electronic Control

Another approach for improving the output power and efficiency of the Lundell alternator is through the use of more sophisticated power electronics. Power electronics technology offers tremendous value in this application. For example, replacing the conventional diode rectifier with a switched-mode rectifier provides an additional degree of design and control freedom and allows substantially higher levels of power and efficiency to be attained from a given machine. One such design is shown in Fig. 32.14. It employs a simple switched-mode rectifier along with a special load-matching control technique to achieve dramatic improvement in alternator output power, efficiency, and transient performance [37]. The switched-mode rectifier provides improved control without the cost and complexity of a full active converter bridge. By controlling the duty ratio of the switched-mode rectifier based on available signals such as alternator speed, the alternator output power characteristic Eq. (32.2) can be altered and improved, particularly for speeds above idle [37]. Improvements in average power capability of a factor of two and average efficiency improvements

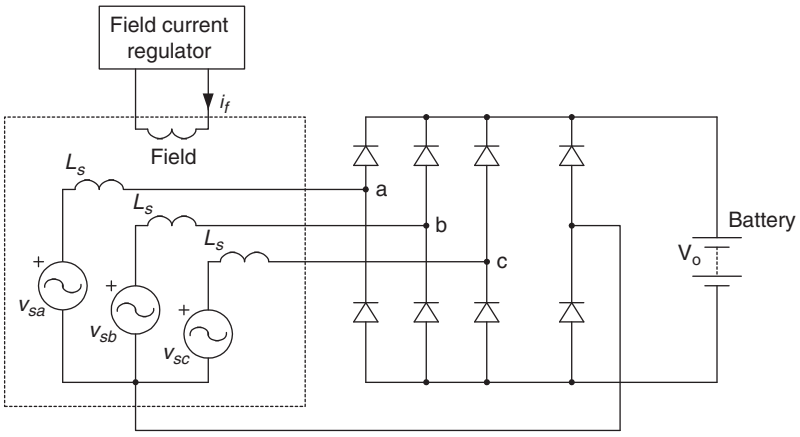


FIG. 32.13 Lundell alternator with booster diodes.

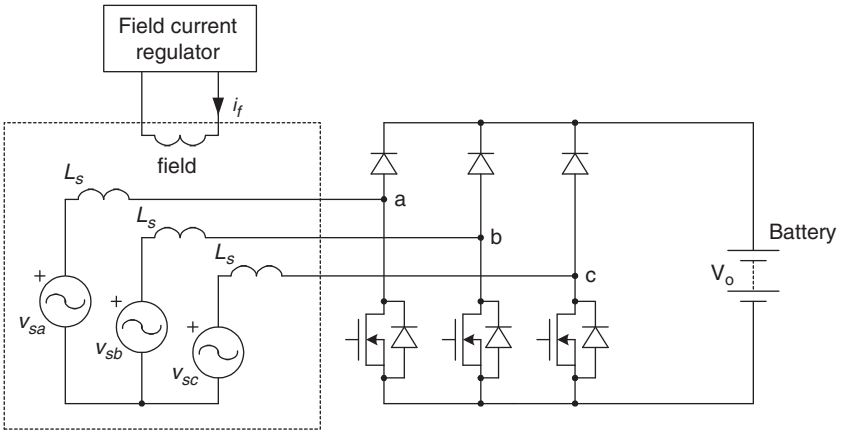


FIG. 32.14 Lundell alternator with a switched-mode rectifier.

on the order of 20% are possible with this technology. Furthermore, the switched-mode rectifier can be employed to achieve greatly improved load-dump transient control.

32.6.3 Alternative Machines and Power Electronics

The demand for increased alternator power levels, efficiency, and performance also motivates the consideration of alternative electric machines, power electronics, and design approaches. While no alternative machine has yet displaced the Lundell alternator in production vehicles, primarily due to cost considerations, some potential candidates are reviewed in this section. These include machines that are mounted directly on the engine rather than driven from a belt. These direct-driven machines become important as power levels rise. This section also addresses the more general case of the combined starter/alternators. While the use of a single machine to do both starting and generation functions is clearly possible, a separate (transient-rated) dc machine is presently used for starting. This is because the large mismatch in starting and generating requirements has made the combined starter/alternator approach unattractive. However, as alternator power ratings increase, the mismatch is reduced, and a single starter/alternator system becomes more practical. A combined system has the potential to eliminate the need for a separate flywheel, starter, solenoid switch, and pinion-engaging drive. It also has the potential to allow regenerative braking and "light hybrid" operation and to provide idle-stop capability (i.e., the ability to turn off the engine when the vehicle is stopped and seamlessly restart when the vehicle needs to move) for reduced fuel consumption. A move to this more sophisticated approach relies upon advanced electric machines and power electronics.

32.6.3.1 Synchronous Machine with a Cylindrical Wound Rotor

The claw-pole rotor can be replaced with a cylindrical rotor to achieve better coupling between the stator and rotor. The cylindrical rotor is made from steel laminations, and the field winding is placed in the rotor slots. The cylindrical rotor is similar to the armature of a dc machine except that the connection of the field winding to the external circuit is made through slip rings instead of a commutator. The cylindrical rotor structure leads to quiet operation and increased output power and efficiency. Unlike the claw-pole alternator, the length of the machine can be increased to get higher output power at a higher efficiency. The efficiency is higher since the effect of the end windings on the machine performance is less in a machine with a long length. It is also possible to build the machine with a salient-pole rotor instead of a cylindrical rotor. However, a machine with a salient-pole rotor is likely to produce more noise than a machine with a cylindrical rotor.

A machine with a cylindrical wound rotor has similar power electronics and control options as a claw-pole machine. If generation-only operation is required, a diode bridge and field current control is sufficient to regulate the output voltage. Better performance can be achieved by using a switched-mode rectifier in conjunction with field control [37]. If motoring operation is desired (e.g., for starting) or even better performance is desired, a full-bridge (active-switch) converter can be used, as shown in Fig. 32.15. Since this is a synchronous machine, some form of rotor position sensing or estimation is typically necessary. The full-bridge converter allows maximum performance and flexibility but carries a significant cost penalty.

32.6.3.2 Induction Machine

The stator of a three-phase induction machine is similar to that of a three-phase synchronous machine. The rotor is either a squirrel-cage or wound rotor. The machine with the squirrel-cage rotor is simpler in construction and more robust than the machine with a wound rotor in which the three-phase rotor winding is brought outside the rotor through slip rings. The rotor is cylindrical and is constructed from steel laminations. It is also possible to use a solid rotor instead of a laminated rotor. However, a solid rotor leads to higher losses as compared with a laminated rotor. The losses in a solid rotor can be

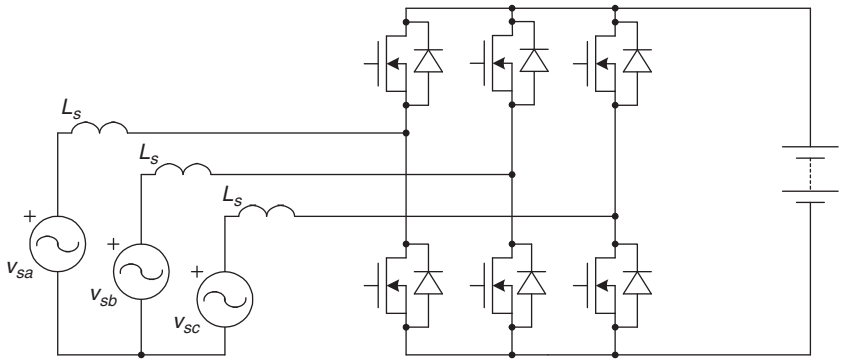


FIG. 32.15 Model of an alternator with full-bridge converter.

reduced by cutting slots in the rotor surface, filling the stator slot openings with magnetic wedges to reduce the field ripple, and placing a copper cage on the rotor.

An induction machine requires a source that can provide the leading reactive power to magnetize the air gap. This means that a three-phase induction generator cannot supply power to a load through a three-phase diode bridge. Capacitor supply of the reactive energy is impractical because of the wide operating speed range. In the most general case (in which both motoring and generating operation can be achieved), a three-phase active bridge can be used. If only generating operation is desired, the power to the load can be supplied through a three-phase diode bridge, and the reactive power can be obtained from a small three-phase active bridge provided for this purpose. This design requires a large number of devices and complex control.

32.6.3.3 Reluctance Machines

The switched reluctance machine is a doubly salient machine. Both the stator and rotor of the machine are made from steel laminations to reduce the iron losses. Only the stator carries windings; the rotor is constructed of steel laminations with a salient shape. The structure of a three-phase switched reluctance machine with six stator poles and four rotor poles is shown in Fig. 32.16A. A winding placed on diametrically opposite stator poles forms a phase winding. When a phase of the machine is excited, a pair of rotor poles tends to align with the excited stator poles to provide a path of minimum reluctance. If the rotor is moving toward alignment with the excited pair of stator poles, then the machine develops a positive torque and acts as a motor. If the rotor is moving away from the excited pair of stator poles, then the machine develops a negative torque and acts as a generator. The advantages of the switched reluctance machine include simple construction, fault-tolerant power electronic circuit, high reliability, unidirectional phase currents, and low cost. The drawbacks of the machine include high levels of torque ripple, vibration and acoustic noise, and a relatively high-power electronic cost.

The synchronous reluctance machine is a singly salient machine. The stator of the machine is similar to that of a synchronous or induction machine. The rotor has a segmented

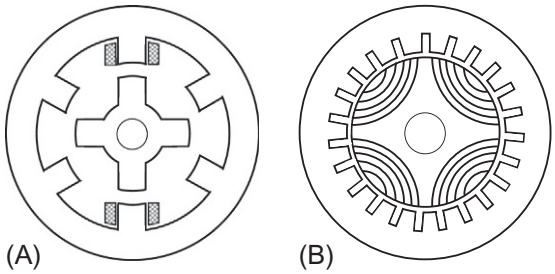


FIG. 32.16 Structures of (A) switched reluctance and (B) synchronous reluctance machines. AA′ represents phase-A winding.

structure with each segment consisting of a stack of axially laminated steel sheets sandwiched with a nonmagnetic material. The structure of a four-pole synchronous reluctance machine is shown in Fig. 32.16B. A synchronous reluctance machine has less torque ripple, lower losses, and higher power density than a comparable switched reluctance machine. Inclusion of permanent magnets in the rotor structure allows both reluctance and magnet torque to be achieved. Such interior permanent-magnet (IPM) machines can achieve very high performance and power density. When permanent magnets are included, however, careful attention must be paid to the effects of shutdown of the power electronics as an uncontrolled back-emf component will exist in this case [41].

The switched reluctance machine, like the induction machine, requires an external source to magnetize the air gap. Several circuits are available to excite the switched reluctance machine. A circuit that is suitable for the automotive application of this machine is shown in Fig. 32.17. A phase leg is needed for each stator phase of the machine. In this case, the switched reluctance machine obtains its excitation from the same bus that it generates into. Unlike the synchronous and induction machines in which the number of wires needed to connect the machines to the power converters is usually equal to the number of phases, the number of wires needed to connect the switched reluctance machine to a converter is equal to twice the number of phases. This is of no particular concern in a switched reluctance machine in which the power converter is integrated with the machine in the same housing. The

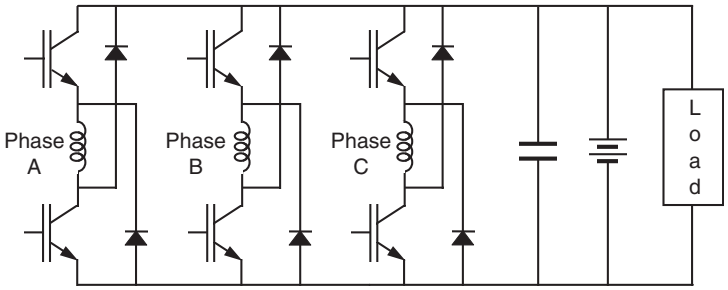


FIG. 32.17 Circuit for a switched reluctance machine.

synchronous reluctance machine also requires an external source to magnetize the air gap. The machine usually employs an active bridge similar to the one used with an induction machine for the desired power conversion. The machine can also employ the converters used with the switched reluctance machine. In this case, the currents through the stator windings are unidirectional. The relative complexity of the power electronics is a disadvantage of these machine types in the case where only generator operation is necessary.

32.6.3.4 Permanent Magnet and Hybrid Synchronous Machines

The permanent-magnet synchronous machine designed with high-energy rare-earth magnets operates with high efficiency, high power density, low rotor inertia, and low acoustic noise. The excitation from the permanent magnets is fixed, and therefore, the regulation of the output voltage of the machine is not as straightforward as in a synchronous machine with a wound rotor. For generator operation, machines of this type can use switched-mode rectifiers to regulate the output voltage [42,43]. The boost rectifier of Fig. 32.14 is one possible implementation of this approach. Alternatively, a diode rectifier followed by a dc/dc converter can be used to regulate the generator system output [44]. Another method proposed for this type of system involves the use of tapped windings and two three-phase SCR bridges [45]. The taps on the phase windings are connected to one bridge, while full-phase windings are connected to the other bridge. The bridge connected to the full-phase windings is used to supply power to the dc bus at low engine speeds, while the converter connected to the taps is used at high speed. The use of a tapped winding and dual bridges helps the system cope with the wide speed range of the alternator and limit the losses associated with the pulsating output currents. In the case when both motoring and generating modes are desired, a full-bridge converter can be used. Again, as this is a synchronous machine, some form of position sensing or estimation is necessary. Also, in all of these systems, the effects of failure of the power electronics must be carefully considered as there is no possibility of regulating the back voltages by field control.

Attempts to develop a simpler voltage regulation scheme for permanent-magnet synchronous machines have led to a permanent-magnet/wound-rotor hybrid synchronous machine in which the rotor consists of two parts, a part with permanent magnets and a part with a field winding [46]. The two parts are placed next to each other on a common shaft. The rotor with the field winding can employ claw-pole, salient-pole, or cylindrical structure. The field current generates a flux that is used to either aid or oppose the permanent-magnet flux and regulate the output voltage of the machine. One possible failure mode of this approach that can lead to catastrophic failure is if the field winding breaks while the machine is operating at high speed. In this case, the generated output voltage will become large and uncontrolled. Some means of mechanically disconnecting the alternator at the input or electrically disconnecting it at the output may be necessary to limit the impact of this failure mode.

32.6.3.5 Axial-airgap Machines

The principle of operation of an axial-air-gap or axial-flux machine is the same as that of a radial-air-gap machine. An axial-air-gap machine is characterized by a short axial length and large diameter. The structure of an axial-air-gap permanent-magnet machine with surface magnets is shown in Fig. 32.18 [47]. The stator of the machine can be slotless or slotted. Two different magnetic circuit configurations are possible. In the NN configuration, the magnetic polarities in one pole pitch on both sides of stator are the same so that there

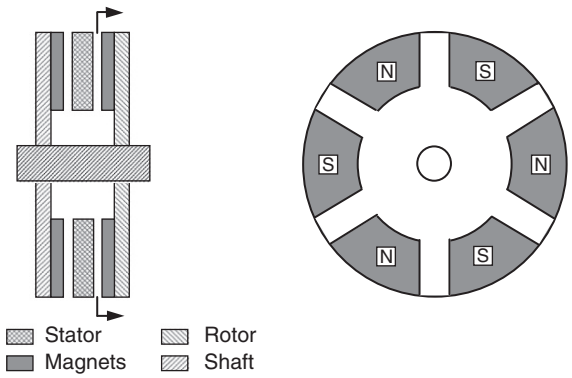


FIG. 32.18 Structure of an axial-air-gap permanent-magnet machine.

are two main fluxes with symmetrical distribution through the stator. In this case, the conductors can be wound into two back-to-back stator slots to make one coil. The machine has a large stator yoke dimension because the flux passes through the yoke but less copper loss because of short end windings. In the NS configuration, the magnetic polarities in one pole pitch on the opposite sides of stator are the opposite of each other so that there is only one main axial flux through the stator. In this case, the stator yoke dimension is small, but the end windings are long because the direction of current in the back-to-back stator slots is the same. The iron losses are small due to small yoke dimension, and the copper losses are high because of long end windings. Heat removal is more challenging due to small stator dimensions. The structure shown in Fig. 32.18 is that of an axial-air-gap permanent-magnet machine with surface magnets. In an axial-air-gap machine with interior permanent magnets, the magnets are embedded in the steel of the rotor.

The axial-air-gap versions of other types of machines, such as the induction and switched reluctance machines, are also possible. The structure of an axial-air-gap induction machine is similar to that of an axial-air-gap permanent-magnet machine except that windings are used instead of permanent magnets.

32.7 Dual/High Voltage Automotive Electrical Systems

The electric system of a 1920s internal-combustion-engine (ICE) automobile had only a few loads: a starter, an ignition device, a horn, and some lamps [48]. The mean power consumption of these loads was less than 100 W. An engine-driven dc generator charged a 6 V lead-acid battery that provided electric power. The power was distributed via point-to-point wiring, with most loads controlled directly by manually operated primary switches located within the reach of the driver. Only the starter was switched indirectly by an electromechanical relay. After the Second World War, the automotive electric system started to grow rapidly in complexity and power consumption as additional features, including radios, multispeed windshield wipers, and power windows, were added. The introduction of higher compression engines stretched the 6 V system beyond its technological limits. The 8.5:1 compression ratio engines required 100%–200% greater ignition voltages than the 6.4:1 engines. As a result, the primary-side current of the ignition coil was doubled or tripled, and the life of the distributor contacts was reduced to an unacceptable level. To overcome this problem, the battery voltage was increased to 12 V in the mid-1950s [49,50].

Over the past four decades, the electric power requirements of automobiles have increased even more rapidly. From a mere 400 W in 1955, the power rating of a luxury vehicle's generator has increased to over 1800 W [51,52]. However, the electric system of a modern automobile is architecturally identical to the 12 V point-to-point system of the 1950s. The only changes that have taken place have been at the component level, such as the replacement of the dc generator by a three-phase alternator-rectifier, the replacement of wound-field dc motors by permanent-magnet ones, and an increased use of relays. The rapid growth in the electric system is expected to continue due to environmental regulations; consumer demand for increased functionality, safety, security, and comfort; and replacement of some mechanical actuators by electric counterparts. The average electric power requirement of a modern luxury vehicle is about 800 W. With the addition of such loads as electric power steering, engine-cooling fan, water pump, and electromechanical engine valves, the average power requirement could increase to 2.5 kW by 2005 [53]. The traditional solution of increasing the size of the alternator and the battery is not practical due to space limitations and fuel efficiency requirements. Furthermore, the peak power requirements of some of the anticipated loads—heated windshield (2.5 kW), heated catalyst (3 kW), electromechanical engine valves (2.4 kW at 3000 rpm), and active suspension (12 kW)—cannot be met economically using the present architecture. These factors have motivated the development of new dual-/high-voltage electric architectures that incorporate a higher-voltage bus in addition to the standard 14 V bus [39,54–56]. A dual-/high-voltage approach allows an efficient supply of power to many loads that benefit from operating at a higher voltage while retaining the 14 V bus for loads (such as lamps and electronics) that do not benefit from a higher voltage. High-voltage architectures that do not retain the 14 V bus are also possible but will require a substantial investment in the design and production of new high-voltage components. This section describes some of the characteristics and preliminary specifications of the new dual-/high-voltage electric system architectures. It also discusses some of the widely considered implementation approaches.

32.7.1 Trends Driving System Evolution

The conventional 12 V automotive electric power system has many defects, including a widely varying steady-state system voltage and large transients, which force the electric functions to be overdesigned. However, these limitations alone have not been a strong enough driver for automotive companies to seriously evaluate advanced alternatives. Now, a number of new factors are changing this situation. The most important of these are future load requirements that cannot be met by the present 12 V architecture.

32.7.1.1 Future Load Requirements

Table 32.6 gives a list of electric loads expected to be introduced into automobiles in the next 10 years [53]. Some of these loads (electrohydraulic power steering, electric engine fan, electric water pump, and electromechanical valves) will replace existing

TABLE 32.6 Electric loads expected to be introduced into automobiles in the next decade [53]

Load	Peak power (W)	Average power (W)
Exhaust air pump	300	10
Electrohydraulic power steering	1000	150
Electric engine fan	800	150
Heated catalytic converter	3000	90
Electric water pump	300	150
Heated windshield	2500	120
Electromechanical engine valves (six cylinders at 6000 rpm)	2400	800
Active suspension	12,000	360
Total		1830

mechanically or hydraulically driven loads. The remaining are new loads introduced to either meet government mandates or satisfy customer needs.

The average electric power requirement of a present-day automobile is in the range of 500–900 W depending on whether it is an entry-level or a luxury vehicle. When the loads of Table 32.6 are introduced, the average electric power requirement will increase by 1.8 kW. Furthermore, if the air-conditioning (A/C) pump was to ever become electrically driven, the peak and average power demands would increase by an additional 3.5 and 1.5 kW, respectively. Distributing such high power at a relatively low voltage will result in unacceptably bulky wiring harnesses and large distribution losses. Since the alternator has to generate both the power consumed by the loads and the power dissipated in the distribution network, its output rating (and hence size and power consumption) will be greater than in an architecture with lower distribution losses. With the large premium attached to the size of the alternator (due to space constraints in the engine compartment), an architectural change in the distribution and generation systems is essential before many of the future loads can be introduced.

There is also an increasing disparity in the voltage requirements of future electric loads. High-pulse-power loads, such as the heated windshield and electrically heated catalytic converter, become feasible only at voltages greater than the current 14 V [57]. On the other hand, incandescent lamps and electronic control units (ECUs) will continue to require low voltages. For example, present-day ECUs have linear regulators that convert the 14 V distribution voltage to the 5 V needed by the integrated circuits. The efficiency of these regulators is equal to the ratio of output to input voltage, that is, 35%. Furthermore, the next generation of higher speed lower power consumption integrated circuits operates at 3.3 V, making the regulators more inefficient. This inefficiency also means that larger heat sinks are required to remove the heat from the ECUs.

32.7.1.2 Higher Fuel Efficiency

A secondary motivating factor for the introduction of a higher system voltage is the challenge of achieving higher fuel economy. The average fuel economy of present-day automobiles in the United States is in the vicinity of 30 mpg. There is little market incentive for automobile manufacturers to increase the fuel economy of vehicles for the US market where the price of fuel is relatively low. The price of gasoline in the United States ($1.70 per gallon) is less than the price of bottled water ($4.00 per gallon when bought by the quart). Although market forces have not been a driver for the development of fuel-efficient vehicles, a number of new incentives have emerged over the past few years. One of these is the fine imposed on the automakers by the US government if the average fuel economy of their fleet falls below the mandated standard. The mandated standard for cars has increased from 24 mpg in 1982 to its 1997 level of 27.5 mpg and will continue to increase. In Europe, the German Automotive Industry Association (VDA) plans to increase the average fleet fuel efficiency to 39.9 mpg by 2005—compared with 31.4 mpg in 1990 [58].

Another driver behind the development of fuel-efficient vehicles is the partnership for a new generation of vehicles (PNGV). This 10-year research program, launched in September 1993, is a collaboration between the US Federal Government and the big three US automakers (General Motors, Ford, and DaimlerChrysler) that aims to strengthen national competitiveness in the automotive industry and reduce dependence on foreign oil. The PNGV has set a goal to develop an 80 mpg midsize vehicle by 2004 [59]. The German Automotive Industry Association is pursuing similar targets. The VDA has undertaken a pledge to introduce a 3 L/100 km (78 mpg) vehicle by the year 2000. This is complemented by the introduction of highly fuel-efficient vehicles (in excess of 50 mpg) in both the Japanese and American markets.

With the present alternator, 800 W of electric power consumes 1.33 L of gasoline for every 100 km driven when the vehicle has an average speed of 33.7 km/h. This represents a 45% increase in fuel consumption for a 3 L/100 km vehicle. Hence, if future high-fuel-economy vehicles are going to have comfort, convenience, and safety features comparable with present-day vehicles, the efficiency of the electric generation and distribution system will have to be substantially improved. Furthermore, as discussed in Section 32.8, one widely considered means of achieving high fuel economy is the use of a hybrid vehicle architecture. In practice, this approach necessitates the introduction of a higher voltage in the vehicle.

32.7.2 Voltage Specifications

A major issue when implementing a high- or dual-voltage system is the nominal voltage of the high-voltage bus and the

TABLE 32.7 Voltage limits for 14 and 42 V buses proposed in Ref. [56]

Voltage	Description	Value
$V_{42,OV-dyn}$	Maximum dynamic overvoltage on 42 V bus during fault conditions	55 V
$V_{42,OV-stat}$	Maximum static overvoltage on 42 V bus	52 V
$V_{42,E-max}$	Maximum operating voltage of 42 V bus while engine is running	43 V
$V_{42,E-nom}$	Nominal operating voltage of 42 V bus while engine is running	41.4 V
$V_{42,E-min}$	Minimum operating voltage of 42 V bus while engine is running	33 V
$V_{42,OP-min}$	Minimum operating voltage on the 42 V bus. Also, lower-limit operating voltage for all noncritical loads (i.e., loads not required for starting and safety)	33 V
$V_{42,FS}$	Fail-safe minimum voltage—lower limit on operating voltage for all loads critical to starting and safety on the 42 V bus	25 V
$V_{14,OV-dyn}$	Maximum dynamic overvoltage on 14 V bus during fault conditions	20 V
$V_{14,OV-stat}$	Maximum static overvoltage on 14 V bus	16 V
$V_{14,E-max}$	Maximum operating voltage of 14 V bus while engine is running	14.3 V
$V_{14,E-nom}$	Nominal operating voltage of 14 V bus while engine is running	13.8 V
$V_{14,E-min}$	Minimum operating voltage of 14 V bus while engine is running	12 V
$V_{14,OP-min}$	Minimum operating voltage of 14 V bus. Also lower-limit operating voltage for all noncritical loads	11 V
$V_{14,FS}$	Fail-safe minimum voltage—lower limit on operating voltage for all critical loads on the 14 V bus	9 V

operating limits of both buses. While there are many possibilities, there is a growing consensus in the automotive industry for a nominal voltage of 42 V for the high-voltage bus (corresponding to a 36 V lead-acid storage battery) [39,56,60]. This voltage is gaining acceptance because it is as high as possible while remaining within acceptable safety limits for open wiring systems (once headroom is added for transients) and it provides substantial benefits in the power semiconductors and wiring harness [61]. Furthermore, this voltage is sufficient to implement starter/alternator systems and "light" hybrid vehicle designs [62,63]. While no vehicles equipped at 42 V are in production at present, availability of 42 V components is rapidly increasing, and 42 V equipped vehicles may be expected early in this decade.

The permissible static and transient voltage ranges in an electric system are important design considerations for power electronic equipment. At present, no universally accepted specification exists for high- or dual-voltage automotive electric systems. However, the preliminary specifications proposed by the European automotive working group, *Forum Bordnetz*, are under wide consideration by the automotive industry [56]. These specifications, summarized in Table 32.7, impose tight static and transient limits on both the 42 and 14 V buses. The upper voltage limit on the 14 V bus is far lower than in the conventional 12 V system. The allowed upper limit on the 42 V bus is also proportionally tight. These strict limits facilitate the use of power semiconductor devices such as power MOSFETs and lower the cost of the protection circuitry needed in individual functions. However, they also require much more sophisticated means for limiting transients (such as load dump) than is found in conventional systems, which imposes a significant cost. Appropriate voltage range specifications for dual-/high-voltage electric systems are thus a subject of ongoing investigation by vehicle manufacturers and will likely continue to evolve for some time.

32.7.3 Dual-Voltage Architectures

Conventional automotive electric systems have a single alternator and battery. Dual-voltage electric systems have two voltage buses and typically two batteries. Single-battery configurations are possible but tend to be less cost-effective [61]. A variety of different methods for generating and supplying energy to the two buses are under investigation in the automotive community. Many of these have power electronic circuits at their core. This section describes three dual-voltage electric system architectures that have received broad attention. In all three cases, the loads are assumed to be partitioned between the two buses with the starter and many of the other high-power loads on the 42 V bus and most of the lamps and electronics on the 14 V bus.

The dc/dc converter-based implementation of Fig. 32.19 is perhaps the most widely considered dual-voltage architecture. In this implementation, an alternator and associated battery provide energy to one bus (typically the 42 V bus), while the other bus is supplied via a dc/dc converter. If a battery is used at the dc/dc converter output, the converter needs to be rated for slightly above average power. Otherwise, the converter needs to be rated a factor of two to three higher to meet peak power requirements [61]. The architecture of Fig. 32.19 has a

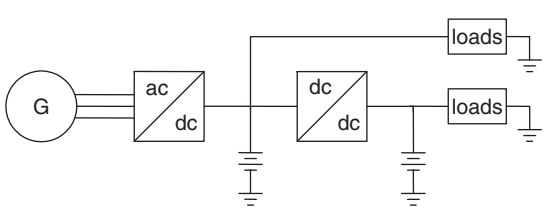


FIG. 32.19 Dual-voltage architecture based on a dc/dc converter.

number of advantages. The dc/dc converter provides high-bandwidth control of energy flow between the two buses, thus enabling better transient control on the 14 V bus than is available in present-day systems or in most other dual-voltage architectures. Furthermore, in systems with batteries on both buses, the dc/dc converter can be used to implement an energy management system so that generated energy is always put to best use. If the converter is bidirectional, it can even be used to recharge the high-voltage (starter) battery from the low-voltage battery, thus providing a *self-jump-start* capability. The major challenge presented by this architecture is the implementation of dc/dc converters having the proper functionality within the tight cost constraints dictated by the automotive industry. Some aspects of design and optimization of converters for this application are addressed in Ref. [64].

The dual-stator alternator architecture of Fig. 32.20 is also often considered for dual-voltage automotive electric systems [65,66]. In this case, an alternator with two armature windings is used along with two rectifiers to provide energy to the buses and their respective batteries. Control of the bus voltages is achieved via a combination of controlled rectification and field control. Typically, field control is used to regulate one output, while the other output is regulated using a controlled rectifier. Fig. 32.21 shows one possible implementation of this architecture. It should be noted that to achieve sufficient output power and power steering from the dual-wound alternator, the winding ratio between the two outputs must be carefully selected. For 42/14 V systems, a winding ratio of 2.5:1 is typical [66]. Advantages of this electric architecture include low cost. However, it does not provide the bidirectional energy control that is possible in the dc/dc converter architecture. Furthermore, there are substantial issues of cross regulation and transient control with this architecture that remain to be fully explored.

In a third architecture, a single-output alternator with a dual-output rectifier is employed. This approach is shown schematically in Fig. 32.22. As with the dual-stator alternator configuration, this architecture has the potential for low cost. One widely considered implementation of the dual-rectified alternator is shown in Fig. 32.23 [65,67–69]. Despite its simplicity, this implementation approach provides less functionality than the dc/dc converter-based architecture, generates substantial low-frequency ripple that must be filtered, and has serious output power and control limitations [66]. An alternative implementation, proposed in Ref. [37] and shown in Fig. 32.24, seems to overcome these limitations and may potentially provide the same capabilities as the dc/dc converter-based architecture at lower cost. Clearly, this architecture has promise for dual-voltage electric systems but remains to be fully explored.

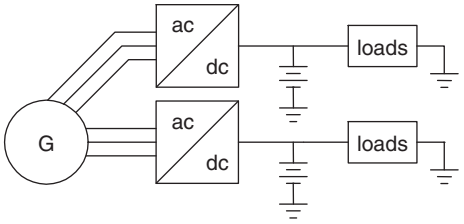


FIG. 32.20 Dual-voltage architecture based on a dual-wound alternator.

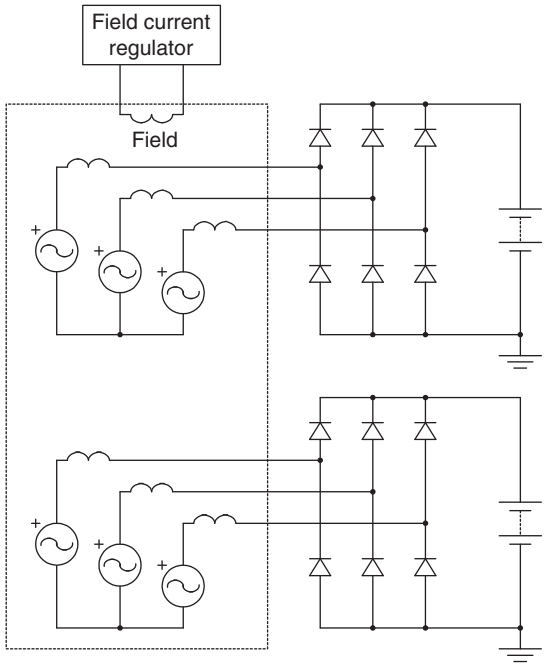


FIG. 32.21 Model for a dual-wound alternator system. The two output voltages are regulated through field control and phase control. For a 42/14 V system, a winding ratio between the two stator windings of 2.5:1 is typical.

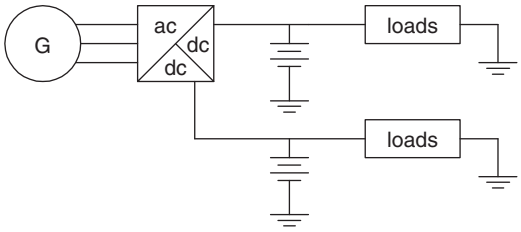


FIG. 32.22 Dual-voltage architecture based on a dual-rectified alternator.

32.8 Electric and Hybrid Electric Vehicles

Battery-powered electric vehicles were first introduced over 100 years ago and continue to incite great public interest because they do not generate tailpipe emissions. Nevertheless, the low-energy-storage density and the high cost of suitable

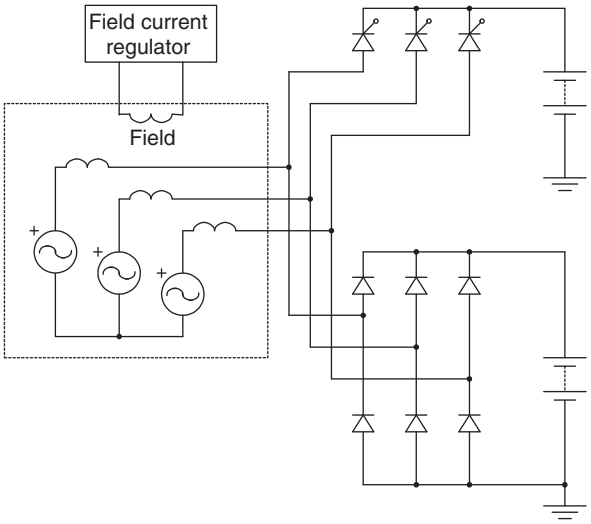


FIG. 32.23 A dual-rectified alternator with a phase-controlled rectifier.

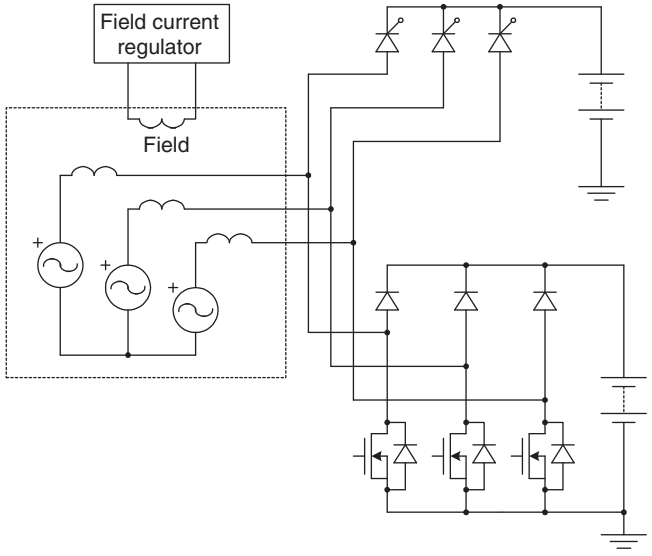


FIG. 32.24 A dual-rectified alternator with a switched-mode rectifier.

batteries make pure electric vehicles noncompetitive with internal-combustion-engine vehicles in most applications. An alternative approach that is generating widespread attention is HEV. An HEV combines electric propulsion with another energy source, such as an internal combustion engine, allowing the traditional range and performance limitations of pure electric vehicles to be overcome [70]. Alternative energy sources, such as fuel cells, are also possible in place of an internal combustion engine.

HEVs can be classified as having either a parallel or series driveline configuration [71]. In a series HEV, all of the propulsion force is produced from electricity; the engine is only used to drive a generator to produce electricity. In a parallel hybrid, propulsive force can come from either the engine or the electric drive. In both cases, batteries or other electric storage devices are used to buffer the instantaneous difference between the power needed for propulsion and that generated by the engine. The selection of a series or parallel driveline depends heavily on the performance requirements and mission of the vehicle.

In a series HEV, all power delivered to the wheels of the vehicle must be delivered through the electric driveline. The electric driveline components, including the batteries, power electronics, and machine(s), must all be rated for the *peak* traction power requirements, making these components relatively large and expensive if performance (e.g., acceleration) comparable with a conventional vehicle is to be achieved. To achieve the required power levels, the electric driveline must operate at hundreds of volts, necessitating the electric subsystem to be sealed from access by the user. The engine, on the other hand, needs only be rated to deliver the *average* power required by the vehicle, which is much lower. In a system that does not require utility recharge of the batteries (i.e., can drive indefinitely on fuel alone), the engine size is set by the power requirements of the vehicle at maximum cruising speed. If utility recharge of the batteries and a battery-limited driving range is acceptable, engine power requirements can be reduced even further. Because the engine does not provide tractive power, it can be designed to run at a single optimized condition, thus maximizing engine efficiency and minimizing emissions. Furthermore, the need for a transmission is eliminated, and there is a great deal of flexibility in the engine placement.

In a parallel HEV, traction power is split between the engine and the electric driveline. One possible approach is to utilize a single machine mounted on the engine crankshaft to provide starting capability along with electric traction power and regeneration [72–75]. This approach can be replaced or complemented with other approaches, such as using of a power-splitting device such as a planetary gear set [70,76] or using different propulsion and generation techniques on different sets of wheels [71,77,78]. In all parallel hybrid approaches, some form of transmission is needed to limit the required speed range of the engine. A wide range of divisions between engine size and electric system size is possible in the parallel hybrid case, depending on structure. Depending on this split, the necessary electric driveline system voltage may be as low as 42 V (which is safe for an open wiring system) or as high as 300 V. Also because the electric subsystem, the internal-combustion-engine subsystem, or both may provide tractive power under different conditions, there exist a wide range of possible operating approaches for a parallel hybrid system. Consequently, the control strategy for a parallel hybrid tends to be substantially more complex than for a series hybrid.

One parallel hybrid approach that is receiving a lot of attention for near-term vehicles is a “light” or “mild” hybrid. In this case, a somewhat conventional vehicle driveline is complemented with a relatively small starter/alternator machine mounted on the crankshaft [62,63,72–75,79]. The electric drive power is

typically below 10 kW average and 20 kW peak. The starter/alternator can be used to provide rapid, clean restart of the vehicle so that the engine can be turned off at idling conditions and seamlessly restarted. This so-called stop-and-go operation of the engine is valuable for fuel economy and emissions. The starter/alternator can also be used to implement regenerative braking, to provide engine torque smoothing (replacing the flywheel and allowing different engine configurations to be used) and to provide boost power for short-term acceleration. At the low-power end, such systems can be integrated directly into the open wiring configuration of a 42 V electric system, simplifying the vehicle electric architecture. System-level control remains a major challenge in realizing the full benefits of such systems. Starter-/alternator-based hybrids are expected to be a significant near-term application of power electronics and machines in automobiles.

The increasing electric and electronic content of automobiles is beginning to stretch the capabilities of the conventional 12 V electric system. Furthermore, there is a desire on the part of vehicle manufacturers to introduce new high-power loads, such as electromechanical engine valves, active suspension, and integrated starter/alternator. These are not likely to be practical within the present 12 V framework. These challenges are forcing the automotive industry to seriously consider high- and dual-voltage electric systems. The ongoing developments in this area were reviewed in Section 32.7

The increasing electric content of vehicles both underscores the need for power electronics and reflects the benefits of their introduction. It is safe to say that power electronics will continue to play an important role in the evolution of automobiles far into the future.

32.9 Summary

Power electronics is playing an increasingly important role in automobiles. It is being used to enhance the output power capability and efficiency of the electric power generation components. Power electronics is also an enabling technology for a wide range of new and improved functions that enhance vehicle performance, safety, and functionality.

The design of automotive power electronic systems is strongly influenced by the challenging electric and environmental conditions found in automobiles. Important factors include the static and transient voltage ranges, electromagnetic interference and compatibility requirements, and temperature and other environmental conditions. Some of the most important design considerations for automotive power electronics were addressed in Section 32.3.

Section 32.4 described some of the vehicle functions that benefit from or are enabled by power electronics. These functions range from lighting to actuation and steering. Power electronic switches also play a central role in multiplexed electric distribution systems. This role of power electronics was addressed in Section 32.5.

The rapid increase in electric power demand in automobiles is motivating the introduction of new technologies for electric power generation and control. Lundell alternators are presently used for power generation in automobiles but are rapidly reaching their power limits. Section 32.6 reviewed the operating characteristics of the Lundell alternator. It also described several techniques for extending the power capabilities of this machine. Meeting the growing demand for electric power, alternative machine, and power electronic configurations may be necessary in the future. A number of candidate machine and power circuit configurations were reviewed in Section 32.6. Such configurations can also be applied toward the design of integrated starter/alternators and hybrid propulsion systems, as was discussed in Section 32.8.

References

[1] Automotive Electric/Electronic Systems, second ed., Robert Bosch GmbH, Stuttgart, Germany, 1995.
[2] T. Denton, Automotive Electrical and Electronic Systems, Arnold, London, UK, 1995.
[3] SAE Electronic Systems Committee, Recommended Environmental Practices for Electronic Equipment Design, SAE Recommended Practice SAE J1211, November 1978.
[4] S.A.E. Handbook, Society of Automotive Engineers, Warrendale, PA, USA, 1999.
[5] J. Alkalay, et al., Survey of conducted transients in the electrical system of a passenger automobile, in: IEEE Symposium on Electromagnetic Compatibility, 1989, pp. 271–278.
[6] SAE EMI Standards Committee, Immunity to Conducted Transients on Power Leads, SAE Standard SAE J1113/11, June 1995.
[7] J.G. Kassakian, M.F. Schlecht, G.C. Verghese, Principles of Power Electronics, Addison-Wesley, New York, 1991.
[8] V. Caliskan, D.J. Perreault, T.M. Jahns, J.G. Kassakian, Analysis of three-phase rectifiers with constant-voltage loads, in: IEEE Power Electronics Specialists Conference, Charleston, SC, USA, 1999, pp. 715–720.
[9] SAE EMI Standards Committee, Limits and Methods of Measurement of Radio Disturbance Characteristics of Components and Modules for the Protection of Receivers Used On Board Vehicles, SAE Standard SAE J1113/41, July 1995.
[10] SAE EMI Test Methods and Standards Committee, Electromagnetic Compatibility—Component Test Procedure—Part 42–Conducted Transient Emissions, SAE Standard SAE J1113/42, July 1994.
[11] T.K. Phelps, W.S. Tate, Optimizing passive input filter design, in: Proceedings of Powercon 6, 1979. G1–1–G1-10.
[12] M.J. Nave, Power Line Filter Design for Switched-Mode Power Supplies, Van Nostrand Reinhold, New York, 1991.
[13] R.D. Middlebrook, Input filter considerations in design and application of switching regulators, in: IEEE Industry Applications Society Annual Meeting, 1976.
[14] H.W. Ott, Noise Reduction Techniques in Electronic Systems, John Wiley, New York, 1988.
[15] Automotive Handbook, third ed., Robert Bosch GmbH, Stuttgart, Germany, 1993.

[16] R.K. Jurgen (Ed.), Automotive Electronics Handbook, second ed., McGraw Hill, New York, 1999.
[17] F.S. Schwartz, W. Hendrischk, J. Jiao, Intelligent automotive lighting, in: Proceedings of International Congress on Transportation Electronics, Dearborn, MI, USA, 1994, pp. 299–303.
[18] T. Yamamoto, T. Futami, Development of 2-lamp type HID headlighting system, in: SAE paper 900562, Proceedings of the SAE International Congress and Exposition, Detroit, MI, USA, 1990, pp. 1–6.
[19] B. Woerner, R. Neumann, Motor vehicle lighting systems with high intensity discharge lamps, in: Proceedings of the SAE International Congress and Exposition, Detroit, MI, USA, 1990, pp. 87–94.
[20] L. So, P. Miller, M. O'Hara, 42 V-PWM—lighting the way in the new millennium, in: SAE paper 2000-01-3053, Future Transportation Technology Conference, Costa Mesa, CA, USA, 2000.
[21] H.P. Schoner, Piezo-electric motors and their applications, Ferroelectrics 133 (1992) 27–34.
[22] J. Wallaschek, Piezoelectric ultrasonic motors, J. Intell. Mater. Syst. Struct. 6 (1995) 71–83.
[23] T. Sashida, T. Kenjo, An introduction to ultrasonic motors, Oxford University Press, New York, 1993.
[24] T. Sashida, Japanese Patent No. 58-148682, February 1982.
[25] M.A. Theobald, B. Lequesne, R. Henry, Control of engine load via electromagnetic valve actuators, in: International Congress and Exposition, SAE Paper 920447, Detroit, MI, USA, 1994.
[26] J.L. Oldenkamp, D.M. Erdman, Automotive electrically driven air conditioner system, in: Proceedings of the IEEE Workshop on Automotive Power Electronics, 1989, pp. 71–72.
[27] R.J. Valentine, Electric steering power electronics, in: IEEE Workshop on Power Electronics in Transportation, Dearborn MI, USA, 1996, pp. 105–110.
[28] J.F. Ziomek, One-wire automotive electrical systems, in: SAE Paper 730132, Proceedings of the SAE International Automotive Engineering Congress, Detroit, MI, USA, 1973.
[29] M. Leonard, Multiplexed buses unravel auto wiring, Electron. Des. (1991) 83–90.
[30] Class B Data Communication Network Interface, SAE J1850, Rev. Aug 91, Society of Automotive Engineers, Warrendale, PA, USA, 1992.
[31] CAN Specification, Robert Bosch GmbH, Stuttgart, Germany, 1991.
[32] R. Frank, Replacing relays with semiconductor devices in automotive applications, in: SAE Paper 880177, 1988, pp. 47–53.
[33] A. Marshall, K.G. Buss, Automotive semiconductor switch technologies, in: Proceedings of IEEE Workshop on Electronic Applications in Transportation, Dearborn, MI, USA, 1990, pp. 68–72.
[34] F. Krieg, Automotive relays, Automot. Eng. 3 (1993) 21–23.
[35] K. Furuichi, K. Ishida, K. Enomoto, K. Akashi, An implementation of class A multiplex application, in: SAE Paper 920230, SAE International Congress and Exposition, Multiplex Technology Applications to Vehicle Wire Harnesses, Detroit, MI, USA, 1992, pp. 125–133.
[36] S. Kuppers, G. Henneberger, Numerical procedures for the calculation and design of automotive alternators, IEEE Trans. Magn. 33 (2) (1997) 2022–2025.
[37] D. Perreault, V. Caliskan, A new design for automotive alternators, in: SAE Paper 2000-01-C084, IEEE-SAE International Conference on Transportation Electronics (Convergence), Dearborn, MI, USA, 2000.
[38] G. Henneberger, S. Kuppers, Improvement of the output performance of claw-pole alternators by additional permanent magnets, in: Proceedings of the International Conference on Electrical Machines, vol. 2, 1994, pp. 472–476.
[39] J.M. Miller, D. Goel, D. Kaminski, H.-P. Shoener, T.M. Jahns, Making the case for a next generation automotive electrical system, in: International Congress on Transportation Electronics (Convergence), Dearborn, MI, USA, 1998, pp. 41–51.
[40] T.A. Radomski, Alternating current generator, U.S. Patent No. 4,882,515, November 21, 1989.
[41] T.M. Jahns, V. Caliskan, Uncontrolled generator operation of interior PM synchronous machines following high-speed inverter shutdown, IEEE Trans. Ind. Appl. 35 (6) (1999) 1347–1357.
[42] G. Venkataramanan, B. Milovska, V. Gerez, H. Nehrir, Variable speed operation of permanent magnet alternator wind turbines using a single switch power converter, J. Solar Energy Eng. Trans. ASME 118 (4) (1996) 235–238.
[43] W.T. Balogh, Boost converter regulated alternator, U.S. Patent No. 5,793,625, August 11, 1998.
[44] H.-J. Gutt, J. Muller, New aspects for developing and optimizing modern motorcar generators, in: IEEE Industry Applications Society Annual Meeting, Denver, CO, USA, 1994.
[45] M. Naidu, N. Boules, R. Henry, A high-efficiency, high power generation system for automobiles, in: Industry Applications Conference, 1995. Thirtieth IAS Annual Meeting, IAS '95, Conference Record of the 1995 IEEE, Orlando, FL, USA, 1995, pp. 709–716.
[46] C.D. Syverson, W.P. Curtiss, Hybrid alternator with voltage regulator, U.S. Patent No. 5,502,368, March 26, 1996.
[47] Z. Zhang, F. Profumo, A. Tenconi, Wheels axial flux machines for electric vehicle applications, in: Proceedings of the International Conference on Electrical Machines, vol. 2, 1994, pp. 7–12.
[48] L. Givens, A technical history of the automobile, Automot. Eng. (1990) 61–67.
[49] S.M. Terry, 12 volts presents its case, SAE J. (1954) 29–30.
[50] H.L. Hartzell, It's still 12 Volts!, SAE J. (1954) 63.
[51] J.G.W. West, Powering up—a higher system voltage for cars, IEE Rev. 35 (1) (1989) 29–32.
[52] J.M. Miller, Multiple voltage electrical power distribution system for automotive applications, in: Intersociety Energy Conversion Engineering Conference, Washington, DC, USA, 1996.
[53] J.G. Kassakian, H.C. Wolf, J.M. Miller, C.J. Hurton, Automotive Electrical Systems circa 2005, IEEE Spectr. 33 (8) (1996) 22–27.
[54] J.V. Hellmann, R.J. Sandel, Dual/high voltage electrical systems, in: Future Transportation Technology Conference and Exhibition, SAE 911652, 1991.
[55] SAE J2232, Vehicle System Voltage—Initial Recommendations, SAE Information Report J2232, June 1992.
[56] Draft Specification of a Dual Voltage Vehicle Electrical Power System 42 V/14 V, Forum Bordnetz, Working Document, Germany, March 4, 1997.
[57] Heated Windshield, PPG Industries Inc., Pittsburg, PA, USA.
[58] Automotive Industry Association Expects Production of Fuel-Efficient Cars to Begin by 2000, The Week in Germany, pp. 4, German Information Center, New York, NY, USA, 15 September 1995.
[59] Review of the Research Program of the Partnership for a New Generation of Vehicles, Second Report, National Academy Press, Washington, DC, USA, 1996.
[60] MIT Prof Drives the Shift to 42-V Cars, Electronic Engineering Times, Issue 1053, pp. 115–116, March 22, 1999.
[61] K.K. Afridi, A Methodology for the Design and Evaluation of Advanced Automotive Electrical Power Systems, PhD Thesis, Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA, USA, February 1999.

[62] J.M. Miller, K. Hampton, R. Eriksson, Identification of the optimum vehicle class for the application of 42 V integrated starter generator, in: SAE Paper 2000-01-C073, IEEE-SAE International Conference on Transportation Electronics (Convergence), Dearborn, MI, 2000.
[63] E.C. Lovelace, T.M. Jahns, J.H. Lang, Impact of saturation and inverter cost on interior PM synchronous machine drive optimization, IEEE Trans. IAS 36 (3) (2000).
[64] T.C. Neugebauer, D.J. Perreault, Computer-aided optimization of dc/dc converters for automotive applications, in: IEEE Power Electronics Specialists Conference, Galway, Ireland, 2000, pp. 689–695.
[65] J.C. Byrum, Comparative Evaluation of Dual-Voltage Automotive Alternators, S.M. Thesis, Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA, USA, September 2000.
[66] V. Caliskan, A Dual/High-Voltage Automotive Electrical Power System with Superior Transient Performance, Ph.D. Thesis, Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA, USA, September 2000.
[67] C.R. Smith, Review of heavy duty dual voltage systems, in: International Off-Highway & Powerplant Congress and Exposition, SAE Paper 911857, 1991.
[68] J. Becker, M. Pourkermani, E. Saraie, Dual-voltage alternators, in: International Truck and Bus Meeting and Exposition, SAE Paper 922488, Toledo, Ohio, USA, 1992.
[69] J. O'Dwyer, C. Patterson, T. Reibe, Dual voltage alternator, in: IEE Colloquium on Machines for Automotive Applications, London, UK, 1996, pp. 4/1–4/5.
[70] D. Hermance, S. Sasaki, Hybrid electric vehicles take to the streets, IEEE Spectr. 35 (11) (1998) 48–52.
[71] A.F. Burke, Hybrid/electric vehicle design options and evaluations, in: Electric and Hybrid Vehicle Technology (SP-915) International Congress and Exposition, SAE Paper 920447, Detroit, MI, USA, 1992.
[72] K. Nakano, S. Ochiai, Development of the motor assist system for the hybrid automobile—the insight, in: IEEE-SAE International Conference on Transportation Electronics (Convergence), SAE Paper 2000-01-C079, Dearborn, MI, USA, 2000.
[73] R.L. Davis, T.L. Kizer, et al., Energy management in DaimlerChrysler's PNGV concept vehicle, in: IEEE-SAE International Conference on Transportation Electronics (Convergence), SAE Paper 2000-01-C063, Dearborn, MI, USA, 2000.
[74] A. Gale, D. Brigham, Starter/alternator design for optimized hybrid fuel economy, in: IEEE-SAE International Conference on Transportation Electronics (Convergence), SAE Paper 2000-01-C061, Dearborn, MI, USA, 2000.
[75] J.M. Miller, A.R. Gale, V.A. Sankaran, Electric drive subsystem for a low-storage requirement hybrid electric vehicle, IEEE Trans. Veh. Technol. 48 (6) (1999).
[76] S. Abe, Development of the hybrid vehicle and its future expectation, in: IEEE-SAE International Conference on Transportation Electronics (Convergence), SAE Paper 2000-01-C042, Dearborn, MI, USA, 2000.
[77] W.L. Shepard, G.M. Claypole, M.G. Kosowski, R.E. York, Architecture for robust efficiency: GM's 'Precept' PNGV vehicle, in: Future Car Congress, SAE Paper 2000-01-1582, Arlington, VA, USA, 2000.
[78] M.G. Kosowski, P.H. Desai, A parallel hybrid traction system for GM's precept PNGV vehicle, in: Future Car Congress, SAE Paper 2000-01-1534, Arlington, VA, USA, 2000.
[79] J.M. Miller, A.R. Gale, P.J. McCleer, F. Lonardi, J.H. Lang, Starter alternator for hybrid electric vehicle: comparison of induction and variable reluctance machines and drives, in: IEEE IAS Annual Meeting, St. Louis, MO, USA, 1998.

33

Fuel-Cell Systems for Transportations

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33.1 Introduction

Recently, energy-related concerns have been increasing in terms of many subtopics such as environmental sustainability, population growth, energy independence, energy security, and political imbalance between developed/developing countries. Among these hot topics, environmental sustainability is a major issue as the conventional fossil-fuel-consumption-based energy production results in significant increase in the global greenhouse gas (GHG) emissions, which in turn may cause global warming [1,2]. Many developed/developing countries have set future targets for reduction in GHG emissions for meeting the targets provided by Kyoto Protocol, Paris Climate Conference (COP21, in Dec. 2015), and European Union 2020 perspective. Thus, due to the existing drawbacks of conventional energy sources, utilization has led to the development of new, cleaner energy-based technologies in different areas, such as transportation and power generation. Among these application areas, special emphasis has been given on the development of a new generation of environment-friendly vehicular systems because of their potential to offer reduced emissions in the transportation sector and to reduce the dependence of many countries on imported fuel [3,4]. The automotive industry is one of the largest global industries, and there are around 1 billion vehicles in use. This sector generates a value of more than $3 trillion per year while enabling the employment of nearly 10 million people [5]. In this regard, the transportation sector plays a crucial and growing role in the world energy use, and it is responsible for approximately 15%–20% of overall GHG emissions [1,5]. The abovementioned factors generated renewed interest in the development of alternative vehicle technologies.

In particular, the efforts for technological improvements and innovation in transport and various electrically driven vehicles (EDVs) have been developed by important vehicular system manufacturers around the world supported by public authorities, nonprofit organizations, researchers, and many private companies promoting sustainable development [1,4,6]. EDVs have significant potential for widespread use in the future, which may include battery-based electric vehicles (BEVs), fuel-cell-powered electric vehicles (FCEVs), hydrogen fuel-cell plug-in hybrid vehicles, or plug-in hybrid electric vehicles (PHEVs) [1].

Many studies in the literature are dedicated to examining the economic and environmental impacts of different EDV technologies, which are based on case studies for different places.

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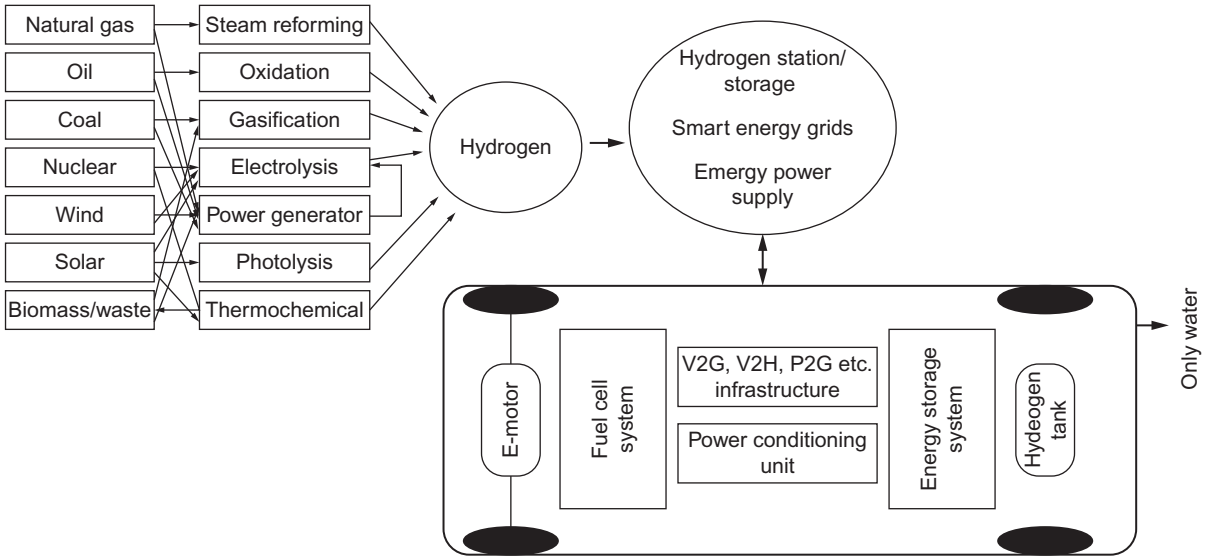


FIG. 33.1 Hydrogen energy chain and FCEV as a part of smart grids for sustainable transportation.

Brady and O'Mahony [7] evaluated the possibility of vehicular system-based emission reduction for the city of Dublin under different EDV market penetration scenarios. The results proved that EDVs could be considered as long-term alternatives to conventional vehicles, with the potential for considerable emissions reduction. The electrification of vehicular systems has the potential to lower the primary energy requirement and CO_2 emissions by 50% per kilometer. Browne et al. [8] focused on the role that can be played by different fuel delivery structures and new EDVs in reducing freight traffic and its environmental impacts in towns and cities. Perujo and Cuiffo [9] found that the vehicle-to-grid (V2G) interaction of EDVs could contribute to the efficiency of the energy distribution system that leads to better environmental results. Görbe et al. [10] described the idea of utilizing EDV batteries as storage devices in a low-voltage grid composed of distributed small-scale renewable power plants to contribute to both grid operation and environmental impact reduction. Moriarty and Honnery [11] explored the efforts promoting the use of EDVs to replace transportation-based fossil-fuel utilization and reduce GHG emissions, with a focus on reducing energy and emissions, and reported the midterm and long-term positive impacts of EDV penetration.

Transportation-specific policies and research & development (R&D) studies are strongly dedicated to find competitive alternative vehicular options to meet the GHG reduction targets in the long term and to enable the political effects of energy independence. Köhler et al. [12] assessed the innovation structures for R&D in low-carbon vehicles in the European Union (EU) automobile industry, which are primarily based on conventional vehicle technologies. This study also compared BEVs with both FCEVs and hydrogen fuel-cell PHEVs. The ever-increasing energy consumption causing the depletion of fossil fuels and rising public awareness for environmental protection resulted in much of the research work to focus on alternative/renewable energy sources. Thus, it becomes a requirement to replace conventional fuels with new energy sources [13]. As a consequence, novel renewable and clean energy power sources must be considered including vehicular systems that are primarily driven by conventional fuel types. Among the possible alternatives, as a part of the change toward the hydrogen-based energy system, hydrogen fuel-cell vehicles are given specific importance and will play a major role to realize sustainable transportation (see Fig. 33.1), improve the quality of life, reduce health-care costs, and promote technological reform in automotive industry [14–18].

An FC is an energy conversion device that converts the chemical energy of a reaction directly into electricity with byproducts of water and heat. There are several types of commercially available FCs, such as polymer electrolyte or proton-exchange membrane (PEM) FCs, solid oxide FCs, alkaline FCs, molten carbonate FCs, phosphoric acid FCs, and direct methanol FCs. Among the various types of FCs, the PEMFC technology has found widespread use, especially in vehicular applications [14].

> The PEMFC technology is still under active R&D investigation for powering systems in many applications. However, the daily operation of systems like vehicular loads and residential units with transient load changes may not be suitable for using a sole PEMFC system. This phenomenon is mainly caused by the limitation of FCs to track fast load variations due to their slow dynamics. These fast energy demand periods frequently occurring in the operation of daily utilized systems to high-voltage drops in a short time, which is defined as starvation phenomenon [16]. In the case of fuel starvation, the FC performance degrades, and cell

voltage drops. This issue may cause a significantly insecure operation for the FC stack. Thus, to utilize an FC in dynamic applications, its current or power slope must be limited to prevent the fuel-starvation problem. Therefore, hybridizing FC system with an energy storage system (ESS) decreases system cost, while sizing improves dynamic performance of overall vehicle system, promotes FC lifetime, and provides fuel economy owing to regenerative braking energy capturing and load sharing. Because of different characteristics of multiple power sources or ESS in a PEMFC-powered hybrid system, the efficiency and the fuel economy of these hybrid units mainly depend on a proper energy management strategy and well-designed power electronics architecture [15]. However, the hybridization with ESS will cause the complexity of the vehicle and the control systems, weight increase, and extra storage cost [5].

Since FCEV is a completely new and complex scientific area with significant capital costs and administrative challenges, it needs systematic approach involving all stakeholders (central and local governments, transportation departments, energy companies, organizations, automakers, auto parts providers, universities, R&D institutes, etc.) [17,19]. Thus, coordination is a requirement about data collection and analysis, policy planning, infrastructure construction, safety, promotion, operation, management, maintenance, finance, etc. Besides, governments should support ambitious plans and incentivize regulations to introduce hydrogen-powered vehicles to the market. Hydrogen, which is one of the key elements of hydrogen-powered vehicles, can be produced from a variety of sources including fossil fuels such as natural gas, oil, and coal and renewable sources such as solar and wind power, biomass, waste, and nuclear energy.

Hydrogen is a future energy carrier, energy transporter, and energy transmitter. By the evaluation of environmental and economic assessments of the hydrogen supply chain, renewable sources, and conversion units such as photovoltaics (PVs), wind turbines (WTs), and FCs have been found to be promising energy sources toward building a sustainable energy economy in the next decade [18,20]. These renewable energy sources, however, suffer from some deficiencies when used as stand-alone energy sources and grid-parallel sources. The power generated by WT and PV systems is highly dependent on weather conditions. In addition, it is difficult to store the power generated by a PV or WT system for future use. To alleviate these problems, WT and PV sources can be integrated with other alternative systems. Therefore, alternative energy conversion systems such as PV cells and wind turbines can be cooperated with fuel cells and FCEVs. Felgenhauer et al. [19] concluded that FCEVs can be used as a part of hydrogen infrastructure may provide hydrogen to the natural gas supply (Power2Gas, P2G). Also, the V2G or vehicle-to-home (V2H) interaction of EDVs can contribute to the efficiency of the smart energy systems (as grid storage and P2G) or stand-alone applications such as emergency power sources [21]. Thus, higher efficiency can be obtained by making the best use of their features while overcoming their limitations [20]. In this case, when power is plentiful, FCEVs can be used both a storage and a flexible load resource [19]. The hydrogen produced by an electrolyzer using renewable power sources is used in the FC system and acts as an energy buffer. Thus, the effects of reduction and even the absence of available power from the renewable energy system can be easily tackled. By using the electrolyzer, hydrogen can be generated and stored for later use in FCV refueling [19].

This chapter focuses on the hydrogen-fueled FC technology, which is used in vehicle applications as an alternative energy converter (hydrogen to electric) for environment-friendly sustainable transportation. This chapter is organized as follows: First, hydrogen infrastructure, hydrogen production methods, and hydrogen storage systems are described. Second, the main types of fuel cells are described in detail. Third, fuel-cell system components and their properties are explained. Fuel-cell-powered automotive applications, their design and energy management architectures, current status and future trends, and safety issues are discussed in the final section.

33.2 Hydrogen Infrastructure and Vehicle Hydrogen Storage System

Hydrogen, which is the simplest and most abundant element in the universe, was discovered in the 1700s. The element is colorless, odorless, tasteless, and 14.4 times lighter than air. Hydrogen does not occur free; it is found in compounds in nature. The most well-known compound is water. Hydrogen is not found naturally; it comes from fossil fuels, renewable sources, and nuclear energy by using reformer, electrolyzer, or fuel processor.

When comparing with other energy sources, hydrogen has the highest energy content in terms of weight. For instance, 1 kg of hydrogen approximately has the energy of 2 kg natural gas or 3 kg oil. However, hydrogen has very low volumetric energy content that requires costly production, storage, and delivery of hydrogen. The capital cost of hydrogen production needs to be solved economically and environment-friendly for a successful hydrogen economy [5]. Recent advancements in hydrogen-powered applications make hydrogen as an indispensable source of energy for the hydrogen economy.

In future energy systems, renewable energy sources will be used to generate hydrogen, and power demand might be satisfied using renewable sources and fuel cells since the hydrogen economy is a vision of the future. Therefore, alternate energy conversion systems such as PV cells and WTs can be cooperated with FCs. Here, to sustain the power demand and solve the energy storage problem when too much renewable electricity is being produced compared with the demand that exists at that moment, electric energy can be stored in the form of hydrogen. By using an electrolyzer, hydrogen can be generated and stored

for future use. Since the process is providing hydrogen to the natural gas supply (Power2Gas, P2G) and combined heat power (CHP) approach, in the near future, they can be a competitive and convenient solution. It has been reported that with the growth in demand, the fuel-cell vehicle infrastructure would substantially reduce the cost [19].

33.2.1 Hydrogen Production Methods

Hydrogen can be produced from both renewable (hydro, wind, solar, biomass, and geothermal) and nonrenewable (coal, natural gas, and nuclear) resources [22]. Hydrogen is mainly produced through fossil-fuel processing. In the entire world, 48% of hydrogen is produced from natural gas, 30% from oil, 18% from coal, and only 4% from renewable sources [23].

The main hydrogen production methods are steam reforming, gasification, partial oxidation, thermochemical cycling, photolysis, and electrolysis. Steam reforming may be used with natural gas, gasification with coal and waste, partial oxidation with oil, thermochemical cycling with nuclear and solar, photolysis with solar, electrolysis with wind and solar, etc. [23,24]. Producing hydrogen with a low cost means reforming it from fossil fuel such as natural gas, which may give rise to pollution by forming carbon dioxide. Manufacturing hydrogen is relatively more expensive [18,25].

Hydrogen production through electrolysis of water is more promising as it avoids carbon emission. Water can be decomposed into its elementary components by passing electric current between two electrodes separated by an electrolyte. According to Faraday's law, hydrogen production rate of an electrolyzer cell is directly proportional to the electric current in the equivalent electrolyzer circuit.

Electrolysis process has been proposed especially for renewable systems. The power generated by these systems highly depends on weather conditions. For example, during cloudy periods and at night, a PV system would not generate any power. In addition, it is difficult to store the power generated by a PV system for future use. To overcome this problem, a PV system can be integrated with other alternate power sources and/or storage systems, such as electrolyzer, hydrogen infrastructure, and FC systems [26]. When assessing recent developments in hydrogen applications, renewable energy sources have been used to generate hydrogen. Besides, energy demand/supply management can be satisfied using renewable sources and hydrogen infrastructure by including FCEVs, smart grids, and hydrogen-fueling systems. The renewable hydrogen cycle coupled with smart grids is shown in Fig. 33.2.

33.2.2 Hydrogen Storage

The driving range of the FCEVs depends on its onboard hydrogen storage capability and other energy management systems. According to the improvements of the hydrogen storage tanks, FCEVs can meet to match driver expectations [5,23]. The use of hydrogen as a vehicle fuel requires an onboard storage that offers inherent safety and both volumetric and gravimetric efficiencies. Onboard storage in vehicular systems is one of the major barriers to the acceptance of hydrogen-powered vehicles

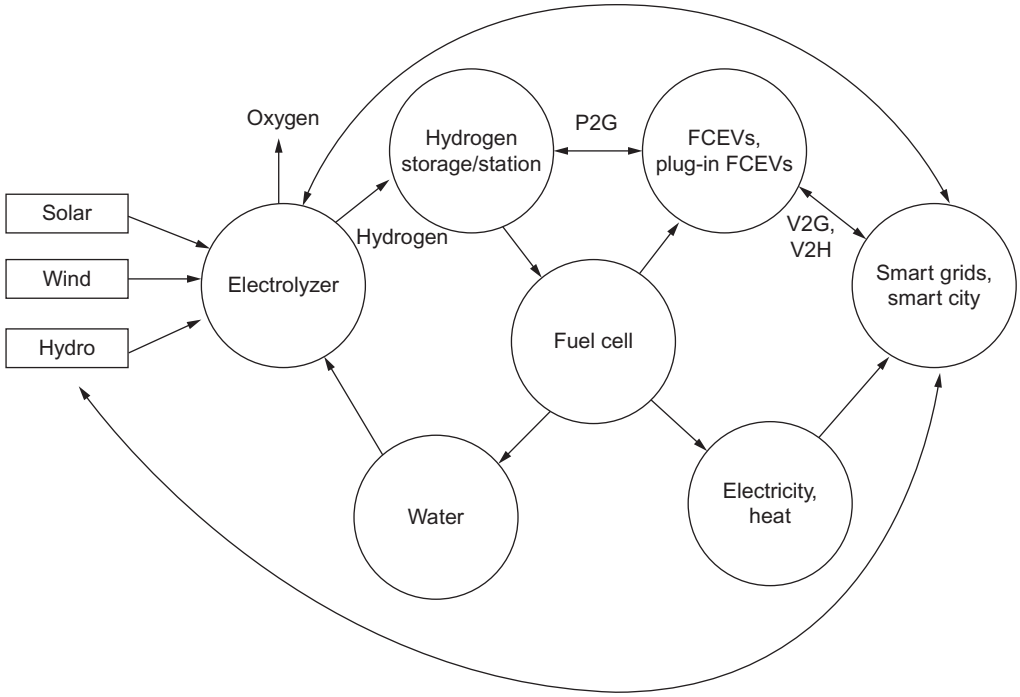


FIG. 33.2 Renewable hydrogen cycle coupled with smart grids.

[27]. Since onboard storage systems increase safety concerns especially for drivers and passengers during dangerous situations such as car accidents, the storage system gives a hazardous impression. The problems associated with hydrogen storage change from one storage technology to another. Thus, hydrogen storage technologies are evaluated as the first step of the current deliverable presentation. There are four technologies available today to store hydrogen aboard vehicles [16,17,28]:

- Compressed hydrogen gas in high-pressure tanks
- Liquefied hydrogen
- Metal hydrides
- New methods currently under development

The most used technique for hydrogen storage is compression of hydrogen into different kinds of high-pressure tanks [16]. According to the Department of Energy (DoE), compressed hydrogen technique will continue to be the most popular type of hydrogen storage for vehicular systems until 2020. Most vehicles currently in the on-road testing phase and on the road commercially are equipped with such a composite high-pressure tank. This is because of its simple structure and charge-discharge easiness. In general, vehicular pressurized hydrogen storage tanks made of very light and robust composite materials [29]. Storage density (gravimetric ratio) of above 0.05 kg of hydrogen per 1 kg of total weight, which means a stored hydrogen ratio of 5%, is easily achievable [16]. This ratio can reach up to 11.3% in this approach. There are two working pressures commonly used in commercialized vehicles such as 350 bar (35 MPa–5000 psi) and 700 bar (70 MPa–10000 psi) [17]. Leading FCEV automakers have mounted the high-pressured storage tanks on their models with their own preferences. For instance, while Toyota, Honda, and Hyundai use 700 bar (10,000 psi), Nissan uses 350 bar (5,000 psi) pressurized tank [5,21].

In another approach, the hydrogen gas is liquefied and stored under lower temperature and pressure compared with the high-pressure approach in liquefaction technique [16]. In this method, the ratio of stored hydrogen per tank weight is around 26%. However, the usage of liquid hydrogen storage system is limited because of its properties, cost of the manufacturing material, and cost of the tank. Besides, the whole process is relatively inefficient because a lot of energy is already consumed in the first stage of hydrogen liquefaction [30]. In this technique, nearly 26% of the stored hydrogen energy is consumed during the hydrogen liquefaction process [28]. In addition, liquid hydrogen tanks suffer from hydrogen leaks due to the unavoidable thermal losses that lead to pressure increase in the tank. This hydrogen self-discharge of the tank may reach to 3% daily, which means a 100% self-discharge in 1 month [31]. Hydrogen liquefaction and use of liquid hydrogen are usually practiced only where achieving high storage density is absolutely essential, such as in aerospace applications [28,16]. Some prototype hydrogen-powered automobiles also use specially developed liquefied hydrogen tanks [16].

Metal hydrides offer alternatives to the storage of hydrogen in gaseous and liquid form. Storing hydrogen as hydride in metals provides some advantages especially for safety in many applications. However, the tank weight provides a significant problem in this approach especially for applications like vehicular systems. The commercially available metal hydride hydrogen tanks offer a stored hydrogen ratio of 4.5% [27]. Besides, the repetition of hydrogen storage (absorption)/release (desorption) further decreases this ratio. Moreover, heat is released during the absorption process, which must be removed in order to achieve the continuity of the reaction. Similarly, during the hydrogen desorption process, heat must be supplied to the storage tank [16]. To overcome these limitations, some new techniques in metal hydride hydrogen storage approach are under investigation, which is expected to reach a hydrogen storage ratio of 10.5% in the near future [31].

New hydrogen storage methods have potential for providing higher energy densities than the conventional methods. These methods contain hydrogen storage in carbon nanotubes, storage in glass microspheres, boron-based storage, or storage in polyhydride chemical complexes [29]. Among them, the nanotube technique seems to be promising according to the recent developments in nanotechnology, which is anticipated to reach to a hydrogen storage ratio of 68% [17]. As another novel hydrogen storage method, boron-based chemical storage materials (like borohydrides and ammonia borane) are promising compounds with their high-hydrogen capacities. However, these hydrogen storage materials create ongoing problems from the kinetic and thermodynamic limitations in practice [32]. Besides, the current costs of these methods are extremely high that prevents the commercial utilization of these approaches [33,34].

33.2.3 Hydrogen Delivery and Fueling Station

It is expected that the FCEVs will have a significant market share in upcoming years. To that end, an effective and efficient utilization of the currently existing hydrogen infrastructure should be reconsidered for widespread penetration of FCEVs. Considering that proof-of-concept experiment with R&D studies for hydrogen generation has been already shown; construction of hydrogen generation and distribution infrastructure is a requirement for commercialization of FCEVs to achieve a sustainable process [19,21].

Hydrogen has poor volumetric energy density, and hence, FCEVs have a limited storage capacity, which makes hydrogen generation and distribution infrastructure a must-have. In addition, to ensure acceptance by public, hydrogen-refueling stations should be constructed and mounted.

Despite the expensiveness and complexity of hydrogen storage, it has been reported that delivering hydrogen by pipeline or tanker trucks to the refueling stations is possible with some adaptive alterations to the current infrastructure [17]. It is significantly important for both developed and developing

countries to realize these studies in a timely manner in order to prevent/reduce the possible future technological dependence on other countries about this issue. Several such studies are realized worldwide, especially in countries such as Japan, the United States, Germany, China, South Korea, and Italy, where renewable sources are used with a high ratio with a vision of future hydrogen economy and hydrogen generation, and distribution infrastructure has been already established or planned [17,19].

If hydrogen-fueled vehicles are used instead of natural gas delivery systems, using central hydrogen delivery system would be more convenient. Furthermore, decentralized and distributed hydrogen stations combined with electrolyzers and renewables will be built to meet the variable demands for hydrogen [5].

In this regard, the fueling and P2G operations of FCEVs should be controllable under the smart grid umbrella. Besides, hydrogen storage of FCEVs in parking condition can be utilized as a backup gas unit when the gas demand increases or fuel cells of FCEVs with suitable power-conditioning unit can supply power to electric loads and appliances. Thus, FCEVs can be considered as multicarrier energy sources. Likewise, BEVs and PHEVs are also considered as both storage and a flexible load resource with a connection to smart grids (including renewables) under a suitable smart charging and discharging approach. Furthermore, smart grids have the potential of exploiting renewable sources and providing the required infrastructure for BEVs and FCEVs [19]. Additionally, CHP of the electrolyzer can be considered as a supplementary.

In this context, Honda proposed and developed novel and efficient complementary applications of hydrogen value chain such as FCEV, compact/smart hydrogen station (SHS), high-pressure storage tank, fuel cell stack, electrolyzer, and power-conditioning units. After accomplishing their proof-of-concept experiments, commercialization by Honda has already started and currently being deployed in some regions [21]. To this end, some governments and automakers are cooperating, aiming to support hydrogen infrastructure development by methods by partially subsidizing operation costs of infrastructure firms [21,35]. However, the abovementioned issues cannot be evaluated independent from smart energy technologies.

33.3 Fuel Cells and Types

The fundamental principles of FC concept were described in 1838 by a Swedish scientist Christian Friedrich Schönbein. Sir William Grove, called the father of the FC, generated electricity by reversing the electrolysis of water in 1839, thus inventing the first FC system. In 1950, Francis Bacon from Cambridge University demonstrated the first 5 kW alkaline FC system. After the successful commercialization of alkaline FC technology, National Aeronautics and Space Administration (NASA) also started working on a weightless power system. In the 1970s, NASA developed a 12 kW alkaline fuel-cell (AFC) system for use with the space shuttle. Furthermore, researchers started R&D studies to use different types of fuel cells on applications like transportation systems. Currently, it is the most important development in the history of decentralized energy supply [5,24,36].

FC is an electrochemical device that generates electricity through a chemical reaction. It is an energy conversion device operating at high temperatures and using chemical energy stored in fuels, such as hydrogen, hydrocarbons, and alcohols without any direct combustion processes. Since the fuel-cell device is producing electricity and heat while altering hydrogen and oxygen into water, it emerged as one of the most promising power sources offering higher energy densities and energy efficiencies without any pollution [5,37,38].

FC is a converter, generating electric and heat energy with the electrochemical combination of hydrogen fuel and oxidant. This reaction emits only water. A fuel-cell system and chemical battery have a structural similarity. Unlike battery systems, the operation of fuel cells is restricted only by the existence of fuel, and there is no charging limitation [13]. Since FCs convert the chemical energy directly into the electric energy, FC efficiencies are not limited by theoretical Carnot efficiencies. Thus, FC has a high conversion efficiency compared with mechanical and combustion processes [38]. If the waste heat/exhaust can be cogenerated with the purpose of heating and cooling (can be used in residential, commercial, and industrial applications), typical values of efficiency would range up to 85% [37].

The main advantages of the FCs are as follows [5,37,39]:

- Potential to provide high operational efficiency and low operational maintenance
- Different fueling options
- Highly modular structure
- Offer zero or low environmental emissions and quiet operation
- No moving parts, except ancillaries (fans and pumps)
- Potential for high reliability

Barriers to more widespread adoption of the FC systems are the following [39]:

- Cost of FCs and the hydrogen infrastructure
- The lack of manufacturing and practical operating experience

FCs are generally classified depending on the type of electrolyte they use. Six main types of FCs are available in the market as listed below:

- Alkaline fuel cells (AFC)
- Molten carbonate fuel cell (MCFC)
- Polymer electrolyte fuel cell (PEMFC)
- Direct methanol fuel cell (DMFC)
- Phosphoric acid fuel cell (PAFC)
- Solid oxide fuel cell (SOFC)

The classification with some technical characteristics is shown in Table 33.1.

TABLE 33.1 Main types of fuel cells with some technical characteristics [5,25,37,40,41]

Types of FC	Operating temperature [°C]	Fuel	Charge carrier	Electrolyte	Oxidant	Start-up time (h)	Efficiency (%)
AFC	50–200	Pure H_2	OH^-	Liquid solution of KOH ($LiAlO_2$)	O_2 in air	<0.1	50–70
MCFC	650	H_2, CO, CH_4, other hydrocarbons	CO_3^{-2}	Lithium and potassium carbonate	O_2 in air	5–10	40–85 with cogeneration
PEMFC	50–100	Pure H_2	H^+	Solid polymer membrane (Nafion)	O_2 in air	<0.1	40–60
DMFC	60–200	CH_3OH	H^+	Solid polymer membrane	O_2 in air	<0.1	35–50
PAFC	160–210	Pure H_2	H^+	Phosphoric acid (H_3PO_4)	O_2 in air	1–4	35–85 with cogeneration
SOFC	800–1000	H_2, CO, CH_4, other hydrocarbons	O^-	Stabilized solid oxide electrolyte (Y_2O_3,ZrO_2)	O_2 in air	1–5	45–60 with cogeneration

33.3.1 Alkaline Fuel Cell

Alkaline fuel-cell system is one of the first developed fuel-cell technology with the simplest structure. It is the first type widely used on space applications [37,41]. AFCs use a liquid solution of potassium hydroxide (KOH) as an electrolyte that conducts ions between two electrodes: anode and cathode. Because the electrolyte is alkaline, the ion conduction mechanism has differences from PEMFCs [24]. At the basic structure of AFCs as given in Fig. 33.3, at the anode side, hydrogen undergoes oxidation reaction that turns hydrogen into a positively charged ion and negatively charged electron. The negatively charged electrons travel through an external circuit that generates electricity and unifies with oxygen atoms at the cathode side [42]. The alkaline electrolyte only lets the composed hydroxyl (OH^-) go through the anode side. By this reaction, hydrogen ions and hydroxyl reunite producing water. Eventually, water, heat and the electricity will be obtained.

Some key advantages of AFC systems can be specified as [43] the following:

- Low operation temperatures (50–200°C)
- Quick start-up range (<0.1 h)
- High efficiency (50%–70%)
- Low catalyst requirement reducing content costs
- Simple structure
- Low weight and volume

Some key disadvantages of AFC systems can be specified as [13,43–45] the following:

- Short operating life since they use a liquid solution of potassium hydroxide (KOH) as an electrolyte that is highly corrosive, thus eroding its parts
- Required oxygen must be provided after purification since they are very intolerant to carbon dioxide
- High cost for commercialized applications and current R&D studies are focusing on reducing costs

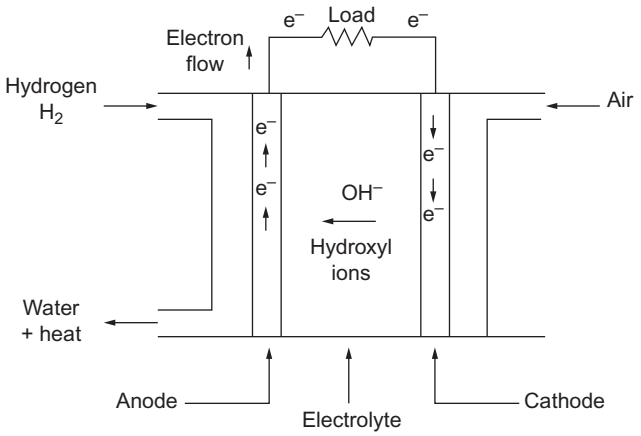


FIG. 33.3 Basic structure of an AFC.

33.3.2 Molten Carbonate Fuel Cell

The main principles of MCFCs are based on SOFCs and the other types of fuel cells. In the mid-1960s, Texas Instruments developed several MCFCs for US Army that led to a widespread use of MCFCs in the field [43].

MCFCs use lithium potassium carbonate salts as an electrolyte as shown in Fig. 33.4. They operate at high temperatures (650°C); therefore, catalysts can be made of low-priced metals to reduce cost, and the heat/exhaust can be utilized [37]. If the heat/exhaust can be utilized (with CHP), the efficiencies of MCFCs can be increased from 60% to 85%. Additionally, higher temperature makes the FC system more tolerant to poisoning (carbon monoxide) than lower temperatures. These systems can use either carbon dioxide or oxygen as a fuel. Currently, there are many molten carbonate systems available with capacities ranging from 100 kW up to 2 MW.

MCFCs do not demand an external reformer; thus, the primary fuel used may not be hydrogen gas. The basic components of natural gas, methane, and steam are processed at a reformer in the MCFC system, and electricity will be produced. The internal reformer reduces the costs compared with the other FC technologies with external reformers.

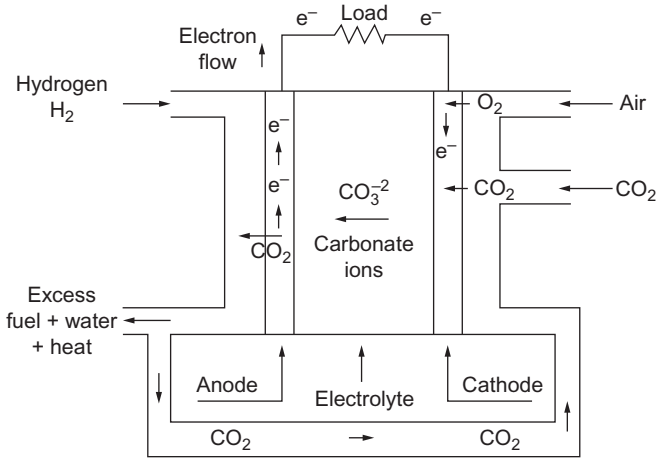


FIG. 33.4 Basic structure of a MCFC.

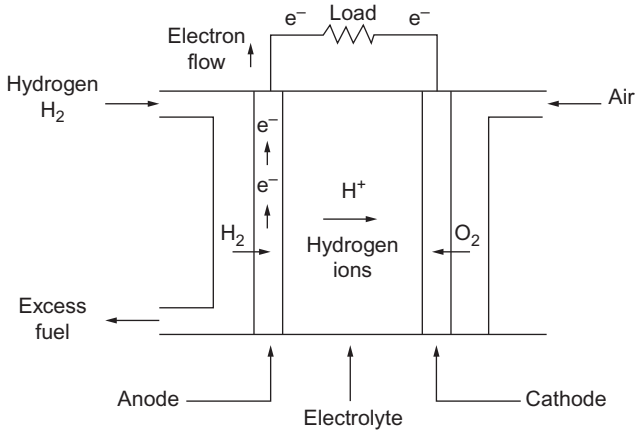


FIG. 33.5 Basic structure of a PEMFC system.

Some key advantages of MCFC systems are specified below [43,46]:

- Using the fuel converted in the system
- Producing so much heat/exhaust that can be cogenerated
- High efficiencies
- Relatively fast response to load changes in steady-state conditions
- Require low-cost catalysts
- Lower sensitivity to poisoning

Some key disadvantages of MCFCs include the following [46]:

- Slow start-up range (5–10 h)
- Demand redesigning with more resistant components to corrosion
- Problems in contenting the liquid electrolyte in the structure
- Requirement of preheating before starting work
- Short operating life especially when using for high-power production systems

33.3.3 Polymer Electrolyte Fuel Cell

Among the various next generation power supplies, the polymer electrolytes or PEMFCs have been found to be one of the most promising energy sources due to their high efficiencies and environment-friendly operations [47].

The basic structure of PEMFC, shown in Fig. 33.5, consists of three segments: the anode (negative characteristic electrode), the cathode (positive characteristic electrode), and the electrolyte membrane sandwiched between the two that allows only positively charged ions/protons to move between the two electrodes. The anode and the cathode have a catalyst, which speeds up the reactions at the electrode. Hydrogen goes to the anode side, and oxygen from the air flow goes to the cathode side. At the anode side, hydrogen undergoes oxidation reaction that turns hydrogen into a positively charged ion and negatively charged electron. After the reaction, protons are being transferred from anode to cathode through the electrolyte membrane, while the electrons travel through an external circuit. When the ions/protons reach the second electrode cathode, they will unify again with electrons and react with oxygen to form water. Eventually, electricity, water, and heat will be generated [39].

Some key advantages of PEMFCs include the following [16]:

- Low operation temperatures (50–100°C)
- Quick start-up range (<0.1 h)
- High efficiencies (40%–60%)
- Structure of electrolytes is more reliable, secure, and stable than other FCs
- High power density is the highest among all the available types of FCs
- High tolerance capability to differential pressures of the reactants
- Robust and simple structural design

Some key disadvantages of PEMFCs are listed below:

- Possess a structure highly depending on the purity of hydrogen
- Very poor tolerance to carbon monoxide and sulfur particles
- Gases require to be moisturized before reacting
- Comprised of a fairly expensive platinum catalyst and a solid polymer membrane

PEMFCs are a good candidate to substitute conventional technologies with their higher efficiencies and lower environmental impacts. The cost of PEMFCs is expected to down to consumer affordable levels in the near future [13].

Many advantages of PEMFCs, including fast response time, low operating temperature, high power density, and life cycling, have made the PEMFCs attractive and promising energy devices from the transportation and mobile applications to

stationary applications as a distributed generation [5,16]. Therefore, lots of big companies such as Ballard, UTC, Nuvera, PlugPower, General Electric, Toshiba, and Sanyo produce PEMFCs commercially. Leading automaker companies such as Honda, Toyota, Daimler-Chrysler, General Motors, BMW, Nissan, Ford, Hyundai, and Renault and worldwide brand-mark companies like Samsung and IBM use this shining technology for their own commercial applications [48].

33.3.4 Direct Methanol Fuel Cell

FCs either use hydrogen directly or reform hydrocarbon fuels like methanol, which is the simplest organic fuel that can be most economically and efficiently produced from relatively plentiful fossil fuel [24]. Thus, the operation of the DMFC is based on oxidation of water mixed with methanol. After the oxidation, methanol goes to the FC anode side [37]. DMFCs use a liquid fuel methanol, which is easier to transport for public using with current infrastructure [41]. DMFCs are often used to supply power for portable electronics and emergency power supply.

Recently, concerns about the poisonous effects of methanol have emerged; thus, companies prefer using ethanol instead of methanol [37]. DMFCs have immature technology, low power density, slow power response, and low efficiency compared with direct hydrogen FCs [24].

33.3.5 Phosphoric Acid Fuel Cell

Phosphoric acid fuel cell is the first developed FC technology and first to be used commercially. They are considered as first generation of modern FC. PAFCs use liquid phosphoric acid as an electrolyte. The PAFC systems have about 40% energy production efficiency and high operating temperatures (150–220°C) [42]. With cogeneration of heat/exhaust, the efficiency can be increased up to 85% [43]. Currently, there are PAFCs with capacities ranging from 200 kW to 11 MW. Necessary improvements for widespread use of PAFCs will require reducing the operating cost while increasing the operating life.

These FC systems have a drawback of weight; therefore, these FCs are not preferable on transport applications. Some key advantages of PAFC systems can be specified as follows [43,46]:

- Tolerant till 30% carbon dioxide content, hence direct usage of atmosphere air
- High efficiency (85%) with cogeneration of heat/exhaust (CHP)
- Operate trouble-free at temperatures (150–220°C)

Some key disadvantages of PAFCs include the following [42,43]:

- Slow start-up range (1–4 h)
- Low tolerant to carbon monoxide component
- Exhausting water content can damage acidic electrolyte (corrosion)
- Massive and heavy structure
- Requirement of external reformer
- Requirement of preheating before starting to operate

33.3.6 Solid Oxide Fuel Cell

SOFCs operate at high temperatures (700–1000°C), and every single solid oxide cell produces 0.8–1 V voltages [43]. The heat/exhaust (around 500–850°C) generated by SOFCs is attractive for cogeneration. SOFC systems are currently used in stationary applications such as backup power units. Furthermore, recent R&D studies are focusing on feasibility of SOFCs at transportation appliances [49,50].

Solid oxide fuel cells are promising with their inherent advantages for industrial applications such as its independence from pure fuel. Therefore, hydrogen and CO, CH_4, and other hydrocarbons can be used as fuel [37] in a SOFC. Since SOFCs operate at high temperatures, these systems can use low-cost catalyst components to enhance operational performance. SOFCs use a solid electrolyte, generally a ceramic material called yttria-stabilized zirconia (YSZ). Because the electrolyte does not involve a liquid-phased reaction, a problem such as fuel flooding does not occur. Also, SOFCs can be manufactured for many configurations, although other FC types with liquid electrolyte cannot [46].

In SOFCs, fuel is supplied to the anode side, and oxygen from the air flow goes to the cathode side as shown in Fig. 33.6. At the anode side, hydrogen undergoes oxidation reaction that turns hydrogen into a positively charged ion and negatively charged electron. The separated electrons travel through an external circuit from anode to cathode to produce electricity and oxygen atoms absorb the electrons. The solid electrolyte membrane only permits the transition of negative charged oxygen ions from cathode to anode. When oxygen ions reach anode, they react with hydrogen ions to form water.

SOFCs have about 45% efficiency that can reach 85% by capturing and utilizing the heat/exhaust. Additionally, the SOFC systems have low gas emissions [51].

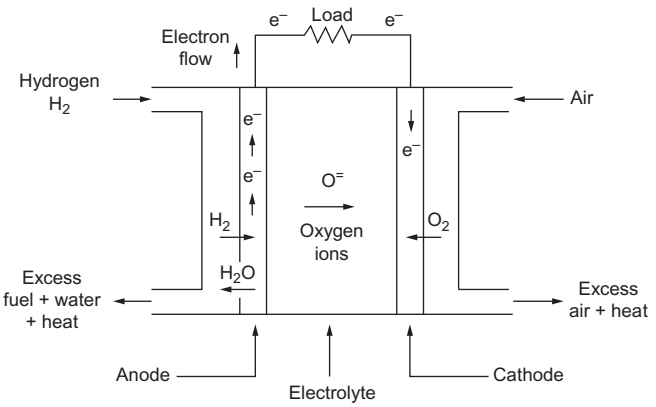


FIG. 33.6 Basic structure of a SOFC system.

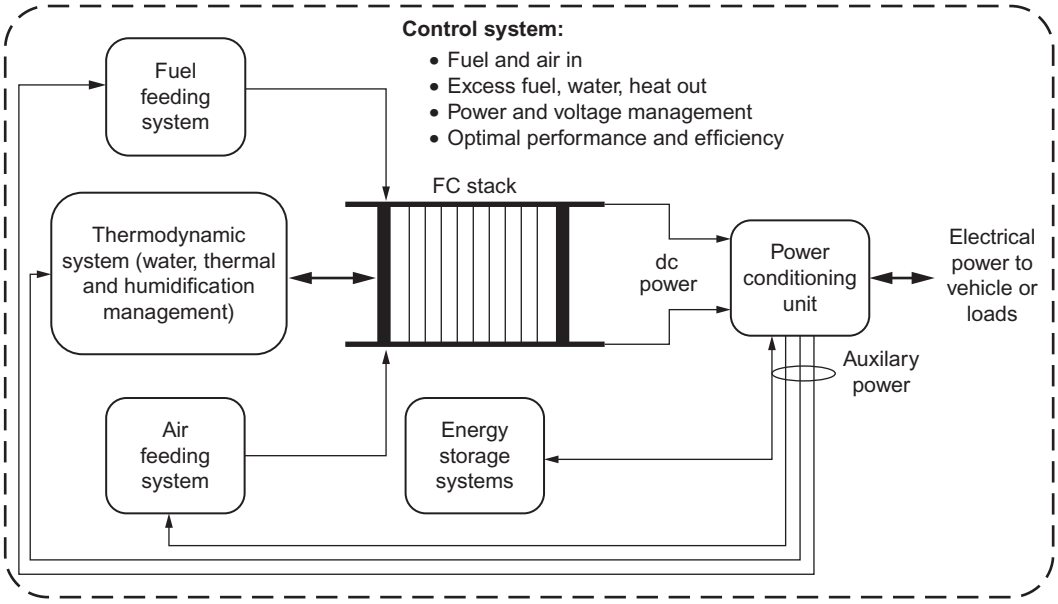


FIG. 33.7 FC system components.

Some key advantages of SOFC systems can be specified as follows [42,45,46]:

- Producing massive amount of heat/exhaust that can be utilized
- Fast chemical reactions
- High efficiency
- The solid electrolyte is more reliable than a liquid electrolyte
- Nonrequirement of external reformer
- No corrosion problems

Some disadvantages of SOFC systems include the following:

- Slow start-up range (1–5 h)
- Requirement of R&D studies on decreasing volumetric and gravimetric parameters
- Low tolerant to sulfur element
- Requirement of long-term proof-of-concept studies

33.4 Fuel Cell System Components

Among the various types of fuel cells, PEMFC has drawn the most attention due to its simplicity, viability, quick start-up range, higher power density, long cycle life, and low operational temperature (80–100°C). Since PEMFCs are the best candidate for vehicular and commercial applications, in this section, PEMFC system components are discussed in detail.

In practice, FC systems need auxiliaries (blowers, pumps, fans, ejectors, motors, turbines, compressors, valves, and regulators) to support their operation [24,52]. The main components of the FC system include the FC stack, fuel feeding, air compressors, humidifiers, power-conditioning unit with control systems, and energy storage system as shown in Fig. 33.7 [25]. All of these components work together to provide power to an electric load while regulating the proper amounts of fuel and ensuring system safety [52].

(i) *Fuel cell stack.* Although the FC stack is the main component of the fuel-cell system, for the required electric energy, all fuel-cell components must work in harmony. To that end, hydrogen fuel and air must be loaded into the stack as pressured gas. Thereafter, the excess hydrogen will be purged, and excess heat will be removed by circulating cooling water through the stacks during processing [23]. During operation, an FC produces dc electricity and water and heat through electrochemical process.

A fuel cell stack is made by assembling cells to deliver the required amount of voltage and power. Since a single cell produces less than 1 V, this voltage ratio is insufficient for most of the applications [21,41]. A single fuel cell consists of three metal plates called separators and two membrane electrode assembly (MEA) plates, which generates electricity. Innovative MEA design can provide effective and efficient fuel flow [21]. The cell generates electricity in the form of direct current (dc) by reacting hydrogen and oxygen in the air at the MEA.

The ideal potential of a hydrogen/oxygen FC under standard state conditions (25°C and 1 atm) is 1.229 V with liquid water product. However, the actual FC potential is lower than the ideal potential value due to the irreversible voltage drops that occurs in the FC system. There are three types of irreversible voltage drops, namely, activation overvoltage, ohmic overvoltage, and concentration overvoltage. At low current densities, the

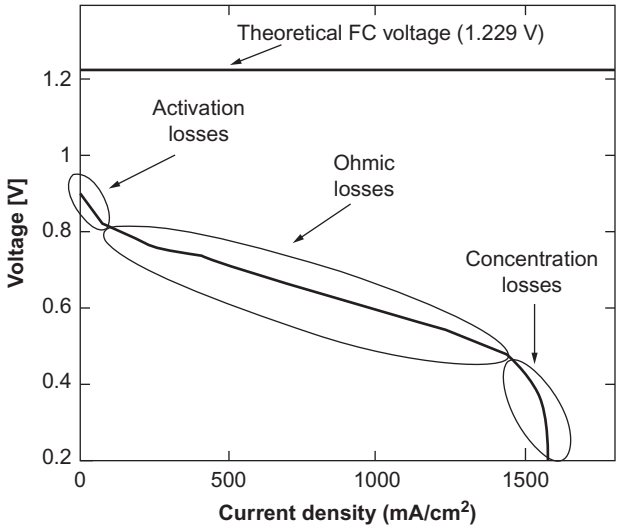


FIG. 33.8 Typical FC polarization curve.

activation overvoltage is responsible for the voltage drop of the FC. Besides, concentration overvoltage becomes more significant at high current densities. The effects of these voltage drops and the corresponding variance of FC voltage can be seen from the FC polarization curve shown in Fig. 33.8 [53]. Operating FC in this linear region is quite important for ensuring overall system efficiency.

The fuel cell stack from combined assembling cells is the most important part of a fuel-cell power system, like an engine in the conventional vehicle. The FC stack provides the current required by governing of a fuel flow rate through the anode channels, that is, the fuel flow rate varies according to the system power requirements [5]. The auxiliaries of FC system also consume 10%–15% of the total power output of the fuel cell stack [24]. The amount of power produced by fuel cell and its performance depends upon several factors, such as cell size, operating temperature, reactant gas stoichiometric flow rates, pressure of gases supplied to the cell, and anode and cathode humidification parameters [41,52].

(ii) *Fuel- and air-feeding systems.* Automotive applications with onboard hydrogen storage tank have control systems consisting of pressure regulators, relative humidity, fuel purity grade, and fluid-dynamic conditions [23]. As mentioned before, FCs have some limitations to track fast load variations, such as acceleration and deceleration for vehicular application, due to their relative slow dynamics, which is defined as FC starvation and flooding phenomenon. Thus, to utilize an FC in dynamic applications, both the air- and fuel-feeding control systems must be well managed and supported by a proper fuel cell energy storage system. To improve FC performance and efficiency, design and control of the air compressor are very important in order to accumulate and efficiently remove water produced from the reaction [21,23,41]. However, some automakers like Hyundai use different design as near-ambient air pressure to provide oxygen to the FC stack [54].

(iii) *Thermodynamic system.* In an FC system, water management, thermal management, and humidification can be increased to optimize overall system performance and improve power generation [23]. These three components must be efficient and reliable for optimum functioning of overall system, which require proper design, control, and water balance. If these conditions cannot be achieved, problems such as membrane drying out, electrode flooding and conductivity inadequacy, and excess water accumulation in the anode side would occur [23,25].

(iv) *Power-conditioning unit.* Another part of FC system is the power-conditioning unit (PCU). Because an FC produces dc electric energy, it must be converted from unregulated low-voltage level (voltage varies in a wide range depending on the load current) to regulated high-voltage level using a dc/dc converter and/or inverted to alternating current (ac) using dc/ac inverter for ac electric loads/drivetrains. The power-conditioning unit in such a vehicular system is mainly composed of dc/dc converters and an inverter unit. The inverter and propulsion motor are emulated using the dc load bank; therefore, only dc/dc converters are designed and built. The dc/dc converters used in FCEV topologies are the essential power-train components as they allow load sharing between main energy source and energy storage systems (ESSs) by using PCU. For example, the FC power stage is assigned for a power-tracking process to supply the determined power value from the FC system. Besides, ESS power stage can be devoted to DC link voltage control. Both power tracking and DC link voltage control processes can be implemented using a controller. Thus, this hybrid system topology provides the capability of delivering the desired power value from the FC system while keeping the bus voltage at desired intervals [55]. The driving motor can either be ac or dc motors such as induction motors, permanent magnet brushless motors, and switched reluctance motors [56]. The proper response of the FC system to the overall load dynamics can be achieved by generating appropriate power-switching signals to the converters [47]. While these converters design and operate, they must be preferred with high voltage ratio, high efficiency, low electromagnetic interference (EMI), and high compactness while keeping low cost [37].

(v) *Energy storage systems.* A stand-alone FC system integrated into an automotive powertrain is not always sufficient to satisfy the load demands of a vehicle. Although FC systems exhibit good power capability during steady-state operation, the response of

fuel cells during transient and instantaneous peak power demands is relatively poor. Therefore, when utilizing a PEMFC, it is recommended to associate it with an auxiliary power source to improve the dynamic performance of the whole system. There are many types of auxiliary units for compensating the slow response characteristics of the PEMFC unit and increasing the efficiency of the overall system. Energy storage units such as batteries, ultracapacitors (UCs), and flywheels, can be classified in the auxiliary power units group for use in hybrid systems including PEMFC. Specifically, not only energy storage units compensate the slow response phenomenon of PEMFC system, but also it provides the advantage of recovering the reusable kinetic energy that occurs in vehicular applications during braking periods. Thus, the consumption of hydrogen for FC units can be significantly decreased.

In many applications, batteries are utilized as ESS. Among the various existing rechargeable batteries, lithium-ion batteries appear to occupy a prime position in various aspects. A battery is needed in an FC system to supply power during the time after a change in the flow of reactants occurs. An auxiliary power source such as a battery bank can be used to improve the FC dynamics. In addition, the use of batteries reduces the size and cost of the FC, increases the lifetime, and avoids overloading. The battery bank supplies auxiliary power during cold start of the FC and supports peak demand periods or transient events. They also compensate the tracking delays of FC system. The state of charge (SoC) is an indicator showing the emptiness or fullness of the battery. The battery current can either be negative or positive, with respect to the mode of operation, for example, charging or discharging [57].

When the load power exceeds the maximum output of FC, battery starts to discharge through a converter located in the PCU and keeps discharging until the overloading ends. Also, if a step or ramp increase in the load demand occurs (even there is no overloading), battery bank helps the FC system until the FC power increases and matches the demanded power. The FC system has a relatively slow response in both step-up and step-down load conditions. When a step-down loading occurs, the output power of the FC slowly matches the reference power. In these conditions, the battery bank captures the differing power to successfully meet the load demands. These recaptured energies sometimes might not be sufficient to keep the battery SoC above a predefined level. Thus, another control loop is used to directly charge the battery bank from FC power plant with respect to the final SoC. The charge and discharge conditions of the battery are controlled with the aid of a dc/dc converter [57]. In the battery discharge current control, the key point is how good the FC power matches the active power requirement of the load. Thus, the positive difference between the FC reference power and the actual FC output power is processed to force the dc/dc converter to draw the reference current from the battery. The discharge current is limited using a saturation system to avoid battery overloading.

The battery can be charged when the FC reference power is above the power demand due to its slow response. While this can be evaluated as a naturally charging condition, another charging control loop is also employed. If all these conditions conforms the respective criteria, battery can be charged. In the battery charge current control, the key point is instantaneous SoC of the battery when compared with its nominal SoC. The battery charge current should be inversely proportional to the depth of discharge [57]. Also, the battery has some effect on meeting the reactive power demand. We can express the reactive power as the oscillating power between source and load buses. In systems including dc/ac conversion such as fuel cells, we observe that the reactive power oscillates between the reversible device (battery or UC) of the dc bus and the ac load bus. The reactive power passes through the antiparallel diodes of the inverter circuit to reach the rechargeable device and then passes to the load side through the next alternant. However, due to the reactive power losses on the contactors and the equivalent system impedance, there is always a dc power to be converted to the reactive power, which results in hydrogen consumption, stack dc voltage drop, and load bus voltage drop [57].

Ultracapacitors are also ESS devices that offer significantly better energy densities than conventional capacitors, better power densities than conventional batteries and can be constructed in modular and/or stackable format. The charge and discharge time of an UC varies from fractions of a second to several minutes, while providing maintenance-free operation. UCs provide the lowest cost per farad and extremely high cycling capability and prove to be environmentally safe [47]. The capacitance of UCs may vary from a few farads to several thousand farads per cell. Because of the aforementioned unique characteristics, UCs are utilized for a wide range of applications. Therefore, a UC bank can effectively serve as a cost-effective alternative to batteries, especially during short peak demand periods.

The natural structure of ultracapacitors is appropriate to meet transient and instantaneous peak power demands. The UC bank is designed to provide the difference between the load demand and the output power generated by the FC system. Without the UC bank, the FC system must supply all power demand, thus increasing the size and cost of the FC system.

The amount of energy drawn from the UC bank is directly proportional to the capacitance and the change in terminal voltage. The effective specific energy for a prescribed load can be supplied by various UC bank configurations. In practical applications, the required amount of terminal voltage and energy or the capacitance of UC storage system can be built using multiple UCs in series and parallel. The terminal voltage determines the number of capacitors, which must be connected in series to form a bank, and the total capacitance determines the number of capacitors, which must be connected in parallel

in the bank. The natural structure of UC is appropriate to meet transient and instantaneous peak power demands.

As a result, while choosing an ESS, the following characteristics should be considered [5,57]: specific energy and energy density; electric power, that is, the electric load required; volume and mass; storage capacity; reliability; durability; safety; cost; recyclability; environmental impact; response time; efficiency; self-discharge rate/charging cycles and excess discharge; sensitivity to temperature; charge-discharge rate lifetime; environmental effects; investing/operating cost; maintenance; availability; design complexity/voltage range; life cycle; and recharge rate of storage element.

33.5 Fuel Cells in Automotive Applications

FCs offer many advantages over the internal combustion engines (ICE) for vehicular applications because they are energy efficient, clean, and fuel flexible. Today, FCs have become smaller, more powerful, and more durable [54]. Since FCEVs provide much better air quality, health problems, such as incidence of asthma and other chest complaints, will decrease [25]. Hydrogen FC systems have the potential to reach 60% peak efficiency [15]. Onboard the vehicle, conversion of hydrogen produces electricity for power train of vehicle and water. Hydrogen can be obtained from various sources with different methods [58]. Leading automobile industries are making every effort to make hydrogen-powered vehicles affordable, environment-friendly, and safe [25,41].

Automobiles, buses, scooters, golf cars, utility vehicles (such as forklifts and airport vehicles), locomotives, tramways, boats, airplanes, and underwater vehicles can be considered as some of the applications of PEMFC systems in transportation area [15]. In automobile systems, almost all major automakers have demonstrated prototypes and commercially available FC vehicles and announced future plans for production and commercialization in the near future. On the other hand, buses seem to be the most likely type of road vehicles for an early market introduction of the FC technology. Also, scooters may be a significant market for FC technologies, especially in developing countries. To conclude, the transportation area seems to be the most promising sector of PEMFC technology.

The need to reduce emissions through the improvement of vehicle efficiency and the depleting fossil fuels has motivated researchers to investigate alternatives to conventional ICE-based vehicular systems. Among the alternatives, FC-powered electric vehicles using hydrogen as fuel are considered as the ultimate route to achieving sustainable long-term alternative propulsion systems [16]. Hydrogen is an energy carrier with many important unique features. It is considered as the lightest, most efficient, and cleanest fuel. One of its unique features is that it can be converted to electricity in FCs through electrochemical processes with higher efficiencies than conversion of fossil fuels to mechanical energy in ICEs. Thus, this particular characteristic allows higher efficiency and practically null emission of polluting agents for FC-powered vehicles compared with ICE-based vehicular systems. Particularly, these efficiency and environmental friendliness advantages become more significant when renewable energy sources such as wind and solar are used for hydrogen production. In particular, passenger vehicles are mostly operated at part loads significantly below their rated power; thus, vehicle running in urban or suburban areas demands a small fraction of the rated FC power most of the time. Thus, the efficiency of the overall system becomes higher as the FC is operated most efficiently. This issue is exhibited by Villatico and Zuccari [59] by comparing the performance of FC and ICE in real driving cycles. Moreover, FC-based vehicles have medium- and long-term potential to be the mainstream vehicle in the future because they have almost zero emission and compatible driving range to ICE-based vehicles [1,5,55]. For real utilization of EVs, many features should be considered, such as performance, cold start, reliability, durability, cost, and fueling/charging times, availability, and infrastructure [13,18]. Both FC and battery EVs have similar components, like driving motors, power conditioners; also, they will coexist in the future. The FCEV is a promising solution because of faster refueling, cold starting, faster warming up to operating temperature and longer driving range features compared with BEV [24,25,60]. Generally, the FCEVs are proper for midsize and long-range vehicles, while the BEV is suitable for small-size and short-range vehicles [5].

Among the various available FC types, PEMFC is the most likely candidate for automotive applications, thanks to its several attractive features, such as low operating temperatures, relatively low cost and quick start-up, simplicity, viability, packaging under the hood of vehicle, and high efficiency [55]. However, the unsteady operation of a vehicle may not be appropriate for the usage of a sole FC system. Moreover, a FC system (in the power train of an automotive) needs to be equipped with the combination of ESS, driving motor, converters, and various auxiliary devices [23]. The power demand of a vehicle motor undergoes significant variations due to acceleration, changes in road surface and traffic conditions. Thus, a sole FC system may not totally satisfy the power demand of a vehicle due to the limitation of fuel cells to track fast load variations because of their slow response dynamics. Besides, load demand fluctuations in vehicle operation may cause fuel starvation, flooding, membrane drying, and pressure imbalance across the FC membrane, which may damage the FC stack and decreases its lifetime [61]. Moreover, an advanced energy management strategy is necessary to split the power demand of a vehicle in a suitable way for the onboard power sources in order to maximize the performance while promoting the fuel economy and endurance of hybrid system components.

33.5.1 Design Architectures for PEMFC Powered Hybridizations

In general, FCEVs are configured as series vehicles [60]. However, the architecture of a FCEV can be configured in series, series-parallel, and parallel. The selection of the hybrid power-train topology is very important for an efficient operation and better market penetration of FCEV systems. Effective and efficient power conversion technologies are strategic for the progress of FCEVs [62]. Interfacing the load/power-train unit requirements with the different operational modes of onboard generation and storage systems call for suitable power electronic converter configuration and control. The selection of power-conditioning unit for hybrid systems including PEMFC is based on some significant factors like lower cost, space requirement, compact structure, higher efficiency, electric isolation, and ripple-free and reliable operation [15,62].

Despite the fact that hybridization concept brings remarkable benefits, the main challenge is to find the appropriate combination of energy sources. Each energy source has unique characteristics and energy conversion efficiency. Thus, each combination is expected to show different performance, efficiency, and fuel/energy consumption. Moreover, in a hybrid topology, these energy sources can be connected to dc bus either directly or via a power converter. In case of utilizing a power converter, which allows higher flexibility in load sharing, an improved hydrogen economy may be expected. However, system efficiency may decrease due to additional conversion stage, which might worsen the equivalent fuel economy.

Considering the abovementioned factors and the load/drive-train requirements, various topologies may be used for the operation of PEMFC hybrid systems. One of the simplest architectures for the parallel operation of PEMFC hybrid systems includes the direct integration of PEMFC system with the auxiliary power unit as shown in Fig. 33.9. During low power demand, the FC system generates up to its load limit, and the excess energy between the load demand and the FC output power is used to charge the auxiliary unit. In this period, the S1 switch is closed, and S2 switch is open. During high-power-demand periods, both the FC system and the auxiliary units supply the load demand. During this period, S1 switch is kept open, and S2 switch is closed. The direct integration topology is attractive, because it does not require a high-power dc/dc converter; thus, the complexity, cost, weight, and volume of the system are significantly reduced [15]. For example, the UC system integration can be achieved with or without power electronic converter via series and parallel connection. Because of the high specific power and power density of UC bank, it may be possible to eliminate the dc/dc converter for voltage regulation so that it can deliver higher output. This topology is proposed by Honda [63] for a combined PEMFC-/UC-powered vehicular system. Also, the direct integration of the FC with the UC bank is possible for relatively low-voltage applications with a dc bus of less than 50 V [64]. The UC bank and the load terminal voltages depend on the FC system terminal voltage, which prevents the power capability of the UC bank from being fully utilized. Therefore, the UC bank size is restricted by the terminal voltage of the FC system, as in the battery/UC hybrid system of Ref. [65].

Different designs of a topology with only one dc/dc converter unit are shown in Figs. 33.10 and 33.11. The topology in Fig. 33.10 regulates the output power of the FC system, while the rest of the energy between the load demand and the FC output power is naturally supplied by the auxiliary unit. Besides, the topology in Fig. 33.11 is based on the regulation of the auxiliary system output power or the regulation of the DC bus voltage. There are many studies in the literature using these two topologies. Some previous studies on these topologies are reviewed and summarized in Ref. [15].

The most common topology for hybrid systems is composed of multiple dc/dc converters as shown in Fig. 33.12. In this kind of topology, the dc/dc converter of one of the available power sources is employed for the dc bus voltage regulation, which is called voltage-oriented-control, and the rest of the converters are controlled for power tracking by power-oriented-control methodology. Thus, the proposed power-conditioning unit provides the capability of delivering the desired power value from the hybrid power sources while keeping the bus voltage

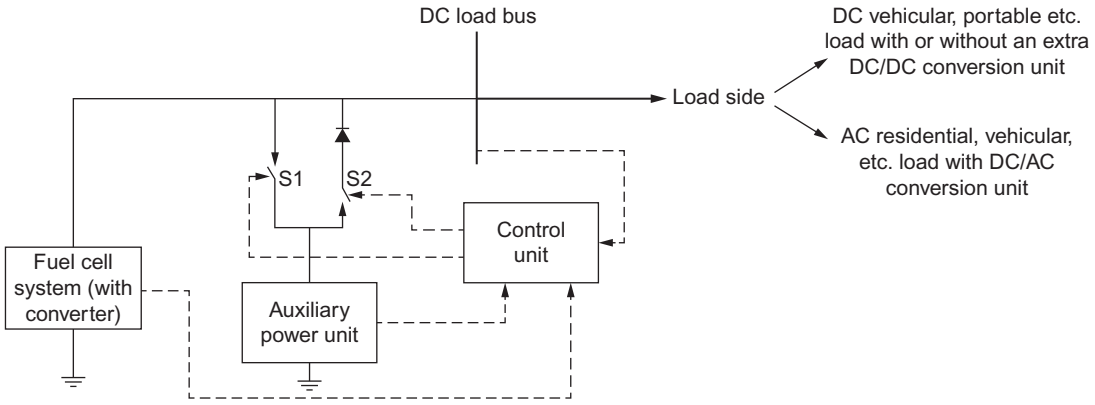


FIG. 33.9 Direct integration topology [15].

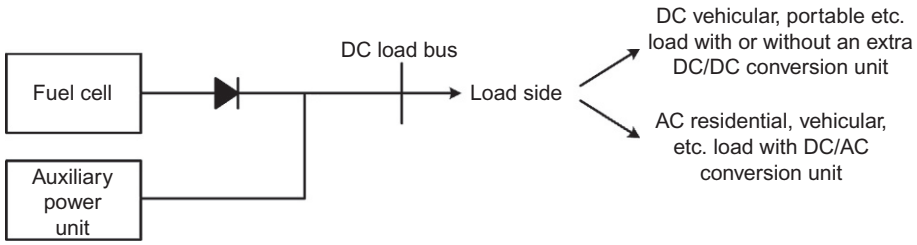


FIG. 33.10 Single converter-based topology [15].

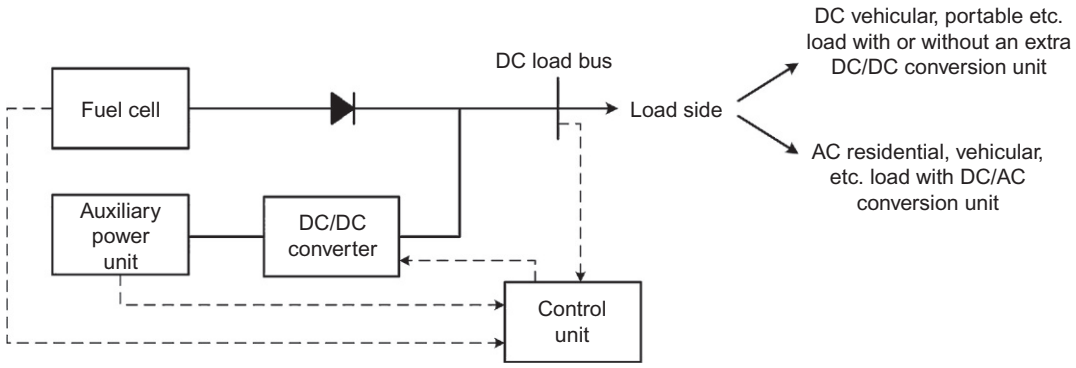


FIG. 33.11 Single converter-based topology [15].

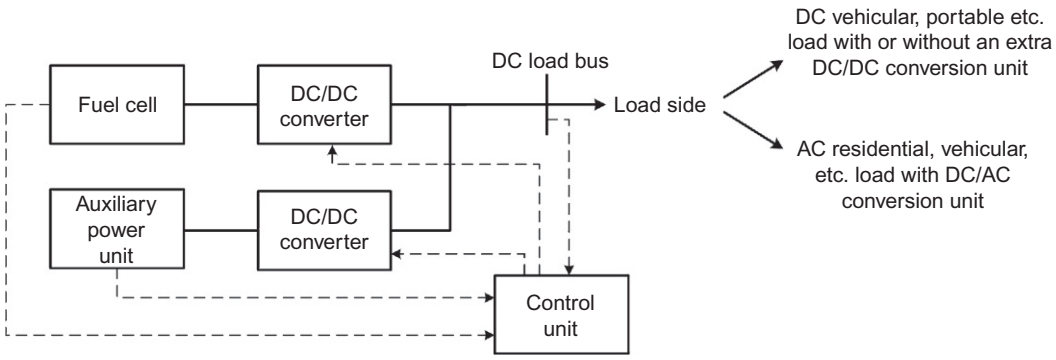


FIG. 33.12 Multiple converter-based topology [15].

at a desired level. Additional architectures for the usage of multiple converter topologies for transportation area are available in Refs. [53,66–70].

Combining the features of multiple converter-based topology, some researchers focused on utilizing multiple-input single-output design architecture as depicted in Fig. 33.13. This topology provides the advantage of reduced number of elements (multiple inputs of power sources can be connected to a dc bus via only one output capacitor) used in power electronics interface design. For example, Ferreira et al. [71], Perez et al. [72], and Napoli et al. [73] utilized the multi-input converter topology for an electric vehicular system consisting of PEMFC, battery, and UC.

The design of the abovementioned single- or multi-input converters can be realized as insulated or uninsulated, unidirectional, or bidirectional according to the area of application. The basic uninsulated unidirectional and bidirectional dc/dc converter topologies are shown in Fig. 33.14. The proposed multi-input and bidirectional converter-based PCU offers the following advantages:

- Voltage levels of the input power sources can be different.
- The input sources can deliver the requested power individually and simultaneously.
- Electrically isolation prevents damage on input sources.
- The proposed PCU can work bidirectionally, that is, the power can flow in either direction between individual input and output.

However, there are different advanced, more advantageous but complex topologies developed by power electronics researchers [15].

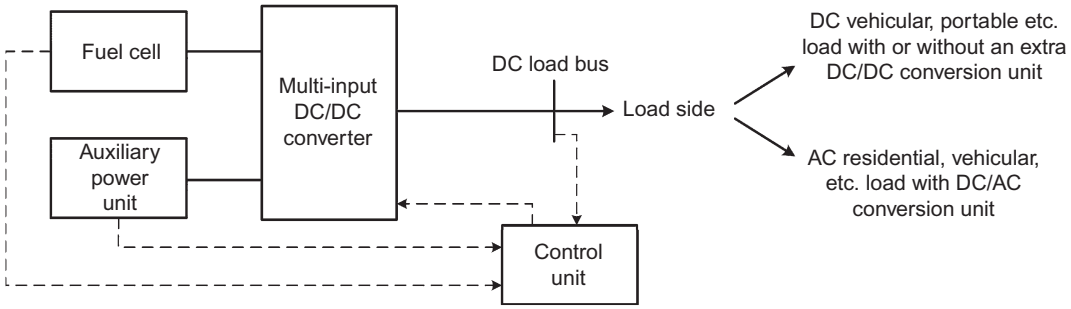


FIG. 33.13 Multi-input converter-based topology [15].

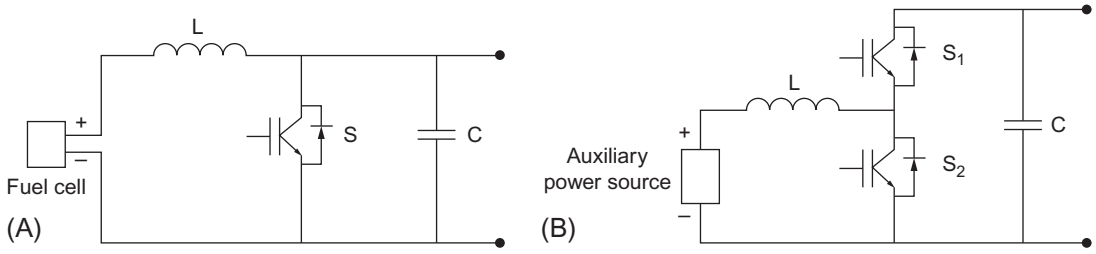


FIG. 33.14 Structures of the basic dc/dc converter topologies: (A) boost converter topology and (B) bidirectional converter topology [15].

33.5.2 Vehicular Power Control Strategy and Energy Management

Due to the different characteristics of multiple power sources, the efficiency and the fuel economy of hybrid systems mainly depend on proper energy management strategy (EMS), which is very important for PEMFC-powered hybrid systems.

An FCEV energy control system must provide good acceleration and high recovery of braking energy. The power sharing between the FC system and energy storage system (battery or UC bank) is determined according to the load sharing and control algorithm. Main requirements of the control algorithm are satisfaction of the power demand and management of the power flow in accordance with efficient operation of the different power sources. Coupled with this, the control system should utilize the FC system and energy storage system to match the vehicle load profile by considering different features of power sources.

Since stable operation of the FC system is vital for efficiency, lifetime and cost, FC system should deliver the base load power without responding to peak power demand. Another purpose of the control system is to adopt the battery or UC bank in stabilizing the dc link voltage. This enables power transfer to/from battery or UC bank and improves the driving performance.

Hybrid systems can provide improved efficiency when a well-designed energy splitting algorithm that considers the individual characteristics of each hybrid system is applied. There are many techniques for energy management that have been investigated in the literature, such as intelligence-based strategies, optimization-based strategies, and frequency decoupling strategies [74].

33.5.2.1 Intelligence-based Energy Management

Recently, many intelligence-based energy management strategies such as fuzzy logic, and neural networks for use in PEMFC-powered systems, have been reported in the literature [15]. Among them, fuzzy logic controller (FLC)-based methodology plays a dominant role due to its independence of a full mathematical plant model and training procedure. Nonlinearity and difficulties in proper identification of parameters of the plant mathematical models limit the use of model-based conventional control approaches.

Fuzzy logic provides suitable structure compared with conventional control methods especially for the systems comprising nonlinear behaviors where an overall mathematical model is difficult to obtain. Moreover, there is no need for historical data, which is an important advantage over other types of intelligent controllers such as neural networks. Thus, FLC provides a suitable structure especially for systems composed of nonlinear behaviors.

In the literature, many researchers applied fuzzy logic approach for hybrid systems with PEMFC for different applications. Among them, Gao et al. [75] provided the power distribution in a hydrogen-powered hybrid bus composed of PEMFC as the main power source and battery/UC combination as the auxiliary unit. In [15], FLC utilized the SoC values of auxiliary units and the required power demand of the bus as inputs for determining the output power values of FC and UC systems. Erdinc et al. [53,67] regulated the energy management in PEMFC/UC and PEMFC-/battery-/UC-powered hybrid vehicular systems using fuzzy logic. The aforementioned architectures [53,67] utilized the SoC values of battery and/or UC

units and a transient-free form of the vehicular power demand, provided by a load-sharing algorithm, based on standard drive cycles as inputs and gave the requested power value from PEMFC system as output. Li et al. [76] proposed a FLC design for a PEMFC/Battery hybrid system with a similar structure to Erdinc et al. [67]; however, they optimized the parameters of their FLC for an optimal energy control. As a contribution to the studies of Erdinc et al. [53,67] and Li et al. [76], Eren et al. [77] inserted the control of internal dynamics of PEMFC system in the fuzzy-logic-based energy management approach in order to provide a safe and efficient operation for PEMFC. Kisacikoglu et al. [78] directly controlled the duty cycles of the converters of PEMFC and UC as the outputs of the FLC in a PEMFC/UC hybrid vehicular system.

Another intelligent method used for the control of hybrid system is the neural network approach. Comparing neural network with one of the most popular intelligence-based technique, fuzzy logic, this quick-response capability provides a significant advantage. Fuzzy logic approach does not need a training procedure; however, the rule-based fuzzy structure makes it longer to respond compared with neural network approach. Thus, neural network control may be a competitive approach with fuzzy logic for some applications. Besides, the abovementioned features would lead the neural networks to solve complex problems precisely and flexibly and provide a suitable basis for the control of complex systems. Consequently, neural network has demonstrated remarkable success in control area [15].

33.5.2.2 Optimization Based Strategies for Energy Management

Power management and control system is very important for improving energy efficiency, vehicle performance, and for reducing the weight, size, and cost. Various flexible control methods and intelligent techniques are used for optimization, subject to system constraints. The power management system not only optimizes the available sources but also manages the load dynamically, based on the need and priority of the demand. In these types of energy management approaches, the optimal reference power signals for onboard power sources are calculated by the minimization of a cost function. This cost function generally represents the fuel consumption or emissions especially for vehicular applications. If this optimization is performed over a fixed driving cycle, a global optimum solution can be found. Many approaches such as optimal control theory, linear programming, dynamic or stochastic programming, genetic algorithm, simulated annealing, linear and nonlinear predictive model, and game theory are utilized for solving the aforementioned global optimization problem.

There is significant number of studies dealing with the energy management of an FC-powered hybrid system utilizing an optimization-based methodology [79,80]. For example, Rodatz et al. [79] presented an experimentally applied equivalent fuel consumption minimization strategy aiming at minimizing the hydrogen consumption while maintaining drivability in a PEMFC/UC hybrid vehicular system. Xu et al. [80] performed a similar optimization approach for an FC/battery hybrid bus. Similar fuel consumption minimization-based approaches were also utilized by Paladini et al. [81] for FC/battery/UC hybridization for a vehicle in a simulated environment.

33.5.2.3 Frequency Decoupling Based Energy Management Strategies

During the daily operation of a system, load transitions may occur frequently. The load power profile is a nonstationary signal and consists of transients. The wavelet transform can be effectively used for analyzing power transients in FCEV power demand profile, because of its ability to deal with nonstationary and/or transient signals. A given signal can be decomposed into transients and desired characteristics can be extracted simultaneously in both the time and frequency domain by using the wavelet transform (WT). The WT decomposes into various components at different time intervals and frequency bands as a windowing technique. In wavelet analysis, long windows are used at low frequencies, and short windows are also used at high frequencies.

One of the most popular mother wavelets is Haar wavelet for detecting and localizing of transients. The Haar basis has the shortest filter length in the time domain in comparison to other wavelet bases. Because of the abovementioned features, the Haar wavelet transform is the most suitable functions for filtering HEV power demand load profile, which consists of transients corresponding to sharp peak power demand. The transients of the HEV power demand signal is clearly observed from the short-term frequency and component magnitude changes.

For some applications like vehicular systems, these transient changes in load demand may occur significantly, which pose dynamic stress onto the FC membrane due to pressure oscillations and possible fuel starvation, which may reduce the lifetime of the FC system. Thus, to ensure FC lifetime prolongation by preventing the FC system from load changes with high frequencies, researchers applied different frequency decoupling techniques. The basic approach for this issue is inserting a transfer function for a delay with a suitable time constant (first-order low-pass filter). Liu et al. [82] proposed such a first-order filter for PEMFC system. Besides, some conventional filtering techniques like Butterworth high- and low-frequency filters have been utilized. These conventional filters decouple the main signal with a predefined cutoff frequency; thus, the FC system can be prevented from transient variations. However, the loss of important edge information is a significant phenomenon in conventional filtering techniques. Considering this issue, some researchers applied a wavelet-transform-based frequency decoupling strategy for PEMFC-powered systems. Wavelet transform is a signal processing method that is well known for its capability to treat transient

signals. The advantage of wavelet analysis, as opposed to conventional techniques, is that wavelet transform decomposes a signal into a series of short duration waves or local basis functions (wavelets) on the time axis, which allows the analysis of local phenomena in signals consisting of many transients. Besides, wavelet transform provides a quadratic mirror filtering application and the loss of important edge information is minimized compared with conventional filtering techniques. Considering these features of wavelet transform, Uzunoglu and Alam [83] applied a wavelet-based energy management strategy for a PEMFC/UC hybrid vehicular system. A similar wavelet-based approach was utilized by Zhang et al. [66] for a PEMFC/battery/UC hybrid system.

With the abovementioned types of frequency decoupling strategies, the transients in the total power demand profile are captured, a safe operating condition for FC-based system can be provided and lifetime of the power sources can be extended [15].

33.5.2.4 Other Methods for Use in Energy Management

Existing methods in the literature in addition to the before mentioned techniques include basic linear proportional-integral (PI)-based approaches, complex adaptive control, robust control, and flatness-based control. A conventional linear PI controller is a basic approach that may be useful for use in real-time implementations of PEMFC systems. Many researchers utilized PI controller especially with a main supervisory controller design. As an example, Thounthong et al. [84,85] utilized a multiobjective PI-based linear technique for SoC sustaining and DC link voltage stabilization. Besides, Payman et al. [86] applied PI controller for the power electronics converter duty cycle determination in order to regulate the desired values of the system parameters determined by a nonlinear flatness-based supervisory control approach.

Another common approach, adaptive control technique, involves modifying the control law used by a controller to cope with the fact that the parameters of the system being controlled are slowly time-varying or uncertain. For example, as an aircraft flies, its mass will slowly decrease as a result of fuel consumption; we need a control law that adapts itself to such changing conditions. Adaptive control does not need a priori information about the bounds on these uncertain or time-varying parameters. Besides, adaptive control is precisely concerned with control law changes. There are mainly two types of adaptive controllers: feedforward and feedback adaptive controllers. There are many types of feedback adaptive controllers such as model reference adaptive controllers (MRACs) and model identification adaptive controllers (MIACs) that are reported in the literature [15].

Robust control methods, which explicitly deal with uncertainty, are designed to function properly so long as uncertain parameters or disturbances are within a typical limit. Robust methods aim to achieve robust performance and/or stability in the presence of bounded modeling errors. In contrast with an adaptive control policy, a robust control policy is static; rather than adapting to measurements of variations, the controller is designed to work assuming that certain variables will be unknown [15].

33.5.3 Current Status and Future Trends of Fuel Cell based Vehicles

Leading automakers have started to make their light-duty hydrogen FCEVs for testing and commercial applications. Available FCEVs are on the road in selected regions like California, Europe, Japan, where access to hydrogen stations are available. Some of these vehicle models include Honda FCV (2016), Toyota Mirai (2017), Mercedes-Benz B-Class F-Cell (2015), Hyundai Tuscon, and SUV (2016). All of these FCEVs uses 100 kW fuel cell stack. They also have quick refueling time of less than 10 min and driving range of around 200–300 mi [21,54,87–89].

The California Fuel Cell Partnership (CaFCP) plays a vital role in preparing to demonstrate and commercialize the vehicle technology of the twenty-first century. This organization is a unique collaborative of automakers, energy and FC technology companies, and government agencies. Currently CaFCP is focused on the marketization and industrialization and while emphasizing the importance for market introduction of FCEVs [90].

Although automakers have produced FC-based commercial vehicles, actually, they started to develop FCEV prototypes many years ago. For example, Toyota has developed various types of FCEVs, after it began its fuel-cell efforts in 1992. Ballard developed and demonstrated a hydrogen-fueled transit bus in 1993. GM demonstrated an FC/battery hybrid FCEV in 1998. Nearly 200 B-Class FC-based Mercedes-Benz vehicles have been with customers in the United States and Europe since 2010 [89]. AC Transit has the most comprehensive program to obtain real-world driving impressions and experiences and realize the earlier phase of the hydrogen FCEVs in North America [17,90]. The new Mercedes GLC F-CELL and next generation Honda FCEVs combine fuel cell and energy storage unit (lithium-ion battery) using plug-in hybrid technology that is planned to come to the market in 2017 and 2018, respectively [21,91].

Some governments (e.g., US and Japan) and automakers (e.g., Honda, Toyota, Daimler, Nissan, and Ford) are working together to support hydrogen infrastructure, public awareness, decrease operational costs of infrastructure firms. By cost reduction and mass production of competitive parts such as the FC stack, hydrogen, fueling stations, compact packaging, storage (battery and ultracapacitors), silicon carbide-based innovative power electronics, and electric motor technologies, these vehicles can be commercialized and introduced to the market for widespread use [18,21,37].

It is necessary to carry out further investigation on the performance, reliability, durability, and cost reduction of FC

systems. FCEV design architecture plays a significant role while considering the performance, packaging, interior-space, efficiency, real-world performance, and durability issues. FCEV systems should be environmentally safe and commercially viable. Without doubt, technologies of a stable supply of highly pure hydrogen and inexpensive cell components are a prerequisite for market penetration of FC systems. In this case, since the number of renewable energy sources is increasing rapidly, new business models and marketing strategies can be developed. For example, the production of green hydrogen from renewable sources (biomass, biowaste, electrolyzers powered by photovoltaic, and wind energy systems) and also other feasible and viable hydrogen production methods can be used to feed the FCEVs and to balance the electric and gas grids under the smart grid concept [5,20]. Besides, as a part of sustainable energy and transportation chain, FCEVs, and their modular infrastructures like power inverter and hydrogen stations can contribute to the efficiency of the smart energy systems (as V2G, V2H, flexible load, storage, combined heat power, grid balancing, energy exchange, feed-in tariffs, and emerging application concepts). These kinds of EVs, like FCEVs, can also be used as an investment tool and as a major player of energy market in the future smart grids and smart cities.

Demonstration infrastructure should be sufficient for envisioned commercialization roadmap [5]. Demonstration projects and proof of concept experiments will act as a seed in addressing problems associated with practical applications, data collection for standardization, durability of FCEVs and accelerate awareness of using hydrogen in our daily life [5,17,21,92]. From the viewpoint of FCEVs market penetration, currently, there are limited commercial FCEVs, but in medium- and long-term periods, there will be huge numbers of FCEVs on the road depending on the abovementioned strategies of developed and developing countries. Thus, they can contribute significantly toward sustainable transportation and hydrogen chain.

33.5.4 Safety

Hydrogen FCs can revolutionize many sectors, since hydrogen is as safe as or even safer than other flammable fuels such as gasoline or natural gas. However, with the lack of professional design and management, hydrogen fuel cells pose several other risks that other flammable fuels do not.

Nowadays, FCEVs, hydrogen refueling stations and other values of hydrogen chain started to operate in different regions, despite pending answers to potential questions (How safe is hydrogen? What are potential hazards of hydrogen? Which improvements does it require to avoid danger?) [5]. Hazards and associated risks for hydrogen fuel cells should be considered by all stakeholders such as designers, regulators, and users in various situations when FCEVs are inoperable, in normal operation and in collision [5,16].

The main potential hazards can be listed as follows [5,16,21]:

- Hydrogen burns (rather than explosion)
- Higher flammability range
- Danger posed by invisible hydrogen flames (adding chemicals like odorant for required luminosity can provide an easier detection)
- Hard detection of hydrogen leak
- Higher tendency to leak since hydrogen is the smallest molecule (professional design may prevent leaks)
- Potential of hydrogen to asphyxiate people
- Frostbite/cold burns of liquid hydrogen
- Refueling station accidents

These hazards may be prevented or the impacts can be decreased with more R&D studies, administrative supports, efforts of all stakeholders, etc. For instance, Honda improved several designs to prevent FCEVs from collision impacts such as fastening bar as an impact resistant to prevent cells, straight frame structure to protect components, and load path structure to disperse the collision load and for efficient absorption of energy [21].

33.6 Conclusion

Almost all major companies have publicized ambitious plans to introduce hydrogen-powered vehicles in the market. Moreover, FCEVs are sold in selected regions with access to hydrogen stations. This vehicle type promises very clean operation and shows higher energy efficiency compared with conventional vehicles. When the FCEV technologies become mature, FCs can also be extended in many diverse areas from portable devices to silent heavy vehicles or aerospace applications. Besides, FCEVs and their infrastructure systems can also be used as a backup or integrated system for renewable energy sources.

In the near future, as a part of smart grid, FCEVs and hydrogen energy chain should be considered for sustainable development.

References

[1] G. Sen, A.R. Boynuegri, M. Uzunoglu, O. Erdinc, J.P. S. Catalo, Design and application of a power unit to use plug-in electric vehicles as an uninterruptible power supply, Energies 9 (3) (2016) 171.

[2] B. Tarroja, J.D. Eichman, L. Zhang, T.M. Brown, S. Samuelsen, The effectiveness of plug-in hybrid electric vehicles and renewable power in support of holistic environmental goals: part 1—evaluation of aggregate energy and greenhouse gas performance, J. Power Sources 257 (2014) 461–470.

[3] G.J. Offer, D. Howey, M. Contestabile, R. Clague, N. P. Brandon, Comparative analysis of battery electric, hydrogen fuel cell and hybrid vehicles in a future sustainable road transport system, Energy Policy 38 (2010) 24–29.

[4] B. Yagcitekin, M. Uzunoglu, A. Karakas, O. Erdinc, Assessment of electrically-driven vehicles in terms of emission impacts and energy requirements: a case study for Istanbul, Turkey, J. Clean. Prod. 96 (3910) (2015) 487–492.
[5] B.G. Pollet, I. Staffell, J.L. Shang, Current status of hybrid, battery and fuel cell electric vehicles: from electrochemistry to market prospects, Electrochim. Acta 84 (1) (2012) 235–249.
[6] D. Margaritis, A. Anagnostopoulou, A. Tromaras, M. Boile, Electric commercial vehicles practice perspectives and future research directions, Res. Transport. Bus. Manag. 18 (2016) 1–4.
[7] J. Brady, M. O'Mahony, The potential impacts of electric vehicles on climate change and urban air quality, Transp. Res. D 16 (2) (2011) 188–193.
[8] M. Browne, J. Allen, J. Leonardi, Evaluating the use of an urban consolidation centre and electric vehicles in central London, IATSS Res. 35 (1) (2011) 1–6.
[9] A. Perujo, B. Cuiffo, The introduction of electric vehicles in the private fleet: potential impact on the electric supply system and on the environment. A case study for the Province of Milan, Italy, Energy Policy 38 (8) (2010) 4549–4561.
[10] P. Görbe, A. Magyar, K.M. Hangos, Reduction of power losses with smart grids fueled with renewable sources and applying EV batteries, J. Clean. Prod. 34 (2012) 125–137.
[11] P. Moriarty, D. Honnery, Greening passenger transport: a review, J. Clean. Prod. 54 (2013) 14–22.
[12] J. Köhler, W. Schade, G. Leduc, T. Wiesenthal, B. Schade, L. T. Espinoza, Leaving fossil fuels behind? An innovation system analysis of low carbon cars, J. Clean. Prod. 48 (2013) 176–186.
[13] A.A. Abd El Monem, Ahmed M. Azmy, S.A. Mahmoud, Effect of process parameters on the dynamic behavior of polymer electrolyte membrane fuel cells for electric vehicle applications, Ain Shams Eng. J. 5 (1) (2014) 75–84.
[14] M. Uzunoglu, M.S. Alam, Dynamic modeling, design and simulation of a PEM fuel cell/ultra-capacitor hybrid system for vehicular applications, Energy Convers. Manag. 48 (5) (2007) 1544–1553.
[15] O. Erdinc, M. Uzunoglu, Recent trends in PEM fuel cell-powered hybrid systems: investigation of application areas, design architectures and energy management approaches, Renew. Sust. Energ. Rev. 14 (9) (2010) 2874–2884.
[16] F. Barbir, PEM Fuel Cells: Theory and Practice, Elsevier Academic Press, London, UK, 2005.
[17] W. Han, G. Zhang, J. Xiao, P. Bénard, R. Chahine, Demonstrations and marketing strategies of hydrogen fuel cell vehicles in China, Int. J. Hydrog. Energy 39 (25) (2014) 13859–13872.
[18] A. Veziroglu, R. Macario, Fuel cell vehicles: state of the art with economic and environmental concerns, Int. J. Hydrog. Energy 36 (1) (2011) 25–43.
[19] M.F. Felgenhauer, M.A. Pellow, S.M. Benson, T. Hamacher, Evaluating co-benefits of battery and fuel cell vehicles in a community in California, Energy 114 (1) (2016) 360–368.
[20] O.C. Onar, M. Uzunoglu, M.S. Alam, Modeling, control and simulation of an autonomous WT/PV/FC/UC hybrid power system, J. Power Sources 185 (2) (2008) 1273–1283.
[21] http://world.honda.com/FuelCell/.
[22] P.P. Edwards, V.L. Kuznetsov, W.I.F. David, N. P. Brandon, Hydrogen and fuel cells: towards a sustainable energy future, Energy Policy 36 (12) (2008) 4356–4362.
[23] P. Corbo, F. Migliardini, O. Veneri, Hydrogen Fuel Cells for Road Vehicles, Springer-Verlag, London, 2011.
[24] M.H. Rashid, Modern Electric, Hybrid Electric, and Fuel Cell Vehicles Fundamentals, Theory, and Design, second ed., Taylor and Francis, 2010.
[25] R. Dell, Patrick T. Moseley, A. David, J. Rand, Towards Sustainable Road Transport, Elsevier, 2014.
[26] M. Uzunoglu, O.C. Onar, M.S. Alam, Modeling, control and simulation of a PV/FC/UC based hybrid power generation system for stand-alone applications, Renew. Energy 34 (3) (2009) 509–520.
[27] C.C. Elam, C.E.G. Padro, G. Sandrock, A. Luzzi, P. Lindblad, E. F. Hagen, Realizing the hydrogen future: the International Energy Agency's efforts to advance hydrogen energy technologies, Int. J. Hydrogen Energy 28 (6) (2003) 601–607.
[28] M. Momirlan, T.N. Veziroglu, Current status of hydrogen energy, Renew. Sust. Energ. Rev. 6 (1-2) (2002) 141–179.
[29] S. Sherif, F. Barbir, T. Veziroglu, Wind energy and the hydrogen economy, in: 41st Aerospace Sciences Meeting and Exhibit, Aerospace Sciences Meetings, 2003.
[30] I. Hadjipaschalis, A. Poullikkas, V. Efthimiou, Overview of current and future energy storage technologies for electric power applications, Renew. Sust. Energ. Rev. 13 (6–7) (2009) 1513–1522.
[31] A. Schell, H. Peng, D. Tran, E. Stamos, C.C. Lin, M.J. Kim, Modelling and control strategy development for fuel cell electric vehicles, Annu. Rev. Control. 29 (1) (2005) 159–168.
[32] T. Umegaki, J.M. Yan, X.B. Zhang, H. Shioyama, N. Kuriyama, Q. Xu, Boron- and nitrogen-based chemical hydrogen storage materials, Int. J. Hydrog. Energy 34 (2009) 2303–2311.
[33] D. Fraser, Solutions for hydrogen storage and distribution, in: The PEI Wind-Hydrogen Symposium, 2003.
[34] F.L. Darkrim, P. Malbrunot, G.P. Tartaglia, Review of hydrogen storage by adsorption in carbon nanotubes, Int. J. Hydrog. Energy 27 (2) (2002) 193–202.
[35] https://www.hydrogen.energy.gov (accessed 23.02.17).
[36] A. Kirubakaran, S. Jain, R.K. Nema, A review on fuel cell technologies and power electronic interface, Renew. Sust. Energ. Rev. 13 (9) (2009) 2430–2440.
[37] A. Emadi, M. Ehsani, J.M. Miller, Vehicular Electric Power Systems, Land, Sea, Air, and Space Vehicles, Marcel Dekker, 2004.
[38] A. Bocarsly, D. Michael, P. Mingos, Fuel Cells and Hydrogen Storage, Springer-Verlag, Berlin Heidelberg, 2011.
[39] C. Spiegel, PEM Fuel Cell Modeling and Simulation Using MATLAB®, Academic Press, 2008.
[40] Y. Wang, D.Y.C. Leung, J. Xuan, H. Wang, A review on unitized regenerative fuel cell technologies, part-A: Unitized regenerative proton exchange membrane fuel cells, Renew. Sust. Energ. Rev. 65 (2016) 961–977.
[41] https://www.energy.gov/eere/fuel-cells/types-fuel-cells (accessed 23.02.17).
[42] J. Larminie, A. Dicks, Fuel Cell Systems Explained, John Wiley & Sons, 2003.
[43] J.M. Andujar, F. Segura, Fuel cells: history and updating. A walk along two centuries, Renew. Sust. Energ. Rev. 13 (9) (2009) 2309–2322.
[44] S. Mekhilef, R. Saidur, A. Safari, Comparative study of different fuel cell technologies, Renew. Sust. Energ. Rev. 16 (1) (2012) 981–989.
[45] Q. Cai, D.J.L. Brett, D. Browning, N.P. Brandon, A sizing-design methodology for hybrid fuel cell power systems and its application to an unmanned underwater vehicle, J. Power Sources 195 (19) (2010) 6559–6569.

[46] U.S. Department of Energy Office of Fossil Energy National Energy Technology Laboratory, Fuel Cell Handbook (seventh ed.), EG&G Technical Services, Inc., Under Contract No. DE-AM26-99FT40575.
[47] M. Uzunoglu, M.S. Alam, Dynamic modeling, design, and simulation of a combined PEM fuel cell and ultracapacitor system for stand-alone residential applications, IEEE Trans. Energy Conver. 21 (3) (2006) 767–775.
[48] J.H. Wee, Applications of proton exchange membrane fuel cell systems, Renew. Sust. Energ. Rev. 11 (8) (2007) 1720–1738.
[49] D.J.L. Brett, P. Aguiar, N.P. Brandon, R.N. Bull, R.C. Galloway, G. W. Hayes, K. Lillie, C. Mellors, C. Smith, A.R. Tilley, Concept and system design for a ZEBRA battery–intermediate temperature solid oxide fuel cell hybrid vehicle, J. Power Sources 157 (2) (2006) 782–798.
[50] L. Guo, K. Yedavalli, D. Zinger, Design and modeling of power system for a fuel cell hybrid switcher locomotive, Energy Convers. Manag. 52 (2) (2010) 1406–1413.
[51] I. Dincer, Technical, environmental and exergetic aspects of hydrogen energy systems, Int. J. Hydrogen Energy 27 (3) (2002) 265–285.
[52] C. Mi, M.A. Masrur, D.W. Gao, Hybrid Electric Vehicles: Principles and Applications with Practical Perspectives, first ed., John Wiley & Sons, 2011.
[53] O. Erdinc, B. Vural, M. Uzunoglu, A Wavelet-Fuzzy Logic based energy management strategy for a fuel cell/battery/ultra-capacitor hybrid vehicular power system, J. Power Sources 194 (1) (2009) 369–380.
[54] https://www.hyundaiusa.com/tucsonfuelcell/index.aspx (accessed 23.02.17).
[55] B. Vural, O. Erdinc, M. Uzunoglu, Parallel combination of FC and UC for vehicular power systems using a multi-input converter-based power interface, Energy Convers. Manag. 51 (12) (2010) 2613–2622.
[56] N. Sulaiman, M.A. Hannan, A. Mohamed, E.H. Majlan, W.R. Wan Daud, A review on energy management system for fuel cell hybrid electric vehicle: issues and challenges, Renew. Sust. Energ. Rev. 52 (2015) 802–814.
[57] O.C. Onar, M. Uzunoglu, M.S. Alam, M.Y. El-Sharkh, A PEM fuel cell/battery hybrid power system under various load conditions, in: Proceedings International Hydrogen Energy Congress and Exhibition IHEC 2007 Istanbul, Turkey, 13–15 July, 2007.
[58] J.H. Wee, Applications of proton exchange membrane fuel cell systems, Renew. Sust. Energ. Rev. 11 (8) (2007) 1720–1738.
[59] F. Villatico, F. Zuccari, Efficiency comparison between FC and ice in real urban driving cycles, Int. J. Hydrogen Energy 33 (12) (2008) 3235–3242.
[60] K. Ettihir, L. Boulon, K. Agbossou, S. Kelouwani, M. Hammoudi, Design of an energy management strategy for PEM fuel cell vehicles, in: Industrial Electronics (ISIE), 2012 IEEE International Symposium on, 28–31 May 2012, 2012.
[61] Z. Liu, L. Yang, Z. Maoa, W. Zhuge, Y. Zhang, L. Wang, Behavior of PEMFC in starvation, J. Power Sources 157 (1) (2006) 166–176.
[62] U.R. Prasanna, P. Xuewei, A.K. Rathore, K. Rajashekara, Propulsion system architecture and power conditioning topologies for fuel cell vehicles, IEEE Trans. Ind. Appl. 51 (1) (2015) 640–650.
[63] Honda Fuel Cell Power FCX. Available: http://world.honda.com/FuelCell/FCX/FCXPK.pdf, December 2004. Press Information [Online].
[64] Key, T.S., Sitzlar, H.E., Geist, T.D., Fast response, load-matching hybrid fuel cell. Final Tech. Prog. Rep., EPRI PEAC Corp., Knoxville, TN NREL/SR-560-32743, 2003.
[65] L. Gao, R.A. Dougal, S. Liu, Power enhancement of an actively controlled battery/ultracapacitor hybrid, IEEE Trans. Power Electron. 20 (1) (2005) 236–243.
[66] X. Zhang, C.C. Mi, A. Masrur, D. Daniszewski, Wavelet-transform-based power management of hybrid vehicles with multiple on board energy sources including fuel cell, battery and ultracapacitor, J. Power Sources 185 (2) (2008) 1533–1543.
[67] O. Erdinc, B. Vural, M. Uzunoglu, Y. Ates, Modeling and analysis of an FC/UC hybrid vehicular power system using a Wavelet-Fuzzy Logic based load sharing and control algorithm, Int. J. Hydrogen Energy 34 (12) (2009) 5223–5233.
[68] P. Thounthong, V. Chunkag, P. Sethakul, B. Davat, M. Hinaje, Comparative study of fuel-cell vehicle hybridization with battery or supercapacitor storage device, IEEE Trans. Vehicular Technol. 58 (8) (2009) 3892–3903.
[69] P. Thounthong, S. Rael, B. Davat, Energy management of fuel cell/battery/super-capacitor hybrid power source for vehicle applications, J. Power Sources 193 (1) (2009) 376–385.
[70] D. Feroldi, M. Serra, J. Riera, Energy management strategies based on efficiency map for fuel cell hybrid vehicles, J. Power Sources 190 (2) (2009) 387–401.
[71] A.A. Ferreira, J.A. Pomilio, G. Spiazzi, L.A. Silva, Energy management fuzzy logic supervisory for electric vehicle power supplies system, IEEE Trans. Power Electron. 23 (1) (2008) 107–115.
[72] A.M. Perez, W. Gao, J.J.F. Lozano, Fuzzy logic energy management strategy for fuel cell/ultracapacitor/battery hybrid vehicle with multiple-input DC/DC converter, in: IEEE Vehicle Power and Propulsion Conference (VPPC '09) 7-10 Sept. 2009, 2009.
[73] A.D. Napoli, F. Crescimbini, L. Solero, F. Caricchi, F. G. Capponi, Multiple-input DC- DC power converter for power-flow management in hybrid vehicles, in: 37th IAS Annual Meeting Conference Record of the Industry Applications Conference, 2002.
[74] A.K. Kaviani, G.H. Riahy, S.H.M. Kouhsari, Optimal design of a reliable hydrogen-based stand-alone wind/PV generating system, considering component outages, Renew. Energy 34 (11) (2009) 2380–2390.
[75] D. Gao, Z. Jin, Q. Lu, Energy management strategy based on fuzzy logic for a fuel cell hybrid bus, J. Power Sources 185 (1) (2008) 311–317.
[76] C.Y. Li, G.P. Liu, Optimal fuzzy power control and management of fuel cell/battery hybrid vehicles, J. Power Sources 192 (2) (2009) 525–533.
[77] Y. Eren, O. Erdinc, H. Gorgun, M. Uzunoglu, B. Vural, A fuzzy logic based supervisory controller for an FC/UC hybrid vehicular power system, Int. J. Hydrogen Energy 34 (20) (2009) 8681–8694.
[78] M.C. Kisacikoglu, M. Uzunoglu, M.S. Alam, Load sharing using fuzzy logic control in a fuel cell/ultra-capacitor hybrid vehicle, Int. J. Hydrogen Energy 34 (3) (2009) 1497–1507.
[79] P. Rodatz, G. Paganelli, A. Sciarretta, L. Guzzella, Optimal power management of an experimental fuel cell/supercapacitor-powered hybrid vehicle, Control. Eng. Pract. 13 (1) (2005) 41–53.
[80] L. Xu, J. Li, J. Hua, X. Li, M. Ouyang, Optimal vehicle control strategy of a fuel cell/battery hybrid city bus, Int. J. Hydrogen Energy 34 (17) (2009) 7323–7333.
[81] V. Paladini, T. Donateo, A. Risi, D. Laforgia, Super-capacitors fuel-cell hybrid electric vehicle optimization and control strategy development, Energy Convers. Manag. 48 (11) (2007) 3001–3008.
[82] G. Liu, J. Zhanga, Y. Sun, High frequency decoupling strategy for the PEM fuel cell hybrid system, Int. J. Hydrogen Energy 33 (21) (2008) 6253–6261.

[83] M. Uzunoglu, M.S. Alam, Modeling and analysis of an FC/UC hybrid vehicular power system using a novel wavelet based load sharing algorithm, IEEE Trans. Energy Conver. 23 (1) (2008) 263–272.
[84] P. Thounthong, S. Rael, B. Davat, Control algorithm of fuel cell and batteries for distributed generation system, IEEE Trans. Energy Conver. 23 (1) (2008) 148–155.
[85] P. Thounthong, S. Rael, B. Davat, Control strategy of fuel cell and supercapacitors association for a distributed generation system, IEEE Trans. Ind. Electron. 54 (6) (2007) 3225–3233.
[86] A. Payman, S. Pierfederici, F.M. Tabar, Energy control of supercapacitor/fuel cell hybrid power source, Energy Convers. Manag. 49 (6) (2008) 1637–1644.
[87] http://www.afdc.energy.gov/vehicles/fuel_cell.html (accessed 23.02.17).
[88] http://www.toyota-global.com/innovation/environmental_technology/fuelcell_vehicle/ (accessed 23.02.17).
[89] https://www.mercedes-benz.com/en/mercedes-benz/innovation/crossing-the-desert-with-the-b-class-f-cell/ (accessed 23.02.17).
[90] http://cafcp.org (accessed 23.02.17).
[91] https://www.mercedes-benz.com/en/mercedes-benz/next/e-mobility/the-fuel-cell-gets-a-plug/ (accessed 23.02.17).
[92] M.J. Kang, H. Park, Impact of experience on government policy toward acceptance of hydrogen fuel cell vehicles in Korea, Energy Policy 39 (6) (2011) 3465–3475.

34

Wireless Charging of Electric Vehicles

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34.1 Introduction to Wireless Electric Vehicles

In this section, a new concept of "wireless electric vehicles (WEVs)," which is coined by the author, is introduced, and wireless power transfer (WPT) technologies including inductive power transfer (IPT) and capacitive power transfer (CPT) are explained. Then, introduction to electric vehicles (EVs) is briefly provided.

34.1.1 The Needs for Wireless Electric Vehicles

Why most people are still not daily driving an electric vehicle?

As a customer, I feel that EVs are still very expensive and inconvenient compared with existing conventional internal combustion engine (ICE) vehicles. The structure of an EV is relatively simple and easy to have maintenance; however, it is not cheap and heavy because of its onboard batteries. Still, most EVs have much shorter driving distance for a full charge compared with ICE vehicles.

Therefore, it can be said that EVs have not been widely commercialized because of battery and charging problems, as shown in Fig. 34.1.

Remark that battery EV (BEV) had been commercialized since the late 19th century, which is about 20 years earlier than the commercialization of ICE vehicles. The original BEVs disappeared from markets because the battery was too heavy, required long time to recharge, had a relatively short driving distance, and was expensive. Amazingly, these problems of battery still exist compared with current ICE vehicles nevertheless the drastic improvement of EV batteries. The expensive price of EVs is mainly due to battery price. The improvement of battery is very slow and does not follow the Moore's law because it is not governed by electronics but governed by chemistry.

Another major obstacle for commercialization of EVs is the charging problem. Even though innovative batteries will become available, still we have charging problems. We should have 30 C (1 C corresponds to the rated power or energy capacity of a battery for an hour) charging capacity in order to recharge an EV in 2 min in case we have such a good battery. For a 50 kWh battery example, which is common to a long-distance EV now, we should have at least 1.5 MW power rating charger and power distribution facility to support it. In practice, we should recharge an EV frequently in order to avoid the battery empty. If a cable charger is used, it is very inconvenient to plug in and plug out daily, and it is potentially

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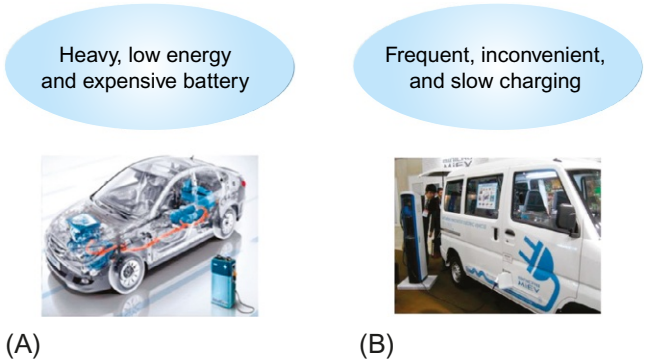


FIG. 34.1 Major obstacles for commercialization of electric vehicles. (A) Battery problems, (B) charging problems.

dangerous to deal with the connector of a cable manually under wet conditions. Currently, a quick charger can recharge an EV battery up to 80% within 20 min, which is still too long time for customers accustomed to 2 min refueling.

Two possible solutions to the abovementioned problems are summarized in Fig. 34.2.

The first solution is to adopt the road-powered EV (RPEV) [1,2] or online electric vehicle (OLEV) [3–19], which does not rely on the battery but gets power directly from roadway power supply rails. This charging method is often referred "the dynamic wireless charging" or simply "dynamic charging" because power is delivered to an EV when it is in motion. An RPEV has a battery for temporary energy storage, but its size is a few times smaller than a BEV, which is not an obstacle for commercialization. As shown in Fig. 34.2A, RPEVs have replaced conventional conductive EVs that have wearable pantographs and cumbersome power lines.

The second solution is stationary wireless charging [20–25], often called as "static charging," by which the inconvenient and dangerous cable charging problems can be completely solved, as shown in Fig. 34.2B. The stationary wireless charging can be applicable to both plug-in EVs (PHEVs) and BEVs. Of course, the slow charging problem cannot be directly solved by the wireless charging, and it must be mitigated by other means such as "interoperable road-powered supply rails [26]," on which this stationary wireless charging is also made together with RPEVs.

I would like to call the stationary and dynamic charging EV solutions as wireless EVs (WEVs), which embrace WPT and wireless communications for EVs. As EVs evolve to information platforms in the future, wireless communications will be essential to every EV, which results in ubiquitously connected cars. WPT will make the WEV complete.

34.1.2 What is Wireless Power Transfer?

In general, the methods of power transfer (PT) can be classified to the stationary PT and mobile PT depending on the movement of loads, as shown in Fig. 34.3. WPT is nowadays the most preferable way of mobile PT that embraces inductive PT (IPT), capacitive PT (CPT), radio-frequency PT (RFPT), and optical PT (OPT), whereas the wired PT can also provide power over a flexibly long distance if properly designed. Currently, IPT is the most widely used one among WPTs, which will play a significant role in realization of the Internet of things (IoT), comprising of digital communication devices, sensors, software, and power sources.

An experiment kit, for example, WPT, is shown in Fig. 34.4, where two air coils are used to transfer power "wirelessly" through "magnetic coupling" or "inductive coupling" of the coils and compensation capacitors are used to nullify the reactance of LC resonant circuits. An inverter is used to provide high-frequency AC current to a transmitter (Tx) coil, and a load transformer is used to adapt the induced voltage of a received (Rx) coil to a load voltage level.

What do you think about the characteristics that a WPT system should have?

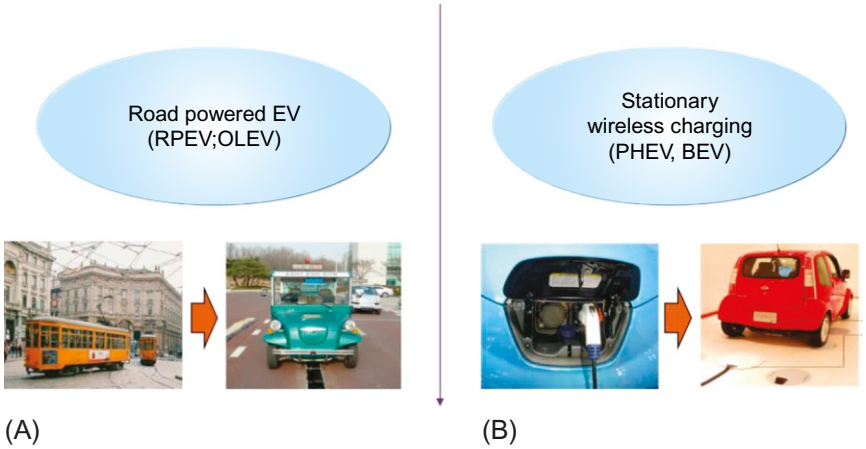


FIG. 34.2 Two possible solutions for current electric vehicles. (A) Road powered EVs, (B) wireless charging.

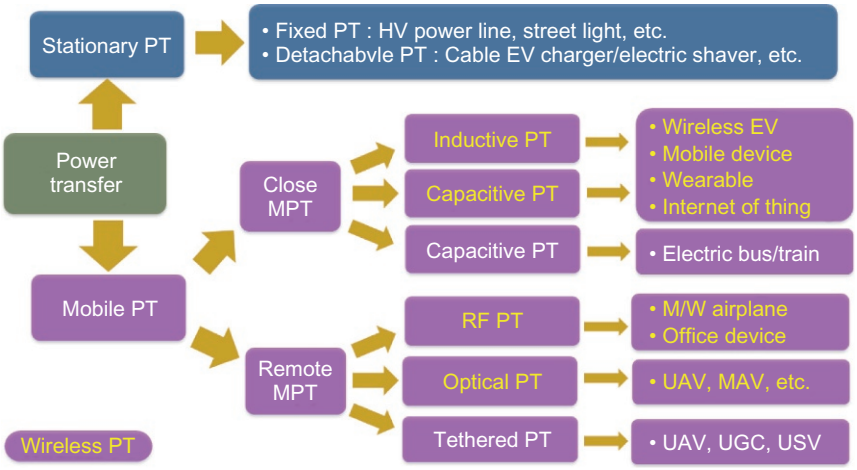


FIG. 34.3 Classification of power transfer method.

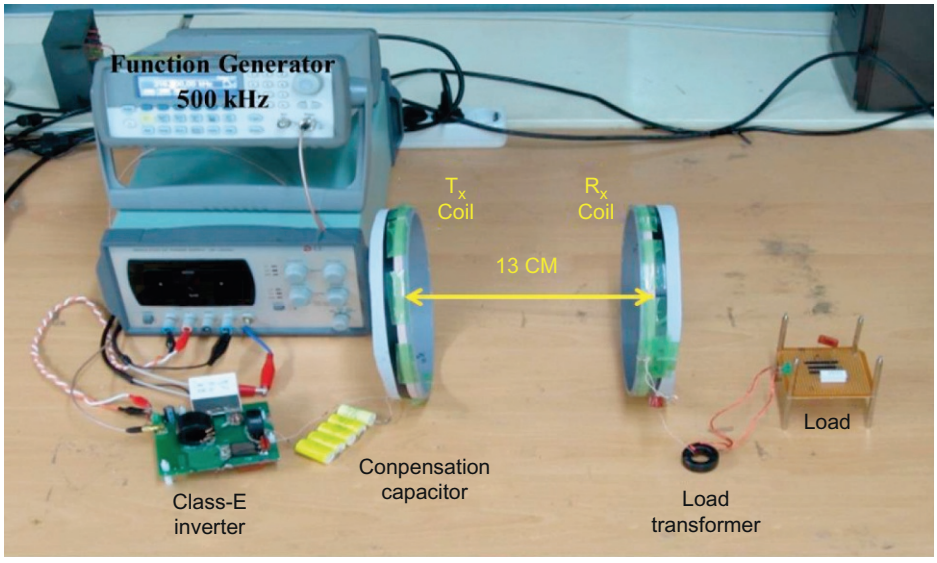


FIG. 34.4 An example IPT of a WPT system consists of two coils operating at 500 kHz switching frequency.

First, the delivered power level for a load should be enough, and its power efficiency should be also high enough not to generate excessive heat and waste electric energy.

Second, the cost, mass, and volume of a WPT system are quite often problems compared with existing wired solutions.

Third, system resilience against resonance parameter changes, load changes, input voltage changes, proximity object movement, electromagnetic interference (EMI), and environment changes such as temperature, humidity, vibration is found to be very important in a WPT system.

Fourth, system dynamics such as response time, stability, and dynamic operating range should be met.

Fifth, accommodation, deployment, and user interfaces of a WPT system should be well considered from design phase for a successful development.

The abovementioned aspects of a WPT system are not necessarily in the order of importance, and they are strongly correlated with each other. Like other systems, the WPT system is a complex system of mechanical and electric compartments, and the design of a WPT system requires comprehensive trade-offs among the requirements. It can be said that the development of a WPT system is not a systematic science but an art of system engineering.

34.1.3 Introduction to Inductive Power Transfer

In general, it can be said that the IPT is governed by Ampere's law and Faraday's law among four Maxwell equations, as shown in Fig. 34.5. The governing equations of IPT in the

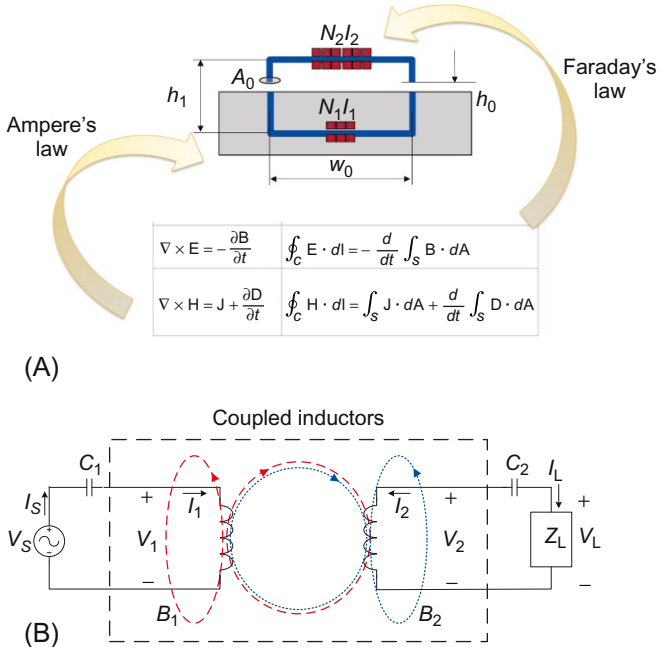


FIG. 34.5 The fundamental principle of IPT. (A) Governing equations of IPT in general, (B) an equivalent circuit of an IPT system in phasor domain, including compensation circuits in the steady state.

steady state for a sinusoidal magnetic field, electric field, and current density at low frequency are approximated by letting $\boldsymbol{D}=0$ as follows:

$$\nabla \times \mathbf{H} = \mathbf{J} \quad \text{(Ampere's law)} \tag{34.1a}$$

$$\nabla \times \mathbf{E} = -j\omega\mathbf{B} \quad \text{(Faraday's law)}. \tag{34.1b}$$

The principle of IPT power delivery can be sequentially explained as follows:

(1) Time-varying magnetic flux is generated from the Tx coil according to Ampere's law.
(2) Induced voltage is generated at the Rx coil according to Faraday's law, where magnetic flux comes from the Tx coil.
(3) Induced voltage, called back emf (counter electromotive force), is also generated at the Tx coil by the Rx coil current.
(4) Power is provided to the Tx coil and fetched from the Rx coil; thus, wireless power is delivered through the coils.

As identified from the above four steps, the IPT is essentially a transformer. A major difference from an ideal transformer, however, is relatively large leakage inductances at both the primary and secondary sides because of weakly coupled inductors. This is why we need the capacitors, as shown in Fig. 34.5B, which are mostly used to compensate the reactance of corresponding leakage inductances. Depending on the source and load types, the compensating capacitors can be connected in series or parallel; Fig. 34.5B shows a series-series (S-S) compensation example.

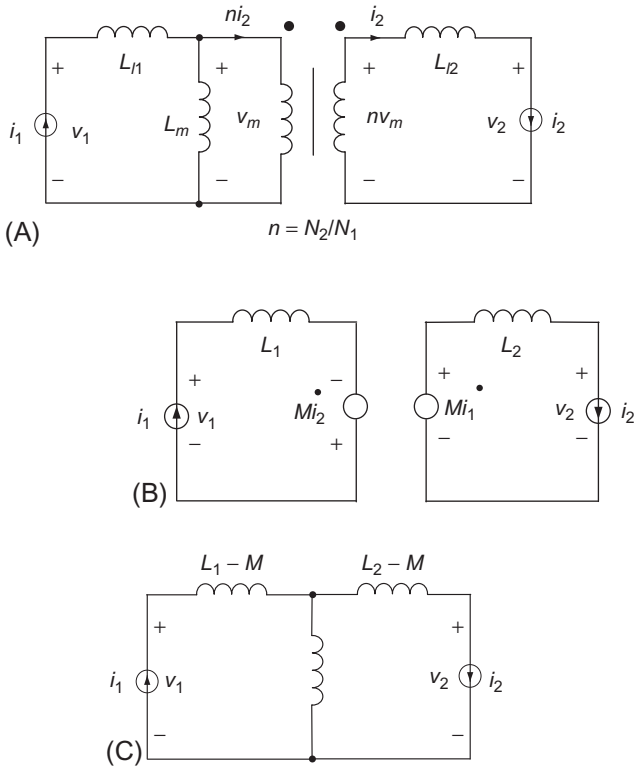


FIG. 34.6 Equivalent circuit models for two coupled coils. (A) Transformer model, (B) M-model, (C) T-model.

For the circuit level analysis of IPT, an equivalent circuit for the coupled inductors in the dotted box of Fig. 34.5B is highly needed. There are three equivalent circuit models widely used for the coupled inductors in IPT, as shown in Fig. 34.6. As shown in Fig. 34.6A, the transformer model is convenient for designing parameters when explicit circuit variables are sought for. The mutual coupling model (M model) of Fig. 34.6B is conveniently used when each side is regarded as an inductor and a back emf voltage source, which represents mutual inductive coupling. Though the trivial galvanic isolation is not countered, the most simplified IPT model would be the "T"-shape model (T model), as shown in Fig. 34.6C, which comprises three inductors only and does not apparently show any turn ratio. Note that the three models are valid not only in the steady state but also in the transient state [27].

The governing equations for the transformer model and M model can be related as follows:

$$v_1 = L_{l1}\dot{i}_1 + L_m\left(\dot{i}_1 - n\dot{i}_2\right) = \left(L_{l1}+L_m\right)\dot{i}_1 - nL_m\dot{i}_2 \equiv L_1\dot{i}_1 - M\dot{i}_2 \tag{34.2a}$$

$$\begin{aligned} v_2 &= \left(nL_m\dot{i}_1 - n^2L_m\dot{i}_2\right) - L_{l2}\dot{i}_2 \\ &= nL_m\dot{i}_1 - \left(n^2L_m + L_{l2}\right)\dot{i}_2 \equiv M\dot{i}_1 - L_2\dot{i}_2 \end{aligned} \tag{34.2b}$$

$$\because M \equiv nL_m, \quad L_1 \equiv L_{l1} + L_m, \quad L_2 \equiv L_{l2} + n^2L_m. \tag{34.2c}$$

Note that the upper dot of a variable is the time derivative of the variable, and the equations are valid for in general.

The T model can be derived from the M model of (34.2) by rearranging terms as follows:

$$v_1 = L_1\dot{i}_1 - M\dot{i}_2 = (L_1 - M)\dot{i}_1 + M\left(\dot{i}_1 - \dot{i}_2\right) \tag{34.3a}$$

$$v_2 = M\dot{i}_1 - L_2\dot{i}_2 = -(L_2 - M)\dot{i}_2 + M\left(\dot{i}_1 - \dot{i}_2\right). \tag{34.3b}$$

34.1.4 Introduction to Capacitive Power Transfer

CPT has not been widely used in WPT compared with IPT due to its low power delivery capacity and high operating frequency. However, CPT has advantages for compact and thin layer applications with low power. The configuration of a CPT system is shown in Fig. 34.7, where other modules are very similar with IPT except for Tx and Rx plates and electric-field-based communication links. The application of CPT to EV is available in a few literatures [25].

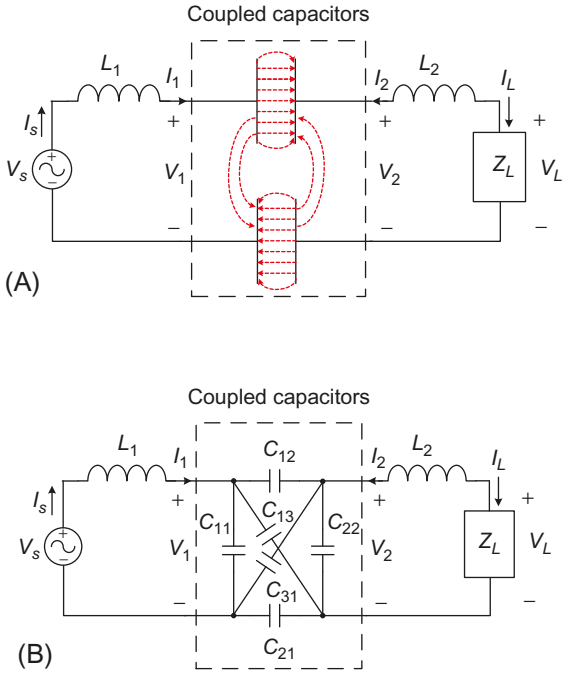


FIG. 34.7 An equivalent CPT system in the phasor domain, including compensation circuits in the steady state. (A) Distributed capacitance model with electric field distribution, (B) lumped capacitance model with six capacitances.

34.1.5 Introduction to Electric Vehicles

Generally speaking, an EV comprises a conventional car body, and EV-specific components such as energy refuel equipment (electric chargers), onboard energy storage (batteries), power converters (inverters and rectifiers), and locomotive (electric motors and transmissions), as shown in Fig. 34.8.

It is instructive to find the analogy between EVs and ICE vehicles: electric charger versus fueling station, battery versus fuel tank, inverter versus fuel injector, and electric motor versus ICE [28].

Depending on the energy source/refueling method, EV-specific components mentioned above, and various applications, EVs can be classified into many categories. EVs can be classified, according to energy source or energy refueling method, as wired power EVs, wireless-powered EVs (WEVs), solar- or RF-powered EVs, and battery-swap EVs. Depending on the onboard energy sources, EVs can be classified as ICE-powered EVs, called hybrid EVs (HEVs) or plug-in hybrid EVs (PHEVs), fuel-cell-powered EVs (FCEVs), and even nuclear-powered EVs though not likely to be commercialized in the near future. EVs can be also classified into applications such as ground (road and rail), aerial, sea (ship/underwater), and space EVs.

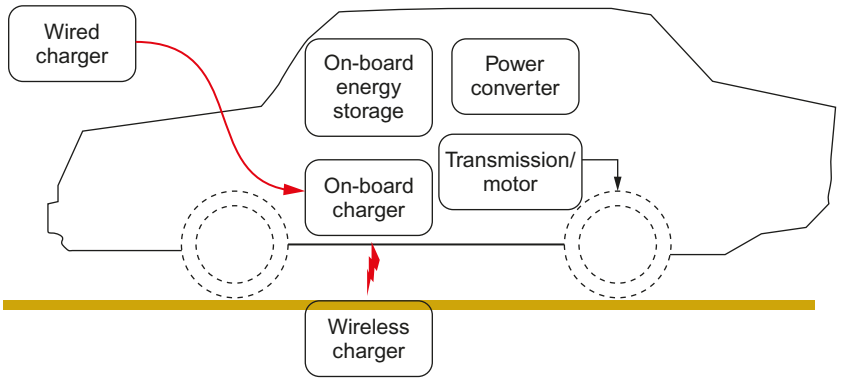


FIG. 34.8 A general configuration of EV, charged by both wired and wireless chargers example.

34.2 Static Inductive Charging of Battery Electric Vehicles

In this section, it is explained how IPT is applied to the static chargers for EVs such as BEVs and PHEVs.

34.2.1 Overview of Static EV Chargers

Because automatic refueling of a vehicle is a wonderful thing for the person, boring of repeated daily cable charging of EVs, static EV chargers of this category are expected to be widely used in the near future. As identified from recently developed autonomous vehicles and self-controlled vehicles, future vehicles will be not only transportation tools but also information platforms. EVs are inherently the most electrified vehicles, which make the information platform be possible.

Among numerous static EV chargers, a few implemented examples are shown in Figs. 34.9 and 34.10.

A static EV charger can be decomposed into a Tx subsystem on ground and an onboard Rx subsystem. The system requirements of a static EV charger include cost, reliability, lifetime, availability, power, efficiency, tolerances (height, longitudinal, and lateral), electromagnetic field (EMF), foreign object detection (FOD), and robustness against mechanical shock for a given source and load conditions, air gap, load change, and operating temperature. Hardware and software implementation issues such as insulation, waterproof, user interface, monitor, communications, and information are also important for the development of the system. Standardization and regulation issues are crucial for commercialization.

34.2.2 Coil Design Issues

Coil design would be the most substantial part of IPT system design because the Tx coil and Rx coil determine power transfer performances such as output voltage, power level, coil-to-coil efficiency, and height/lateral tolerances. The configuration of a static charger includes Tx and Rx windings and cores, as shown in Fig. 34.11. The goal of coil design is to focus magnetic field from the Tx to Rx coils so that leakage flux is minimized to lower EMF. In detail, to design the coil is to determine the ampere-turns (N_1, N_2, I_1, and I_2) and detail dimensions of coils for a given air gap, width of coil, operating frequency, power supply voltage, delivered output power, and ambient operating temperature (h_s, w_p, f_s, V_s, P_o, and T).



(A) (B)

FIG. 34.9 Static EV chargers of 30–150 kW level at bus stops, deployed in Waseda University, Japan. (A) Deployed bus, (B) deployed Tx subsystem.



(A) (B)

FIG. 34.10 Static EV chargers of 3.3–6.6 kW level for passenger cars at parking area, deployed in Jeju Island, Korea. (A) Before charging, (B) being charged.

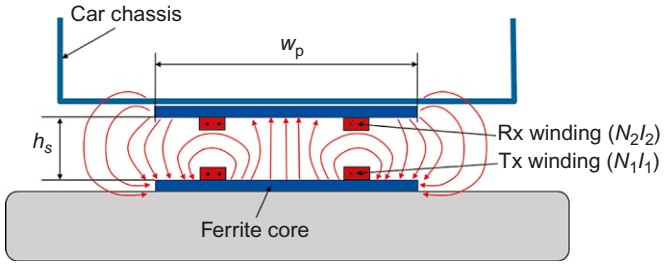


FIG. 34.11 Configuration of Tx and Rx coils of a static EV charger when Tx coil is energized and Rx coil current is zero.

There are a few decision issues in the design of Tx and Rx coils of static EV chargers. One of them is the coil shape, as shown in Fig. 34.12. The merits of the two types are listed below. The thick arrows depict lateral tolerances of two directions: the larger the arrow length, the bigger the tolerance. "S" and "N" denote magnetic polarity. There could be other shapes such as round shape, which is basically rectangular but its corners are round, and octagonal shape. Basically, the shape of the coil is largely governed by the shape of the mother body, that is, a car underbody, depending on applications.

As shown in Fig. 34.13, the lateral tolerance of a dual-pole coil could be better than that of a single-pole coil because the number of magnetic pole is only two for the dual-pole coil. The demerits are written in italic letters in Fig. 34.13.

You should also determine the coil type depending on magnetic field shape you want, as shown in Fig. 34.14, where loop coil and dipole coil examples are selected. For a given size of the Tx and Rx coil, the dipole coil has larger lateral tolerance in side direction but has large EMF that needs more magnetic shield.

The core could be dense or sparse structures, as shown in Fig. 34.15. Note that the total amount of core use could be unchanged by the average density of core if the core thickness of dense core structure is optimized. If not the case, the core use of sparse structure tends to be smaller than the dense structure.

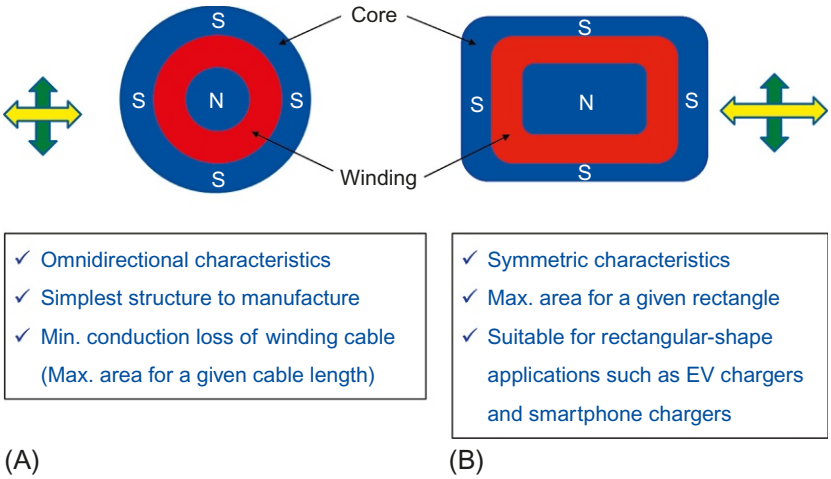


FIG. 34.12 Shape of Tx and Rx coils (plane view). (A) Circular, (B) rectangular.

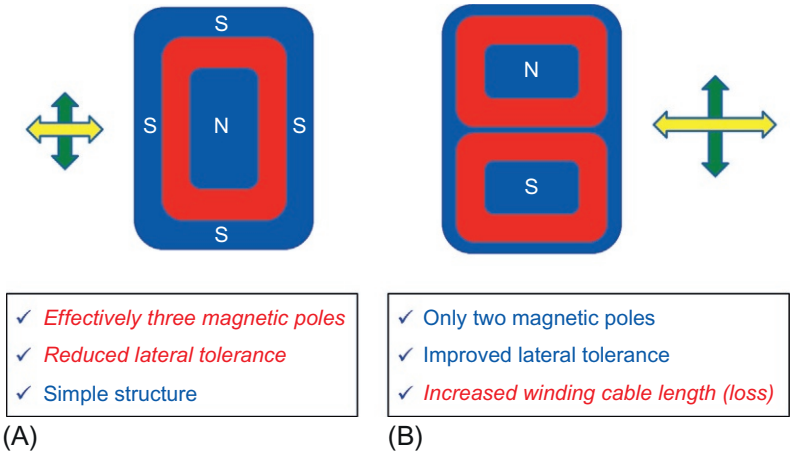


FIG. 34.13 Number of poles in Tx and Rx coils (plane view). (A) Single pole, (B) dual pole.

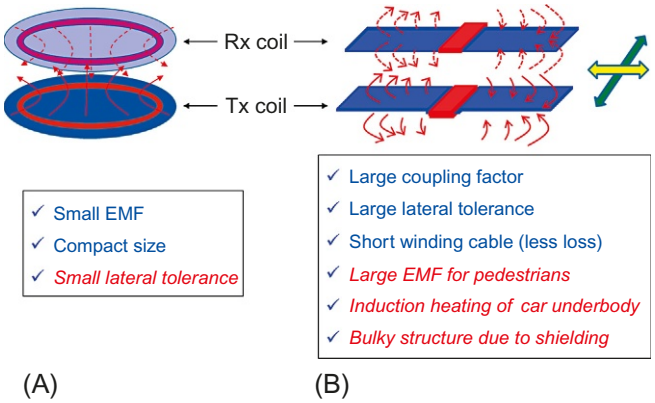


FIG. 34.14 Magnetic field shape of Tx and Rx coils (bird's-eye view). (A) Loop coil, (B) dipole coil.

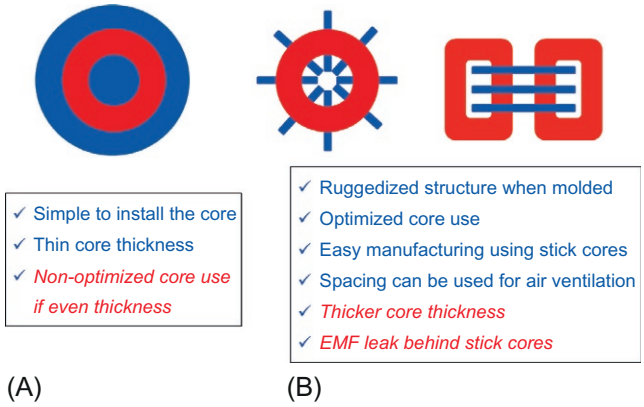


FIG. 34.15 Core structure of Tx and Rx coils (plane view). (A) Dense core structure, (B) sparse core structures.

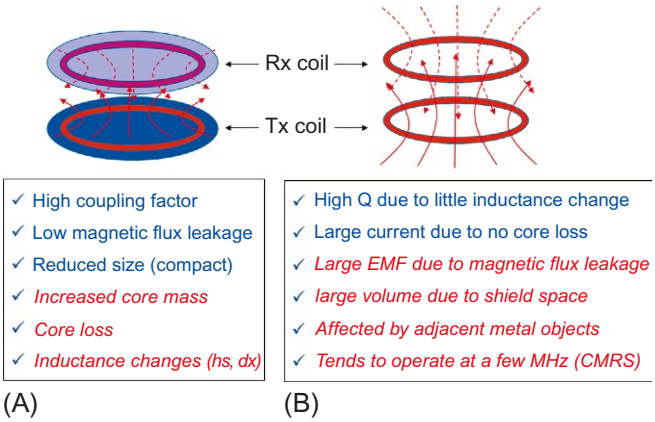


FIG. 34.16 Core use of Tx and Rx coils (bird's-eye view). (A) With core, (B) coreless.

Another category of core structure is the use of core, as shown in Fig. 34.16. Core is not necessarily always used, especially when the operating frequency is too high to use any core, as shown in Fig. 34.16B. Note that the coreless coil is quite often referred as the coupled magnetic resonance system (CMRS),

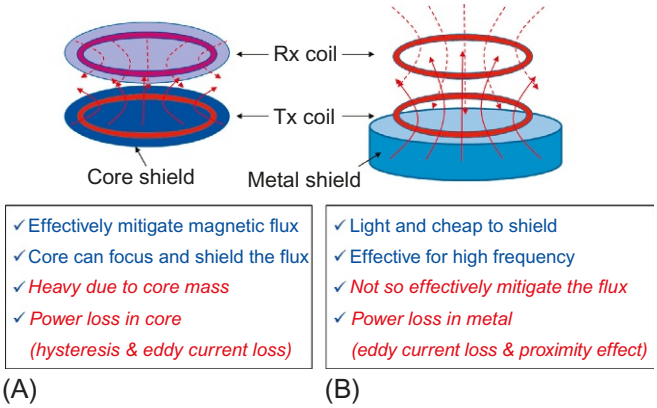


FIG. 34.17 Magnetic field shield of Tx and Rx coils (bird's-eye view). (A) Core shield, (B) metal shield.

whereas the coil with core is called conventional inductive power transfer system (IPTS). The beginner who studies CMRS often thinks that it is quite different from IPTS due to its inherent large Q and no change of primary and secondary inductances against air-gap change. The wonderful characteristics of CMRS, however, do not come from its resonant type but come from its coreless structure, as the author announced at the Special Session of Wireless Power Transfer of the 2013 IEEE ECCE conference. As an evidence, 5 m-long-distance IPTS was built and first demonstrated that long-distance WPT is possible not only by CMRS but also by IPTS [29]. As denoted in Fig. 34.16, there are a lot of penalties for the coreless structure.

We have two shielding methods: core shield and metal shield, as shown in Fig. 34.17. Both shields are often used to enhance magnetic shielding effect. Note again that there are not many theories available for metal shield design compared with core shield design.

34.2.3 Misalignment Issues

A very important and difficult problem in IPT design is position tolerance issue arising from air-gap change and misalignments between Tx and Rx coils, as shown in Fig. 34.18. As the coils are misaligned each other, induced voltage drops in general, and resonant frequencies of Tx and Rx sides usually change as well. Therefore, the position tolerance affects to not only coil design but also compensation circuit, controller, and converter designs such as power rating, zero voltage switching (ZVS) condition, and power factor.

34.3 Dynamic Inductive Charging of Road Powered Electric Vehicles

In this section, the WPT system (WPTS) for RPEVs is explained. Most recently commercialized OLEVs including narrow-width power rails of I-type and ultraslim power rails

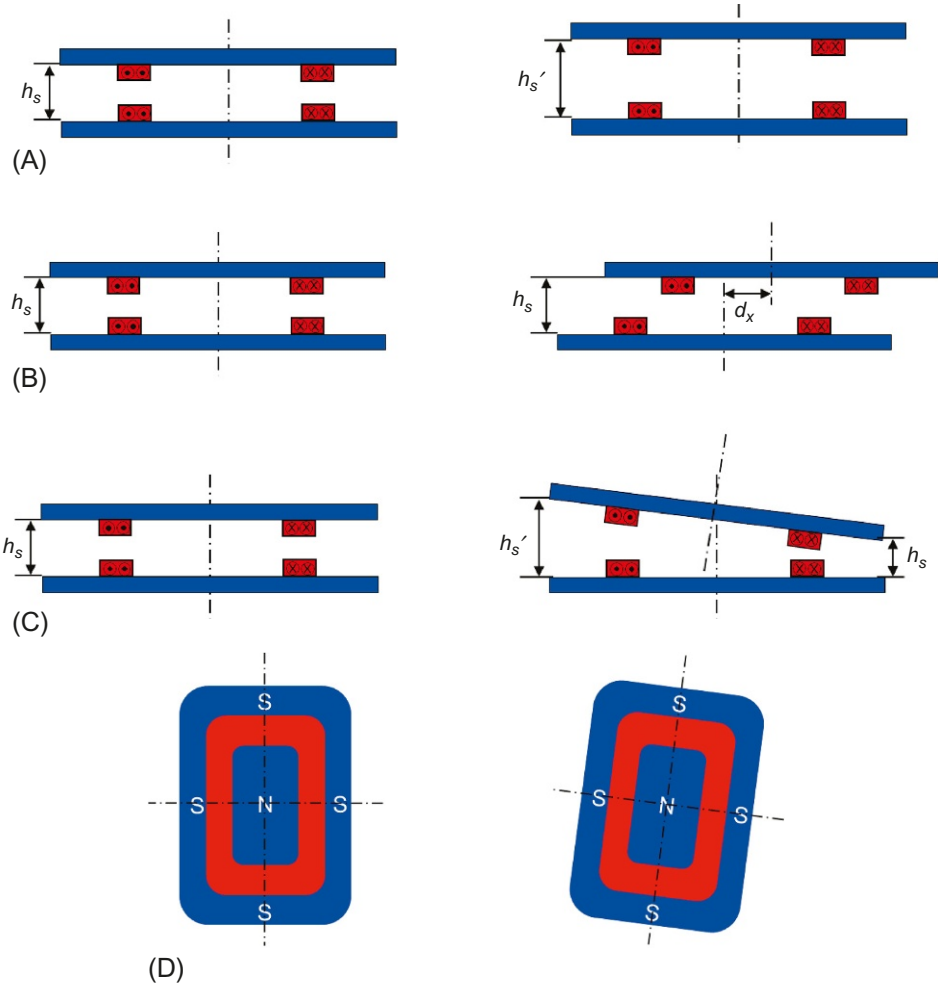


FIG. 34.18 Position tolerance problem, arising from relative position changes of Tx and Rx coils. (A) Airgap change (side view), (B) lateral misalignment (side view), (C) tilt misalignment (side view), (D) rotation misalignment (plane view).

of S-type are explained, where the width of power rail is important in road construction of infrastructure for RPEVs.

34.3.1 Overall Configuration of RPEVs

The WPTS for an RPEV should be capable of delivering high power efficiently through a moderate air gap for avoiding collisions between the RPEV and ground. The WPTS is composed of two subsystems: One is the roadway subsystem for providing power, which includes a rectifier, a high-frequency inverter, a primary capacitor bank, and a power supply rail, and another is the onboard subsystem for receiving power, which includes a pickup coil, a secondary capacitor bank, a rectifier, and a regulator for battery, as shown in Fig. 34.19. The roadway subsystem should be so robust and cheap that it may withstand severe road environments for a lifetime of an EV and should be economic to install over a long distance, whereas the onboard subsystem should be compact in size and light in weight so that it may be adopted into the RPEV.

An example overall circuit diagram of an IPTS developed for OLEVs is shown in Fig. 34.20, where the inverter provides constant current to the Tx power rail by a feedback control.

The overall system breakdown of an RPEV mission system is shown in Fig. 34.21, which is drawn, reflecting the experience of developing OLEV systems by the author. The RPEV mission system includes not only the WPTS system but also the control system and EV system. The control system is unique and crucial for RPEV because it senses and identifies the EV and then appropriately turns on and off the inverters. Moreover, it monitors the health of IPTS and RPEV and provides accounting service and communication links.

IPTS for RPEV is differentiated from conventional IPTS for stationary charging because additional requirements such as larger lateral tolerance, higher air gap, and lower construction cost should be considered for dynamic charging [3–19]. Moreover, IPTS for RPEV should survive from harsh road conditions such as extremely high and low temperatures, high humidity, and repetitive mechanical shocks for at least 10 years. Basically,

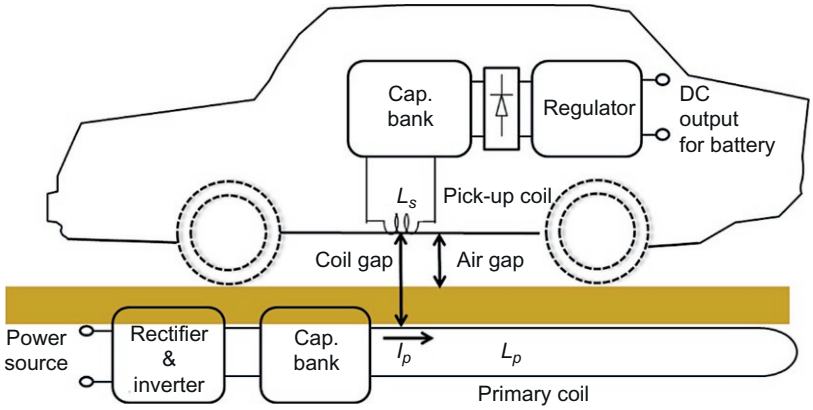


FIG. 34.19 Overall configuration of an RPEV.

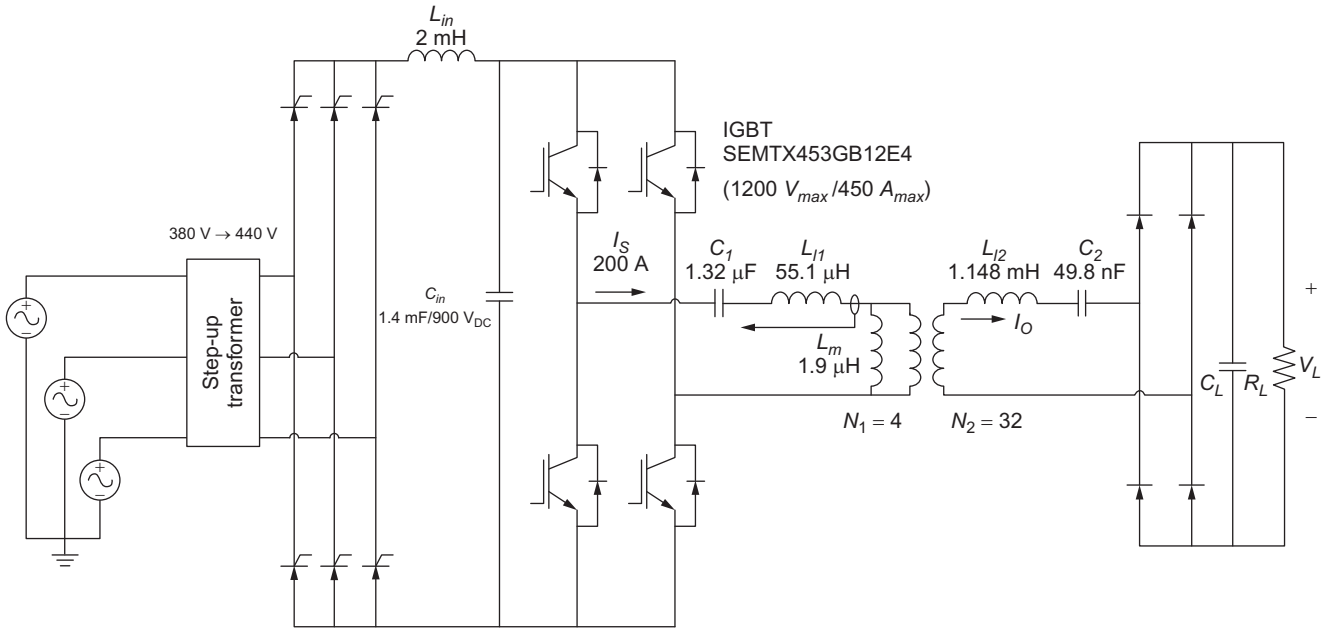


FIG. 34.20 Overall circuit diagram of the IPTS for OLEVs (an example).

the high-voltage power rail under a road should be electrically and mechanically protected well, but electricity under the conditions of a wet and fragile structure is not compatible with a road, in general. Therefore, it is quite challenging to build the roadway subsystem robustly. On the other hand, the onboard subsystem should also survive from the harsh road conditions and vibrating RPEV operating conditions, where strict technical and legislative regulations for vehicles should be met.

34.3.2 Design Issues of Dynamic Inductive Charging

The design goals of IPTS are summarized as follows:

(1) To increase magnetic coupling as much as possible so that higher induced voltage can be obtained.
(2) To increase power efficiency for a given power capacity, device ratings, and cost.
(3) To make modules as compact as possible to accommodate for a given space and weight.
(4) Not to increase or cancel out EMF.
(5) To manage resonance frequency variation and coupling factor change due to misalignment of pickup position, air-gap change, and even temperature change.

In order to meet the design goals, several important design issues of the IPTSs, which are unique for RPEVs, should be resolved as follows:

1. *Switching frequency*: The switching frequency of the inverter and rectifier of an RPEV governs overall performances. As the switching frequency f_s increases, the coil

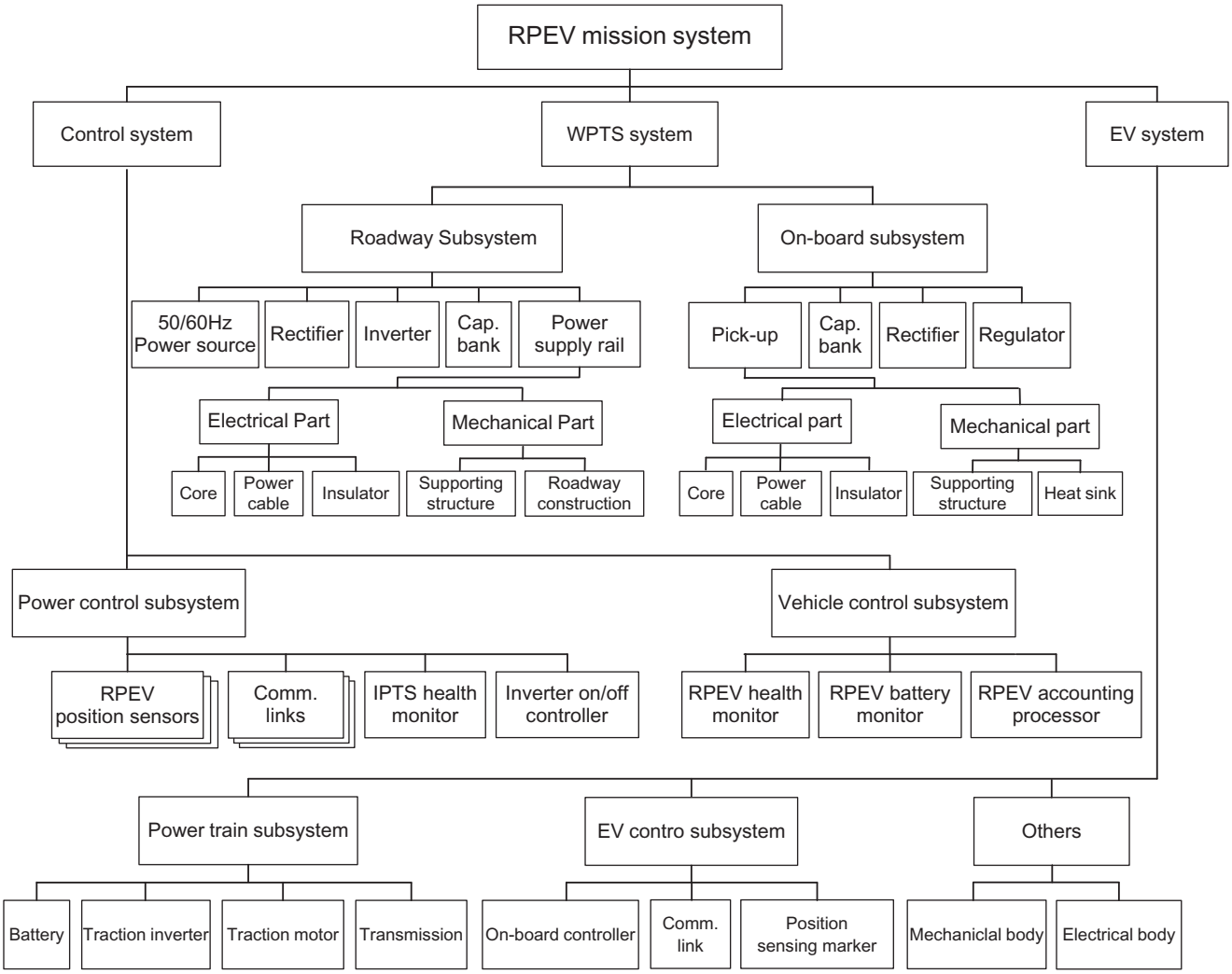


FIG. 34.21 Overall system breakdown of an RPEV.

and capacitor size decreases for the same required power, but the switching loss and core loss as well as the conduction loss of wires due to the skin effect increase. In the case of the switching frequency lower than 20 kHz, acoustic noise may be a problem [1]. Another unique feature of RPEVs concerning frequency is the increased voltage stress in a distributed power supply rail V_{l1} for higher switching frequency, which is proportional to the frequency and line current I_s as follows:

$$V_{l1} = j\omega_s L_{l1} I_s \tag{34.4a}$$

$$\frac{\partial V_{l1}}{\partial x} = j\omega_s I_s \frac{\partial L_{l1}}{\partial x}. \tag{34.4b}$$

Because of these restrictions, the switching frequency tends to be no less than 20 kHz but not far beyond 50 kHz. For OLEVs, the frequency was finally selected as 20 kHz after examining for 20 kHz, 25 kHz, and 30 kHz.

The interoperability of IPTS between RPEVs and stationary wireless EVs is an important issue that needs further study because the design of IPTSs for RPEVs is not a direct extension of that of stationary chargers. The design goals of IPTS of RPEV such as low infra cost, high power, continuity of power delivery, and low fluctuation during in-motion are not so important for stationary chargers.

2. *High power and large current*: In addition to the high operating frequency of RPEVs, high power of hundreds of kW with large current of hundreds of A makes it difficult to handle cables, converters, and devices. For example, a Litz wire of 300 A rating with 20 kV insulation capability is not commercially produced. Capacitors and IGBTs, which have high voltage and large current ratings with an operating frequency higher than 100 kHz, become scarce. Furthermore, all the inverters, rectifiers, coils, capacitors, and cables used in the IPTS of RPEV are operated outdoors, where debris and salty and wet material may damage them.

3. *Power efficiency*: In order to make RPEV competitive against internal combustion engine vehicle (ICEV), the power efficiency or energy efficiency should not be too low. The bottom line of the overall power efficiency, which is defined from the AC power source to the DC output power for battery, would be about 50%, considering grid loss and fuel cost. Fortunately, modern IPTSs have fairly good power efficiency larger than 80%. More importantly, power loss rather than power efficiency is a serious problem in designing the inverter and pickup due to over temperature.
4. *Coil design*: In order to focus magnetic field for Tx and Rx coils and to mitigate magnetic leakage flux so that large induced voltage and low EMF level can be achieved, a novel coil design is crucial for IPTS. This design is unique for the roadway subsystem in that the cost per km is critical; therefore, the roadway power supply rail should be cheap enough not to deteriorate the economic feasibility of overall RPEV solution, whereas the pickup should be neither heavy nor thick so that it can be successfully implemented on the bottom of an RPEV.
5. *Insulation*: In order to guarantee stable operation of IPTS, a few kV level insulations of the roadway subsystem and onboard subsystem should be provided. The insulation of a roadway power supply is of great importance because high voltage is induced along through the distributed power rail over a road rather than over a point and is increased by the back emf of the pickup coil abruptly displaced on the power supply rail. The insulation of the pickup coil is also an important issue when high power output is sought because the large output current of the pickup coil induces high voltage, which could be as much as 10 kV if not appropriately mitigated.
6. *Segmentation of power supply rail*: RPEV typically requires many IPTS along a road because a power supply rail cannot be infinitely deployed. It should be segmented so that each segment can be independently turned on and off. The length of a power supply rail is an important design issue because it would be too expensive if the length is very short due to an increased number of inverters and switch boxes, whereas the power loss would be too large if the length is very long due to increased resistance. Besides these issues, the amount of cable use, EMF level, and car length should be considered when determining the segmentation scheme.
7. *Roadway construction*: In order to minimize traffic obstruction, the roadway construction time of IPTS should be as short as possible. Moreover, there are numerous difficulties in roadway work because of debris and dirt. Keeping all of the electric components of IPTS clean during roadway construction for a few days or weeks is a serious problem in practice. There should be a smart way to overcome these problems.
8. *Resonant frequency variation*: The resonant frequencies of the roadway subsystem and onboard subsystem are significantly varied as the magnetic coupling between a power supply rail and a pickup changes due to air-gap change, lateral misalignment, and longitudinal movement. Moreover, the frequency changes are different from time to time for different cars and different numbers of cars on a power supply rail. There should be either the smart coil design or inverter design to cope with these frequency changes or *in situ* frequency tuning capability.
9. *Control of dynamic resonating circuits*: The resonant circuit, as shown in Fig. 34.20, has finite dynamic response times and may arise high voltage and current peaks that can destroy electric devices. They should be moderately controlled so that the voltage and current level can be mitigated, where the frequency response of AC circuits can be managed with the recently developed Laplace phasor transformation [30,31]. A resonating LC circuit has a first-order response in the dynamic phasor domain [32]; hence, high-order IPTS with more than two resonating circuits can be managed with the general phasor transforms [33,34].

After the two frontier projects of RPEV, the Partners for Advanced Transit and Highways (PATH) program began in 1992 to determine the technical viability of RPEV in the University of California, Berkeley. Throughout the PATH program, broad research and field tests on RPEV, as shown in Fig. 34.22, including designs of IPTS, installations of an IPTS to a bus, road constructions of power supply rails, and environmental impact studies, were performed. The PATH team achieved an efficiency of 60% at an output power of 60 kW with a 7.6 cm air gap [1].

The PATH program, however, had not been successfully commercialized due to high-power rail construction cost of around 1 M$/km, heavy coils, and acoustic noises, as well as relatively low power efficiency and large primary current of thousand amperes owing to a low operating frequency of 400 Hz. Furthermore, the small air gap does not meet road safety regulations, and lateral displacement of less than 10 cm is not acceptable for practical use. Despite the limitations for practical applications, the PATH team's work was well documented and stimulated subsequent research and development on modern RPEVs.

34.3.3 Developments of On-Line Electric Vehicles

34.3.3.1 Overview of OLEV

A stream of modern RPEVs is the OLEV, which has solved most of the remaining problems of the PATH team's work, as shown in Fig. 34.23. The OLEV project has started since 2009 by a research team led by KAIST, including the author, Korea [3–19]. Innovative coil designs and roadway

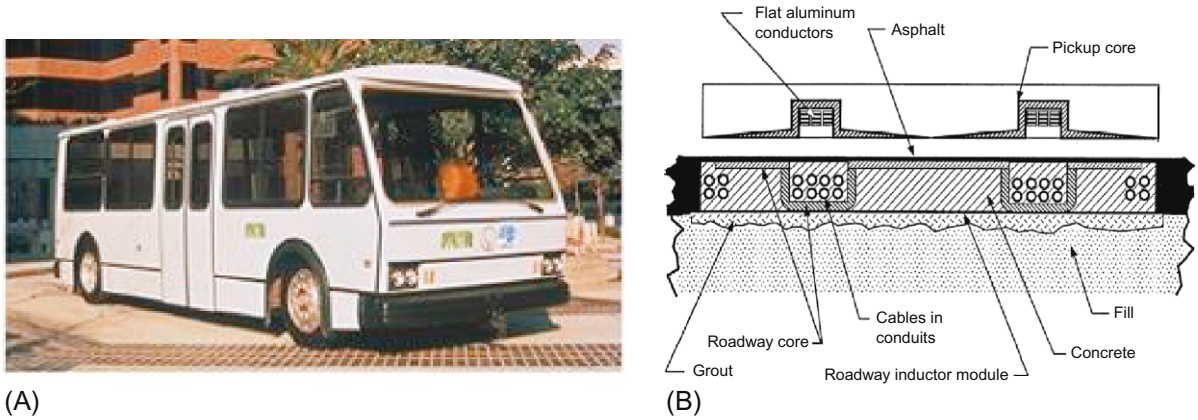


FIG. 34.22 The first operational prototype RPEV developed by the PATH team in the 1990s. (A) Appearance of the developed RPEV bus, (B) prototype coils of the IPTS.

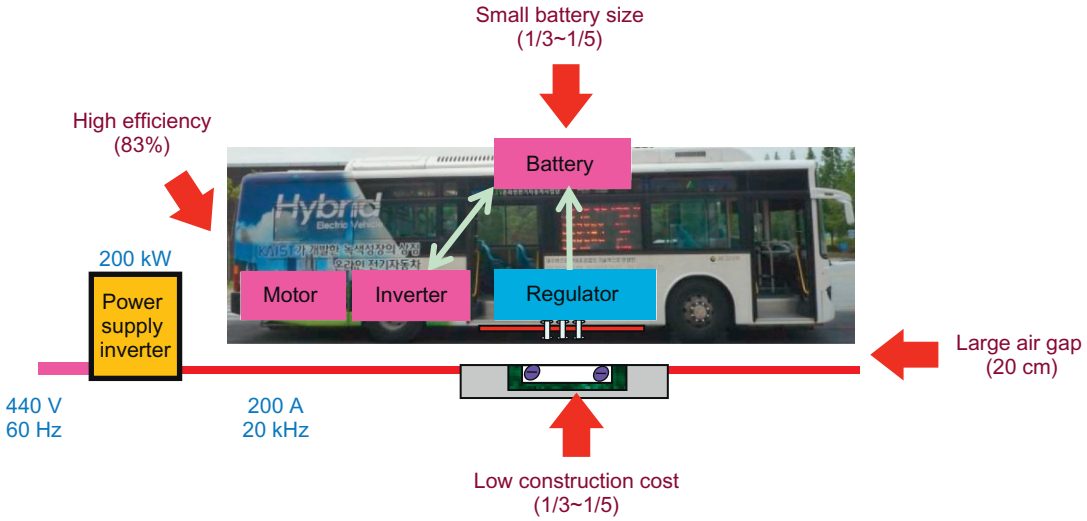


FIG. 34.23 The development concepts of the OLEV bus developed by KAIST.

construction techniques and all of the systems operating at a reasonably high frequency of 20 kHz made it possible to achieve the highest power efficiency of 83% at an output power of 60 kW with a large air gap of 20 cm and a fairly good lateral tolerance of 24 cm. Moreover, the power rail construction cost of the OLEV, which is responsible for more than 80% of the total deployment cost for RPEVs, has been dramatically reduced to at least a third of that of the PATH project. The primary current has been also reasonably mitigated as low as 200 A, and the battery size has been significantly reduced to 20 kWh, which can be further reduced by increasing the length of the power supply rails.

The first-generation (1G) concept demonstration car of OLEV, the second-generation (2G) OLEV buses, and the third-generation (3G) OLEV passenger car were developed and extensively tested at the test sites of KAIST since 2009, and three OLEV trains (3^+G) had been successfully deployed at the Seoul Grand Park, Korea, since 2010. Two upgraded OLEV buses (3^+G) were deployed at the 2012 Yeosu EXPO, Korea, and other two OLEV buses (3^+G) have been in full operation at the main campus of KAIST since 2012. Recently, two OLEV buses (3^+G) were firstly commercialized at a 48 km route in Gumi, Korea. The fourth-generation (4G) OLEV, showing more practical performances such as a very narrow rail width of 10 cm, a larger lateral displacement of 40 cm, lower EMF level, and lower power rail construction cost compared with the previous generation OLEV, has been also developed. The development of the fifth-generation (5G) OLEV is in progress, where an ultraslim S-type power supply coil of 4 cm rail width is proposed for power rail construction with much less cost and time [18,19].

34.3.3.2 2G OLEV

The 2G OLEV, announced on 14 July 2009, focused on drastically improving the air gap of the 1G OLEV without mechanical moving parts and finally achieved a 17 cm air gap, which

meets road regulations, 12 cm in Korea and 16 cm in Japan. At the same time, it achieved a maximum efficiency of 72% and a maximum output power of 60 kW using 10 pickups. The power supply rail, where the width is 1.4 m and the total length is 240 m, is paved with asphalt to provide the same friction force as normal roads. In order to realize the 17 cm air gap, the U-type power supply rail and the flat pickup coil of IPTS have been developed, where the name "U-type" stems from the cross section of the power supply rail, as shown in Fig. 34.24. A pair of return power cables is used to mitigate the EMF from the power supply rail for the ICNIRP guidelines [35,36]. With the U-type power supply rail and I-type pickup coil, it is found that an effective area of the magnetic path between the power supply rail and the pickup coil increases as the air gap increases due to fringe effect, as shown in Figs. 34.24 and 34.25.

The cross section of the core plates of the power rail, as shown in Fig. 34.24, is significantly reduced by using the high operating frequency of 20 kHz, which is 50 times of the PATH team. The reason for selecting 20 kHz is that it is the lowest inaudible frequency, which mitigates the line voltage stress, as in (34.4). The upward magnetic flux generated from the pickup coil was appropriately shielded by an aluminum plate with a 5 cm distance.

34.3.3.3 3G OLEV

The 3G OLEV sports utility vehicle (SUV), announced on Aug. 14, 2009, adopted the W-type power supply rail and the flat pickup with overlapped double coils for higher power and increased lateral tolerance. Thus, the upward magnetic leakage flux from the pickup of 2G OLEV had been drastically mitigated by using the flat pickup core, which prohibits the magnetic flux between the power supply rail and pickup from leaking. The magnetic field shield such as an aluminum plate or additional space is no longer required.

The overall efficiency and air gap of the 3G OLEV were 71% and 17 cm, respectively, which are respectable, but slightly disappointing numbers; therefore, overall systems including a roadway rectifier and inverter, power supply rail, pickup, and onboard regulator were redesigned to achieve a maximum efficiency of 83% with a 20 cm air gap, and this new design was called the $3G^{+}$ OLEV.

The W-type power supply rail, as shown in Fig. 34.26, has many cores of "W" shape, where the total magnetic resistance becomes three-quarters smaller than that of the 2G OLEV for the same air gap, and this eventually leads to the increase of the output power from 6 to 15 kW for each pickup. Moreover, the width of the power supply rail is decreased to 70 cm, which is just a half of that of the 2G OLEV, and it can reduce the deployment cost of OLEV for commercialization. The EMF at 1.75 m distance meets the ICNIRP guideline because the two power cables of opposite polarity of magnetic flux cancel each other out [18,19].

One of the problems found during the development of 2G OLEV was the inherently weak structure of the power supply

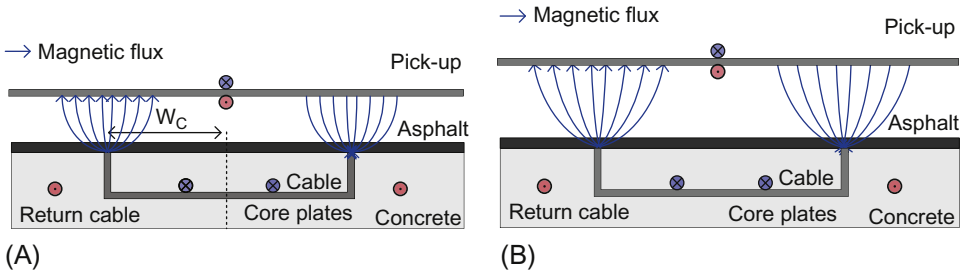


FIG. 34.24 Cross section of the U-type power supply rail and I-type pickup coil. (A) Small air-gap, (B) large air-gap.

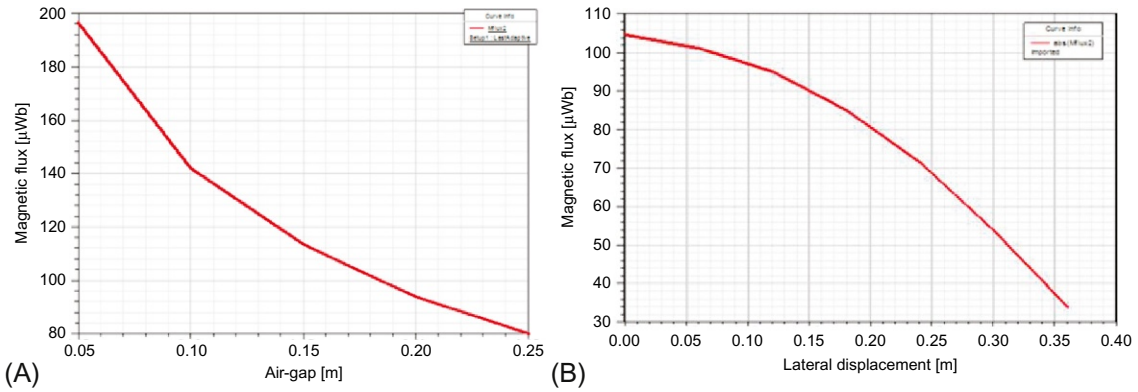


FIG. 34.25 Magnetic flux characteristics of the 2G IPTS [18]. (A) Along the air-gap, (B) along the lateral displacement.

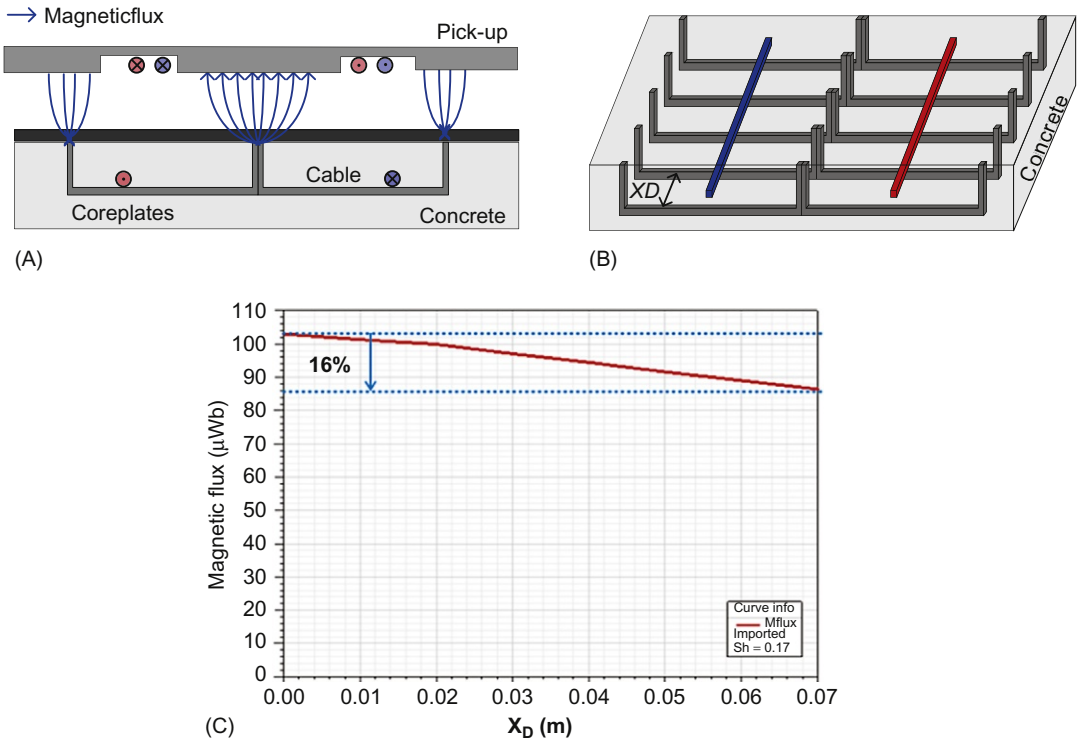


FIG. 34.26 Views of the W-type power supply rail and flat pickup coil [18]. (A) Cross-section view, (B) Bird's eye view of a bone structure, (C) simulated magnetic flux characteristics for different bone core-gap X_D.

rail, where the core separates the concrete into two and undergoes severe mechanical stress from heavy vehicles. As a remedy for this mechanical weakness, bone structure core of the power supply rail, as shown in Fig. 34.26B, has been proposed, where the bone structure core is installed with the bone core-gap X_D. Despite the large gap between cores, the magnetic flux does not decrease considerably, as shown in Fig. 34.26C.

In addition, during power rail road construction, concretes can percolate down through the bone structure cores. Therefore, the power supply rail, which is reinforced with two iron bars and in which power cables are protected by fiber-reinforced plastic (FRP) pipes, has almost the same endurance of concrete, as shown in Fig. 34.27. In practice, roadway construction of the power supply rail takes a few weeks, being affected by weather and debris, and this delay obstructs the commercialization of OLEV.

34.3.3.4 4G OLEV

As shown in Fig. 34.28, the 4G OLEV, announced in 2010, has an innovative I-type structure of a power supply rail with a maximum output power of 27 kW for a double pickup coil having a 20 cm air gap and 24 cm lateral displacement. As shown in Fig. 34.28A, the I-type power supply rail, where the name "I-type" stems from its front shape, has only 10 cm width,

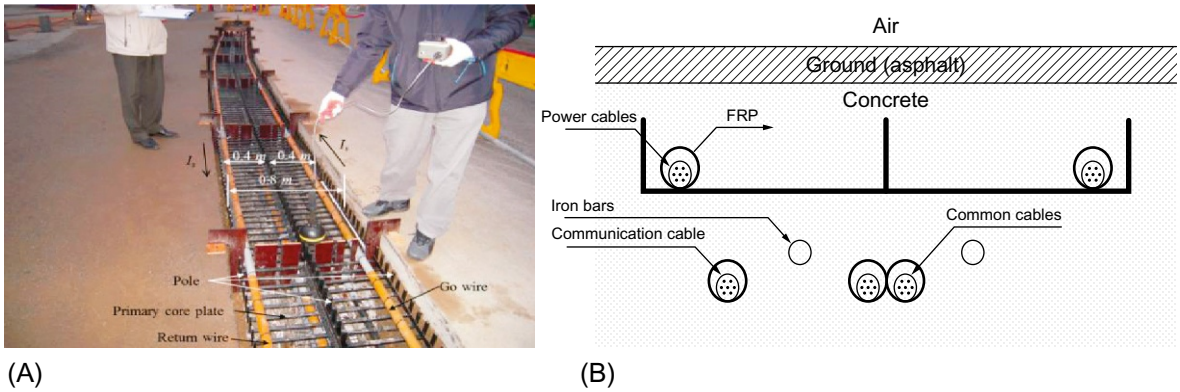


FIG. 34.27 The W-type power supply rail of the 3G OLEV [18]. (A) Under road construction, (B) cross-section view.

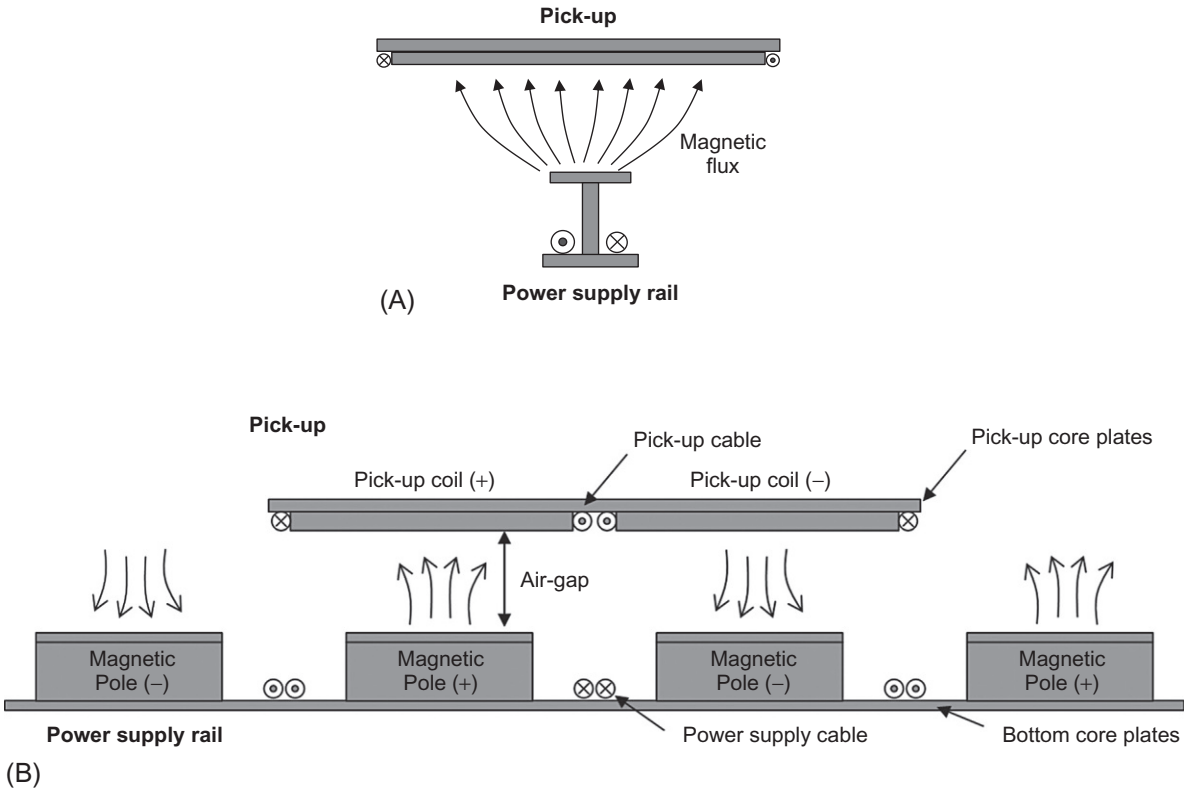


FIG. 34.28 The I-type power supply rail and double flat pickup coil [18]. (a) Front view, (b) side view.

which leads to a deployment cost reduction of 20% compared with the 3G OLEV. Unlike previous generations of OLEV, a very low EMF for pedestrians, as low as 1.5 μT at a distance of 1 m from the center of the power supply rail, can be obtained because the power supply rail has alternating magnetic poles along the road, as shown in Fig. 34.28B.

As shown in Fig. 34.29, the 4G OLEV adopted a module concept for the I-type power supply rail to reduce the deployment time within a few hours, which had been one of the drawbacks of the 3G OLEV. The I-type power supply module, which includes the power supply rail and capacitor banks inside, as shown in Fig. 34.29A, should be robust to high humidity and external mechanical impacts at least for 10 years, for example.

34.3.3.5 5G OLEV

To further reduce the construction cost and to increase the robustness of power supply rails, the 5G OLEV of ultraslim S-type core was recently proposed, which has an S-shape when viewed from the front, as shown in Fig. 34.30C.

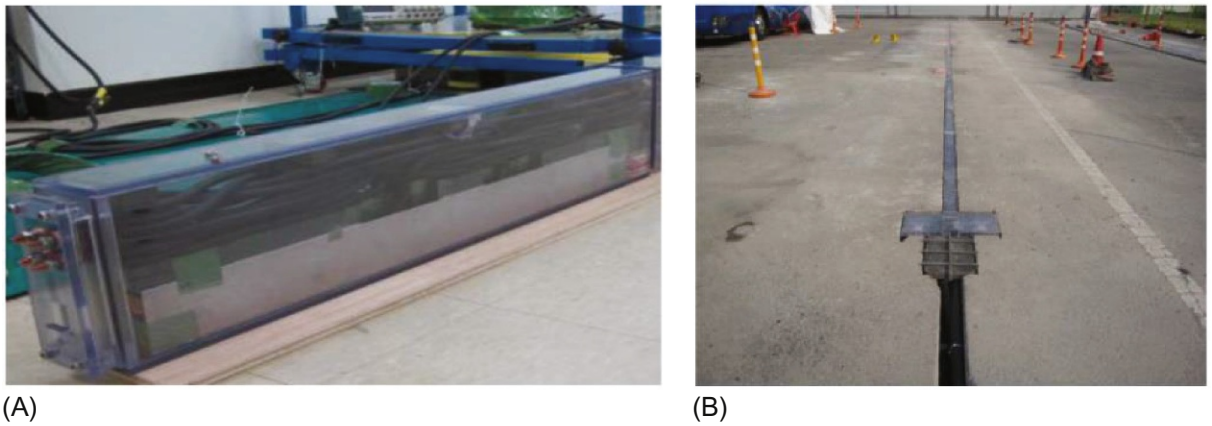


FIG. 34.29 The I-type power supply module of the 4G OLEV [18]. (A) A prototype module, (B) deployed modules at the 24 m test site.

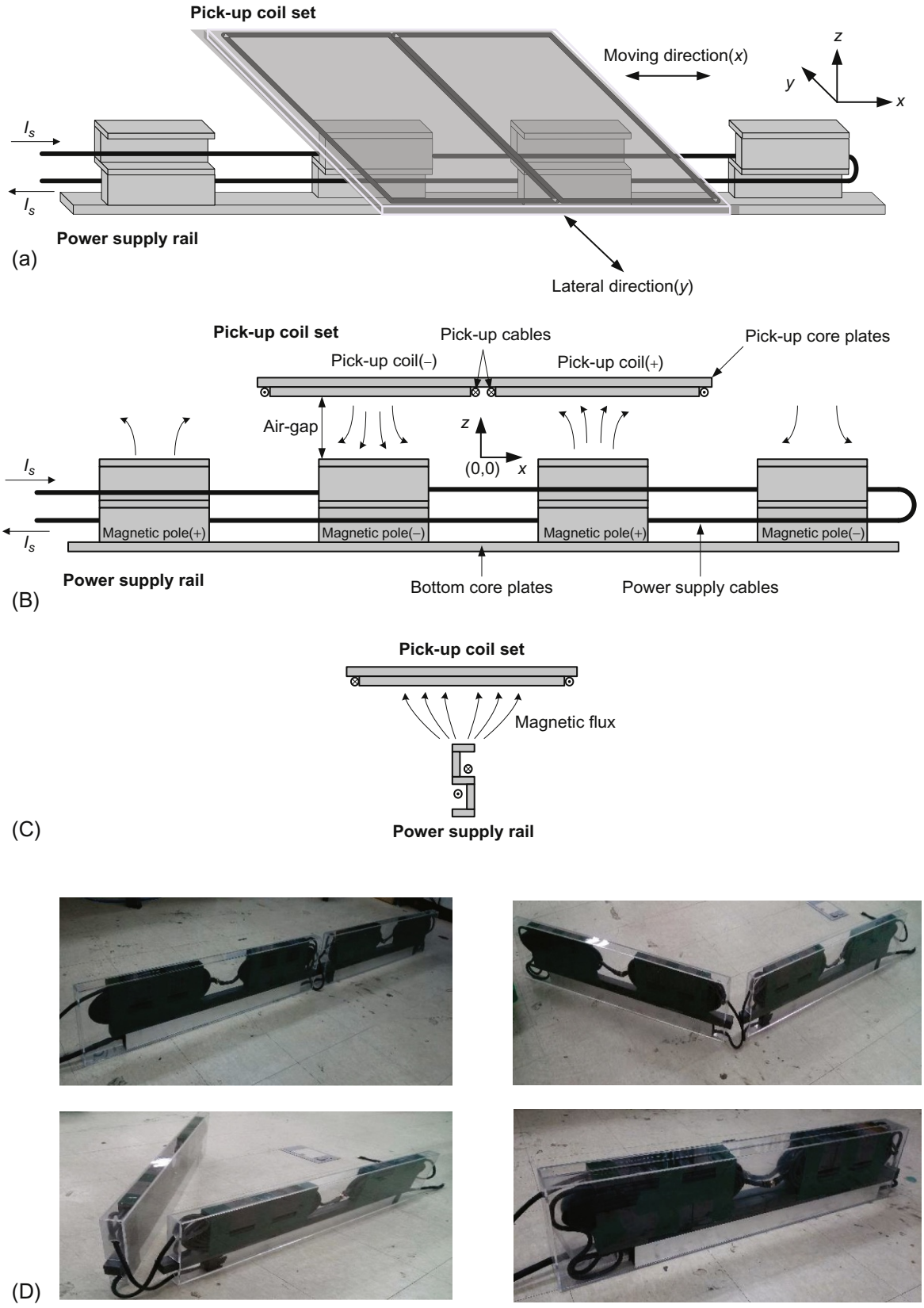


FIG. 34.30 The concept and fabrication of ultraslim S-type power supply modules [18]. (A) Bird's view, (B) side view, (C) front view, (D) deployment process.

The S-type power supply module has a width of only 4 cm, which has been decreased from the I-type width of 10 cm; hence, the S-type model leads to less construction cost and deployment time. Moreover, the S-type model makes it easier to fold itself, which means connecting power cables is no longer necessary after being deployed. The impact of deploying the S-type power supply modules on the surface of roads is now minimal, which fortunately does not change existing road operation conditions.

34.4 Design Considerations of Wireless Electric Vehicles

A few common design consideration issues applicable to both stationary and dynamic charging EVs are explained here. The issues are compensation, electric and magnetic circuit analyses, EMF cancel, and segmentation.

34.4.1 Compensation Circuit Design

Due to large inductive reactances of IPT, capacitors are preferably adopted to nullify the total reactance and to resonate to a certain frequency for filtering out harmonics. One of widely used compensation circuits is two-capacitor type, called basic compensation circuit, as shown Fig. 34.31. There are eight possible circuit topologies for compensation depending on current (I) or voltage (V) source types and serial (S) or parallel (P) configurations. In case the magnetic coupling factor k between Tx and Rx coils varies a lot, the three conditions should be met for practical applications: (1) load-independent output voltage or output current, (2) k-independent compensation, and (3) allowance of no magnetic coupling ($k=0$).

It is identified that only I-SS and I-SP can satisfy all of the three criteria simultaneously among the eight compensation schemes [37]. I-SS has the voltage-source-type output characteristics, which enable large load current; whereas, I-SP has the current-source-type output characteristics, which enable high load voltage. Of course, other schemes may be also used if the three conditions are not needed.

Substantial equivalence and duality between I-SS and I-SP are found in the aspect of efficiency, power transfer characteristics, and voltage and current ratings of reactive components, as shown in Fig. 34.32. This means that there is no privilege between I-SS and I-SP, so we can freely choose compensation scheme according to large-current or high-voltage applications.

One of the ways to implement the current source of IPT is to make the current of a primary coil constant by feedback, as shown in Fig. 34.20. Another way of getting the current source is to use an LC filter for a given voltage source so that the Norton equivalent circuit has infinite output impedance when the source frequency is tuned to the resonance frequency, as shown in Fig. 34.33. This is known to be LCC topology of IPT [27,37], which has the current source input and voltage source output characteristics.

34.4.2 Gyrator Based Circuit Analysis

The electric analysis of IPT including compensation circuits is quite challenging because there are at least five energy storage circuit elements. Therefore, a powerful circuit analysis tool is recently invented, called gyrator-based circuit analysis by the author [38]. This method drastically simplifies the analysis process and makes it possible to get analytic results without cumbersome manipulation of equations. Applying Kirchhoff's voltage law on V_1 and V_2 in Fig. 34.34A gives us the following equations in the steady state of sinusoidal AC circuits:

$$V_1 = (-jX_0) \times (I_1 - I_2) + jX_0 \times I_1 = jX_0 \times I_2 \tag{34.5a}$$

$$V_2 = (-jX_0) \times (I_1 - I_2) + jX_0 \times (-I_2) = -jX_0 \times I_1 = (jX_0)^* \times I_1. \tag{34.5b}$$

As shown in Fig. 34.34B, Eq. (34.5) describes the imaginary gyrator, first introduced in the literature [38].

As shown in Fig. 34.35, the T model of IPT can be decomposed into the imaginary gyrator and the primary and secondary inductances. This gyrator equivalent circuit is applied to the analysis of an example V-SS circuit of Fig. 34.36, where the series-series resonant circuits L_1-C_1 and L_2-C_2 are tuned to the source frequency, respectively.

From the gyrator characteristics, the load current of V-SS is solely determined by the source voltage and independent of load resistance and load voltage as follows:

$$A_G \equiv \frac{I_L}{V_s} = -\frac{1}{j\omega_0 M}, \tag{34.6}$$

$$\frac{\partial I_L}{\partial R_L} = 0. \tag{34.7}$$

In this way, other features of the V-SS in Fig. 34.36 such as input power factor, voltage and current stresses of each component, and input and output impedances can be deduced from the equivalent gyrator circuit without using high-order matrix manipulation.

34.4.3 Magnetic Mirror Based Coil Design

In the coil design, we are quite often encountered to calculation of magnetic flux density, but you will readily see that there is nearly no available theoretical tool to finish your job. The difficulties of magnetic field calculation come from the complex interaction between current and magnetic material, which denies the application of Ampere's law that gives us the result only when appropriate current is given.

Fortunately, the magnetic flux density of an open magnetic circuit can be simply calculated by the magnetic mirror model [15], as shown in Fig. 34.37, where a reflected current at the

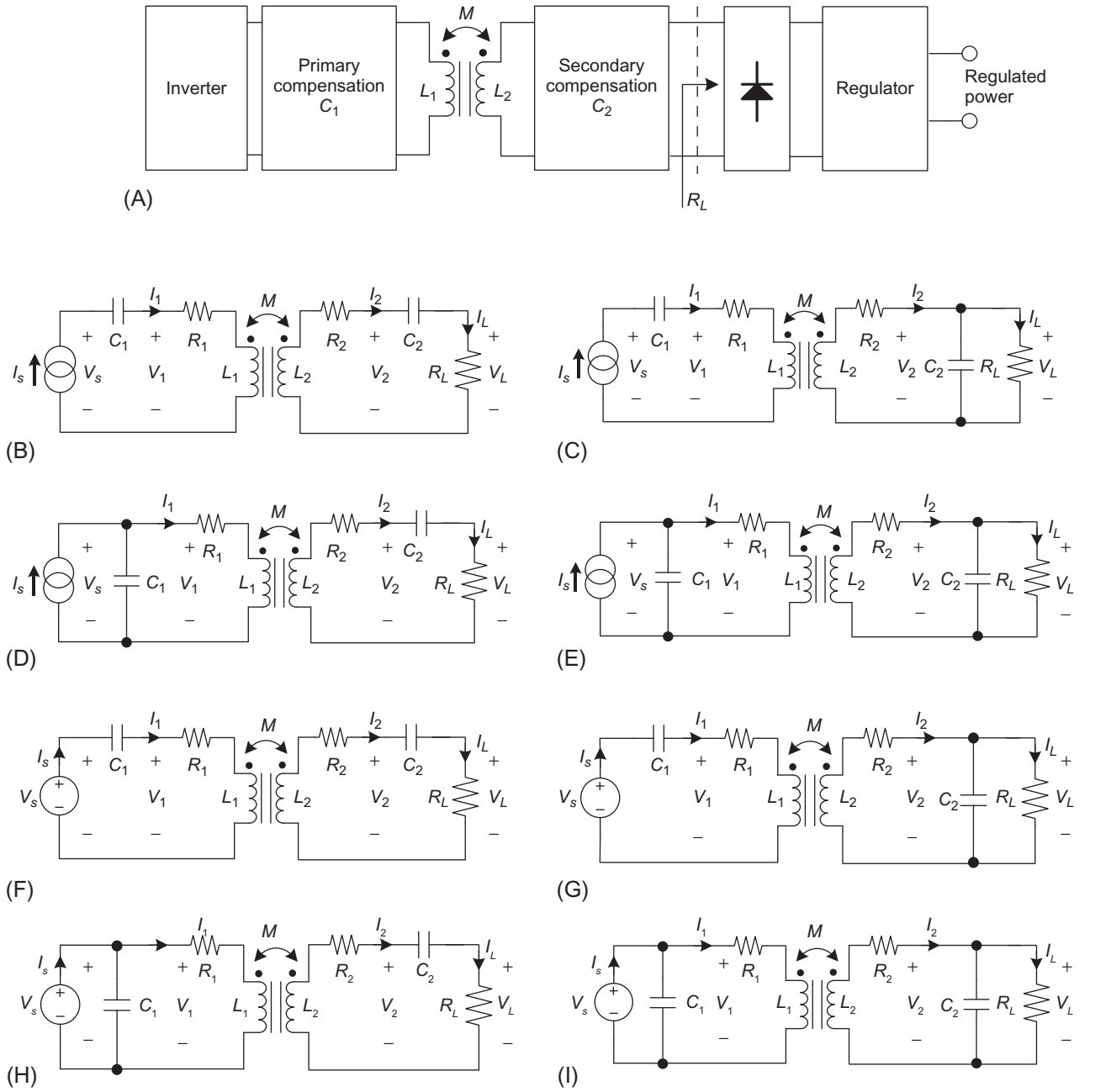


FIG. 34.31 The eight basic compensation circuits of IPT. (A) General configuration of an IPT system, (B) current-source-type primary series-secondary series (I-SS), (C) current-source-type primary series-secondary parallel (I-SP), (D) current-source-type primary parallel-secondary series (I-PS), (E) current-source-type primary parallel-secondary parallel (I-PP), (F) voltage-source-type primary series-secondary series (V-SS), (G) voltage-source-type primary series-secondary parallel (V-SP), (H) voltage-source-type primary parallel-secondary series (V-PS), (I) voltage-source-type primary parallel-secondary parallel (V-PP).

same distance from the surface of a magnetic plate exists with a reduced amplitude as follows:

$$d_m = d_s = d,\ \ \gamma_1 \equiv \frac{I_m}{I_s} \cong \left(1 - e^{-\frac{w_o}{\alpha_1 y}}\right)\ \ \because \alpha_1 \cong 1.7. \tag{34.8}$$

Then, the magnetic flux density of a mono coil B_1 for a mirror current I_m and a source current I_s at an arbitrary measurement point (x, y) are obtained as follows:

$$B_1 \equiv |\boldsymbol{B}_1| = |\mu_0 \boldsymbol{H}_1| = \left|\frac{\mu_0 I_s}{2\pi}\frac{\boldsymbol{\alpha}_x(y-d_s)-\boldsymbol{\alpha}_y x}{r_s^2} + \frac{\mu_0 I_m}{2\pi}\frac{\boldsymbol{\alpha}_x(y+d_m)-\boldsymbol{\alpha}_y x}{r_m^2}\right|$$

$$= \frac{\mu_o I_s}{2\pi}\sqrt{\left\{\frac{y-d_s}{r_s^2} + \gamma_1\frac{y+d_m}{r_m^2}\right\}^2 + \left\{\frac{x}{r_s^2} + \gamma_1\frac{x}{r_m^2}\right\}^2}\ \ for\ |x| < \frac{w_o}{2}, 0 \le y \tag{34.9a}$$

$$r_s = \sqrt{x^2 + (y-d_s)^2},\ r_m = \sqrt{x^2 + (y+d_m)^2}. \tag{34.9b}$$

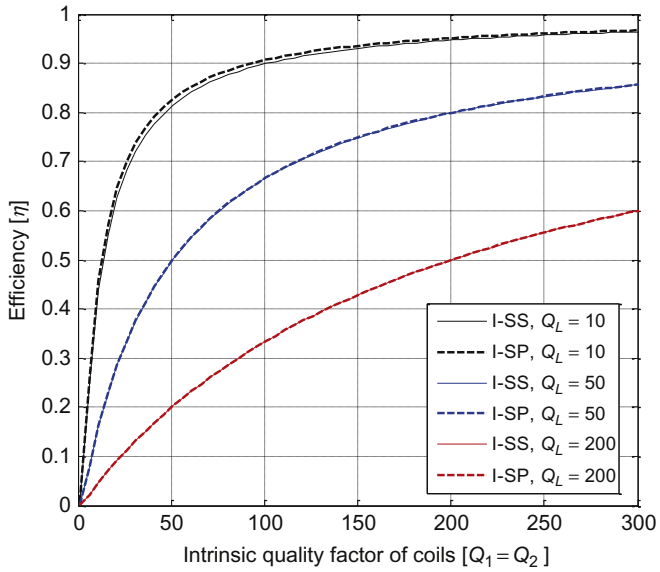


FIG. 34.32 Efficiencies η versus quality factor Q_1 for I-SS and I-SP when $\omega = \omega_2$ and $k = 0.3$.

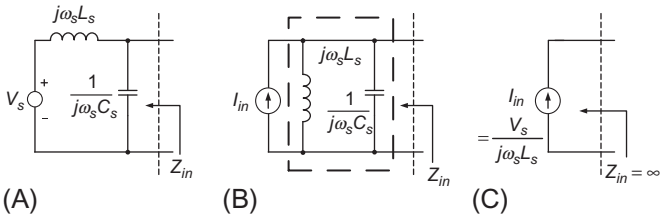


FIG. 34.33 An LC-tuned filter with a voltage source becomes an ideal current source. (A) Original LC input filter, (B) Norton equivalent circuit, (C) final equivalent circuit for tuned case.

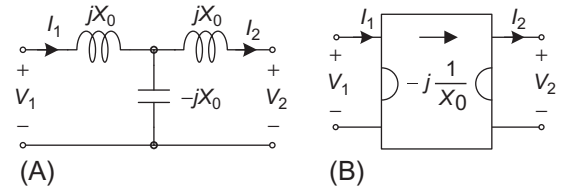


FIG. 34.34 A T-network consists of all equal reactance and its equivalent gyrator circuit. (A) Gyratorin a T-network, (B) A Gyrator circuit model.

As identified from Fig. 34.37 and Eqs. (34.8)–(34.9), the magnetic flux density is at best doubled by the magnetic core for an open magnetic circuit. This is one of the backgrounds on no core use for some applications.

34.4.4 Generalized Active EMF Cancellation Methods

In the IPTS of OLEV, the total EMF, which is the summation of EMF generated by the power supply rail and the pickup coil, should be lower than the ICNIRP guideline for the safety of pedestrians. Among EMF cancellation methods [35,36,39–44], passive methods rely on the use of ferromagnetic materials, conductive materials, and selective surfaces for protecting against radio-frequency interference [39–41], which is found to be inadequate for OLEV. An active EMF cancellation design was applied to the RPEV of PATH team [1], where a canceling coil mitigates the EMF without RPEV. Note that the EMF is generated from both the power supply rail and pickup coil of the IPTS, as shown in Fig. 34.38; therefore, they must be canceled together without the need for accurate sensing of EMF and complicated control circuits, which is requisite for practical use.

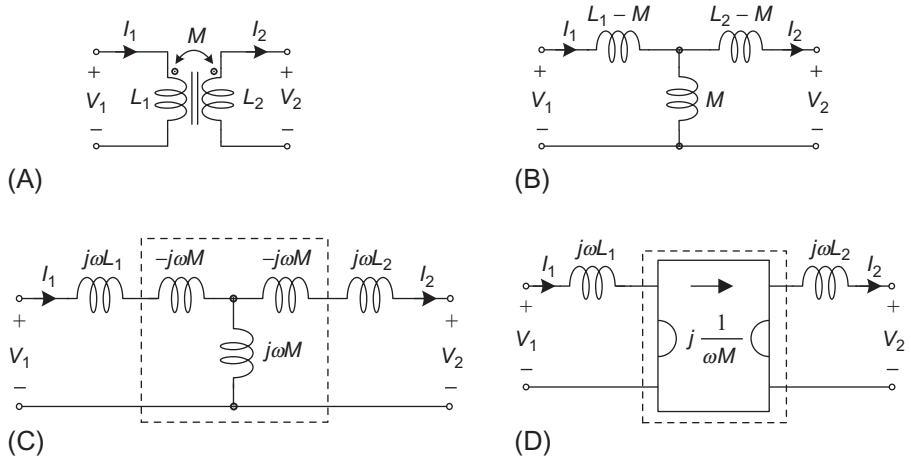


FIG. 34.35 Representation of coupled inductors with a gyrator. (A) Circuit model of coupled inductors, (B) equivalent T-model of coupled inductors, (C) equivalent circuit of (B), (D) Representation of (C) with a gyrator model.

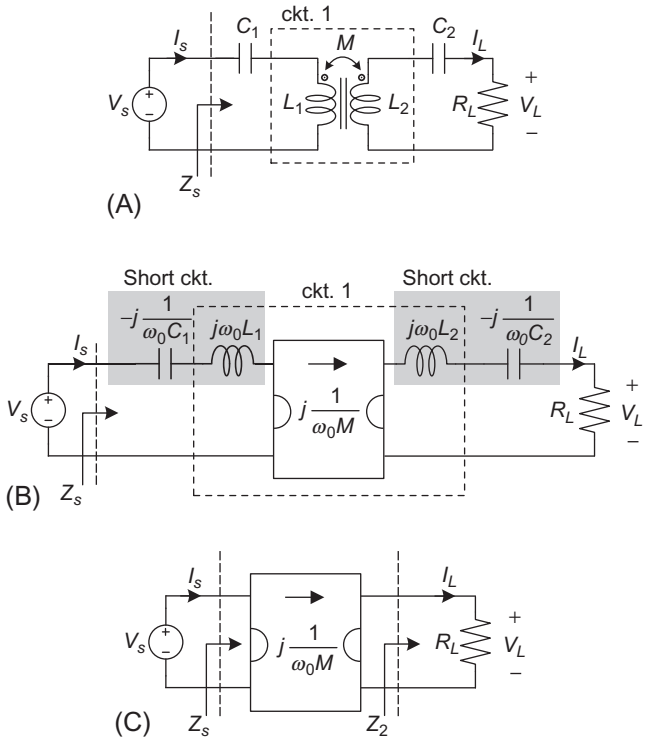


FIG. 34.36 V-SS and the equivalent gyrator-based models. (A) V-SS circuit model, (B) equivalent V-SS circuit of (A) with a gyrator, (C) equivalent V-SS circuit of (B) with a gyrator,when primary and secondary LC's are tuned.

A generalized active EMF design principle, which can be extended to any IPTS, has been developed [44], where there are three design methods: independent self EMF cancellation (ISEC), 3 dB dominant EMF cancellation (3DEC), and

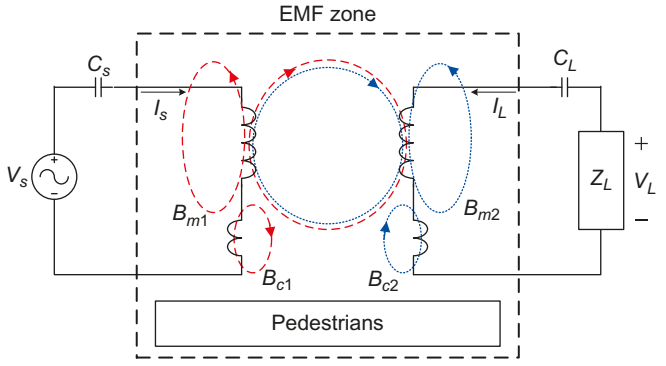


FIG. 34.38 Independent self EMF cancellation (ISEC) method for primary and secondary sides, fetching its cancellation current from each main coil.

leakage-free EMF cancellation (LFEC). By adding an active EMF cancellation coil to each power supply rail and pickup coil without EMF sensing and control circuits, the EMF generated from each main coil can be independently canceled by their corresponding cancellation coils. Because the current of each cancellation coil is fetched from its corresponding main coil, the magnetic flux of a cancellation coil is in the phase of that of a main coil; hence, the EMF $\boldsymbol{B}_t$ becomes independent of both phase and load conditions as follows:

$$\boldsymbol{B}_t = (\boldsymbol{B}_{m1} + \boldsymbol{B}_{c1}) + (\boldsymbol{B}_{m2} + \boldsymbol{B}_{c2}) \cong 0, \quad \because \ \boldsymbol{B}_{c1} \cong -\boldsymbol{B}_{m1}, \quad \boldsymbol{B}_{c2} \cong -\boldsymbol{B}_{m2} \quad \text{and} \quad \boldsymbol{B}_k \equiv B_{kx}\boldsymbol{x}_0 + B_{ky}\boldsymbol{y}_0 + B_{kz}\boldsymbol{z}_0. \tag{34.10}$$

Together with ISEC, the 3DEC method is quite useful in practice for designing IPTS because it makes it possible to completely isolate the primary and secondary cancellation designs from each other.

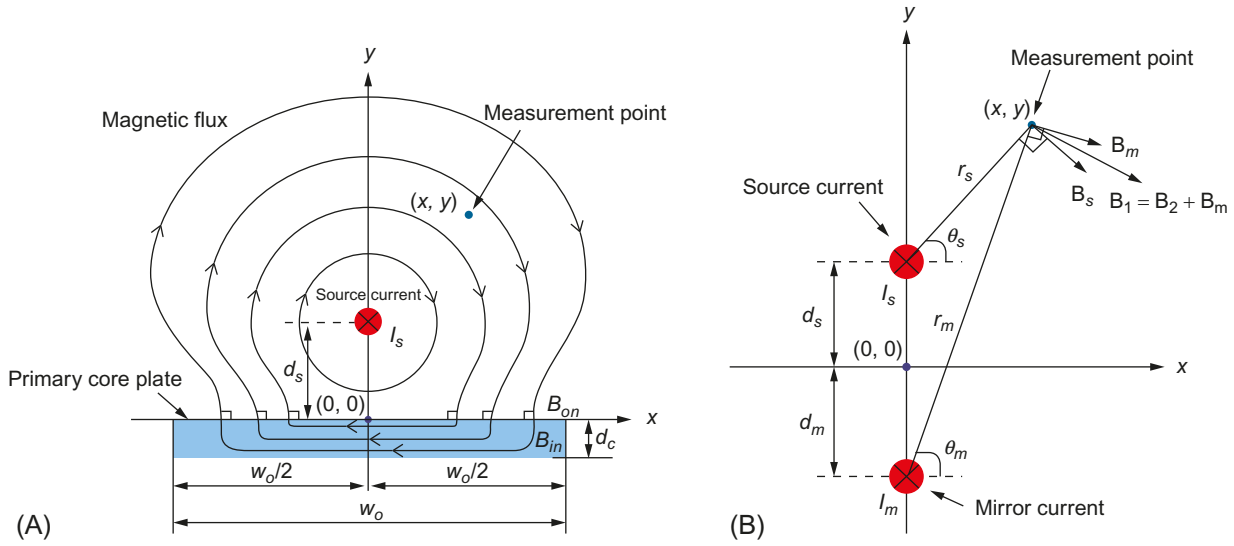


FIG. 34.37 The magnetic mirror model. (A) Mono coil consists of a source current and a core plate with finite width and infinite permeability, (B) the magnetic mirror current of the mono coil.

For the full resonant IPTS that is very common in practice, the primary and secondary currents are in quadrature, that is, $B_{1x} \perp B_{2x}$, $B_{1y} \perp B_{2y}$, and $B_{1z} \perp B_{2z}$. Then, the total magnetic field B_t can be constrained to the ICNIRP guidelines so far as the dominating magnetic field B_1 is less than 3 dB below the guideline as follows:

$$B_t \equiv |\boldsymbol{B}_t| = \sqrt{|\boldsymbol{B}_1|^2 + |\boldsymbol{B}_2|^2} = \sqrt{B_1^2 + B_2^2} \le \sqrt{B_1^2 + B_1^2} = \sqrt{2}B_1 \le B_{ref} \quad \because B_1 \equiv |\boldsymbol{B}_1|, B_2 \equiv |\boldsymbol{B}_2|, \quad B_2 \le B_1. \tag{34.11}$$

A design example for the 4G I-type IPTS based on the ISEC and 3DEC is shown in Fig. 34.39, where no cancellation coil was used for the power supply rail due to the low EMF generated from itself.

In case the EMF cancellation coils are involved in an unwanted magnetic linkage, as shown in Fig. 34.40, the induced load voltage drops; therefore, it is highly recommended to design the cancellation coils based on the LFEC method so that the magnetic linkage does not intersect them. The LFEC method can improve the load voltage as much as 21% [44].

34.4.5 Segmentation of Power rails

Unlike stationary charging EV, the RPEV needs its own roadway, where power supply rails should be activated when RPEVs are on the roadway, but they should be deactivated not to waste electric power and generate unwanted EMF for pedestrians; this is why the power supply rail is sometimes segmented into a few subrails. Each subrail can be activated by providing it with high-frequency current through a switch box from an inverter, as shown in Fig. 34.41.

The first segmented power supply rail developed for OLEV, as shown in Fig. 34.41A, was the centralized switching type composed of a few subrails, a bundle of supply cables, and a centralized switch box, where an inverter is connected to one of several pairs of supply cables through the switch box at a time. One of the demerits of the centralized one is that too many bundles of power cables are needed.

This is why the distributed switching power rail, as shown in Fig. 34.41B, was proposed, which is composed of a few subrails, a pair of common power supply cables, and multiple switch boxes located between two subrails.

Thus, the total length of the cable could be reduced compared with the centralized one, especially for a larger number

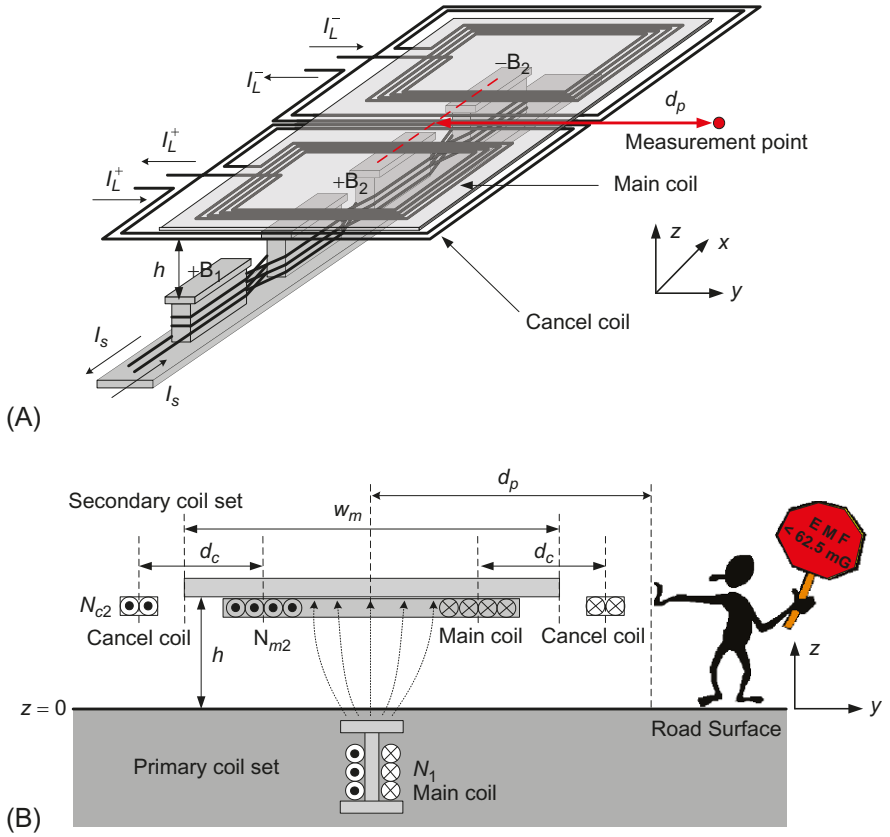


FIG. 34.39 An active EMF cancellation design example for the I-type IPTS. (A) Bird's eye view, (B) front view.

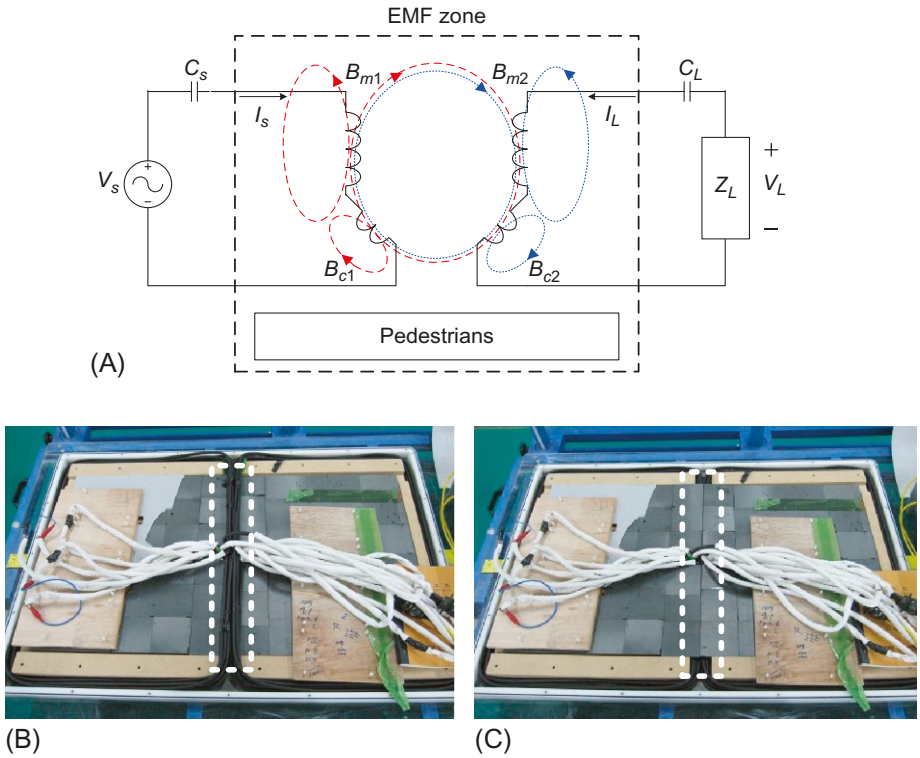


FIG. 34.40 Leakage-free EMF cancellation (LFEC). (A) A bad design case for cancellation coils, which are strongly coupled with main magnetic linkage, (B) the application of the LFEC design to a pick-up set, (C) the case where not applied.

of the cables. The distributed one, however, requires the common power supply cables, which increases the power rail construction cost and conductive power loss.

A recently proposed cross segmented power supply rail (X-rail) [16], consisting of segmented subrails, autocompensation switch boxes, control signal lines, and roadway harnesses, as shown in Fig. 34.41C, has the shortest length of power cable among the segmentations developed so far, and the inverter can drive multiple RPEVs, unlike the previous segmentations that activate only one subrail at a time.

As shown in Fig. 34.42, the cable cost of the X-rail is nearly halved compared with the distributed switching, and the cable length reduction effect becomes dominant as the number of segmented subrails increases.

If applicable, nonsegmented power rail would be better than the segmented one, considering increased cost and complexities. One of the possible candidates is the autotuned IPTS, where power is delivered only when EVs are on the power supply coils.

34.5 Summary

The concepts of WPT and its practical applications to EVs are explained throughout the chapter. IPT for stationary and dynamic charging EVs is explained. The development of IPTS for RPEV including state-of-the-art technologies is explained in detail. RPEV is becoming a viable solution for future transportation as the first commercialized online EV has demonstrated its validity.

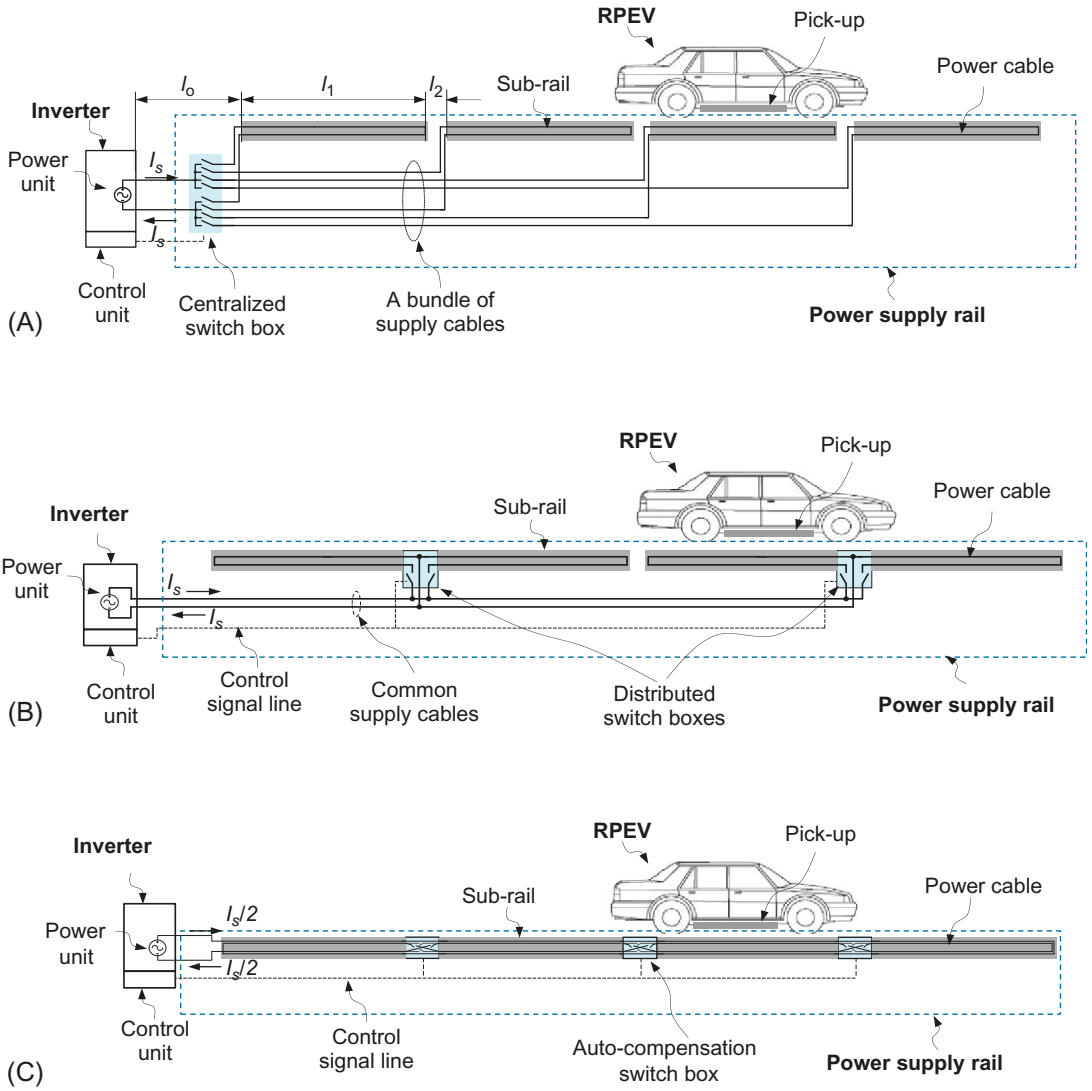


FIG. 34.41 Segmentation of power supply rails for RPEV. (A) Centralized switching, (B) distributed switching, (C) X-segmented switching.

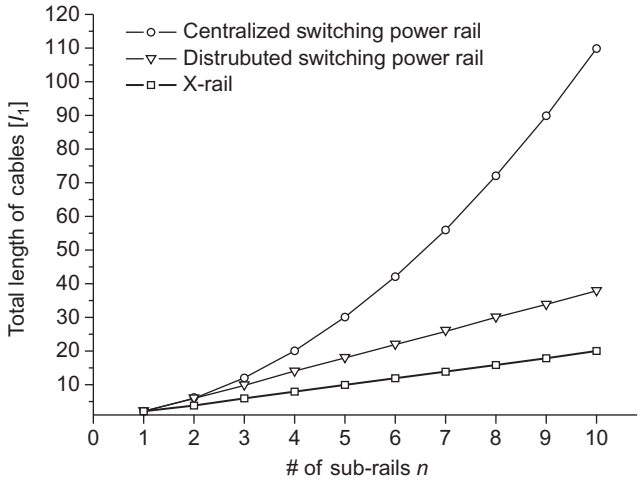


FIG. 34.42 Comparison of the total length of power cables of the X-rail with that of the conventional switching rails.

References

[1] California PATH Program, Road powered electric vehicle project track construction and testing program phase 3D, California PATH Research Paper, Mar. 1994.

[2] G.A. Covic, J.T. Boys, M. Kissin, H. Lu, A three-phase inductive power transfer system for roadway power vehicles, IEEE Trans. Ind. Electron. 54 (6) (Dec. 2007) 3370–3378.

[3] N.P. Suh, D.H. Cho, C.T. Rim, Design of on-line electric vehicle (OLEV, in: Plenary Lecture at the 2010 CIRP Design Conference, 2010, pp. 3–8.

[4] S.W. Lee, J. Huh, C.B. Park, N.S. Choi, G.H. Cho, C.T. Rim, On-line electric vehicle (OLEV) using inductive power transfer system, in: IEEE Energy Conversion Congress and Exposition (ECCE), 2010, pp. 1598–1601.

[5] J. Huh, S.W. Lee, C.B. Park, G.H. Cho, C.T. Rim, High performance inductive power transfer system with narrow rail width for on-line electric vehicles, in: IEEE Energy Conversion Congress and Exposition (ECCE), 2010. pp. 647–651.

[6] Chun T. Rim, Electric vehicle system, Patent WO 2010 076976, 2010
[7] N.P. Suh, D.H. Cho, G.H. Cho, J.G. Cho, Chun T. Rim, S.H. Jang, Ultra slim power supply and collector device for electric vehicle, Patent KR 1010406620000, 2011.
[8] S.Z. Jeon, D.H. Cho, Chun T. Rim, G.H. Jeong, Load-segmentation-based full bridge inverter and method for controlling same, Patent WO 2011 078424, 2011.
[9] S.Z. Jeon, D.H. Cho, Chun T. Rim, G.H. Jeong, Load-segmentation-based 3-level inverter and method for controlling the same, Patent WO 2011 078425, 2011.
[10] N.P. Suh, D.H. Cho, J.G. Cho, Chun T. Rim, J. Huh, J.H Kim, C.S. Choi, K.H. Lee, B.Y. Song, Y.J. Cho, C.H. Rim, Monorail type power supply device for electric vehicle including EMF cancellation apparatus, Patent WO 2011 046374, 2011.
[11] N.P. Suh, S.H. Jang, D.H. Cho, G.H. Cho, Chun T. Rim, S.W. Lee, C.B. Park, J. Huh, H.J. Kim, Space division multiplexed power supply and collector device, Patent WO 2011 152678, 2011.
[12] N.P. Suh, S.H. Jang, D.H. Cho, G.H. Cho, Chun T. Rim, J. Huh, B.H. Lee, Y.H. Kim, Cross-type segment power supply, Patent WO 2011 152677, 2011.
[13] J. Huh, S.W. Lee, W.Y. Lee, G.H. Cho, C.T. Rim, Narrow-width inductive power transfer system for on-line electrical vehicles (OLEV), IEEE Trans. Power Electron. 26 (12) (2011) 3666–3679.
[14] N.P. Suh, S.H. Jang, D.H. Cho, G.H. Cho, Chun T. Rim, S.W. Lee, C.B. Park, EMI cancellation device in power supply and collector device for magnetic induction power transmission, Patent WO 2011 149263, 2012.
[15] W.Y. Lee, J. Huh, S.Y. Choi, X.V. Thai, J.H. Kim, E.A. Al-Ammar, M. A. El-Kady, C.T. Rim, Finite-width magnetic mirror models of mono and dual coils for wireless electric vehicles, IEEE Trans. Power Electron. 28 (3) (Mar. 2013) 1413–1428.
[16] S.Y. Choi, J. Huh, W.Y. Lee, S.W. Lee, C.T. Rim, New cross-segmented power supply rails for road powered electric vehicles, IEEE Trans. Power Electron. 28 (12) (2013) 5832–5841.
[17] S.Y. Choi, J. Huh, W.Y. Lee, J.G. Cho, C.T. Rim, Asymmetric coil sets for wireless stationary EV chargers with large lateral tolerance by dominant field analysis, IEEE Trans. Power Electron. 29 (12) (2014) 6406–6420.
[18] S.Y. Choi, B.W. Gu, S.Y. Jeong, C.T. Rim, Advances in wireless power transfer systems for road powered electric vehicles, IEEE J. Emerg. Sel. Top. Power Electron. 3 (1) (2015) 18–36.
[19] C. Mi, G. Buja, S.Y. Choi, C.T. Rim, Modern advances in wireless power transfer systems for roadway powered electric vehicles, *IEEE Trans. Ind. Electron.* 63 (10) (2016) 6533–6545.
[20] K.W. Klontz, D.M. Divan, D.W. Novotny, R.D. Lorenz, Contactless power delivery system for mining applications, IEEE Trans. Ind. Appl. 31 (1) (1995) 27–35.
[21] C.S. Wang, G.A. Covic, O.H. Stielau, Power transfer capability and bifurcation phenomena of loosely coupled inductive power transfer systems, IEEE Trans. Ind. Electron. 51 (1) (2004) 148–157.
[22] C.S. Wang, O.H. Stielau, G.A. Covic, Design considerations for a contactless electric vehicle battery charger, IEEE Trans. Ind. Electron. 52 (5) (2005) 1308–1314.
[23] M. Budhia, J.T. Boys, G.A. Covic, C.-Y. Huang, Development of a single-sided flux magnetic coupler for electric vehicle IPT charging systems, IEEE Trans. Ind. Electron. 60 (1) (2013) 318–328.
[24] G.A. Covic, J.T. Boys, Modern trends in inductive power transfer for transportation applications, IEEE J. Emerg. Sel. Top. Power Electron. 1 (1) (2013) 28–41.
[25] H. Zhang, F. Lu, H. Hofmann, W. Liu, C. Mi, A 4-Plate compact capacitive coupler and *LCL* compensation topology for capacitive power transfer in electric vehicle charging applications, IEEE Trans. Power Electron. 31 (12) (2016) 8541–8551.
[26] V.X. Thai, S.Y. Choi, S.Y. Jeong, C.T. Rim, Coreless power supply rails compatible with both stationary and dynamic charging of electric vehicles, in: IEEE International Future Energy Electronics Conference (IEEE IFEEC 2015), 978-1-4799-7657-7, 2015.
[27] C.T. Rim, C. Mi, Wireless Power Transfer for Electric Vehicles and Mobile Devices, Wiley, USA, 2017.
[28] K.T. Chau, Energy Systems for Electric and Hybrid Vehicles, IET, London, 2016.
[29] C. Park, S. Lee, G.H. Cho, C.T. Rim, Innovative 5 m-off-distance inductive power transfer systems with optimum shaped dipole coils, IEEE Trans. Power Electron. 30 (2) (2015) 817–827.
[30] C.B. Park, S.W. Lee, C.T. Rim, Static and dynamic analyses of three-phase rectifier with LC input filter by Laplace phasor transformation, in: Energy Conversion Congress and Exposition (ECCE), Sep. 2012, pp. 1570–1577.
[31] S. Lee, B. Choi, C.T. Rim, Dynamics characterization of the inductive power transfer system for on-line electric vehicles (OLEV) by Laplace phasor transform, IEEE Trans. Power Electron. 28 (12) (2013) 5902–5909.
[32] C.T. Rim, G.H. Cho, Phasor transformation and its application to the dc/ac analyses of frequency phase-controlled series resonant converters (SRC), IEEE Trans. Power Electron. 5 (2) (1990) 201–211.
[33] C.T. Rim, Unified general phasor transformation for AC converters, IEEE Trans. Power Electron. 26 (9) (2011) 2465–2745.
[34] C.T. Rim, Phasor Power Electronics, Springer, Singapore, 2016.
[35] Guidelines for limiting exposure to time-varying electric and magnetic fields (Up to 300 GHz), ICNIRP Guidelines, 1998.
[36] Guidelines for limiting exposure to time-varying electric and magnetic fields (Up to 100 kHz), ICNIRP Guidelines, 2010.
[37] Y.H. Son, B.H. Choi, E.S. Lee, G.C. Lim, G.H. Cho, C.T. Rim, General unified analyses of two-capacitor inductive power transfer systems: equivalence of current-source ss and sp compensations, IEEE Trans. Power Electron. 30 (11) (2015) 6030–6045.
[38] Y.H. Son, B.H. Choi, G.H. Cho, C.T. Rim, Gyrator-based analysis of resonant circuits in inductive power transfer systems, IEEE Trans. Power Electron. 31 (10) (2016) 6824–6843.
[39] P.R. Bannister, New theoretical expressions for predicting shielding effectiveness for the plane shield case, IEEE Trans. Electromagn. Compat. EMC-10 (1) (1968) 2–7.
[40] D. Yaping, T.C. Cheng, A.S. Farag, Principles of power-frequency magnetic field shielding with flat sheets in a source of long conductors, IEEE Trans. Electromagn. Compat. 38 (3) (1996) 450–459.
[41] P. Moreno, R.G. Olsen, A simple theory for optimizing finite width ELF magnetic field shields for minimum dependence on source orientation, IEEE Trans. Electromagn. Compat. 39 (4) (1997) 340–348.
[42] M.L. Hiles, K.L. Griffing, Power frequency magnetic field management using a combination of active and passive shielding technology, IEEE Trans. Power Delivery Electron. (1998) 171–179.
[43] P. Wu, F. Bai, Q. Xue, S.Y.R. Hui, Use of frequency selective surface for suppressing radio-frequency interference from wireless charging pads, IEEE Trans. Ind. Electron. 61 (8) (2014) 3969–3977.
[44] S.Y. Choi, B.W. Gu, S.W. Lee, W.Y. Lee, J. Huh, C. T. Rim, Generalized active EMF cancel methods for wireless electric vehicles, IEEE Trans. Power Electron. 29 (11) (2014) 5770–5783.

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Section VI

Control

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35

Linear and Nonlinear Control of Switching Power Converters

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35.1 Introduction

Switching power converters must be suitably designed and controlled in order to supply the voltages, currents, or frequency ranges needed for the load and to guarantee the requested dynamics [1–4]. Furthermore, they can be designed to serve as "clean" interfaces between most loads and the electric utility system. Thereafter, the set switching power converter plus load behaves as an almost pure electric utility resistive load.

This chapter provides basic and advanced skills to control electronic power converters, taking into account that the control of switching power converters is a vast and interdisciplinary subject. Control designers for switching power converters should know the static and dynamic behavior of the electronic power converter and how to design its elements for the intended operating modes. Designers must be experts on control techniques, especially the nonlinear ones, since switching converters are nonlinear, time-variant, discrete systems, and designers must be capable of analog or digital implementation of the derived modulators, regulators, or compensators. Powerful modeling methodologies and sophisticated control processes must be used to obtain stable-controlled switching power converters, not only with satisfactory static and dynamic performance but also with low sensitivity against load or line disturbances or, preferably, robustness.

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In Section 35.2, the techniques to obtain suitable nonlinear and linear state-space models, for most switching converters, are presented and illustrated through examples. The derived linear models are used to create equivalent circuits and to design linear feedback controllers for converters operating in the continuous or discontinuous mode. The classical linear time-invariant system control theory, based on Laplace transform, transfer function concepts, Bode plots, or root locus, is best used with state-space averaged models or derived circuits and well-known triangular wave modulators for generating the switching variables or the trigger signals for the power semiconductors.

Nonlinear state-space models and sliding-mode controllers, presented in Section 35.3, provide a more consistent way of handling the control problem of switching converters, since sliding mode is aimed at variable structure systems, as are switching power converters. Chattering, a characteristic of sliding mode, is inherent to switching power converters, even if they are controlled with linear methods. Chattering is very hard to remove and is acceptable in certain converter variables. The described sliding-mode methodology defines exactly the variables that need to be measured, while providing the necessary equations (control law and switching law) whose implementation gives the robust modulator and compensator low-level hardware (or software). Therefore, the sliding-mode control integrates the design of the switching converter modulator and controller electronics, reducing the needed designer expertise. This approach requires measurement of the state variables but eliminates conventional modulators and linear feedback compensators, enabling better performance and robustness. It also reduces the converter cost, control complexity, volume, and weight (increasing power density). The so-called main drawback of sliding mode, variable switching frequency, is also addressed, providing fixed-frequency auxiliary functions and suitable augmented control laws to null steady-state errors due to the use of constant switching frequency.

Predictive control (Section 35.4) uses a detailed nonlinear dynamic model (including system bounds, saturations, and hysteresis) of the switching power converter to forecast the converter future behavior upon application of every possible switching state or vector. For all possible switching states (vectors), the control errors are evaluated and weighted, and the vector that leads to the minimum value of a suitable cost function is selected and applied to the converter. Predictive controllers also integrate the design of the switching converter modulator and controller electronics using fast microprocessors or fast algorithms. The steps in designing a predictive optimum controller for switching power converters with finite small number of switching states are explained in Section 35.4. Upon choosing a suitable cost function, obtained converter performances are usually better than obtained using linear or even sliding-mode controllers. This arises as sliding mode tries to go as fast as possible toward the sliding regime but chatters along the sliding surface, while predictive control aims to zero the error at the next sampling step.

In contrast, fuzzy control of switching converters (Section 35.5) is a control technique that needs no converter models, parameters, or operating conditions, but only an expert qualitative knowledge of the converter dynamics. Fuzzy controllers can be used in a diverse array of switching converters with only small adaptations, since the controllers, based on fuzzy sets, are obtained simply from the knowledge of the system dynamics, using a model reference adaptive control philosophy. Obtained fuzzy control rules can be built into a decision-lookup table, in which the control processor simply picks up the control input corresponding to the sampled measurements. Fuzzy controllers are almost resistant to system parameter fluctuations, since they do not take into account their values. The steps to obtain a fuzzy controller are described, and the example provided compares the fuzzy controller performance to the current-mode control.

Backstepping control (Section 35.6) is presented as a recursive method for stabilizing the origin of a converter modeled in a strict-feedback form. The procedure interconnects the choice of a candidate Lyapunov function with the design of the feedback control loop using Lyapunov's second method. Backstepping offers stability, tracking, and robust control under conditions less restrictive than other methods. Integral action is included to ensure the convergence, in steady state, of the tracking error to zero, regardless of nonmodeled disturbances and parameter uncertainty. Backstepping control is a nonlinear method that can be used with conventional fixed-frequency duty-cycle modulators for power converters to prevent chattering at variable frequency.

35.2 Switching Power Converter Control Using State-Space Averaged Models

35.2.1 Introduction

State-space models provide a general and strong basis for dynamic modeling of various systems including switching converters. State-space models are useful to design the needed linear control loops and can also be used to computer simulate the steady state and the dynamic behavior, of the switching converter, fitted with the designed feedback control loops and subjected to external perturbations. Furthermore, state-space models are the basis for applying powerful nonlinear control methods such as sliding mode. State-space averaging and linearization provide an elegant solution for the application of widely known linear control techniques to most switching power converters.

35.2.2 State-Space Modeling

Consider a switching power converter with sets of power semiconductor structures, each one with two different circuit configurations, according to the state of the respective semiconductors, and operating in the continuous mode of conduction. Supposing the power semiconductors as controlled ideal switches

(zero on-state voltage drops, zero off-state currents, and instantaneous commutation between the on- and off-states), the time (t) behavior of the circuit, over period T, can be represented by the general form of the state-space model Eq. (35.1):

$$\begin{aligned}\dot{\mathbf{x}} &= \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u}\\ \mathbf{y} &= \mathbf{C}\mathbf{x} + \mathbf{D}\mathbf{u}\end{aligned} \tag{35.1}$$

where $\mathbf{x}$ is the state vector; $\dot{\mathbf{x}} = \mathbf{dx/dt}$; $\mathbf{u}$ is the input or control vector; $\mathbf{y}$ is the output vector; and $\mathbf{A}$, $\mathbf{B}$, $\mathbf{C}$, and $\mathbf{D}$ are, respectively, the dynamics (or state), the input, the output, and the direct transmission (or feedforward) matrices.

Since the power semiconductors will be either conducting or blocking, a time-dependent switching variable $\delta(t)$ can be used to describe the allowed switch states of each structure (i.e., $\delta(t)=1$ for the on-state circuit and $\delta(t)=0$ for the off-state circuit). Then, two subintervals must be considered: subinterval 1 for $0 \le t \le \delta_1 T$, when $\delta(t)=1$, where δ_1 is the duty ratio between the on-state and the off-state, and subinterval 2 for $\delta_1 T \le t \le T$ when $\delta(t)=0$. The state equations of the circuit, in each of the circuit configurations, can be written as

$$\begin{aligned}\dot{\mathbf{x}} &= \mathbf{A}_1\mathbf{x} + \mathbf{B}_1\mathbf{u}\\ \mathbf{y} &= \mathbf{C}_1\mathbf{x} + \mathbf{D}_1\mathbf{u}\end{aligned} \quad \text{for} \quad 0 \le t \le \delta_1 T \quad \text{where } \delta(t)=1 \tag{35.2}$$

$$\begin{aligned}\dot{\mathbf{x}} &= \mathbf{A}_2\mathbf{x} + \mathbf{B}_2\mathbf{u}\\ \mathbf{y} &= \mathbf{C}_2\mathbf{x} + \mathbf{D}_2\mathbf{u}\end{aligned} \quad \text{for} \quad \delta_1 T \le t \le T \quad \text{where } \delta(t)=0 \tag{35.3}$$

35.2.2.1 Switched State-Space Model

Given the two binary values of the switching variable $\delta(t)$, Eqs. (35.2) and (35.3) can be combined to obtain the nonlinear and time-variant switched state-space model of the switching converter circuit, Eq. (35.4) or (35.5):

$$\begin{aligned}\dot{\mathbf{x}} &= [\mathbf{A}_1\delta(t) + \mathbf{A}_2(1-\delta(t))]\mathbf{x} + [\mathbf{B}_1\delta(t) + \mathbf{B}_2(1-\delta(t))]\mathbf{u}\\ \mathbf{y} &= [\mathbf{C}_1\delta(t) + \mathbf{C}_2(1-\delta(t))]\mathbf{x} + [\mathbf{D}_1\delta(t) + \mathbf{D}_2(1-\delta(t))]\mathbf{u}\end{aligned} \tag{35.4}$$

$$\begin{aligned}\dot{\mathbf{x}} &= \mathbf{A}_S\mathbf{x} + \mathbf{B}_S\mathbf{u}\\ \mathbf{y} &= \mathbf{C}_S\mathbf{x} + \mathbf{D}_S\mathbf{u}\end{aligned} \tag{35.5}$$

where $\mathbf{A}_S = [\mathbf{A}_1\delta(t) + \mathbf{A}_2(1-\delta(t))]$, $\mathbf{B}_S = [\mathbf{B}_1\delta(t) + \mathbf{B}_2(1-\delta(t))]$, $\mathbf{C}_S = [\mathbf{C}_1\delta(t) + \mathbf{C}_2(1-\delta(t))]$, and $\mathbf{D}_S = [\mathbf{D}_1\delta(t) + \mathbf{D}_2(1-\delta(t))]$.

35.2.2.2 State-Space Averaged Model

Since the state variables of the $\mathbf{x}$ vector are continuous, using Eq. (35.4), with the initial conditions $\mathbf{x}_1(0) = \mathbf{x}_2(T)$ and $\mathbf{x}_2(\delta_1 T) = \mathbf{x}_1(\delta_1 T)$, and considering the duty cycle δ_1 as the average value of $\delta(t)$, the time evolution of the converter state variables can be obtained, integrating Eq. (35.4) over the intervals $0 \le t \le \delta_1 T$ and $\delta_1 T \le t \le T$, although it often requires excessive calculation effort. However, a convenient approximation can be devised, considering λ_{max}, the maximum of the absolute values of all eigenvalues of $\mathbf{A}$ (usually, λ_{max} is related to the cut-off frequency f_c of an equivalent low-pass filter with $f_c \ll 1/T$). For $\lambda_{max} T \ll 1$, the exponential matrix (or state transition matrix) $e^{\mathbf{A}t} = \mathbf{I} + \mathbf{A}t + \mathbf{A}^2 t^2/2 + \ldots + \mathbf{A}^n t^n/n!$, where $\mathbf{I}$ is the identity or unity matrix, can be approximated by $e^{\mathbf{A}t} \approx \mathbf{I} + \mathbf{A}t$. Therefore, $e^{\mathbf{A}_1\delta_1 t} \cdot e^{\mathbf{A}_2(1-\delta_1)t} \approx \mathbf{I} + [\mathbf{A}_1\delta_1 + \mathbf{A}_2(1-\delta_1)]t$. Hence, the solution over the period T, for the system represented by Eq. (35.4), is found to be

$$\begin{aligned}\mathbf{x}(T) \cong\ & e^{[\mathbf{A}_1\delta_1 + \mathbf{A}_2(1-\delta_1)]T}\mathbf{x}_1(0)\\ &+ \int_0^T e^{[\mathbf{A}_1\delta_1 + \mathbf{A}_2(1-\delta_1)](T-\tau)}[\mathbf{B}_1\delta_1 + \mathbf{B}_2(1-\delta_1)]\mathbf{u}\,d\tau\end{aligned} \tag{35.6}$$

This approximate response of Eq. (35.4) is identical to the exact response obtained from the nonlinear continuous time-invariant state-space model (35.7), supposing that the average values of $\mathbf{x}$, denoted $\overline{\mathbf{x}}$, are the new state variables and considering $\delta_2 = 1 - \delta_1$. Moreover, if $\mathbf{A}_1\,\mathbf{A}_2 = \mathbf{A}_2\,\mathbf{A}_1$, the approximation is exact:

$$\begin{aligned}\dot{\overline{\mathbf{x}}} &= [\mathbf{A}_1\delta_1 + \mathbf{A}_2\delta_2]\,\overline{\mathbf{x}} + [\mathbf{B}_1\delta_1 + \mathbf{B}_2\delta_2]\,\overline{\mathbf{u}}\\ \overline{\mathbf{y}} &= [\mathbf{C}_1\delta_1 + \mathbf{C}_2\delta_2]\,\overline{\mathbf{x}} + [\mathbf{D}_1\delta_1 + \mathbf{D}_2\delta_2]\,\overline{\mathbf{u}}\end{aligned} \tag{35.7}$$

For $\lambda_{max} T \ll 1$, the model (35.7), often referred to as the state-space averaged model, is also said to be obtained by "averaging" Eq. (35.4) over one period, under small ripple and slow variations, as the average of products is approximated by products of the averages. Comparing Eq. (35.7) with Eq. (35.1), the relations (35.8), defining the state-space averaged model, are obtained:

$$\begin{aligned}&\mathbf{A} = [\mathbf{A}_1\delta_1 + \mathbf{A}_2\delta_2]; \quad \mathbf{B} = [\mathbf{B}_1\delta_1 + \mathbf{B}_2\delta_2];\\ &\mathbf{C} = [\mathbf{C}_1\delta_1 + \mathbf{C}_2\delta_2]; \quad \mathbf{D} = [\mathbf{D}_1\delta_1 + \mathbf{D}_2\delta_2]\end{aligned} \tag{35.8}$$

Example 35.1 State-space models for the buck–boost dc/dc converter

Consider the simplified circuitry of the buck-boost converter of Fig. 35.1 switching at $f_s = 20$ kHz ($T = 50$ µs) with $V_{DCmax} = 28$ V, $V_{DCmin} = 22$ V, $V_o = 24$ V, $L_i = 400$ µH, $C_o = 2700$ µF, and $R_o = 2\ \Omega$.

The differential equations governing the dynamics of the state vector $\mathbf{x} = [i_L,\ v_o]^T$ (^{T} denotes the transpose of vectors or matrices) are

$$\begin{aligned}L_i\frac{di_L}{dt} &= V_{DC}\\ C_o\frac{dv_o}{dt} &= -\frac{v_o}{R_o}\end{aligned} \quad \text{for } 0 \le t \le \delta_1 T \quad (\delta(t)=1,\ Q_1 \text{ is on and } D_1 \text{ is off}) \tag{35.9}$$

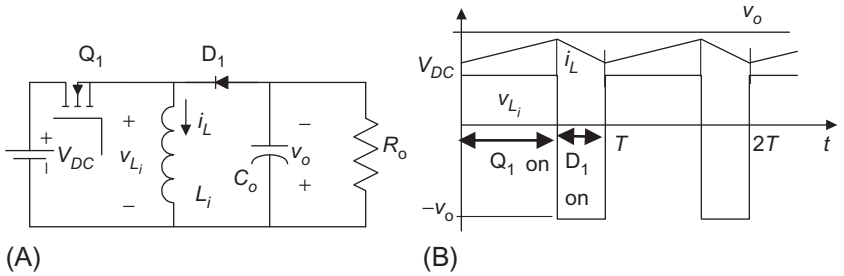


FIG. 35.1 (A) Basic circuit of the buck-boost dc/dc converter and (B) ideal waveforms.

$$\begin{aligned} L_i\frac{di_L}{dt} &= -v_o \\ C_o\frac{dv_o}{dt} &= i_L - \frac{v_o}{R_o} \end{aligned} \quad \text{for } \delta_1 T \le t \le T \quad (\delta(t)=0;\ Q_1 \text{ is off and } D_1 \text{ is on}) \tag{35.10}$$

Comparing Eqs. (35.9) and (35.10) with Eqs. (35.2) and (35.3) and considering $\mathbf{y}=[v_o,\ i_L]^T$, the following matrices can be identified:

$$\mathbf{A}_1=\begin{bmatrix}0 & 0\\ 0 & -1/(R_oC_o)\end{bmatrix};\ \mathbf{A}_2=\begin{bmatrix}0 & -1/L_i\\ -1/C_o & -1/(R_oC_o)\end{bmatrix};$$

$$\mathbf{B}_1=[1/L_i,0]^T;\ \mathbf{B}_2=[0,0]^T;\ \mathbf{u}=[V_{DC}];$$

$$\mathbf{C}_1=\begin{bmatrix}0 & 1\\ 1 & 0\end{bmatrix};\ \mathbf{C}_2=\begin{bmatrix}0 & 1\\ 1 & 0\end{bmatrix};$$

$$\mathbf{D}_1=[0,0]^T;\ \mathbf{D}_2=[0,0]^T$$

From Eqs. (35.4) and (35.5), the switched state-space model of this switching converter is

$$\begin{aligned} \begin{bmatrix}\dot{i}_L\\ \dot{v}_o\end{bmatrix} &= \begin{bmatrix}0 & -(1-\delta(t))/L_i\\ (1-\delta(t))/C_o & -1/(R_oC_o)\end{bmatrix}\begin{bmatrix}i_L\\ v_o\end{bmatrix}+\begin{bmatrix}\delta(t)/L_i\\ 0\end{bmatrix}V_{DC}\\ \begin{bmatrix}v_o\\ i_L\end{bmatrix} &= \begin{bmatrix}0 & 1\\ 1 & 0\end{bmatrix}\begin{bmatrix}i_L\\ v_o\end{bmatrix}+\begin{bmatrix}0\\ 0\end{bmatrix}[V_{DC}] \end{aligned} \tag{35.11}$$

Now, applying Eq. (35.7), Eqs. (35.12) and (35.13) can be obtained:

$$\begin{aligned} \begin{bmatrix}\dot{\bar{i}}_L\\ \dot{\bar{v}}_o\end{bmatrix} &= \left(\begin{bmatrix}0 & 0\\ 0 & -1/(R_oC_o)\end{bmatrix}\delta_1+\begin{bmatrix}0 & -1/L_i\\ 1/C_o & -1/R_oC_o\end{bmatrix}\delta_2\right)\\ &\quad\times\begin{bmatrix}\bar{i}_L\\ \bar{v}_o\end{bmatrix}+\left(\begin{bmatrix}1/L_i\\ 0\end{bmatrix}\delta_1+\begin{bmatrix}0\\ 0\end{bmatrix}\delta_2\right)[\overline{V}_{DC}] \end{aligned} \tag{35.12}$$

$$\begin{aligned} \begin{bmatrix}\bar{v}_o\\ \bar{i}_L\end{bmatrix} &= \left(\begin{bmatrix}0 & 1\\ 1 & 0\end{bmatrix}\delta_1+\begin{bmatrix}0 & 1\\ 1 & 0\end{bmatrix}\delta_2\right)\begin{bmatrix}\bar{i}_L\\ \bar{v}_o\end{bmatrix}\\ &\quad+\left(\begin{bmatrix}0\\ 0\end{bmatrix}\delta_1+\begin{bmatrix}0\\ 0\end{bmatrix}\delta_2\right)[\overline{V}_{DC}] \end{aligned} \tag{35.13}$$

From Eqs. (35.12) and (35.13), the state-space averaged model, written as a function of δ_1, is

$$\begin{bmatrix}\dot{\bar{i}}_L\\ \dot{\bar{v}}_o\end{bmatrix}=\begin{bmatrix}0 & -(1-\delta_1)/L_i\\ (1-\delta_1)/C_o & -1/(R_oC_o)\end{bmatrix}\begin{bmatrix}\bar{i}_L\\ \bar{v}_o\end{bmatrix}+\begin{bmatrix}\delta_1/L_i\\ 0\end{bmatrix}[\overline{V}_{DC}] \tag{35.14}$$

$$\begin{bmatrix}\bar{v}_o\\ \bar{i}_L\end{bmatrix}=\begin{bmatrix}0 & 1\\ 1 & 0\end{bmatrix}\begin{bmatrix}\bar{i}_L\\ \bar{v}_o\end{bmatrix}+\begin{bmatrix}0\\ 0\end{bmatrix}[\overline{V}_{DC}] \tag{35.15}$$

The eigenvalues $s_{bb_{1,2}}$ or characteristic roots of $\mathbf{A}$ are the roots of $|s\mathbf{I}-\mathbf{A}|$. Therefore,

$$s_{bb_{1,2}}=\frac{-1}{2R_oC_o}\pm\sqrt{\frac{1}{4(R_oC_o)^2}-\frac{(1-\delta_1)^2}{L_iC_o}} \tag{35.16}$$

Since λ_{max} is the maximum of the absolute values of all the eigenvalues of $\mathbf{A}$, the model (35.14) and (35.15) is valid for switching frequencies f_s ($f_s=1/T$) that verify $\lambda_{max}T\ll 1$. Therefore, as $T\ll 1/\lambda_{max}$, the values of T that approximately verify this restriction are $T\ll 1/\max(|s_{bb1,2}|)$. Given these buck-boost converter data, $T\ll 2$ ms is obtained. Therefore, the converter switching frequency must obey $f_s\gg\max(|s_{bb1,2}|)$, implying switching frequencies above, say, 5 kHz. Consequently, the buck-boost switching frequency, the inductor value, and the capacitor value were chosen accordingly.

This restriction can be further used to discuss the maximum frequency ω_{max} for which the state-space averaged model is still valid, given a certain switching frequency. As λ_{max} can be regarded as a frequency, the preceding constraint brings $\omega_{max}\ll 2\pi f_s$, say $\omega_{max}<2\pi f_s/10$, which means that the state-space averaged model is a good approximation at frequencies under one-tenth of the power converter switching frequency.

The state-space averaged model (35.14) and (35.15) is also the state-space model of the circuit represented in Fig. 35.2. Hence, this circuit is often named "the averaged equivalent circuit" of the buck-boost converter and allows the determination, under small ripple and slow variations, of the average equivalent circuit of the converter switching cell (power transistor plus diode).

The average equivalent circuit of the switching cell (Fig. 35.3A) is represented in Fig. 35.3B and emerges directly from the state-space averaged model (35.14) and (35.15). This equivalent circuit can be viewed as the model of an "ideal transformer" (Fig. 35.3C), whose primary to secondary

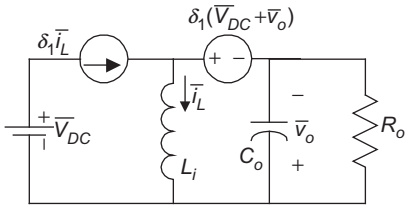


FIG. 35.2 Equivalent circuit of the averaged state-space model of the buck-boost converter.

ratio (v_1/v_2) can be calculated applying Kirchhoff's voltage law to obtain $-v_1+v_s-v_2=0$. As $v_2=\delta_1 v_s$, it follows that $v_1=v_s(1-\delta_1)$, giving $(v_1/v_2)=(1-\delta_1)/\delta_1$. The same ratio could be obtained beginning with $i_L=i_1+i_2$ and $i_1=\delta_1 i_L$ (Fig. 35.3B), which gives $i_2=i_L(1-\delta_1)$ and $(i_2/i_1)=\delta_2/\delta_1$.

The average equivalent circuit concept, obtained from Eq. (35.7) or Eqs. (35.14) and (35.15), can be applied to other switching converters, with or without a similar switching cell, to obtain transfer functions or to simulate the converter average behavior. The average equivalent circuit of the switching cell can be applied to converters with the same switching cell operating in the continuous conduction mode. However, note that the state variables of Eq. (35.7) or Eqs. (35.14) and (35.15) are the mean values of the converter instantaneous variables and, therefore, do not represent their ripple components. The inputs of the state-space averaged model are the mean values of the converter inputs over one switching period.

35.2.2.3 Linearized State-Space Averaged Model

The converter outputs $\overline{\mathbf{y}}$ must be regulated actuating on the duty cycle $\delta(t)$, and the converter inputs $\bar{\mathbf{u}}$ usually present perturbations due to the load and power supply variations. State variables are decomposed in small ac perturbations (denoted by "~") and dc steady-state quantities (represented by uppercase letters). Therefore,

$$\begin{aligned}\overline{\mathbf{x}}&=\mathbf{X}+\widetilde{\mathbf{x}}\\ \overline{\mathbf{y}}&=\mathbf{Y}+\widetilde{\mathbf{y}}\\ \overline{\mathbf{u}}&=\mathbf{U}+\widetilde{\mathbf{u}}\\ \delta_1&=\Delta_1+\widetilde{\delta}\\ \delta_2&=\Delta_2-\widetilde{\delta}\end{aligned}\tag{35.17}$$

Using Eq. (35.17) in Eq. (35.7) and rearranging terms, it is obtained:

$$\begin{aligned}\dot{\widetilde{\mathbf{x}}}=&[\mathbf{A}_1\Delta_1+\mathbf{A}_2\Delta_2]\mathbf{X}+[\mathbf{B}_1\Delta_1+\mathbf{B}_2\Delta_2]\mathbf{U}\\&+[\mathbf{A}_1\Delta_1+\mathbf{A}_2\Delta_2]\widetilde{\mathbf{x}}+[(\mathbf{A}_1-\mathbf{A}_2)\mathbf{X}+(\mathbf{B}_1-\mathbf{B}_2)\mathbf{U}]\widetilde{\delta}\\&+[\mathbf{B}_1\Delta_1+\mathbf{B}_2\Delta_2]\widetilde{\mathbf{u}}+[(\mathbf{A}_1-\mathbf{A}_2)]\widetilde{\mathbf{x}}+(\mathbf{B}_1-\mathbf{B}_2)\widetilde{\mathbf{u}}]\widetilde{\delta}\end{aligned}\tag{35.18}$$

$$\begin{aligned}\mathbf{Y}+\widetilde{\mathbf{y}}=&[\mathbf{C}_1\Delta_1+\mathbf{C}_2\Delta_2]\mathbf{X}+[\mathbf{D}_1\Delta_1+\mathbf{D}_2\Delta_2]\mathbf{U}\\&+[\mathbf{C}_1\Delta_1+\mathbf{C}_2\Delta_2]\widetilde{\mathbf{x}}+[(\mathbf{C}_1-\mathbf{C}_2)\mathbf{X}+(\mathbf{D}_1-\mathbf{D}_2)\mathbf{U}]\widetilde{\delta}\\&+[\mathbf{D}_1\Delta_1+\mathbf{D}_2\Delta_2]\widetilde{\mathbf{u}}+[(\mathbf{C}_1-\mathbf{C}_2)]\widetilde{\mathbf{x}}+(\mathbf{D}_1-\mathbf{D}_2)\widetilde{\mathbf{u}}]\widetilde{\delta}\end{aligned}\tag{35.19}$$

The terms $[\mathbf{A}_1\Delta_1+\mathbf{A}_2\ \Delta_2]\ \mathbf{X}+[\mathbf{B}_1\ \Delta_1+\mathbf{B}_2\ \Delta_2]\ \mathbf{U}$ and $[\mathbf{C}_1\ \Delta_1+\mathbf{C}_2\ \Delta_2]\ \mathbf{X}+[\mathbf{D}_1\ \Delta_1+\mathbf{D}_2\ \Delta_2]\ \mathbf{U}$, respectively, from Eqs. (35.18) and (35.19) represent the steady-state behavior of the system. As in steady-state $\dot{\mathrm{X}}=0$, the following relationships hold:

$$\mathbf{0}=[\mathbf{A}_1\Delta_1+\mathbf{A}_2\Delta_2]\mathbf{X}+[\mathbf{B}_1\Delta_1+\mathbf{B}_2\Delta_2]\mathbf{U}\tag{35.20}$$

$$\mathbf{Y}=[\mathrm{C}_1\Delta_1+\mathbf{C}_2\Delta_2]\mathbf{X}+[\mathbf{D}_1\Delta_1+\mathbf{D}_2\Delta_2]\mathbf{U}\tag{35.21}$$

Neglecting higher-order terms $([(\mathbf{A}_1-\mathbf{A}_2)\widetilde{\mathbf{x}}+(\mathbf{B}_1-\mathbf{B}_2)\widetilde{\mathbf{u}}])\widetilde{\delta}\approx 0$ of Eqs. (35.18) and (35.19), the linearized small-signal state-space averaged model is

$$\begin{aligned}\dot{\widetilde{\mathbf{x}}}=&[\mathbf{A}_1\Delta_1+\mathbf{A}_2\Delta_2]\widetilde{\mathbf{x}}+[(\mathbf{A}_1-\mathbf{A}_2)\mathbf{X}+(\mathbf{B}_1-\mathbf{B}_2)\mathbf{U}]\widetilde{\delta}\\&+[\mathbf{B}_1\Delta_1+\mathbf{B}_2\Delta_2]\widetilde{\mathbf{u}}\\\widetilde{\mathbf{y}}=&[\mathbf{C}_1\Delta_1+\mathbf{C}_2\Delta_2]\widetilde{\mathbf{x}}+[(\mathbf{C}_1-\mathbf{C}_2)\mathbf{X}+(\mathbf{D}_1-\mathbf{D}_2)\mathbf{U}]\widetilde{\delta}\\&+[\mathbf{D}_1\Delta_1+\mathbf{D}_2\Delta_2]\widetilde{\mathbf{u}}\end{aligned}\tag{35.22}$$

or

$$\begin{aligned}\dot{\widetilde{\mathbf{x}}}&=\mathbf{A}_{av}\widetilde{\mathbf{x}}+\mathbf{B}_{av}\widetilde{\mathbf{u}}+[(\mathbf{A}_1-\mathbf{A}_2)\mathbf{X}+(\mathbf{B}_1-\mathbf{B}_2)\mathbf{U}]\widetilde{\delta}\\\widetilde{\mathbf{y}}&=\mathbf{C}_{av}\widetilde{\mathbf{x}}+\mathbf{D}_{av}\widetilde{\mathbf{u}}+[(\mathbf{C}_1-\mathbf{C}_2)\mathbf{X}+(\mathbf{D}_1-\mathbf{D}_2)\mathbf{U}]\widetilde{\delta}\end{aligned}\tag{35.23}$$

with

$$\begin{aligned}\mathbf{A}_{av}&=[\mathbf{A}_1\Delta_1+\mathbf{A}_2\Delta_2]\\\mathbf{B}_{av}&=[\mathbf{B}_1\Delta_1+\mathbf{B}_2\Delta_2]\\\mathbf{C}_{av}&=[\mathbf{C}_1\Delta_1+\mathbf{C}_2\Delta_2]\\\mathbf{D}_{av}&=[\mathbf{D}_1\Delta_1+\mathbf{D}_2\Delta_2]\end{aligned}\tag{35.24}$$

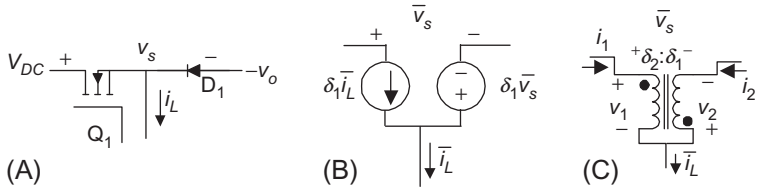


FIG. 35.3 Average equivalent circuit of the switching cell: (A) switching cell, (B) average equivalent circuit, and (C) average equivalent circuit using an ideal transformer.

35.2.3 Converter Transfer Functions

Using Eq. (35.20) in Eq. (35.21), the input **U** to output **Y** steady-state relations (35.25), needed for open-loop and feedforward control, can be obtained:

$$\frac{\mathbf{Y}}{\mathbf{U}} = -\mathbf{C}_{av}\mathbf{A}_{av}^{-1}\mathbf{B}_{av} + \mathbf{D}_{av} \tag{35.25}$$

Applying Laplace transforms to Eq. (35.23) with zero initial conditions and using the superposition theorem, the small-signal duty-cycle $\widetilde{\delta}$ -to-output $\tilde{y}$ transfer functions (35.26) can be obtained considering zero line perturbations ($\tilde{u}=0$):

$$\begin{aligned}\frac{\widetilde{\mathbf{y}}(s)}{\widetilde{\delta}(s)} = {} & \mathbf{C}_{av}[s\mathbf{I}-\mathbf{A}_{av}]^{-1}[(\mathbf{A}_1-\mathbf{A}_2)\mathbf{X}+(\mathbf{B}_1-\mathbf{B}_2)\mathbf{U}] \\ & +[(\mathbf{C}_1-\mathbf{C}_2)\mathbf{X}+(\mathbf{D}_1-\mathbf{D}_2)\mathbf{U}]\end{aligned} \tag{35.26}$$

The line-to-output transfer function (or audio susceptibility transfer function) (35.27) is derived using the same method, considering now zero small-signal duty-cycle perturbations $\left(\widetilde{\delta}=0\right)$:

$$\frac{\widetilde{\mathbf{y}}(s)}{\widetilde{\mathbf{u}}(s)} = \mathbf{C}_{av}[s\mathbf{I}-\mathbf{A}_{av}]^{-1}\mathbf{B}_{av} + \mathbf{D}_{av} \tag{35.27}$$

Example 35.2 Buck–Boost dc/dc converter transfer functions

From Eqs. (35.14) and (35.15) of Example 35.1 and Eq. (35.23), making $\mathbf{X}=[I_L,\ V_o]^{\mathrm{T}}$, $\mathbf{Y}=[V_o,\ I_L]^{\mathrm{T}}$ and $\mathbf{U}=[V_{DC}]$, the linearized small-signal state-space model of the buck-boost converter is

$$\begin{aligned}\begin{bmatrix}\dot{\widetilde{i}}_L\\ \dot{\widetilde{v}}_o\end{bmatrix} &= \begin{bmatrix}0 & -(1-\Delta_1)/L_i\\ (1-\Delta_1)/C_o & -1/(R_oC_o)\end{bmatrix}\begin{bmatrix}\widetilde{i}_L\\ \widetilde{v}_o\end{bmatrix} + \begin{bmatrix}\Delta_1/L_i\\ 0\end{bmatrix}[\widetilde{v}_{DC}] \\ &+ \begin{bmatrix}0 & \widetilde{\delta}/L_i\\ -\widetilde{\delta}/C_o & 0\end{bmatrix}\begin{bmatrix}I_L\\ V_o\end{bmatrix} + \begin{bmatrix}V_{DC}/L_i\\ 0\end{bmatrix}[\widetilde{\delta}] \\ \begin{bmatrix}\widetilde{v}_o\\ \widetilde{i}_L\end{bmatrix} &= \begin{bmatrix}0 & 1\\ 1 & 0\end{bmatrix}\begin{bmatrix}\widetilde{i}_L\\ \widetilde{v}_o\end{bmatrix} + \begin{bmatrix}0\\ 0\end{bmatrix}[\widetilde{v}_{DC}]\end{aligned} \tag{35.28}$$

From Eqs. (35.24) and (35.28), the following matrices are identified:

$$\mathbf{A}_{av} = \begin{bmatrix}0 & -(1-\Delta_1)/L_i\\ (1-\Delta_1)/C_0 & -1/(R_oC_o)\end{bmatrix};\ \mathbf{B}_{av} = \begin{bmatrix}\Delta_1/L_i\\ 0\end{bmatrix};$$
$$\mathbf{C}_{av} = \begin{bmatrix}0 & 1\\ 1 & 0\end{bmatrix};\ \mathbf{D}_{av} = \begin{bmatrix}0\\ 0\end{bmatrix} \tag{35.29}$$

The averaged linear equivalent circuit, resulting from Eq. (35.28) or from the linearization of the averaged equivalent circuit (Fig. 35.2) derived from Eqs. (35.14) and (35.15), now includes the small-signal current source $\widetilde{\delta}I_L$ in parallel with the current source $\Delta_1\tilde{i}_L$ and the small-signal voltage source $\widetilde{\delta}(V_{DC}+V_o)$ in series with the voltage source $\Delta_1(\widetilde{v}_{dc}+\widetilde{v}_o)$. The supply voltage source $\overline{V}_{DC}$ is replaced by the voltage source $\widetilde{v}_{DC}$.

Using Eq. (35.29) in Eq. (35.25), the *input U to output Y steady-state relations* are

$$\frac{I_L}{V_{DC}} = \frac{\Delta_1}{R_o(\Delta_1-1)^2} \tag{35.30}$$

$$\frac{V_o}{V_{DC}} = \frac{\Delta_1}{1-\Delta_1} \tag{35.31}$$

These relations are the well-known steady-state transfer relationships of the buck-boost converter [2,5,6]. For open-loop control of the V_o output, knowing the nominal value of the power supply V_{DC} and the required V_o, the value of Δ_1 can be offline calculated from Eq. (35.31) ($\Delta_1 = V_o/(V_o+V_{DC})$). A modulator such as that described in Section 35.2.4, with the modulation signal proportional to Δ_1, would generate the signal $\delta(t)$. The open-loop control for fixed output voltages is possible, if the power supply V_{DC} is almost constant and the converter load does not change significantly. If the V_{DC} value presents disturbances, then the feedforward control can be used, calculating Δ_1 online, so that its value will always be in accordance with Eq. (35.31). The correct V_o value will be attained at steady state, despite input voltage variations. However, because of converter parasitic reactances, not modeled here (see Example 35.3), in practice, a steady-state error would appear. Moreover, the transient dynamics imposed by the converter would present overshoots, being often not suited for demanding applications.

From Eq. (35.27), the *line-to-output transfer functions* are

$$\frac{\widetilde{i}_L(s)}{\widetilde{v}_{DC}(s)} = \frac{\Delta_1(1+sC_oR_o)}{s^2L_iC_oR_o + sL_i + R_o(1-\Delta_1)^2} \tag{35.32}$$

$$\frac{\widetilde{v}_o(s)}{\widetilde{v}_{DC}(s)} = \frac{R_o\Delta_1(1-\Delta_1)}{s^2L_iC_oR_o + sL_i + R_o(1-\Delta_1)^2} \tag{35.33}$$

From Eq. (35.26), *the small-signal duty-cycle $\widetilde{\delta}$ -to-output $\tilde{y}$ transfer functions are*

$$\frac{\widetilde{i}_L(s)}{\widetilde{\delta}(s)} = \frac{V_{DC}(1+\Delta_1+sC_oR_o)/(1-\Delta_1)}{s^2L_iC_oR_o + sL_i + R_o(1-\Delta_1)^2} \tag{35.34}$$

$$\frac{\widetilde{v}_o(s)}{\widetilde{\delta}(s)} = \frac{V_{DC}(R_o-sL_i\Delta_1)/(1-\Delta_1)^2)}{s^2L_iC_oR_o + sL_i + R_o(1-\Delta_1)^2} \tag{35.35}$$

These transfer functions enable the choice and feedback loop design of the compensation network. Note the positive zero in $\widetilde{v}_o(s)/\widetilde{\delta}(s)$, pointing out a nonminimum-phase

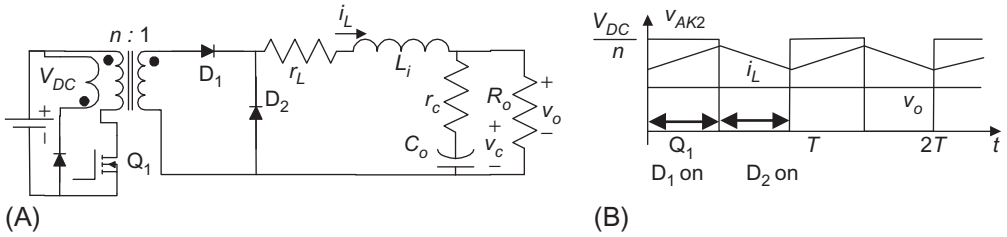


FIG. 35.4 (A) Basic circuit of the forward dc/dc converter and (B) circuit main waveforms.

system. These equations could also be obtained using the small-signal equivalent circuit derived from Eq. (35.28) or from the linearized model of the switching cell (Fig. 35.3B), substituting the current source $\delta_1 \bar{i}_L$ by the current sources $\Delta_1 \tilde{i}_L$ and $\tilde{\delta} I_L$ in parallel and the voltage source $\delta_1 \bar{v}_s$ by the voltage sources $\Delta_1(\tilde{v}_{DC} + \tilde{v}_o)$ and $\tilde{\delta}(V_{DC} + V_o)$ in series.

EXAMPLE 35.3 Transfer functions of the forward dc/dc converter

Consider the forward (buck-derived) converter of Fig. 35.4 switching at $f_s = 100$ kHz ($T = 10$ μs) with $V_{DC} = 300$ V, $n = 30$, $V_o = 5$ V, $L_i = 20$ μH, $r_L = 0.01\ \Omega$, $C_o = 2200$ μF, $r_C = 0.005\ \Omega$, and $R_o = 0.1\ \Omega$.

Assuming $\mathbf{x} = [i_L, v_C]^T$, $\delta(t) = 1$ when both Q_1 and D_1 are on and D_2 is off ($0 \le t \le \delta_1 T$), and $\delta(t) = 0$ when both Q_1 and D_1 are off and D_2 is on ($\delta_1 T \le t \le T$), the switched state-space model of the forward converter, considering as output vector $\mathbf{y} = [i_L, v_o]^T$, is

$$\begin{aligned}
\frac{di_L}{dt} &= -\frac{(R_o r_C + R_o r_L + r_L r_C)}{L_i(R_o + r_C)} i_L \\
&\quad - \frac{R_o}{L_i(R_o + r_C)} v_c + \frac{\delta(t)}{n} V_{DC} \\
\frac{dv_C}{dt} &= \frac{R_o}{(R_o + r_C)C_o} i_L - \frac{1}{(R_o + r_C)C_o} v_C \\
v_o &= \frac{r_C}{1 + r_C/R_o} i_L + \frac{1}{1 + r_C/R_o} v_C
\end{aligned} \tag{35.36}$$

Making $r_{cm} = r_C/(1 + r_C/R_o)$, $R_{oc} = R_o + r_C$, $k_{oc} = R_o/R_{oc}$, and $r_P = r_L + r_{cm}$ and comparing Eq. (35.36) with Eqs. (35.2) and (35.3), the following matrices can be identified:

$$\mathbf{A}_1 = \mathbf{A}_2 = \begin{bmatrix} -r_p/L_i & -k_{oc}/L_i \\ k_{oc}/C_o & -1/(R_{oc}C_o) \end{bmatrix};$$

$$\mathbf{B}_1 = [1/(nL_i), 0]^T;\ \mathbf{B}_2 = [0\ 0]^T;\ \mathbf{u} = [V_{DC}]$$

$$\mathbf{C}_1 = \mathbf{C}_2 = \begin{bmatrix} 1 & 0 \\ r_{cm} & k_{oc} \end{bmatrix};\ \mathbf{D}_1 = \mathbf{D}_2 = [00]^T$$

Now, applying Eq. (35.7), the exact (since $\mathbf{A}_1 = \mathbf{A}_2$) state-space averaged model (35.37) and (35.38) is obtained:

$$\begin{bmatrix} \dot{\bar{i}}_L \\ \dot{\bar{v}}_C \end{bmatrix} = \begin{bmatrix} -r_p/L_i & -k_{oc}/L_i \\ k_{oc}/C_o & -1/(R_{oc}C_o) \end{bmatrix} \begin{bmatrix} \bar{i}_L \\ \bar{v}_C \end{bmatrix} + \begin{bmatrix} \delta_1/(nL_i) \\ 0 \end{bmatrix} [\bar{V}_{DC}] \tag{35.37}$$

$$\begin{bmatrix} \bar{i}_L \\ \bar{v}_o \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ r_{cm} & k_{oc} \end{bmatrix} \begin{bmatrix} \bar{i}_L \\ \bar{v}_o \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} [\bar{V}_{DC}] \tag{35.38}$$

Since $\mathbf{A}_1 = \mathbf{A}_2$, this model is valid for $\omega_{max} < 2\pi f_s$. The converter eigenvalues $s_{f_{1,2}}$ are

$$s_{f_{1,2}} = -\frac{L_i + C_o R_{oc} r_p}{2R_{oc}L_i C_o} \pm \frac{\sqrt{-4R_{oc}L_i C_o\left(R_{oc}k_{oc}^2 + r_p\right) + \left(L_i + C_o R_{oc} r_p\right)^2}}{2R_{oc}L_i C_o} \tag{35.39}$$

The equivalent circuit arising from Eqs. (35.37) and (35.38) is represented in Fig. 35.5. It could also be obtained with the concept of the switching cell equivalent circuit Fig. 35.3 of Example (35.1).

Making $\mathbf{X} = [I_L, V_C]^T$, $\mathbf{Y} = [I_L, V_o]^T$ and $\mathbf{U} = [V_{DC}]$, from Eq. (35.23), the small-signal state-space averaged model is

$$\begin{bmatrix} \dot{\tilde{i}}_L \\ \dot{\tilde{v}}_C \end{bmatrix} = \begin{bmatrix} -r_p/L_i & -k_{oc}/L_i \\ k_{oc}/C_o & -1/(R_{oc}C_o) \end{bmatrix} \begin{bmatrix} \tilde{i}_L \\ \tilde{v}_C \end{bmatrix} + \begin{bmatrix} \Delta_1/(nL_i) \\ 0 \end{bmatrix} [\tilde{v}_{DC}] + \begin{bmatrix} V_{DC}/(nL_i) \\ 0 \end{bmatrix} [\tilde{\delta}] \tag{35.40}$$

$$\begin{bmatrix} \tilde{i}_L \\ \tilde{v}_o \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ r_{cm} & k_{oc} \end{bmatrix} \begin{bmatrix} \tilde{i}_L \\ \tilde{v}_C \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} [\tilde{v}_{DC}] \tag{35.41}$$

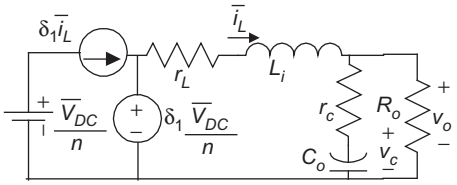


FIG. 35.5 Equivalent circuit of the averaged state-space model of the forward converter.

From Eq. (35.25), the input **U** to output **Y** steady-state relations are

$$\frac{I_L}{V_{DC}} = \frac{\Delta_1}{n\left(k_{oc}^2 R_{oc} + r_p\right)} \tag{35.42}$$

$$\frac{V_o}{V_{DC}} = \frac{\Delta_1\left(k_{oc}^2 R_{oc} + r_{cm}\right)}{n\left(k_{oc}^2 R_{oc} + r_p\right)} \tag{35.43}$$

Making $r_C = 0$, $r_L = 0$, and $n = 1$, the former relations give the well-known dc transfer relationships of the buck dc/dc converter. Relations (35.42) and (35.43) allow the open-loop and feedforward control of the converter, as discussed in Example 35.2, provided that all the modeled parameters are time-invariant and accurate enough.

From Eq. (35.27), the line-to-output transfer functions are derived:

$$\frac{\widetilde{i}_L(s)}{\widetilde{v}_{DC}(s)} = \frac{(\Delta_1/n)(1 + sC_oR_{oc})}{s^2L_iC_oR_{oc} + s\left(L_i + C_oR_{oc}r_p\right) + k_{oc}^2R_{oc} + r_p} \tag{35.44}$$

$$\frac{\widetilde{v}_o(s)}{\widetilde{v}_{DC}(s)} = \frac{(\Delta_1/n)\left(k_{oc}^2R_{oc} + r_{cm} + sC_oR_{oc}r_{cm}\right)}{s^2L_iC_oR_{oc} + s\left(L_i + C_oR_{oc}r_p\right) + k_{oc}^2R_{oc} + r_p} \tag{35.45}$$

Using Eq. (35.26), the small-signal duty-cycle $\widetilde{\delta}$-to-output $\tilde{y}$ transfer functions are

$$\frac{\widetilde{i}_L(s)}{\delta(s)} = \frac{(V_{DC}/n)(1 + sC_oR_{oc})}{s^2L_iC_oR_{oc} + s\left(L_i + C_oR_{oc}r_p\right) + k_{oc}^2R_{oc} + r_p} \tag{35.46}$$

$$\frac{\widetilde{v}_o(s)}{\delta(s)} = \frac{(V_{DC}/n)\left(k_{oc}^2R_{oc} + r_{cm} + sC_oR_{oc}r_{cm}\right)}{s^2L_iC_oR_{oc} + s\left(L_i + C_oR_{oc}r_p\right) + k_{oc}^2R_{oc} + r_p} \tag{35.47}$$

The real zero of Eq. (35.47) is due to r_C, the equivalent series resistance (ESR) of the output capacitor. A similar zero would occur in the buck-boost converter (Example 35.2), if the ESR of the output capacitor had been included in the modeling.

35.2.4 Pulse Width Modulator Transfer Functions

In what is often referred to as the pulse-width-modulation (PWM) voltage-mode control, the output voltage $u_c(t)$ of the error (between desired and actual output) amplifier plus regulator, processed if needed, is compared with a repetitive or carrier waveform $r(t)$, to obtain the switching variable $\delta(t)$ (Fig. 35.6A). This function controls the power switch, turning it on at the beginning of the period and turning it off when the ramp exceeds the $u_c(t)$ voltage. In Fig. 35.6B, the opposite occurs (turnoff at the end of the period and turn-on when the $u_c(t)$ voltage exceeds the ramp).

Considering $r(t)$ as represented in Fig. 35.6A ($r(t) = u_{cmax}t/T$), δ_k is obtained equating $r(t) = u_c$ giving $\delta_k = u_c\ (t)/u_{cmax}$ or $\delta_k/u_c\ (t) = G_M$ ($G_M = 1/u_{cmax}$). In Fig. 35.6B, the switching-on angle α_k is obtained from $r(t) = u_{cmax} - 2u_{cmax}\omega t/\pi$ and $u_c\ (t) = u_{cmax} - 2u_{cmax}\ \alpha_k/\pi$, giving $\alpha_k = (\pi/2) \times (1 - u_c/u_{cmax})$ and $G_M = \partial\alpha_k/\partial u_c = -\pi/(2u_{cmax})$.

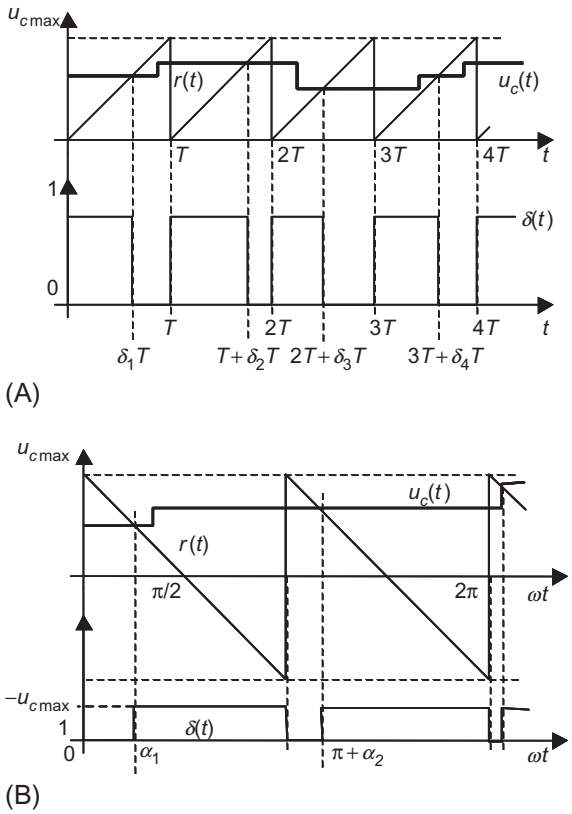


FIG. 35.6 Waveforms of pulse-width modulators showing the variable time delays of the modulator response: (A) $r(t) = u_{cmax}\ t/T$ and (B) $r(t) = u_{cmax} - 2u_{cmax}\ \omega t/\pi$.

Since, after turnoff or turn-on, any control action variation of $u_c(t)$ will only affect the converter duty cycle in the next period (or sample for digital hardware), a time delay is introduced in the control loop. For simplicity, with small-signal perturbations around the operating point, this delay is assumed almost constant and equal to its mean value ($T/2$). Then, the transfer function of the PWM modulator is

$$\frac{\widetilde{\delta}(s)}{\widetilde{u}_c(s)} = G_M e^{-sT/2} = \frac{G_M}{e^{s(T/2)}} = \frac{G_M}{1 + s\frac{T}{2} + \frac{s^2}{2!}\left(\frac{T}{2}\right)^2 + \ldots + \frac{s^j}{j!}\left(\frac{T}{2}\right)^j + \ldots} \approx \frac{G_M}{1 + s\frac{T}{2}} \tag{35.48}$$

The final approximation of Eq. (35.48), valid for $\omega T/2 < \sqrt{2}/2$, [7] suggests that the PWM modulator can be considered as an amplifier with gain G_M and a dominant pole. Notice that this pole occurs at a frequency doubling the switching frequency, and most state-space averaged models are valid only for frequencies below one-tenth of the switching frequency.

Therefore, in most situations, this modulator pole can be neglected, being simply $\delta(s) = G_M u_c(s)$, as the dominant pole of Eq. (35.48) stays at least one decade to the left of the dominant poles of the converter.

35.2.5 Linear Feedback Design Ensuring Stability

In the application of classical linear feedback control to switching power converters, Bode plots and root locus are, usually, suitable methods to assess system performance and stability. General rules for the design of the compensated open-loop transfer function are as follows:

The low-frequency gain should be high enough to minimize output steady-state errors.

The frequency of 0 dB gain (unity gain), ω_{0dB}, should be placed close to the maximum allowed by the modeling approximations ($\lambda_{max} T \ll 1$), to allow fast response to transients. In practice, this frequency should be almost an order of magnitude lower than the switching frequency.

To ensure stability, the phase margin, defined as the additional phase shift needed to render the system unstable without gain changes (or the difference between the open-loop system phase at ω_{0dB} and $-180°$), must be positive and in general greater than 30° (45 − 70° is desirable). In the root locus, no poles should enter the right half of the complex plane.

To increase stability, the gain should be less than −30 dB at the frequency where the phase reaches −180° (gain margin greater than 30 dB).

Transient behavior and stability margins are related: The obtained damping factor is generally 0.01 times the phase margin (in degrees), and overshoot (in percent) is given approximately by 75° minus the phase margin. The product of the rise time (in seconds) and the closed-loop bandwidth (in rad/s) is close to 2.8.

To guarantee gain and phase margins, the following series compensation transfer functions (usually implemented with operational amplifiers) are often used [8]:

35.2.5.1 Types of Compensation

Lag and lead compensation

Lag compensation should be used in converters with good stability margin but poor steady-state accuracy. If the frequencies $1/T_p$ and $1/T_z$ of Eq. (35.49) with $1/T_p < 1/T_z$ are chosen sufficiently below the unity gain frequency, lag-lead compensation lowers the loop gain at high frequency but maintains the phase unchanged for frequencies $f \gg 1/T_z$. Then, the dc gain can be increased to reduce the steady-state error without significantly decreasing the phase margin:

$$C_{LL}(s) = k_{LL}\frac{1+sT_z}{1+sT_p} = k_{LL}\frac{T_z}{T_p}\frac{s+1/T_z}{s+1/T_p} \tag{35.49}$$

Lead compensation can be used in converters with good steady-state accuracy but poor stability margin. If the frequencies $1/T_p$ and $1/T_z$ of Eq. (35.49) with $1/T_p > 1/T_z$ are chosen below the unity gain frequency, lead-lag compensation increases the phase margin without significantly affecting the steady-state error. The T_p and T_z values are chosen to increase the phase margin, fastening the transient response and increasing the bandwidth.

Proportional–Integral compensation

Proportional-integral (PI) compensators (35.50) are used to guarantee null steady-state error with acceptable rise times. The PI compensators are a particular case of lag-lead compensators, therefore suitable for converters with good stability margin but poor steady-state accuracy:

$$\begin{aligned} C_{PI}(s) &= \frac{1+sTz}{sT_p} = \frac{T_z}{T_p} + \frac{1}{sT_p} = K_p + \frac{K_i}{s} = K_p\left(1+\frac{K_i}{K_p s}\right) \\ &= K_p\left(1+\frac{1}{sT_z}\right) = \frac{1+sT_z}{sT_z/K_p} \end{aligned} \tag{35.50}$$

Proportional–integral plus high-frequency pole compensation

This integral plus zero-pole compensation (35.51) combines the advantages of a PI with lead or lag compensation. It can be used in converters with good stability margin but poor steady-state accuracy. If the frequencies $1/T_M$ and $1/T_z$ ($1/T_z < 1/T_M$) are carefully chosen, compensation lowers the loop gain at high frequency while only slightly lowering the phase to achieve the desired phase margin:

$$\begin{aligned} C_{ILD}(s) &= \frac{1+sT_z}{sT_p(1+sT_M)} = \frac{T_z}{T_p T_M}\frac{s+1/T_z}{s(s+1/T_M)} \\ &= W_{cp}\frac{s+\omega_z}{s(s+\omega_M)} \end{aligned} \tag{35.51}$$

Proportional-integral derivative (PID), plus high-frequency poles

The PID notch filter type (35.52) scheme is used in converters with two lightly damped complex poles, to increase the response speed, while ensuring zero steady-state error. In most switching power converters, the two complex zeros are selected to have a damping factor greater than the converter complex poles and slightly smaller oscillating frequency. The high-frequency pole is placed to achieve the needed phase margin [9]. The design is correct if the complex pole loci, heading to the complex zeros in the system root locus, never enter the right half plane:

$$\begin{aligned} C_{PIDnf}(s) &= T_{cp}\frac{s^2 + 2\xi_{cp}\omega_{0cp}s + \omega_0^2 cp}{s\left(1+s/\omega_{p1}\right)} \\ &= \frac{T_{cp}s}{1+s/\omega_{p1}} + \frac{2T_{cp}\xi_{cp}\omega_{0cp}}{1+s/\omega_{p1}} + \frac{T_{cp}\omega_0^2 cp}{s\left(1+s/\omega_{p1}\right)} \\ &= \frac{T_{cp}s}{1+s/\omega_{p1}} + \frac{T_{cp}\omega_{0pc}^2\left(1+2s\xi_{cp}/\omega_{0cp}\right)}{s\left(1+s/\omega_{p1}\right)} \end{aligned} \tag{35.52}$$

For systems with a high-frequency zero placed at least one decade above the two lightly damped complex poles, the compensator (35.53), with $\omega_{z1} \approx \omega_{z2} < \omega_p$, can be used. Usually, the two real zeros present frequencies slightly lower than the frequency of the converter complex poles. The two high-frequency poles are placed to obtain the desired phase margin [9]. The obtained overall performance will often be inferior to that of the PID type notch filter:

$$C_{PID}(s) = W_{cp} \frac{(1 + s/\omega_{z1})(1 + s/\omega_{z2})}{s(1 + s/\omega_p)^2} \tag{35.53}$$

35.2.5.2 Compensator Selection and Design

The procedure to select the compensator and to design its parameters can be outlined as follows:

1. Compensator selection: In general, since V_{DC} perturbations exist, null steady-state error guarantee is needed. High-frequency poles are usually necessary, if the transfer function shows a −6 dB/octave roll-off due to high-frequency left plane zeros. Therefore, in general, two types of compensation schemes with integral action (35.51) or (35.50) and (35.52) or (35.53) can be tried. Compensator (35.52) is usually convenient for systems with lightly damped complex poles.
2. Unity gain frequency ω_{0dB} choice:
   - If the selected compensator has no complex zeros, it is better to be conservative, choosing ω_{0dB} sufficiently below the frequency of the lightly damped poles of the converter (or the frequency of the right half-plane zeros if lower). However, because of the resonant peak of most converter transfer functions, the phase margin can be obtained at a frequency near the resonance. If the phase margin is not enough, the compensator gain must be lowered.
   - If the selected compensator has complex zeros, ω_{0dB} can be chosen slightly above the frequency of the lightly damped poles.
3. Desired phase margin (φ_M) specification $\varphi_M \geq 30°$ (preferably between 45 and 70°).
4. Compensator zero-pole placement to achieve the desired phase margin:
   - With the integral plus zero-pole compensation type (35.51), the compensator phase φ_{cp}, at the maximum frequency of unity gain (often ω_{0dB}), equals the phase margin (φ_M) minus 180° and minus the converter phase φ_{cv},($\varphi_{cp} = \varphi_M - 180° - \varphi_{cv}$). The zero-pole position can be obtained calculating the factor $f_{ct} = tg\,(\pi/2 + \varphi_{cp}/2)$ being $\omega_z = \omega_{0dB}/f_{ct}$ and $\omega_M = \omega_{0dB} f_{ct}$.
   - With the PID notch filter type (35.52) controller, the two complex zeros are placed to have a damping factor ξ_p roughly equal to two times the damping ξ_z of the converter complex poles and oscillating frequency ω_{0cp} 30% smaller than the complex poles frequency ω_p. The high-frequency pole ω_{p1} is placed to achieve the needed phase margin ($\omega_{p1} \approx (\omega_{0cp} \cdot \omega_{0dB})^{1/2} f_{ct}^2$ with $f_{ct} = \text{tg}\ (\pi/2 + \varphi_{cp}/2)$ and $\varphi_{cp} = \varphi_M - 180° - \varphi_{cv}$ [5]). Alternatively, since for stability $\xi_z\ \omega_{0cp} > \xi_p\ \omega_p$ and $\omega_p \sqrt{1 - \xi_p^2} > \omega_{0cp} \sqrt{1 - \xi_z^2}$, it is obtained $1 > \xi_z > \xi_p$ and using the geometric mean, $\omega_{0cp} = \omega_p \sqrt{\frac{\xi_p}{\xi_z} \sqrt{\frac{1 - \xi_p^2}{1 - \xi_z^2}}}$.
5. Compensator gain calculation (the product of the converter and compensator gains at the ω_{0dB} frequency must be one).
6. Stability margin verification using Bode plots and root locus.
7. Result evaluation. Restarting the compensator selection and design, if the attained results are still not good enough.

Note that several modern computer programs, such as MATLAB, provide very easy and efficient tools (such as SISOTOOL) to design these controllers, even considering that switching power converters are discrete systems. Optimum controllers such as linear-quadratic-Gaussian (LQG, LQR) controllers, whose performances might be much better than linear controllers, can also be designed using the same tools. However, in evaluating optimum controller results, care must be taken in order to guarantee that the controlled converter frequency bandwidth and gain are not beyond the validity limits of the used models.

35.2.6 Examples: Buck–Boost DC/DC Converter, Forward DC/DC Converter, 12 Pulse Rectifiers, Buck–Boost DC/DC Converter in the Discontinuous Mode (Voltage and Current Mode), Three-phase PWM Inverters

EXAMPLE 35.4 Feedback design for the buck–boost dc/dc converter

Consider the converter output voltage v_o (Fig. 35.1) to be the controlled output. From Example 35.2 and Eqs. (35.33) and (35.35), the block diagram of Fig. 35.7 is obtained. The modulator transfer function is considered a pure gain ($G_M = 0.1$). The magnitude and phase of the open-loop transfer function v_o/u_c (Fig. 35.8A trace 1) shows a resonant peak due to the two lightly damped complex poles and the associated −12 dB/octave roll-off. The right half-plane zero changes the roll-off to −6 dB/octave and adds −90° to the converter phase (nonminimum-phase converter).

Compensator selection. As V_{DC} perturbations exist, null steady-state error guarantee is needed.

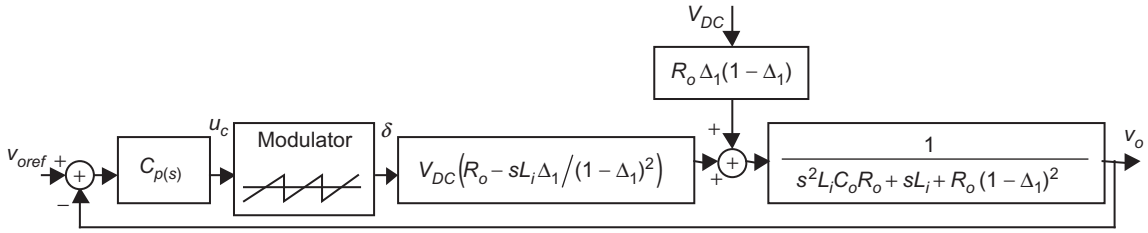


FIG. 35.7 Block diagram of the linearized model of the closed-loop buck-boost converter.

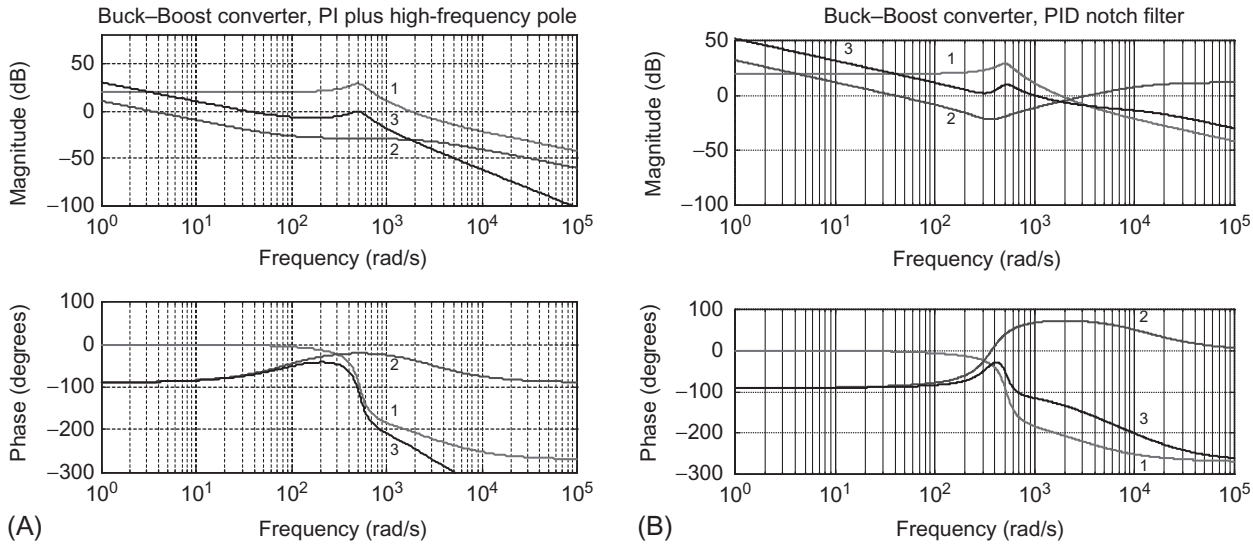


FIG. 35.8 Bode plots for the buck-boost converter. Trace 1, switching power converter magnitude and phase; trace 2, compensator magnitude and phase; and trace 3, resulting magnitude and phase of the compensated converter: (A) PI plus high-frequency pole compensation with 60° phase margin, $\omega_{0dB} = 500$ rad/s, and (B) PID notch filter compensation with 65° phase margin, $\omega_{0dB} = 1000$ rad/s.

High-frequency poles are needed given the −6 dB/octave final slope of the transfer function. Therefore, two compensation schemes (35.51) and (35.52) with integral action are tried here. The buck-boost converter controlled with integral plus zero-pole compensation presents, in closed-loop, two complex poles closer to the imaginary axes than in open loop. These poles should not dominate the converter dynamics. Instead, the real pole resulting from the open-loop pole placed at the origin should be almost the dominant one, thus slightly lowering the calculated compensator gain. If the ω_{0dB} frequency is chosen too low, the integral plus zero-pole compensation turns into a pure integral compensator ($\omega_z = \omega_M = \omega_{0dB}$). However, the obtained gains are too low, leading to very slow transient responses.

Results showing the transient responses to v_{oref} and V_{DC} step changes, using the selected compensators and converter Bode plots (Fig. 35.8), are shown (Fig. 35.9). The compensated real converter transient behavior occurs in the buck and in the boost regions. Notice the nonminimum-phase behavior of the converter (mainly in Fig. 35.9B), the superior performance of the PID notch filter compensator, and the unacceptable behavior of the PI with high-frequency pole. Care should be taken with load changes, when using this compensator, since instability can easily occur.

The compensator critical values, obtained with the root-locus studies, are $W_{cpcrit} = 700\ \text{s}^{-1}$ for the integral plus zero-pole compensator, $T_{cpcrit} = 0.0012$ s for the PID notch filter, and $W_{Icpcrit} = 18\ \text{s}^{-1}$ for the integral compensation derived from the integral plus zero-pole compensator ($\omega_z = \omega_M$). This confirms the Bode-plot design and allows stability estimation with changing loads and power supply.

Example 35.5 Feedback design for the forward dc/dc converter

Consider the output voltage v_o of the forward converter (Fig. 35.4A) to be the controlled output. From Example 35.3 and Eqs. (35.45) and (35.47), the block diagram of Fig. 35.10 is obtained. As in Example 35.4, the modulator transfer function is considered as a pure gain

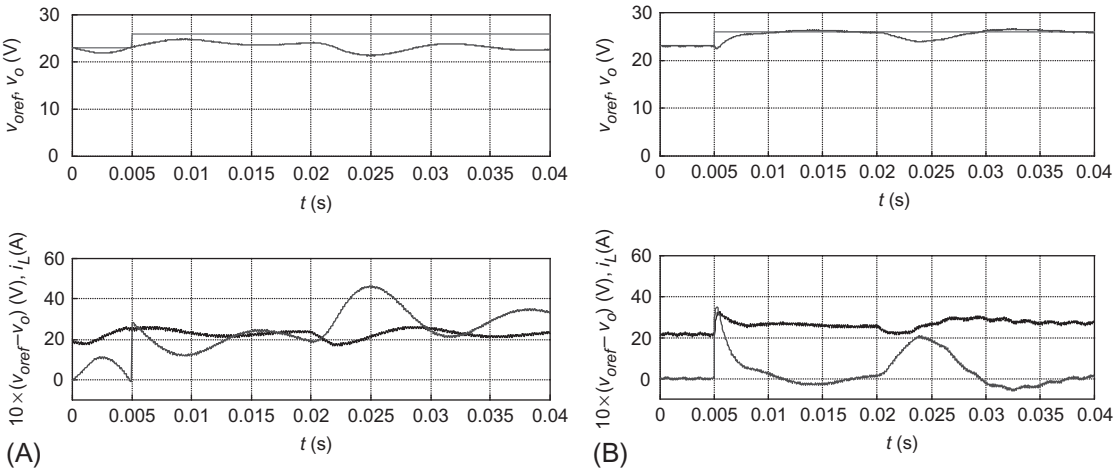


FIG. 35.9 Transient responses of the compensated buck-boost converter. At $t=0.00$ s, v_{oref} step from 23 to 26 V. At $t=0.02$ s, V_{DC} step from 26 to 23 V. Top graphs, step reference v_{oref} and output voltage v_o. Bottom graphs, trace starting at 20 is i_L current; trace starting at zero is $10\times(v_{oref}-v_o)$: (A) PI plus high-frequency pole compensation with 60° phase margin and $\omega_{0dB}=500$ rad/s and (B) PID notch filter compensation with 64° phase margin and $\omega_{0dB}=1000$ rad/s.

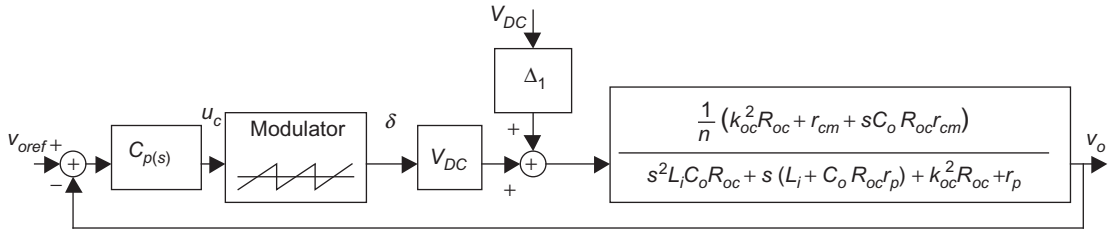


FIG. 35.10 Block diagram of the linearized model of the closed-loop controlled forward converter.

($G_M=0.1$). The magnitude and phase of the open-loop transfer function v_o/u_c (Fig. 35.11A trace 1) shows an open-loop stable system. Since integral action is needed to have some disturbance rejection of the voltage source V_{DC}, the compensation schemes used in Example 35.4, obtained using the same procedure (Fig. 35.11), were also tested.

Results, showing the transient responses to v_{oref} and V_{DC} step changes, are shown (Fig. 35.12). Both compensators (35.51) and (35.52) are easier to design than the ones for the buck-boost converter, and both have acceptable performances. Moreover, the PID notch filter presents a much faster response.

Alternatively, a PID feedback controller such as Eq. (35.53) can be easily hand-adjusted, starting with the proportional, integral, and derivative gains all set to zero. In the first step, the proportional gain is increased until the output presents an oscillatory response with nearly 50% overshoot. Next, the derivative gain is slowly increased until the overshoot is eliminated. Finally, the integral gain is increased to eliminate the steady-state error as quickly as possible.

EXAMPLE 35.6 Feedback design for phase controlled rectifiers in the continuous mode

Phase-controlled, p pulse ($p>1$), thyristor rectifiers (Fig. 35.13A), operating in the continuous mode, present an output voltage with p identical segments within the mains period T. Given this cyclic waveform, the **A**, **B**, **C**, and **D** matrices for all these p intervals can be written with the same form, in spite of the topological variation. Hence, the state-space averaged model is obtained simply by averaging all the variables within the period T/p. Assuming small variations, the mean value of the rectifier output voltage U_{DC} can be written as [4]:

$$U_{DC}=U_p\frac{p}{\pi}\sin\left(\frac{\pi}{p}\right)\cos\alpha \tag{35.54}$$

where α is the triggering angle of the thyristors and U_p the maximum peak value of the rectifier output voltage, determined by the rectifier topology and the ac supply voltage. The α value can be obtained ($\alpha=(\pi/2)\times(1-u_c/u_{cmax})$) using the modulator of Fig. 35.6B, where $\omega=2\pi/T$ is the mains frequency. From Eq. (35.54), the incremental gain K_R of the modulator plus rectifier yields

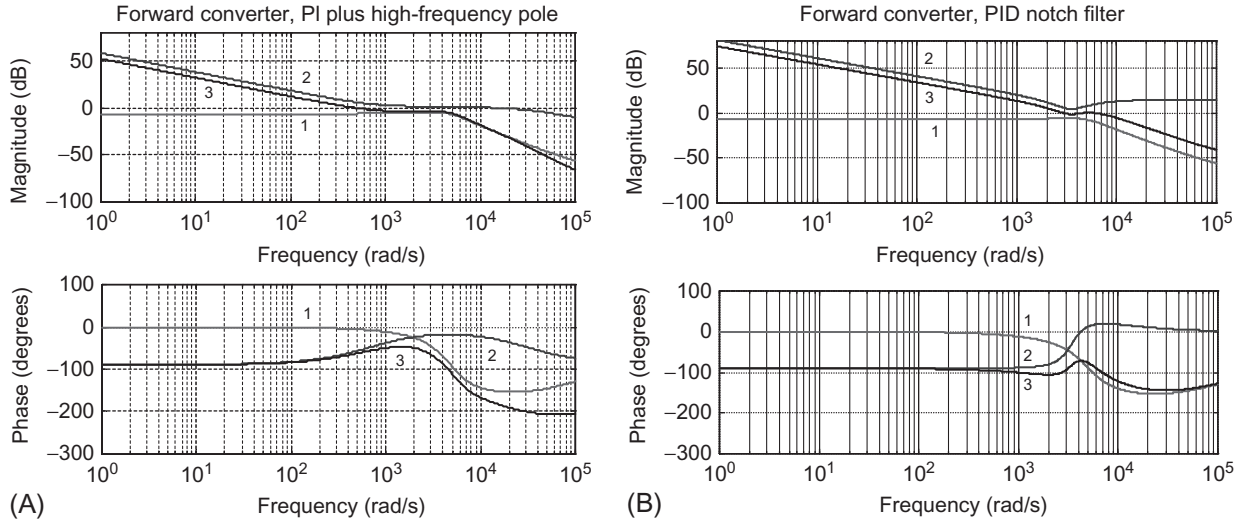


FIG. 35.11 Bode plots for the forward converter. Trace 1, switching power converter magnitude and phase; trace 2, compensator magnitude and phase; trace 3, resulting magnitude and phase of the compensated converter: (A) PI plus high-frequency pole compensation with 115° phase margin, $\omega_{0dB} = 500$ rad/s, and (B) PID notch filter compensation with 85° phase margin, $\omega_{0dB} = 6000$ rad/s.

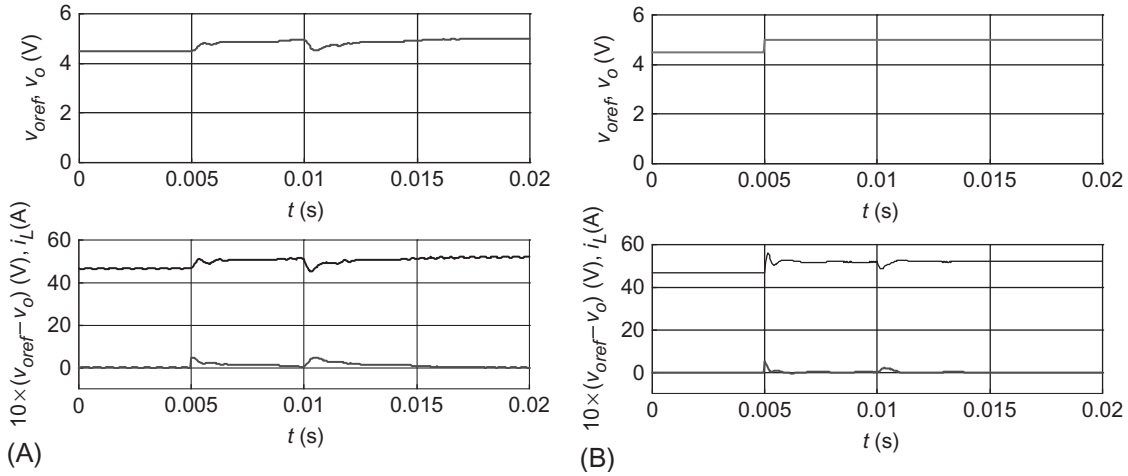


FIG. 35.12 Transient responses of the compensated forward converter. At $t = 0.005$ s, v_{oref} step from 4.5 to 5 V. At $t = 0.01$ s, V_{DC} step from 300 to 260 V. Top graphs: step reference v_{oref} and output voltage v_o. Bottom graphs: top traces i_L current and bottom traces $10 \times (v_{oref} - v_o)$; (A) PI plus high-frequency pole compensation with 115° phase margin and $\omega_{0dB} = 500$ rad/s and (B) PID notch filter compensation with 85° phase margin and $\omega_{0dB} = 6000$ rad/s.

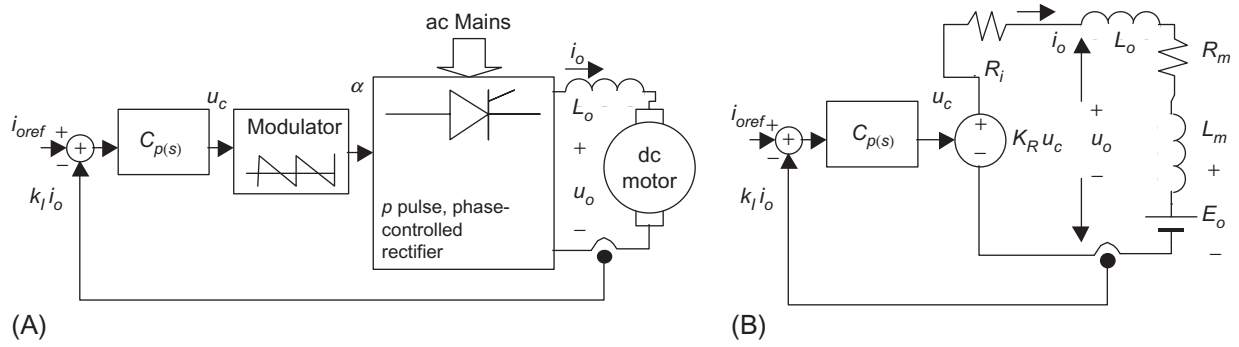


FIG. 35.13 (A) Block diagram of a p pulse phase-controlled rectifier feeding a separately excited dc motor and (B) equivalent averaged circuit.

$$K_R = \frac{\partial U_{DC}}{\partial u_c} = U_p \frac{p}{2u_{cmax}} \sin\left(\frac{\pi}{p}\right) \cos\left(\frac{\pi u_c}{2u_{cmax}}\right) \tag{35.55}$$

For a given rectifier, this gain depends on u_c and should be calculated for a certain quiescent point. However, for feedback design purposes, keeping in mind that the rectifier could be required to be stable in all operating points, the maximum value of K_R, denoted K_{RM}, can be used:

$$K_{RM} = U_p \frac{p}{2u_{cmax}} \sin\left(\frac{\pi}{p}\right) \tag{35.56}$$

The operation of the modulator, coupled to the rectifier thyristors, introduces a nonnegligible time delay, with mean value $T/2p$. Therefore, from Eq. (35.48), the modulator-rectifier transfer function $G_R(s)$ is

$$G_R(s) = \frac{U_{DC}(s)}{u_c(s)} = K_{RM} e^{-s(T/2p)} \approx \frac{K_{RM}}{1 + s(T/2p)} \tag{35.57}$$

Considering zero U_p perturbations, the rectifier equivalent averaged circuit (Fig. 35.13B) includes the loss-free rectifier output resistance R_i, due to the overlap in the commutation phenomenon caused by the mains inductance. Usually, $R_i \approx p\omega l/\pi$ where l is the equivalent inductance of the lines paralleled during the overlap, half of the line inductance for most rectifiers, except for single-phase bridge rectifiers where l is the line inductance. Here, L_o is the smoothing reactor, and R_m, L_m, and E_o are, respectively, the armature internal resistance, inductance, and back electromotive force of a separately excited dc motor (typical load). Assuming the mean value of the output current as the controlled output, making $L_t = L_o + L_m$, $R_t = R_i + R_m$, and $T_t = L_t/R_t$, and applying Laplace transforms to the differential equation obtained from the circuit of Fig. 35.13B, the output current transfer function is

$$\frac{i_o(s)}{U_{DC}(s) - E_o(s)} = \frac{1}{R_t(1 + sT_t)} \tag{35.58}$$

The rectifier and load are now represented by a perturbed (E_o) second-order system (Fig. 35.14). To achieve zero steady-state error, which ensures steady-state insensitivity to the perturbations, and to obtain closed-loop second-order dynamics, a PI controller (35.50) was selected for $C_p(s)$ (Fig. 35.14). Canceling the load pole $(-1/T_t)$ with the PI zero $(-1/T_z)$ yields

$$T_z = L_t/R_t \tag{35.59}$$

The rectifier closed-loop transfer function $i_o(s)/i_{oref}(s)$, with zero E_o perturbations, is

$$\frac{i_o(s)}{i_{oref}(s)} = \frac{2pK_{RM}k_I/(R_t T_p T)}{s^2 + (2p/T)s + 2pK_{RM}k_I/(R_t T_p T)} \tag{35.60}$$

The final value theorem enables the verification of the zero steady-state error. Comparing the denominator of Eq. (35.60) with the second-order polynomial $s^2 + 2\varsigma\omega_n s + \omega_n^2$ yields

$$\omega_n^2 = 2pK_{RM}k_I/(R_t T_p T) \qquad 4\zeta^2\omega_n^2 = (2p/T)^2 \tag{35.61}$$

Since only one degree of freedom is available (T_p), the damping factor ζ is imposed. Usually, $\zeta = \sqrt{2}/2$ is selected, since it often gives the best compromise between response speed and overshoot. Therefore, from Eq. (35.61), Eq. (35.62) arises:

$$T_p = 4\zeta^2 K_{RM}k_I T/(2pR_t) = K_{RM}k_I T/(pR_t) \tag{35.62}$$

Note that both T_z (35.59) and T_p (35.62) are dependent upon circuit parameters. They will have the correct values only for dc motors with parameters closed to the nominal load value. Using Eq. (35.62) in Eq. (35.60) yields Eq. (35.63), the second-order closed-loop transfer function of the rectifier, showing that, with loads close to the nominal value, the rectifier dynamics depend only on the mean delay time $T/2p$:

$$\frac{i_o(s)}{i_{oref}(s)} = \frac{1}{2(T/2p)^2 s^2 + sT/p + 1} \tag{35.63}$$

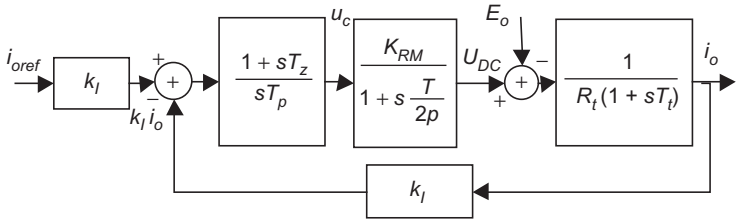


FIG. 35.14 Block diagram of a PI-controlled p pulse rectifier.

From Eq. (35.63), $\omega_n = \sqrt{2}p/T$ results, which is the maximum frequency allowed by $\omega T/2p < \sqrt{2}/2$, the validity limit of Eq. (35.48). This implies that $\zeta \geq \sqrt{2}/2$, which confirms the preceding choice. For $U_p = 300$ V, $p = 6$, $T = 20$ ms, $l = 0.8$ mH, $R_m = 0.5\ \Omega$, $L_t = 50$ mH, $E_o = -150$ V, $u_{cmax} = 10$ V, and $k_I = 0.1$, Fig. 35.15A shows the rectifier output voltage u_{oN} ($u_{oN} = u_o/U_p$) and the step response of the output current i_{oN} ($i_{oN} = i_o/40$) in accordance with Eq. (35.63). Notice that the rectifier is operating in the inverter mode. Fig. 35.15B shows the effect, in the i_o current, of a 50% reduction in the E_o value. The output current is initially disturbed, but the error vanishes rapidly with time.

These modeling and compensator design are valid for small perturbations. For large perturbations, the rectifier firing angles will either saturate at the zero value or originate large current overshoots. For large signals, antiwindup schemes (Fig. 35.16A) or error ramp limiters (or soft starters) and limiters of the PI integral component (Fig. 35.16B) must be used. These solutions will also work with other switching power converters.

To use this rectifier current controller as the inner control loop of a cascaded controller for the dc motor speed regulation, a useful first-order approximation of Eq. (35.63) is $i_o(s)/i_{oref}(s) \approx 1/(sT/p + 1)$.

Although allowing a straightforward compensator selection and precise calculation of its parameters, the rectifier modeling presented here is not suited for stability studies. The rectifier root locus will contain two complex conjugate poles in branches parallel to the imaginary axis. To study the current controller stability, at least the second-order term of Eq. (35.48) in Eq. (35.57) is needed. Alternative ways include the first-order Padé approximation of $e^{-sT/2p}$, $e^{-sT/2p} \approx (1 - sT/4p)/(1 + sT/4p)$, or the second-order approximation, $e^{-sT/2p} \approx (1 - sT/4p + (sT/2p)^2/12)/(1 + sT/4p + (sT/2p)^2/12)$. These approaches introduce zeros in the right half-plane (nonminimum-phase systems) and/or extra poles, giving more realistic results. Taking a first-order approximation and root-locus techniques, it is found that the rectifier is stable for $T_p > K_{RM}\, k_I\, T/(4pR_t)$ ($\zeta > 0.25$). Another approach uses the conditions of magnitude and angle of the delay function $e^{-sT/2p}$ to obtain the system root locus. Also, the switching power converter can be considered as a sampled data system, at frequency p/T, and Z transform can be used to determine the critical gain and first frequency of instability $p/(2\ T)$, usually half the switching frequency of the rectifier.

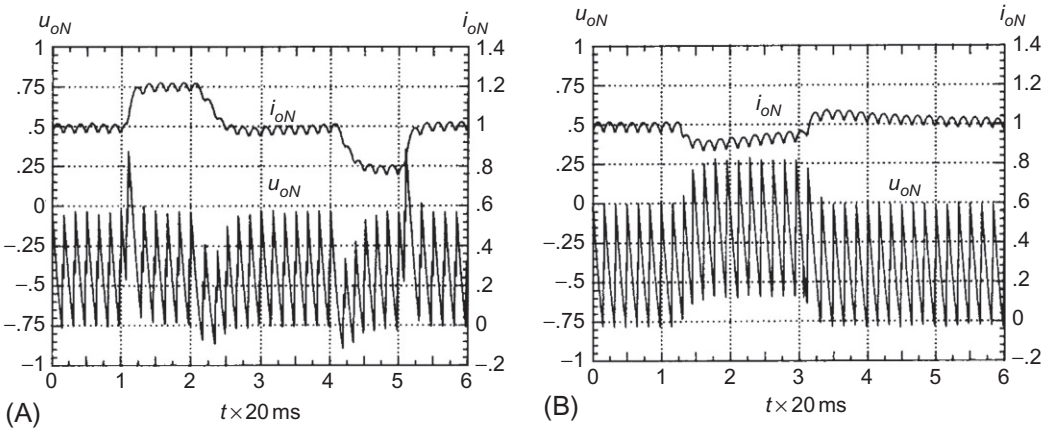


FIG. 35.15 Transient response of the compensated rectifier: (A) step response of the controlled current i_o and (B) the current i_o response to a step chance to 50% of the E_o nominal value during 1.5 T.

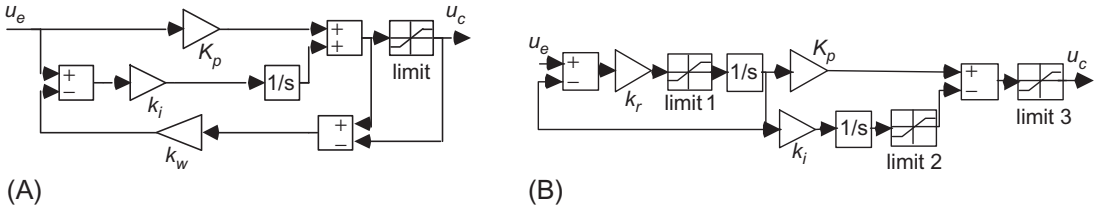


FIG. 35.16 (A) PI implementation with antiwindup (usually $1/K_p \leq k_w \leq K_i/K_p$) to deal with rectifier saturation and (B) PI with ramp limiter/soft starter ($k_r \gg K_p$) and integral component limiter to deal with large perturbations.

EXAMPLE 35.7 Buck–Boost dc/dc converter feedback design in the discontinuous mode

The methodologies just described do not apply to switching power converters operating in the discontinuous mode. However, the derived equivalent averaged circuit approach can be used, calculating the mean value of the discontinuous current supplied to the load, to obtain the equivalent circuit. Consider the buck-boost converter of Example 35.1 (Fig. 35.1) with the new values $L_i = 40\ \mu H$, $C_o = 1000\ \mu F$, and $R_o = 15\ \Omega$. The mean value of the current i_{Lo}, supplied to the output capacitor and resistor of the circuit operating in the discontinuous mode, can be calculated noting that, if the input V_{DC} and output v_o voltages are essentially constant (low ripple), the inductor current rises linearly from zero, peaking at $I_P = (V_{DC}/L_i)\delta_1\, T$ (Fig. 35.17A). As the mean value of i_{Lo}, supposed linear, is $I_{Lo} = (I_P\delta_2 T)/(2\ T)$, using the steady-state input-output relation $V_{DC}\delta_1 = V_o\delta_2$ and the above I_P value, I_{Lo} can be written as

$$I_{Lo} = \frac{\delta_1^2 V_{DC}^2 T}{2 L_i V_o} \tag{35.64}$$

This is a nonlinear relation that could be linearized around an operating point. However, switching power converters in the discontinuous mode seldom operate just around an operating point. Therefore, using a quadratic modulator (Fig. 35.18), obtained integrating the ramp $r(t)$ (Fig. 35.6A) and comparing the quadratic curve to the term $u_{cPI}v_o/V_{DC}^2$ (which is easily implemented using the Unitrode UC3854 integrated circuit), the duty cycle δ_1 is $\delta_1 = \sqrt{u_{cPI}V_o/\left(u_{cmax}V_{DC}^2\right)}$, and a constant incremental factor K_{CV} can be obtained:

$$K_{CV} = \frac{\partial I_{Lo}}{\partial u_{cPI}} = \frac{T}{2 u_{cmax} L_i} \tag{35.65}$$

Considering zero-voltage perturbations and neglecting the modulator delay, the equivalent averaged circuit (Fig. 35.17B) can be used to derive the output voltage to input current transfer function $v_o(s)/i_{Lo}(s) = R_o/(sC_oR_o + 1)$. Using a PI controller (35.50), the closed-loop transfer function is

$$\frac{v_o(s)}{v_{oref}(s)} = \frac{K_{CV}(1 + sT_z)/(C_oT_p)}{s^2 + s\left(T_p + T_zK_{CV}k_vR_o\right)/(C_oR_oT_p) + K_{CV}k_V/(C_oT_p)} \tag{35.66}$$

Since two degrees of freedom exist, the PI constants are derived imposing ζ and ω_n for the second-order denominator of Eq. (35.66), usually $\zeta \geq \sqrt{2}/2$ and $\omega_n \leq 2\pi f_s/10$. Therefore,

$$\begin{aligned} T_p &= K_{CV}k_v/\left(\omega_n^2 C_o\right) \\ T_z &= T_p(2\zeta\omega_n C_oR_o - 1)/(K_{CV}k_vR_o) \end{aligned} \tag{35.67}$$

The transient behavior of this converter, with $\zeta = 1$ and $\omega_n \approx \pi f_s/10$, is shown in Fig. 35.19A. Compared with

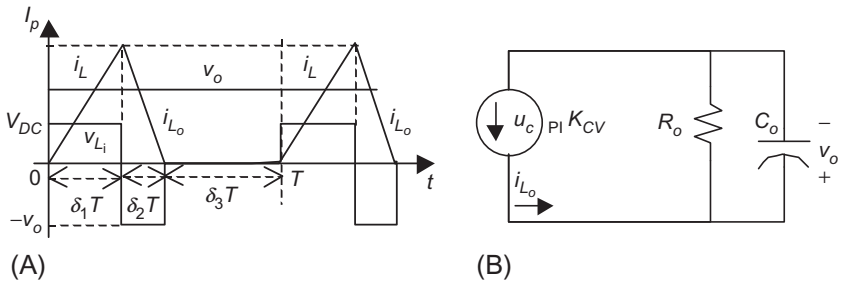


FIG. 35.17 (A) Waveforms of the buck-boost converter in the discontinuous mode and (B) equivalent averaged circuit.

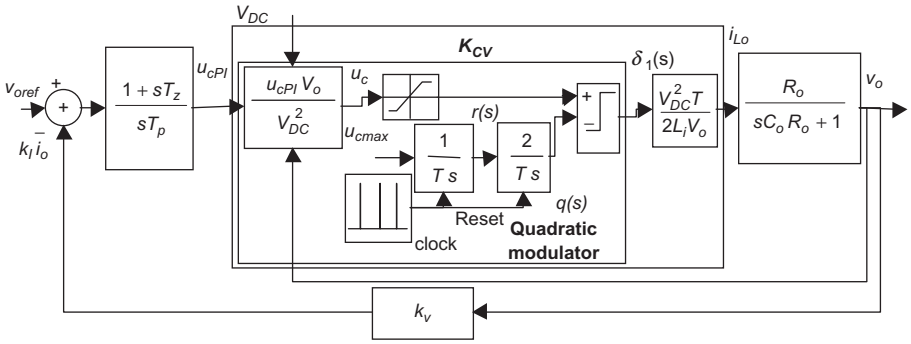


FIG. 35.18 Block diagram of a PI-controlled (feedforward linearized) buck-boost converter operating in the discontinuous mode.

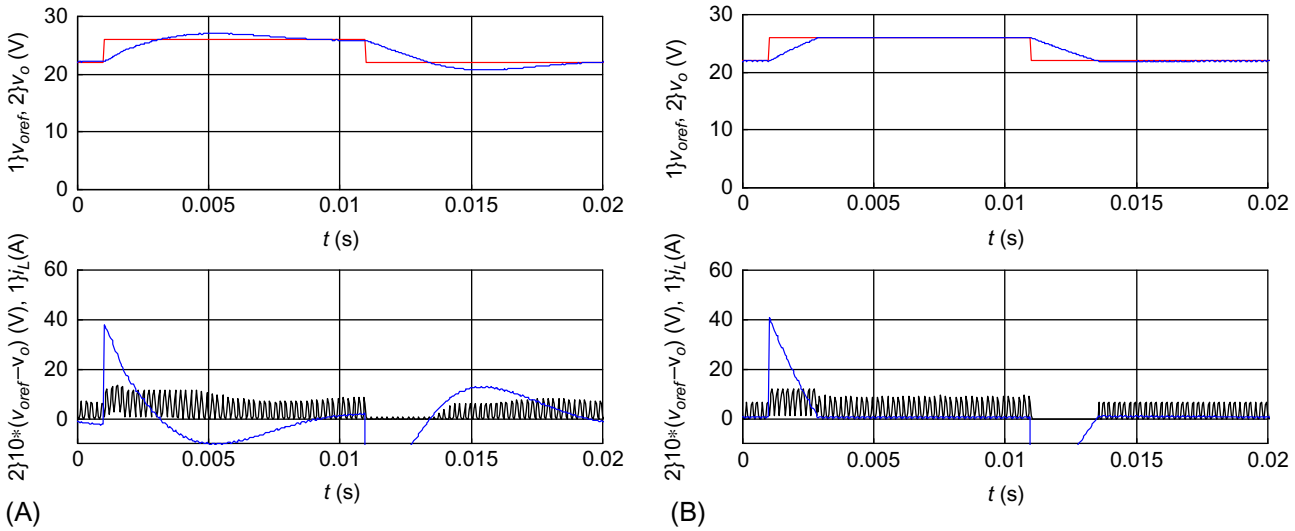


FIG. 35.19 Transient response of the compensated buck-boost converter in the discontinuous mode. At $t=0.001$ s, v_{oref} step from 23 to 26 V. At $t=0.011$ s, v_{oref} step from 26 to 23 V. Top graphs: step reference v_{oref} and output voltage v_o. Bottom graphs: pulses and i_L current; trace peaking at 40, $10\times(v_{oref}-v_o)$: (A) PI-controlled and feedforward linearized buck-boost converter with $\zeta=1$ and $\omega_n\approx\pi f_s/10$ and (B) current-mode-controlled buck-boost with $\zeta=1$ and maximum value $I_{pmax}=15$ A.

Example 35.2, the operation in the discontinuous conduction mode reduces, by 1, the order of the state-space averaged model and eliminates the zero in the right half of the complex plane. The inductor current does not behave as a true state variable, since during the interval $\delta_3 T$ this current is zero, and this value is always the i_{Lo} current initial condition. Given the differences between these two examples, care should be taken to avoid the operation in the continuous mode of converters designed and compensated for the discontinuous mode. This can happen during turn-on or step load changes, and if not prevented, the feedback design should guarantee stability in both modes (Example 35.8 and Fig. 35.20).

EXAMPLE 35.8 Feedback design for the buck–boost dc/dc converter operating in the discontinuous mode and using current-mode control

The performances of the buck-boost converter operating in the discontinuous mode can be greatly enhanced if a *current-mode control* scheme is used, instead of the voltage-mode controller designed in Example 35.7. Current-mode control in switching power converters is the simplest form of state feedback. Current mode needs the measurement of the current i_L (Fig. 35.1) but greatly simplifies the modulator design (compare Fig. 35.18 with Fig. 35.20), since no modulator linearization is used. The measured value, proportional to the current i_L, is

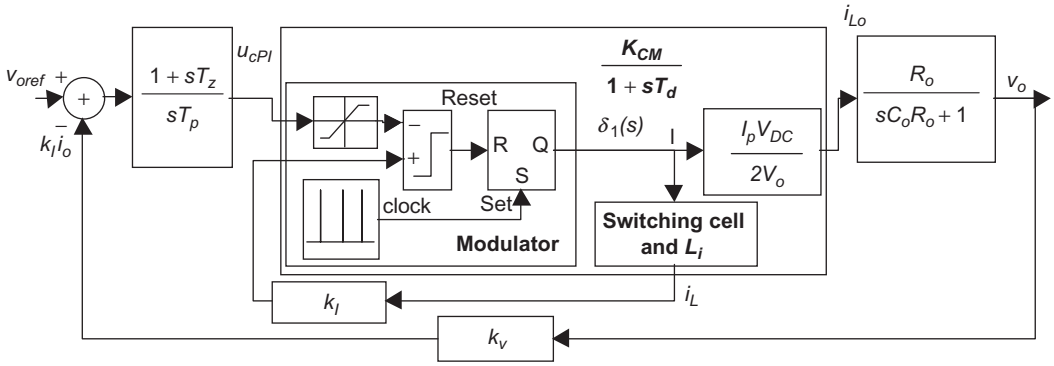


FIG. 35.20 Block diagram of a current-mode controlled buck-boost converter operating in the discontinuous mode.

compared with the value u_{cPI} given by the output voltage controller (Fig. 35.20). The modulator switches off the power semiconductor when $k_I I_P = u_{cPI}$.

Expressed as a function of the peak i_L current I_P, I_{Lo} becomes (Example 35.7) $I_{Lo} = I_P \delta_1 V_{DC}/(2V_o)$, or considering the modulator task $I_{Lo} = u_{cPI}\delta_1 V_{DC}/(2k_I V_o)$. For small perturbations, the incremental gain is $K_{CM} = \partial I_{Lo}/\partial u_{cPI} = \delta_1 V_{DC}/(2k_I V_o)$. An I_{Lo} current delay $T_d = 1/(2f_s)$, related to the switching frequency f_s, can be assumed. The current-mode control transfer function $G_{CM}(s)$ is

$$G_{CM}(s) = \frac{I_{Lo}(s)}{u_{cPI}(s)} \approx \frac{K_{CM}}{1 + sT_d} \approx \frac{\delta_1 V_{DC}}{2k_I V_o(1 + sT_d)} \tag{35.68}$$

Using the approach of Example 35.6, the values for T_z and T_p are given by Eq. (35.69).

$$\begin{aligned} T_z &= R_o C_o \\ T_p &= 4\zeta^2 K_{CM} k_v R_o T_d \end{aligned} \tag{35.69}$$

The transient behavior of this converter, with $\zeta = 1$ and maximum value for I_p, $I_{pmax} = 15$ A, is shown in Fig. 35.19B. The output voltage step response presents no overshoot, no steady-state error, and better dynamics, compared with the response (Fig. 35.19A) obtained using the quadratic modulator (Fig. 35.18). Notice that, with current-mode control, the converter behaves like a reduced-order system and the right half-plane zero is not present.

The current-mode control scheme can be advantageously applied to converters operating in the continuous mode, guarantying short-circuit protection, system order reduction, and better performances. However, for converters operating in the step-up (boost) regime, a stabilizing ramp with negative slope is required, to ensure stability. The stabilizing ramp will transform the signal u_{cPI} in a new signal $u_{cPI} - \text{rem}(k_{sr}t/T)$ where k_{sr} is the needed amplitude for the compensation ramp and the function rem is the remainder of the division of $k_{sr}t$ by T. In the next section, current control of switching power converters will be detailed.

Closed-loop control of resonant converters can be achieved using the outlined approaches, if the resonant phases of operation last for small intervals compared with the fundamental period. Otherwise, the equivalent averaged circuit concept can often be used and linearized, now considering the resonant converter input-output relations, normally functions of the driving frequency and input or output voltages, to replace the δ_1 variable.

EXAMPLE 35.9 Output voltage control in three-phase voltage-source inverters using sinusoidal wave PWM (SPWM) and space-vector modulation (SVM)

Sinusoidal wave PWM

Voltage-source three-phase inverters (Fig. 35.21) are often used to drive squirrel cage induction motors (IM) in variable speed applications.

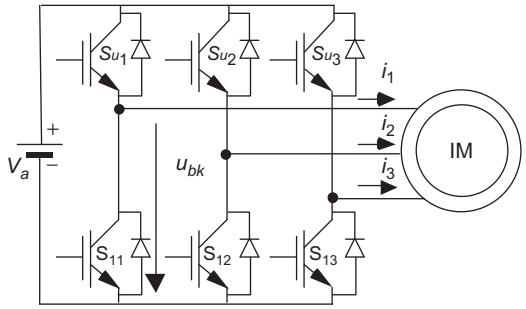


FIG. 35.21 IGBT-based voltage-sourced three-phase inverter with induction motor.

Considering almost ideal power semiconductors, the output voltage $u_{bk}(k \in \{1, 2, 3\})$ dynamics of the inverter is negligible as the output voltage can hardly be considered a state variable in the time scale describing the motor behavior. Therefore, the best known method to create sinusoidal output voltages uses an open-loop modulator with low-frequency sinusoidal waveforms $\sin(\omega t)$, with the amplitude defined by the modulation index m_i ($m_i \in [0, 1]$), modulating high-frequency triangular waveforms $r(t)$ (carriers) (Fig. 35.22), a process similar to the one described in Section 35.2.4. The frequency and phase of the triangular carriers should guarantee half-wave and quarter-wave symmetry for minimum harmonic distortion.

This sinusoidal wave PWM (SPWM) modulator generates the variable γ_k, represented in Fig. 35.22 by the rectangular waveform, which describes the inverter k leg state:

$$\gamma_k = \begin{cases} 1 \rightarrow \text{when } m_i \sin(\omega t) > r(t) \\ 0 \rightarrow \text{when } m_i \sin(\omega t) < r(t) \end{cases} \tag{35.70}$$

The turn-on and turn-off signals for the k leg inverter switches are related with the variable γ_k as follows:

$$\gamma_k = \begin{cases} 1 \rightarrow \text{when } Su_k \text{ is on and } Sl_k \text{ is off} \\ 0 \rightarrow \text{when } Su_k \text{ is off and } Sl_k \text{ is on} \end{cases} \tag{35.71}$$

This applies constant-frequency sinusoidally weighted PWM signals to the gates of each insulated-gate bipolar transistor (IGBT). The PWM signals for all the upper IGBTs (Su_k, $k \in \{1, 2, 3\}$) must be 120° out of phase, and the PWM signal for the lower IGBT Sl_k must be the complement of the Su_k signal. Since transistor turn-on times are usually shorter than turn-off times, some dead time must be included between the Su_k and Sl_k pulses to prevent internal short circuits.

Sinusoidal PWM can be easily implemented using a microprocessor or two digital counters/timers generating the addresses for two lookup tables (one for the triangular function and another for supplying the per unit basis of the sine, whose frequency can vary). Tables can be

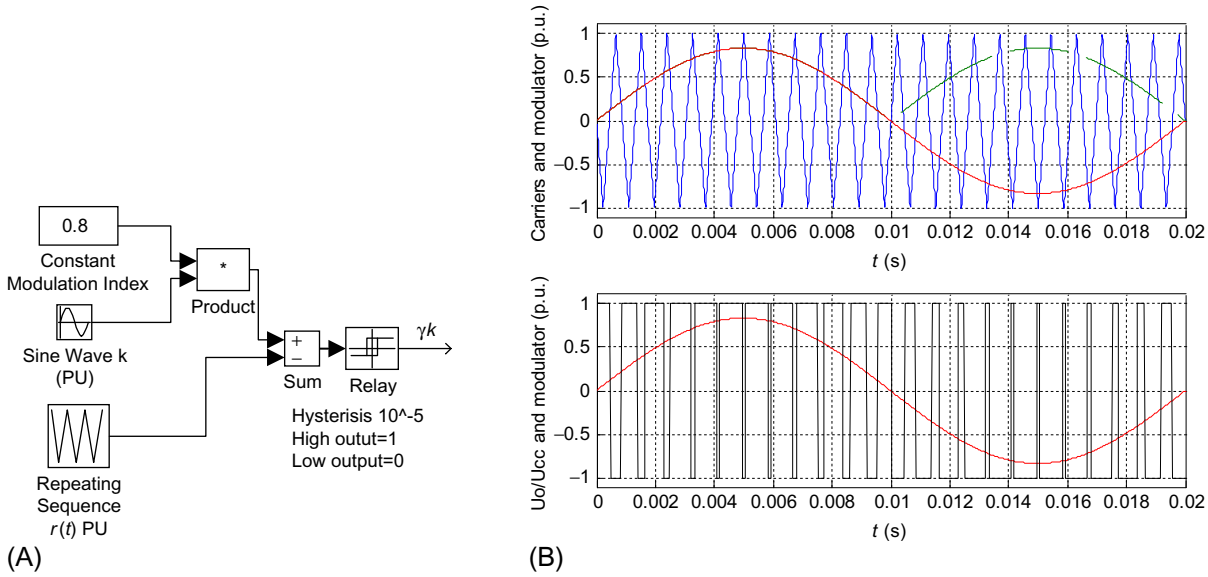


FIG. 35.22 (A) SPWM modulator schematic and (B) main SPWM signals.

stored in read-only memories, ROM, or erasable programmable ROM, EPROM. One multiplier for the modulation index (perhaps into the digital-to-analog (D/A) converter for the sine ROM output) and one hysteresis comparator must also be included.

With SPWM, the first harmonic maximum amplitude of the obtained line-to-line voltage is only about 86% of the inverter dc supply voltage V_a. Since it is expectable that this amplitude should be closer to V_a, different modulating voltages (e.g., adding a third-order harmonic with one-fourth of the fundamental sine amplitude) can be used as long as the fundamental harmonic of the line-to-line voltage is kept sinusoidal. Another way is to leave SPWM and consider the eight possible inverter output voltages trying to directly use then. This will lead to space-vector modulation.

Space vector modulation

Space vector modulation (SVM) is based on the polar representation (Fig. 35.23) of the eight possible base output voltages of the three-phase inverter (Table 35.1, where v_α and v_β are the vector components of vector $\vec{V}_g$, $g \in \{0, 1, 2, 3, 4, 5, 6, 7\}$, obtained with Eq. (35.72)). Therefore, as all the available voltages can be used, SVM does not present the voltage limitation of SPWM.

Furthermore, being a vector technique, SVM fits nicely with the vector control methods often used in IM drives:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \gamma_1 \\ \gamma_2 \\ \gamma_3 \end{bmatrix} V_a \qquad (35.72)$$

Consider that the vector $\vec{V}_s$ (magnitude V_s and angle [Fcy]) must be applied to the IM. Since there is no such

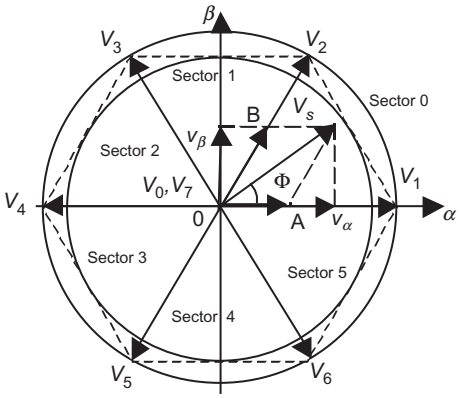


FIG. 35.23 α and β space-vector representation of the three-phase bridge inverter leg base vectors.

TABLE 35.1 The three-phase inverter with eight possible γk combinations, vector numbers, and respective α and β components

γ_1	γ_2	γ_3	u_{bk}	$u_{bk} - u_{bk+1}$	v_α	v_β	Vector
0	0	0	0	0	0	0	$\vec{V}_0$
1	0	0	$\gamma_k V_a$	$(\gamma_k - \gamma_{k+1})V_a$	$\sqrt{2/3}V_a$	0	$\vec{V}_1$
1	1	0	$\gamma_k V_a$	$(\gamma_k - \gamma_{k+1})V_a$	$V_a/\sqrt{6}$	$V_a/\sqrt{2}$	$\vec{V}_2$
0	1	0	$\gamma_k V_a$	$(\gamma_k - \gamma_{k+1})V_a$	$-V_a/\sqrt{6}$	$V_a/\sqrt{2}$	$\vec{V}_3$
0	1	1	$\gamma_k V_a$	$(\gamma_k - \gamma_{k+1})V_a$	$-\sqrt{2/3}V_a$		$\vec{V}_4$
1	1	1	V_a	0	0	0	$\vec{V}_7$
1	0	1	$\gamma_k V_a$	$(\gamma_k - \gamma_{k+1})V_a$	$V_a/\sqrt{6}$	$-V_a/\sqrt{2}$	$\vec{V}_6$
0	0	1	$\gamma_k V_a$	$(\gamma_k - \gamma_{k+1})V_a$	$-V_a/\sqrt{6}$	$-V_a/\sqrt{2}$	$\vec{V}_5$

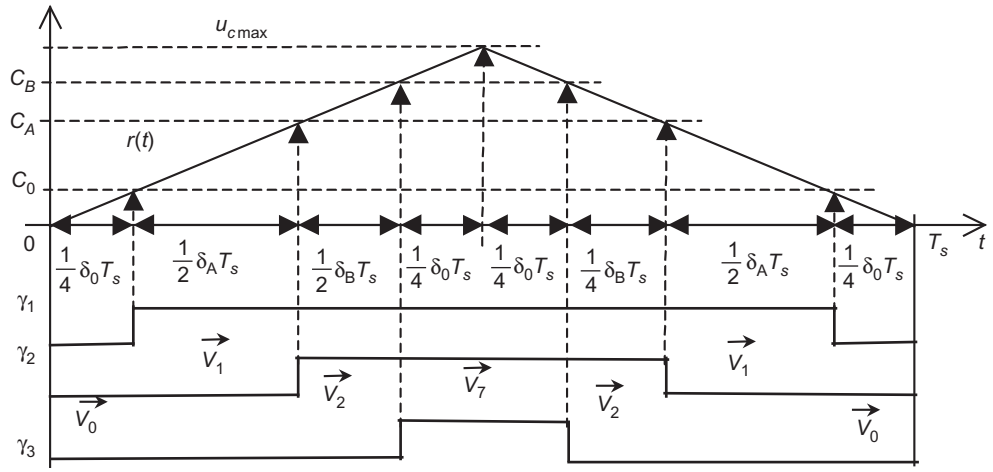


FIG. 35.24 Symmetrical SVM.

vector available directly, SVM uses an averaging technique to apply the two vectors, $\vec{V}_1$ and $\vec{V}_2$, closest to $\vec{V}_s$. The vector $\vec{V}_1$ will be applied during $\delta_A T_s$, while vector $\vec{V}_2$ will last $\delta_B T_s$ (where $1/T_s$ is the inverter switching frequency and δ_A and δ_B are duty cycles, δ_A and $\delta_B \in [0, 1]$). If there is any leftover time in the PWM period T_s, then the zero vector is applied during time $\delta_0 T_s = T_s - \delta_A T_s - \delta_B T_s$. Since there are two zero vectors ($\vec{V}_0$ and $\vec{V}_7$), a symmetrical PWM can be devised, which uses both $\vec{V}_0$ and $\vec{V}_7$, as shown in Fig. 35.24. Such a PWM arrangement minimizes the power semiconductor switching frequency and IM torque ripples

The input to the SVM algorithm is the space vector $\vec{V}_s$, into the sector s_n, with magnitude V_s and angle Φ_s. This vector can be rotated to fit into sector 0 (Fig. 35.23) reducing Φ_s to the first sector, $\Phi = \Phi_s - s_n\pi/3$. For any $\vec{V}_s$ that is not exactly along one of the six nonnull inverter base vectors (Fig. 35.23), SVM must generate an approximation by applying the two adjacent vectors during an appropriate amount of time. The algorithm can be devised considering that the projections of $\vec{V}_s$, onto the two closest base vectors, are values proportional to δ_A and δ_B duty cycles. Using simple trigonometric relations in sector 0 ($0 < \Phi < \pi/3$) (Fig. 35.23) and considering K_T the proportional ratio, δ_A and δ_B are, respectively, $\delta_A = K_T \overline{\mathrm{OA}}$ and $\delta_B = K_T \overline{\mathrm{OA}}$, yielding

$$\begin{aligned} \delta_A &= K_T \frac{2V_s}{\sqrt{3}} \sin\left(\frac{\pi}{3} - \Phi\right) \\ \delta_B &= K_T \frac{2V_s}{\sqrt{3}} \sin\Phi \end{aligned} \tag{35.73}$$

The K_T value can be found if we notice that when $\vec{V}_s = \vec{V}_1$, $\delta_A = 1$, and $\delta_B = 0$ (or when $\vec{V}_s = \vec{V}_2$, $\delta_A = 0$, and $\delta_B = 1$). Therefore, since when $\vec{V}_s = \vec{V}_1$, $V_s = \sqrt{v_\alpha^2 + v_\beta^2} = \sqrt{2/3}V_a$, $\Phi = 0$, or when $\vec{V}_s = \vec{V}_2$, $V_s = \sqrt{2/3}V_a$, $\Phi = \pi/3$, the K_T constant is $K_T = \sqrt{3}/\left(\sqrt{2}V_a\right)$. Hence,

$$\begin{aligned} \delta_A &= \frac{\sqrt{2}V_s}{V_a} \sin\left(\frac{\pi}{3} - \Phi\right) \\ \delta_B &= \frac{\sqrt{2}V_s}{V_a} \sin\Phi \\ \delta_0 &= 1 - \delta_A - \delta_B \end{aligned} \tag{35.74}$$

The obtained resulting vector $\vec{V}_s$ cannot extend beyond the hexagon of Fig. 35.23. This can be understood if the maximum magnitude V_{sm} of a vector with $\Phi = \pi/6$ is calculated. For $\Phi = \pi/6$, the maximum duty cycles are $\delta_A = 1/2$ and $\delta_B = 1/2$. Then, from Eq. (35.74,) $V_{sm} = V_a/\sqrt{2}$ is obtained. This magnitude is lower than that of the vector $\vec{V}_1$ since the ratio between these magnitudes is $\sqrt{3/2}$. To generate sinusoidal voltages, the vector $\vec{V}_s$ must be inside the inner circle of Fig. 35.23, so that it can be rotated without crossing the hexagon boundary. Vectors with tips between this circle and the hexagon are reachable but produce nonsinusoidal line-to-line voltages.

For sector 0 (Fig. 35.23), SVM symmetrical PWM switching variables (γ_1, γ_2, and γ_3) and intervals (Fig. 35.24) can be obtained by comparing a triangular wave with amplitude u_{cmax} (Fig. 35.24, where $r(t) = 2u_{cmax}t/T_s$ and $t \in [0, T_s/2]$), with the following values:

$$\begin{aligned} C_0 &= \frac{u_{c\max}}{2}\delta_0 = \frac{u_{c\max}}{2}(1 - \delta_A - \delta_B) \\ C_A &= \frac{u_{c\max}}{2}\left(\frac{\delta_0}{2} + \delta_A\right) = \frac{u_{c\max}}{2}(1 + \delta_A - \delta_B) \\ C_B &= \frac{u_{c\max}}{2}\left(\frac{\delta_0}{2} + \delta_A + \delta_B\right) = \frac{u_{c\max}}{2}(1 + \delta_A + \delta_B) \end{aligned} \tag{35.75}$$

Extension of Eq. (35.75) to all six sectors can be done if the sector number s_n is considered, together with the auxiliary matrix $\boldsymbol{\Xi}$:

$$\Xi^T = \begin{bmatrix} -1 & -1 & 1 & 1 & 1 & -1 \\ -1 & 1 & 1 & 1 & -1 & -1 \end{bmatrix} \tag{35.76}$$

Generalization of the values C_0, C_A, and C_B, denoted C_{0sn}, C_{Asn}, and C_{Bsn}, is written in Eq. (35.77), knowing that, for example, $\Xi_{\left((sn+4)_{\text{mod }6}+1\right)}$ is the $\boldsymbol{\Xi}$ matrix row with number $(s_n+4)_{\text{mod }6}+1$:

$$\begin{aligned} C_{0sn} &= \frac{u_{c\max}}{2}\left(1+\Xi_{\left((Sn)_{\text{mod}6}+1\right)}\begin{bmatrix}\delta_A\\ \delta_B\end{bmatrix}\right) \\ C_{Asn} &= \frac{u_{c\max}}{2}\left(1+\Xi_{\left((Sn+4)_{\text{mod}6}+1\right)}\begin{bmatrix}\delta_A\\ \delta_B\end{bmatrix}\right) \\ C_{Bsn} &= \frac{u_{c\max}}{2}\left(1+\Xi_{\left((Sn+2)_{\text{mod}6}+1\right)}\begin{bmatrix}\delta_A\\ \delta_B\end{bmatrix}\right) \end{aligned} \tag{35.77}$$

Therefore, γ_1, γ_2, and γ_3 are

$$\begin{aligned} \gamma_1 &= \begin{cases} 0 \rightarrow \text{when } r(t) < C_{0sn} \\ 1 \rightarrow \text{when } r(t) > C_{0sn} \end{cases} \\ \gamma_2 &= \begin{cases} 0 \rightarrow \text{when } r(t) < C_{Asn} \\ 1 \rightarrow \text{when } r(t) > C_{Asn} \end{cases} \\ \gamma_3 &= \begin{cases} 0 \rightarrow \text{when } r(t) < C_{Bsn} \\ 1 \rightarrow \text{when } r(t) > C_{Bsn} \end{cases} \end{aligned} \tag{35.78}$$

Supposing that the space vector $\vec{V}_s$ is now specified in the orthogonal coordinates $\alpha,\beta\left(\vec{V}_\alpha, \vec{V}_\beta\right)$, instead of magnitude V_s and angle Φ_s, the duty cycles δ_A and δ_B can be easily calculated knowing that $v_\alpha = V_s \cos \Phi$ and $v_\beta = V_s \sin \Phi$ and using Eq. (35.74):

$$\begin{aligned} \delta_A &= \frac{\sqrt{2}}{2V_a}\left(\sqrt{3}v_\alpha - v_\beta\right) \\ \delta_B &= \frac{\sqrt{2}}{V_a}v_\beta \end{aligned} \tag{35.79}$$

This equation enables the use of Eqs. (35.77) and (35.78) to obtain SVM in orthogonal coordinates.

Using SVM or SPWM, the closed-loop control of the inverter output currents (induction motor stator currents) can be performed using an approach similar to that outlined in Example 35.6 and decoupling the currents expressed in a d and q rotating frame.

35.3 Sliding-Mode Control of Switching Power Converters

35.3.1 Introduction

All the designed controllers for switching power converters are in fact variable structure controllers, in the sense that the control action changes rapidly from one to another of, usually, two possible $\delta(t)$ values, cyclically changing the converter topology. This is accomplished by the modulator (Fig. 35.6), which creates the switching variable $\delta(t)$ imposing $\delta(t)=1$ or $\delta(t)=0$, to turn on or off the power semiconductors. As a consequence of this discontinuous control action, indispensable for efficiency reasons, state trajectories move back and forth around a certain average surface in the state-space, and variables present some ripple. To avoid the effects of this ripple in the modeling and to apply linear control methodologies to time-variant systems, average values of state variables and state-space averaged models or circuits were presented (Section 35.2). However, a nonlinear approach to the modeling and control problem, taking advantage of the inherent ripple and variable structure behavior of switching power converters, instead of just trying to live with them, would be desirable, especially if enhanced performances could be attained.

In this approach, switching power converter topologies, as discrete nonlinear time-variant systems, are controlled to switch from one dynamics to another when just needed. If this switching occurs at a very high frequency (theoretically infinite), the state dynamics described as in Eq. (35.4) can be enforced to slide along a certain prescribed state-space trajectory. The converter is said to be in sliding mode, the allowed deviations from the trajectory (the ripple) imposing the practical switching frequency.

Sliding-mode control of variable structure systems, such as switching power converters, is particularly interesting because of the inherent robustness [10,11], capability of system order reduction, and appropriateness to the on/off switching of power semiconductors. The control action, being the control equivalent of the management paradigm "just in time" (JIT), provides timely and precise control actions, determined by the control law and the allowed ripple. Therefore, the switching frequency is not constant over all operating regions of the converter.

This section treats the derivation of the control (sliding surface) and switching laws, robustness, stability, constant-frequency operation, and steady-state error elimination necessary for sliding-mode control of switching power converters, also giving some examples.

35.3.2 Principles of Sliding-mode Control

Consider the state-space switched model Eq. (35.4) of a switching converter subsystem and input-output linearization or another technique, to obtain, from state-space equations, one

Eq. (35.80), for each controllable subsystem output $\mathbf{y}=\mathbf{x}$. In the controllability canonical form [12] (also known as input-output decoupled or companion form), Eq. (35.80) is

$$\frac{\mathrm{d}}{\mathrm{d}t}\left[x_h,\ldots x_{j-1},x_j\right]^T=\left[x_{h+1},\ldots,x_j,-f_h(\mathbf{x})-p_h(t)+b_h(\mathbf{x})u_h(t)\right]^{\mathrm{T}} \tag{35.80}$$

where $\mathbf{x}=[x_h,\ldots,x_{j-1},x_j]^{\mathrm{T}}$ is the subsystem state vector, $f_h(\mathbf{x})$ and $b_h(\mathbf{x})$ are functions of $\mathbf{x}$, $p_h(t)$ represents the external disturbances, and $u_h(t)$ is the control input. In this special form of state-space modeling, the state variables are chosen so that the x_{i+1} variable ($i\in\{h,\ldots,j-1\}$) is the time derivative of x_i, that is, $\mathbf{x}=\left[x_h,\dot{x}_h,x_h,\ldots,\overset{m}{x}_h\right]^{\mathrm{T}}$, where $m=j-h$ [13].

35.3.2.1 Control Law (Sliding Surface)

The required closed-loop dynamics for the subsystem output vector $\mathbf{y}=\mathbf{x}$ can be chosen to verify Eq. (35.81) with selected k_i values. This is a model reference adaptive control approach to impose a state trajectory that advantageously reduces the system order ($j-h+1$):

$$\frac{\mathrm{d}x_j}{\mathrm{d}t}=-\sum_{i=h}^{j-1}\frac{k_i}{k_j}x_{i+1} \tag{35.81}$$

Effectively, in a single-input single-output (SISO) subsystem, the order is reduced by unity, applying the restriction Eq. (35.81). In a multiple-input multiple-output (MIMO) system, in which ν-independent restrictions could be imposed (usually with ν degrees of freedom), the order could often be reduced in ν units. Indeed, from Eq. (35.81), the dynamics of the jth term of $\mathbf{x}$ is linearly dependent from the $j-h$ first terms:

$$\frac{\mathrm{d}x_j}{\mathrm{d}t}=-\sum_{i=h}^{j-1}\frac{k_i}{k_j}x_{i+1}=-\sum_{i=h}^{j-1}\frac{k_i}{k_j}\frac{\mathrm{d}x_i}{\mathrm{d}t} \tag{35.82}$$

The controllability canonical model allows the direct calculation of the needed control input to achieve the desired dynamics Eq. (35.81). In fact, as the control action should enforce the state vector $\mathbf{x}$, to follow the reference vector $\mathbf{x}_r=\left[x_{h_r},\dot{x}_{h_r},\ddot{x}_{h_r},\ldots,x_{h_r}^m\right]^T$, the tracking error vector will be $\mathbf{e}=\left[x_{h_r}-x_h,\ldots,x_{j-1r}-x_{j-1},x_{jr}-x_j\right]^T$ or $\mathbf{e}=\left[e_{x_h},\ldots,e_{xj-1},e_{x_j}\right]^T$. Thus, equating the subexpressions for $\mathrm{d}x_j/\mathrm{d}t$ of Eqs. (35.80) and (35.81), the necessary control input $u_h(t)$ is

$$u_h(t)=\frac{p_h(t)+f_h(x)+\dfrac{\mathrm{d}x_j}{\mathrm{d}t}}{b_h(x)}=\frac{p_h(t)+f_h(x)-\displaystyle\sum_{i=h}^{j-1}\frac{k_i}{k_j}x_{i+1_r}+\sum_{i=h}^{j-1}\frac{k_i}{k_j}e_{x_{i+1}}}{b_h(x)} \tag{35.83}$$

This expression is the required closed-loop control law, but unfortunately, it depends on the system parameters and on external perturbations and is difficult to compute. Moreover, for some output requirements, Eq. (35.83) would give extremely high values for the control input $u_h(t)$, which would be impractical or almost impossible.

In most switching power converters, $u_h(t)$ is discontinuous. Yet, if we assume one or more discontinuity borders dividing the state-space into subspaces, the existence and uniqueness of the solution are guaranteed out of the discontinuity borders, since in each subspace the input is continuous. The discontinuity borders are subspace switching hypersurfaces, whose order is the space order minus one, along which the subsystem state slides, since its intersections with the auxiliary equations defining the discontinuity surfaces can give the needed control input.

Within the sliding-mode control (SMC) theory, assuming a certain dynamic error driven to zero, one auxiliary equation (sliding surface) and the equivalent control input $u_h(t)$ can be obtained, integrating both sides of Eq. (35.82) with null initial conditions:

$$k_jx_j+\sum_{i=h}^{j-1}k_ix_i=\sum_{i=h}^{j}k_ix_i=0 \tag{35.84}$$

This equation represents the discontinuity surface (hyperplane) and just defines the necessary sliding surface $S(x_i,\,t)$ to obtain the prescribed dynamics of Eq. (35.81):

$$S(x_i,t)=\sum_{i=h}^{j}k_ix_i=0 \tag{35.85}$$

In fact, by taking the first time derivative of $S(x_i,\,t)$, $\dot{S}(x_i,t)=0$; solving it for $\mathrm{d}x_j/\mathrm{d}t$; and substituting the result in Eq. (35.83), the dynamics specified by Eq. (35.81) is obtained. This means that the control problem is reduced to a first-order problem, since it is only necessary to calculate the time derivative of Eq. (35.85) to obtain the dynamics (35.81) and the needed control input $u_h(t)$.

The sliding surface Eq. (35.85), as the dynamics of the converter subsystem, must be a Routh-Hurwitz polynomial and verify the sliding manifold invariance conditions, $S(x_i,\,t)=0$ and $\dot{S}(x_i,t)=0$. Consequently, the closed-loop controlled system behaves as a stable system of order $j-h$, whose dynamics is imposed by the coefficients k_i, which can be chosen by pole placement of the poles of the order $m=j-h$ polynomial. Alternatively, certain kinds of polynomials can be advantageously used [14]: Butterworth, Bessel, Chebyshev, elliptic (or Cauer), binomial, and minimum integral of time absolute error product (ITAE). Most useful are Bessel polynomials $B_E(s)$ (Eq. (35.88)), which minimize the system response time t_r, providing no overshoot; the polynomials $I_{TAE}(s)$ (Eq. (35.87)) that minimize the ITAE criterion for a system with desired natural oscillating frequency ω_o; and binomial

polynomials $B_I(s)$ (Eq. (35.86)). For $m>1$, ITAE polynomials give faster responses than binomial polynomials:

$$B_I(s)_m=(s+\omega_o)^m = \begin{cases} m=0\Rightarrow B_I(s)=1 \\ m=1\Rightarrow B_I(s)=s+\omega_o \\ m=2\Rightarrow B_I(s)=s^2+2\omega_o s+\omega_0^2 \\ m=3\Rightarrow B_I(s)=s^3+3\omega_o s^2+3\omega_0^2 s+\omega_0^3 \\ m=4\Rightarrow B_I(s)=s^4+4\omega_o s^3+6\omega_0^2 s^2+4\omega_0^3 s+\omega_0^4 \\ \dots \end{cases} \tag{35.86}$$

$$I_{TAE}(s)_m = \begin{cases} m=0\Rightarrow I_{TAE}(s)=1 \\ m=1\Rightarrow I_{TAE}(s)=s+\omega_o \\ m=2\Rightarrow I_{TAE}(s)=s^2+1.4\omega_o s+\omega_0^2 \\ m=3\Rightarrow I_{TAE}(s)=s^3+1.75\omega_o s^2+2.15\omega_0^2 s+\omega_0^3 \\ m=4\Rightarrow I_{TAE}(s)=s^4+2.1\omega_o s^3+3.4\omega_0^2 s^2 \\ \qquad\qquad +2.7\omega_0^3 s+\omega_0^4 \\ \dots \end{cases} \tag{35.87}$$

$$B_E(s)_m = \begin{cases} m=0\Rightarrow B_E(s) = 1 \\ m=1\Rightarrow B_E(s) = st_r+1 \\ m=2\Rightarrow B_E(s) = \dfrac{(st_r)^2+3st_r+3}{3} \\ m=3\Rightarrow B_E(s) = \dfrac{\left((st_r)^2+3.678st_r+6.459\right)(st_r+2.322)}{15} \\ \qquad\qquad = \dfrac{(st_t)^3+6(st_r)^2+15st_r+15}{15} \\ m=4\Rightarrow B_E(s) = \dfrac{(st_r)^4+10(st_r)^3+45(st_r)^2+105(st_r)+105}{105} \\ \dots \end{cases} \tag{35.88}$$

These polynomials can be the reference model for this model reference adaptive control method.

35.3.2.2 Closed-Loop Control Input–Output Decoupled Form

For closed-loop control applications, instead of the state variables x_i, it is worthy to consider, as new state variables, the errors e_{x_i}, components of the error vector $\mathbf{e}=\left[e_{x_h}, \dot{e}_{x_h}, e_{x_h}, \dots, \overset{m}{e}_{x_h}\right]^{\mathrm{T}}$ of the state-space variables x_i, relative to a given reference x_{i_r} Eq. (35.90). The new controllability canonical model of the system is

$$\frac{\mathrm{d}}{\mathrm{d}t}\left[e_{x_h}, \dots, e_{x_{j-1}}, e_{x_j}\right]^{\mathrm{T}} = \left[e_{x_{h+1}}, \dots, e_{x_j}, -f_e(\mathbf{e})+p_e(t)-b_e(\mathbf{e})u_h(t)\right]^{\mathrm{T}} \tag{35.89}$$

where $f_e(\mathbf{e})$, $p_e(t)$, and $b_e(\mathbf{e})$ are functions of the error vector $\mathbf{e}$.

As the transformation of variables

$$e_{x_i}=x_{i_r}-x_i \quad \text{with} \quad i=h,\dots,j \tag{35.90}$$

is linear, the Routh-Hurwitz polynomial for the new sliding surface $S(e_{x_i},t)$ is

$$S(e_{x_i},t)=\sum_{i=h}^{j} k_i e_{x_i}=0 \tag{35.91}$$

Since $e_{x_{i+1}}(s)=se_{x_i}(s)$, this *control law*, from Eqs. (35.86) to (35.88), can be written as $S(\mathbf{e},s)=e_{x_i}(s+\omega_o)^m$ and is robust as it does not depend on circuit parameters, disturbances, or operating conditions, but only on the imposed k_i parameters and on the state variable errors e_{x_i}, which can usually be measured or estimated. The control law Eq. (35.91) enables the desired dynamics of the output variable(s), if the semiconductor switching strategy is designed to guarantee the system stability. In practice, the finite switching frequency of the semiconductors will impose a certain dynamic error ε steered to zero. The control law Eq. (35.91) is the required controller for the closed-loop SISO subsystem with output $\mathbf{y}$.

35.3.2.3 Stability

Existence condition. The existence of the operation in sliding mode implies $S(e_{x_i},t)=0$. Also, to stay in this regime, the control system should guarantee $\dot{S}(e_{x_i},t)=0$. Therefore, the semiconductor switching law must ensure the stability condition for the system in sliding mode, written as

$$S(e_{x_i},t)\dot{S}(e_{x_i},t)<0 \tag{35.92}$$

The fulfillment of this inequality ensures the convergence of the system state trajectories to the sliding surface $S(e_{x_i},t)=0$, since

- if $S(e_{x_i},t)>0$ and $\dot{S}(e_{x_i},t)<0$, then $S(e_{x_i},t)$ will decrease to zero,
- if $S(e_{x_i},t)<0$ and $\dot{S}(e_{x_i},t)>0$, then $S(e_{x_i}t)$ will increase toward zero.

Hence, if Eq. (35.92) is verified, then $S(e_{x_i},t)$ will converge to zero. The condition (35.92) is the manifold $S(e_{x_i},t)$ invariance condition or the sliding-mode existence condition.

Given the state-space model Eq. (35.89) as a function of the error vector $\mathbf{e}$ and, from $\dot{S}(e_{x_i},t)=0$, the equivalent average control input $U_{eq}(t)$ that must be applied to the system in order that the system state slides along the surface, Eq. (35.91) is given by

$$U_{eq}(t)=\frac{k_h\dfrac{\mathrm{d}e_{x_h}}{\mathrm{d}t}+k_{h+1}\dfrac{\mathrm{d}e_{x_{h+1}}}{\mathrm{d}t}+\dots+k_{j-1}+\dfrac{\mathrm{d}e_{x_{j-1}}}{\mathrm{d}t}+k_j(-f_e(\mathbf{e})+p_e(t))}{k_j b_e(\mathbf{e})} \tag{35.93}$$

This control input $U_{eq}(t)$ ensures the converter subsystem operation in the sliding mode.

Reaching condition. The fulfillment of $S(e_{x_i},t)\dot{S}(e_{x_i},t)<0$ as $S(e_{x_i},t)\dot{S}(e_{x_i},t)=(1/2)\dot{S}^2(e_{x_i},t)$ implies that the distance between the system state and the sliding surface will tend to zero, since $S^2(e_{x_i},t)$ can be considered as a measure for this distance. This means that the system will reach sliding mode. Additionally, from Eq. (35.89), it can be written as

$$\frac{de_{x_j}}{dt}=-f_e(\mathbf{e})+p_e(t)-b_e(\mathbf{e})u_h(t) \tag{35.94}$$

From Eq. (35.91), Eq. (35.95) is obtained:

$$S(e_{x_i}t)=\sum_{i=h}^{j}k_ie_{x_i}=k_he_{x_h}+k_{h+1}\frac{\mathrm{d}e_{x_h}}{\mathrm{d}t}+k_{h+2}\frac{\mathrm{d}^2e_{x_h}}{\mathrm{d}t^2}+\ldots+k_j\frac{\mathrm{d}^me_{x_h}}{\mathrm{d}t^m} \tag{35.95}$$

If $S(e_{x_i},t)>0$, from the Routh-Hurwitz property of Eq. (35.91), then $e_{x_j}>0$. In this case, to reach $S(e_{x_i},t)=0$, it is necessary to impose $-b_e(\mathbf{e})u_h(t)=-U$ in Eq. (35.94), with U chosen to guarantee $\mathrm{d}e_{x_j}/\mathrm{d}t<0$. After a certain time, e_{x_j} will be $e_{x_j}=\mathrm{d}^me_{x_h}/\mathrm{d}t^m<0$, implying along with Eq. (35.95) that $\dot{S}(e_{x_i},t)<0$, thus verifying Eq. (35.92). Therefore, every term of $S(e_{x_i},t)$ will be negative, which implies, after a certain time, an error $e_{x_h}<0$ and $S(e_{x_i},t)<0$. Hence, the system will reach sliding mode, staying there if $U=U_{eq}(t)$. This same reasoning can be made for $S(e_{x_i},t)<0$; it is now being necessary to impose $-b_e(\mathbf{e})u_h(t)=+U$, with U high enough to guarantee $\mathrm{d}e_{x_j}/\mathrm{d}t>0$.

To ensure that the system always reaches sliding-mode operation, it is necessary to calculate the maximum value of $U_{eq}(t)$ and U_{eqmax} and also impose the reaching condition:

$$U>U_{eqmax} \tag{35.96}$$

This means that the power supply voltage values U should be chosen high enough to additionally account for the maximum effects of the perturbations. With step inputs, even with $U>U_{eqmax}$, the converter usually loses sliding mode, but it will reach it again, even if the U_{eqmax} is calculated considering only the maximum steady-state values for the perturbations.

35.3.2.4 Switching Law

From the foregoing considerations, supposing a system with two possible structures, the semiconductor switching strategy must ensure $S(e_{x_i},t)\dot{S}(e_{x_i},t)<0$. Therefore, if $S(e_{x_i},t)>0$, then $\dot{S}(e_{x_i},t)<0$, which implies, as seen, $-b_e(\mathbf{e})u_h(t)=-U$ (the sign of $b_e(\mathbf{e})$ must be known). Also, if $S(e_{x_i},t)<0$, then $\dot{S}(e_{x_i},t)>0$, which implies $-b_e(\mathbf{e})u_h(t)=+U$. This imposes the switching between two structures at infinite frequency. Since power semiconductors can only switch at finite frequency, in practice, a small enough error for $S(e_{x_i},t)$ must be allowed $(-\varepsilon<S(e_{x_i},t)<+\varepsilon)$. Hence, the switching law between the two possible system structures might be

$$u_h(t)=\begin{cases}U/b_e(\mathbf{e}) \text{ for } S(e_{x_i}t)>+\varepsilon\\ -U/b_e(\mathbf{e}) \text{ for } S(e_{x_i}t)<-\varepsilon\end{cases} \tag{35.97}$$

The condition Eq. (35.97) determines the control input to be applied and therefore represents the semiconductor switching strategy or switching function. This law determines a two-level pulse-width modulator with JIT switching (variable frequency).

35.3.2.5 Robustness

The dynamics of a system, with closed-loop control using the control law Eq. (35.91) and the switching law Eq. (35.97), does not depend on the system operating point, load, circuit parameters, power supply, or bounded disturbances, as long as the control input $u_h(t)$ is large enough to maintain the converter subsystem in sliding mode. Therefore, it is said that the switching power converter dynamics, operating in sliding mode, is robust against changing operating conditions, variations of circuit parameters, and external disturbances. The desired dynamics for the output variable(s) is determined only by the k_i coefficients of the control law Eq. (35.91), as long as the switching law (35.97) maintains the converter in sliding mode.

35.3.3 Constant-Frequency Operation

Prefixed switching frequency can be achieved, even with the sliding-mode controllers, at the cost of losing the JIT action. As the sliding-mode controller changes the control input when needed and not at a certain prefixed rhythm, applications needing constant switching frequency (such as thyristor rectifiers or resonant converters) must compare $S(e_{xi}, t)$ (hysteresis width 2ι much narrower than 2ε) with auxiliary triangular waveforms (Fig. 35.25A), auxiliary sawtooth functions (Fig. 35.25B), three-level clocks (Fig. 35.25C), or phase-locked loop control of the comparator hysteresis variable width 2ε [15]. However, as illustrated in Fig. 35.25D, steady-state errors do appear. Often, they should be eliminated as described in Section 35.3.4.

35.3.4 Steady-State Error Elimination in Converters with Continuous Control Inputs

In the ideal sliding mode, state trajectories are directed toward the sliding surface (35.91) and move exactly along the discontinuity surface, switching between the possible system structures at infinite frequency. Practical sliding modes cannot switch at infinite frequency and therefore exhibit phase-plane trajectory oscillations inside a hysteresis band of width 2ε, centered in the discontinuity surface.

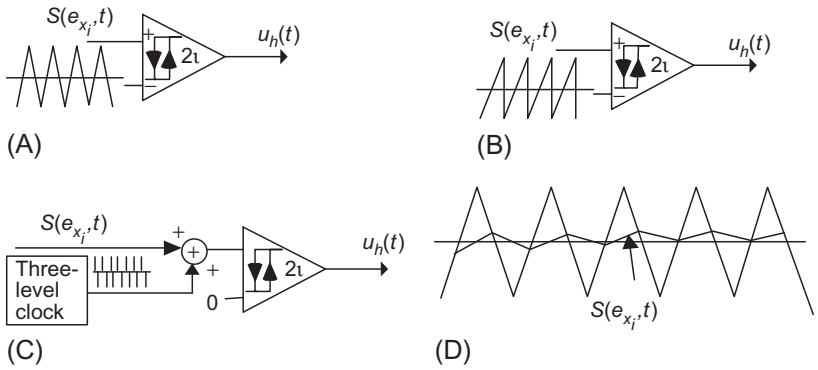


FIG. 35.25 Auxiliary functions and methods to obtain constant switching frequency with sliding-mode controllers. (A) Using a triangular carrier; (B) using a sawtooth carrier; (C) using a three-level clock; (D) generation of steady-state error.

The switching law Eq. (35.91) permits no steady-state errors as long as $S(e_{x_i}, t)$ tends to zero, which implies no restrictions on the commutation frequency. Control circuits operating at constant frequency or needed continuous inputs or particular limitations of the power semiconductors, such as minimum on or off times, can originate $S(e_{x_i}, t) = \varepsilon_1 \neq 0$. The steady-state error (e_{x_h}) of the x_h variable $x_{h_r} - x_h = \varepsilon_1 / k_h$ can be eliminated, increasing the system order by 1. The new state-space controllability canonical form, considering the error e_{x_j}, between the variables and their references, as the state vector, is

$$\frac{\mathrm{d}}{\mathrm{d}t}\left[\int e_{x_h}dt, e_{x_h}, \ldots, e_{x_{j-1}}, e_{x_j}\right]^{\mathrm{T}} = \left[e_{x_h}, e_{x_{h+1}}, \ldots, e_{x_j}, -f_e(\mathbf{e}) - p_e(t) - b_e(\mathbf{e})u_h(t)\right]^{\mathrm{T}} \tag{35.98}$$

The new sliding surface $S(e_{x_i}, t)$ written from Eq. (35.91), considering the new system in Eq. (35.98), is

$$S(e_{x_i}t) = k_0 \int e_{x_h}\mathrm{d}t + \sum_{i=h}^{j} k_i e_{x_i} = 0 \tag{35.99}$$

This sliding surface offers zero-state error, even if $S(e_{x_i}, t) = \varepsilon_1$ due to the hardware errors or fixed (or limited) frequency switching. Indeed, at the steady state, the only nonzero term is $k_0 \int e_{x_h}\mathrm{d}t = \varepsilon_1$. Also, like Eq. (35.91), this closed-loop control law does not depend on system parameters or perturbations to ensure a prescribed closed-loop dynamics similar to Eq. (35.81) with an error approaching zero.

The approach outlined herein precisely defines the control law (sliding surface (35.91) or (35.99)) needed to obtain the selected dynamics and the switching law Eq. (35.97). As the control law allows the implementation of the system controller and the switching law gives the PWM modulator, there is no need to design linear or nonlinear controllers, based on linear converter models, or devise offline PWM modulators. Therefore, sliding-mode control theory, applied to switching power converters, provides a systematic method to generate both the controller(s) (usually nonlinear) and the modulator(s) that will ensure a model reference robust dynamics, solving the control problem of switching power converters.

In the next examples, it is shown that the sliding-mode controllers use (nonlinear) state feedback, therefore, needing to measure the state variables and often other variables, since they use more system information. This is a disadvantage since more sensors are needed. However, the straightforward control design and obtained performances are much better than those obtained with the averaged models, the use of more sensors being really valued. Alternatively to the extra sensors, state observers can be used [12,13].

35.3.5 Examples: Buck–Boost DC/DC Converter, Half-bridge Inverter, 12-Pulse Parallel Rectifiers, Audio Power Amplifiers, Near Unity Power Factor Rectifiers, Multilevel Inverters, Matrix Converters

EXAMPLE 35.10 Sliding-mode control of the buck–boost dc/dc converter

Consider again the buck-boost converter of Fig. 35.1 and assume the converter output voltage v_o to be the controlled output. From Section 35.2, using the switched state-space model of Eq. (35.11), making $\mathrm{d}v_o/\mathrm{d}t = \theta$, and calculating the first time derivative of θ, the controllability canonical model (35.100), where $i_o = v_o/R_o$, is obtained:

$$\begin{aligned}\frac{\mathrm{d}v_o}{\mathrm{d}t} &= \theta = \frac{1-\delta(t)}{C_o}i_L - \frac{i_o}{C_o}\\ \frac{\mathrm{d}\theta}{\mathrm{d}t} &= -\frac{(1-\delta(t))^2}{L_i C_o}v_o - \frac{C_o\theta + i_o}{C_o(1-\delta(t))}\frac{\mathrm{d}\delta(t)}{\mathrm{d}t}\\ &\quad -\frac{1}{C_o}\frac{\mathrm{d}i_o}{\mathrm{d}t} + \frac{\delta(t)(1-\delta(t))}{C_o L_i}V_{DC}\end{aligned} \tag{35.100}$$

This model, written in the form of Eq. (35.80), contains two state variables, v_o and θ. Therefore, from Eq. (35.91) and considering $e_{v_o} = v_{o_r} - v_o, e_\theta = \theta_r - \theta$, the control law (sliding surface) is

$$S(e_{x_i}t)=\sum_{i=h}^{2}k_i e_{x_i}=k_1(v_{o_r}-v_o)+k_2\frac{\mathrm{d}v_{o_r}}{\mathrm{d}t}-k_2\frac{\mathrm{d}v_o}{\mathrm{d}t}$$
$$=k_1(v_{o_r}-v_o)+k_2\frac{\mathrm{d}v_{or}}{\mathrm{d}t}-\frac{k_2}{C_o}(1-\delta(t))i_L$$
$$+\frac{k_2}{C_o}i_o=0 \tag{35.101}$$

This sliding surface depends on the variable $\delta(t)$, which should be precisely the result of the application, in Eq. (35.101), of a switching law similar to Eq. (35.97). Assuming an ideal up-down converter and slow variations, from Eq. (35.31), the variable $\delta(t)$ can be averaged to $\delta_1=v_o/(v_o+V_{DC})$. Substituting this relation in Eq. (35.101) and rearranging, Eq. (35.102) is derived:

$$S(e_{x_i}t)=\frac{C_o k_1}{k_2}\left(\frac{v_o+V_{DC}}{v_o}\right)$$
$$\times\left((v_{or}-v_0)+\frac{k_2}{k_1}\frac{\mathrm{d}v_{o_r}}{\mathrm{d}t}+\frac{k_2}{k_1}\frac{1}{C_o}i_o\right)-i_L=0 \tag{35.102}$$

This control law shows that the power supply voltage V_{DC} must be measured, as well as the output voltage v_o and the currents i_o and i_L.

To obtain the switching law from stability considerations (35.92), the time derivative of $S(e_{x_i},t)$, supposing $(v_o+V_{DC})/v_o$ almost constant, is

$$\dot{S}(e_{x_i},t)=\frac{C_o k_1}{k_2}\left(\frac{v_o+V_{DC}}{v_o}\right)$$
$$\times\left(\frac{\mathrm{d}e_{v_o}}{\mathrm{d}t}+\frac{k_2}{k_1}\frac{\mathrm{d}^2v_{o_r}}{\mathrm{d}t^2}+\frac{k_2}{k_1C_o}\frac{\mathrm{d}i_o}{\mathrm{d}t}\right)-\frac{\mathrm{d}i_L}{\mathrm{d}t} \tag{35.103}$$

If $S(e_{x_i},t)>0$, then, from Eq. (35.92), $\dot{S}(e_{x_i},t)<0$ must hold. Analyzing Eq. (35.103), we can conclude that, if $S(e_{x_i},t)>0$, $\dot{S}(e_{x_i},t)$ is negative if, and only if, $\mathrm{d}i_L/\mathrm{d}t>0$. Therefore, for positive errors $e_{v_o}>0$, the current i_L must be increased, which implies $\delta(t)=1$. Similarly, for $S(e_{x_i},t)<0$, $\mathrm{d}i_L/\mathrm{d}t<0$, and $\delta(t)=0$. Thus, a switching law similar to Eq. (35.97) is obtained:

$$\delta(t)=\begin{cases}1 & \text{for } S(e_{x_i},t)>+e\\ 0 & \text{for } S(e_{x_i},t)<-e\end{cases} \tag{35.104}$$

The same switching law could be obtained from knowing the dynamic behavior of this nonminimum-phase up-down converter: to increase (decrease) the output voltage, a previous increase (decrease) of the i_L current is mandatory.

Eq. (35.101) shows that, if the buck-boost converter is into the sliding mode ($S(e_{x_i},t)=0$), the dynamics of the output voltage error tends exponentially to zero with time constant k_2/k_1 ($k_2/k_1>0$). Since during step transients, the converter is in the reaching mode, the time constant k_2/k_1 cannot be designed to originate error variations larger than the one allowed by the self-dynamics of the converter excited by a certain maximum permissible i_L current. Given the polynomials (35.86–35.88) with $m=1$, $k_1/k_2=\omega_o$ should be much lower than the finite switching frequency ($1/T$) of the converter. Therefore, the time constant must obey $k_2/k_1\gg T$. Then, knowing that k_2 and k_1 are both imposed, the control designer can tailor the time constant as needed, provided that the above restrictions are observed.

Short-circuit-proof operation for the sliding-mode-controlled buck-boost converter can be derived from Eq. (35.102), noting that all the terms to the left of i_L represent the set point for this current. Therefore, limiting these terms (Fig. 35.26, saturation block, with $i_{Lmax}=40$ A), the switching law (35.104) ensures that the output current will not rise above the maximum imposed limit. Given the converter nonminimum-phase behavior, this i_L current limit is fundamental to reach the sliding mode of operation with step disturbances.

The block diagram (Fig. 35.26A) of the implemented control law Eq. (35.102) (with $C_o k_1/k_2=4$) and switching law (35.103) (with $\varepsilon=0.3$) does not include the time derivative of the reference ($\mathrm{d}v_{o_r}/\mathrm{d}t$) since, in a dc/dc converter, its value is considered zero. The controller hardware (or software), derived using just the sliding-mode approach, operates only in a closed-loop.

The resulting performance (Fig. 35.26B) is much better than that obtained with the PID notch filter (compare with Example 35.4 and Fig. 35.9B), with a higher response speed and robustness against power supply variations.

35.3.5.1 Example 35.11: Sliding Mode Control of the Single-Phase Half-Bridge Converter

Consider the half-bridge four-quadrant converter of Fig. 35.27 with the output filter and the inductive load ($V_{DCmax}=300$ V, $V_{DCmin}=230$ V, $R_i=0.1\ \Omega$, $L_o=4$ mH, $C_o=470\ \mu$F, inductive load with nominal values $R_o=7\ \Omega$, and $L_o=1$ mH).

Assuming that power switches, output filter capacitor, and power supply are all ideal and a generic load with allowed slow variations, the switched state-space model of the converter, with state variables v_o and i_L, is

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix}v_o\\ i_L\end{bmatrix}=\begin{bmatrix}0 & 1/C_o\\ -1/L_o & -R_i/L_o\end{bmatrix}\begin{bmatrix}v_o\\ i_L\end{bmatrix}$$
$$+\begin{bmatrix}-1/C_o & 0\\ 0 & 1/L_o\end{bmatrix}\begin{bmatrix}i_o\\ \delta(t)V_{DC}\end{bmatrix} \tag{35.105}$$

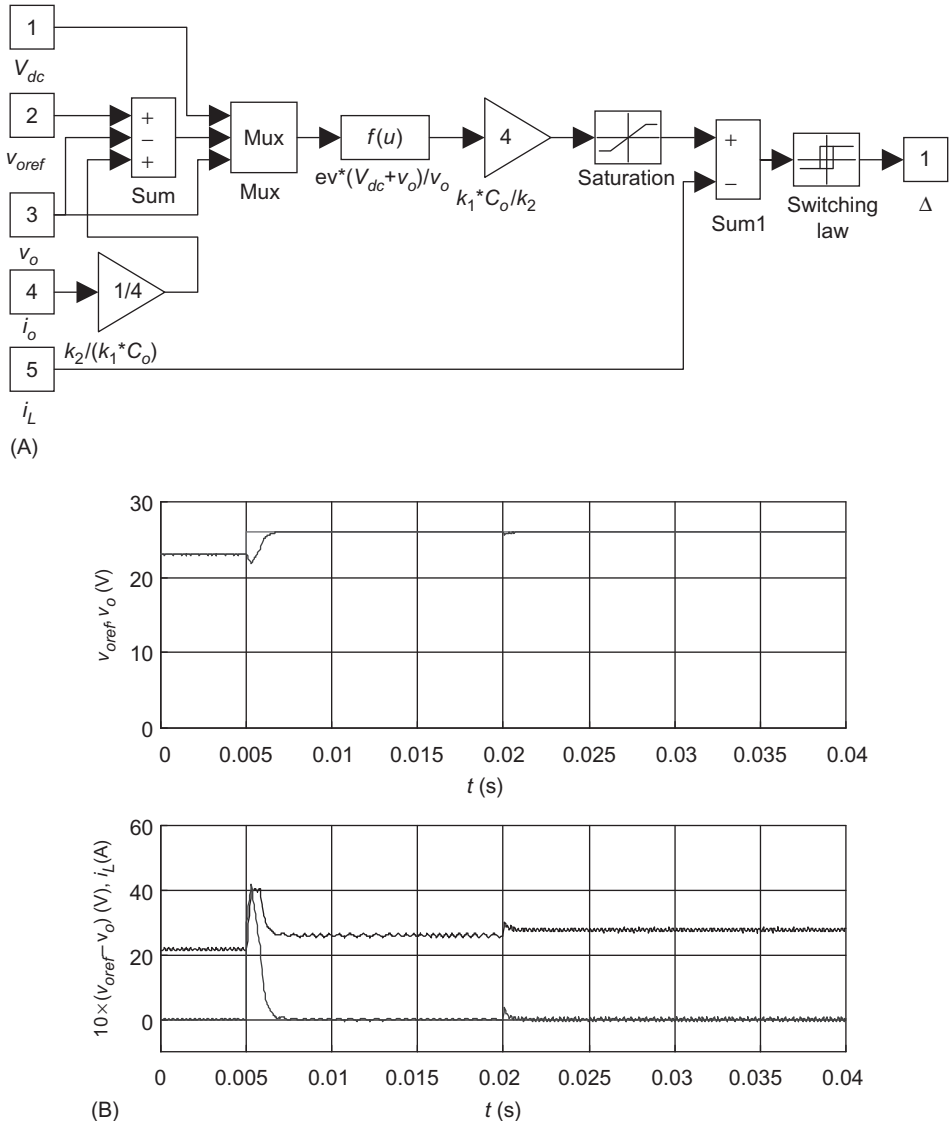


FIG. 35.26 (A) Block diagram of the sliding-mode nonlinear controller for the buck-boost converter and (B) transient responses of the sliding-mode-controlled buck-boost converter. At $t=0.005$ s, v_{oref} step from 23 to 26 V. At $t=0.02$ s, V_{DC} step from 26 to 23 V. Top graph: step reference v_{oref} and output voltage v_o. Bottom graph: trace starting at 20 is i_L current; trace starting at zero is $10\times(v_{oref}-v_o)$.

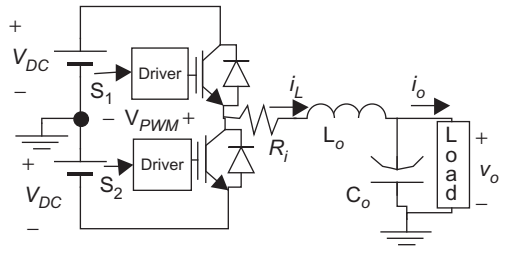


FIG. 35.27 Half-bridge power inverter with insulated-gate bipolar transistors, output filter, and load.

where i_o is the generic load current and $v_{PWM}=\delta(t)V_{DC}$ is the extended PWM output voltage ($\delta(t)=+1$ when one of the upper main semiconductors of Fig. 35.27 is conducting and $\delta(t)=-1$ when one of the lower semiconductors is on).

Output current control (current-mode control)

To perform as a v_{i_L} voltage-controlled i_L current source (or sink) with transconductance g_m ($g_m=i_L/v_{i_L}$), this converter must supply a current i_L to the output inductor, obeying $i_L=g_m v_{i_L}$. Using a bounded v_{i_L} voltage to provide output short-circuit protection, the reference current for a sliding-mode controller must be $i_{L_r}=g_m v_{iL}$. Therefore, the controlled output is the i_L current, and the controllability canonical model (35.106) is obtained from the second equation of (35.105), since the dynamics of this

subsystem, being governed by $\delta(t)V_{DC}$, is already in the controllability canonical form for this chosen output:

$$\frac{di_L}{dt} = -\frac{R_i}{L_o}i_L - \frac{1}{L_o}v_o + \frac{\delta(t)V_{DC}}{L_o} \tag{35.106}$$

A suitable sliding surface (35.107) is obtained from Eq. (35.91), making $e_{i_L} = i_{L_r} - i_L$:

$$S(e_{i_L}, t) = k_p e_{i_L} = k_p(i_{L_r} - i_L) = k_p(g_m v_{i_L} - i_L) = 0 \tag{35.107}$$

The switching law Eq. (35.108) can be devised calculating the time derivative of Eq. (35.107) $\dot{S}(e_{i_L}, t)$ and applying Eq. (35.92). If $S(e_{i_L}, t) > 0$, then $di_L/dt > 0$ must hold to obtain $S(e_{i_L}, t) < 0$, implying $\delta(t) = 1$:

$$\delta(t) = \begin{cases} 1 & \text{for } S(e_{i_L}t) > +\varepsilon \\ -1 & \text{for } S(e_{i_L}t) < -\varepsilon \end{cases} \tag{35.108}$$

The k_p value and the allowed ripple ε define the instantaneous value of the variable switching frequency. The sliding-mode controller is represented in Fig. 35.28A. Step response (Fig. 35.29A) shows the variable-frequency operation, a very short rise time (limited only by the available power supply), and confirms the expected robustness against supply variations.

For systems where fixed-frequency operation is needed, a triangular wave, with frequency (10 kHz) slightly greater than the maximum variable frequency, can be added (Fig. 35.28B) to the sliding-mode controller, as explained in Section 35.3.3. Performances (Fig. 35.29B) are comparable with those of the variable-frequency sliding-mode controller (Fig. 35.29A). Fig. 35.29B shows not only the constant switching frequency but also a steady-state error dependent on the operating point.

To eliminate this error, a new sliding surface Eq. (35.109), based on Eq. (35.99), should be used. The constants k_p and k_0 can be calculated, as discussed in Example 35.10:

$$S(e_{i_L}t) = k_0 \int e_{i_L} dt + k_p e_{i_L} = 0 \tag{35.109}$$

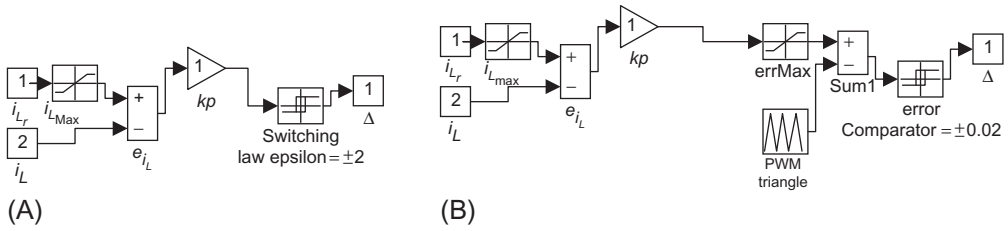


FIG. 35.28 (A) Implementation of short-circuit-proof sliding-mode current controller (variable frequency) and (B) implementation of fixed-frequency, short-circuit-proof sliding-mode current controller using a triangular waveform.

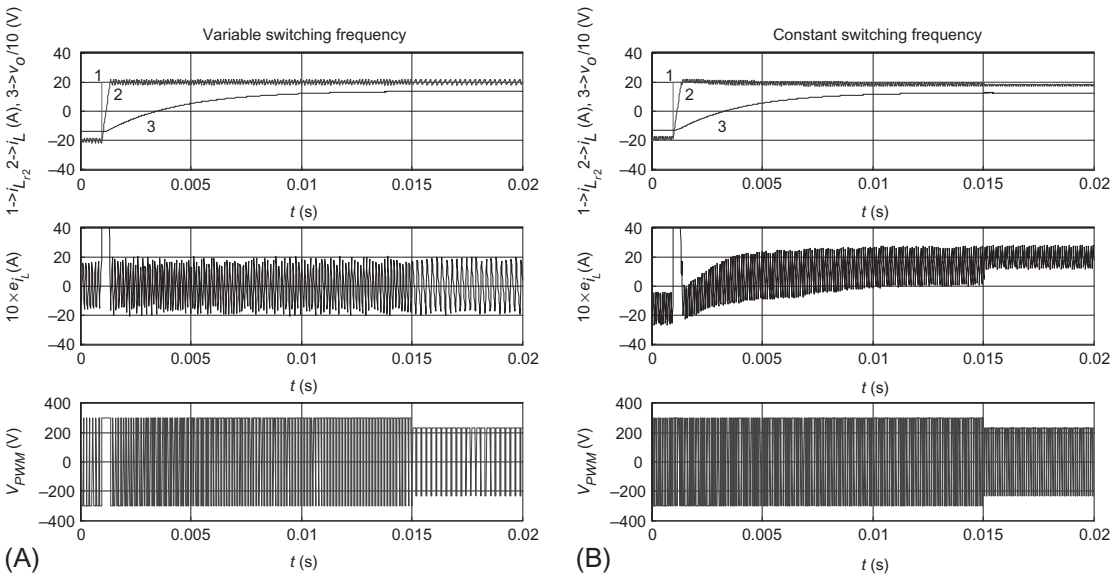


FIG. 35.29 Performance of the transconductance amplifier; response to an i_{Lr} step from −20 to 20 A at $t = 0.001$ s and to a V_{DC} step from 300 to 230 V at $t = 0.015$ s: (A) variable-frequency sliding-mode controller and (B) fixed-frequency sliding-mode controller.

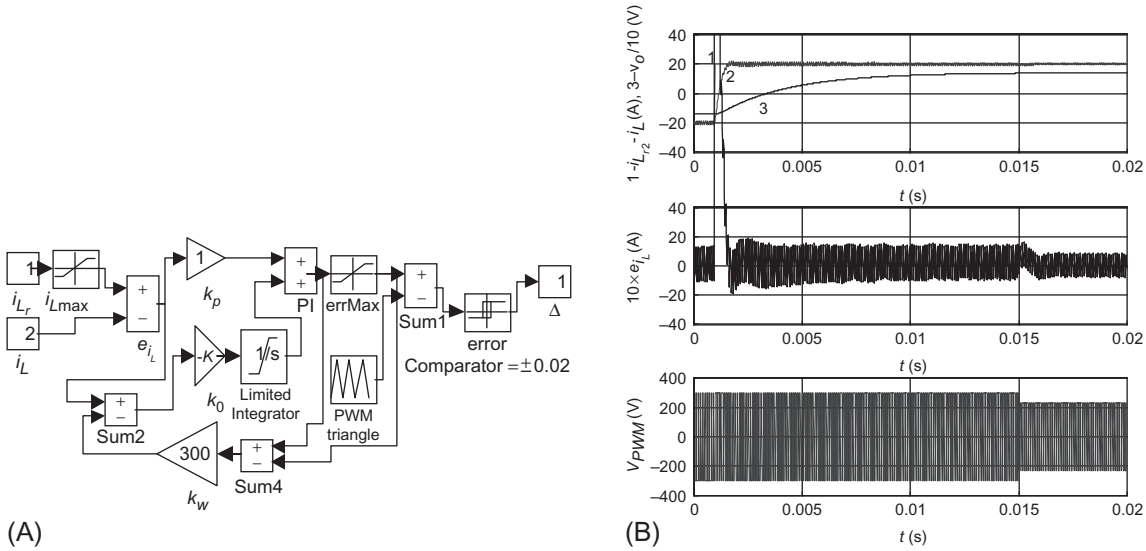


FIG. 35.30 (A) Block diagram of the average current-mode controller (sliding mode) and (B) performance of the fixed-frequency sliding-mode controller with removed steady-state error: response to an i_{L_r} step from −20 to 20 A at $t=0.001$ s and to a V_{DC} step from 300 to 230 V at $t=0.015$ s.

The new constant-frequency sliding-mode current controller (Fig. 35.30A), with added antiwindup techniques (Example 35.6), since a saturation (errMax) is needed to keep the frequency constant, now presents no steady-state error (Fig. 35.30B). Performances are comparable with those of the variable-frequency controller, and no robustness loss is visible. The applied sliding-mode approach led to the derivation of the known average current-mode controller.

Output voltage control

To obtain a power operational amplifier suitable for building uninterruptible power supplies, power filters, power gyrators, inductance simulators, or power factor active compensators, v_o must be the controlled converter output. Therefore, using the input-output linearization technique, it is seen that the first time derivative of the output $(\mathrm{d}v_o/\mathrm{d}t)=(i_L-i_o)/C_o=\theta$ does not explicitly contain the control input $\delta(t)V_{DC}$. Then, the second derivative must be calculated. Taking into account Eq. (35.105), as $\theta=(i_L-i_o)/C_o$, Eq. (35.110) is derived

$$\frac{\mathrm{d}^2 v_o}{\mathrm{d}t^2}=\frac{\mathrm{d}}{\mathrm{d}t}\theta=\frac{\mathrm{d}}{\mathrm{d}t}\left(\frac{i_L-i_o}{C_o}\right)=-\frac{R_i}{L_o}\theta-\frac{1}{L_oC_o}v_o-\frac{R_i}{L_oC_o}i_o-\frac{1}{C_o}\frac{\mathrm{d}i_o}{\mathrm{d}t}+\frac{1}{L_oC_o}\delta(t)V_{DC} \tag{35.110}$$

This expression shows that the second derivative of the output depends on the control input $\delta(t)V_{DC}$. No further time derivative is needed, and the state-space equations of the equivalent circuit, written in the phase canonical form, are

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} v_o \\ \theta \end{bmatrix}=\begin{bmatrix} \theta \\ -\frac{R_i}{L_o}\theta-\frac{1}{L_oC_o}v_o-\frac{R_i}{L_oC_o}i_o-\frac{1}{C_o}\frac{\mathrm{d}i_o}{\mathrm{d}t}+\frac{1}{L_oC_o}\delta(t)V_{DC} \end{bmatrix} \tag{35.111}$$

According to Eqs. (35.91), (35.111), and (35.105), considering that e_{v_o} is the feedback error $e_{v_o}=v_{o_r}-v_o$, a sliding surface $S(e_{v_o},t)$ can be chosen:

$$S(e_{v_o}t)=k_1e_{v_o}+k_2\frac{\mathrm{d}e_{v_o}}{\mathrm{d}t}=e_{v_o}+\frac{k_2}{k_1}\frac{\mathrm{d}e_{v_o}}{\mathrm{d}t}=e_{v_o}+\beta\frac{\mathrm{d}e_{v_o}}{\mathrm{d}t}=\frac{C_o}{\beta}(v_{o_r}-v_o)+C_o\frac{\mathrm{d}v_{o_r}}{\mathrm{d}t}+i_o-i_L=0 \tag{35.112}$$

where β is the time constant of the desired first-order response of output voltage ($\beta\gg T>0$), as the strong relative degree [13] of this system is 2, and the sliding-mode operation reduces by one, the order of this system (the strong relative degree of a system is the least positive integer r for which the rth derivative of the output $\mathrm{d}^r v_o/\mathrm{d}t^r$ is an explicit function of the control input u, being $\mathrm{d}^i v_o/\mathrm{d}u=0$ for $0\le i\le r-1$ and $\mathrm{d}^r v_o/\mathrm{d}u\neq 0$).

Calculating $\dot{S}(e_{v_o},t)$, the control strategy (switching law) Eq. (35.113) can be devised since, if $S(e_{v_o},t)>0$, then $\mathrm{d}i_L/\mathrm{d}t$ must be positive to obtain $\dot{S}(e_{i_L},t)<0$, implying $\delta(t)=1$. Otherwise, $\delta(t)=-1$:

$$\delta(t)=\begin{cases} 1 & \text{for } S(e_{v_o},t)>0 \,(v_{PWM}=+V_{DC}) \\ -1 & \text{for } S(e_{v_o},t)<0 \,(v_{PWM}=-V_{DC}) \end{cases} \tag{35.113}$$

In the ideal sliding-mode dynamics, the filter input voltage v_{PWM} switches between V_{DC} and $-V_{DC}$ with the infinite frequency. This switching generates the equivalent control voltage V_{eq} that must satisfy the sliding manifold invariance conditions, $S(e_{v_o},t)=0$ and $\dot{S}(e_{v_o},t)=0$. Therefore, from $\dot{S}(e_{v_o},t)=0$, using Eqs. (35.112) and (35.105) (or from Eq. (35.110)), V_{eq} is

$$V_{eq} = L_o C_o \left[\frac{d^2 v_{o_r}}{dt^2} + \frac{1}{\beta} \frac{dv_{o_r}}{dt} + \frac{v_o}{L_o C_o} + \frac{(\beta R_i - L_o) i_L}{\beta L_o C_o} \frac{i_o}{\beta C_o} + \frac{1}{C_o} \frac{di_o}{dt} \right] \tag{35.114}$$

This equation shows that only smooth input v_{o_r} signals ("smooth" functions) can be accurately reproduced at the inverter output, as it contains derivatives of the v_{o_r} signal. This fact is a consequence of the stored electromagnetic energy. The existence of the sliding-mode operation implies the following necessary and sufficient condition:

$$-V_{DC} < V_{eq} < V_{DC} \tag{35.115}$$

Eq. (35.115) enables the determination of the minimum input voltage V_{DC} needed to enforce the sliding-mode operation. Moreover, even in the case of $|V_{eq}| > |V_{DC}|$, the system experiences only a saturation transient and eventually reaches the region of sliding-mode operation, except if the operating point and disturbances enforce $|V_{eq}| > |V_{DC}|$ in steady state.

In the ideal sliding mode, at infinite switching frequency, state trajectories are directed toward the sliding surface and move exactly along the discontinuity surface. Practical switching power converters cannot switch at infinite frequency, so a typical implementation of Eq. (35.112) (Fig. 35.31A) with neglected $\dot{v}_{o_r}$ features a comparator with hysteresis 2ε, switching occurring at $|S(e_{v_o}, t)| > \varepsilon$ with frequency depending on the slopes of i_L. This hysteresis causes phase-plane trajectory oscillations of width 2ε around the discontinuity surface $S(e_{v_o}, t) = 0$, but the V_{eq} voltage is still correctly generated, since the resulting duty cycle is a continuous variable (except for error limitations in the hardware or software, which can be corrected using the approach pointed out by Eq. (35.98)).

The design of the compensator and the modulator is integrated with the same theoretical approach, since the signal $S(e_{v_o}, t)$ applied to a comparator generates the pulses for the power semiconductors drives. If the short-circuit-proof operation is built into the power semiconductor drives, there is the possibility to measure only the capacitor current $(i_L - i_o)$.

Short-circuit protection and fixed-frequency operation of the power operational amplifier

If we note that all the terms to the left of i_L in Eq. (35.112) represent the value of i_{L_r}, a simple way to provide short-circuit protection is to bound the sum of all these terms (Fig. 35.31A with $i_{L_{rmax}} = 100$A). Alternatively, the output current controllers of Fig. 35.28 can be used, comparing Eq. (35.107) with Eq. (35.112), to obtain $i_{L_r} = S(e_{v_o}, t)/k_p + i_L$. Therefore, the block diagram of Fig. 35.31A provides the i_{L_r} output (for $k_p = 1$) to be the input of the current controllers (Figs. 35.28 and 35.31A). As seen, the controllers of Figs. 35.28B and 35.30A also ensure fixed-frequency operation.

For comparison purposes, a proportional-integral (PI) controller, with antiwindup (Fig. 35.31B) for output voltage control, was designed, supposing the current-mode control of the half bridge ($i_{L_r} = g_m v_{i_L}/(1 + sT_d)$ considering a small delay T_d) and a pure resistive load R_o and using the approach outlined in Examples 35.6 and 35.8 ($k_v = 1$, $g_m = 1$, $\zeta^2 = 0.5$, and $T_d = 600$ μs). The obtained PI (35.50) parameters are

$$\begin{aligned} T_z &= R_o C_o \\ T_p &= 4\zeta^2 g_m k_v R_o T_d \end{aligned} \tag{35.116}$$

Both variable frequency (Fig. 35.32) and constant frequency (Fig. 35.33) sliding-mode output voltage controllers present excellent performance and robustness with nominal loads. With loads much higher than the nominal value (Figs. 35.32B and 35.33B), the performance and robustness are also excellent. The sliding-mode constant-frequency PWM controller presents the additional advantage of injecting lower ripple in the load.

As expected, the PI regulator presents lower performance (Fig. 35.34). The response speed is lower, and the insensitivity to power supply and load variations (Fig. 35.34B) is not as high as with the sliding mode. Nevertheless, the PI performances are acceptable, since its design was carried considering a slow and fast manifold sliding-mode approach: the fixed-frequency sliding-mode current controller (35.109) for the fast manifold (the i_L current dynamics) and the antiwindup PI for the slow manifold (the v_o voltage dynamics, usually much slower than the current dynamics).

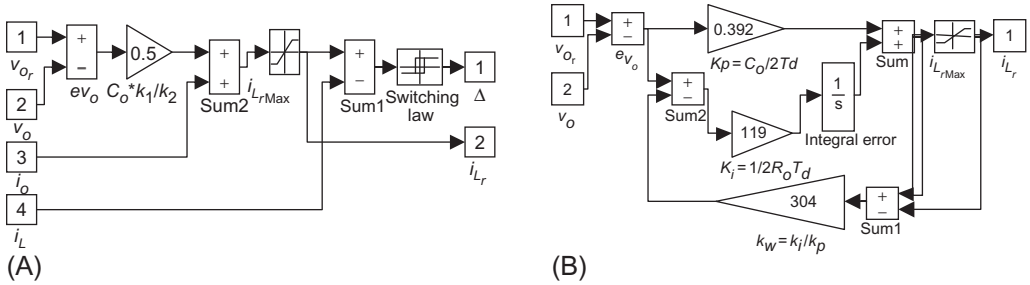


FIG. 35.31 (A) Implementation of short-circuit-proof, sliding-mode output voltage controller (variable frequency) and (B) implementation of antiwindup PI current-mode (fixed frequency) controller.

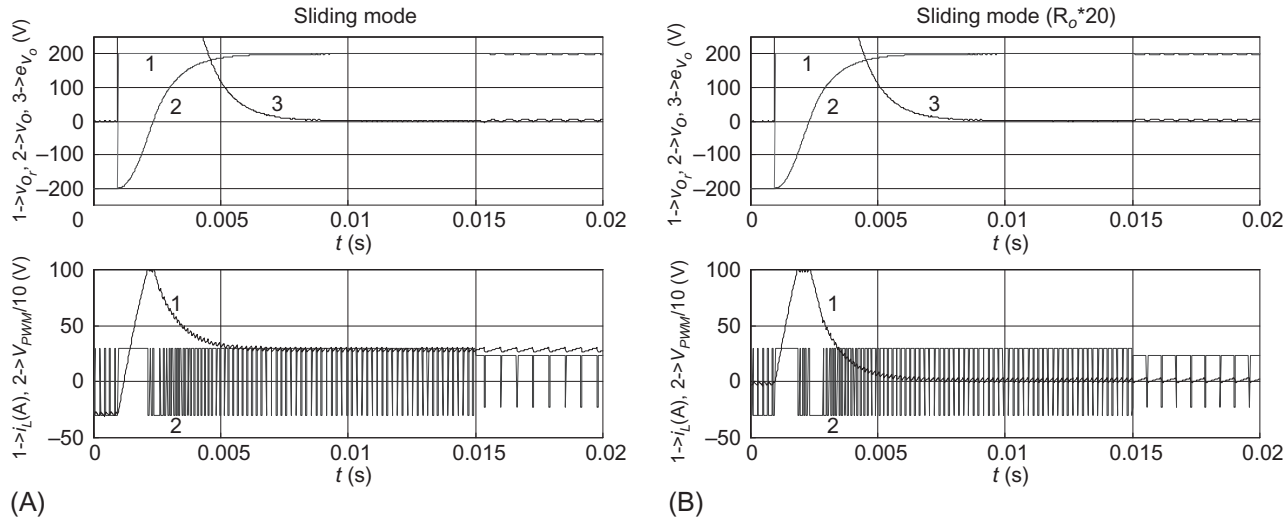


FIG. 35.32 Performance of the power operational amplifier; response to a v_{o_r} step from −200 to 200 V at $t=0.001$ s and to a V_{DC} step from 300 to 230 V at $t=0.015$ s: (A) variable-frequency sliding mode (nominal load) and (B) variable-frequency sliding mode ($R_o \times 20$).

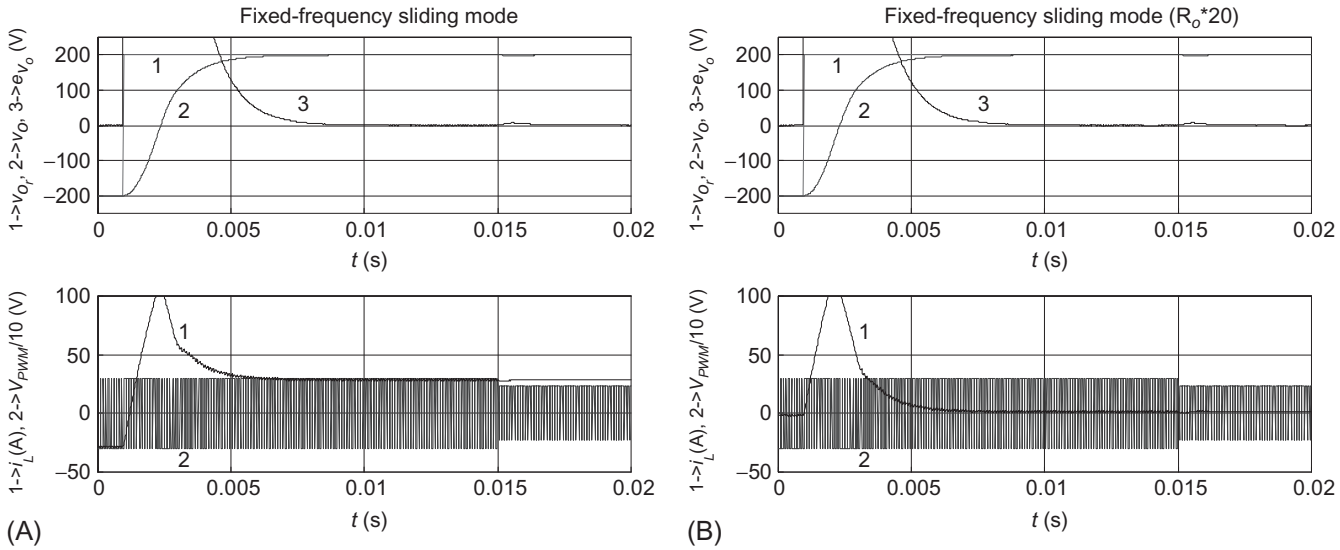


FIG. 35.33 Performance of the power operational amplifier; response to a v_{o_r} step from −200 to 200 V at $t=0.001$ s and to a V_{DC} step from 300 to 230 V at $t=0.015$ s: (A) fixed-frequency sliding mode (nominal load) and (B) fixed-frequency sliding mode ($R_o \times 20$).

35.3.5.2 Example 35.12: Constant-Frequency Sliding-Mode Control of *p* Pulse Parallel Rectifiers

This example presents a new paradigm to the control of thyristor rectifiers. Since p pulse rectifiers are variable-structure systems, sliding-mode control is applied here to 12-pulse rectifiers, still useful for very high-power applications [3]. The design determines the variables to be measured, and the controlled rectifier presents robustness and much shorter response times, even with the parameter uncertainty, perturbations, noise, and nonmodeled dynamics. These performances are not feasible using linear controllers, obtained here for comparison purposes.

Modeling the 12-pulse parallel rectifier

The 12-pulse rectifier (Fig. 35.35A) is built with four three-phase half-wave rectifiers, connected in parallel with current-sharing inductances l and l' merged with capacitors C' and C_2, to obtain a second-order LC filter. This allows low-ripple output voltage and continuous mode of operation (laboratory model with $l=44$ mH, $l'=13$ mH, $C'=C_2=10$ mF, star-delta-connected ac sources with $E_{RMS}\approx 65$ V, and power rating 2.2 kW, load approximately resistive $R_o\approx 3$–5 Ω).

To control the output voltage v_{c2}, given the complexity of the whole system, the best approach is to derive a low-order model. By averaging the four half-wave rectifiers, neglecting the rectifier

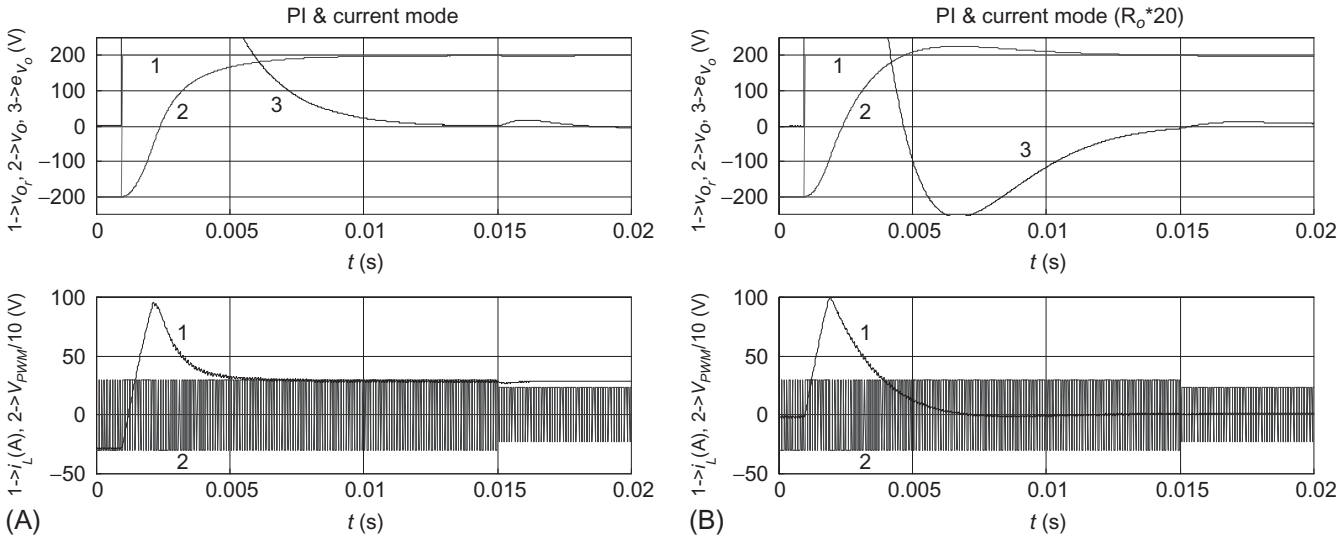


FIG. 35.34 Performance of the PI-controlled power operational amplifier; response to a v_{o_r} step from −200 to 200 V at $t=0.001$ s and to a V_{DC} step from 300 to 230 V at $t=0.015$ s: (A) PI current-mode controller (nominal load) and (B) PI current-mode controller ($R_o \times 20$).

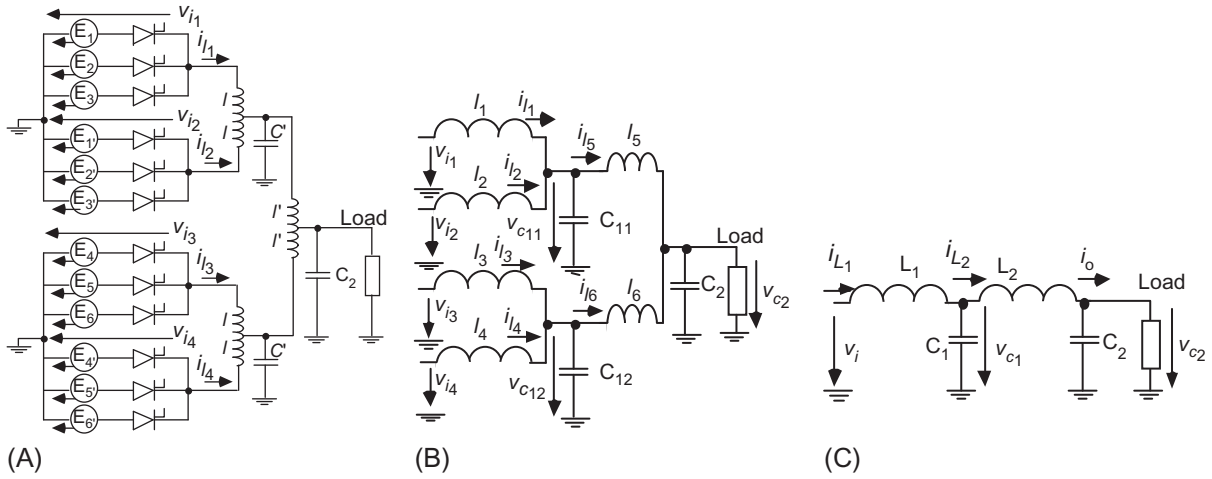


FIG. 35.35 (A) Twelve-pulse rectifier with interphase reactors and intermediate capacitors, (B) rectifier model neglecting the half-wave rectifier dynamics, and (C) low-order averaged equivalent circuit for the 12-pulse rectifier with the resulting output double LC filter.

dynamics and mutual couplings, the equivalent circuit of Fig. 35.35B is obtained ($l_1=l_2=l_3=l_4=l$, $l_5=l_6=l'$, and $C_{11}=C_{12}=C'$). Since the rectifiers are identical, the equivalent 12-pulse rectifier model of Fig. 35.35C is derived, simplifying the resulting parallel associations ($L_1=l/4$, $L_2=l/2$, and $C_1=2C'$).

Considering the load current i_o as an external perturbation and v_i the control input, the state-space model of the equivalent circuit of Fig. 35.35C is

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{L_1} \\ i_{L2} \\ v_{c_1} \\ v_{c_2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -1/L_1 & 0 \\ 0 & 0 & 1/L_2 & -1/L_2 \\ 1/C_1 & -1/C_1 & 0 & 0 \\ 0 & 1/C_2 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{L_1} \\ i_{L2} \\ v_{c_1} \\ v_{c_2} \end{bmatrix} + \begin{bmatrix} 1/L_1 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & -1/C_2 \end{bmatrix} \begin{bmatrix} v_i \\ i_o \end{bmatrix} \tag{35.117}$$

Sliding-mode control of the 12-pulse parallel rectifier

Since the output voltage v_{c_2} of the system must follow the reference $v_{c_{2r}}$, the system equations in the phase canonical (or controllability) form must be written, using the error $e_{v_2}=v_{c_{2r}}-v_{c_2}$ and its time derivatives as new state error variables, as done in Example 35.11:

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} e_{v_{c_2}} \\ e_\theta \\ e_\gamma \\ e_\beta \end{bmatrix} = \begin{bmatrix} e_\theta \\ e_\gamma \\ e_\beta \\ -\left(\dfrac{1}{C_1L_1}+\dfrac{1}{C_1L_2}+\dfrac{1}{C_2L_2}\right)e_\gamma - \dfrac{e_{v_{c_2}}}{C_1L_1C_2L_2} - \left(\dfrac{1}{C_1L_1C_2}+\dfrac{1}{C_1C_2L_2}\right)\dfrac{\mathrm{d}i_o}{\mathrm{d}t} - \dfrac{1}{C_2}\dfrac{\mathrm{d}^3 i_o}{\mathrm{d}t^3} - \dfrac{v_i}{C_1L_1C_2L_2} \end{bmatrix} \tag{35.118}$$

The sliding surface $S(e_{x_i}, t)$, designed to reduce the system order, is a linear combination of all the phase canonical state variables. Considering Eqs. (35.118) and (35.117) and the

errors $e_{v_{c_2}}$, e_θ, e_γ, and e_β, the sliding surface can be expressed as a combination of the rectifier currents, voltages, and their time derivatives:

$$\begin{aligned} S(e_{x_i}t) &= e_{v_{c_2}} + k_\theta e_\theta + k_\gamma e_\gamma + k_\beta e_\beta \\ &= v_{c_{2r}} + k_\theta\theta_r + k_\gamma\gamma_r + k_\beta\beta_r - \left(1 - \frac{k_\gamma}{C_2L_2}\right)v_{c_2} \\ &\quad - \frac{k_\gamma}{C_2L_2}v_{c_1} + \left(\frac{k_\theta}{C_2} - \frac{k_\beta}{C_2^2L_2}\right)i_o + \frac{k_\gamma}{C_2}\frac{\mathrm{d}i_o}{\mathrm{d}t} + \frac{k_\beta}{C_2}\frac{\mathrm{d}^2i_o}{\mathrm{d}t^2} \\ &\quad - \frac{k_\beta}{C_1C_2L_2}i_{L_1} - \left(\frac{k_\theta}{C_2} - \frac{k_\beta}{C_1C_2L_2} - \frac{k_\beta}{C_2^2L_2}\right)i_{L_2} = 0 \end{aligned} \tag{35.119}$$

Eq. (35.119) shows the variables to be measured ($v_{c_2}, v_{c_1}, i_o, i_{L_1}$, and i_{L_2}). Therefore, it can be concluded that the output current of each three-phase half-wave rectifier must be measured.

The existence of the sliding mode implies $S(e_{x_i}, t) = 0$ and $\dot{S}(e_{x_i}, t) = 0$. Given the state models (35.117) and (35.118) and from $\dot{S}(e_{x_i}, t) = 0$, the available voltage of the power supply v_i must exceed the equivalent average dc input voltage V_{eq} (35.120), which should be applied at the filter input, in order that the system state slides along the sliding surface (35.119):

$$\begin{aligned} V_{eq} &= \frac{C_1L_1C_2L_2}{k_\beta}\left(\theta_r + k_\theta\gamma_r + k_\gamma\beta_r + k_\beta\dot{\beta}_r\right) + v_{c_2} - \frac{C_1L_1C_2L_2}{k_\beta} \\ &\quad \times \left(\theta + k_\gamma\beta\right) + \left(C_2L_2 + C_2L_1 + C_1L_1 - C_1L_1C_2L_2\frac{k_\theta}{k_\beta}\right)\gamma \\ &\quad + (L_1 + L_2)\frac{\mathrm{d}i_o}{\mathrm{d}t} + C_1L_1L_2\frac{\mathrm{d}^3i_o}{\mathrm{d}t^3} \end{aligned} \tag{35.120}$$

This means that the power supply root mean square (RMS) voltage values should be chosen high enough to account for the maximum effects of the perturbations. This is almost the same criterion adopted when calculating the RMS voltage values needed with linear controllers. However, as the V_{eq} voltage contains the derivatives of the reference voltage, the system will not be able to stay in sliding mode with a step as the reference.

The switching law would be derived, considering that, from Eq. (35.97), $b_e(\mathbf{e}) > 0$. Therefore, from Eq. (35.119), if $S(e_{x_i}, t) > +\varepsilon$, then $v_i(t) = V_{eq_{max}}$, else if $S(e_{x_i}, t) < -\varepsilon$, then $v_i(t) = -V_{eq_{max}}$. However, because of the lack of gate turn-off capability of the rectifier thyristors, power rectifiers cannot generate the high-frequency switching voltage $v_i(t)$, since the statistical mean delay time is $T/2p$ ($T = 20$ ms) and reaches $T/2$ when switching from $+V_{eq_{max}}$ to $-V_{eq_{max}}$. To control mains switched rectifiers, the described constant-frequency sliding-mode operation method is used, in which the sliding surface $S(e_{x_i}, t)$ instead of being compared with zero is compared with an auxiliary constant-frequency function $r(t)$ (Fig. 35.6B) synchronized with the mains frequency. The new switching law is

$$\left.\begin{array}{l} \text{if } k_pS(e_{x_i}, t) > r(t) + \iota \Rightarrow \text{Trigger the next thyristor} \\ \text{if } k_pS(e_{x_i}, t) < r(t) - \iota \Rightarrow \text{Do not trigger any thyristor} \end{array}\right\} \Rightarrow v_i(t) \tag{35.121}$$

Since now $S(e_{x_i}, t)$ is not near zero, but around some value of $r(t)$, a steady-state error $e_{v_{c_{2av}}}$ appears $\left(\min[r(t)]/k_p < e_{v_{c_{2av}}} < \max[r(t)]/k_p\right)$, as seen in Example 35.11. Increasing the value of k_p (toward the ideal saturation control) does not overcome this drawback, since oscillations would appear even for moderate k_p gains, because of the rectifier dynamics. Instead, the sliding surface (35.122), based on Eq. (35.99), should be used. It contains an integral term, which, given the canonical controllability form and the Routh-Hurwitz property, is the only nonzero term at steady state, enabling the complete elimination of the steady-state error:

$$S_i(e_{x_i}, t) = \int e_{v_{c_2}}dt + k_{1v}e_{v_{c_2}} + k_{1\theta}e_\theta + k_{1\gamma}e_\gamma + k_{1\beta}e_\beta \tag{35.122}$$

To determine the k constants of Eq. (35.122), a pole-placement technique is selected, according to a fourth-order Bessel polynomial $B_E(s)_m$, $m = 4$, from Eq. (35.88), in order to obtain the smallest possible response time with almost no overshoot. For a delay characteristic as flat as possible, the delay t_r is taken inversely proportional to a frequency f_{ci} just below the lowest cutoff frequency ($f_{ci} < 8.44$ Hz) of the double LC filter. For this fourth-order filter, the delay is $t_r = 2.8/(2\pi f_{ci})$. By choosing $f_{ci} = 7$ Hz ($t_r \approx 64$ ms) and dividing all the Bessel polynomial terms by st_r, the characteristic polynomial (35.123) is obtained:

$$S_i(e_{x_i}, s) = \frac{1}{st_r} + 1 + \frac{45}{105}st_r + \frac{10}{105}s^2t_r^2 + \frac{1}{105}s^3t_r^3 \tag{35.123}$$

This polynomial must be applied to Eq. (35.122) to obtain the four sliding functions needed to derive the thyristor trigger pulses of the four three-phase half-wave rectifiers. These sliding functions will enable the control of the output current ($i_{l_1}, i_{l_2}, i_{l_3}$ and i_{l_4}) of each half-wave rectifier, improving the current sharing among them (Fig. 35.35B). Supposing equal current share, the relation between the i_{L_1} current and the output currents of each three-phase rectifier is $i_{L_1} = 4i_{l_1} = 4i_{l_2} = 4i_{l_3} = 4i_{l_4}$. Therefore, for the nth half-wave three-phase rectifier, since, for $n = 1$ and $n = 2$, $v_{c_1} = v_{c_{11}}$ and $i_{L_2} = 2i_{l_5}$ and, for $n = 3$ and $n = 4$, $v_{c_1} = v_{c_{12}}$ and $i_{L_2} = 2i_{l_6}$, the four sliding surfaces are ($k_{1v} = 1$)

$$S_i(e_{x_i}t)_n = \Bigg[k_{1v}v_{c_{2r}} + \frac{45t_r}{105}\theta_r + \frac{10t_r^2}{105}\gamma_r + \frac{t_r^3}{105}\beta_r + \frac{1}{t_r}\int (v_{c_{2r}} - v_{c_2})dt - \left(\frac{k_{1v}}{C_2L_2} - \frac{10t_r^2}{105C_2L_2}\right)v_{c_2} - \frac{10t_r^2}{105C_2L_2}v_{c_{1,2}} + \left(\frac{45t_r}{105C_2} - \frac{t_r^3}{105C_2^2L_2}\right)i_o + \left(\frac{10t_r^2}{105C_2}\right)\frac{di_o}{dt} + \left(\frac{t_r^3}{105C_2}\right)\frac{d^2i_o}{dt^2}\Bigg]/4 - \left[\left(\frac{45t_r}{105C_2} - \frac{t_r^3}{105C_2^2L_2} - \frac{t_r^3}{105C_1L_2C_2}\right)i_{l_{5,6}}\right]/2 - \left(\frac{t_r^3}{105C_1L_2C_2}\right)i_{l_n} \tag{35.124}$$

If an inexpensive analog controller is desired, the successive time derivatives of the reference voltage and the output current of Eq. (35.124) can be neglected (furthermore, their calculation is noise prone). Nonzero errors on the first-, second-, and third-order derivatives of the controlled variable will appear, worsening the response speed. However, the steady-state error is not affected.

To implement the four equations (35.124), the variables $v_{c_2}, v_{c11}, v_{c12}, i_o, i_{l_5}, i_{l_6}, i_{l_1}, i_{l_2}, i_{l_3}$ and i_{l_4} must be measured. Although this could be done easily, it is very convenient to further simplify the practical controller, keeping its complexity and cost at the level of linear controllers, while maintaining the advantages of sliding mode. Therefore, the voltages $v_{c_{11}}$ and $v_{c_{12}}$ are assumed almost constant over one period of the filter input current, and $v_{c_{11}} = v_{c_{12}} = v_{c_2}$, meaning that $i_{l_5} = i_{l_6} = i_o/2$. With these assumptions, valid as the values of C' and C_2 are designed to provide an output voltage with very low ripple, the new sliding-mode functions are

$$S_i(e_{x_i}t)_n \approx \frac{\frac{1}{t_r}\int (v_{c2r} - v_{c2})dt + k_{1v}(v_{c_{2r}} - v_{c_2}) + \frac{t_r^3}{105}\frac{1}{C_1C_2L_2}i_o}{4} - \left(\frac{t_r^3}{105C_1L_2C_2}\right)i_{ln} \tag{35.125}$$

These approximations disregard only the high-frequency content of v_{c11}, v_{c12}, i_{l_5}, and i_{l_6} and do not affect the rectifier steady-state response, but the step response will be a little slower, although still much faster (150 ms, Fig. 35.39) than that obtained with linear controllers (280 ms, Fig. 35.38). Regardless of all the approximations, the low switching frequency of the rectifier would not allow the elimination of the dynamic errors. As a benefit of these approximations, the sliding-mode controller (Fig. 35.36A) will need only an extra current sensor (or a current observer) and an extra operational amplifier in comparison with linear controllers derived hereafter (which need four current sensors and six operational amplifiers). Compared with the total cost of the 12-pulse rectifier plus output filter, the control hardware cost is negligible in both cases, even for medium-power applications.

Average current-mode control of the 12-pulse rectifier

For comparison purposes, a PI-based controller structure is designed (Fig. 35.36B), taking into account that small mismatches of the line voltages or of the trigger angles can completely destroy the current share of the four paralleled rectifiers, in spite of the current equalizing inductances (l and l'). Output voltage control sensing only the output voltage is, therefore, not feasible. Instead, the slow and fast manifold approach is selected. For the fast manifold, four internal current control loops guarantee the same dc current level in each three-phase rectifier and limit the short-circuit currents. For

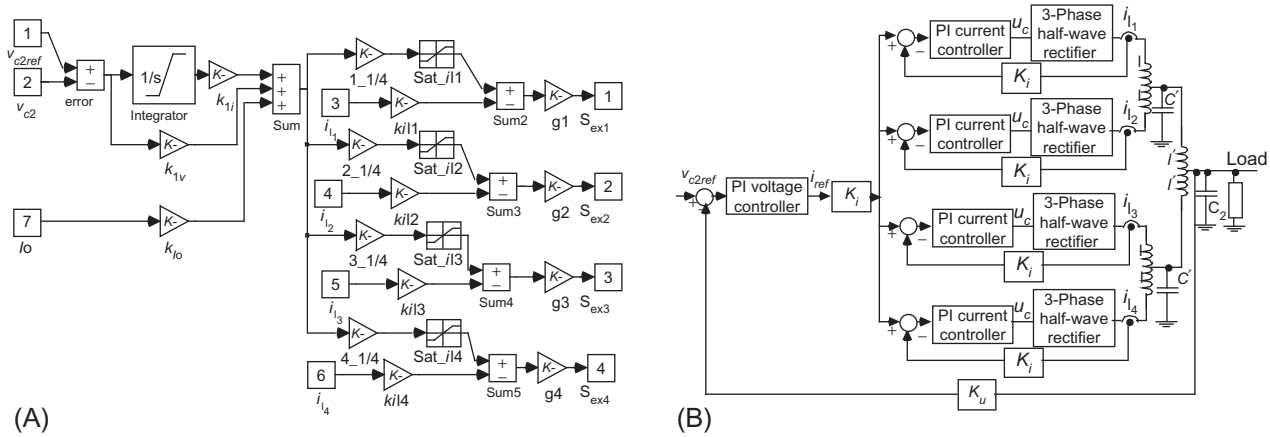


FIG. 35.36 (A) Sliding-mode controller block diagram and (B) linear control hierarchy for the 12-pulse rectifier.

the output slow dynamics, an external cascaded output voltage control loop (Fig. 35.36B), measuring the voltage applied to the load, is the minimum.

For a straightforward design, given the much slower dynamics of the capacitor voltages compared with the input current, the PI current controllers are calculated as shown in Example 35.6, considering the capacitor voltage constant during a switching period and $r_t \approx 1\ \Omega$ the intrinsic resistance of the transformer windings, thyristor overlap, and inductor l. From Eq. (35.59), $T_z = l/r_t \approx 0.044$ s. From Eq. (35.62), with the common assumptions, $T_p \approx 0.16\, k_I$ s ($p=3$). These values guarantee a small overshoot ($\approx 5\%$) and a current rise time of approximately $T/3$.

To design the external output voltage control loop, each current-controlled rectifier can be considered a voltage-controlled current source $i_{L_1}(s)/4$, since each half-wave rectifier current response will be much faster than the filter output voltage response. Therefore, in the equivalent circuit of Fig. 35.35B, the current source $i_{L_1}(s)$ substitutes the input inductor, yielding the transfer function $v_{c_2}(s)/i_{L_1}(s)$:

$$\frac{V_{c_2}(s)}{i_{L_1}(s)} = \frac{R_o}{C_2C_1L_2R_os^3 + C_1L_2s^2 + (C_2R_o + C_1R_o)s + 1} \tag{35.126}$$

Given the real pole ($p_1 = -6.7$) and two complex poles ($p_{2,3} = -6.65 \pm j140.9$) of Eq. (35.126), the PI voltage controller zero ($1/T_{zv} = p_1$) can be chosen with a value equal to the transfer function real pole. The integral gain T_{pv} can be determined using a root-locus analysis to determine the maximum gain that still guarantees the stability of the closed-loop controlled system. The critical gain for the PI was found to be $T_{zv}/T_{pv} \approx 0.4$ and then $T_{pv} > 0.37$. The value $T_{pv} \approx 2$ was selected to obtain weak oscillations, together with almost no overshoot.

The dynamic and steady-state responses of the output currents of the four rectifiers ($i_{l_1}, i_{l_2}, i_{l_3}, i_{l_4}$) and the output voltage V_{c_2} were analyzed using a step input from 2 to 2.5 A applied at $t = 1.1$ s, for the currents, and from 40 to 50 V for the V_{c_2} voltage. The PI current controllers (Fig. 35.37) show good sharing of the total current, slight overshoot ($\zeta = 0.7$), and response time 6.6 ms (T/p).

The open-loop voltage V_{c_2} presents a rise time of 0.38 s. The PI voltage controller (Fig. 35.38) shows a response time of 0.4 s,

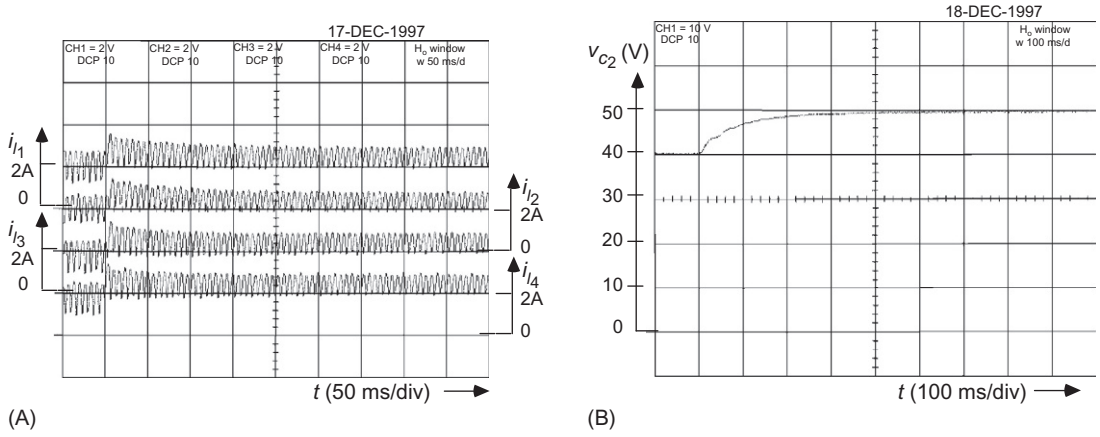


FIG. 35.37 PI current controller performance: (A) $i_{l_1}, i_{l_2}, i_{l_3}, i_{l_4}$ closed-loop currents and (B) open-loop output voltage V_{c_2}.

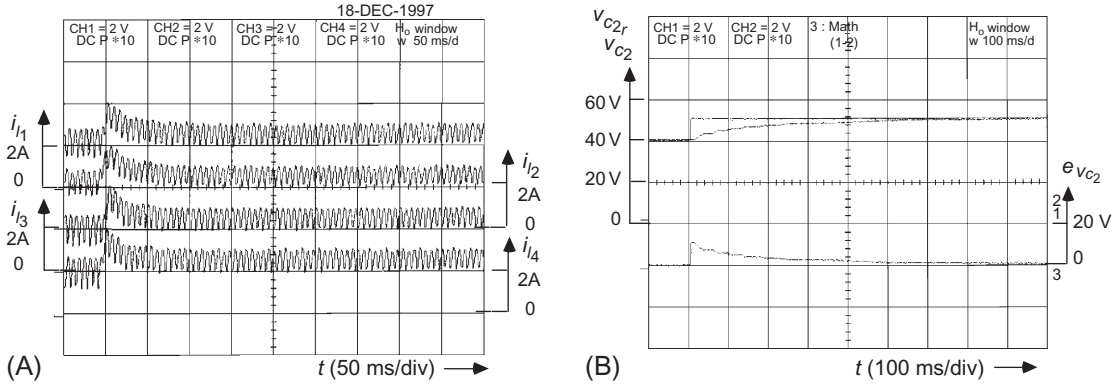


FIG. 35.38 PI voltage controller performance: (A) $i_{l_1}, i_{l_2}, i_{l_3}, i_{l_4}$ closed-loop currents and (B) closed output voltage V_{c_2} and $l_{v_{c_2}}$ output voltage error.

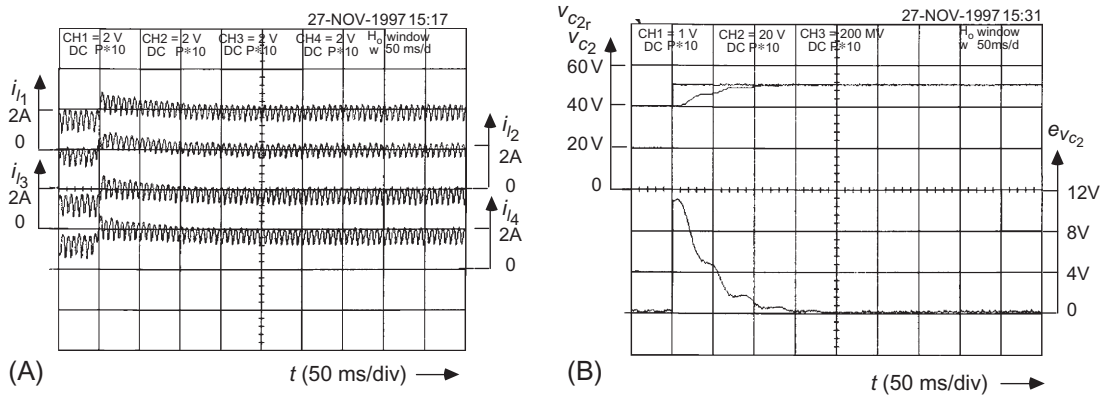


FIG. 35.39 Closed-loop constant-frequency sliding-mode controller performance: (A) $i_{l_1}, i_{l_2}, i_{l_3}, i_{l_4}$ closed-loop currents and (B) closed output voltage V_{c_2} and $e_{v_{c_2}}$ output voltage error.

no overshoot. The four three-phase half-wave rectifier output currents $(i_{l_1}, i_{l_2}, i_{l_3}, \text{and } i_{l_4})$ present nearly the same transient and steady-state values, with no very high current peaks. These results validate the assumptions made in the PI design.

The closed-loop performance of the fixed-frequency sliding-mode controller (Fig. 35.39) shows that all the $i_{l_1}, i_{l_2}, i_{l_3}, \text{and } i_{l_4}$ currents are almost equal and have peak values only slightly higher than those obtained with the PI linear controllers. The output voltage presents a much faster response time (150 ms) than the PI linear controllers, negligible or no steady-state error, and no overshoot. From these waveforms, it can be concluded that the sliding-mode controller provides a much more effective control of the rectifier, as the output voltage response time is much lower than the obtained with PI linear controllers, without significantly increasing the thyristor currents, overshoots, or costs. Furthermore, sliding mode is an elegant way to know the variables to be measured and to design all the controller and the modulator electronics.

35.3.5.3 Example 35.13: Sliding-Mode Control of Pulse Width Modulation Audio Power Amplifiers

Linear audio power amplifiers can be astonishing but have efficiencies as low as 15%–20% with speech or music signals. To improve the efficiency of audio systems while preserving the quality, PWM switching power amplifiers, enabling the reduction of the power supply cost, volume, and weight and compensating the efficiency loss of modern loudspeakers, are needed. Moreover, PWM amplifiers can provide a complete digital solution for audio power processing.

For high-fidelity systems, PWM audio amplifiers must present flat passbands of at least 16–20 kHz (±0.5 dB), distortions less than 0.1% at the rated output power, fast dynamic response, and signal-to-noise ratios above 90 dB. This requires fast power semiconductors (usually metal-oxide-semiconductor field-effect transistor (MOSFET) transistors), capable of switching at frequencies near 500 kHz, and fast nonlinear controllers to provide the precise and timely control actions needed to accomplish the mentioned requirements and to eliminate the phase delays in the LC output filter and loudspeakers.

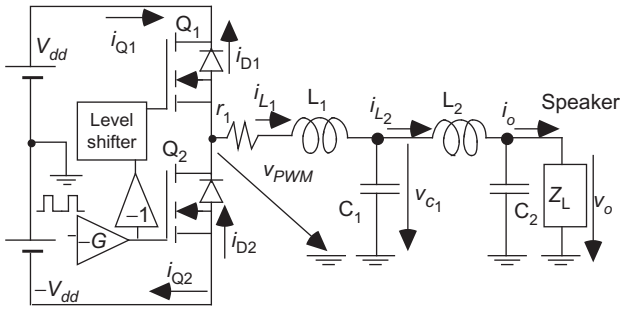


FIG. 35.40 PWM audio amplifier with fourth-order Chebyshev low-pass output filter and loudspeaker load.

A low-cost PWM audio power amplifier, able to provide over 80 W to 8 Ω loads (V_{dd} = 50 V), can be obtained using a half-bridge power inverter (switching at $f_{PWM} \approx 450$ kHz), coupled to an output filter for high-frequency attenuation (Fig. 35.40). A low-sensitivity, doubly terminated passive ladder (double LC), low-pass filter using fourth-order Chebyshev approximation polynomials is selected, given its ability to meet, while minimizing the number of inductors, the following requirements: passband edge frequency 21 kHz, passband ripple 0.5 dB, stopband edge frequency 300 kHz, and 90 dB minimum attenuation in the stopband ($L_1 = 80$ μH, $L_2 = 85$ μH, $C_1 = 1.7$ μF, $C_2 = 820$ nF, $R_2 = 8$ Ω, and $r_1 = 0.47$ Ω).

Modeling the PWM audio amplifier

The two half-bridge switches must always be in complementary states, to avoid power supply internal short circuits. Their state can be represented by the time-dependent variable γ, which is $\gamma = 1$ when Q1 is on and Q2 is off, and is $\gamma = -1$ when Q1 is off and Q2 is on.

Neglecting switch delays, on-state semiconductor voltage drops, and auxiliary networks and supposing small dead times, the half-bridge output voltage (v_{PWM}) is $v_{PWM}=\gamma V_{dd}$. Considering the state variables and circuit components of Fig. 35.40 and modeling the loudspeaker load as a disturbance represented by the current i_o (ensuring robustness to the frequency -dependent impedance of the speaker), the switched state-space model of the PWM audio amplifier is

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{L_1} \\ v_{c_1} \\ i_{L_2} \\ v_o \end{bmatrix} = \begin{bmatrix} -r_1/L_1 & -1/L_1 & 0 & 0 \\ 1/C_1 & 0 & -1/C_1 & 0 \\ 0 & 1/L_2 & 0 & -1/L_2 \\ 0 & 0 & 1/C_2 & 0 \end{bmatrix}\begin{bmatrix} i_{L_1} \\ v_{c_1} \\ i_{L_2} \\ v_o \end{bmatrix} + \begin{bmatrix} 1/L_1 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & -1/C_2 \end{bmatrix}\begin{bmatrix} \gamma V_{dd} \\ i_o \end{bmatrix} \tag{35.127}$$

This model will be used to define the output voltage v_o controller.

Sliding-mode control of the PWM audio amplifier

The filter output voltage v_o, divided by the amplifier gain ($1/k_v$), must follow a reference v_{o_r}. Defining the output error as $e_{v_o}=v_{o_r}-k_v v_o$ and also using its time derivatives (e_θ, e_γ, and e_β) as a new state vector $\mathbf{e}=\left[e_{v_o}, e_\theta, e_\gamma, e_\beta\right]^{\mathrm{T}}$, the system equations, in the phase canonical (or controllability) form, can be written in the form

$$\frac{\mathrm{d}}{\mathrm{d}t}\left[e_{v_o}, e_\theta, e_\gamma, e_\beta\right]^{\mathrm{T}} = \left[e_\theta, e_\gamma, e_\beta - f\left(e_{v_o}, e_\theta, e_\gamma, e_\beta\right) + p_e(t) - \gamma V_{dd}/C_1L_1C_2L_2\right]^{\mathrm{T}} \tag{35.128}$$

Sliding-mode control of the output voltage will enable a robust and reduced-order dynamics, independent of semiconductors, power supply, filter, and load parameters. According to Eqs. (35.91) and (35.128), the sliding surface is

$$\begin{aligned} S\left(e_{v_o}, e_\theta, e_\gamma, e_\beta, t\right) &= e_{v_o} + k_\theta e_\theta + k_\gamma e_\gamma + k_\beta e_\beta \\ &= v_{o_r} - k_v v_o + k_\theta \frac{\mathrm{d}(v_{o_r} - k_v v_o)}{\mathrm{d}t} \\ &\quad + k_\gamma \frac{\mathrm{d}}{\mathrm{d}t}\left(\frac{\mathrm{d}(v_{o_r} - k_v v_o)}{\mathrm{d}t}\right) \\ &\quad + k_\beta \frac{\mathrm{d}}{\mathrm{d}t}\left[\frac{\mathrm{d}}{\mathrm{d}t}\left(\frac{\mathrm{d}(v_{o_r} - k_v v_o)}{\mathrm{d}t}\right)\right] = 0 \end{aligned} \tag{35.129}$$

In sliding mode, Eq. (35.129) confirms the amplifier gain ($v_o/v_{o_r}=1/kv$). To obtain a stable system and the smallest possible response time t_r, a pole placement according to a third-order Bessel polynomial is used. Taking t_r inversely proportional to a frequency just below the lowest cutoff frequency (ω_1) of the double LC filter ($t_r \approx 2.8/\omega_1 \approx 2.8/(2\pi \times 21\ \mathrm{kHz}) \approx 20\ \mu\mathrm{s}$) and using Eq. (35.88) with $m=3$, the characteristic polynomial Eq. (35.130), verifying the Routh-Hurwitz criterion, is obtained:

$$S(\mathbf{e}, s) = 1 + st_r + \frac{6}{15}(st_r)^2 + \frac{1}{15}(st_r)^3 \tag{35.130}$$

From Eq. (35.97), the switching law for the control input at time t_k, $\gamma(t_k)$, must be

$$\gamma(t_k) = \mathrm{sgn}\{S(\mathrm{e}, t_k) + \varepsilon\,\mathrm{sgn}[S(\mathrm{e}, t_{k-1})]\} \tag{35.131}$$

To ensure reaching and existence conditions, the power supply voltage V_{dd} must be greater than the maximum required mean value of the output voltage in a switching period $V_{dd} > (\overline{v_{PWMmax}})$. The sliding-mode controller (Fig. 35.41) is obtained from Eqs. (35.129)–(35.131) with $k_\theta = t_r$, $k_\gamma = 6t_r^2/15$, $k_\beta = t_r^3/15$. The derivatives can be approximated by the block diagram of Fig. 35.41B, where h is the oversampling period.

Fig. 35.42A shows the v_{PWM}, v_{o_r}, $v_o/10$, and error $10\times(v_{o_r}-v_o/10)$ waveforms for a 20 kHz sine input. The overall behavior is much better than the obtained with the sigma-delta controllers (Figs. 35.43 and 35.44) explained below for comparison purposes. There is no 0.5 dB loss or phase delay over the entire audio band; the Chebyshev filter behaves as a maximally flat filter, with higher stopband attenuation. Fig. 35.42B shows v_{PWM}, v_{o_r}, and $10\times(v_{o_r}-v_o/10)$ with a

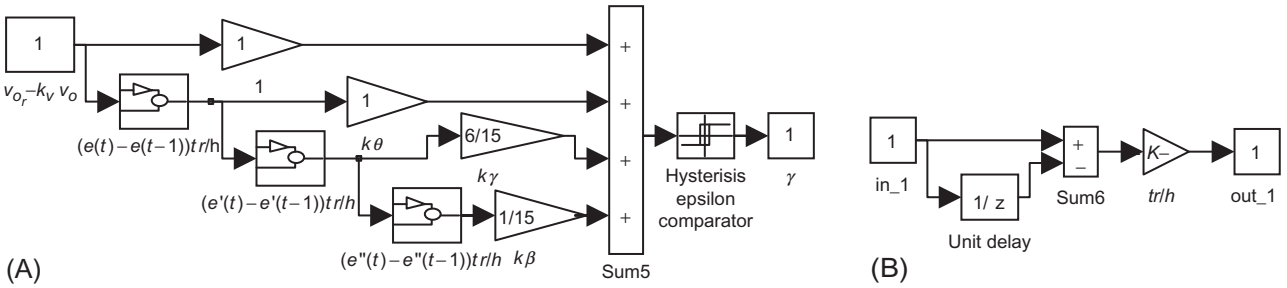


FIG. 35.41 (A) Sliding-mode controller for the PWM audio amplifier and (B) implementation of the derivative blocks.

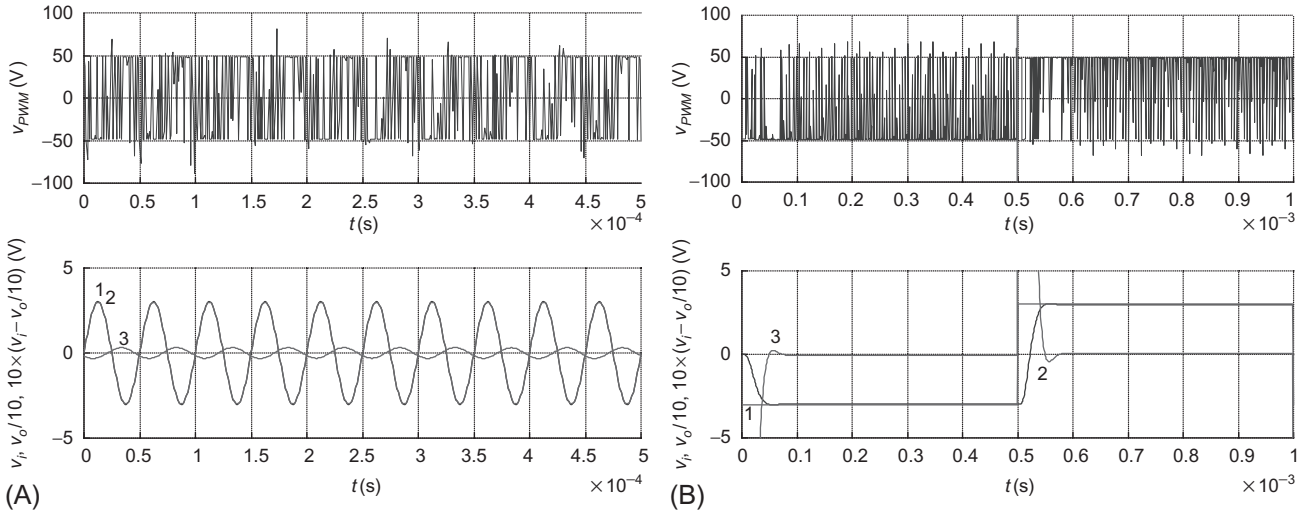


FIG. 35.42 Sliding-mode-controlled audio power amplifier performance (upper graphs show v_{PWM}, lower graphs trace 1 show $v_{o_r}(v_{o_r} \equiv v_i)$, lower graphs trace 2 show $v_o/10$, and lower graphs trace 3 show $10 \times (v_{o_r} - v_o/10)$): (A) response to a 20 kHz sine input, at 55 W output power, and (B) response to 1 kHz square wave input, at 100 W output power.

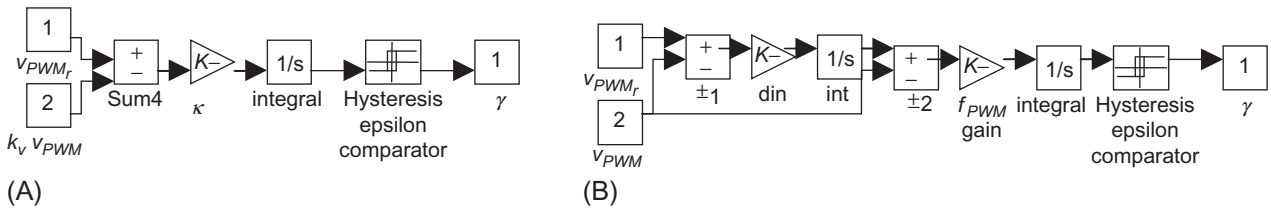


FIG. 35.43 (A) First-order sigma-delta modulator and (B) second-order sigma-delta modulator.

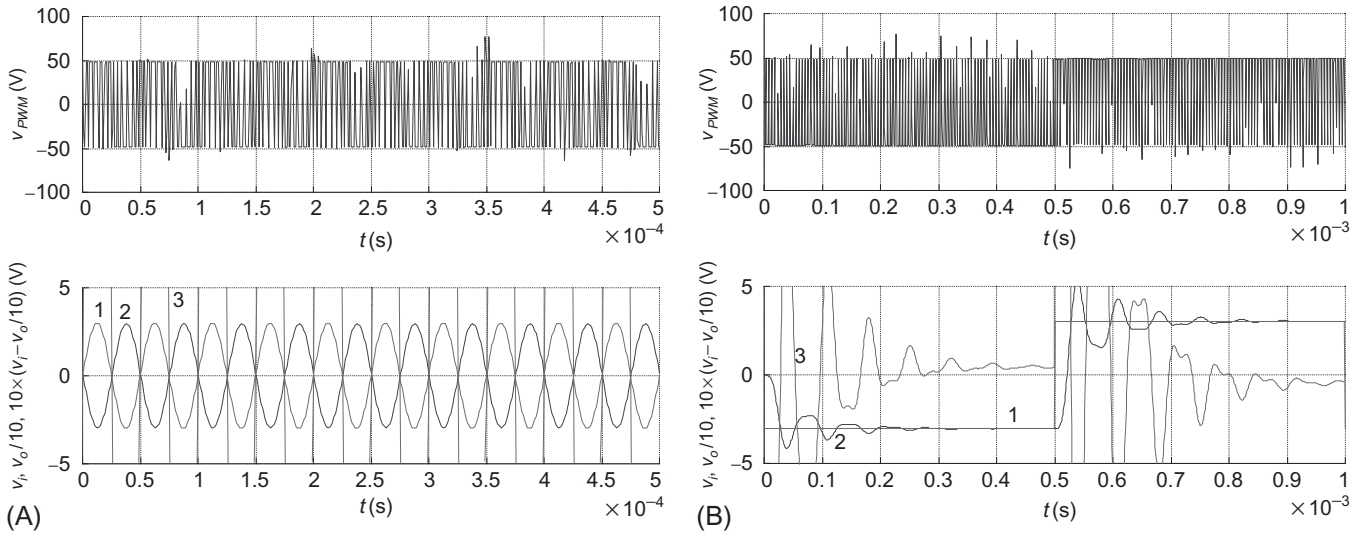


FIG. 35.44 First-order sigma-delta audio amplifier performance (upper graphs show v_{PWM}, lower graphs trace 1 show $v_{o_r}(v_{o_r} \equiv v_i)$, lower graphs trace 2 shows $v_o/10$, and lower graphs trace 3 show $10 \times (v_{o_r} - v_o/10)$): (A) response to a 20 kHz sine input, at 55 W output power, and (B) response to 1 kHz square wave input, at 100 W output power.

1 kHz square input. There is almost no steady-state error and almost no overshoot on the speaker voltage v_o, attesting to the speed of response ($t \approx 20$ μs as designed, since, in contrast to Example 35.12, no derivatives were neglected). The stability, the system order reduction, and the sliding-mode controller usefulness for the PWM audio amplifier are also shown.

Sigma delta controlled PWM audio amplifier

Assume now the fourth-order Chebyshev low-pass filter, as an ideal filter removing the high-frequency content of the v_{PWM} voltage. Then, the v_{PWM} voltage can be considered as the amplifier output. However, the discontinuous voltage $v_{PWM} = \gamma V_{dd}$ is not a state variable and cannot follow the almost continuous reference v_{PWM_r}. The new error variable $e_{vPWM} = v_{PWM_r} - k_v \gamma V_{dd}$ is always far from the zero value. Given this nonzero error, the approach outlined in Section 35.3.4 can be used. The switching law remains Eq. (35.131), but the new control law Eq. (35.132) is

$$S(e_{vPVM}, t) = k \int (v_{PWM_r} - k_v \gamma V_{dd}) dt = 0 \qquad (35.132)$$

The κ parameter is calculated to impose the maximum switching frequency f_{PWM}. Since $\kappa \int_0^{1/2f_{PWM}} \left(v_{PWM_{r\,max}} + k_v V_{dd}\right) \mathrm{d}t = 2\varepsilon$, we obtain

$$f_{PWM} = \kappa (v_{PWM_{rmax}} + k_v V_{dd})/4\varepsilon \qquad (35.133)$$

Assuming that v_{PWM_r} is nearly constant over the switching period $1/f_{PWM}$, Eq. (35.132) confirms the amplifier gain, since $\overline{v_{PWM}} = v_{PWM_r}/k_v$.

Practical implementation of this control strategy can be done using an integrator with gain κ ($\kappa \approx 1800$) and a comparator with hysteresis ε ($\varepsilon \approx 6$ mV) (Fig. 35.43A). Such an arrangement is called a first-order sigma-delta ($\Sigma\Delta$) modulator.

Fig. 35.44A shows the v_{PWM}, v_{or}, and $v_o/10$ waveforms for a 20 kHz sine input. The overall behavior is as expected, because the practical filter and loudspeaker are not ideal, but notice the 0.5 dB loss and phase delay of the speaker voltage v_o, mainly due to the output filter and speaker inductance. In Fig. 35.44B, the v_{PWM}, v_{o_r}, $v_o/10$, and error $10 \times (v_{o_r} - v_o/10)$ for a 1 kHz square input are shown. Note the oscillations and steady-state error of the speaker voltage v_o, due to the filter dynamics and double termination.

A second-order sigma-delta modulator is a better compromise between circuit complexity and signal-to-quantization noise ratio. As the switching frequency of the two power MOSFET (Fig. 35.40) cannot be further increased, the second-order structure named "cascaded integrators with feedback" (Fig. 35.43B) was selected and designed to eliminate the step response overshoot found in Fig. 35.44B.

Fig. 35.45A, for 1 kHz square input, shows much less overshoot and oscillations than Fig. 35.44B. However, the v_{PWM}, v_{o_r}, and $v_o/10$ waveforms, for a 20 kHz sine input presented in Fig. 35.45B, show increased output voltage loss, compared to the first-order sigma-delta modulator, since the second-order modulator was designed to eliminate the v_o output voltage ringing (therefore reducing the amplifier bandwidth). The obtained performances with these and other sigma-delta structures are inferior to the sliding-mode performances (Fig. 35.42). Sliding mode brings definite advantages as the system order is reduced, flatter passbands are obtained, power supply rejection ratio is

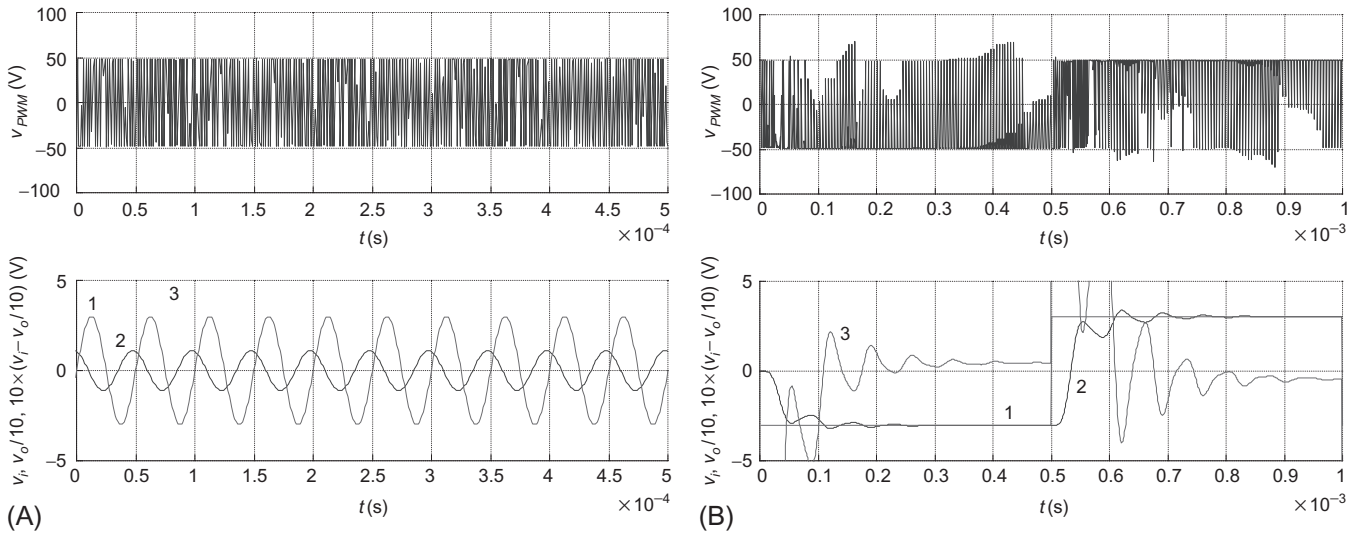


FIG. 35.45 Second-order sigma-delta audio amplifier performance (upper graphs show v_{PWM}, lower graphs trace 1 show $v_{o_r} \equiv v_i$, lower graphs trace 2 show $v_o/10$, and lower graphs trace 3 show $10 \times (v_{o_r} - v_o/10)$): (A) response to 1 kHz square wave input, at 100 W output power, and (B) response to a 20 kHz sine input, at 55 W output power.

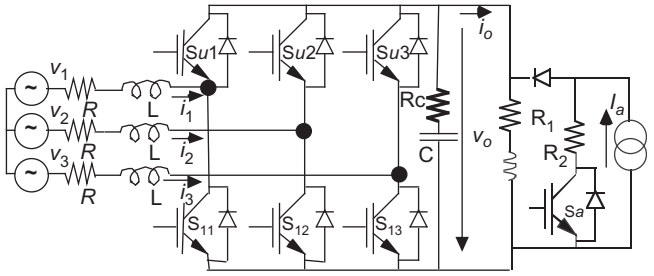


FIG. 35.46 Voltage-sourced three-phase PWM rectifier with IGBTs and test load.

increased, and the nonlinear effects, together with the frequency-dependent phase delays, are canceled out.

35.3.5.4 Example 35.14: Sliding-Mode Control of Near Unity Power Factor PWM Three Phase Rectifiers

Boost-type voltage-sourced three-phase rectifiers (Fig. 35.46) are multiple-input multiple-output (MIMO) systems capable of bidirectional power flow, near unity power factor operation, and almost sinusoidal input currents and can behave as ac/dc power supplies or power factor compensators.

The fast power semiconductors used (usually MOSFETs or IGBTs) can switch at frequencies much higher than the mains frequency, enabling the voltage controller to provide an output voltage with fast dynamic response.

Modeling the three phase PWM boost rectifier

Neglecting switch delays and dead times, the states of the switches of the kth inverter leg (Fig. 35.46) can be represented by the time-dependent nonlinear variables γ_k, defined as

$$\gamma_k = \begin{cases} 1 > \text{if } Su_k \text{ is on and } Sl_k \text{ is off} \\ 0 > \text{if } Su_k \text{ is off and } Sl_k \text{ is on} \end{cases} \tag{35.134}$$

Consider the displayed variables of the circuit (Fig. 35.46), where L is the value of the boost inductors, R their resistance, C the value of the output capacitor, and R_c its equivalent series resistance (ESR). Neglecting semiconductor voltage drops, leakage currents, and auxiliary networks, the application of Kirchhoff laws (taking the load current i_o as a time-dependent perturbation) yields the following switched state-space model of the boost rectifier:

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_o \end{bmatrix} = \begin{bmatrix} -R/L & 0 & 0 & (-2\gamma_1+\gamma_2+\gamma_3)/(3L) \\ 0 & -R/L & 0 & (-2\gamma_2+\gamma_3+\gamma_1)/(3L) \\ 0 & 0 & -R/L & (-2\gamma_3+\gamma_1+\gamma_2)/(3L) \\ A_{41} & A_{42} & A_{43} & A_{44} \end{bmatrix}\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_o \end{bmatrix} + \begin{bmatrix} 1/L & 0 & 0 & 0 & 0 \\ 0 & 1/L & 0 & 0 & 0 \\ 0 & 0 & 1/L & 0 & 0 \\ \gamma_1 R_c/L & \gamma_2 R_c/L & \gamma_3 R_c/L & -1/C & -R_c \end{bmatrix}\begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ i_o \\ \mathrm{d}i_o/\mathrm{d}t \end{bmatrix} \tag{35.135}$$

where $A_{41} = \gamma_1\left(\frac{1}{C} - \frac{RR_c}{L}\right)$, $A_{42} = \gamma_2\left(\frac{1}{C} - \frac{RR_c}{L}\right)$, $A_{43} = \gamma_3\left(\frac{1}{C} - \frac{RR_c}{L}\right)$, $A_{44} = \frac{-2R_c(\gamma_1(\gamma_1-\gamma_2)+\gamma_2(\gamma_2-\gamma_3)+\gamma_3(\gamma_3-\gamma_1))}{3L}$

Since the input voltage sources have no neutral connection, the preceding model can be simplified, eliminating one equation. Using the relationship (35.136) between the fixed frames x_1, 2, 3, and $x_{\alpha,\beta}$, in Eq. (35.135), the state-space model (35.137), in the α,β frame, is obtained:

$$\begin{bmatrix} x_1 \\ x_2 \end{bmatrix} = \begin{bmatrix} \sqrt{2/3} & 0 \\ -\sqrt{1/6} & \sqrt{1/2} \end{bmatrix}\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \tag{35.136}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_\alpha \\ i_\beta \\ v_o \end{bmatrix} = \begin{bmatrix} -R/L & \omega & -\gamma_\alpha/L \\ 0 & -R/L & -\gamma_\alpha/L \\ A^\alpha_{31} & A^\alpha_{32} & A^\alpha_{33} \end{bmatrix}\begin{bmatrix} i_\alpha \\ i_\beta \\ v_o \end{bmatrix} + \begin{bmatrix} 1/L & 0 & 0 & 0 \\ 0 & 1/L & 0 & 0 \\ \gamma_\alpha R_c/L & \gamma_\beta R_c/L & -1/C & -R_c \end{bmatrix}\begin{bmatrix} v_\alpha \\ v_\beta \\ i_o \\ \mathrm{d}i_o/\mathrm{d}t \end{bmatrix} \tag{35.137}$$

where $A^\alpha_{31} = \gamma_\alpha\left(\frac{1}{C} - \frac{RR_c}{L}\right)$, $A^\alpha_{32} = \gamma_\beta\left(\frac{1}{C} - \frac{RR_c}{L}\right)$, $A^\alpha_{33} = \frac{-R_c\left(\gamma_\alpha^2+\gamma_\beta^2\right)}{L}$

Sliding-mode control of the PWM rectifier

The model (35.137) is nonlinear and time-variant. Applying the Park transformation (35.138), using a frequency ω rotating reference frame synchronized with the mains (with the q component of the supply voltages equal to zero), the nonlinear, time-invariant model (35.139) is written as

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & -\sin(\omega t) \\ \sin(\omega t) & \cos(\omega t) \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{35.138}$$

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ v_o \end{bmatrix} = \begin{bmatrix} -R/L & \omega & -\gamma_d/L \\ -\omega & -R/L & -\gamma_q/L \\ A^d_{31} & A^d_{32} & A^d_{33} \end{bmatrix}\begin{bmatrix} i_d \\ i_q \\ v_o \end{bmatrix} + \begin{bmatrix} 1/L & 0 & 0 & 0 \\ 0 & 1/L & 0 & 0 \\ \gamma_d R_c/L & \gamma_q R_c/L & -1/C & -R_c \end{bmatrix}\begin{bmatrix} v_d \\ v_q \\ i_o \\ di_o dt \end{bmatrix} \tag{35.139}$$

where $A^d_{31} = \gamma_d\left(\frac{1}{C} - \frac{RR_c}{L}\right)$, $A^d_{32} = \gamma_q\left(\frac{1}{C} - \frac{RR_c}{L}\right)$, $A^d_{33} = \frac{-R_c\left(\gamma_d^2+\gamma_q^2\right)}{L}$

This state-space model can be used to obtain the feedback controllers for the PWM boost rectifier. Considering the output voltage v_o and the i_q current as the controlled outputs and γ_d and γ_q the control inputs (MIMO system), the input-output linearization of Eq. (35.72) gives the state-space equations in the controllability canonical form (35.140):

$$\frac{di_q}{dt} = -\omega i_d - \frac{R}{L} i_q - \frac{\gamma_q}{L} v_o + \frac{1}{L} v_q$$

$$\frac{dv_o}{dt} = \theta$$

$$\frac{d\theta}{dt} = \frac{R + R_c\left(\gamma_d^2 + \gamma_q^2\right)}{L}\theta - \frac{\gamma_d^2 + \gamma_q^2}{LC} v_o + \frac{\gamma_d v_d + \gamma_q v_q}{LC} - \frac{R i_o}{LC} - \left(\frac{1}{C} + \frac{RR_c}{L}\right)\frac{di_o}{dt} + \omega\left(\frac{1}{C} - \frac{RR_c}{L}\right)\left(\gamma_d i_q - \gamma_d i_q\right) - R_c \frac{d^2 i_o}{dt^2} \tag{35.140}$$

where

$$\theta = \left(\frac{1}{C} - \frac{RR_c}{L}\right)\left(\gamma_d i_d + \gamma_q i_q\right) - \frac{R_c\left(\gamma_d^2 + \gamma_q^2\right)}{L} v_o + \frac{R_c}{L}\left(\gamma_d v_d + \gamma_q v_q\right) - \frac{i_o}{C} - R_c \frac{di_o}{dt}$$

Using the rectifier overall power balance (from Tellegen's theorem, the converter is conservative, i.e., the power delivered to the load or dissipated in the converter intrinsic devices equals the input power) and neglecting the switching and output capacitor losses, $v_d i_d + v_q i_q = v_o i_o + R i_d^2$. Supposing unity power factor ($i_{qr} \approx 0$) and the output v_o at steady state, $\gamma_d i_d + \gamma_q i_q \approx i_o$, $v_d = \sqrt{3} V_{RMS}$, $v_q = 0, \gamma_q \approx v_q / v_o, \gamma_d \approx (v_d - R i_d)/v_o$. Then, from Eqs. (35.140) and (35.91), the following two sliding surfaces can be derived:

$$S_q\left(e_{i_q}, t\right) = k_{e_{i_q}}\left(i_{qr} - i_q\right) = 0 \tag{35.141}$$

$$S_d(e_{v_o}, e_\theta, t) \approx \left[\beta^{-1}(v_{o_r} - v_o) + \frac{dv_{o_r}}{dt} + \frac{1}{C} i_o + R_c \frac{di_o}{dt}\right] \times \frac{LC}{L - CRR_c} \frac{v_o}{\sqrt{3} V_{RMS} - R i_d} - i_d = i_{d_r} - i_d = 0 \tag{35.142}$$

where β^{-1} is the time constant of the desired first-order response of output voltage v_o ($\beta \gg T > 0$). For the synthesis of the closed-loop control system, notice that the terms of Eq. (35.142) inside the square brackets can be assumed as the i_d reference current i_{d_r}. Furthermore, from Eqs. (35.141) and (35.142), it is seen that the current control loops for i_d and i_q are needed. Considering Eqs. (35.138) and (35.136), the two sliding surfaces can be written as

$$S_\alpha\left(e_{i_\alpha}, t\right) = i_{\alpha_r} - i_\alpha = 0 \tag{35.143}$$

$$S_\beta\left(e_{i_\beta}, t\right) = i_{\beta_r} - i_\beta = 0 \tag{35.144}$$

The switching laws relating the sliding surfaces (35.143) and (35.144) with the switching variables γ_k are

$$\begin{cases} \text{if } S_{\alpha\beta}\left(e_{i_{\alpha\beta}}, t\right) > \varepsilon \text{ then } i_{\alpha\beta_r} > i_{\alpha\beta} \text{ hence choose } \gamma_k \text{ to increase the } i_{\alpha\beta} \text{ current} \\ \text{if } S_{\alpha\beta}\left(e_{i_{\alpha\beta}}, t\right) < -\varepsilon \text{ then } i_{\alpha\beta_r} > i_{\alpha\beta} \text{ hence choose } \gamma_k \text{ to decrease the } i_{\alpha\beta} \text{ current} \end{cases} \tag{35.145}$$

The practical implementation of this switching strategy could be accomplished using three independent two-level hysteresis comparators. However, this might introduce limit cycles as only two line currents are independent. Therefore, the control laws (35.143) and (35.144) can be implemented using the block diagram of Fig. 35.47A, with d, q/α, and β (from Eq. (35.138)) and 1,2,3/α, and β (from Eq. (35.136)) transformations and two

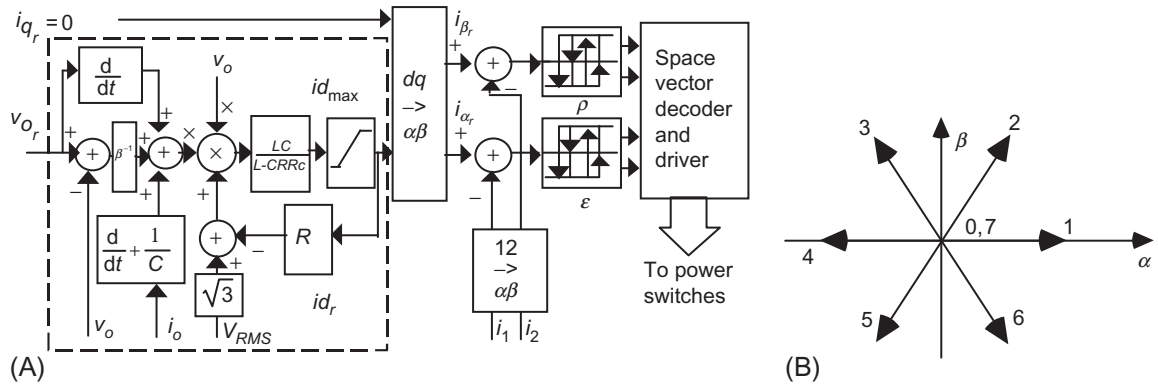


FIG. 35.47 (A) Sliding-mode PWM controller modulator for the unity power factor three-phase PWM rectifier and (B) α and β space-vector representation of the PWM bridge rectifier leg voltages.

three-level hysteretic comparators with equivalent hysteresis ε and ρ to limit the maximum switching frequency. A limiter is included to bound the i_d reference current to i_{dmax}, keeping the input line currents within a safe value. This helps to eliminate the nonminimum-phase behavior (outside sliding mode) when large transients are present while providing short-circuit proof operation.

α, β space vector current modulator

Depending on the values of γ_k, the bridge rectifier leg output voltages can assume only eight possible distinct states represented as voltage vectors in the α and β reference frame (Fig. 35.47B), for sources with isolated neutral.

With only two independent currents, two three-level hysteresis comparators, for the current errors, must be used in order to accurately select all eight available voltage vectors. Each three-level comparator [16] can be obtained by summing the outputs of two comparators with two levels each. One of these two comparators ($\delta_{L\alpha}$ and $\delta_{L\beta}$) has a wide hysteresis width, and the other ($\delta_{N\alpha}$ and $\delta_{N\beta}$) has a narrower hysteresis width. The hysteresis bands are represented by ε and ρ. Table 35.1 represents all possible output combinations of the resulting four two-level comparators, their sums giving the two three-level comparators (δ_α and δ_β), plus the voltage vector needed to accomplish the current tracking strategy $\left(i_{\alpha,\beta_r} - i_{\alpha,\beta}\right) = 0$ (ensuring $\left(i_{\alpha,\beta_r} - i_{\alpha,\beta}\right) \times d\left(i_{\alpha,\beta_r} - i_{\alpha,\beta}\right)/dt < 0$, plus the γ_k variables and the α and β voltage components).

From the analysis of the PWM boost rectifier, it is concluded that, if, for example, the voltage vector 2 is applied ($\gamma_1 = 1$, $\gamma_2 = 1$, and $\gamma_3 = 0$), in boost operation, the currents i_α and i_β will both decrease. Oppositely, if the voltage vector 5 ($\gamma_1 = 0$, $\gamma_2 = 0$, and $\gamma_3 = 1$) is applied, the currents i_α and i_β will both increase. Therefore, vector 2 should be selected when both i_α and i_β currents are above their respective references, that is, for $\delta_\alpha = -1$, $\delta_\beta = -1$, whereas vector 5 must be chosen when both i_α and i_β currents are under their respective references or, for $\delta_\alpha = 1$, $\delta_\beta = 1$. Nearly all the outputs of Table 35.2 can be filled using this kind of reasoning.

In the cases where $\delta_\alpha = 0$ and $\delta_\beta = -1$, the vector is selected upon the value of the i_α current error (if $\delta_{L\alpha} > 0$ and $\delta_{N\alpha} < 0$, then vector 2 and if $\delta_{L\alpha} < 0$ and $\delta_{N\alpha} > 0$, then vector 3). When $\delta_\alpha = 0$ and $\delta_\beta = 1$, if $\delta_{L\alpha} > 0$ and $\delta_{N\alpha} < 0$, then vector 6, else if $\delta_{L\alpha} < 0$ and $\delta_{N\alpha} > 0$, then vector 5. The vectors 0 and 7 are selected in order to minimize the switching frequency (if two of the three upper switches are on, then vector 7, otherwise vector 0). The space-vector decoder can be stored in a lookup table (or in an EPROM) whose inputs are the four two-level comparator outputs and the logic result of the operations needed to select between vectors 0 and 7.

PI output voltage control of the current-mode PWM rectifier

Using the α and β current-mode hysteresis modulators to enforce the i_d and i_q currents to follow their reference values, i_{d_r}, i_{q_r} (the values of L and C are such that the i_d and i_q currents usually exhibit a very fast dynamics compared with the slow dynamics of v_o), a first-order model (35.146) of the rectifier output voltage can be obtained from Eq. (35.73):

$$\frac{dv_o}{dt} = \left(\frac{1}{C} - \frac{RR_c}{L}\right)\left(\gamma_d i_{d_r} + \gamma_q i_{q_r}\right) - \frac{R_c\left(\gamma_d^2 + \gamma_q^2\right)}{L} v_o + \frac{R_c}{L}\left(\gamma_d v_d + \gamma_q v_q\right) - \frac{i_o}{C} - R_c \frac{di_o}{dt} \tag{35.146}$$

Assuming now a pure resistor load $R_1 = v_o/i_o$ and a mean delay T_d between the i_d current and the reference i_{d_r}, continuous

TABLE 35.2 Two-level and three-level comparator results, showing corresponding vector choice, corresponding γk and vector α and β component voltages; vectors are mapped in Fig. 35.47B

$\delta_{L\alpha}$	$\delta_{N\alpha}$	$\delta_{L\beta}$	$\delta_{N\beta}$	δ_α	δ_β	**Vector**	$\gamma 1$	$\gamma 2$	$\gamma 3$	v_α	v_β
−0.5	−0.5	−0.5	−0.5	−1	−1	**2**	1	1	0	$v_o/\sqrt{6}$	$v_o/\sqrt{2}$
0.5	−0.5	−0.5	−0.5	0	−1	**2**	1	1	0	$v_o/\sqrt{6}$	$v_o/\sqrt{2}$
0.5	0.5	−0.5	−0.5	1	−1	**3**	0	1	0	$-v_o/\sqrt{6}$	$v_o/\sqrt{2}$
−0.5	0.5	−0.5	−0.5	0	−1	**3**	0	1	0	$-v_o/\sqrt{6}$	$v_o/\sqrt{2}$
−0.5	0.5	0.5	−0.5	0	0	**0** or **7**	0 or 1	0 or 1	0 or 1	0	0
0.5	0.5	0.5	−0.5	1	0	**4**	0	1	1	$-\sqrt{2/3}v_o$	0
0.5	−0.5	0.5	−0.5	0	0	**0** or **7**	0 or 1	0 or 1	0 or 1	0	0
−0.5	−0.5	0.5	−0.5	−1	0	**1**	1	0	0	$\sqrt{2/3}v_o$	0
−0.5	−0.5	0.5	0.5	−1	1	**6**	1	0	1	$v_o/\sqrt{6}$	$-v_o/\sqrt{2}$
0.5	−0.5	0.5	0.5	0	1	**6**	1	0	1	$v_o/\sqrt{6}$	$-v_o/\sqrt{2}$
0.5	0.5	0.5	0.5	1	1	**5**	0	0	1	$-v_o/\sqrt{6}$	$-v_o/\sqrt{2}$
−0.5	0.5	0.5	0.5	0	1	**5**	0	0	1	$-v_o/\sqrt{6}$	$-v_o/\sqrt{2}$
−0.5	0.5	−0.5	0.5	0	0	**0** or **7**	0 or 1	0 or 1	0 or 1	0	0
0.5	0.5	−0.5	0.5	1	0	**4**	0	1	1	$-\sqrt{2/3}v_o$	0
0.5	−0.5	−0.5	0.5	0	0	**0** or **7**	0 or 1	0 or 1	0 or 1	0	0
−0.5	−0.5	−0.5	0.5	−1	0	**1**	1	0	0	$\sqrt{2/3}v_o$	0

transfer functions result for the i_d current ($i_d = i_{dr}(1+sTd)^{-1}$) and for the v_o voltage ($v_o = k_A i_d/(1+sk_B)$ with k_A and k_B obtained from Eq. (35.146)). Therefore, using the same approach as Examples 35.6, 35.8, and 35.11, a linear PI regulator, with gains K_p and K_i (35.147), sampling the error between the output voltage reference v_{o_r} and the output v_o, can be designed to provide a voltage proportional (k_I) to the reference current $i_{d_r}\left(i_{d_r} = \left(K_p + K_i/s\right)K_I(v_{o_r} - v_o)\right)$:

$$K_p = \frac{R_1 + R_c}{4\zeta^2 T_d R_1 K_1 \gamma_d (1/C - RR_c/L)}$$
$$K_i = \frac{R_c\left(\gamma_d^2 + \gamma_q^2\right)/L + 1/(R_1 C)}{4\zeta^2 T_d K_1 \gamma_d (1/C - RR_c/L)} \quad (35.147)$$

These PI regulator parameters depend on the load resistance R_1, on the rectifier parameters (C, R_c, L, and R), on the rectifier operating point γ_d, on the mean delay time T_d, and on the required damping factor ζ. Therefore, the expected response can only be obtained with the nominal load and input voltages, the line current dynamics depending on the K_p and K_i gains.

Results (Fig. 35.48) obtained with the values $V_{RMS} \approx 70$ V, $L \approx 1.1$ mH, $R \approx 0.1\ \Omega$, $C \approx 2000\ \mu$F with equivalent series resistance ESR $\approx 0.1\ \Omega$ ($R_c \approx 0.1\ \Omega$), $R_1 \approx 25\ \Omega$, $R_2 \approx 12\ \Omega$, $\beta = 0.0012$, $K_p = 1.2$, $K_i = 100$, and $k_I = 1$ show that the α and β space-vector current modulator ensures the current tracking needed (Fig. 35.48) [17–19]. The v_o step response reveals a faster sliding-mode controller and the correct design of the current-mode/PI controller parameters. The robustness property of the sliding-mode-controlled output v_o, compared with the current mode/PI, is shown in Fig. 35.49.

35.3.5.5 Example 35.15: Sliding-Mode Controllers for Multilevel Inverters

Diode-clamped multilevel inverters (Fig. 35.50) are the converters of choice for high-voltage high-power dc/ac or ac/ac (with dc link) applications, as the active semiconductors (usually gate turn-off thyristors (GTO) or IGBT transistors) of n-level power conversion systems, must withstand only a fraction (normally $U_{cc}/(n-1)$) of the total supply voltage U_{cc}. Moreover, the output voltage of multilevel converters, being staircase-like waveforms with n steps, features lower harmonic

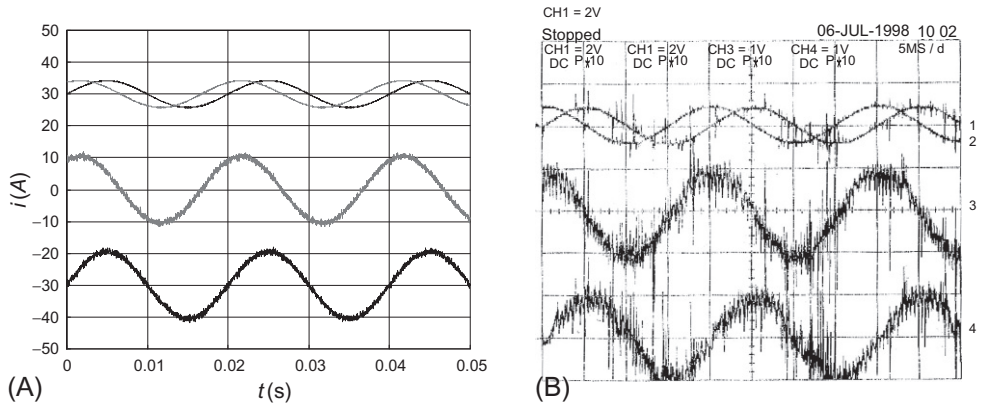


FIG. 35.48 α and β space-vector current modulator operation at near unity power factor: (A) simulation result ($i_{1r} + 30; i_{2_r} + 30; 2 \times i_1; 2 \times i_2 - 30$) and (B) experimental result ($1 \rightarrow i_{1r}, 2 \rightarrow i_{2r}$ (10 A/div); $3 \rightarrow i_1, 4 \rightarrow i_2$ (5 A/div)).

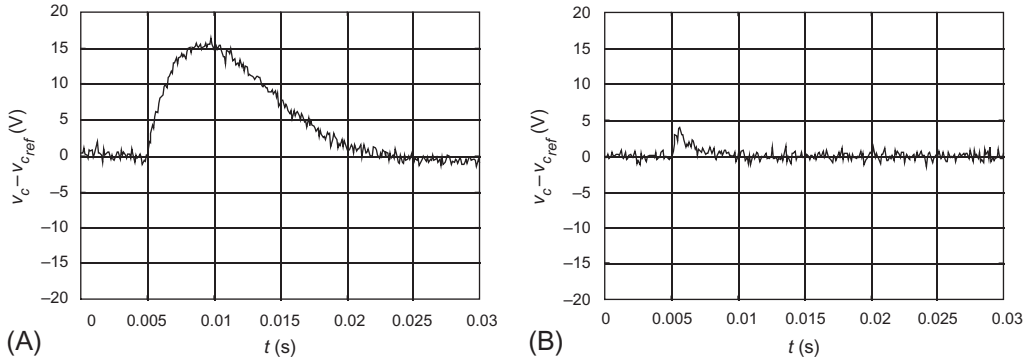


FIG. 35.49 Transition from rectifier to inverter operation (i_o from 8 to −8 A) obtained by switching off IGBT S_a (Fig. 35.46) and using $I_a = 16$ A: (A) $v_o - v_{or}$ (v) with sliding-mode control and (B) $v_o - v_{or}$ (v) with current-mode/PI control.

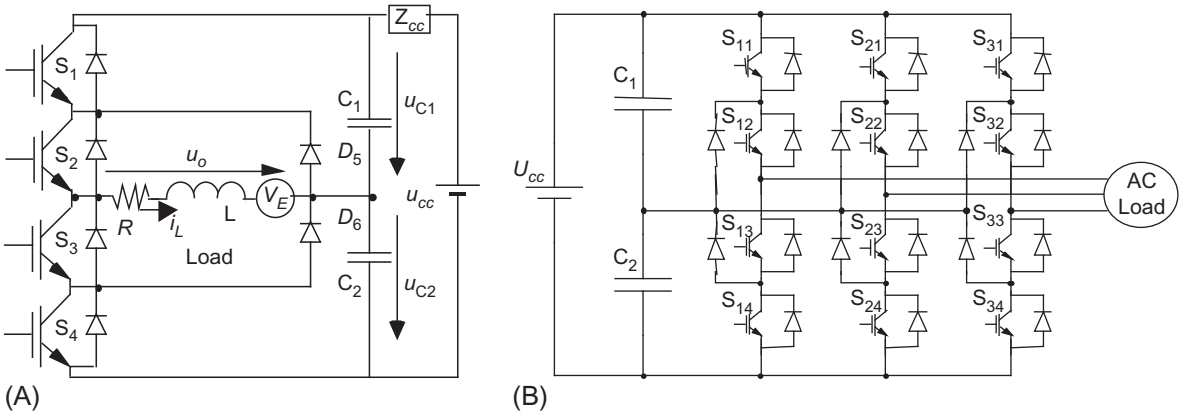


FIG. 35.50 (A) Single-phase, neutral-point-clamped, three-level inverter with IGBTs and (B) three-phase, neutral-clamped, three-level inverter.

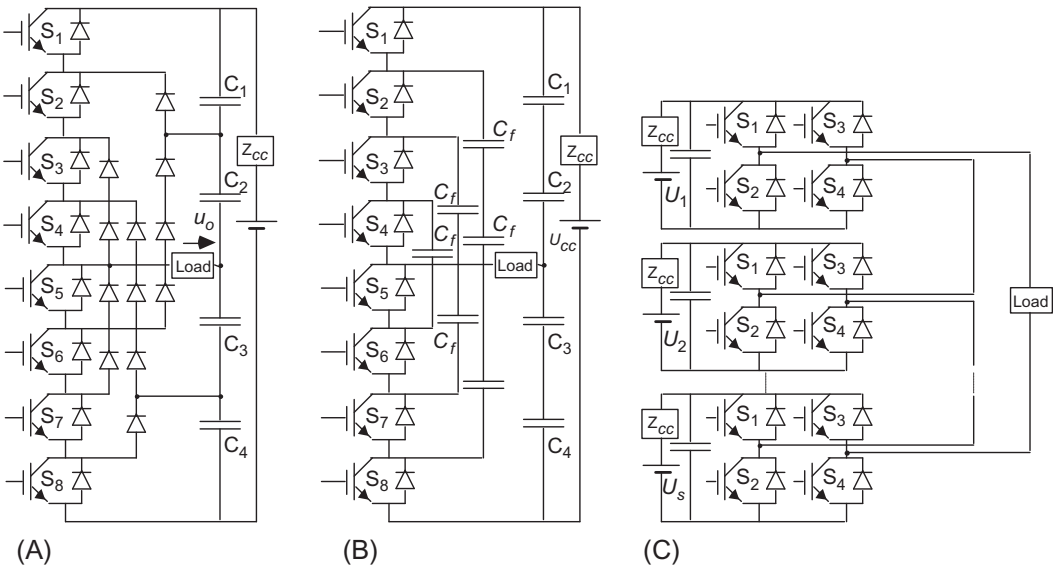


FIG. 35.51 (A) Five-level ($n=5$) diode-clamped inverter with IGBTs, (B) five-level ($n=5$) flying capacitor converter, and (C) multilevel converter based on cascaded full-bridge inverters.

distortion compared with the two-level waveforms with the same switching frequency.

The advantages of multilevel converters are paid into the price of the capacitor supply voltage dividers (Fig. 35.51) and voltage equalization circuits, into the cost of extra power supply arrangements (Fig. 35.51C) and into increased control complexity. This example shows how to extend the two-level switching law (35.97) to n-level converters and how to equalize the voltage of the capacitive dividers.

Considering single-phase three-level inverters (Fig. 35.50A), the open-loop control of the output voltage can be made using three-level SPWM. The two-level modulator, seen in Example 35.9, can be easily extended (Fig. 35.52A) to generate the γ_{III} command (Fig. 35.52B) to three-level inverter legs, from the two-level γ_{II} signal, either with a dedicated modulator or using the following relation:

$$\gamma_{III} = \gamma_{II}(m_i sin(\omega t) - \text{sgn}(m_i \sin(\omega t))/2 - r(t)/2) - 1/2 + \text{sgn}(m_i \sin(\omega t))/2 \quad (35.148)$$

The required three-level SPWM modulators for the output voltage synthesis seldom take into account the semiconductors and the capacitor voltage divider nonideal characteristics. Consequently, the capacitor voltage divider tends to drift, one capacitor being overcharged and the other discharged, and an asymmetry appears in the currents of the power supply. A steady-state error in the output voltage can also be present. Sliding-mode control can provide the optimum switching

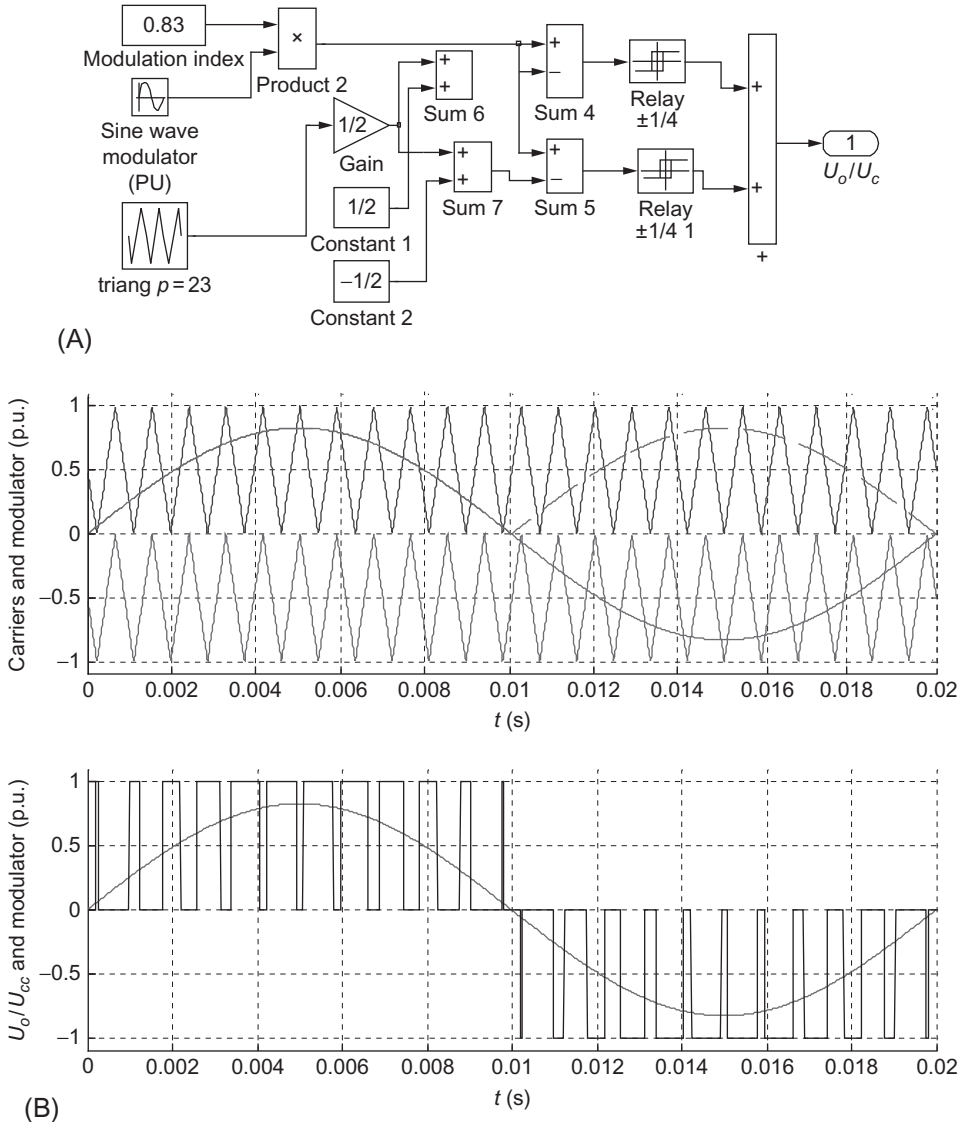


FIG. 35.52 (A) Three-level SPWM modulator schematic and (B) main three-level SPWM signals.

timing between all the converter levels, together with robustness to supply voltage disturbances, semiconductor nonidealities, and load parameters.

Sliding-mode surface and switching law

For a variable-structure system where the control input $u_i(t)$ can present n levels, consider the n values of the integer variable γ, being $-(n-1)/2 \leq \gamma \leq (n-1)/2$ and $u_i(t) = \gamma U_{cc}/(n-1)$, dependent on the topology and on the conducting semiconductors. To ensure the sliding-mode manifold invariance condition (35.92) and the reaching mode behavior, the switching strategy $\gamma(t_{k+1})$ for the time instant t_{k+1}, considering the value of $\gamma(t_k)$, must be

$$\gamma(t_{k+1}) = \begin{cases} \gamma(t_k) + 1 \text{ if } S(e_{x_i}, t) > \varepsilon \wedge \dot{S}(e_{x_i}, t) \\ \qquad > \varepsilon \wedge \gamma(t_k) < (n-1)/2 \\ \gamma(t_k) - 1 \text{ if } S(e_{x_i}, t) < -\varepsilon \wedge \dot{S}(e_{x_i}, t) \\ \qquad < -\varepsilon \wedge \gamma(t_k) > -(n-1)/2 \end{cases} \tag{35.149}$$

This switching law can be implemented as depicted in Fig. 35.53A and for five levels in B. An alternative is shown in Fig. 35.53C and named stability condition-based modulator [20], where the switching law (35.149) is directly used, calculating the sliding-mode surface and its time derivative, implemented as a discrete time variation. They are two-level quantized, and upon their values (obtained by half of their sum), the

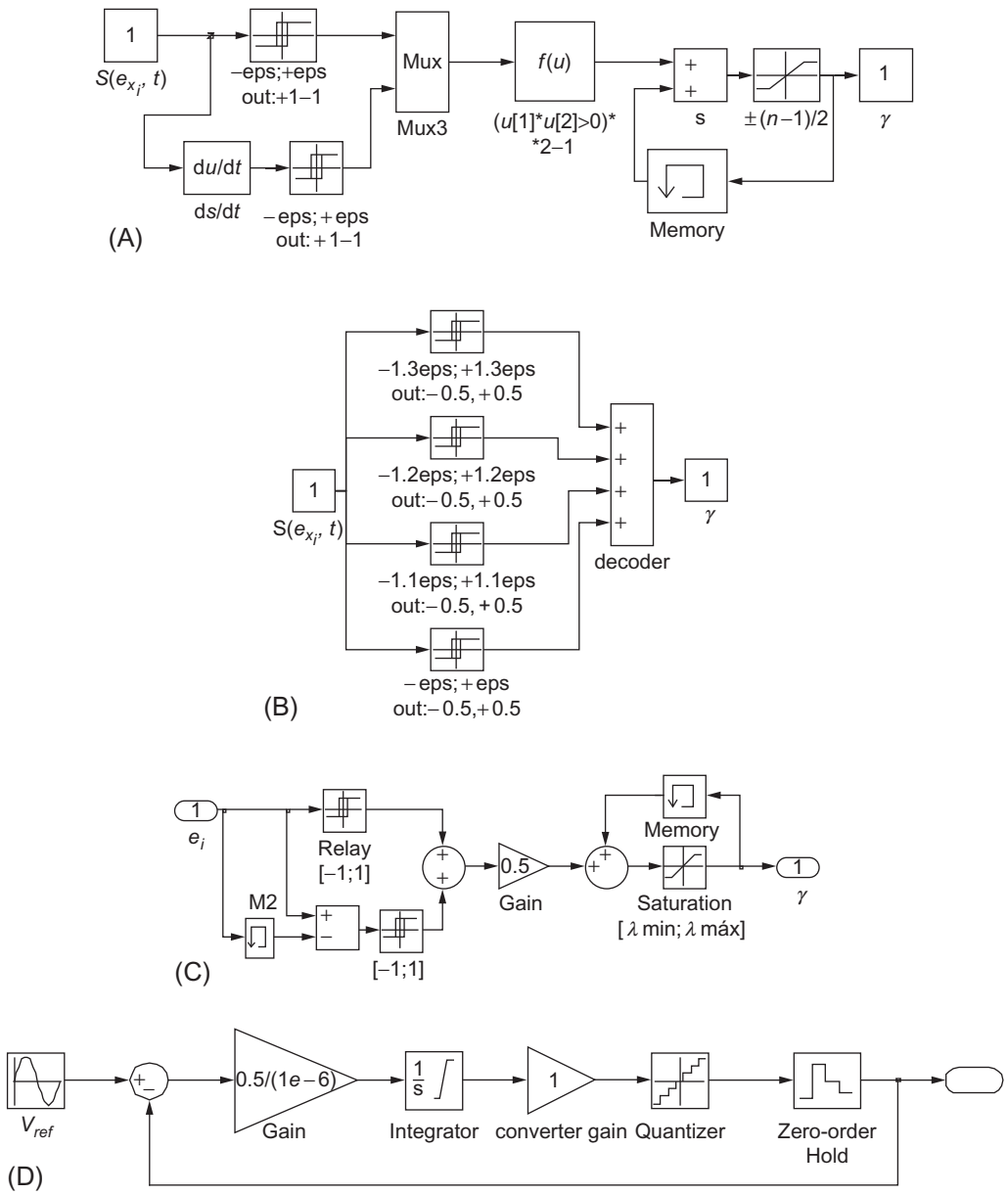


FIG. 35.53 (A) Multilevel sliding-mode PWM modulator with n-level hysteresis comparator with quantization interval ε, (B) four hysteresis comparator implementation of a five-level switching law, (C) stability condition-based multilevel modulator (one phase), (D) generalized sigma-delta n-level modulator.

voltage level is increased (or decreased), until it reaches the maximum (or the minimum). Therefore, the output level is increased (or decreased) if the error and its derivative are both positive (or negative), with the upper limit $\lambda_{máx} = (n-1)/2$ and lower limit $\lambda_{min} = -(n-1)/2$.

Other implementations are possible (Fig. 35.53D), since in every modulation method the generated pulse levels must have the same volt-second average of the fundamental sinusoidal (i.e., the integral over time of the n-level voltage waveform minus the value of the fundamental should be zero).

Control of the output voltage in single-phase multilevel converters

To control the inverter output voltage, in closed-loop and in diode-clamped multilevel inverters with n levels and supply voltage U_{cc}, a control law similar to Eq. (35.132), $S(e_{uo}, t) = \kappa \int (u_{o_r} - k_v \gamma(t_k) U_{cc}/(n-1))dt = 0$, is suitable.

Fig. 35.54A shows the waveforms of a five-level sliding-mode-controlled inverter, namely, the input sinus voltage, the generated output staircase wave, and the sliding-surface

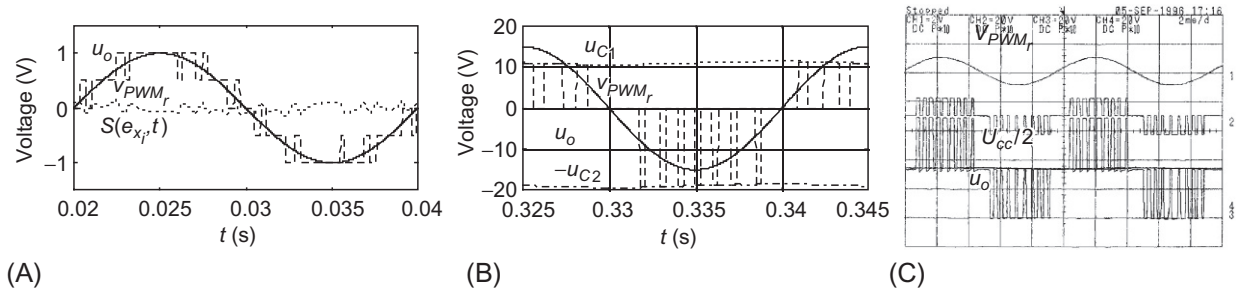


FIG. 35.54 (A) Scaled waveforms of a five-level sliding-mode-controlled single-phase converter, showing the input sinus voltage v_{PWM_r}, the generated output staircase wave u_o, and the value of the sliding surface $S(e_{x_i}, t)$; (B) scaled waveforms of a three-level neutral-point-clamped inverter showing the capacitor voltage unbalance (shown as two near-flat lines touching the tips of the PWM pulses); and (C) experimental results from a laboratory prototype of a three-level single-phase power inverter with the capacitor voltage equalization described.

instantaneous error. This error is always within a band centered around the zero value and presents zero mean value, which is not the case of sigma-delta modulators followed by n-level quantizers, where the error presents an offset mean value in each half period.

Experimental multilevel converters always show capacitor voltage unbalances (Fig. 35.54B) due to small differences between semiconductor voltage drops and circuitry offsets. To obtain capacitor voltage equalization, the voltage error $(v_{c_2} - U_{cc}/2)$ is fed back to the controller (Fig. 35.55A) to counteract the circuitry offsets. Experimental results (Fig. 35.54C) clearly show the effectiveness of the correction made. The small steady-state error, between the voltages of the two capacitors, still present, could be eliminated using an integral regulator (Fig. 35.55B).

Fig. 35.56 confirms the robustness of the sliding-mode controller to power supply disturbances.

Output current control in single-phase multilevel converters
Considering an inductive load with current i_L, the control law (35.107) and the switching law of (35.149) should be used for single-phase multilevel inverters. Results obtained using the capacitor voltage equalization principle just described are shown in Fig. 35.57.

35.3.5.6 Example 35.16: Sliding-Mode Controllers for Three-Phase Multilevel Inverters

Three-phase n-level inverters (Fig. 35.58) are suitable for high-voltage, high-power dc/ac applications, such as modern high-speed railway traction drives, as the controlled turn-off

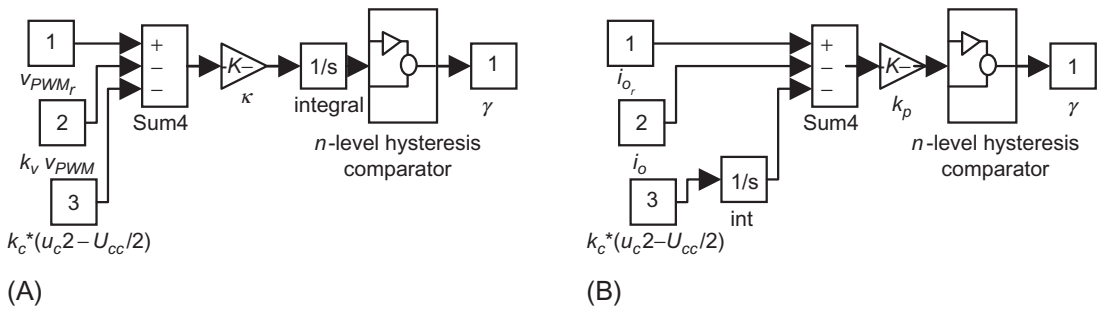


FIG. 35.55 (A) Multilevel sliding-mode output voltage controller and PWM modulator with capacitor voltage equalization and (B) sliding-mode output current controller with capacitor voltage equalization.

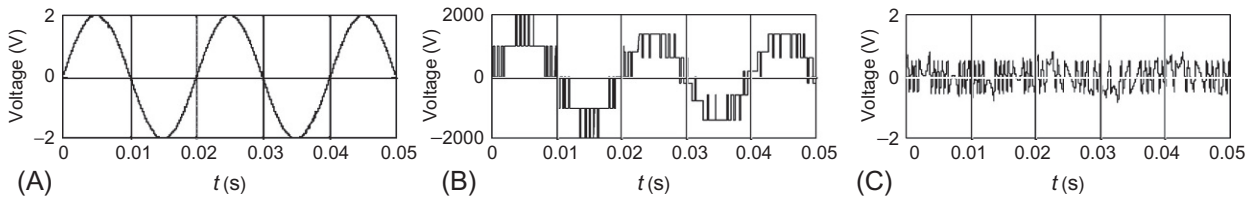


FIG. 35.56 Simulated performance of a five-level power inverter, with a U_{cc} voltage dip (from 2 to 1.5 kV). Response to a sinusoidal wave of frequency 50 Hz: (A) v_{PWM_r} input, (B) PWM output voltage u_o, and (C) the integral of the error voltage, which is maintained close to zero.

semiconductors must block only a fraction (normally $U_{dc}/(n-1)$) of the total supply voltage U_{dc}.

This example presents a real-time modulator for the control of the three output voltages and capacitor voltage equalization, based on the use of sliding mode and space vectors represented in the α and β frame. Capacitor voltage equalization is done with the proper selection of redundant space vectors.

Output voltage control in multilevel converters

To guarantee the topological constraints of this converter and the correct sharing of the U_{dc} voltage by the semiconductors, the switching strategy for the k leg ($k \in \{1, 2, 3\}$) must ensure complementary states to switches S_{k1} and S_{k3}.

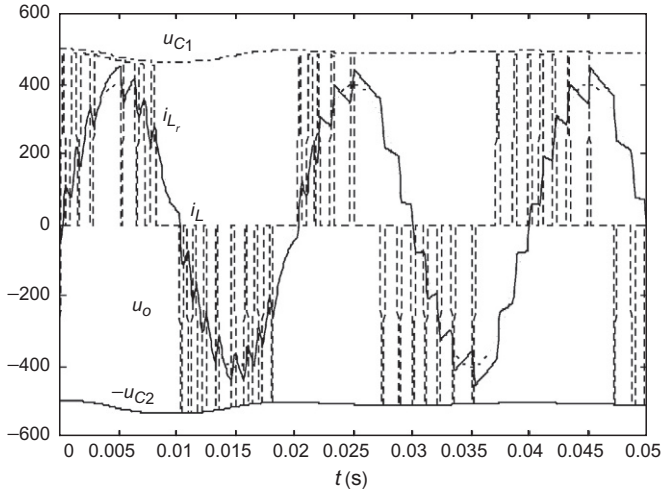


FIG. 35.57 Operation of a three-level neutral-point-clamped inverter as a sinusoidal current source: Scaled waveforms of the output current sine wave reference i_{Lr}, the output current i_L, showing ripple, together with the PWM-generated voltage u_o, with nearly equal pulse heights, corresponding to the equalized dc capacitor voltages u_{C1} and u_{C2}.

The same restriction applies for S_{k2} and S_{k4}. Neglecting switching delays, dead times, on-state semiconductor voltage drops, snubber networks, and power supply variations; supposing small dead times and equal capacitor voltages $U_{C1} = U_{C2} = U_{dc}/2$; and using the time-dependent switching variable $\gamma_k(t)$, the leg output voltage U_k (Fig. 35.58) will be $U_k = \gamma_k(t) U_{dc}/2$, with

$$\gamma_k(t) = \begin{cases} 1 & \text{if } S_{k1} \wedge S_{k2} \text{ are ON} \wedge S_{k3} \wedge S_{k4} \text{ are OFF} \\ 0 & \text{if } S_{k2} \wedge S_{k3} \text{ are ON} \wedge S_{k1} \wedge S_{k4} \text{ are OFF} \\ -1 & \text{if } S_{k3} \wedge S_{k4} \text{ are ON} \wedge S_{k1} \wedge S_{k2} \text{ are OFF} \end{cases} \tag{35.150}$$

The converter output voltages U_{Sk} of vector $\mathbf{U}_S$ can be expressed as

$$\mathrm{U}_S = \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ -1/3 & 2/3 & -1/3 \\ -1/3 & -1/3 & 2/3 \end{bmatrix} \begin{bmatrix} \gamma_1 \\ \gamma_2 \\ \gamma_3 \end{bmatrix} \frac{U_{dc}}{2} \tag{35.151}$$

The application of the Concordia transformation $U_{S1,2,3} = [\mathbf{C}]\, U_{S\alpha,\,\beta,\,o}$ (Eq. (35.152) to (35.151))

$$\begin{bmatrix} U_{S1} \\ U_{S2} \\ U_{S3} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 & 1/\sqrt{2} \\ -1/2 & \sqrt{3}/2 & 1/\sqrt{2} \\ -1/2 & -\sqrt{3}/2 & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} U_{S\alpha} \\ U_{S\beta} \\ U_{So} \end{bmatrix} \tag{35.152}$$

gives the output voltage vector in the α and β coordinates $\mathbf{U}_{S_{\alpha,\beta}}$:

$$\mathbf{U}_{S_{\alpha,\beta}} = \begin{bmatrix} U_{s\alpha} \\ U_{s\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \Gamma_1 \\ \Gamma_2 \\ \Gamma_3 \end{bmatrix} \frac{U_{dc}}{2} = \begin{bmatrix} \Gamma_\alpha \\ \Gamma_\beta \end{bmatrix} \frac{U_{dc}}{2} \tag{35.153}$$

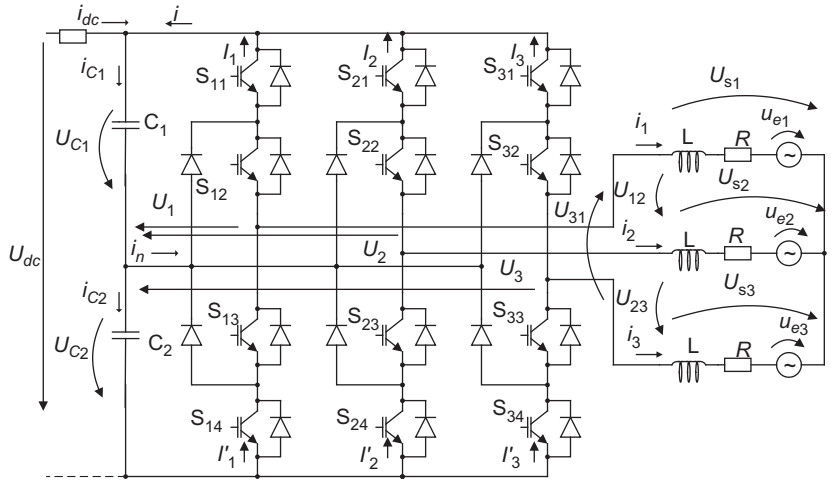


FIG. 35.58 Three-phase, neutral-point-clamped, three-level inverter with IGBTs.

where

$$\Gamma_1=\frac{2}{3}\gamma_1-\frac{1}{3}\gamma_2-\frac{1}{3}\gamma_3;\ \ \Gamma_2=\frac{2}{3}\gamma_2-\frac{1}{3}\gamma_3-\frac{1}{3}\gamma_1;$$
$$\Gamma_3=\frac{2}{3}\gamma_3-\frac{1}{3}\gamma_1-\frac{1}{3}\gamma_2 \tag{35.154}$$

The output voltage vector in the α and β coordinates $\mathbf{U}_{S_{\alpha,\beta}}$ is discontinuous. A suitable state variable for this output can be its average value $\overline{\mathbf{U}}_{S_{\alpha,\beta}}$ during one switching period:

$$\overline{\mathbf{U}}_{S_{\alpha,\beta}}=\frac{1}{T}\int_0^T \mathbf{U}_{S_{\alpha,\beta}}\mathrm{d}t=\frac{1}{T}\int_0^T \Gamma_{\alpha,\beta}\frac{U_{dc}}{2}\mathrm{d}t \tag{35.155}$$

The controllable canonical form is

$$\frac{\mathrm{d}}{\mathrm{d}t}\overline{\mathbf{U}}_{S_{\alpha,\beta}}=\frac{\mathbf{U}_{S_{\alpha,\beta}}}{T}=\frac{\Gamma_{\alpha,\beta}}{T}\frac{U_{dc}}{2} \tag{35.156}$$

Considering the control goal $\overline{\mathbf{U}}_{S_{\alpha,\beta}}=\overline{\mathbf{U}}_{S_{\alpha,\beta_{ref}}}$ and Eq. (35.91), the sliding surface is

$$\mathbf{S}(\mathbf{e}_{\alpha,\beta},t)=\sum_{o=1}^{\varphi}\mathbf{k}_{\alpha\beta_o}\mathbf{e}_{\alpha,\beta_o}=\mathbf{k}_{\alpha,\beta_1}\mathbf{e}_{\alpha,\beta_1}=\mathbf{k}_{\alpha,\beta_1}\left(\overline{\mathbf{U}}_{S_{\alpha,\beta_{ref}}}-\overline{\mathbf{U}}_{S_{\alpha,\beta}}\right)$$
$$=\frac{\mathbf{k}_{\alpha,\beta}}{T}\int_0^T\left(\mathbf{U}_{S_{\alpha,\beta ref}}-\mathbf{U}_{S_{\alpha,\beta}}\right)dt=0 \tag{35.157}$$

To ensure reaching mode behavior and sliding-mode stability (35.92), as the first derivative of Eq. (35.157), $\dot{\mathbf{S}}(\mathbf{e}_{\alpha,\beta},t)$ is

$$\dot{\mathbf{S}}(\mathbf{e}_{\alpha,\beta},t)=\frac{\mathbf{k}_{\alpha,\beta}}{T}\left(\mathbf{U}_{S_{\alpha,\beta ref}}-\mathbf{U}_{S_{\alpha,\beta}}\right) \tag{35.158}$$

The switching law is

$$\begin{aligned}&\mathbf{S}(\mathbf{e}_{\alpha,\beta},t)>0\Rightarrow\dot{\mathbf{S}}(\mathbf{e}_{\alpha,\beta},t)<0\Rightarrow\mathbf{U}_{S_{\alpha,\beta}}>\mathbf{U}_{S_{\alpha,\beta ref}}\\&\mathbf{S}(\mathbf{e}_{\alpha,\beta},t)<0\Rightarrow\dot{\mathbf{S}}(\mathbf{e}_{\alpha,\beta},t)>0\Rightarrow\mathbf{U}_{S_{\alpha,\beta}}<\mathbf{U}_{S_{\alpha,\beta ref}}\end{aligned} \tag{35.159}$$

This switching strategy must select the proper values of $\mathbf{U}_{S_{\alpha,\beta}}$ from the available outputs. As each inverter leg (Fig. 35.58) can deliver one of the three possible output voltages ($U_{dc}/2$, 0, and $-U_{dc}/2$), all the 27 possible output voltage vectors listed in Table 35.3 can be represented in the α and β frame of

TABLE 35.3 Vectors of the three-phase three-level converter, switching variables γk, switch states skj, and the corresponding output voltages, line to neutral point, line to line, and α and β components in per units

Vector	$\gamma1$	$\gamma2$	$\gamma3$	S_{11}	S_{12}	S_{13}	S_{14}	S_{21}	S_{22}	S_{23}	S_{24}	S_{31}	S_{32}	S_{33}	S_{34}	U_1	U_2	U_3	U_{12}	U_{23}	U_{31}	$U_{s\alpha}/U_{dc}$	$U_{s\beta}/U_{dc}$
1	1	1	1	1	1	0	0	1	1	0	0	1	1	0	0	$U_{dc}/2$	$U_{dc}/2$	$U_{dc}/2$	0	0	0	0.00	0.00
2	1	1	0	1	1	0	0	1	1	0	0	0	1	1	0	$U_{dc}/2$	$U_{dc}/2$	0	0	$U_{dc}/2$	$-U_{dc}/2$	0.20	0.35
3	1	1	−1	1	1	0	0	1	1	0	0	0	0	1	1	$U_{dc}/2$	$U_{dc}/2$	$-U_{dc}/2$	0	U_{dc}	$-U_{dc}$	0.41	0.71
4	1	0	−1	1	1	0	0	0	1	1	0	0	0	1	1	$U_{dc}/2$	0	$-U_{dc}/2$	$U_{dc}/2$	$U_{dc}/2$	$-U_{dc}$	0.61	0.35
5	1	0	0	1	1	0	0	0	1	1	0	0	1	1	0	$U_{dc}/2$	0	0	$U_{dc}/2$	0	$-U_{dc}/2$	0.41	0.00
6	1	0	1	1	1	0	0	0	1	1	0	1	1	0	0	$U_{dc}/2$	0	$U_{dc}/2$	$U_{dc}/2$	$-U_{dc}/2$	0	0.20	−0.35
7	1	−1	1	1	1	0	0	0	0	1	1	1	1	0	0	$U_{dc}/2$	$-U_{dc}/2$	$U_{dc}/2$	U_{dc}	$-U_{dc}$	0	0.41	−0.71
8	1	−1	0	1	1	0	0	0	0	1	1	0	1	1	0	$U_{dc}/2$	$-U_{dc}/2$	0	U_{dc}	$-U_{dc}/2$	$-U_{dc}/2$	0.61	−0.35
9	1	−1	−1	1	1	0	0	0	0	1	1	0	0	1	1	$U_{dc}/2$	$-U_{dc}/2$	$-U_{dc}/2$	U_{dc}	0	$-U_{dc}$	0.82	0.00
10	0	−1	−1	0	1	1	0	0	0	1	1	0	0	1	1	0	$-U_{dc}/2$	$-U_{dc}/2$	$U_{dc}/2$	0	$-U_{dc}/2$	0.41	0.00
11	0	−1	0	0	1	1	0	0	0	1	1	0	1	1	0	0	$-U_{dc}/2$	0	$U_{dc}/2$	$-U_{dc}/2$	0	0.20	−0.35
12	0	−1	1	0	1	1	0	0	0	1	1	1	1	0	0	0	$-U_{dc}/2$	$U_{dc}/2$	$U_{dc}/2$	$-U_{dc}$	$U_{dc}/2$	0.00	−0.71
13	0	0	1	0	1	1	0	0	1	1	0	1	1	0	0	0	0	$U_{dc}/2$	0	$-U_{dc}/2$	$U_{dc}/2$	−0.20	−0.35
14	0	0	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0.00	0.00
15	0	0	−1	0	1	1	0	0	1	1	0	0	0	1	1	0	0	$-U_{dc}/2$	0	$U_{dc}/2$	$-U_{dc}/2$	0.20	0.35
16	0	1	−1	0	1	1	0	1	1	0	0	0	0	1	1	0	$U_{dc}/2$	$-U_{dc}/2$	$-U_{dc}/2$	U_{dc}	$-U_{dc}/2$	0.00	0.71
17	0	1	0	0	1	1	0	1	1	0	0	0	1	1	0	0	$U_{dc}/2$	0	$-U_{dc}/2$	$U_{dc}/2$	0	−0.20	0.35
18	0	1	1	0	1	1	0	1	1	0	0	1	1	0	0	0	$U_{dc}/2$	$U_{dc}/2$	$-U_{dc}/2$	0	$U_{dc}/2$	−0.41	0.00
19	−1	1	1	0	0	1	1	1	1	0	0	1	1	0	0	$-U_{dc}/2$	$U_{dc}/2$	$U_{dc}/2$	$-U_{dc}$	0	U_{dc}	−0.82	0.00
20	−1	1	0	0	0	1	1	1	1	0	0	0	1	1	0	$-U_{dc}/2$	$U_{dc}/2$	0	$-U_{dc}$	U_{dc}	$U_{dc}/2$	−0.61	0.35
21	−1	1	−1	0	0	1	1	1	1	0	0	0	0	1	1	$-U_{dc}/2$	$U_{dc}/2$	$-U_{dc}/2$	$-U_{dc}$	U_{dc}	0	−0.41	0.71
22	−1	0	−1	0	0	1	1	0	1	1	0	0	0	1	1	$-U_{dc}/2$	0	$-U_{dc}/2$	$-U_{dc}/2$	$U_{dc}/2$	0	−0.20	0.35
23	−1	0	0	0	0	1	1	0	1	1	0	0	1	1	0	$-U_{dc}/2$	0	0	$-U_{dc}/2$	0	$U_{dc}/2$	−0.41	0.00
24	−1	0	1	0	0	1	1	0	1	1	0	1	1	0	0	$-U_{dc}/2$	0	$U_{dc}/2$	$-U_{dc}/2$	$-U_{dc}/2$	U_{dc}	−0.61	−0.35
25	−1	−1	1	0	0	1	1	0	0	1	1	1	1	0	0	$-U_{dc}/2$	$-U_{dc}/2$	$U_{dc}/2$	0	$-U_{dc}/2$	U_{dc}	−0.41	−0.71
26	−1	−1	0	0	0	1	1	0	0	1	1	0	1	1	0	$-U_{dc}/2$	$-U_{dc}/2$	0	0	$-U_{dc}/2$	$U_{dc}/2$	−0.20	−0.35
27	−1	−1	−1	0	0	1	1	0	0	1	1	0	0	1	1	$-U_{dc}/2$	$-U_{dc}/2$	$-U_{dc}/2$	0	0	0	0.00	0.00

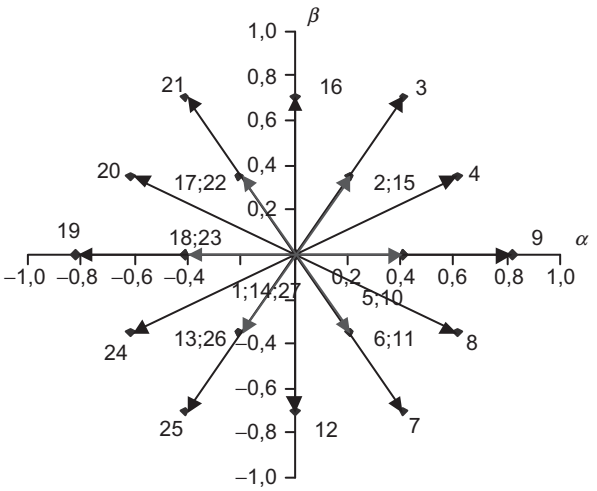


FIG. 35.59 Output voltage vectors (1–27) of three-phase, neutral-clamped three-level inverters, in the α and β frame.

Fig. 35.59 (in per units, 1 p.u. $= U_{dc}$). There are nine different levels for the α space vector component and only five for the β component. However, considering any particular value of α (or β) component, there are at most five levels available in the remaining orthogonal component. From the load viewpoint, the 27 space vectors of Table 35.3 define only 19 distinct space positions (Fig. 35.59).

To select one of these 19 positions from the control law (35.157) and the switching law of Eq. (35.159), two five-level hysteretic comparators (Fig. 35.53B) must be used ($5^2 = 25$). Their outputs are the integer variables λ_α and λ_β, denoted $\lambda_{\alpha,\beta}$ ($\lambda_\alpha, \lambda_\beta \in \{-2; -1; 0; 1; 2\}$) corresponding to the five selectable levels of Γ_α and Γ_β. Considering the sliding-mode stability, $\lambda_{\alpha,\beta}$, at time step $j+1$, is given by Eq. (35.160), knowing their previous values at step j. This means that the output level is increased (decreased) if the error and its derivative are both positive (negative), provided the maximum (minimum) output level is not exceeded:

$$\begin{cases} \left(\lambda_{\alpha,\beta}\right)_{j+1} = \left(\lambda_{\alpha,\beta}\right)_j + 1 \quad \text{if } \mathbf{S}\left(\mathbf{e}_{\alpha,\beta}, t\right) > \varepsilon \wedge \dot{\mathbf{S}}\left(\mathbf{e}_{\alpha,\beta}, t\right) \\ \qquad\qquad > \varepsilon \wedge \left(\lambda_{\alpha,\beta}\right)_j < 2 \\ \left(\lambda_{\alpha,\beta}\right)_{j+1} = \left(\lambda_{\alpha,\beta}\right)_j - 1 \quad \text{if } \mathbf{S}\left(\mathbf{e}_{\alpha,\beta}, t\right) < -\varepsilon \wedge \dot{\mathbf{S}}\left(\mathbf{e}_{\alpha,\beta}, t\right) \\ \qquad\qquad < -\varepsilon \wedge \left(\lambda_{\alpha,\beta}\right)_j > -2 \end{cases} \tag{35.160}$$

The available space vectors must be chosen not only to reduce the mean output voltage errors but also to guarantee transitions only between the adjacent levels, to minimize the capacitor voltage unbalance, to minimize the switching frequency, to observe minimum on or off times if applicable, and to equally stress all the semiconductors.

Using Eq. (35.160) and the control laws $S(\mathbf{e}_{\alpha,\beta,t})$ Eq. (35.157), Tables 35.4 and 35.5 can be used to choose the correct voltage vector in order to ensure stability, output voltage tracking, and DC capacitor voltage equalization. The vector with α and β components corresponding to the levels of the pair λ_β and λ_α is selected, provided that the adjacent transitions on inverter legs are obtained. If there is no directly corresponding vector, then the nearest vector guaranteeing adjacent transitions is selected. If a zero vector must be applied, then one of the three zero vectors (1, 14, and 27) is selected, to minimize the switching frequency. If more than one vector is the nearest, then one of them is selected to equalize the capacitor voltages, as shown next.

TABLE 35.4 Switching table to be sed if $(U_{C1} - U_{C2}) > \varepsilon_{eU}$ in the inverter mode or $(U_{C1} - U_{C2}) < -\varepsilon_{eU}$ in the regenerative mode, showing vector selection upon the variables λ_α and λ_β

$\lambda_\beta \backslash \lambda_\alpha$	−2	−1	0	1	2
−2	25	25	12	7	7
−1	24	13	13, 6	6	8
0	19	18	1, 14, 27	5	9
1	20	17	17, 2	2	4
2	21	21	16	3	3

TABLE 35.5 Switching table to be used if $(U_{C1} - U_{C2}) > \varepsilon_{eU}$ in the regenerative mode or $(U_{C1} - U_{C2}) < -\varepsilon_{eU}$ in the inverter mode, showing vector selection upon the variables λ_α and λ_β

$\lambda_\beta / \lambda_\alpha$	−2	−1	0	1	2
−2	25	25	12	7	7
−1	24	26	26, 11	11	8
0	19	23	1, 14, 27	10	9
1	20	22	22,15	15	4
2	21	21	16	3	3

DC capacitor voltage equalization

The discrete values of $\lambda_{\alpha,\beta}$ allow 25 different combinations. As only 19 are distinct from the load viewpoint, the extra ones can be used to select vectors that are able to equalize the capacitor voltages ($U_{C1} = U_{C2} = U_{dc/2}$).

Considering the control goal $U_{C1} = U_{C2}$, since the first derivatives of U_{C1} and U_{C2} Eq. (35.161) directly depend on the $\gamma_k(t)$ control inputs, from Eq. (35.91), the sliding surface is given by Eq. (35.162), where k_U is a positive gain:

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} U_{C1} \\ U_{C2} \end{bmatrix} = \begin{bmatrix} -\dfrac{\gamma_1(1+\gamma_1)}{2C_1} & -\dfrac{\gamma_2(1+\gamma_2)}{2C_1} & -\dfrac{\gamma_3(1+\gamma_3)}{2C_1} & \dfrac{1}{C_1} \\ -\dfrac{\gamma_1(1-\gamma_1)}{2C_2} & -\dfrac{\gamma_2(1-\gamma_2)}{2C_2} & -\dfrac{\gamma_3(1-\gamma_3)}{2C_2} & \dfrac{1}{C_2} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_{dc} \end{bmatrix} \tag{35.161}$$

$$S(e_{Uc}, t) = k_U e_{Uc}(t) = k_U (U_{C1} - U_{C2}) = 0 \tag{35.162}$$

The first derivative of $U_{C1} - U_{C2}$ (the sliding surface) is (Fig. 35.58 with $C_1 = C_2 = C$)

$$\frac{\mathrm{d}}{\mathrm{d}t}e_{Uc}=\frac{i_{C1}}{C_1}-\frac{i_{C2}}{C_2}=\frac{i_n}{C}=\frac{\left(\gamma_3^2-\gamma_1^2\right)i_1+\left(\gamma_3^2-\gamma_2^2\right)i_2}{C} \tag{35.163}$$

To ensure reaching mode behavior and sliding-mode stability, from Eq. (35.92), considering a small enough $e_{Uc}(t)$ error, ε_{eU}, the switching law is

$$\begin{aligned} S(e_{Uc},t)>\varepsilon_{eU}\Rightarrow\dot{S}(e_{Uc},t)<0\Rightarrow i_n<0\\ S(e_{Uc},t)<-\varepsilon_{eU}\Rightarrow\dot{S}(e_{Uc},t)>0\Rightarrow i_n>0 \end{aligned} \tag{35.164}$$

From circuit analysis, it can be seen that vectors (2, 5, 6, 13, 17, and 18) result in the discharge of capacitor C_1, if the converter operates in inverter mode, or in the charge of C_1, if the converter operates in boost rectifier (regenerative) mode. Similar reasoning can be applied for vectors (10, 11, 15, 22, 23, and 26) and capacitor C_2, since this vector set gives i_n currents with opposite sign relatively to the set (2, 5, 6, 13, 17, and 18). Therefore, considering the vector $[\Upsilon_1,\Upsilon_2]=\left[\left(\gamma_1^2-\gamma_3^2\right),\left(\gamma_2^2-\gamma_3^2\right)\right]$, the switching law is the following:

If $(U_{C1}-U_{C2})>\varepsilon_{eU}$,

THEN { IF the candidate vector from {2, 5, 6, 13, 17, 18} gives $(\Upsilon_1 i_1+\Upsilon_2 i_2)>0$, THEN choose the vector according to $\lambda_{\alpha,\beta}$ on Table 34.4; ELSE, the candidate vector of {10, 11, 15, 22, 23, 26} gives $(\Upsilon_1 i_1+\Upsilon_2 i_2)>0$, the vector being chosen according to $\lambda_{\alpha,\beta}$ from (table 34.5)

If $(U_{C1}-U_{C2})<\varepsilon_{eU}$,

THEN { IF the candidate vector from {2, 5, 6, 13, 17, 18} gives $(\Upsilon_1 i_1+\Upsilon_2 i_2)<0$, THEN choose the vector according to $\lambda_{\alpha,\beta}$ on Table 34.4; ELSE, the candidate vector of {10, 11, 15, 22, 23, 26} gives $(\Upsilon_1 i_1+\Upsilon_2 i_2)<0$, the vector being chosen according to $\lambda_{\alpha,\beta}$ from (table 34.5)

For example, consider the case where $U_{C1}>U_{C2}+\varepsilon_{eU}$. Then, the capacitor C_2 must be charged, and Table 35.4 must be used if the multilevel inverter is operating in the inverter mode or Table 35.5 for the regenerative mode. Additionally, when using Table 35.4, if $\lambda_\alpha=-1$ and $\lambda_\beta=-1$, then vector 13 should be used.

Experimental results shown in Fig. 35.61 were obtained with a low-power, scaled-down laboratory prototype (150 V and 3 kW) of a three-level inverter (Fig. 35.60), controlled by two four-level comparators, and described capacitor voltage equalizing procedures and EPROM-based lookup Tables 35.3–35.5. Transistors IGBT (MG25Q2YS40) were switched at frequencies

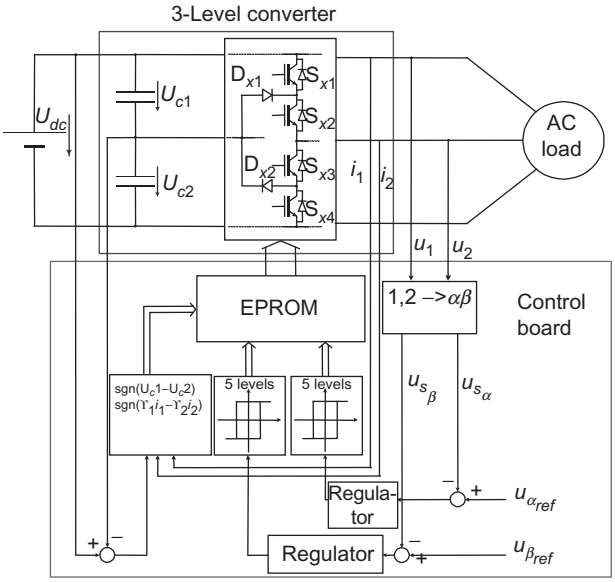


FIG. 35.60 Block diagram of the multilevel converter and control board.

near 4 kHz, with neutral clamp diodes 40HFL, $C_1\approx C_2\approx 20$ mF. The load was mainly inductive (3×10 mH and 2 Ω).

The inverter number of levels (three for the phase voltage and five for the line voltage), together with the adjacent transitions of inverter legs between levels, is shown in Fig. 35.61A and, in detail, in Fig. 35.62A.

The performance of the capacitor voltage equalizing strategy is shown in Fig. 35.62B, where the reference current of phase 1 and the output current of phase 3, together with the power supply voltage ($U_{dc}\approx 100$ V) and the voltage of capacitor $C_2(U_{C2})$, can be seen. It can be noted that the U_{C2} voltage is nearly half of the supply voltage. Therefore, the capacitor voltages are nearly equal. Furthermore, it can be stated that without this voltage equalization procedure, the three-level inverter operates only during a brief transient, during which one of the capacitor voltages vanishes to nearly 0 V and the other is overcharged to the supply voltage. Fig. 35.61B shows the harmonic spectrum of the output voltages, where the harmonics due to the switching frequency (≈4.5 kHz) and the fundamental harmonic can be seen.

On-line output current control in multilevel inverters

Considering a standard inductive balanced load (R and L) with electromotive force (u) and isolated neutral, the converter output currents i_k can be expressed:

$$U_{Sk}=Ri_k+L\frac{\mathrm{d}i_k}{\mathrm{d}t}+u_{ek} \tag{35.165}$$

Now analyzing the circuit of Fig. 35.58, the multilevel converter switched state-space model can be obtained:

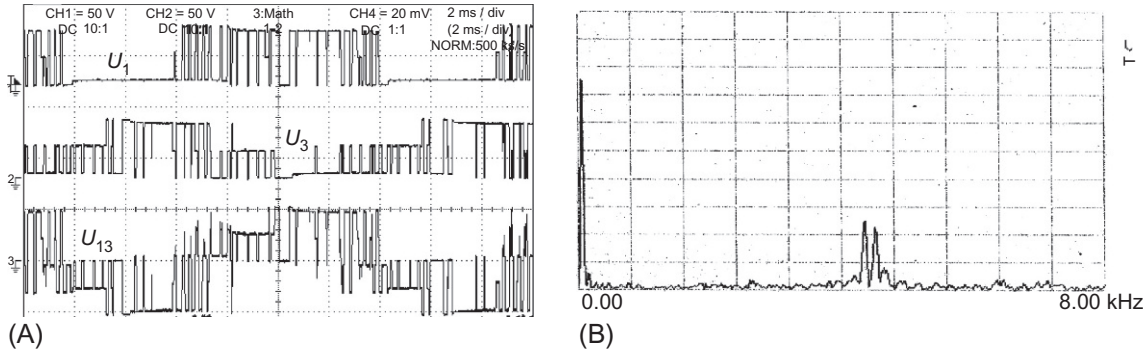


FIG. 35.61 (A) Experimental results showing phase and line voltages and (B) harmonic spectrum of output voltages.

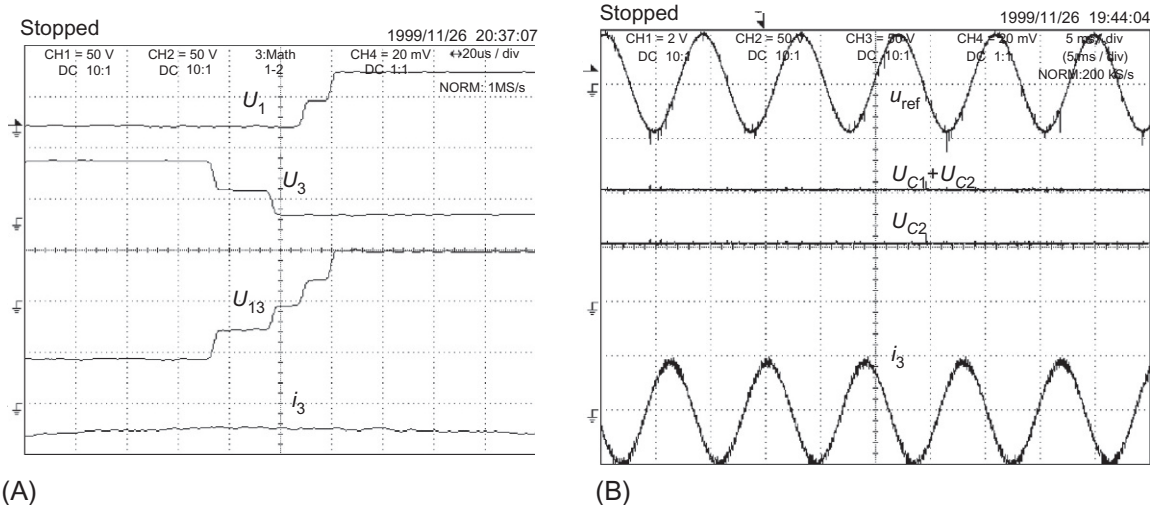


FIG. 35.62 Experimental results showing (A) the transitions between adjacent voltage levels (50 V/div and time 20 μs/div) and (B) performance of the capacitor voltage equalizing strategy; from top trace to bottom, 1 is the voltage reference input; 2 is the power supply voltage; 3 is the midpoint capacitor voltage, which is maintained close to $U_{dc}/2$; and 4 is the output current of phase 3 (2 A/div, 50 V/div, and 5 ms/div).

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = -\begin{bmatrix} \frac{R}{L} & 0 & 0 \\ 0 & \frac{R}{L} & 0 \\ 0 & 0 & \frac{R}{L} \end{bmatrix}\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} - \begin{bmatrix} \frac{1}{L} & 0 & 0 \\ 0 & \frac{1}{L} & 0 \\ 0 & 0 & \frac{1}{L} \end{bmatrix}\begin{bmatrix} u_{e1} \\ u_{e2} \\ u_{e3} \end{bmatrix} + \begin{bmatrix} \frac{\Gamma_1}{L} \\ \frac{\Gamma_2}{L} \\ \frac{\Gamma_3}{L} \end{bmatrix}\frac{U_{dc}}{2} \tag{35.166}$$

The application of the Concordia matrix Eqs. (35.152)–(35.166) reduces the number of the new model equations (Eq. (35.167)) to two, since an isolated neutral is assumed:

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = -\begin{bmatrix} \frac{R}{L} & 0 \\ 0 & \frac{R}{L} \end{bmatrix}\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} - \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix}\begin{bmatrix} u_{e\alpha} \\ u_{e\beta} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix}\begin{bmatrix} U_{S\alpha} \\ U_{S\beta} \end{bmatrix} \tag{35.167}$$

The model Eq. (35.167) of this multiple-input multiple-output system (MIMO) with outputs i_α and i_β reveals the control inputs $U_{S\alpha}$ and $U_{S\beta}$, dependent on the control variables $\gamma_k(t)$.

From Eqs. (35.167) and (35.91), the two sliding surfaces $\mathbf{S}(\mathbf{e}_{\alpha,\,\beta,}\,t)$ are

$$\mathbf{S}\left(\mathbf{e}_{\alpha,\beta,}t\right) = \mathbf{k}_{\alpha,\beta}\left(\mathbf{i}_{\alpha,\beta ref} - \mathbf{i}_{\alpha,\beta}\right) = \mathbf{k}_{\alpha,\beta}\mathbf{e}_{\alpha,\beta} = 0 \tag{35.168}$$

The first derivatives of Eq. (35.167), denoted $\dot{\mathbf{S}}\left(\mathbf{e}_{\alpha,\beta},t\right)$, are

$$\begin{aligned}\dot{\mathbf{S}}\left(\mathbf{e}_{\alpha,\beta},t\right) &= \mathbf{k}_{\alpha,\beta}\left(\dot{\mathbf{i}}_{\alpha,\beta ref} - \dot{\mathbf{i}}_{\alpha,\beta}\right) \\ &= \mathbf{k}_{\alpha,\beta}\left[\dot{\mathbf{i}}_{\alpha,\beta ref} + \mathbf{R}\mathbf{L}^{-1}\mathbf{i}_{\alpha,\beta} + \mathbf{u}_{e\alpha,\beta}\mathbf{L}^{-1} - \mathbf{U}_{S\alpha,\beta}\mathbf{L}^{-1}\right]\end{aligned} \tag{35.169}$$

Therefore, the switching law is

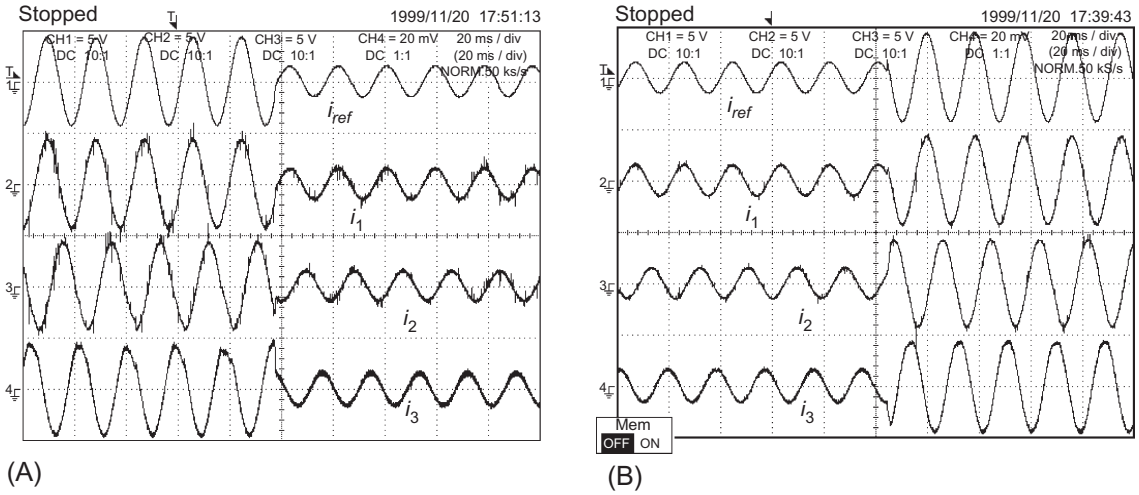


FIG. 35.63 Step response of the current control method: (A) step from 4 to 2 A. Traces show the reference current for phase 1 and the three output currents with 150 V power supply (5 A/div and time scale 20 ms/div) and (B) step from 2 to 4 A in the reference amplitude at 52 Hz. Traces show the reference current for phase 1 and the three output currents with 50 V power supply.

$$\mathbf{S}(\mathbf{e}_{\alpha,\beta},t)>0\Rightarrow\dot{\mathbf{S}}(\mathbf{e}_{\alpha,\beta},t)<0\Rightarrow\mathbf{U}_{\mathbf{S}\alpha,\beta}>\mathbf{L}\dot{\mathbf{i}}_{\alpha,\beta ref}+\mathbf{R}\mathbf{i}_{\alpha,\beta}+\mathbf{u}_{e\alpha,\beta}$$
$$\mathbf{S}(\mathbf{e}_{\alpha,\beta},t)<0\Rightarrow\dot{\mathbf{S}}(\mathbf{e}_{\alpha,\beta},t)>0\Rightarrow\mathbf{U}_{\mathbf{S}\alpha,\beta}>\mathbf{L}\dot{\mathbf{i}}_{\alpha,\beta ref}+\mathbf{R}\mathbf{i}_{\alpha,\beta}+\mathbf{u}_{e\alpha,\beta} \quad (35.170)$$

These switching laws are implemented using the same α and β vector modulator described above in this example.

Fig. 35.63A shows the experimental results. The multilevel converter and proposed control behavior are obtained for step inputs (4–2 A) in the amplitude of the sinus references with frequency near 52 Hz ($U_{dc}\approx 150$ V). Observe the tracking ability, the fast transient response, and the balanced three-phase currents. Fig. 35.63B shows almost the same test (step response from 2 to 4 A at the same frequency), but now, the power supply is set at 50 V, and the inductive load was unbalanced (±30% on resistor value). The response remains virtually the same, with tracking ability, almost no current distortions due to dead times or semiconductor voltage drops. These results and other works [21,51] confirm experimentally that the designed controllers are robust concerning these nonidealities.

35.3.5.7 Example 35.17: Sliding-Mode Vector Controllers for Matrix Converters

Matrix converters are all silicon ac/ac switching power converters, able to provide almost sinusoidal output voltages with adjustable amplitude and frequency, almost sinusoidal input currents, and controllable input power factor [22]. They have been used in ac drive speed control and are well suited for applications related to power-quality enhancement. The lack of an intermediate energy storage link results in high power density, their main advantage, but implies an input/output coupling that increases the control complexity.

This example presents the design of sliding-mode controllers considering the switched state-space model of the matrix converter (nine bidirectional power switches), including the three-phase input filter and the output load (Fig. 35.64).

Output voltage control

Ideal three-phase matrix converters are obtained by assembling nine bidirectional switches, with the turn-off capability, to allow the connection of each one of the input phases to any one of the output phases (Fig. 35.64). The states of these switches are usually represented as a nine-element matrix **S** (Eq. (35.171)), in which each matrix element, S_{kj} $k, j\in\{1, 2, 3\}$, has two possible states: $S_{kj}=1$ if the switch is closed (ON) and $S_{kj}=0$ if it is open (OFF). Only 27 switching combinations are possible (Table 35.6), as a result of the topological constraints (the input phases should never be short-circuited, and the output inductive currents should never be interrupted), which implies that the sum of all the S_{kj} of each one of the matrix, k rows, must always equal to 1 (Eq. (35.171)):

$$\mathbf{S}=\begin{bmatrix}S_{11} & S_{12} & S_{13}\\ S_{21} & S_{22} & S_{23}\\ S_{31} & S_{32} & S_{33}\end{bmatrix} \quad \sum_{j=1}^{3}S_{kj}=1 \quad k,j\in\{1,2,3\} \quad (35.171)$$

Based on matrix **S**, output voltages related to input neutral v_{on_1}, v_{on_2}, and v_{on_3} and line voltages $v_{o_{12}}$, $v_{o_{23}}$, and $v_{o_{31}}$ can be expressed in terms of matrix converter input phase voltages v_{i_1}, v_{i_2}, and v_{i_3}. Input currents i_{i_1}, i_{i_2}, and i_{i_3} can be expressed as a function of output currents i_{o_1}, i_{o_2}, and i_{o_3}:

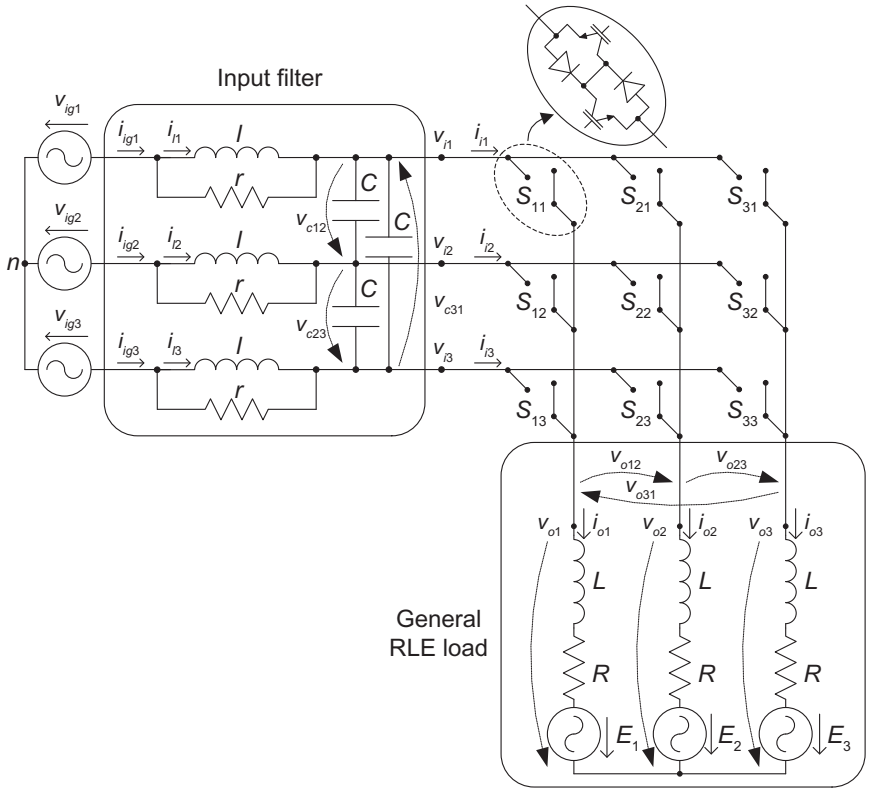


FIG. 35.64 AC/AC matrix converter with input *lCr* filter.

TABLE 35.6 Switching combinations and output line voltage/input current state-space vectors

Group	Name	v_{on1}	v_{on2}	v_{on3}	v_{o12}	v_{o23}	v_{o31}	i_{i1}	i_{i2}	i_{i3}	V_{ol}	δ_o	I_i	μ_i
I	1 g	v_{i1}	v_{i2}	v_{i3}	v_{i12}	v_{i23}	v_{i31}	i_{o1}	i_{o2}	i_{o3}	v_i	δ_i	i_o	μ_o
	2 g	v_{i1}	v_{i3}	v_{i2}	$-v_{i31}$	$-v_{i23}$	$-v_{i12}$	i_{o1}	i_{o3}	i_{o2}	$-v_i$	$-\delta_i+4\pi/3$	i_o	$-\mu_o$
	3 g	v_{i2}	v_{i1}	v_{i3}	$-v_{i12}$	$-v_{i31}$	$-v_{i23}$	i_{o2}	i_{o1}	i_{o3}	$-v_i$	$-\delta_i$	i_o	$-\mu_o+2\pi/3$
	4 g	v_{i2}	v_{i3}	v_{i1}	v_{i23}	v_{i31}	v_{i12}	i_{o3}	i_{o1}	i_{o2}	v_i	$\delta_i+4\ \pi/3$	i_o	$\mu_o+2\pi/3$
	5 g	v_{i3}	v_{i1}	v_{i2}	v_{i31}	v_{i12}	v_{i23}	i_{o2}	i_{o3}	i_{o1}	v_i	$\delta_i+2\ \pi/3$	i_o	$\mu_o+4\pi/3$
	6 g	v_{i3}	v_{i2}	v_{i1}	$-v_{i23}$	$-v_{i12}$	$-v_{i31}$	i_{o3}	i_{o2}	i_{o1}	$-v_i$	$-\delta_i+2\ \pi/3$	i_o	$-\mu_o+4\pi/3$
II	+1	v_{i1}	v_{i2}	v_{i2}	v_{i12}	0	$-v_{i12}$	i_{o1}	$-i_{o1}$	0	$2/\sqrt{3}\ v_{i12}$	$\pi/6$	$2/\sqrt{3}\ i_{o1}$	$-\pi/6$
	–1	v_{i2}	v_{i1}	v_{i1}	$-v_{i12}$	0	v_{i12}	$-i_{o1}$	i_{o1}	0	$-2/\sqrt{3}\ v_{i12}$	$\pi/6$	$-2/\sqrt{3}\ i_{o1}$	$-\pi/6$
	+2	v_{i2}	v_{i3}	v_{i3}	v_{i23}	0	$-v_{i23}$	0	i_{o1}	$-i_{o1}$	$2/\sqrt{3}\ v_{i23}$	$\pi/6$	$2/\sqrt{3}\ i_{o1}$	$\pi/2$
	–2	v_{i3}	v_{i2}	v_{i2}	$-v_{i23}$	0	v_{i23}	0	$-i_{o1}$	i_{o1}	$-2/\sqrt{3}\ v_{i23}$	$\pi/6$	$-2/\sqrt{3}\ i_{o1}$	$\pi/2$
	+3	v_{i3}	v_{i1}	v_{i1}	v_{i31}	0	$-v_{i31}$	$-i_{o1}$	0	i_{o1}	$2/\sqrt{3}\ v_{i31}$	$\pi/6$	$2/\sqrt{3}\ i_{o1}$	$7\pi/6$
	–3	v_{i1}	v_{i3}	v_{i3}	$-v_{i31}$	0	v_{i31}	i_{o1}	0	$-i_{o1}$	$-2/\sqrt{3}\ v_{i31}$	$\pi/6$	$-2/\sqrt{3}\ i_{o1}$	$7\pi/6$
	+4	v_{i2}	v_{i1}	v_{i2}	$-v_{i12}$	v_{i12}	0	i_{o2}	$-i_{o2}$	0	$2/\sqrt{3}\ v_{i12}$	$5\pi/6$	$2/\sqrt{3}\ i_{o2}$	$-\pi/6$
	–4	v_{i1}	v_{i2}	v_{i1}	v_{i12}	$-v_{i12}$	0	$-i_{o2}$	i_{o2}	0	$-2/\sqrt{3}\ v_{i12}$	$5\pi/6$	$-2/\sqrt{3}\ i_{o2}$	$-\pi/6$
	+5	v_{i3}	v_{i2}	v_{i3}	$-v_{i23}$	v_{i23}	0	0	i_{o2}	$-i_{o2}$	$2/\sqrt{3}\ v_{i23}$	$5\pi/6$	$2/\sqrt{3}\ i_{o2}$	$\pi/2$
	–5	v_{i2}	v_{i3}	v_{i2}	v_{i23}	$-v_{i23}$	0	0	$-i_{o2}$	i_{o2}	$-2/\sqrt{3}\ v_{i23}$	$5\pi/6$	$-2/\sqrt{3}\ i_{o2}$	$\pi/2$
	+6	v_{i1}	v_{i3}	v_{i1}	$-v_{i31}$	v_{i31}	0	$-i_{o2}$	0	i_{o2}	$2/\sqrt{3}\ v_{i31}$	$5\pi/6$	$2/\sqrt{3}\ i_{o2}$	$7\pi/6$
	–6	v_{i3}	v_{i1}	v_{i3}	v_{i31}	$-v_{i31}$	0	i_{o2}	0	$-i_{o2}$	$-2/\sqrt{3}\ v_{i31}$	$5\pi/6$	$-2/\sqrt{3}\ i_{o2}$	$7\pi/6$
	+7	v_{i2}	v_{i2}	v_{i1}	0	v_{i12}	v_{i12}	i_{o3}	$-i_{o3}$	0	$2/\sqrt{3}\ v_{i12}$	$3\pi/2$	$2/\sqrt{3}\ i_{o3}$	$-\pi/6$
	–7	v_{i1}	v_{i1}	v_{i2}	0	v_{i12}	v_{i12}	$-i_{o3}$	i_{o3}	0	$-2/\sqrt{3}\ v_{i12}$	$3\pi/2$	$-2/\sqrt{3}\ i_{o3}$	$-\pi/6$
	+8	v_{i3}	v_{i3}	v_{i2}	0	$-v_{i23}$	v_{i23}	0	i_{o3}	$-i_{o3}$	$2/\sqrt{3}\ v_{i23}$	$3\pi/2$	$2/\sqrt{3}\ i_{o3}$	$\pi/2$
	–8	v_{i2}	v_{i2}	v_{i3}	0	v_{i23}	$-v_{i23}$	0	$-i_{o3}$	i_{o3}	$-2/\sqrt{3}\ v_{i23}$	$3\pi/2$	$-2/\sqrt{3}\ i_{o3}$	$\pi/2$
	+9	v_{i1}	v_{i1}	v_{i3}	0	$-v_{i31}$	v_{i31}	$-i_{o3}$	0	i_{o3}	$2/\sqrt{3}\ v_{i31}$	$3\pi/2$	$2/\sqrt{3}\ i_{o3}$	$7\pi/6$
	–9	v_{i3}	v_{i3}	v_{i1}	0	v_{i31}	$-v_{i31}$	i_{o3}	0	$-i_{o3}$	$-2/\sqrt{3}\ v_{i31}$	$3\pi/2$	$-2/\sqrt{3}i_{o3}$	$7\pi/6$
III	z_1	v_{i1}	v_{i1}	v_{i1}	0	0	0	0	0	0	0	–	0	–
	z_2	v_{i2}	v_{i2}	v_{i2}	0	0	0	0	0	0	0	–	0	–
	z_3	v_{i3}	v_{i3}	v_{i3}	0	0	0	0	0	0	0	–	0	–

$$\begin{bmatrix} v_{on_1} \\ v_{on_2} \\ v_{on_3} \end{bmatrix} = \mathbf{S} \begin{bmatrix} v_{i_1} \\ v_{i_2} \\ v_{i_3} \end{bmatrix}$$
$$\begin{bmatrix} v_{o_{12}} \\ v_{o_{23}} \\ v_{o_{31}} \end{bmatrix} = \begin{bmatrix} S_{11}-S_{21} & S_{12}-S_{22} & S_{13}-S_{23} \\ S_{21}-S_{31} & S_{22}-S_{32} & S_{23}-S_{33} \\ S_{31}-S_{11} & S_{32}-S_{12} & S_{33}-S_{13} \end{bmatrix} \begin{bmatrix} v_{i_1} \\ v_{i_2} \\ v_{i_3} \end{bmatrix} \quad (35.172)$$
$$\begin{bmatrix} i_{i_1} \\ i_{i_2} \\ i_{i_3} \end{bmatrix} = \mathbf{S}^T \begin{bmatrix} i_{o_1} \\ i_{o_2} \\ i_{o_3} \end{bmatrix}$$

The application of Concordia transformation $[X_{\alpha,\beta,0}]^{\mathrm{T}} = \mathbf{C}^{\mathrm{T}} [X_{1,2,3}]^{\mathrm{T}}$ to the output line-to-line voltages of Eq. (35.172) results in the output voltage vector:

$$\mathbf{v_{ol_{\alpha\beta}}} = \begin{bmatrix} v_{ol_\alpha} \\ v_{ol_\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} S_{11}-S_{21} & S_{12}-S_{22} & S_{13}-S_{23} \\ S_{21}-S_{31} & S_{22}-S_{32} & S_{23}-S_{33} \\ S_{31}-S_{11} & S_{32}-S_{12} & S_{33}-S_{13} \end{bmatrix} \begin{bmatrix} v_{i_1} \\ v_{i_2} \\ v_{i_3} \end{bmatrix}$$
$$= \begin{bmatrix} \rho_{v_{\alpha\alpha}} & \rho_{v_{\alpha\beta}} \\ \rho_{v_{\beta\alpha}} & \rho_{v_{\beta\beta}} \end{bmatrix} \begin{bmatrix} v_{ic_\alpha} \\ v_{ic_\beta} \end{bmatrix} \quad (35.173)$$

where $v_{ic\alpha\beta}$ is the input filter capacitor voltage and $\rho_{v_{\alpha\alpha}}$, $\rho_{v_{\alpha\beta}}$, $\rho_{v_{\beta\alpha}}$, and $\rho_{v_{\beta\beta}}$ are functions of the ON/OFF state of the nine S_{kj} switches:

$$\begin{bmatrix} \rho_{v_{\alpha\alpha}} & \rho_{v_{\alpha\beta}} \\ \rho_{v_{\beta\alpha}} & \rho_{v_{\beta\beta}} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} (S_{11}-S_{21}-S_{12}+S_{22}) \\ \sqrt{3}(S_{11}+S_{21}-2S_{31}-S_{12}-S_{22}+2S_{32}) \\ \sqrt{3}(S_{11}-S_{21}+S_{12}-S_{22}) \\ (S_{11}+S_{21}-2S_{31}+S_{12}+S_{22}+2S_{32}) \end{bmatrix} \quad (35.174)$$

The average value $\overline{v_{ol_{\alpha\beta}}}$ of the output line-to-line voltages, in $\alpha\beta$ coordinates, during one switching period, is the output variable to be controlled (since $v_{ol\alpha\beta}$ is discontinuous) [23,50]:

$$\overline{v_{ol_{\alpha\beta}}} = \frac{1}{T_s} \int_{nT_s}^{(n+1)T_s} v_{ol_{\alpha\beta}} \mathrm{d}t \quad (35.175)$$

Considering the control goal $\overline{v_{ol_{\alpha\beta}}} = \overline{v_{ol_{\alpha\beta\,ref}}}$, the sliding surface $S(e_{\alpha\beta}, t)(k_{\alpha\beta} > 0)$ is

$$S(e_{\alpha\beta}, t) = \frac{k_{\alpha\beta}}{T} \int_0^T \left(v_{ol_{\alpha\beta_{ref}}} - v_{ol_{\alpha\beta}} \right) \mathrm{d}t = 0 \quad (35.176)$$

The first derivative of Eq. (35.176) is

$$\dot{S}(e_{\alpha\beta}, t) = k_\alpha \left(v_{ol_{\alpha\beta ref}} - v_{ol_{\alpha\beta}} \right) \quad (35.177)$$

As the sliding-mode stability is guaranteed if $S_{\alpha\beta}(e_{\alpha\beta}, t)\, \dot{S}_{\alpha\beta}(e_{\alpha\beta}, t) < 0$, the criterion to choose the output line voltages state-space vectors is

$$\begin{aligned} S_{\alpha\beta}(e_{\alpha\beta}, t) < 0 \;\Rightarrow\; \dot{S}_{\alpha\beta}(e_{\alpha\beta}, t) > 0 \;\Rightarrow\; v_{ol_{\alpha\beta}} < v_{ol_{\alpha\beta\,ref}} \\ S_{\alpha\beta}(e_{\alpha\beta}, t) > 0 \;\Rightarrow\; \dot{S}_{\alpha\beta}(e_{\alpha\beta}, t) < 0 \;\Rightarrow\; v_{ol_{\alpha\beta}} > v_{ol_{\alpha\beta\,ref}} \end{aligned} \quad (35.178)$$

This implies that the sliding mode is reached only when the vector applied to the converter has the desired amplitude and phase.

According to Table 35.6, the six vectors of group I have fixed amplitude but time-varying phase, the 18 vectors of group II have variable amplitude, and the vectors of group III are null. Therefore, from the load viewpoint, the 18 highest amplitude vectors (6 vectors from group I and 12 vectors from group II) and one null vector are suitable to guarantee the sliding-mode stability.

Therefore, if two three-level comparators ($C_{\alpha\beta} \in \{-1, 0, 1\}$) are used to quantize the deviations of Eq. (35.178) from zero, the nine output voltage error combinations (3^3) are not enough to guarantee the choice of all the 19 available vectors. The extra vectors may be used to control the input power factor. As an example, if the output voltage error is quantized as $C_\alpha = 1$ and $C_\beta = 1$, at sector V_i1 (Fig. 35.65), the vectors −3, +1, or 1 g might be used to control the output voltage. The final choice would depend on the input current error.

Output current control

For some applications, it is more useful to control the output currents, which implies some changes on the previously designed controllers. From Fig. 35.64, the output currents can be obtained as a function of the phase voltages applied to the load:

$$\begin{cases} \dfrac{di_{o_\alpha}}{dt} = -\dfrac{R}{L} i_{o_\alpha} + \dfrac{1}{L} v_{o_\alpha} + \dfrac{1}{L} E_\alpha \\ \dfrac{di_{o_\beta}}{dt} = -\dfrac{R}{L} i_{o_\beta} + \dfrac{1}{L} v_{o_\beta} + \dfrac{1}{L} E_\beta \end{cases} \quad (35.179)$$

As the output currents are state variables, with a strong relative degree of 1, the sliding surfaces should depend directly on their errors:

$$S_{io_{\alpha\beta}}(e_{io_{\alpha\beta}}, t) = k_{i_o} \left(i_{o_{\alpha\beta ref}} - i_{o_{\alpha\beta}} \right) \quad (35.180)$$

The state-space vectors should be chosen to guarantee the stability criterion $S_{io_{\alpha\beta}}(e_{io_{\alpha\beta}}, t)\ \dot{S}_{io_{\alpha\beta}}(e_{io_{\alpha\beta}}, t) < 0$, according to the following:

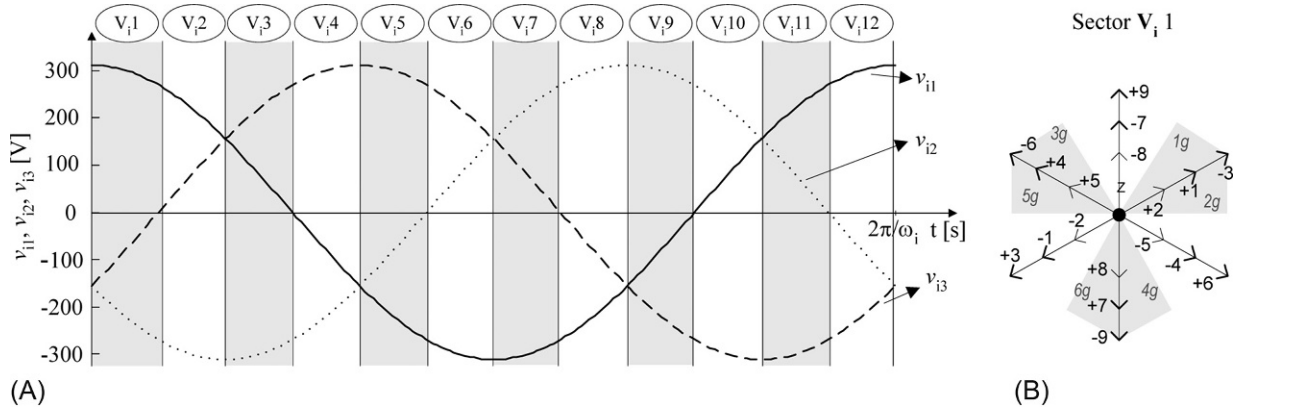


FIG. 35.65 (A) Input voltages and their corresponding sector and (B) representation of the output voltage state-space vectors when the input voltages are located at sector V_i1.

(a) If $S_{io_{\alpha\beta}}\left(e_{io_{\alpha\beta}}, t\right) < 0$, then $i_{o_{\alpha\beta}} > i_{o_{\alpha\beta ref}}$ and the output current must decrease $i_{o_{\alpha\beta}} \downarrow$. This means that the chosen output voltage $v_{o_{\alpha\beta}}$ phase vector should be low enough to guarantee $\mathrm{d}i_{o_{\alpha\beta}}/\mathrm{d}t < 0$.

(b) If $S_{io_{\alpha\beta}}\left(e_{io_{\alpha\beta}}, t\right) > 0$, then $i_{o_{\alpha\beta}} < i_{o_{\alpha\beta ref}}$ and the output current must increase $i_{o_{\alpha\beta}} \uparrow$. This means that the chosen output voltage $v_{o_{\alpha\beta}}$ phase vector should be high enough to guarantee $\mathrm{d}i_{o_{\alpha\beta}}/\mathrm{d}t > 0$.

The output voltage phase vectors can be obtained from the output voltage line vectors of Table 35.6, using the well-known relations between three-phase line and phase voltages:

$$\mathbf{V_o} = \begin{bmatrix} v_{o_1} & v_{o_2} & v_{o_3} \end{bmatrix}^T = \left[\frac{2v_{o_{12}} + v_{o_{23}}}{3} \quad \frac{2v_{o_{23}} + v_{o_{31}}}{3} \quad \frac{2v_{o_{31}} + v_{o_{12}}}{3} \right]^T \tag{35.181}$$

As expected, the resultant output voltage phase vectors will have an amplitude $\sqrt{3}$ lower than the voltage line vectors of Table 35.6 and a lagging phase of $\pi/6$. As an example, from Fig. 35.65B, this will result in a $-\pi/6$ rotation of all the voltage vectors represented.

Therefore, if two three-level comparators ($C_{\alpha\beta} \in \{-1,0,1\}$) are used to quantize the deviations of Eq. (35.180) from zero and if the output current error is quantized as $C_\alpha = 1$ and $C_\beta = 1$, at sector V_i1 (Fig. 35.65), the vectors +9 or −7 might be used to control the output current. The final choice would depend on the input current error.

Input power factor control

Assuming that the source is a balanced sinusoidal three-phase voltage supply with frequency ω_i, the switched state-space model equations of the converter input filter are obtained in 123 coordinates:

$$\begin{cases} \dfrac{\mathrm{d}i_{l_1}}{\mathrm{d}t} = \dfrac{1}{3l}v_{c23} + \dfrac{2}{3l}v_{c31} + \dfrac{1}{l}v_{ig_1} \\ \dfrac{\mathrm{d}i_{l_2}}{\mathrm{d}t} = -\dfrac{2}{3l}v_{c23} - \dfrac{1}{3l}v_{c31} + \dfrac{1}{l}v_{ig_2} \\ \dfrac{\mathrm{d}v_{c23}}{\mathrm{d}t} = \dfrac{1}{3C}i_{l_1} + \dfrac{2}{3C}i_{l_2} - \dfrac{1}{3Cr}v_{c23} + \dfrac{1}{3Cr}v_{ig_1} + \dfrac{2}{3Cr}v_{ig_2} \\ \qquad - \dfrac{1}{3C}(S_{11} - S_{31} + 2S_{12} - 2S_{32})\, i_{o_1} \\ \qquad - \dfrac{1}{3C}(S_{21} - S_{31} + 2S_{22} - 2S_{32})\, i_{o_2} \\ \dfrac{\mathrm{d}v_{c31}}{\mathrm{d}t} = -\dfrac{2}{3C}i_{l_1} - \dfrac{1}{3C}i_{l_2} - \dfrac{1}{3Cr}v_{c31} - \dfrac{2}{3Cr}v_{ig_1} - \dfrac{1}{3Cr}v_{ig_2} \\ \qquad + \dfrac{1}{3C}(2S_{11} - 2S_{31} + S_{12} - S_{32})\, i_{o_1} \\ \qquad + \dfrac{1}{3C}(2S_{21} - 2S_{31} + S_{22} - S_{32})\, i_{o_2} \end{cases} \tag{35.182}$$

To control the input power factor, a reference frame synchronous with input voltage v_{ig1} may be used applying the Blondel-Park transformation to the matrix converter switched state-space model (Eq. (35.183)), where $\rho_{i_{dd}}$, $\rho_{i_{dq}}$, $\rho_{i_{qd}}$, and $\rho_{i_{qq}}$ are functions of the on/off states of the nine S_{kj} switches:

$$\begin{cases} \dfrac{\mathrm{d}i_{l_d}}{\mathrm{d}t} = \omega_i i_{lq} - \dfrac{1}{2l}v_{c_d} - \dfrac{1}{2\sqrt{3}l}v_{c_q} + \dfrac{1}{l}v_{ig_d} \\ \dfrac{\mathrm{d}i_{l_q}}{\mathrm{d}t} = -\omega_i i_{l_d} + \dfrac{1}{2\sqrt{3}l}v_{c_d} - \dfrac{1}{2l}v_{c_q} + \dfrac{1}{l}v_{ig_q} \\ \dfrac{\mathrm{d}v_{c_d}}{\mathrm{d}t} = \dfrac{1}{2C}i_{l_d} - \dfrac{1}{2\sqrt{3}C}i_{l_q} - \dfrac{1}{3Cr}v_{c_d} + \omega_i v_{c_q} + \dfrac{-\rho_{i_{dd}} + \left(\rho_{i_{qd}}/\sqrt{3}\right)}{2C}i_{o_d} \\ \qquad + \dfrac{-\rho_{i_{dq}} + \left(\rho_{i_{qq}}/\sqrt{3}\right)}{2C}i_{o_q} + \dfrac{1}{2Cr}v_{ig_d} - \dfrac{1}{2\sqrt{3}Cr}v_{ig_q} \\ \dfrac{\mathrm{d}v_{c_q}}{\mathrm{d}t} = \dfrac{1}{2\sqrt{3}C}i_{l_d} + \dfrac{1}{2C}i_{l_q} - \omega_i v_{c_d} - \dfrac{1}{3Cr}v_{c_q} + \dfrac{-\left(\rho_{i_{dd}}/\sqrt{3}\right) - \rho_{i_{qd}}}{2C}i_{o_d} \\ \qquad + \dfrac{-\left(\rho_{i_{dq}}/\sqrt{3}\right) - \rho_{i_{qq}}}{2C}i_{o_q} + \dfrac{1}{2\sqrt{3}Cr}v_{ig_d} + \dfrac{1}{2Cr}v_{ig_q} \end{cases} \tag{35.183}$$

As a consequence, neglecting ripples, all the input variables become time invariant, allowing a better understanding of the sliding-mode controller design, and the choice of the most adequate state-space vector. Using this state-space model, the input i_{igd} and i_{igq} currents are

$$\begin{cases} i_{ig_d} = i_{l_d} + \dfrac{l}{r}\left(\dfrac{di_{l_d}}{dt} - \omega_i i_{l_q}\right) \\ i_{ig_q} = i_{l_q} + \dfrac{l}{r}\left(\dfrac{di_{l_q}}{dt} + \omega_i i_{l_d}\right) \end{cases} \Leftrightarrow \begin{cases} i_{ig_d} = i_{l_d} - \dfrac{1}{2r}v_{c_d} - \dfrac{1}{2\sqrt{3}r}v_{c_q} + \dfrac{1}{r}v_{ig_d} \\ i_{ig_q} = i_{l_q} + \dfrac{1}{2\sqrt{3}r}v_{c_d} - \dfrac{1}{2r}v_{c_q} + \dfrac{1}{r}v_{ig_q} \end{cases} \tag{35.184}$$

The input power factor controller should consider the input-output power constraint (Eq. (35.185)) (the converter losses and ripples are neglected), obtained as a function of the input and output voltages and currents (the input voltage v_{igq} is equal to zero in the chosen dq rotating frame). The choice of one output voltage vector automatically defines the instantaneous value of the input $i_{igd}(t)$ current:

$$v_{ig_d} i_{ig_d} \approx \frac{1}{3}\left(\frac{\sqrt{3}}{2}v_{ol_d} + \frac{1}{2}v_{ol_q}\right) i_{o_d} + \frac{1}{3}\left(-\frac{1}{2}v_{ol_d} + \frac{\sqrt{3}}{2}v_{ol_q}\right) i_{o_q} \tag{35.185}$$

Therefore, only the sliding surface associated to the i_{igq} current is needed, expressed as a function of the system state variables and based on the state-space model determined in Eq. (35.183):

$$\begin{aligned} \frac{di_{ig_q}}{dt} = &-\omega_i i_{l_d} - \frac{1}{3Cr} i_{l_q} + \left(-\frac{1}{6\sqrt{3}Cr^2} + \frac{\omega_i}{2r} + \frac{1}{2\sqrt{3}l}\right) v_{c_d} \\ &+ \left(\frac{\omega_i}{2\sqrt{3}r} + \frac{1}{6Cr^2} - \frac{1}{2l}\right) v_{c_q} + \frac{1}{3Cr}\left(\rho_{i_{qd}} i_{o_d} + \rho_{i_{qq}} i_{o_q}\right) \\ &+ \left(-\frac{1}{3Cr^2} + \frac{1}{l}\right) v_{ig_q} + \frac{1}{r}\frac{dv_{ig_q}}{dt} \end{aligned} \tag{35.186}$$

As the derivative of the input $i_{igq}(t)$ current depends directly on the control variables $\rho_{i_{qd}}$ and $\rho_{i_{qq}}$, the sliding function $S_{i_q}(e_{i_q}, t)$ will depend only on the input current error $e_{i_q} = i_{ig_{qref}} - i_{ig_q}$:

$$S_{i_q}(e_{i_q}, t) = k_{i_q}\left(i_{ig_{qref}} - i_{ig_q}\right) \tag{35.187}$$

As the sliding-mode stability is guaranteed if $S_{i_q}(e_{i_q}, t)\,\dot{S}_{i_q}(e_{i_q}, t) < 0$, the criterion to choose the state-space vectors is [23]

$$\begin{aligned} &S_{i_q}(e_{i_q}t) > 0 \;\Rightarrow\; \dot{S}_{i_q}(e_{i_q}t) < 0 \;\Rightarrow\; \frac{di_{ig_q}}{dt} > \frac{di_{ig_{qref}}}{dt} \;\Rightarrow\; i_{ig_q}\uparrow \\ &S_{i_q}(e_{i_q}t) < 0 \;\Rightarrow\; \dot{S}_{i_q}(e_{i_q}t) > 0 \;\Rightarrow\; \frac{di_{ig_q}}{dt} < \frac{di_{ig_{qref}}}{dt} \;\Rightarrow\; i_{ig_q}\downarrow \end{aligned} \tag{35.188}$$

Also, to choose the adequate input current vector, it is necessary (a) to know the location of the output currents, as the input currents depend on the output currents location (Table 35.6), and (b) to know the dq frame location. As in the chosen frame (synchronous with the v_{ig1} input voltage), the dq-axis location depends on the v_{ig1} input voltage location; the sign of the input current vector i_{igq} component can be determined knowing the location of the input voltages and the location of the output currents (Fig. 35.66).

Considering the previous example, at sector V_i1 (Fig. 35.65), for an error of $C_\alpha = 1$ and $C_\beta = 1$, vector −3, +1, or 1 g might be used to control the output voltage. When compared, at sector I_o1 (Fig. 35.66B), these three vectors have positive i_d components and, as a result, will have a similar effect on the input i_{igd} current. However, they have a different effect on the i_{igq} current: Vector −3 has a positive i_{iq} component, vector +1 has a negative i_{iq} component, and vector 1 g has a nearly zero i_{iq} component. As a result, if the output voltage errors are $C_\alpha = 1$ and $C_\beta = 1$, at sectors V_i1 and I_o1, vector −3 should be chosen if the input current error is quantized as $C_{iq} = 1$ (Fig. 35.66B), vector +1 should be chosen if the input current error is quantized as $C_{iq} = -1$, and if the input current error is $C_{iq} = 0$, vector 1 g or −3 might be used.

When the output voltage errors are quantized as zero $C_{\alpha\beta} = 0$, the null vectors of group III should be used only if the input current error is $C_{iq} = 0$. Otherwise (being $C_{i_q} \neq 0$),

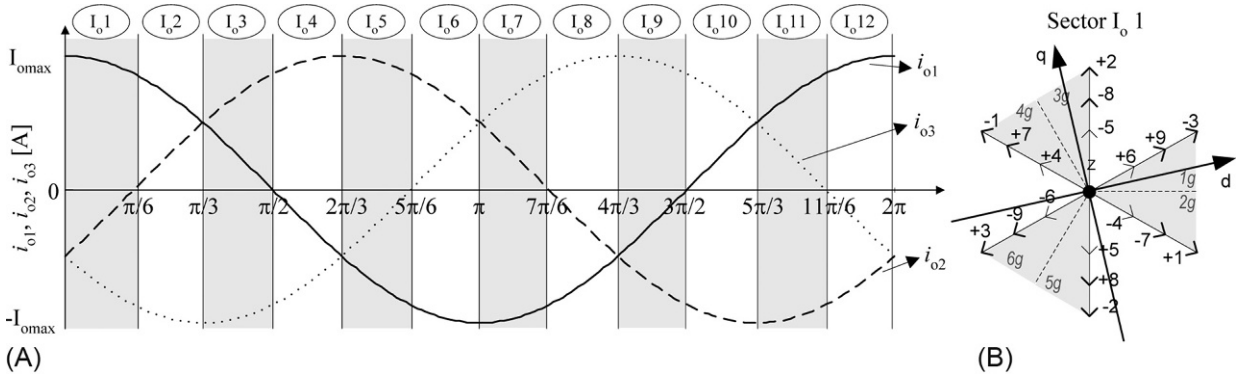


FIG. 35.66 (A) Output currents and their corresponding sector and (B) representation of input current state-space vectors, when the output currents are located at sector I_o1. The dq-axis is represented considering that the input voltages are located in zone V_i1.

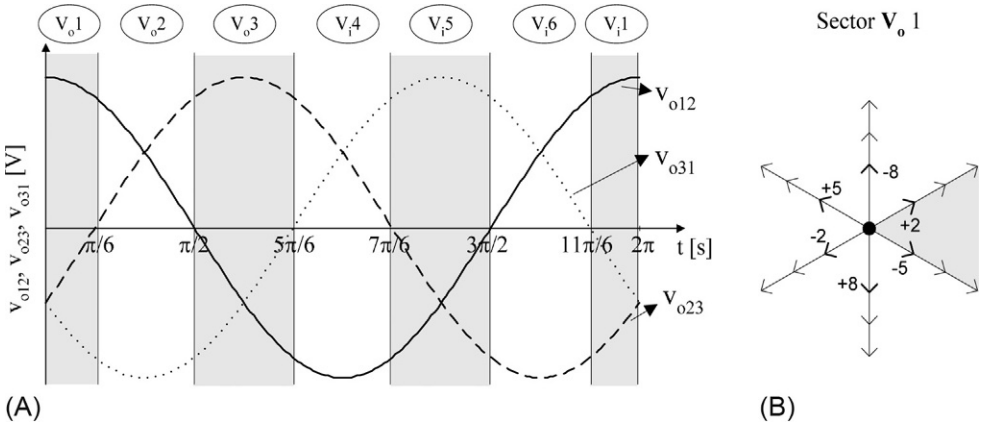


FIG. 35.67 (A) Output voltages and their corresponding sector and (B) representation of the lowest amplitude output voltage vectors, when the input voltages are located at sector V_o1.

the lowest amplitude voltage vectors ({+2, −8, +5, −2, +8, −5} at sector V_i1 of Fig. 35.65B) that were not used to control the output voltages might be chosen to control the input i_{igq} current as these vectors may have a strong influence on the input i_{igq} current component (Fig. 35.66B).

To choose one of these six vectors, only the vectors located as near as possible to the output voltages sector (Fig. 35.67) are chosen (to minimize the output voltage ripple), and a five-level comparator is enough. As a result, there will be $9 \times 5 = 45$ error combinations to select 27 space vectors. Therefore, the same vector may have to be used for more than one error combination.

With this reasoning, it is possible to obtain Table 35.7 for sector V_i1, I_o1, and V_o1 and generalize it for all the other sectors.

The experimental results shown in (Fig. 35.68) were obtained with a low-power prototype (1 kW), with two three-level comparators and one five-level comparator. The transistors IGBT were switched at frequencies near 10 kHz.

The results show the response to a step on the output voltage reference (Fig. 35.68A) and on the input reference current (Fig. 35.68B), for a three-phase output load (R = 7 Ω and $L = 15$ mH), with $k_{\alpha\beta} = 100$ and $k_{iq} = 2$. It can be seen that the matrix converter may operate with a near unity input power factor (Fig. 35.68A – $f_o = 20$ Hz) or with lead/lag power factor (Fig. 35.68B), guaranteeing very low ripple on the output currents, a good tracking capability and fast transient response times.

Also, some simulation results were obtained for the output current-controlled matrix converter. The results (Fig. 35.69A) show the response to a step on the output current reference at $t = 0.22$ s, a step of the output current frequency at $t = 0.28$ s, and a step at the input i_{ig_q} current at $t = 0.34$ s, for a three-phase output load ($R = 3\ \Omega$ and $L = 30$ mH), with $k_{io\alpha\beta} = 10$ and $k_{iq} = 2$. Again, these results show that matrix converter may operate with lead/lag power factor, guaranteeing very low ripple on the output currents, a good tracking capability and fast transient response times for both input and output currents.

TABLE 35.7 State-space vector choice at sector V_i1, I_o1, and V_o1

C_α	C_β	C_{iq}				
		−2	**−1**	**0**	**1**	**2**
−1	**−1**	+3	+3	+3	−1	−1
−1	**0**	5 g	+3	−6	−1	−1
−1	**1**	−6	−6	−6	+4	3 g
0	**−1**	6 g	−9	−9	+7	4 g
0	**0**	+8	+8	0	−5	+2
0	**1**	−7	−7	+9	+9	+9
1	**−1**	−4	−4	+6	+6	+6
1	**0**	+1	+1	+6	−3	−3
1	**1**	+1	+1	1 g	−3	−3

35.3.5.8 Example 35.18: PI Linear Controllers for Matrix Converters

For comparison purposes, a PI-based controller using a pulse-width-modulation (PWM) technique is designed. From Eq (35.171), the modulation indexes m_{ij} associated to the matrix converter with nine switches are represented as a nine-element matrix $\mathbf{M}(t)$ (Eq. (35.189)) [24]:

$$\mathbf{M}(t) = \begin{bmatrix} m_{11}(t) & m_{12}(t) & m_{13}(t) \\ m_{21}(t) & m_{22}(t) & m_{23}(t) \\ m_{31}(t) & m_{32}(t) & m_{33}(t) \end{bmatrix} \quad \begin{array}{l} \sum_{j=1}^{3} m_{kj}(t) = 1 \\ 0 \le m_{kj}(t) \le 1 \quad k, j \in [1,\ 2,\ 3] \end{array} \tag{35.189}$$

These modulation indexes are used to synthesize the output voltages $\mathbf{V_{on}}(t) = [v_{on_1}(t)\ \ v_{on_2}(t)\ \ v_{on_3}(t)]^T$ as a function of input voltages $\mathbf{V_i}(t) = [v_{i_1}(t)\ \ v_{i_2}(t)\ \ v_{i_3}(t)]^T$ Eq. (35.190) and input currents $\mathbf{I_i}(t) = [i_{i_1}(t)\ \ i_{i_2}(t)\ \ i_{i_3}(t)]^T$ as a function of output load currents $\mathbf{I_o}(t) = [i_{o_1}(t)\ \ i_{o_2}(t)\ \ i_{o_3}(t)]^T$ Eq. (35.190):

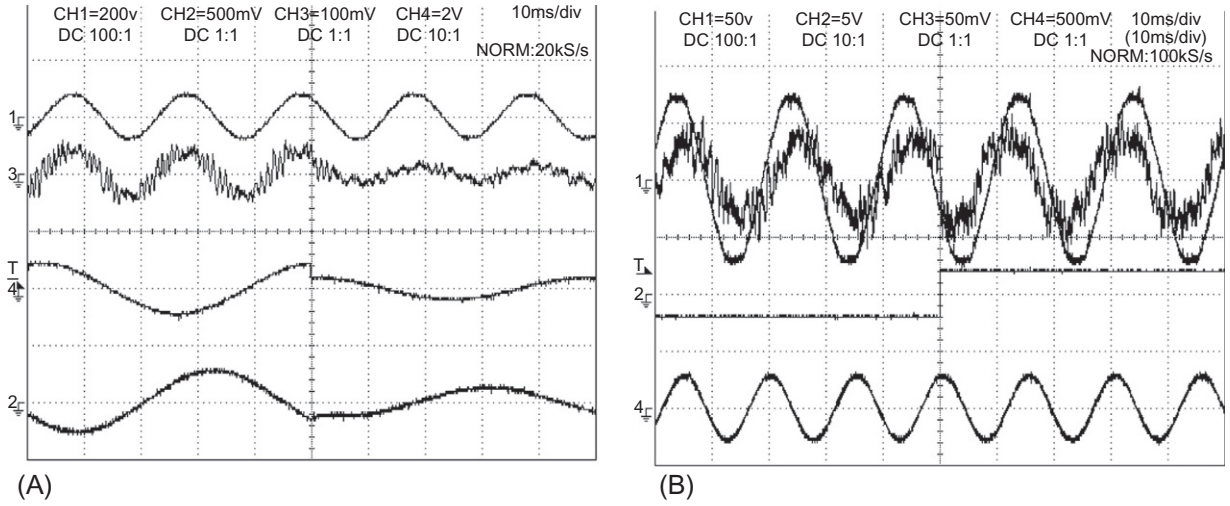


FIG. 35.68 Dynamic responses obtained with a three-phase load: (A) output reference voltage step ($R=7\ \Omega$, $L=15$ mH, and $f_o=20$ Hz): input voltage $v_{ig1}(t)$ (CH1), input current $i_{ig1}(t)$ (CH3), output reference voltage $v_{o23ref}(t)$ (CH4), and output current $i_{o1}(t)$ (CH2) and (B) input reference current $i_{igqref}(t)$ step: input voltage $v_{ig1}(t)$ (CH1), input current $i_{ig1}(t)$ (CH3), input reference current $i_{igqref}(t)$ (CH2), and output current $i_{o1}(t)$ (CH4).

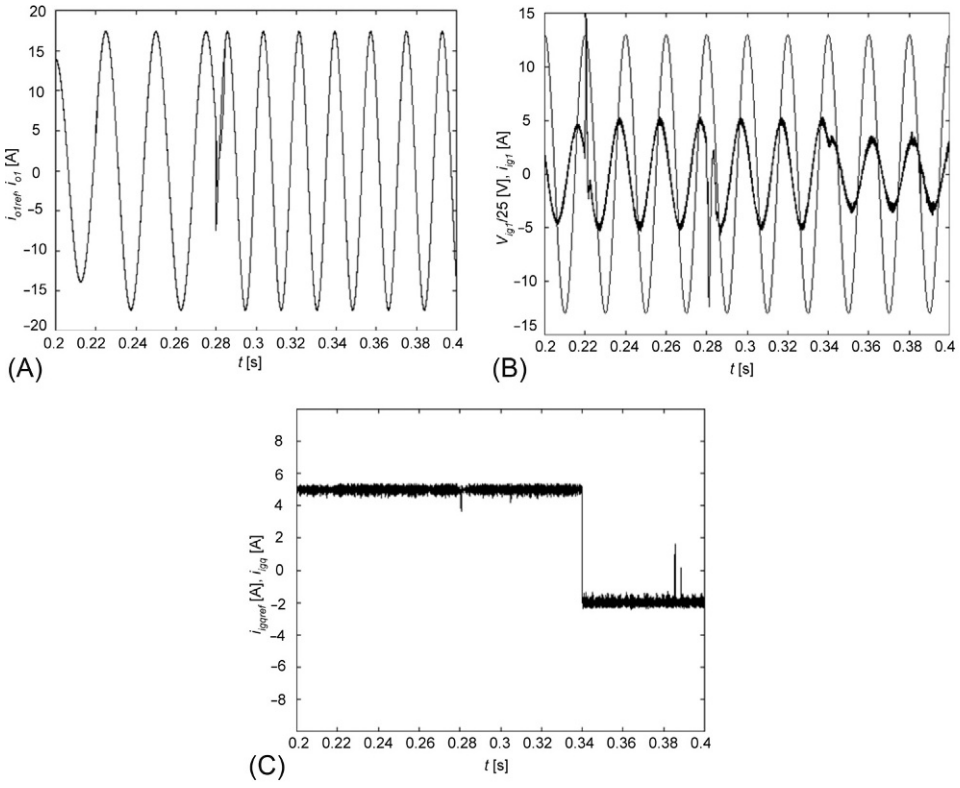


FIG. 35.69 Dynamic responses obtained with a three-phase load ($R=3\ \Omega$ and $L=30$ mH) for a step in the output reference current amplitude at $t=0.22$ s, in the output reference current frequency at $t=0.28$ s and in the input $i_{igq}(t)$ current at $t=0.34$ s, (A) output reference current $i_{o1ref}(t)$ and output current $i_{o1}(t)$, (B) input grid voltage $v_{ig1}(t)$ and input grid current $i_{ig1}(t)$, and (C) input reference current $i_{igqref}(t)$ and input grid current $i_{igq}(t)$.

$$\begin{aligned}\mathbf{V_{on}}(t) &= \mathbf{M}(t)\ \mathbf{V_i}(t)\\ \mathbf{I_i}(t) &= \mathbf{M}(t)^T\ \mathbf{I_o}(t)\end{aligned} \tag{35.190}$$

However, assuming a balanced source system $\sum_{k=1}^{3} v_{i_k}(t) = 0$ with input and output neutral wires not connected $\sum_{k=1}^{3} i_{i_k}(t) = 0$, $\sum_{k=1}^{3} i_{o_k}(t) = 0$, and restriction (35.189), the modulation index matrix may be reduced to a four element $a_{kj}(t)$ (k, $j = \{1, 2\}$) matrix Eq. (35.191) [25]:

$$\mathbf{M_a} = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix} = \begin{bmatrix} m_{11} - m_{31} & m_{21} - m_{31} \\ m_{12} - m_{32} & m_{22} - m_{32} \end{bmatrix} \tag{35.191}$$

Based on Eq. (35.189), Eq. (35.190), and Eq. (35.191), input currents are obtained as a function of output currents:

$$\begin{bmatrix} i_{i_1} & i_{i_2} \end{bmatrix}^{\mathrm{T}} = \mathbf{M_a} \begin{bmatrix} i_{o_1} & i_{o_2} \end{bmatrix}^{\mathrm{T}} \tag{35.192}$$

From Eq. (35.189) and Eq. (35.190), output load phase voltages Eq. (35.193) can be directly obtained from input phase voltages using a four modulation index matrix Eq. (35.194) based on Eq. (35.191):

$$\begin{bmatrix} v_{o_1} & v_{o_2} \end{bmatrix}^{\mathrm{T}} = \mathbf{M_v} \begin{bmatrix} v_{i_1} & v_{i_2} \end{bmatrix}^{\mathrm{T}} \tag{35.193}$$

$$\mathbf{M_v} = \frac{1}{3} \begin{bmatrix} 4a_{11} - 2a_{12} + 2a_{21} - a_{22} & 2a_{11} - a_{12} + 4a_{21} - 2a_{22} \\ -2a_{11} + 4a_{12} - a_{21} + 2a_{22} & -a_{11} + 2a_{12} - 2a_{21} + 4a_{22} \end{bmatrix} \tag{35.194}$$

Assuming ideal input filtering, phase voltages Eq. (35.195) applied to matrix converter should be approximately equal to grid voltages:

$$v_{i_k}(t) \approx v_{ig_k}(t) = \sqrt{2}\, V_i \cos\left(\omega_i t - 2(k-1)\pi/3\right) \quad k \in [1, 2, 3] \tag{35.195}$$

Also, assuming ideal output filtering, output currents Eq. (35.196) should be nearly equal to their fundamental harmonics (with frequency ω_o and displacement factor ϕ_o):

$$i_{o_k}(t) = \sqrt{2} I_o \cos\left(\omega_o t - \varphi_o - 2(k-1)\pi/3\right) \quad k \in [1, 2, 3] \tag{35.196}$$

If switching frequencies are much higher than input and output frequencies ($f_s \gg f_i$ and $f_s \gg f_o$), then input currents Eq. (35.197) and output load voltages Eq. (35.198) should be approximately equal to their references:

$$i_{i_k}(t) = \sqrt{2} I_i \cos\left(\omega_i t - \varphi_i - 2(k-1)\pi/3\right) \quad k \in [1, 2, 3] \tag{35.197}$$

$$v_{o_k}(t) = \sqrt{2} V_o \cos\left(\omega_o t - 2(k-1)\pi/3\right) \quad k, j \in [1, 2, 3] \tag{35.198}$$

Applying Concordia and Park transformation [26] to Eq. (35.192) and Eq. (35.193) and choosing a reference frame synchronous with input phase voltages ($\Theta_i = \omega_i t$) for all the input variables and a reference frame synchronous with output phase voltages ($\Theta_o = \omega_o t$) for all the output variables, then, three-phase input and output variables (Eq. (35.199) and Eq. (35.200)) may become time invariant:

$$\begin{aligned}\mathbf{T}_{\Theta_o}{}^T\ \mathbf{V}_{\mathbf{o}_{123}} &= \left(\mathbf{T}_{\Theta_o}{}^T \mathbf{M_v}\ \mathbf{T}_{\Theta_i}\right)\ \mathbf{T}_{\Theta_i}{}^T \mathbf{V}_{\mathbf{i}_{123}}\\ \mathbf{V}_{\mathbf{o}_{dq}} &= \mathbf{M_{dq}} \mathbf{V}_{\mathbf{i}_{dq}}\end{aligned} \tag{35.199}$$

$$\begin{aligned}\mathbf{T}_{\Theta_i}{}^T\ \mathbf{I}_{\mathbf{i}_{123}} &= \left(\mathbf{T}_{\Theta_i}{}^T \mathbf{M_a}\ \mathbf{T}_{\Theta_o}\right)\ \mathbf{T}_{\Theta_o}{}^T \mathbf{I}_{o_{123}}\\ \mathbf{I}_{\mathbf{i}_{dq}} &= \mathbf{M}_{\mathbf{dq}}^{\mathbf{T}} \mathbf{I}_{\mathbf{o}_{dq}}\end{aligned} \tag{35.200}$$

From Eqs. (35.199) and (35.200), in the new coordinate frame, input phase voltages should be given by Eq. (35.201), and target input currents should be equal to Eq. (35.202):

$$\begin{bmatrix} v_{i_d} & v_{i_q} \end{bmatrix}^{\mathrm{T}} = \mathbf{T}_{\Theta_i}{}^T \mathbf{V}_{\mathbf{i}_{abc}} = \begin{bmatrix} \sqrt{3} V_i & 0 \end{bmatrix}^{\mathrm{T}} \tag{35.201}$$

$$\begin{bmatrix} i_{i_d} & i_{i_q} \end{bmatrix}^{\mathrm{T}} = \mathbf{T}_{\Theta_i}{}^T\ \mathbf{I}_{\mathbf{i}_{abc}} = \sqrt{3} I_i \begin{bmatrix} \cos(\varphi_i) & -\sin(\varphi_i) \end{bmatrix}^{\mathrm{T}} \tag{35.202}$$

Target output load phase voltages Eq. (35.203) and output currents Eq. (35.204) should be

$$\begin{bmatrix} v_{o_d} & v_{o_q} \end{bmatrix}^{\mathrm{T}} = \mathbf{T}_{\Theta_o}{}^T\ \mathbf{V}_{\mathbf{o}_{abc}} = \begin{bmatrix} \sqrt{3} V_o & 0 \end{bmatrix}^{\mathrm{T}} \tag{35.203}$$

$$\begin{bmatrix} i_{o_d} & i_{o_q} \end{bmatrix}^{\mathrm{T}} = \mathbf{T}_{\Theta_o}{}^T \mathbf{I}_{o_{abc}} = \sqrt{3} I_o \begin{bmatrix} \cos(\varphi_o) & -\sin(\varphi_o) \end{bmatrix}^{\mathrm{T}} \tag{35.204}$$

From Eq. (35.199), in the new coordinate frame, matrix converter modulation indexes are given by Eq. (35.205):

$$\mathbf{M_{dq}} = \mathbf{T}_{\Theta_o}{}^T \mathbf{M_v}\ \mathbf{T}_{\Theta_i} = \begin{bmatrix} \gamma_{dd} & \gamma_{dq} \\ \gamma_{qd} & \gamma_{qq} \end{bmatrix} \tag{35.205}$$

From Eq. (35.199), using input voltages Eq. (35.201), two independent control actions based on different modulation indexes, allowing the independent control of each output voltage component, are obtained:

$$\begin{bmatrix} v_{o_d} & v_{o_q} \end{bmatrix}^{\mathrm{T}} = \sqrt{3} V_i \begin{bmatrix} \gamma_{dd} & \gamma_{qd} \end{bmatrix}^{\mathrm{T}} \tag{35.206}$$

Solving Eq. (35.206) using target output voltages Eq. (35.203), it is possible to calculate γ_{dd} Eq. (35.207) and γ_{qd} Eq. (35.208) modulation indexes:

$$\gamma_{dd} = \frac{V_o}{V_i} \tag{35.207}$$

$$\gamma_{qd} = 0 \tag{35.208}$$

Input/output power constraint can be verified Eq. (35.209) by calculating current $i_{i_d} = \gamma_{dd} i_{o_d} + \gamma_{qd} i_{o_q}$ from Eq. (35.200) and Eq. (35.205), assuming an ideal matrix converter without losses and input/output ideal filtering, using the previously calculated modulation indexes γ_{dd} Eq. (35.207) and γ_{qd} Eq. (35.208), input target currents Eq. (35.202) and output currents Eq. (35.204):

$$V_i I_i \cos(\varphi_i) = V_o I_o \cos(\varphi_o) \tag{35.209}$$

From Eqs. (35.209) and (35.206), it is possible to conclude the following:

(a) Output voltages (Eq. (35.206)) and input i_{i_d} current control depend only on γ_{dd} and γ_{qd} modulation indexes. This shows the well-known nonlinear coupling between output voltages and input currents that results from the input/output active power constraint.
(b) Output voltages and input i_{i_d} current are independent from input i_{i_q} current, which depends only on γ_{dq} and γ_{qq} modulation indexes. This shows that the input power factor is controllable and independent from output voltages control.

From Eqs. (35.200) and (35.205), to guarantee decoupled i_{i_d} and i_{i_q} current components, then, γ_{dq} and γ_{qq} modulation indexes should be given by Eqs. (35.210) and (35.211):

$$\gamma_{dq} = 0 \tag{35.210}$$

$$\gamma_{qq} = k\gamma_{dd} \tag{35.211}$$

From the previously defined modulation indexes and Eq. (35.200), input i_{i_q} current component can be determined by Eq. (35.212):

$$i_{i_q} = \gamma_{qq}\, i_{o_q} = k\gamma_{dd}\, i_{o_q} \tag{35.212}$$

Constant k (Eq. (35.213)) is calculated from Eq. (35.212) using output currents (Eq. (35.204)), target input currents (Eq. (35.202)), and input/output power constraint (Eq. (35.209)):

$$k = \frac{\tan(\varphi_i)}{\tan(\varphi_o)} \tag{35.213}$$

In the previously defined reference frame, the modulation index matrix (Eq. (35.214)) is time invariant and can be obtained from Eqs. (35.207), (35.208), (35.210), (35.211), and (35.213):

$$\mathbf{M_{dq}} = \begin{bmatrix} \gamma_{dd} & \gamma_{dq} \\ \gamma_{qd} & \gamma_{qq} \end{bmatrix} = \begin{bmatrix} \frac{V_o}{V_i} & 0 \\ 0 & \frac{\tan(\varphi_i)}{\tan(\varphi_o)} \frac{V_o}{V_i} \end{bmatrix} \tag{35.214}$$

As a conclusion, from Eqs. (35.206) and (35.212), there are three possible control actions:

(a) γ_{dd} and γ_{qd} to control output currents dq components
(b) k to control input currents power factor

Output current controllers

In order to design the output current controllers, it is assumed that matrix converter is feeding a three-phase general RLE load (Fig. 35.64). In the synchronized dq coordinate frame, output currents are given by Eq. (35.215):

$$\begin{cases} \frac{di_{o_d}}{dt} = -\frac{R}{L} i_{o_d} + \omega_o i_{o_q} + \frac{1}{L} v_{o_d} + \frac{1}{L} E_d \\ \frac{di_{o_q}}{dt} = -\frac{R}{L} i_{o_q} - \omega_o i_{o_d} + \frac{1}{L} v_{o_q} + \frac{1}{L} E_q \end{cases} \tag{35.215}$$

From Eq. (35.215), assuming nearly constant E_d and E_q voltages, H_{dq} (Eq. (35.216)) command voltages will guarantee that i_{o_d} and i_{o_q} output currents follow their references:

$$\begin{cases} H_d = \omega_o L i_{o_q} + v_{o_d} \\ H_q = -\omega_o L i_{o_d} + v_{o_q} \end{cases} \tag{35.216}$$

From Eq. (35.206) and H_{dq} command variables (Eq. (35.216)), matrix converter γ_{dd} and γ_{qd} modulation indexes (Eq. (35.217)) are calculated as functions of H_{dq} command voltages, allowing d and q control action decoupling (Fig. 35.70):

$$\begin{cases} \gamma_{dd} = \frac{H_d - \omega L i_{o_q}}{\sqrt{3} V_i} \\ \gamma_{qd} = \frac{H_q + \omega L i_{o_d}}{\sqrt{3} V_i} \end{cases} \tag{35.217}$$

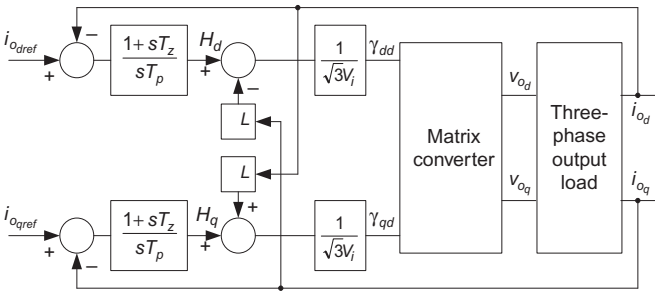


FIG. 35.70 Decoupled block diagram of the current controllers.

Often, the crossed terms $\omega L i_{o_d}$ and $\omega L i_{o_q}$ do not have a significant weight and can be neglected.

Matrix converter should be defined as having a unitary gain and a dominant pole dependent on the average delay time T_d (usually one half of the switching period) [24–27]

$$G_M(s) = \frac{v_{o_{dq}}(s)}{H_{dq}(s)} = \frac{1}{sT_d + 1} \tag{35.218}$$

The first-order dynamics load may be represented as in Eq. (35.219), where R is the load resistance and τ is the load time constant:

$$G_L(s) = \frac{v_{o_{dq}}(s)}{i_{o_{dq}}(s)} = \frac{1}{R(1 + s\tau)} \tag{35.219}$$

Usually, the zero of the compensator is chosen to cancel the pole introduced by the load.

$$T_z = \tau \tag{35.220}$$

From Eqs. (35.218) and (35.219) and Fig. 35.70, the closed-loop transfer function is given by

$$G_{cl}(s) = \frac{\dfrac{K_i}{T_p R T_d}}{s^2 + s\dfrac{1}{T_d} + \dfrac{K_i}{T_p R T_d}} \tag{35.221}$$

Comparing this transfer function with a second-order system in the canonical form, then, $\omega_n^2 = K_i/(T_p R T_d)$, where ω_n is the natural frequency, and $2\xi\omega_n = 1/T_d$, where ξ is the damping factor. Choosing $\xi = \sqrt{2}/2$ to minimize the closed-loop response overshoot and rise time, it is possible to calculate T_p (Eq. (35.222)):

$$T_p = \frac{2K_i T_d}{R} \tag{35.222}$$

Input current controller

Due to the input/output power constraint (Eq. (35.209)), input i_{i_d} current depends on the same modulation indexes as output voltages. On the contrary, i_{i_q} is linearly independent from output voltages and i_{i_d} input current and depends on variable k (Eq. (35.212)):

$$i_{i_q} = \gamma_{qd} i_{o_d} + \gamma_{qq} i_{o_q} \tag{35.223}$$

Using the expected values of γ_{qd} (Eq. (35.208)) and γ_{dd} (Eq. (35.207)) modulation indexes and the target output currents (Eq. (35.204)) in Eq. (35.223), input i_{i_q} current is shown to depend linearly on variable k:

$$i_{i_q} = k\sqrt{3} I_o \frac{V_o}{V_i} \sin\varphi_o \tag{35.224}$$

Neglecting the input filter dynamics, a nearly unitary matrix converter input power factor is obtained for $k = 0$ and, from Eq. (35.211), for $\gamma_{qq} = 0$. However, as the input filter is not ideal, this will usually result in leading power factor on the grid side connection. To control matrix converter input power factor, a simple integral controller would be enough, as the matrix converter input currents have no associated dynamics, depending directly on the switches states. However, due to the input filter capacitive characteristic, in general, and depending on the operating power conditions, the input power factor on the grid connection will be leading when compared with the controlled matrix converter input power factor.

To consider the input filter dynamics in the controller design, it is necessary to relate the grid current i_{ig_q} to the matrix converter input current i_{i_q}. The resultant second-order transfer function can be further used to design an adequate higher order input current linear controller.

Results

Considering an output three-phase RL load $R = 3\ \Omega$ and $L = 30$ mH, some results were obtained for a step of the output current amplitude at $t = 0.22$ s, a step of the output current frequency at $t = 0.28$ s, and a step of matrix converter input i_{i_q} current at $t = 0.34$ s (Fig. 35.71). The input filter dynamics was not considered, and an integral controller was used to control matrix converter input power factor.

These results were obtained using the block diagram of Fig. 35.70, assuming that matrix converter model is characterized by $T_d = 1/(2\ f_m)$, where f_m, the triangular modulator frequency, is $f_m = 10$ kHz. They show that the designed controllers guarantee a good response to step changes in the references: The output current i_{o1} and its reference i_{o1ref} are almost coincident (Fig. 35.71A), and the matrix converter input current i_{iq} follows its reference value i_{iqref}. As expected, due to the input filter, the grid current is slightly in advance when compared with the i_{iqref} reference current or when compared with matrix converter input current i_{iq}.

35.4 Predictive Optimum Control of Switching Power Converters

35.4.1 Introduction

Predictive optimum controllers are based on linear optimum control systems theory and aim to solve the minimization problem of a cost functional [13,28]. Predictive optimum controllers automatically ensure closed-loop stability and some degree of robustness concerning parameter variation and system disturbances while being easy to numerically implement [13,28].

Predictive controllers can be designed to minimize switching power converter state output errors, together with the switching frequency, being useful to control converter state variables,

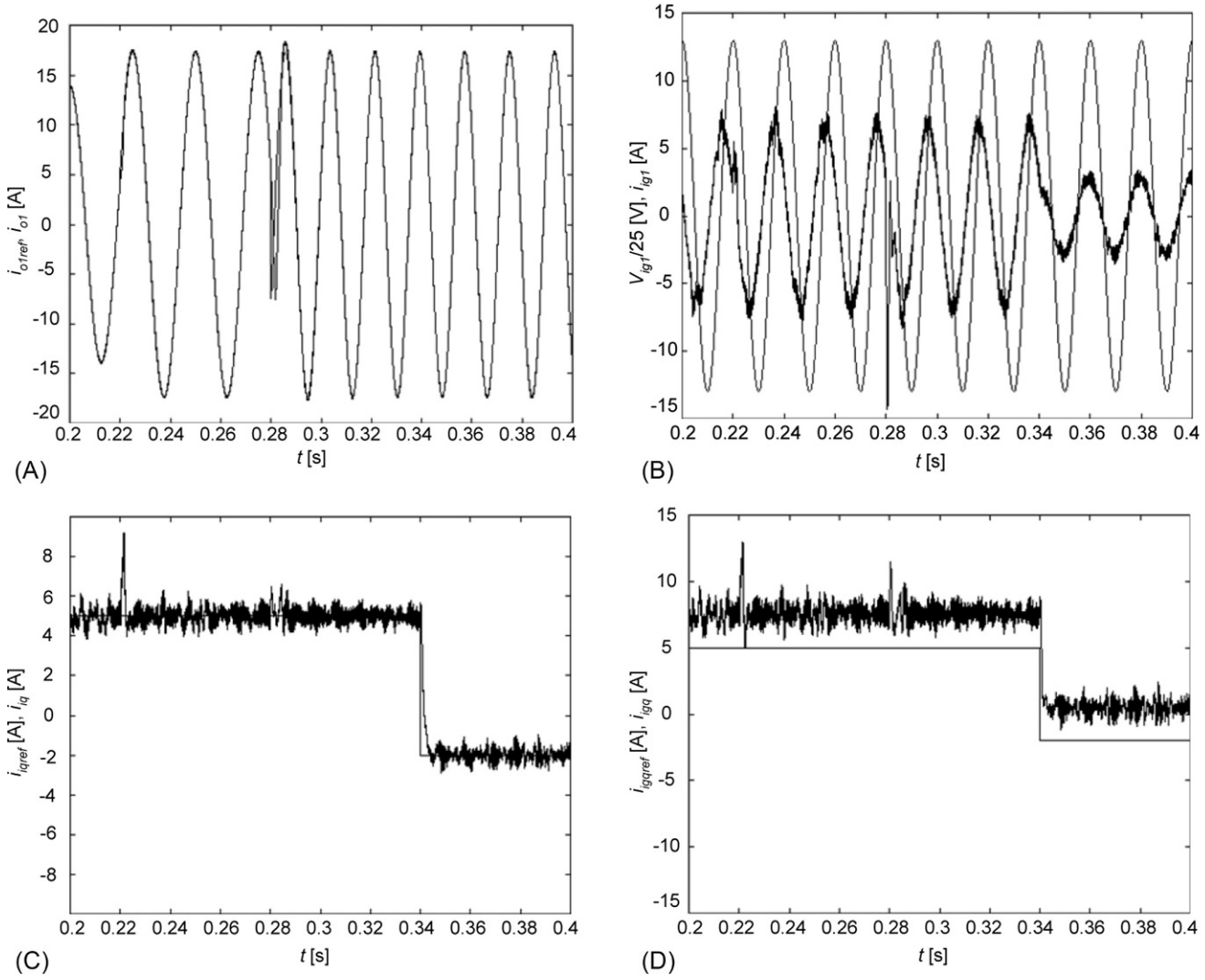


FIG. 35.71 Dynamic responses obtained with a three-phase load ($R=3\ \Omega$ and $L=30$ mH) for a step in the output reference current amplitude at $t=0.22$ s, in the output reference current frequency at $t=0.28$ s, and in the input $i_{iq}(t)$ current at $t=0.34$ s: (A) output reference current $i_{o1ref}(t)$ and output current $i_{o1}(t)$, (B) input grid voltage $v_{ig1}(t)$ and input grid current $i_{ig1}(t)$, (C) matrix converter input reference current $i_{iqref}(t)$ and matrix converter input filtered current $i_{iq}(t)$, and (D) input reference current $i_{igqref}(t)$ and input grid current $i_{igq}(t)$.

such as currents, voltages, or powers, even with coupled dynamics. Several approaches to the predictive control of switching power converters are being developed, and obtained results show improvements comparatively to standard modulation techniques or to sliding-mode control [29–38].

35.4.2 Principles of Non-Linear Predictive Optimum Control

The first step in designing a predictive controller is to obtain a detailed nonlinear direct dynamic model (including bounds, saturations, hysteresis, or other effects) of the switching power converter. This model must contain just enough detail for the converter dynamics to allow the model to forecast, in real time and with negligible error, from initial conditions the future behavior of the converter state-space variables and load, over the next sampling steps, with the converter subjected to each possible switching state (or vector).

The next step is to define a cost functional to evaluate the error cost of the application of every vector to the converter. The cost functional contains the weighted control errors and usually is defined as a norm of the error vector and/or weight control efforts, such as the switching frequency.

Known, measured (sampled), or estimated the initial conditions of the state variables, the predictive control algorithm executes by applying every possible control vector to the model. The predicted values of the state-space variables are used to evaluate the controlled output errors corresponding to each

one of the available vectors. The errors are weighted, and the value of the cost functional is calculated and stored as a vector.

After applying all the vectors to the model, the minimum of the cost functional vector indicates which switching vector must be applied to the converter in order to nearly zero the output errors in the next sampling step, that is, the next control action of the switching power converter is the vector that obtained the least value of the cost functional. Then, the algorithm is executed again in the next sampling step.

This procedure needs a powerful microprocessor to execute all the predictions in real time using fixed sampling steps (usually within 10–30 ms).

This control technology, here called nonlinear predictive optimum control, is feasible in switching power converters, as they have a reduced set of control actions: from just two in simple dc-dc converters to eight vectors in three-phase PWM inverters or 27 in three-level, three-phase multilevel or matrix converters. Therefore, for these converters, the optimization problem is reduced to the calculation and selection of the vector that generates the minimum value of the cost functional vector. However, for multilevel converters with higher number of levels, the number of vectors steeply increases (125 in five-level three-phase converters). This greatly increases the cost of the control system, since the microprocessor must execute the 125 predictions using a nonlinear model roughly within the same 10–30 ms sampling time. A faster alternative to the predictive optimum controller is also proposed.

35.4.2.1 State and Output Prediction

Consider again the state-space model (35.1), where the input vector has been separated in control vector $\mathbf{u}$ and disturbance vector $\mathbf{v}$, being $\mathbf{E}$ the disturbance matrix:

$$\begin{aligned}\dot{\mathbf{x}} &= \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} + \mathbf{E}\mathbf{v}\\ \mathbf{y} &= \mathbf{C}\mathbf{x} + \mathbf{D}\mathbf{u}\end{aligned} \tag{35.225}$$

We want to predict the operation of the switching power converter output vector at a future time $t+h$, $\mathbf{y}_{t+h}$, where h is the predictive controller sampling step. We assume to know both the system state at step t and the system switching vector at step $t+h$ (i.e., we measure the state variables at step t, $\mathbf{x}_t$, and know the system matrices at step $t+h$, $\mathbf{A}_{t+h}$, $\mathbf{B}_{t+h}$, $\mathbf{C}_{t+h}$, $\mathbf{D}_{t+h}$, and $\mathbf{E}_{t+h}$, since they depend on a known way from the converter switching vector or they are time invariant). To predict $\mathbf{y}_{t+h}$, we could use the system response obtained from (35.6), substituting the switching period T, by the time difference h between step $t+h$ and step t. For practical converters, Eq. (35.6) must be simplified to minimize calculation time, for example, making $e^{\mathbf{A}h} \approx \mathbf{I} + \mathbf{A}h$ for $\mathbf{A}h \ll \mathbf{I}$, which gives the explicit Euler forward method of integration:

$$\begin{aligned}\mathbf{x}_{t+h} &= \mathbf{x}_t + h\dot{\mathbf{x}}_t\\ \mathbf{y}_{t+h} &= \mathbf{C}_{t+h}\mathbf{x}_{t+h} + \mathbf{D}_{t+h}\mathbf{u}_{t+h}\end{aligned} \tag{35.226}$$

Looking carefully, this prediction method is only a rough approximation, since the switching vector to be applied at $t+h$ is included only in $\mathbf{C}_{t+h}$ and $\mathbf{D}_{t+h}$, but not in $\mathbf{A}_{t+h}$, $\mathbf{B}_{t+h}$, and $\mathbf{E}_{t+h}$, which are usually strongly dependent on the switching vector applied to the converters. The Euler forward method of integration can be devised to be a first-order truncation of the $\mathbf{x}_t$ Taylor series expansion in the neighborhood of t:

$$\mathbf{x}_{t+h} = \mathbf{x}_t + h\dot{\mathbf{x}}_t + \frac{h^2}{2!}\ddot{\mathbf{x}}_t + \frac{h^3}{3!}\dddot{\mathbf{x}}_t + \ldots \tag{35.227}$$

For prediction, the Euler forward is not formally adequate since the future converter switching configuration (vector) is not included explicitly in the predictive equations. Nevertheless, it has been used in predictive control, by using some equation replacement to include the needed converter matrices. Furthermore, the Euler forward method is stable only if the step h obeys $h < 2/\lambda_{max}$, where λ_{max} is the maximum of the absolute values of all eigenvalues of $\mathbf{A}$. This means that the sampling step must often be too small, which helps to reduce the relative step error (close to $h^2/4$), but increases the needed computing power [29].

The Euler backward is an implicit method derived by backward rewriting a truncated Taylor series as

$$\mathbf{x}_t = \mathbf{x}_{t+h} - h\dot{\mathbf{x}}_{t+h} - \ldots \tag{35.228}$$

The unconditionally stable Euler backward algorithm can converge even with long sampling steps, although they are bounded by a relative step error close to $-h^2/4$ [29]:

$$\mathbf{x}_{t+h} = \mathbf{x}_t + h\dot{\mathbf{x}}_{t+h} \tag{35.229}$$

Stable and lower relative step error methods could be used, like the trapezoidal integration method (35.230), but as it needs to calculate both $\dot{\mathbf{x}}_t$ and $\dot{\mathbf{x}}_{t+h}$, it loses the relative step error $h^3/12$ advantage [29] to longer computing times:

$$\mathbf{x}_{t+h} = \mathbf{x}_t + \frac{h}{2}(\dot{\mathbf{x}}_t + \dot{\mathbf{x}}_{t+h}) \tag{35.230}$$

Since we must predict the result of the application of the switching vector at $t+h$, we should use $\mathbf{A}_{t+h}$, $\mathbf{B}_{t+h}$, and $\mathbf{E}_{t+h}$, for prediction, by selecting the Euler backward method, which gives the system time derivatives at $t+h$:

$$\dot{\mathbf{x}}_{t+h} = \mathbf{A}_{t+h}\mathbf{x}_{t+h} + \mathbf{B}_{t+h}\mathbf{u}_{t+h} + \mathbf{E}_{t+h}\mathbf{v}_{t+h} \tag{35.231}$$

Therefore, the converter state variables and outputs at $t+h$ will be

$$\begin{aligned}\mathbf{x}_{t+h} &= [\mathbf{I} - h\mathbf{A}_{t+h}]^{-1}[\mathbf{x}_t + h(\mathbf{B}_{t+h}\mathbf{u}_{t+h} + \mathbf{E}_{t+h}\mathbf{v}_{t+n})]\\ \mathbf{y}_{t+h} &= \mathbf{C}_{t+h}\mathbf{x}_{t+h} + \mathbf{D}_{t+h}\mathbf{u}_{t+h}\end{aligned} \tag{35.232}$$

This equation means that to predict the converter behavior, the switching vector must define the matrices $\mathbf{A}_{t+h}$, $\mathbf{B}_{t+h}$, $\mathbf{C}_{t+h}$, $\mathbf{D}_{t+h}$, and $\mathbf{E}_{t+h}$ (or they must be time invariant) and we must measure (or estimate) the state $\mathbf{x}_t$, the inputs $\mathbf{u}_t$, and disturbances $\mathbf{v}_t$ to estimate $\mathbf{u}_{t+h}$ and $\mathbf{v}_{t+h}$. If $\mathbf{u}_{t+h}$ values are based on the switching

vectors times dc quantities $\mathbf{U}$, then it might be $\mathbf{U}_{t+h} \approx \mathbf{U}_t$, or $\mathbf{U}_{t+h}$ can be estimated using linear extrapolations, such as Euler backward or at least the Euler forward. If $\mathbf{v}_t$ contains ac sinusoidal voltages, then it should be for $\omega h \ll 1$:

$$\begin{aligned}\sin(\omega(t+h)) &= \sin(\omega t)\cos(\omega h) + \sin(\omega h)\cos(\omega t)\\ &\approx \sin(\omega t) + \omega h \cos(\omega t)\\ \cos(\omega(t+h)) &= \cos(\omega t)\cos(\omega h) - \sin(\omega t)\sin(\omega h)\\ &\approx \cos(\omega t) - \omega h \sin(\omega t)\end{aligned} \tag{35.233}$$

The above equations can also be used to predict the future values of the output vector reference values $\mathbf{y}_{ref}$ at $t+h$, if sinusoidal references are being in use and tracking control is sought.

In predictive control, the direct dynamics equations (35.232) are used to predict all the possible future values of the converter outputs, assuming open-loop stability, observability, and all state variables are accessible for measuring or estimation.

35.4.2.2 Minimization of the Cost Functional in Converters with a Reduced Set of Vectors

To solve the minimization problem of the cost functional in a system with a reduced set of m control vectors, consider the errors $\mathbf{e}_j$ ($j \in \{1,m\}$) between the output vector reference values $\mathbf{y}_{ref}$ and the output at $t+h$ corresponding to the vector j of the control vector set, $\mathbf{y}_{jt+h}$, defined as

$$\mathbf{e}_j = \mathbf{y}_{ref} - \mathbf{y}_{j_{t+h}} \tag{35.234}$$

Define also $\mathbf{J}_{t+h}$ (35.235) as an m components vector, the quadratic cost functional of the weighted errors $\mathbf{e}_j$, and the weighted control action $\mathbf{u}_j$, for each control vector j, with weighting matrices $\boldsymbol{\rho}_e$ and $\boldsymbol{\rho}_u$, respectively, for the errors and control actions:

$$\mathbf{J}_{t+h} = \int_0^\infty \left(\mathbf{e}_j^{\mathrm{T}} \boldsymbol{\rho}_e \mathbf{e}_j + \mathbf{u}_j^{\mathrm{T}} \boldsymbol{\rho}_u \mathbf{u}_j\right) \mathrm{d}t \tag{35.235}$$

The weighting matrices $\boldsymbol{\rho}_e$ and $\boldsymbol{\rho}_u$ are the predictive optimum controller degrees of freedom to penalize excessively high errors or high control efforts, such as high switching frequencies.

After calculating all the m components of the quadratic cost functional $\mathbf{J}_{t+h}$, the last step in the design of predictive optimum controller is to select the control vector $\mathbf{u}_j$ to be applied to the converter, as the control vector j for which the quadratic cost functional is minimum:

$$\mathbf{u}_j \Leftrightarrow \min_j \left[J_{1t+h}, J_{2t+h}, \ldots, J_{j_{t+h}}, \ldots, J_{mt+h}\right] \tag{35.236}$$

It is worth to note that the control vector $\mathbf{u}_j$ just minimizes the defined quadratic cost functional, subjected to the constraints imposed in the converter direct dynamics (35.225). The usual system performance indexes (overshoot, stability margin, disturbance rejection, and robustness) can have little relation with the minimization of the defined quadratic cost functional. This must be considered when defining the cost functional and the weighting matrices of predictive optimum controllers. The designed predictive controller will only perform correctly if, while minimizing the cost functional, it also guarantees adequate steady-state and dynamic behavior. Nevertheless, predictive optimum controllers use state feedback of all the state variables to be controlled and therefore can be tailored to present optimum or near optimum dynamics, considering the physical bounds.

35.4.3 Principles of Non-Linear Fast Predictive Optimum Control

The above algorithm needs to evaluate Eqs (35.232)–(35.235) m times, which can be time-consuming for three-phase multilevel converters with five or more levels.

To reduce the microprocessor computational task, the use of a subset of either adjacent vectors (for minimum switching frequency) or vectors that can zero one or several harmonics, is an alternative to reduce the number of candidate vectors to be analyzed in real time.

Another possibility is to use the converter inverse dynamics to obtain a fast predictive optimum controller, which is here introduced.

From the output equation of the state-space model (35.225), it can be written as

$$\mathbf{x}_{ref} = \mathbf{C}^{-1}\left[\mathbf{y}_{ref} - \mathbf{D}\,\mathbf{u}_{t+h}\right] \tag{35.237}$$

Note also that if we suppose that the control objective is attained at sampling time $t+h$, then $\mathbf{x}_{t+h} = \mathbf{x}_{ref}$, and from (35.229),

$$\dot{\mathbf{x}}_{t+h} = h^{-1}\left[\mathbf{x}_{t+h} - \mathbf{x}_t\right] = h^{-1}\left[\mathbf{x}_{ref} - \mathbf{x}_t\right] \tag{35.238}$$

Using (35.237) in (35.238) and the result in the state equation of (35.225), the converter inverse dynamics, needed to estimate the necessary control vector $\mathbf{u}_{t+h}$, can be obtained:

$$\begin{aligned}\mathbf{u}_{t+h} = &\left[\mathbf{A}\mathbf{C}^{-1}\mathbf{D} - \mathbf{B} - \left[h^{-1}\mathbf{C}^{-1}\right]\mathbf{D}\right]^{-1}\left[\left[\mathbf{A}\mathbf{C}^{-1} - \left[h^{-1}\mathbf{C}^{-1}\right]\right]\mathbf{y}_{ref}\right.\\ &\left. + \mathbf{E}\mathbf{v} + \left[h^{-1}\mathbf{x}_t\right]\right]\end{aligned} \tag{35.239}$$

This equation defines the needed components of the control vector $\mathbf{u}_{t+h}$. An alternative way to generate the needed control vector $\mathbf{u}_{t+h}$ is to use the controllability canonical form of the converter dynamics to compute the equivalent control, similar to (35.83).

Seldom, the converter will be able to replicate the vector in (35.239), since it is a continuously variable equivalent control vector and the converter only outputs a reduced set of control vectors. Therefore, the control vector $\mathbf{u}_{t+h}$ might be either

obtained as a kind of space-vector modulation or found by minimization of a quadratic cost functional, based on the norm of the difference vector between the needed $\mathbf{u}_{t+h}$ and the available set of vectors $\mathbf{u}_j$:

$$J_{j_{t+h}} = \left\|\mathbf{u}_{t+h} - \mathbf{u}_j\right\| = \sqrt{\left(u_{1t+h} - u_{1j}\right)^2 + \ldots + \left(u_{mt+h} - u_{mj}\right)^2} \tag{35.240}$$

Then, this functional is computed for all $\mathbf{u}_j$, to find the vector that leads to the minimum value of the cost functional (35.240) accordingly to (35.236).

The fast predictive optimum control needs much less computational time, as it only evaluates 35.239 one time per step and (35.240) m times. However, preliminary inspection of Eq. (35.239) indicates that it can only be directly applied to converters with input and output circuits that have time-invariant dynamic matrices.

35.4.4 Examples: Predictive Control of Multilevel Inverters and Matrix Converters

35.4.4.1 Example 35.19: Non-linear Predictive Optimum Control of Multilevel Inverters

Consider the multilevel inverter of Fig. 35.58, with three-phase ac current direct dynamics in the αβ plane given by (35.167) and 35.161, which can be rewritten as

$$\begin{bmatrix} \frac{di_\alpha}{dt} \\ \frac{di_\beta}{dt} \\ \frac{dU_{C1}}{dt} \\ \frac{dU_{C2}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & 0 & \frac{\Gamma_{1\alpha}}{L} & \frac{\Gamma_{2\alpha}}{L} \\ 0 & -\frac{R}{L} & \frac{\Gamma_{1\beta}}{L} & \frac{\Gamma_{2\beta}}{L} \\ -\frac{\Gamma_{1\alpha}}{C_1} & -\frac{\Gamma_{1\beta}}{C_1} & 0 & 0 \\ -\frac{\Gamma_{2\alpha}}{C_2} & -\frac{\Gamma_{2\beta}}{C_2} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \\ U_{C1} \\ U_{C2} \end{bmatrix} + \begin{bmatrix} -\frac{1}{L} & 0 & 0 \\ 0 & -\frac{1}{L} & 0 \\ 0 & 0 & \frac{1}{C_1} \\ 0 & 0 & \frac{1}{C_2} \end{bmatrix} \begin{bmatrix} U_{e\alpha} \\ U_{e\beta} \\ i_{dc} \end{bmatrix}. \tag{35.241}$$

where $\Gamma_{i\alpha} = \sqrt{\frac{2}{3}}\left(\Gamma_{i1} - \frac{\Gamma_{i2}}{2} - \frac{\Gamma_{i3}}{2}\right)$, $\Gamma_{i\beta} = \sqrt{\frac{2}{3}}\left(\frac{\sqrt{3}}{2}\Gamma_{i2} - \frac{\sqrt{3}}{2}\Gamma_{i3}\right)$, and $i \in \{1,2\}$.

The optimal controller is designed to choose the best output voltage vector able to minimize both the ac current, i_α and i_β, errors and the input dc capacitor U_{C1} and U_{C2} voltage unbalance.

Predictive equations for ac αβ currents

To design a real-time optimal predictive controller, the obtained αβ converter model (35.167) will be solved to predict the state variable values at the next sampling period, for all the 27 available vectors, assuming a sampling time h small enough, so that U_{C1}, U_{C2}, and u_{ep}, $p \in \{\alpha,\beta\}$, can be considered nearly constant during step time h. Therefore, the simplified model is decoupled and, using (35.229) in (35.167), the αβ current i_{pt+h} ($p \in \{\alpha,\beta\}$) prediction is obtained:

$$i_{p_{t+h}} \approx \frac{i_{p_t} + \frac{h}{L}\left(U_{Sp_{t+h_j}} - u_{ep_{t+h}}\right)}{\left(1 + \frac{hR}{L}\right)} \tag{35.242}$$

where the perturbations u_{ep} can be estimated using (35.233).

Predictive equations for dc capacitor voltage unbalance

To predict the capacitor voltage difference or unbalance, $U_{C1} - U_{C2}$, the corresponding dynamic equations (35.241) must be solved. Assuming h small enough, $C_1 = C_2 = C$, and small control errors, it can be assumed that the ac currents follow their references, for example, $i_{pt+h} = i_{pref}$. Then, from (35.241) and (35.229),

$$\left(U_{C1} - U_{C2}\right)_{t+h} = \left(U_{C1} - U_{C2}\right)_t + \frac{h}{C}\left[\left(\Gamma_{2\alpha} - \Gamma_{1\alpha}\right)_j i_{\alpha ref} + \left(\Gamma_{2\beta} - \Gamma_{1\beta}\right)_j i_{\beta ref}\right] \tag{35.243}$$

Quadratic cost functional

In NPC multilevel converters operated as ac current sources, three independent variables can be controlled, such as two ac currents $i_\alpha(t)$ and $i_\beta(t)$, and the dc capacitor voltage unbalance U_{C1}-U_{C2}. Therefore, the tracking error vector is defined as

$$\left[e_{i\alpha}, e_{i\beta}, e_{UC}\right]_j = \left[i_{\alpha ref} - i_{\alpha t+h}, i_{\beta ref} - i_{\beta t+h}, \left(U_{C1} - U_{C2}\right)_{t+h}\right]_j \tag{35.244}$$

The ac current references $i_{\alpha ref}$ and $i_{\beta ref}$ are obtained one sample step forward (using (35.233)) to avoid the delay time due to processor calculation time.

The main objective of the predictive optimum controller is the minimization of both the ac currents errors and the capacitor voltage difference using the following quadratic cost functional:

$$J_{j_{t+h}} = \sqrt{\rho_\alpha e_{i\alpha_j}^2 + \rho_\beta e_{i\beta_j}^2 + \rho_U e_{UC_j}^2} \tag{35.245}$$

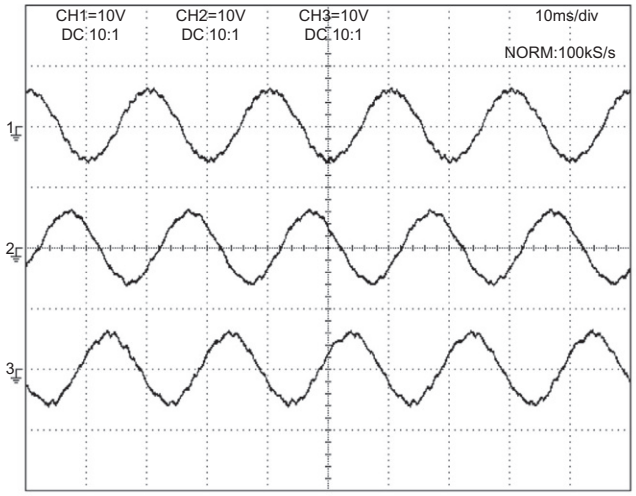
This functional is calculated for all the multilevel 27 available vectors and the resultant value stored (Eqs 35.242–35.245 are calculated 27 times). Using the procedure outlined in

(35.236), the vector leading to the minimum value of the cost functional is selected to be applied to the multilevel converter.

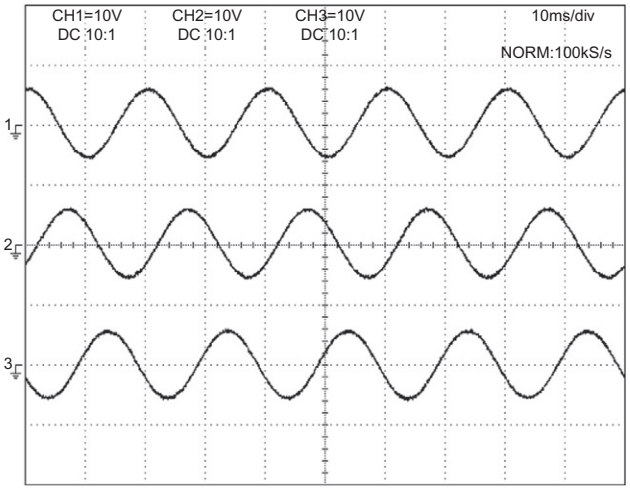
Results

The above procedure was implemented in a PowerPC-based board (DS1103) to execute in $h = 25$ ms. The following parameters were used: $U_{dc} = 300$ V, $C_1 = 4.4$ mF, $C_2 = 4.4$ mF, $L = 15.1$ mH, $R = 0.1\ \Omega$, $i_{ac} = 7$ A, U_e obtained from 230/400 V, 50 Hz through a 400/230 V transformer, and $\rho_\alpha = \rho_\beta = 11$ and $\rho_U = 25$. The ac-controlled currents and dc capacitor voltage balance are compared with the results of a sliding-mode controller. Fig. 35.72 shows that the predictive optimum controller performance is better than the sliding-mode controller. The predictive optimum controller presents some robustness to industrial component tolerances. Results showed a tolerance from −50% to +100%.

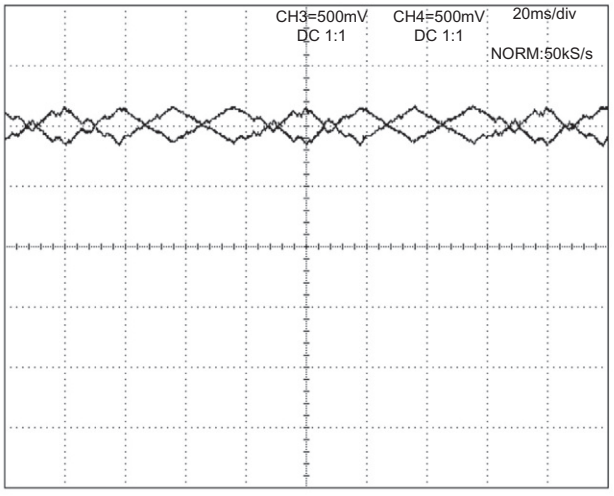
Further experiments [37,38] revealed that harmonics of ac currents were 46 dB below the 50 Hz fundamental level, improving by 14 dB the sliding-mode controller result. The switching frequency of the predictive optimum controller spreads over the frequency spectrum below 2.5 kHz, reducing and softening the audible noise. The average switching frequency of the predictive optimum controlled multilevel converter is reduced to half of the value of a sliding-mode-controlled multilevel at the same



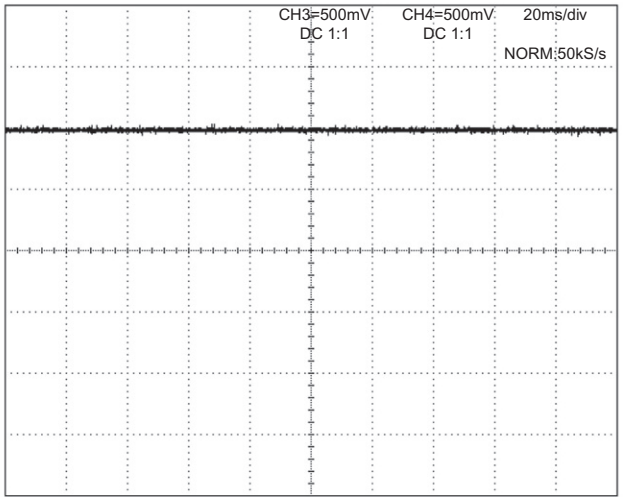
(A) Sliding mode controller ac currents (12A/Div)



(B) Predictiv optimumm controller ac currents (12A/Div)



(C) Sliding mode controller dc capacitor voltage balancing (10 V/Div)



(D) Predictiv optimum controller dc capacitor voltage balancing (10 V/Div)

FIG. 35.72 Multilevel converter sinusoidal ac currents, i_1, i_2, and i_3, in steady-state operation and dc capacitor voltages, using sliding-mode controllers (A, C) and predictive optimum controller (B, D). (A) Sliding-mode controller ac currents (12 A/div), (B) Predictive optimum controller ac currents (12 A/div), (C) Sliding-mode controller dc capacitor voltage balancing (10 V/div), (D) Predictive optimum controller dc capacitor voltage balancing (10 V/div).

current ripple. Further reduction could be obtained by weighting the switching frequency in the quadratic cost functional [39].

35.4.4.2 Example 35.20: Fast Predictive Optimum Control of Matrix Converters

Consider the three-phase ac/ac matrix converter with input *lCr* filter of Fig. 35.64, and suppose we want to control the output currents i_{o_1}, i_{o_2}, and i_{o_3} while guaranteeing an almost unity input power factor and near sinusoidal input currents i_{ig1}, i_{ig2}, and i_{ig3}.

The converter direct dynamics of the output currents in dq frame at frequency ω_o, i_{od}, i_{oq} is

$$\begin{cases} \dfrac{di_{o_d}}{dt} = -\dfrac{R}{L} i_{o_d} + \dfrac{1}{L} v_{o_d} + \dfrac{1}{L} E_d + \omega_o i_{o_q} \\ \dfrac{di_{o_q}}{dt} = -\dfrac{R}{L} i_{o_q} + \dfrac{1}{L} v_{o_q} + \dfrac{1}{L} E_q - \omega_o i_{o_d} \end{cases} \tag{35.246}$$

The converter direct dynamics of the input currents in dq frame at frequency ω_i, i_{igd}, i_{igq} is given in (35.183) and (35.184). To control the matrix input power factor, the dynamics of the input dq currents, neglecting the effects of the matrix input filter damping resistor ($r \to \infty$), can be simplified to be

$$\begin{cases} \dfrac{di_{igd}}{dt} = \omega_i i_{igq} - \dfrac{1}{2l} v_{cd} - \dfrac{1}{2\sqrt{3}l} v_{cq} + \dfrac{1}{l} V_{igd} \\ \dfrac{di_{igq}}{dt} = -\omega_i i_{igd} + \dfrac{1}{2\sqrt{3}l} v_{cd} - \dfrac{1}{2l} v_{cq} + \dfrac{1}{l} V_{igq} \\ \dfrac{dv_{cd}}{dt} = \omega_i v_{cq} - \dfrac{1}{2\sqrt{3}C} i_{igq} + \dfrac{1}{2C} i_{igd} - \dfrac{1}{2C} i_{id} + \dfrac{1}{2\sqrt{3}C} i_{iq} \\ \dfrac{dv_{cq}}{dt} = -\omega_i v_{cd} + \dfrac{1}{2\sqrt{3}C} i_{igd} + \dfrac{1}{2C} i_{igq} - \dfrac{1}{2\sqrt{3}C} i_{id} - \dfrac{1}{2C} i_{iq} \end{cases} \tag{35.247}$$

The control vector $\mathbf{u}_{t+h}$ are defined by v_{odt+h}, v_{oqt+h}, and i_{iqt+h}. From the input and output dynamics of the matrix converter, Eq. (35.248) computes the necessary vector components to ensure convergence to the reference values within one sampling step h. Most terms of the i_{iqt+h} current can be neglected for simplicity, the essential ones being the difference $i_{igqref} - i_{igqt}$ with associated gain and the feedforward value of i_{igqref}:

$$\begin{aligned} v_{o_{d_{t+h}}} &= \frac{L}{h}\left(i_{o_{d_{ref}}} - i_{o_{d_t}}\right) + R i_{o_{d_{ref}}} - E_d - \omega_o l i_{o_{q_{ref}}} \\ v_{o_{q_{t+h}}} &= \frac{L}{h}\left(i_{o_{q_{ref}}} - i_{o_{q_t}}\right) + R i_{o_{q_{ref}}} - E_q + \omega_o l i_{o_{d_{ref}}} \\ i_{i_{q_{t+h}}} &= \frac{6Cl}{h^2}\left(i_{igq_{ref}} - 2i_{igq_t} + i_{igq_{t-h}}\right) + \left(3Cl\omega_i^2 + 1\right) i_{igq_{ref}} \\ &\quad -3\omega_i C v_{cd} - \sqrt{3}\omega_i C v_{cq} + 3\omega_i C V_{gd} \approx \\ &\approx \frac{6Cl}{h^2}\left(i_{igq_{ref}} - 2i_{igq_t} + i_{igq_{t-h}}\right) + \left(3Cl\omega_i^2 + 1\right) i_{igq_{ref}} \end{aligned} \tag{35.248}$$

Only one calculation for the optimum vector with components (35.247) is needed, avoiding the currents and the respective errors computation for all the 27 possible converter vectors, speeding the predictive method. Since the discrete time derivative and damping terms are calculated using the current future values, the Euler backward algorithm is used, ensuring convergence.

In practice, none of the available converter vectors will present exactly the necessary components. Therefore, the distance from each vector to the optimum vector (the vector error norm) must be computed, using the cost functional:

$$J_{j_{t+h}} = \sqrt{\rho_{vd}\left(v_{o_{d_{t+h}}} - v_{o_{d_j}}\right)^2 + \rho_{vq}\left(v_{o_{q_{t+h}}} - v_{o_{q_j}}\right)^2 + \rho_{iq}\left(i_{i_{q_{t+h}}} - i_{i_{q_j}}\right)^2} \tag{35.249}$$

Results using $\rho_{vd} = \rho_{vq} = \rho_{iq} = 1$ show that fast predictive optimum controllers, using the converter inverse dynamics, present better performances than state-of-art sliding-mode controllers (Fig. 35.73). Stability and robustness of fast predictive optimum controllers, concerning parameter variation, disturbances, and nonmodeled dynamics, must be investigated. The fast predictive methodology was successful applied to other converters [40]:

35.5 Fuzzy Logic Control of Switching power converters

35.5.1 Introduction

Fuzzy logic control is a heuristic approach that easily embeds the knowledge and key elements of human thinking in the design of nonlinear controllers [41–43]. Qualitative and heuristic considerations, which cannot be handled by conventional control theory, can be used for control purposes in a systematic form, applying fuzzy control concepts [44]. Fuzzy logic control does not need an accurate mathematical model, can work with imprecise inputs, can handle nonlinearity, and can present disturbance insensitivity greater than the most nonlinear controllers. Fuzzy logic controllers usually outperform other controllers in complex, nonlinear, or undefined systems for which a good practical knowledge exists.

Fuzzy logic controllers are based on fuzzy sets, that is, classes of objects in which the transition from membership to nonmembership is smooth rather than abrupt. Therefore, boundaries of fuzzy sets can be vague and ambiguous, making them useful for approximation models.

The first step in the fuzzy controller synthesis procedure is to define the input and output variables of the fuzzy controller. This is done accordingly with the expected function of the controller. There are no general rules to select those variables, although typically the variables chosen are the states of the

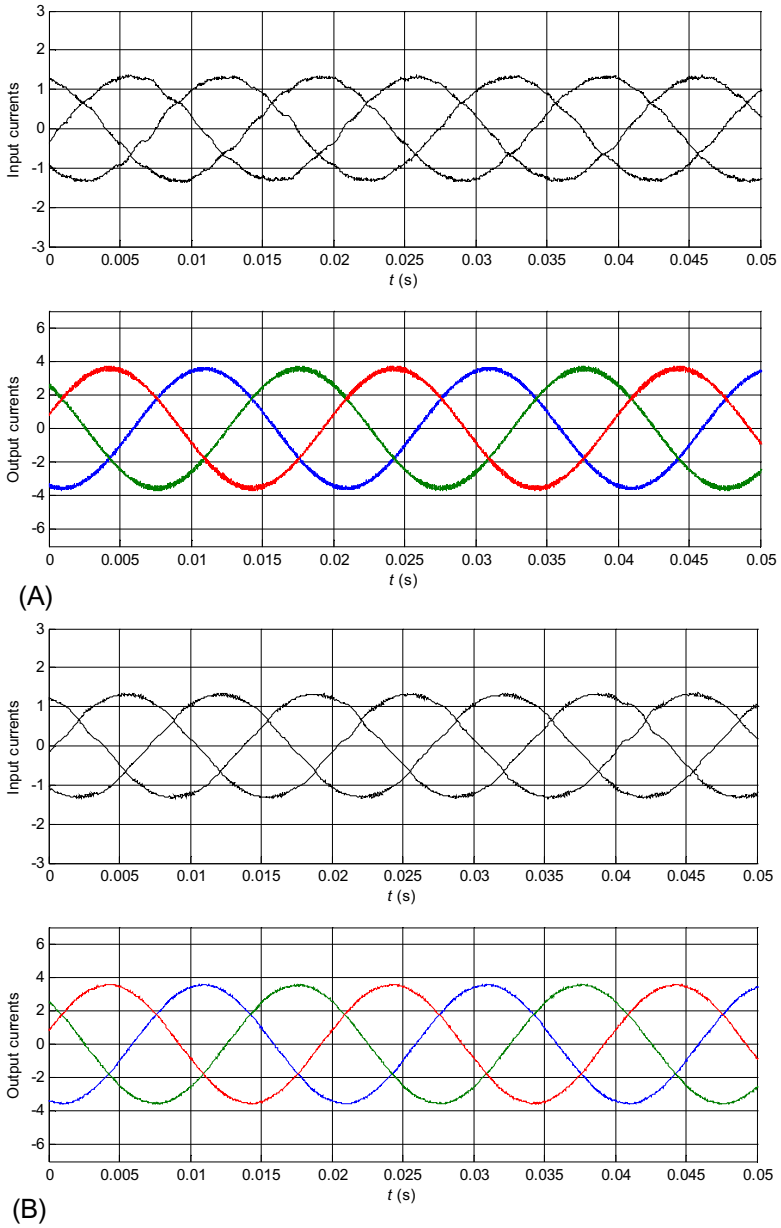


FIG. 35.73 Matrix converter sinusoidal ac input and output currents, i_1, i_2, and i_3, in steady-state operation, using sliding-mode controllers (A) and fast predictive optimum controllers (B).

controlled system, their errors, error variation, and/or error accumulation. In switching power converters, the fuzzy controller input variables are commonly the output voltage or current error and/or the variation or accumulation of this error. The output variables $u(k)$ of the fuzzy controller can define the converter duty cycle (Fig. 35.74) or a reference current to be applied in an inner current-mode PI or a sliding-mode controller.

The fuzzy controller rules are usually formulated in linguistic terms. Thus, the use of linguistic variables and fuzzy sets implies the fuzzification procedure, that is, the mapping of the input variables into suitable linguistics values.

Rule evaluation or decision-making infers, using an inference engine, the fuzzy control action from the knowledge of the fuzzy rules and the linguistic variable definition.

The output of a fuzzy controller is a fuzzy set, and thus, it is necessary to perform a defuzzification procedure, that is, the conversion of the inferred fuzzy result to a nonfuzzy (crisp) control action, that better represents the fuzzy one. This last step obtains the crisp value for the controller output $u(k)$ (Fig. 35.74).

These steps can be implemented online or offline. Online implementation, useful if an adaptive controller is intended, performs real-time inference to obtain the controller output

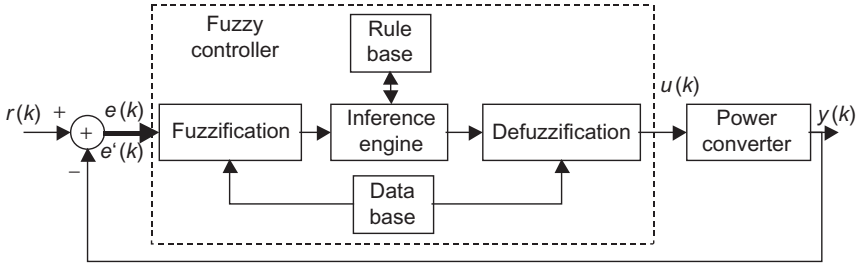


FIG. 35.74 Structure of a fuzzy logic controller.

and needs a fast enough processor. Off-line implementation employs a lookup table built according to the set of all possible combinations of input variables. To obtain this lookup table, the input values in a quantified range are converted (fuzzification) into fuzzy variables (linguistic). The fuzzy set output, obtained by the inference or decision-making engine according to linguistic control rules (designed by the knowledge expert), is then, converted into numeric controller output values (defuzzification). The table contains the output for all the combinations of quantified input entries. Off-line process can actually reduce the controller actuation time since the only effort is limited to consulting the table at each iteration.

This section presents the main steps for the implementation of a fuzzy controller suitable for switching power converter control. A meaningful example is provided.

35.5.2 Fuzzy Logic Controller Synthesis

Fuzzy logic controllers consider neither the parameters of the switching power converter or their fluctuations nor the operating conditions, but only the experimental knowledge of the switching power converter dynamics. In this way, such a controller can be used with a wide diversity of switching power converters implying only small modifications. The necessary fuzzy rules are simply obtained considering roughly the knowledge of the switching power converter dynamic behavior.

35.5.2.1 Fuzzification

Assume, as fuzzy controller input variables, an output voltage (or current) error and the variation of this error. For the output, assume a signal $u(k)$, the control input of the converter.

A. Quantization Levels

Consider the reference $r(k)$ of the converter output kth sample, $y(k)$. The tracking error $e(k)$ is $e(k)=r(k)-y(k)$, and the output error change $\Delta_e(k)$, between the samples k and $k-1$, is determined by $\Delta_e(k)=e(k)-e(k-1)$.

These variables and the fuzzy controller output $u(k)$, usually ranging from -10 to 10 V, can be quantified in m levels $\{-(m-1)/2, +(m-1)/2\}$. For offline implementation, m sets a compromise between the finite length of a lookup table and the required precision.

B. Linguistic Variables and Fuzzy Sets

The fuzzy sets for x_e, the linguistic variable corresponding to the error $e(k)$; for $x_{\Delta e}$, the linguistic variable corresponding to the error variation $\Delta_e(k)$; and for x_u, the linguistic variable of the fuzzy controller output $u(k)$ are usually defined as positive big (*PB*), positive medium (*PM*), positive small (*PS*), zero (*ZE*), negative small (*NS*), negative medium (*NM*), and negative big (*NB*), instead of having numerical values.

In most cases, the use of these seven fuzzy sets is the best compromise between accuracy and computational task.

C. Membership Functions

A fuzzy subset, for example, $\mathbf{S}_i$ ($\mathbf{S}_i=$(NB, NM, NS, ZE, PS, PM, or PB)) of a universe E, collection of $e(k)$ values denoted generically by $\{e\}$, is characterized by a membership function μ_{Si}: $E\rightarrow[0,1]$, associating with each element e of universe E, a number $\mu_{Si}(e)$ in the interval [0,1], which represents the grade of membership of e to E. Therefore, each variable is assigned a membership grade to each fuzzy set, based on a corresponding membership function (Fig. 35.75). Considering the m quantization levels, the membership function $\mu_{Si}(e)$ of the element e in the universe of discourse E, may take one of the discrete values included in $\mu_{Si}(e)\in\{0; 0.2; 0.4; 0.6; 0.8; 1; 0.8; 0.6; 0.4; 0.2; 0\}$. Membership functions are stored in the database (Fig. 35.74).

Considering $e(k)=2$ and $\Delta_e(k)=-3$, taking into account the staircase-like membership functions shown in Fig. 35.75, it can be said that x_e is *PS* and also *ZE*, being equally *PS* and *ZE*. Also, $x_{\Delta e}$ is *NS* and *ZE*, being less *ZE* than *NS*.

D. Linguistic Control Rules

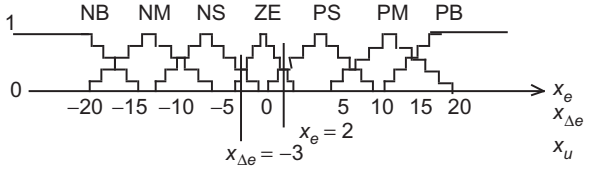


FIG. 35.75 Membership functions in the universe of discourse.

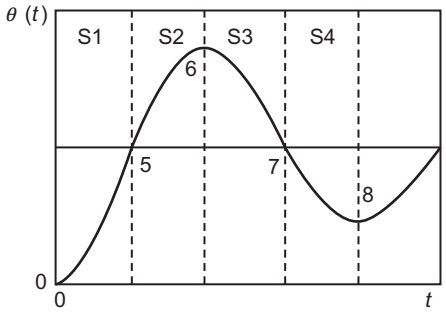


FIG. 35.76 Reference dynamic model of switching power converters: second-order damped oscillating error response.

The generic linguistic control rule has the following form: "IF $x_e(k)$ is membership of the set $\mathbf{S}_i$ = (NB, NM, NS, ZE, PS, PM, or PB) AND $x_{\Delta e}(k)$ is membership of the set $\mathbf{S}_j$ = (NB, NM, NS, ZE, PS, PM, or PB), THEN the output control variable $x_u(k+1)$ is membership of the set $\mathbf{S}_u$ = (NB, NM, NS, ZE, PS, PM, or PB)."

Usually, the rules are obtained considering the most common dynamic behavior of switching power converters, the second-order system with damped oscillating response (Fig. 35.76). Analyzing the error and its variation, together with the rough linguistic knowledge of the needed control input, an expert can obtain linguistic control rules such as the ones displayed in Table 35.8. For example, at point six of Fig. 35.76, the rule is "if $x_e(k)$ is NM AND $x_{\Delta e}(k)$ is ZE, THEN $x_u(k+1)$ should be NM."

Table 35.8, for example, states that

IF $x_e(k)$ is NB AND $x_{\Delta e}(k)$ is NB, THEN $x_u(k+1)$ must be NB, or
IF $x_e(k)$ is PS AND $x_{\Delta e}(k)$ is NS, THEN $x_u(k+1)$ must be NS, or
IF $x_e(k)$is PS AND $x_{\Delta e}(k)$ is ZE, THEN $x_u(k+1)$ must be PS, or
IF $x_e(k)$ is ZE AND $x_{\Delta e}(k)$ is NS, THEN $x_u(k+1)$ must be NS, or
IF $x_e(k)$ is ZE AND $x_{\Delta e}(k)$ is ZE, THEN $x_u(k+1)$ must be ZE, or
IF….

TABLE 35.8 Linguistic control rules

$x_e(k)x_{\Delta e}(k)$	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NM	NM	PS	PM
NM	NB	NB	NM	NS	NM	PM	PB
NS	NB	NB	NM	NS	NS	PM	PB
ZE	NB	NM	NS	ZE	PS	PM	PB
PS	NB	NM	PS	PS	PM	PB	PB
PM	NB	NM	PM	PS	PM	PB	PB
PB	NM	NS	PM	PM	PB	PB	PB

These rules (rule base) alone do not allow the definition of the control output, as several of them may apply at the same time.

35.5.2.2 Inference Engine

The result of a fuzzy control algorithm can be obtained using the control rules of Table 35.8, the membership functions, and an inference engine. In fact, any quantified value for $e(k)$ and $\Delta_e(k)$ is often included into two linguistic variables. With the membership functions used and knowing that the controller considers $e(k)$ and $\Delta_e(k)$, the control decision generically must be taken according to four linguistic control rules.

To obtain the corresponding fuzzy set, the min-max inference method can be used. The minimum operator describes the "AND" present in each of the four rules, that is, it calculates the minimum between the discrete value of the membership function $\mu_{Si}(x_e(k))$ and the discrete value of the membership function $\mu_{Sj}(x_{\Delta e}(k))$. The "THEN" statement links this minimum to the membership function of the output variable. The membership function of the output variable will therefore include trapezoids limited by the segment $\min(\mu_{Si}(x_e(k))$ and $\mu_{Sj}(x_{\Delta e}(k)))$.

The OR operator linking the different rules is implemented by calculating the maximum of all the (usually four) rules. This mechanism to obtain the resulting membership function of the output variable is represented in Fig. 35.77.

35.5.2.3 Defuzzification

As shown, the inference method provides a resulting membership function $\mu_{Sr}(x_u(k))$, for the output fuzzy variable x_u (Fig. 35.77). Using a defuzzification process, this final membership function, obtained by combining all the membership functions, as a consequence of each rule, is then converted into a numerical value, called $u(k)$. The defuzzification strategy can be the center of area (COA) method. This method generates one output value $u(k)$, which is the abscissa of the gravity center of the resulting membership function area, given by the following relation:

$$u(k) = \left(\sum_{i=1}^{m} \mu_{Sr}(x_u(k))x_u(k)\right) \Big/ \sum_{i=1}^{m} \mu_{Sr}(x_u(k)) \qquad (35.250)$$

This method provides good results for output control. Indeed, for a weak variation of $e(k)$ and $\Delta_e(k)$, the center of the area will move just a little and so does the controller output value. By comparison, the alternative defuzzification method, mean of maximum strategy (MOM) is advantageous for fast response, but it causes a greater steady-state error and overshoot (considering no perturbations).

35.5.2.4 Lookup Table Construction

Using the rules given in Table 35.8, the min-max inference procedure and COA defuzzification, all the controller output

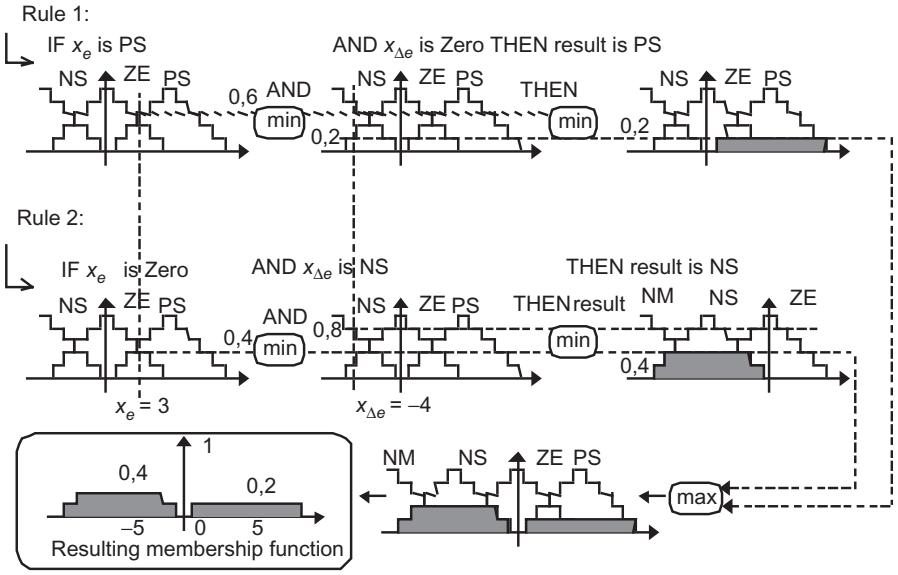


FIG. 35.77 Application of the min-max operator to obtain the output membership function.

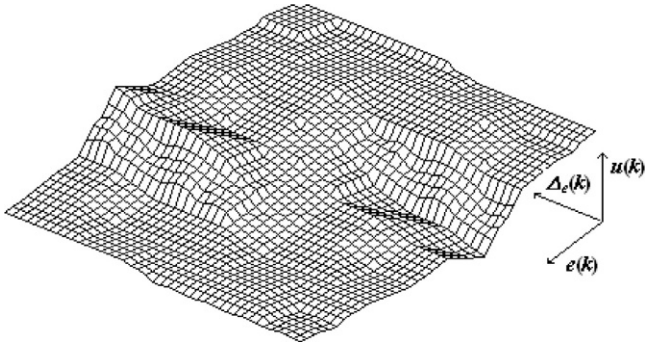


FIG. 35.78 Three-dimensional view of the lookup table.

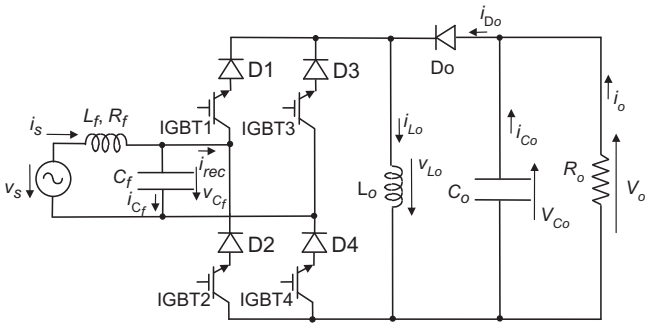


FIG. 35.79 Power factor buck-boost rectifier with four IGBTs.

values for all quantified $e(k)$ and $\Delta_e(k)$, can be stored in an array to serve as the decision-lookup table. This lookup table usually has a three-dimensional representation similar to Fig. 35.78. A microprocessor-based control algorithm just picks up output values from the lookup table.

35.5.3 Near Unity Power Factor Buck–Boost PWM Rectifier

35.5.3.1 Example 35.21: Fuzzy Logic Control of Unity Power Factor Buck–Boost Rectifiers

Consider the near unity power factor buck-boost rectifier of Fig. 35.79, where the diodes in series with the transistors enable them to withstand negative voltages.

The switched state-space model of this converter can be written as

$$\begin{cases} \dfrac{di_s}{dt} = -\dfrac{R_f}{L_f} i_s - \dfrac{1}{L_f} v_{C_f} + \dfrac{1}{L_f} v_s \\ \dfrac{dv_{C_f}}{dt} = \dfrac{1}{C_f} i_s - \dfrac{\gamma_p}{C_f} i_{L_o} \\ \dfrac{di_{L_o}}{dt} = \dfrac{\gamma_p}{L_o} v_{C_f} - \dfrac{\gamma\left(1 - \left|\gamma_p\right|\right)}{L_o} V_{C_o} \\ \dfrac{dV_{C_o}}{dt} = \dfrac{1 - \left|\gamma_p\right|}{C_o} i_{L_o} - \dfrac{1}{R_o C_o} V_o \end{cases} \tag{35.251}$$

where $\gamma_p = \begin{cases} 1, & (\textit{switch 1 and 4 are ON}) \ \textit{and} \ (\textit{switch 2 and 3 are OFF}) \\ 0, & \textit{all the switches are OFF} \\ -1, & (\textit{switch 2 and 3 are ON}) \ \textit{and} \ (\textit{switch 1 and 4 are OFF}) \end{cases}$

and $\gamma = \begin{cases} 1, & i_{L_o} > 0 \\ 0, & i_{L_o} \leq 0 \end{cases}$.

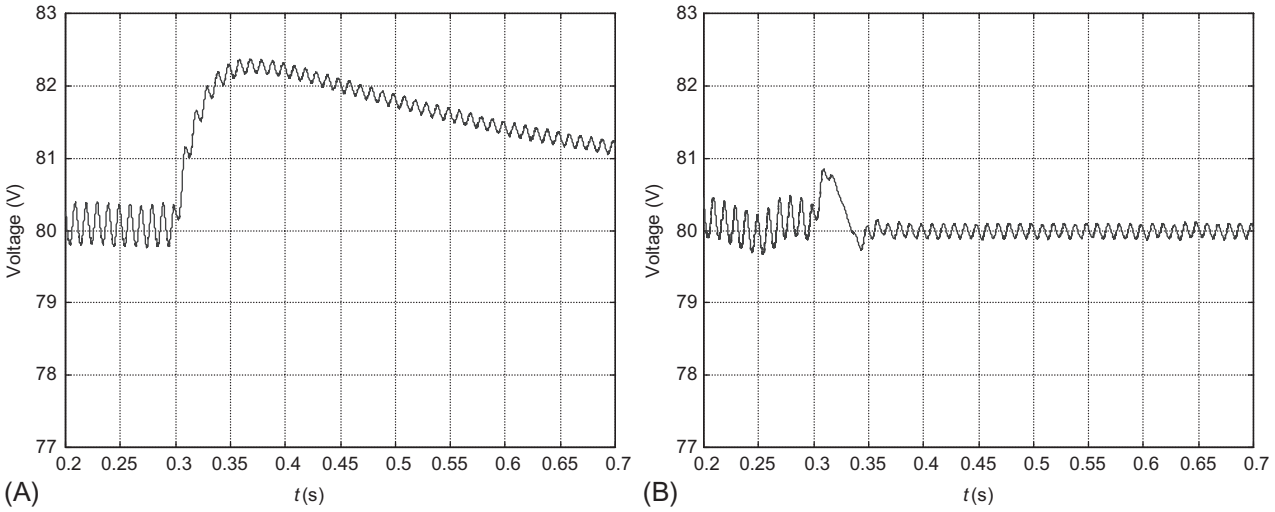


FIG. 35.80 Simulated result of the output voltage response to load disturbances ($R_o = 50$–$150\ \Omega$ at time 0.3 s): (A) PI control and (B) fuzzy logic control.

For comparison purposes, a PI output voltage controller is designed considering that a current-mode PWM modulator enforces the reference value for the i_s current (which usually exhibits a fast dynamics compared with the dynamics of V_{Co}). A first-order model, similar to Eq. (35.146), is obtained. The PI gains are similar to Eq. (35.116) and load-dependent ($K_p = C_o/(2T_d)$ and $K_i = 1/(2T_dR_o)$).

A fuzzy controller is obtained considering the approach outlined, with seven membership functions for the output voltage error, five for its change, and three membership functions for the output. The linguistic control rules are obtained as the ones depicted in Table 35.8, and the lookup table gives a mapping similar to Fig. 35.78. Performances obtained for the step response show a fuzzy controlled rectifier behavior close to the PI behavior. The advantages of the fuzzy controller emerge for perturbed loads or power supplies, where the low sensitivity of the fuzzy controller to system parameters is clearly seen (Fig. 35.80). Therefore, the fuzzy controllers can be advantageous for switching power converters with changing loads, power supply voltages, and other external disturbances.

35.6 Backstepping Control of Switching Power Converters

35.6.1 Principles of Backstepping Control

The backstepping control methodology [45,46] may be implemented using a recursive procedure interconnecting the choice of a candidate Lyapunov function with the design of the feedback control loop using the second method of Lyapunov stability (direct method). Backstepping offers tracking ability, stability, and robust control under conditions less restrictive than other methods [47]. Backstepping uses a strict-feedback form of the system model:

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} x \\ z_1 \\ \cdots \\ z_m \end{bmatrix} = \begin{bmatrix} f_0(x) + g_0(x)z_1 \\ f_1(xz_1) + g_1(xz_1)z_2 \\ \cdots \\ f_m(x, z_1, \ldots, z_m) + g_m(x, z_1, \ldots, z_m)u \end{bmatrix} \tag{35.252}$$

where $x \in \Re^n$, z_1–z_m are scalar state variables, f_0–f_m are nonlinearities dependent only on the state variables that are fed back [x, z_1,…, z_m] (strict feedback), and $g_i \neq 0$ is dependent on $(x, z_1, \ldots, z_i)$ for $1 \leq i \leq m$.

To apply the backstepping method [47] and stabilize the system to the origin (zero error), the following steps can be used:

(1) The recursive procedure starts with the subsystem of (35.252):

$$\frac{\mathrm{d}x}{\mathrm{d}t} = f_0(x) + g_0(x)z_1 \tag{35.253}$$

where z_1 is a state variable, whose dynamics can be enforced, called a stabilizing control input (or virtual control input).

(2) Proceed to obtain z_1 by defining the control objective $x = x_{ref}$, and considering the tracking error e_x,

$$e_x = x - x_{ref} \tag{35.254}$$

Select a Lyapunov function $V_1(x,t)$ globally positive definite, continuously differentiable, and radially

unbounded for all e_x. Denoting $V_1(x,t)$ by V_1 for simplicity, a candidate function for this case can be written as

$$V_1 = \frac{e_x^2}{2} \tag{35.255}$$

To guarantee the control solution is globally asymptotically stable, from Lyapunov's second method of stability, the time derivative of the positive-definite Lyapunov function V_1 must be globally negative definite for all (x,t), so that $V_1\dot{V}_1 < 0$ [47], as in the sliding-mode stability condition (35.92):

$$\frac{dV_1}{dt} = e_x\frac{de_x}{dt} < 0 \Rightarrow e_x\frac{de_x}{dt} = -k_1e_x^2 \Rightarrow \frac{de_x}{dt} = -k_1e_x \tag{35.256}$$

The constant k_1 must be positive definite (for stability). The last relation implies that the tracking error will converge to zero asymptotically with time constant $1/k_1$. Eq. (35.256) will be satisfied if $z_1 = z_{1ref}$. Using (35.254) and (35.253) in (35.256), then,

$$\frac{de_x}{dt} = -k_1e_x \Rightarrow \frac{dx}{dt} - \frac{dx_{ref}}{dt} = -k_1e_x \Rightarrow f_0(x) + g_0(x)z_{1ref} - \frac{dx_{ref}}{dt} = -k_1e_x \tag{35.257}$$

Solving for z_{1ref}, $(g_0(x) \neq 0)$, it results

$$z_{1ref} = \frac{-k_1\left(x - x_{ref}\right) - f_0(x) + \dfrac{dx_{ref}}{dt}}{g_0(x)} \tag{35.258}$$

(3) Proceed to the second recursion to obtain z_{2ref} by considering the tracking error

$$e_{z1} = z_1 - z_{1ref} \tag{35.259}$$

and select a recursively defined composite Lyapunov function V_2 positive definite:

$$V_2 = \frac{e_x^2}{2} + \frac{e_{z1}^2}{2} \tag{35.260}$$

The stability condition is $dV_2/dt < 0$:

$$\frac{dV_2}{dt} = e_x\frac{de_x}{dt} + e_{z1}\frac{de_{z1}}{dt} = -k_1e_x^2 - k_2e_{z1}^2 \tag{35.261}$$

where k_1 and k_2 must be positive (k_1 and $k_2 > 0$) for asymptotic stability.

From (35.261) using (35.254), (35.253), (35.259), and the second equation of (35.252), replacing $z_1 = e_{z1} + z_{1ref}$ in (35.257), and using the result of (35.257), it is written as

$$\begin{aligned} &e_x\left(f_0(x) + g_0(x)\left(e_{z1} + z_{1ref}\right) - \frac{dx_{ref}}{dt}\right) \\ &+ e_{z1}\left(f_1(xz_1) + g_1(xz_1)z_{2ref} - \frac{dz_{1ref}}{dt}\right) = \\ &= -k_1e_x^2 - k_2e_{z1}^2 \Rightarrow e_{z1}\left(g_0(x)e_x + f_1(xz_1) + g_1(xz_1)z_{2ref} - \frac{dz_{1ref}}{dt}\right) \\ &= -k_2e_{z1}^2 \end{aligned} \tag{35.262}$$

If dz_{1ref}/dt is independent of z_2, solving for z_{2ref} returns,

$$z_{2ref} = \frac{-k_2e_{z1} - g_0(x)e_x - f_1(xz_1) + \dfrac{dz_{1ref}}{dt}}{g_1(xz_1)} \tag{35.263}$$

(4) Proceed recursively (return to step 1) up to the definition of the control law of z_m, by selecting a recursively defined composite positive-definite Lyapunov function.

Alternatively, the integral action backstepping approach can be used in the first recursion.

Define a control objective $x = x_{ref}$ and consider the tracking error $e_x = x - x_{ref}$ as in (35.254). Now, add the integral of the tracking error e_I to the control action. The integral term is useful to ensure the convergence, in steady state, of the tracking error to zero regardless of nonmodeled disturbances and parameter uncertainty:

$$e_I = \int_0^t e_x d\tau \tag{35.264}$$

Use a positive-definite Lyapunov function V_I that weights (with k_0) the integral action to be added to the state feedback control law:

$$V_I = \frac{1}{2}k_0e_I^2 + \frac{e_x^2}{2} \tag{35.265}$$

Compute the time derivative of the Lyapunov function V_I and enforce it to be negative definite ($\dot{V}_I = -k_1e_x^2$, $k_1 > 0$):

$$\frac{dV_I}{dt} = k_0e_I\frac{de_I}{dt} + e_x\frac{de_x}{dt} = e_x\left(k_0e_I + \frac{de_x}{dt}\right) = -k_1e_x^2 \tag{35.266}$$

Eq. (35.266) will be satisfied if $z_1 = z_{1ref}$. Using (35.266), (35.254), and (35.253), then,

$$\begin{aligned} &k_0e_I + \frac{de_x}{dt} = -k_1e_x \Rightarrow k_0e_I + \frac{dx}{dt} - \frac{dx_{ref}}{dt} = -k_1e_x \Rightarrow \\ &\Rightarrow k_0e_I + f_0(x) + g_0(x)z_{1ref} - \frac{dx_{ref}}{dt} = -k_1e_x \end{aligned} \tag{35.267}$$

Solving for z_{1ref}, being $g_0(x) \neq 0$, and using (35.264), then,

$$z_{1ref} = \frac{-k_1 e_x - k_0 \int_0^t e_x d\tau - f_0(x) + \frac{dx_{ref}}{dt}}{g_0(x)} \tag{35.268}$$

This is the backstepping equivalent of a proportional-integral (PI) linear controller. Besides the proportional k_1 and integral k_0 gains, it adds the influence of the plant characteristics $f_0(x)$ and $g_0(x)$ and the derivative of the reference dx_{ref}/dt, by including the correspondent feed-forward terms, which are not in the linear PI.

35.6.2 Example 35.22: Backstepping Control of the Buck–Boost Converter

Consider the buck-boost converter (Fig. 35.81) strict-feedback averaged subsystem model (35.269), where D is the average value of the transistor duty-cycle $\delta(t)$:

$$\begin{aligned} \frac{dv_{PV}}{dt} &= \frac{i_{PV}}{C_1} - \frac{i_{L1}}{C_1} D \\ \frac{di_{L1}}{dt} &= \frac{v_{PV}}{L_1} D - \frac{v_p}{L_1}(1-D) \end{aligned} \tag{35.269}$$

In this example, the current source I_{PV} is a simple model of a photovoltaic panel and depends on v_{PV}. To obtain the maximum power from the panel, the v_{PV} voltage must be regulated to track the maximum power point (MPPT), defined by an MPPT algorithm [48,49], so that the control objective is $v_{PV} = v_{PVref}$, the control input is the averaged duty-cycle D, and the stabilizing virtual control input is i_{L1}:

(1) Consider the strict-feedback subsystem:

$$\frac{dv_{PV}}{dt} = \frac{i_{PV}}{C_1} - \frac{i_{L1}}{C_1} D \tag{35.270}$$

(2) Define the control objective $v_{PV} = v_{PVref}$ and the tracking error:

$$e_{PV} = v_{PV} - v_{PVref} \tag{35.271}$$

Define a positive-definite Lyapunov function V_{1b}:

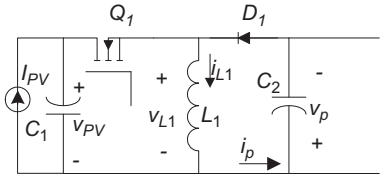


FIG. 35.81 Buck-boost dc/dc converter feed from a current source I_{PV}.

$$V_{1b} = \frac{e_{PV}^2}{2} \tag{35.272}$$

The time derivative of V_{1b} must be negative definite for asymptotic stability. Similarly to (35.256) and considering (35.270),

$$\begin{aligned} \frac{de_{PV}}{dt} &= \frac{dv_{PV}}{dt} - \frac{dv_{PVref}}{dt} = -k_{PV} e_{PV} \Rightarrow \frac{i_{PV}}{C_1} - \frac{i_{L1ref}}{C_1} D - \frac{dv_{PVref}}{dt} \\ &= -k_{PV} e_{PV} \end{aligned} \tag{35.273}$$

where k_{PV} is a positive constant, selected to impose the time constant of the tracking error vanishing asymptotically to zero. Then, the virtual control law (stabilizing function) reference value i_{L1ref} for the i_{L1} current ($i_{L1} = i_{L1ref}$) if ($D \neq 0$) is

$$i_{L1ref} = \frac{C_1 k_{PV} e_{PV}}{D} + \frac{i_{PV}}{D} - \frac{C_1}{D} \frac{dv_{PVref}}{dt} \tag{35.274}$$

Note that this reference current might be enforced using a sliding-mode controller and $D = V_P/(V_{PV} + V_P)$. To consider parameter uncertainty and disturbances, the integral action backstepping could be used.

(3) Start the second recursion to obtain the control input averaged duty-cycle D, by defining the inductor current i_{L1} error e_{iL1}:

$$e_{iL1} = i_{iL1} - i_{iL1ref} \tag{35.275}$$

Select a suitable composite positive-definite Lyapunov function V_{2b}:

$$V_{2b} = \frac{e_{PV}^2}{2} + \frac{e_{iL1}^2}{2} \tag{35.276}$$

Apply the asymptotic stability condition, where k_{PV} and k_{iL} are positive constants:

$$\frac{dV_{2b}}{dt} = e_{PV} \frac{de_{PV}}{dt} + e_{iL1} \frac{de_{iL1}}{dt} = -k_{PV} e_{PV}^2 - k_{iL} e_{iL1}^2 \tag{35.277}$$

As this converter is a nonminimum-phase system, the stabilizing function reference value i_{L1ref} in (35.274) depends on the control input D. To evaluate de_{iL1}/dt in (35.277), first compute di_{L1ref}/dt using (35.273), (35.274) and (35.275):

$$\begin{aligned} \frac{di_{L1ref}}{dt} &= -k_{PV} e_{iL1} - \frac{C_1 k_{PV}^2}{D} e_{PV} + \frac{1}{D} \frac{di_{PV}}{dt} - \frac{C_1}{D} \frac{d^2 v_{PVref}}{dt^2} \\ &\quad - \frac{i_{L_1 ref}}{D} \frac{dD}{dt} \end{aligned} \tag{35.278}$$

Substitute (35.270) in (35.277), and use the second equation of (35.269) for di_{L1}/dt, replacing $iL1$ by $e_{iL1}+i_{L1ref}$, and use (35.278) to obtain

$$\frac{dV_{2b}}{dt}=e_{PV}\frac{de_{PV}}{dt}+e_{iL1}\frac{de_{iL1}}{dt}=e_{PV}\left(\frac{i_{PV}}{C_1}-\frac{e_{iL1}+i_{L_1ref}}{C_1}D-\frac{dv_{PVref}}{dt}\right)+$$

$$+e_{iL1}\left(\frac{v_{PV}}{L_1}D-\frac{v_p}{L_1}(1-D)+k_{PV}e_{iL1}+\frac{C_1k_{PV}^2}{D}e_{PV}-\frac{1}{D}\frac{di_{PV}}{dt}\right.$$

$$\left.+\frac{C_1}{D}\frac{d^2v_{PVref}}{dt^2}+\frac{i_{L_1ref}}{D}\frac{dD}{dt}\right)=$$

$$=-k_{PV}e_{PV}^2-k_{iL}e_{iL1}^2 \tag{35.279}$$

Remember (35.273) to receive

$$-e_{PV}^2k_{PV}-e_{PV}\frac{e_{iL1}}{C_1}D$$

$$+e_{iL1}\left(\begin{array}{l}\frac{-v_p}{L_1}+\frac{v_{PV}+v_p}{L_1}D+k_{PV}e_{iL1}+\\+\frac{C_1k_{PV}^2}{D}e_{PV}-\frac{1}{D}\frac{di_{PV}}{dt}+\frac{C_1}{D}\frac{d^2v_{PVref}}{dt^2}+\frac{i_{L_1ref}}{D}\frac{dD}{dt}\end{array}\right)=$$

$$=-k_{PV}e_{PV}^2-k_{iL}e_{iL1}^2 \tag{35.280}$$

Simplify and group terms relative to e_{iL1}:

$$e_{iL1}\left(\begin{array}{l}\frac{-v_p}{L_1}+\frac{v_{PV}+v_p}{L_1}D+k_{PV}e_{iL1}+\\+\left(\frac{C_1k_{PV}^2}{D}-\frac{D}{C_1}\right)e_{PV}-\frac{1}{D}\frac{di_{PV}}{dt}+\frac{C_1}{D}\frac{d^2v_{PVref}}{dt^2}+\frac{i_{L_1ref}}{D}\frac{dD}{dt}\end{array}\right)$$

$$=-k_{iL}e_{iL1}^2 \tag{35.281}$$

Solve for dD/dt and integrate to obtain the duty-cycle D controller ($i_{L1ref}\neq 0$):

$$D=\int_0^\tau\left[\frac{1}{i_{L_1ref}}\left(-e_{iL1}(k_{iL}+k_{PV})D+\frac{v_p}{L_1}D-\frac{v_{PV}+v_p}{L_1}D^2\right.\right.$$

$$\left.\left.-\left(C_1k_{PV}^2-\frac{D^2}{C_1}\right)e_{PV}+\frac{di_{PV}}{dt}-C_1\frac{d^2v_{PVref}}{dt^2}\right)\right]d\tau \tag{35.282}$$

This result shows that the duty-cycle controller D has to go back to the input through an integrator.

Using this procedure, backstepping can stabilize nonminimum-phase systems, provided it is known how to obtain the origin stabilizing virtual control input.

Fig. 35.82 shows the buck-boost backstepping controller (35.282) transient response to a step change in v_{PVref} from 18–15 V at t = 0.3 s. The buck-boost switching frequency is

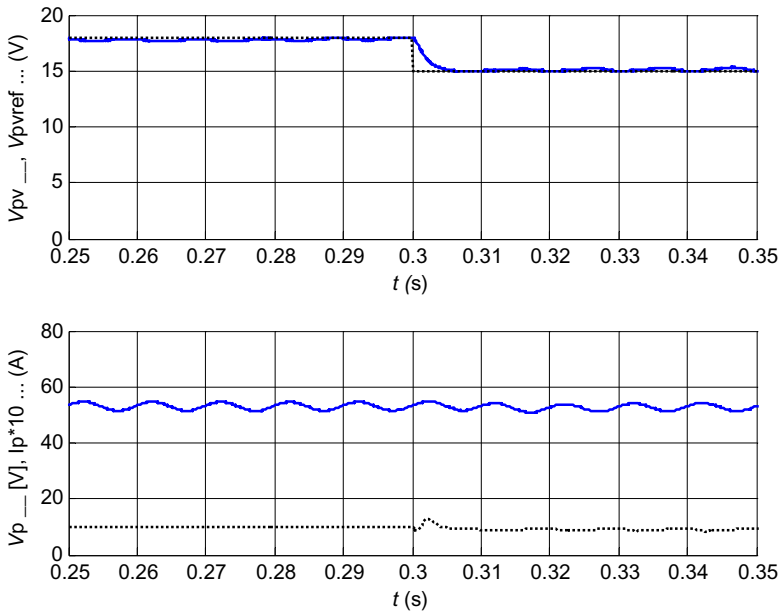


FIG. 35.82 Upper graph, the v_{PV} controlled voltage (solid gray line) and its reference (dotted line) and bottom graph, the buck-boost v_p output voltage (solid line) and the average value of the i_p (× 10) current (dotted line).

15 kHz, and controller gains are $k_{PV}=150$ and $k_{iL}=1500$ ($C_1=1$ mF, $C_2=1$ mF, $L_1=3$ mH, and $I_{PV}\approx 3$ A). The buck-boost load is a single-phase inverter connected to a 50 Hz grid. Voltage dynamics is nearly a first-order system response, even with a nonlinear load, whose dynamics was not included in the controller design. A small steady-state error is visible due to nonmodeled switch and inductor resistors and modulator delay. Response time is less than 5 ms.

35.6.3 Example 35.23: Backstepping Control of a Single Phase Inverter

Consider a single-phase dc-ac inverter (Fig. 35.83) that enforces a dc voltage v_p at the output capacitor of the previous buck-boost (Fig. 35.81), using a fixed-frequency PWM modulator to inject a sinusoidal i_{L2} current into the grid, so that the power received from the buck-boost is injected in the grid v_R.

Assuming unity power factor, unity efficiency, and the output capacitor of the buck-boost converter, the strict-feedback averaged model can be written as

$$\begin{aligned}\frac{dv_p^2}{dt}&=\frac{2}{C_2}i_p v_p-\frac{2}{C_2}v_R i_{L2}\\ \frac{di_{L2}}{dt}&=\frac{\beta v_p}{L_2}-\frac{v_R}{L_2}\end{aligned}\tag{35.283}$$

where the voltage v_{pwm} is obtained from v_p using the sinusoidal modulating waveform β, such as $v_{pwm}=\beta\ v_p$. The stabilizing virtual control input will be the root mean square value I_{L2RMS} of the i_{L2} current. The control input is the modulation waveform β:

(1) Consider the strict-feedback subsystem:

$$\frac{dv_p^2}{dt}=\frac{2}{C_2}i_p v_p-\frac{2}{C_2}v_R i_{L2}\tag{35.284}$$

(2) Define the control objective $v_p^2=v_{pref}^2$ and the tracking error:

$$e_{vp2}=v_p^2-v_{pref}^2\tag{35.285}$$

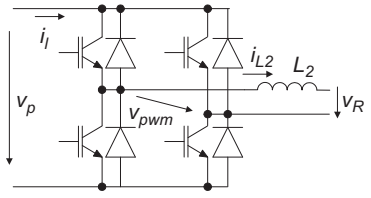


FIG. 35.83 Single-phase inverter fed from the buck-boost.

Select a suitable positive-definite Lyapunov function:

$$V_{vp2}=\frac{e_{vp2}^2}{2}\tag{35.286}$$

To ensure asymptotic stability, the time derivative of this Lyapunov function must be negative, which is true if

$$\frac{de_{vp2}}{dt}=-k_{vp2}e_{vp2}\tag{35.287}$$

where k_{vp2} is a positive constant. The stability condition will be satisfied if the root mean square value of i_{L2} is I_{L2RMS} in (35.284), giving

$$\frac{2\left(i_p v_p-I_{L2RMS}\ v_R\right)}{C_2}-\frac{dv_{pref}^2}{dt}=-k_{vp2}e_{vp2}\tag{35.288}$$

The virtual control law (stabilizing function) is I_{L2RMS} (with $v_R\neq 0$):

$$I_{L2RMS}=\frac{C_2 k_{vp2}e_{vp2}}{2v_R}+i_p\frac{v_p}{v_R}-\frac{C_2}{2v_R}\frac{dv_{pref}^2}{dt}\tag{35.289}$$

This I_{L2RMS} value is "constant" regarding the switching period of the inverter semiconductors.

(3) Knowing that the inverter input power is a constant at the scale of the switching period whereas the inverter output power varies along the v_R grid period (the mean value is the active power), the converter fast dynamics (i_{L2} current) and slow dynamics (DC v_p voltage) must be separated. Otherwise, the backstepping controller would impose the energy balance during the semiconductor switching period, distorting the i_{L2} current. This sinusoidal current may be written as $i_{L2ref}=I_{L2RMS}\ v_{Rpu}$, being the tracking error:

$$e_{iL2}=i_{L2ref}-i_{L2}\tag{35.290}$$

Select a positive-definite Lyapunov function:

$$V_{iL2}=\frac{e_{iL2}^2}{2}\tag{35.291}$$

Use the stability condition, with a positive constant k_{iL2}, and the second equation of (35.283) to write

$$\frac{de_{iL2}}{dt}=-k_{iL2}e_{iL2}\Rightarrow\frac{di_{L2ref}}{dt}-\frac{\beta v_p-v_R}{L_2}=-k_{iL2}e_{iL2}\tag{35.292}$$

Solve to obtain the modulation waveform β ($v_p\neq 0$):

$$\beta=\frac{L_2\dfrac{di_{L2ref}}{dt}+v_R+k_{iL2}L_2e_{iL2}}{v_p}\tag{35.293}$$

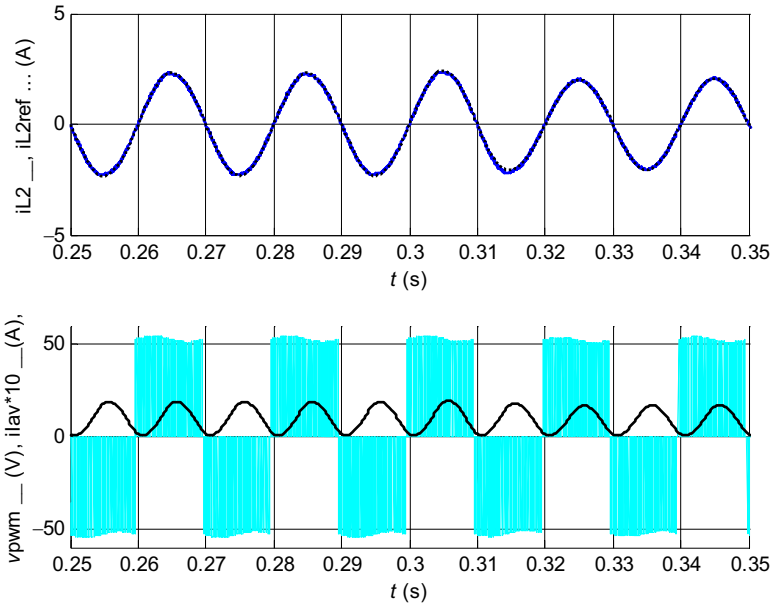


FIG. 35.84 Upper graph, the i_{L2} ac grid current (solid line) and its reference (dotted line) and bottom graph, the inverter v_{pwm} output voltage (gray line) and the average value of the i_I ($\times$ 10) inverter input current (black solid line).

Fig. 35.84 shows the buck-boost-fed single-phase inverter backstepping controller ((35.293) and (35.289)) response to the step change in v_{PVref} of the buck-boost from 18–15 V at $t = 0.3$ s. The PWM modulator frequency is 15 kHz, and controller gains are $k_{vp2} = 0.05$ and $k_{iL2} = 0.025$ ($L_2 = 10$ mH, $v_R \approx 45$ V and 50 Hz). The ac current is almost not distorted by v_{PVref} step change, and its total harmonic distortion is less than 2%.

35.7 Conclusions

Control techniques for switching power converters were reviewed. Linear controllers based on state-space averaged models or circuits are well established and suitable for the application of linear systems control theory. Obtained linear controllers are useful, if the converter operating point is almost constant and the disturbances are not relevant. For changing operating points and strong disturbances, linear controllers can be enhanced with nonlinear, antiwindup, soft-start, or saturation techniques. Current-mode control will also help to overcome the main drawbacks of linear controllers.

Sliding mode is a nonlinear approach well adapted for the variable structure of the switching power converters. The critical problem of obtaining the correct sliding surface was highlighted, and examples were given. The sliding-mode control law allows the implementation of the switching power converter controller, and the switching law gives the PWM modulator. The system variables to be measured and fed back are identified. The obtained reduced-order dynamics is not dependent on system parameters or power supply (as long as it is high enough), presents no steady-state errors, and has a faster response speed (compared with linear controllers), as the system order is reduced and nonidealities are eliminated. Should the measure of the state variables be difficult, state observers may be used, with steady-state errors easily corrected. Sliding-mode controllers provide robustness against bounded disturbances and an elegant way to obtain the controller and modulator, using just the same theoretical approach. Fixed-frequency operation was addressed and solved, together with the short-circuit-proof operation. Presently, fixed-frequency techniques were applied to converters that can only operate with fixed frequency. Sliding-mode techniques were successfully applied to MIMO switching power converters and to multilevel converters, solving the capacitor voltage divider equalization. Sliding-mode control needs more information from the controlled system than do the linear controllers but is probably the most adequate tool to solve the control problem of switching power converters.

Predictive optimum control of power converters is based on a detailed nonlinear direct dynamics model that includes converter bounds. The predictive optimum algorithm uses the model to forecast in real time the converter future behavior, which is dependent on the applied control vector. The minimization of a suitable cost functional gives the optimum vector. Predictive optimum controllers designed to minimize converter output errors, together with the switching frequency, present better performances than sliding-mode controllers, even when controlling nonlinear outputs with cross coupled dynamics. Fast predictive controllers, using the converter inverse dynamics, designed to save computation power, also show promising results.

Fuzzy logic controller synthesis was briefly presented. Fuzzy logic controllers are based on human experience and intuition and do not depend on system parameters or operating points. Fuzzy logic controllers can be easily applied to various types of power converters having the same qualitative dynamics. Fuzzy logic controllers, like sliding-mode controllers, show robustness to load and power supply perturbations, semiconductor nonidealities (such as switch delays or uneven conduction voltage drops), and dead times. The controller implementation is simple, if based on the offline concept. Online implementation requires a fast microprocessor but can include adaptive techniques to optimize the rule base and/or the database.

Backstepping control was explained using a strict-feedback form of the converter dynamic model and a recursive approach. The procedure correctly selects positive-definite Lyapunov functions and designs the feedback control loop to ensure stability using Lyapunov's second method. Integral action control may be included to overcome nonmodeled disturbances and parameter uncertainty, ensuring convergence, in steady state, of the tracking error to zero. Backstepping control is a robust method to be used with conventional fixed-frequency duty-cycle modulators, being ideal for nonminimum-phase converters, while needing less computing power compared with predictive controllers.

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References

[1] B.K. Bose, Power Electronics and AC Drives, Prentice-Hall, New Jersey, 1986.
[2] J. Kassakian, M. Schlecht, G. Verghese, Principles of Power Electronics, Addison Wesley, Reading, MA, USA, 1992.
[3] M. Rashid, Power Electronics: Circuits, Devices and Applications, second ed., Prentice-Hall International, New Jersey, USA, 1993.
[4] J. Fernando Silva, Electrónica Industrial: Semicondutores e Conversores de Potência, série Manuais Universitários, Fundação Calouste Gulbenkian, Lisboa, ISBN 978-972-31-1499-7, 2013, 740 pp.
[5] N. Mohan, T. Undeland, W. Robbins, Power Electronics: Converters, Applications, and Design, third ed., John Wiley, New York, NY, 2002.
[6] K.K. Sum, Switched Mode Power Conversion, Marcel Dekker Inc., New York, USA, 1984
[7] H. Bühler, Electronique de Réglage et de Commande, Traité D'électricité, vol. XV, éditions Georgi, 1979.
[8] J.D. Irwin (Ed.), The Industrial Electronics Handbook, CRC/IEEE Press, Boca Raton, USA, 1996.
[9] G. Chryssis, High Frequency Switching Power Supplies, McGraw-Hill, USA, 1984.
[10] V.I. Utkin, Sliding Modes and Their Application on Variable Structure Systems, MIR Publishers, Moscow, Russia, 1978.
[11] V.I. Utkin, Sliding Modes in Control Optimization, Springer-Verlag, Berlin, Germany, 1981.
[12] K. Ogata, Modern Control Engineering, third ed., Prentice-Hall International, New Jersey, USA, 1997.
[13] W.S. Levine (Ed.), The Control Handbook, CRC/IEEE Press, Boca Raton, USA, 1996.
[14] J. Fernando Silva, Electrónica Industrial, Fundação Calouste Gulbenkian, Lisboa, 1998.
[15] J. Fernando Silva, Sliding mode control design of control and modulator electronics for power converters, special issue on power electronics, J. Circuit. Syst. Comp. 5 (3) (1995) 355–371.
[16] J.F.A. Martins, A.J. Pires, J.F. Silva, A novel and simple current controller for three-phase PWM power inverters, IEEE Trans. Ind. Electron. 45 (5) (1998) 802–805.
[17] J. Fernando Silva, Sliding mode control of voltage sourced boost-type reversible rectifiers, in: Proc. IEEE/ISIE'97 Conference (ISBN 0-7803-3937-1), Guimarães, Portugal, Julho, vol. 2, 1997, pp. 329–334.
[18] J. Fernando Silva, Sliding mode control of boost type unity power factor PWM rectifiers, Special Section on High-Power-Factor Rectifiers IIEEE Trans. on Industrial Electronics . ISBN 0278-004646 (3) (1999) 594–603.
[19] J. Silva, V. Pires, S. Pinto, J. Barros, Advance control methods for power converters, Transactions on Mathematics and Computers in Simulation, IMACS, 63 Elsevier, 2003 3–5, pp. 281–295.
[20] L. Encarnação, J. Fernando Silva, Stability Condition Based Sliding Mode Modulators for Multilevel Power Converters, in: 35th Annual Conference of the IEEE Industrial Electronics Society, IECON Porto, Portugal, 2009.
[21] J. Verveckken, J.F. Silva, J.D. Barros, J. Driesen, Direct power control of series converter of unified power-flow controller with three-level neutral point clamped converter, IEEE Trans. Power Delivery 27 (4) (2012) 1772–1782.
[22] José Rodriguez, Special section on matrix converters, IEEE Trans. Ind. Electron. 49 (2) (2002).
[23] S. Pinto, J. Silva, Sliding mode direct control of matrix converters, IET Proc. Electric Power Applications 1 (3) (May 2007) 439–448.
[24] A. Alesina, M. Venturini, Analysis and design of optimum-amplitude nine-switch direct AC-AC converters, IEEE Trans. Power Electron. 4 (1) (1989) 101–112.
[25] S. Pinto, J. Silva, Matrix converters: a new approach on venturini modulation technique, in: Proc. PEMC'04 Conference, Riga, Latvia, 2004.
[26] W. Kwon, G. Cho, Analyses of static and dynamic characteristics of practical step-up nine-switch matrix convertor, IEE Proceedings B, vol. 140, No. 2, March 1993.
[27] S. Pinto, J. Silva, P. Gambôa, Current Control of a Venturini Based Matrix Converter, in: Proc. ISIE'06, Montréal, Canada, 2006.
[28] M. Athans, Lecture Notes on Design of Robust Multivariable Feedback Control System, Prof. of Electrical Engineering (emeritus),

MIT, Visiting Research Prof ISR/IST, athans@isr.ist.utl.pt, Lisboa, 2004.
[29] J.F. Silva, Predictive Control of Rectifiers by Simulation with Commutation failures Elimination, Ph.D. Thesis in Electrical and Computer Enginnering, IST, TULisbon, Lisboa 1989 (in Portuguese "Controlo Preditivo por Simulação para Rectificadores com Eliminação de Falhas de Comutação").
[30] J.F. Silva, B. Borges, António A. Anunciada, Improving control strategies for HF resonant link converters: the Current Mode Predictive Modulator, in: Power Electronics Specialists Conference, IEEE PESC'91, ISSN 0275-9306, Boston, USA, 1991, pp. 268–275.
[31] J.F. Silva, Detailed Model Predictive Control for a 3 Phase Thyristor Current Source, IMACS-MCTS, Moudni, Borne, Tzafestas (Editors), ISBN 29502908-1-1, vol. I, 1991, pp. 236–241.
[32] S. Muller, U. Ammann, S. Rees, New time-discrete modulation scheme for matrix converters, IEEE Trans. Ind. Electron. 52 (6) (2005) 1607–1615.
[33] D. Barros, J.F. Silva, Sliding mode assisted preditive pseudo-optimal control for three-phase three-level converters, in: 10th International Conference on Optimization of Electrical and Electronic Equipment OPTIM2006, Vol. 2, 2006.
[34] J. Rodríguez, J. Pontt, C.A. Silva, P. Correa, P. Lezana, P. Cortés, U. Ammann, Predictive current control of voltage source inverter, IEEE Trans. Ind. Electron. 54 (1) (2007) 495–503.
[35] J.D. Barros, J.F. Silva, Optimal predictive control of three-phase NPC multilevel inverter: comparison to robust sliding mode controller, in: IEEE 38th Annual Power Electronics Specialists Conference (PESC07), Orlando, USA, 2007, pp. 2061–2067.
[36] R. Vargas, P. Cortes, U. Ammann, J. Rodriguez, J. Pontt, Predictive control of a three-phase neutral-point-clamped inverter, IEEE Trans. Ind. Electron. 54 (5) (October 2007) 2697–2705.
[37] J.D. Barros, J.F. Silva, Optimal predictive control of three-phase npc multilevel converter for power quality applications, IEEE Trans. Ind. Electron. 55 (10) (2008) 3670–3681.
[38] J.D. Barros, J.F. Silva, Multilevel optimal predictive dynamic voltage restorer, Special issue on multilevel converters, IEEE Trans. Ind. Electron. 57 (8) (2010).
[39] J. Monteiro, J.F. Silva, S.F. Pinto, J. Palma, Linear and sliding mode control design for matrix converter based unified power flow controllers, IEEE Trans. Power Electron. 29 (7) (2014) 3357–3367.
[40] M. Chaves, E. Margato, J.F. Silva, S.F. Pinto, J. Santana, Fast optimum-predictive control and capacitor voltage balancing strategy for bipolar back-to-back NPC converters in high-voltage direct current transmission systems, IET Gener. Transm. Distrib. 5 (3) (2011) 368–375.
[41] L.A. Zadeh, Fuzzy Sets, Inf. Control. 8 (1965) 338–353.
[42] L.A. Zadeh, Outline of a new approach to the analysis of complex systems and decision process, IEEE Trans. Syst. Man Cybern. SMC-3 (1973) 28–44.
[43] H.J. Zimmermann, Fuzzy Sets: Theory and its Applications, Kluwer-Nijhoff, New York, 1995.
[44] A. Candel, G. Langholz, Fuzzy Control Systems, CRC Press, Boca Raton, USA, 1994.
[45] K. Ezal, Z. Pan, P.V. Kokotovic, Locally optimal and robust backstepping design, IEEE Trans. Autom. Control 45 (2) (2000) 260–271.
[46] R.A. Freeman, P.V. Kokotovic, Tools and procedures for robust control of nonlinear systems, in: 33rd IEEE Conference on Decision and Control, 4 2003, pp. 3458–3463.
[47] H.K. Khalil, Nonlinear Systems, third ed., Prentice Hall, Upper Saddle River NJ, 2002.
[48] A.D. Martin, J.R. Vazquez, Backstepping controller design to track maximum power in photovoltaic systems, Automatika 55 (1) (2014) 22–31.
[49] Aranzazu D. Martin, J.M. Cano, Fernando A. Silva, Jesus R. Vazquez, Back-stepping control of smart-grid connected distributed photovoltaic power supplies for telecom equipment, IEEE Trans. Energy Convers. 30 (4) (2015) 1496–1504.
[50] S. Pinto, J. Fernando Silva, Direct control method for matrix converters with input power factor regulation, in: IEEE Proc. PESC'2004, CD ROM ISBN 0-7803-8400-8, Aachen, Germany, June 2004, pp. 2366–2372.
[51] M. Chaves, E. Margato, J.F. Silva, S.F. Pinto, J. Santana, HVDC transmission systems: bipolar back-to-back diode clamped multilevel converter with fast optimum-predictive control and capacitor balancing strategy, Elsevier, Electr. Power Syst. Res. 81 (7) (2011) 1436–1445.

36

Fuzzy-Logic Applications in Electric Drives and Power Electronics

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36.1 Introduction

Improving the popular proportional-integral-derivative (PID) controller using fuzzy logic (FL) is currently an important research topic. Years of various applications have shown different techniques for customizing the PID controller [1–7]. Recent work by Sant [1] employs an FL controller combined with a classical PID controller with a switching function between them for speed control of a motor drive. The switching algorithm allows each controller type to perform better under different operations. In another recent example, Hohan [2] has developed a fuzzy-PID controller based upon the error, the difference in error, and the difference to create a delta change in the control signal at each time step. Hohan includes analytic stability analysis for bounded inputs, important for fuzzy systems to gain acceptance among control engineers. The

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application of fuzzy reasoning to improve the PID controller is evident in the research community today to build state-of-the-art control systems. Recent work on self-tuning PID controllers demonstrates adaptive control of motor drive systems. Typically, an engineer might retune the gains of a nominal PID controller during operation, but an adaptive PID system autonomously tunes gains as performance diminishes. The work of Rubaai [3] employs a genetic algorithm to evolve optimal scale factors of fuzzy-based PID gains for improved control of a motor drive. This genetic-based scale factor in conjunction with FL gain selection enhances the sensitivity of the PID control to error. Another class of fuzzy-PID control design mimics PID control via blending FL networks with absolute and incremental control values at a given control time step. The work of Kuo [4] employs two FL structures to formulate a control of a suspension system. One FL mimics PD control, while the other FL generates a change in control to mimic a PI control signal. These FL structures adapt using a genetic algorithm as well. The work of Hu [5] also employs fuzzy-PD and fuzzy-PI elements as part of a control strategy. Li [6] designs an FL based on error and error derivative to generate an initial control estimate that then feeds a PI logic and a PD logic. This work demonstrates robustness of the control algorithm through simulations of a dynamic model. The recent work of Masiala [7] demonstrates incremental fuzzy-PI control of an induction motor drive. For Masiala, the FL decision at each time step modifies the control current based on the error and a change in error. All these controllers use FL to generate absolute and incremental control signals to mimic control techniques seen in PID control. Kalman filter (KF) is another research topic that has been applied to a wide range of engineering disciplines. For a linear system, the KF is an established control design feature, but the improved application of variants of the KF to account for nonlinearity in systems inspires research today. Barut [8] employs an extended Kalman filter (EKF) for a speed sensorless control of an induction motor. This work depends on high-fidelity equations of motion model and noise characteristics. Szabat [9] demonstrates an adaptively tuned EKF for control of an industrial drive. Ahn [10] designs an EKF algorithm to update parameters of parallel FL systems, which generate a PID gain set for control of a motor drive system. Treating the controller as a process and deriving appropriate derivatives allow for adaptive update to the FL components. So, while PID control is a commonly known algorithm, current research applications of adaptive tuning are yielding better tuned PID systems. The artificial neural network (ANN) is a computational data structure modeled after the firing of neurons in the brain. Training exercises may adjust the parameters within the ANN to improve modeling capabilities. The work of Lary [11] details an EKF algorithm for training an ANN to model correlations between chemical compounds. Singhal [12] shows that the EKF training algorithm treats all ANN parameters as a state vector, and thus, the ANN becomes a nonlinear stationary process. Research experience demonstrates that the EKF training compares favorably to the BP update method in terms of iterations of training epochs, but with higher computational cost per time step. The ANN is an important contribution to the control field. The fuzzy neural network (FNN) combines aspects of FL and the ANN and is at the state of the art in control research today. For example, recent work of Ho [13] simulates PID control using an FNN structure that updates time constants in the dynamic models that generate the PID gains online. Ho compares the orthogonal simulated annealing learning technique to a genetic technique to improve performance of the FNN portion of the controller. Campo [14] designs an embedded hardware FNN updated by the Takagi-Sugeno training method for performance improvement. Such a chip enables for a fuzzy system embedded into a hardware control loop. Uddin [15] also developed a hybrid neuro-fuzzy-PI controller adapted by a real-coded genetic algorithm to control an IPMSM. In this case, a fuzzy basis function network similar to an FNN output PI gains sensitive to error conditions. The cutting-edge work of many researchers today relies on the FNN to improve the performance of fuzzy control systems in electric applications.

36.2 PI/PD-Like Fuzzy Control Structure

The FNN PI/PD-like fuzzy controller using EKF control structure presented in this chapter is an instantiation of a feedback control loop. The FNN PI/PD-like fuzzy consists of two independent fuzzy structures, namely, fuzzy-PD controller and fuzzy-PI controller. EKF technique is used to modify the weights and the membership functions of the FNN PI/PD controller to adaptively control the rotor speed of the drive system. The summation of the outputs of the two FNNs forms the control signal. Fig. 36.1 shows the architecture of the neural-fuzzy PI-/PD-based EKF learning scheme. The control structure is anticipated to accommodate the robust stabilization and disturbance rejection problems. The fuzzy controller generates a control signal based upon two FL structures. The first structure is a fuzzy PD that generates a fuzzy-PD control signal. The second structure is a fuzzy PI that generates an incremental fuzzy-PI control signal.

$$\mathrm{UPD} = \mathrm{FLPD}(e_{\mathrm{filt}}, \Delta e_{\mathrm{filt}})$$

$$\Delta\mathrm{UPI} = \mathrm{FLPI}(e_{\mathrm{filt}}, \Delta e_{\mathrm{filt}})$$

The incremental fuzzy-PI signal sums with the previous fuzzy-PI signal to generate the fuzzy-PI signal for the time step at hand. The fuzzy-PI/fuzzy-PD controller generates a control signal with the summation of the fuzzy-PI/fuzzy-PD control signals:

$$U = \mathrm{UPD} + \mathrm{UPI}$$

The control signal is limited by a discontinuous range-limiting saturation element. The saturation equation caps the signal between a maximum and minimum value:

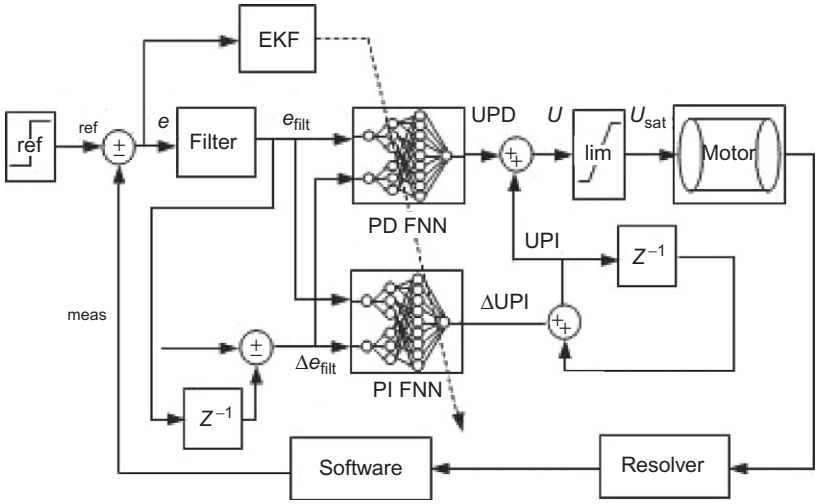


FIG. 36.1 FNN PI/PD-like fuzzy control structure.

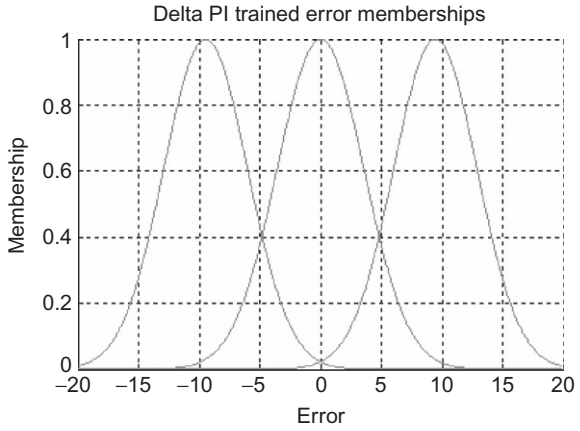


FIG. 36.2 Trained membership function for speed error.

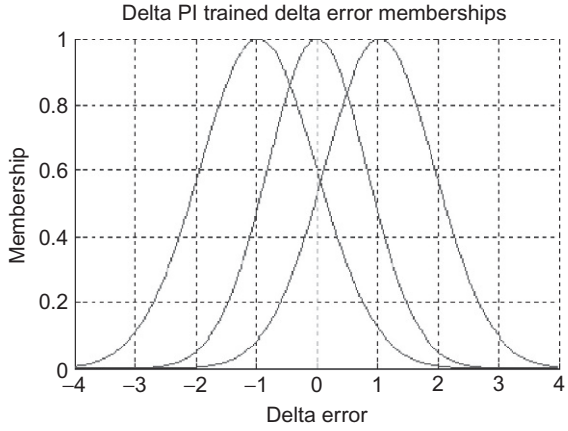


FIG. 36.3 Trained membership functions for the delta speed error.

$$u_{sat} = \begin{cases} u_{max} & \text{if } U > u_{max} \\ u_{min} & \text{if } U < u_{min} \\ U & \text{otherwise} \end{cases}$$

36.2.1 Fuzzy-Based PI Controller

The fuzzy-PI system implements an FL for the PI control signals e_{filt} and Δe_{filt}, the error and the delta error, respectively, the linguistic inputs to the system. The FL output is the PI control ΔUPI signal. The error signal has three fuzzy variables: positive (P), zero (Z), and negative (N). The delta error signal has three fuzzy variables: positive (P), zero (Z), and negative (N). The membership function for each fuzzy variable is a Gaussian function. Figs. 36.2 and 36.3 display the trained membership functions for the fuzzy inputs.

The linguistic control rules are established considering the dynamic behavior of the BLDC drive system and analyzing the error and its variation. The fuzzy inference system has nine rules.

Rule 1: IF speed error is negative (N) AND delta speed error is negative (N), THEN the fuzzy-PI control voltage (output of FL) is negative large (NL). This rule pertains to the condition that $w_{ref} < w_{meas}$ and that the difference between them is increasing. Thus, the control action must act to change the error momentum and bring the motor rate back down to the reference rate. Therefore, a large negative change in control voltage is necessary.

Rule 2: IF speed error is negative (N) AND delta speed error is zero (Z), THEN the fuzzy-PI control voltage (output of FL) is negative medium (NM). This rule pertains to the condition that $w_{ref} < w_{meas}$ and that the difference between them is steady. Thus, the control action need not change the error momentum but still bring the motor rate back down to the reference rate. Therefore, a medium negative change in control voltage is necessary.

Rule 3: IF speed error is zero (Z) AND delta speed error is negative (N), THEN the fuzzy-PI control voltage (output of FL) is negative small (NS). This rule pertains to the condition that $w_{ref} = w_{meas}$ but tending toward $w_{ref} < w_{meas}$ as the error

trends more negative. Thus, the control action must act to halt the error momentum but maintain the motor rate being close to the reference rate. Therefore, a small negative change in control voltage is necessary.

Rule 4: IF speed error is negative (N) AND delta speed error is positive (P), THEN the fuzzy-PI control voltage (output of FL) is zero (ZE). This rule pertains to the condition that $w_{ref} < w_{meas}$ and that the difference between them is decreasing. Thus, the control action of nothing allows the error momentum to bring the motor rate back down to the reference rate. Therefore, no change in control voltage is necessary.

Rule 5: IF speed error is zero (Z) AND delta speed error is zero (Z), THEN the fuzzy-PI control voltage (output of FL) is zero (ZE). This rule pertains to the condition that $w_{ref} = w_{meas}$ and that the difference between them is steady. Thus, the control action of nothing allows the error momentum to remain negligible to leave the motor rate at the reference rate. Therefore, no change in control voltage is necessary.

Rule 6: IF speed error is positive (P) AND delta speed error is positive (P), THEN the fuzzy-PI control voltage (output of FL) is positive large (PL). This rule pertains to the condition that $w_{ref} > w_{meas}$ and that the difference between them is increasing. Thus, the control action must act to change the error momentum and bring the motor rate back up to the reference rate. Therefore, a large positive change in control voltage is necessary.

Rule 7: IF speed error is positive (P) AND delta speed error is zero (Z), THEN the fuzzy-PI control voltage (output of FL) is negative medium (NM). This rule pertains to the condition that $w_{ref} > w_{meas}$ and that the difference between them is steady. Thus, the control action need not change the error momentum but still bring the motor rate back down to the reference rate. Therefore, a medium positive change in control voltage is necessary.

Rule 8: IF speed error is zero (Z) AND delta speed error is positive (P), THEN the fuzzy-PI control voltage (output of FL) is positive small (PS). This rule pertains to the condition that $w_{ref} = w_{meas}$ but tending toward $w_{ref} > w_{meas}$ as the error trends more positive. Thus, the control action must act to halt the error momentum but maintain the motor rate being close to the reference rate. Therefore, a small positive change in control voltage is necessary.

Rule 9: IF speed error is positive (P) AND delta speed error is negative (N), THEN the fuzzy-PI control voltage (output of FL) is zero (ZE). This rule pertains to the condition that $w_{ref} > w_{meas}$ and that the difference between them is decreasing. Thus, the control action of nothing allows the error momentum to bring the motor rate back down to the reference rate. Therefore, no change in control voltage is necessary.

Each rule is implemented via a weighted product of the membership variables. The fuzzy centroid method generates a crisp output from the nine-dimensional fuzzy rule vector. This scaled output corresponds to the control signal, ΔUPI. Figs. 36.4 and 36.5 illustrate the initial and trained fuzzy control output ΔUPI as a function of the error and the change of error.

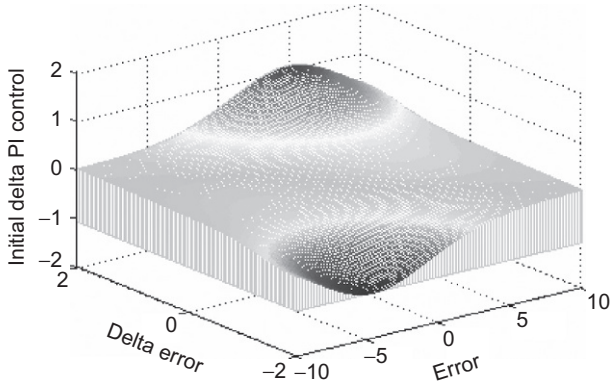


FIG. 36.4 Initial fuzzy delta PI control surface.

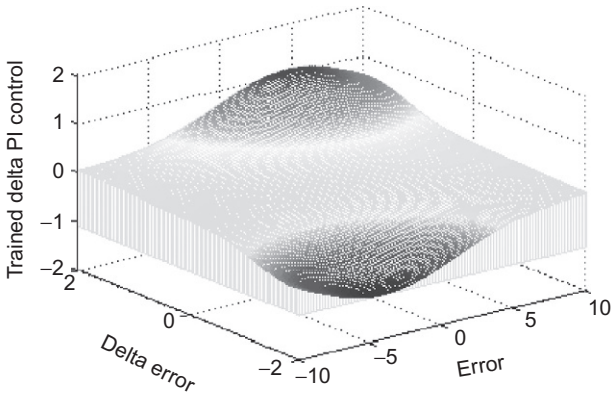


FIG. 36.5 Trained fuzzy delta PI control surface.

36.2.2 Fuzzy-Based PD Controller

The same technique applied to the fuzzy-PI controller is applied to the fuzzy-PD controller. The controller has two inputs and one output. The fuzzy-PD system implements an FL for the PD control signal. The signals e_{filt} and Δe_{filt}, the error and the delta error, respectively, are the linguistic inputs to the system. The FL output is the PD control signal *UPD*. The error signal has three fuzzy variables: positive (P), zero (Z), and negative (N). The delta error signal has three fuzzy variables: positive (P), zero (Z), and negative (N). The membership function for each fuzzy variable is a Gaussian function. Figs. 36.6 and 36.7 show the trained membership functions for the PD fuzzy inputs.

Similarly, the number of fuzzy rules that are required is equal to the product of the number of fuzzy sets that make up each of the two fuzzy input variables. Therefore, a total of nine fuzzy rules are instituted. The nine fuzzy rules are composed of the same fuzzy rules generated for the fuzzy-PI controller and are not repeated here. Each rule is implemented via a weighted product of the membership variables. The fuzzy centroid method generates a crisp output from the nine-dimensional fuzzy rule vector. This scaled output corresponds to the control

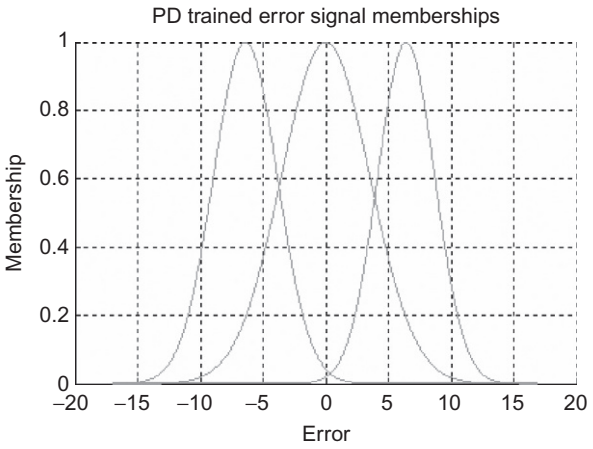


FIG. 36.6 Trained membership functions for speed error.

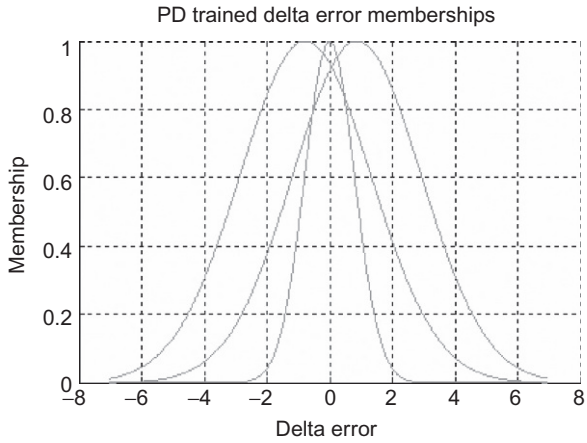


FIG. 36.7 Trained membership functions for delta speed error.

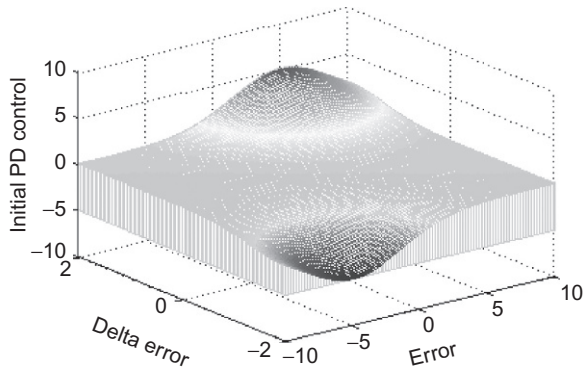


FIG. 36.8 Initial fuzzy-PD control surface.

signal, UPD. Figs. 36.8 and 36.9 demonstrate the initial and trained fuzzy control output, UPD, as a function of the error and the change of error.

Figs. 36.8 and 36.9 provide an indication of how well the EKF learning algorithm succeeds in training the output fuzzy-PD

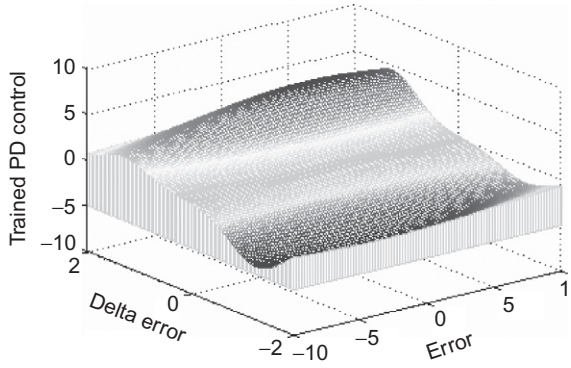


FIG. 36.9 Trained fuzzy-PD control surface.

control signal. This is an indication of how well the control process is proceeding during the experimental implementation.

36.3 FNN PI/PD-Like Fuzzy Control Architecture

The proposed FNN has four layers: an input layer, a membership layer, a rule layer, and an output layer. The input layer is a pass-through capture of each input signal. The membership layer creates a fuzzy set for each input using Gaussian membership functions. The rule layer consists of a truth table like evaluation of the fuzzy membership sets by product pairing. The output layer consists of a weighted summation of the rules. Three numbers define the size of an FNN: the number of inputs to the logic, the number of memberships per input, and the number of outputs, respectively, that is, $2 \times 3 \times 1$. The PI/PD demands two $2 \times M \times 1$ FNNs, where M, the number of memberships, is customizable. A larger number of memberships enhance accuracy of the FNN for modeling; however, a smaller number of memberships yields a smaller training calculation time period per step (there are less calculations to perform) enabling a faster system rate on real-time hardware. The membership number of 3 is selected. The parameters of the FNN are the means and sigmas of the Gaussian memberships and the weights of the output layer. For a $2 \times 3 \times 1$ FNN, there are (six means + six sigmas + nine weights) 21 parameters. Figs. 36.10 and 36.11 display the structure of FNN-based PI and FNN-based PD. Below is the definition of the function of each layer.

36.3.1 Input Layer

The input layer passes the input value, assigned for each FNN as follows (let be the feedback error).

Network\input	u_1	u_2
PI FNN	e_{filt}	Δe_{filt}
PD FNN	e_{filt}	Δe_{filt}

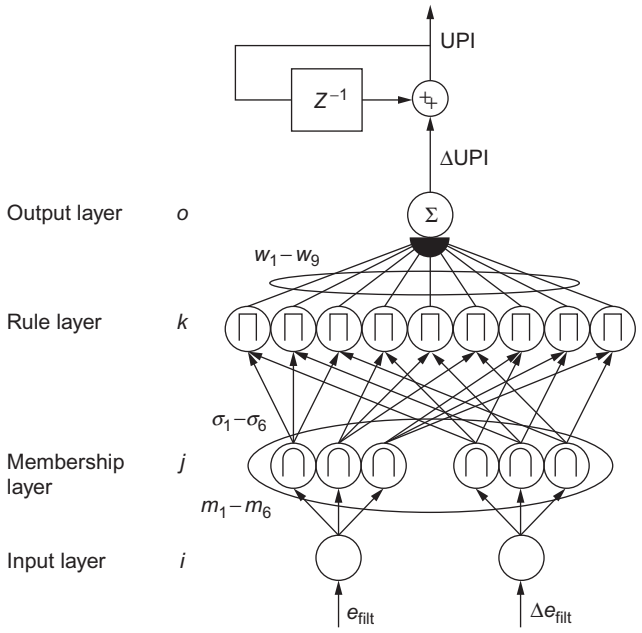


FIG. 36.10 Proposed $2 \times 3 \times 1$ FNN PI structure.

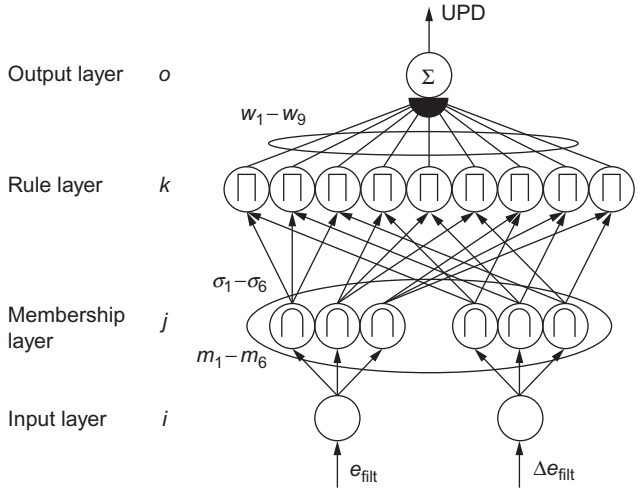


FIG. 36.11 Proposed $2 \times 3 \times 1$ FNN PD structure.

36.3.2 The Membership Layer

Each membership function into the fuzzy set is a Gaussian; the following evaluation occurs (note that m_{ij} and σ_{ij} are parameters): $y_{ij}^{\text{mem}} = \exp \dfrac{\left(u_i - m_{ij}\right)^2}{\sigma_{ij}^2}$ for input $i = 1,2$ and member $j = 1,2,3$ of that input.

For further derivations, allow the matrix y^{mem} to be vectorized as follows:

$$y_1^{\text{mem}} = y_{11}^{\text{mem}}, y_2^{\text{mem}} = y_{12}^{\text{mem}}, y_3^{\text{mem}} = y_{13}^{\text{mem}}, y_4^{\text{mem}} = y_{21}^{\text{mem}},$$
$$y_5^{\text{mem}} = y_{22}^{\text{mem}}, y_6^{\text{mem}} = y_{23}^{\text{mem}}$$

and allow the same vectorization for the means m matrix into a vector and sigmas σ matrix into a vector.

36.3.3 The Rule Layer

Each rule function is a product of two membership outputs. Refer to the table: each table cell is a rule layer output calculated by the product of the row and column label values.

Row\column	y_{21}^{mem}	y_{22}^{mem}	y_{23}^{mem}
y_{11}^{mem}	y_1^{rule}	y_4^{rule}	y_7^{rule}
y_{12}^{mem}	y_2^{rule}	y_5^{rule}	y_8^{rule}
y_{13}^{mem}	y_3^{rule}	y_6^{rule}	y_9^{rule}

36.3.4 The Output Layer

The weighted summation of the rules composes the output layer (note parameters W_k): $y = \Sigma_{k=1}^{9} y_k^{\text{rule}} W_k$ where $k = 1,9$.

36.4 Learning Algorithm-Based EKF

At each time step, for each $2 \times 3 \times 1$ FNN, there is a state vector comprised of 21 elements: $x = [W_1 \cdots W_9, m_1 \cdots m_6, \sigma_1 \cdots \sigma_6]$ (noting vector form of m, σ).

Furthermore, define the following: the reference model output ω_{ref}, measured output ω_{meas}, control signal U, PI FNN output control signal ΔUPI, and PD FNN output control signal UPD. Also, allow for the matrix notation of the membership outputs to be vectorized as follows:

The EKF innovation process is the difference from a reference signal to the measured output of the system $\widetilde{Z} = \omega_{\text{ref}} - \omega_{\text{meas}}$. A state gradient vector h must be created, such that $h_i = d(\omega_{\text{meas}})/dx_i$ using the chain rule backpropagation. The change in system output with respect to input $(\omega_{\text{meas}})/d(U)$ is assumed as unity. This is a dangerous assumption, and a more sophisticated control algorithm would attempt to model this scalar value, perhaps with an FNN identification structure.

The control signal is the summation $U = \text{UPI} + \text{UPD}$. Thus, to propagate into each FNN, the following are useful: $d(U)/d(\text{UPI}) = 1$ and $d(U)/d(\text{UPD}) = 1$ and $d(\text{UPI})/d(\Delta\text{UPI}) = 1$.

Within the FNN, the change in output layer calculation with respect to each weight is $d(y)/d(W_k) = y_k^{\text{rule}}$ for $k = [1, 9]$ and note $y = \Delta$UPI and $y =$ UPD for each FNN.

Within the FNN, to propagate to the membership layer, the vector $d(y)/d\left(y_k^{\text{rule}}\right) = W_k$ is the change in the FNN output with respect to each rule.

Each rule is a product of two fuzzy set elements from the membership layer. The following matrix defines the gradient of rules to a vector form of membership outputs.

$$\frac{d\left(y^{\text{rule}}\right)^T}{d\left(y^{\text{mem}}\right)}=\begin{bmatrix} y_4^{\text{mem}} & 0 & 0 & y_!^{\text{mem}} & 0 & 0 \\ y_5^{\text{mem}} & 0 & 0 & 0 & y_1^{\text{mem}} & 0 \\ y_6^{\text{mem}} & 0 & 0 & 0 & 0 & y_1^{\text{mem}} \\ 0 & y_4^{\text{mem}} & 0 & y_2^{\text{mem}} & 0 & 0 \\ 0 & y_5^{\text{mem}} & 0 & 0 & y_2^{\text{mem}} & 0 \\ 0 & y_6^{\text{mem}} & 0 & 0 & 0 & y_2^{\text{mem}} \\ 0 & 0 & y_4^{\text{mem}} & y_3^{\text{mem}} & 0 & 0 \\ 0 & 0 & y_5^{\text{mem}} & 0 & y_3^{\text{mem}} & 0 \\ 0 & 0 & y_6^{\text{mem}} & 0 & 0 & y_3^{\text{mem}} \end{bmatrix}$$

Each membership is Gaussian. The partial with respect to the mean and sigma are necessary:

$$d\left(y_{ij}^{\text{mem}}\right)/d\left(m_{ij}\right)=y_{ij}^{\text{mem}}2\left(u_i-m_{ij}\right)/\sigma_{ij}^2$$

and

$$d\left(y_{ij}^{\text{mem}}\right)/d\left(\sigma_{ij}\right)=y_{ij}^{\text{mem}}2\left(u_i-m_{ij}\right)^2/\sigma_{ij}^3$$

Note that the resulting matrix may be vectorized as seen previously for y^{mem}.

Applying the chain rule, the following gradients for each FNN are (where $y=\Delta\text{UPI}$ and $y=\text{UPD}$ for each respective calculation) and * represents element-wise multiplication:

$$d(\omega_{\text{meas}})/d(w)=\frac{d(\omega_{\text{meas}})}{d(U)}\frac{d(U)}{d(y)}\frac{d(y)}{d(W)}$$

$$d(\omega_{\text{meas}})/d(m)=\frac{d(\omega_{\text{meas}})}{d(U)}\frac{d(U)}{d(y)}\frac{d(y)^T}{d(y^{\text{rule}})}\frac{d\left(y^{\text{rule}}\right)^{T^T}}{d(y^{\text{mem}})}*\frac{d(y^{\text{mem}})}{d(m)}$$

$$d(\omega_{\text{meas}})/d(\sigma)=\frac{d(\omega_{\text{meas}})}{d(U)}\frac{d(U)}{d(y)}\frac{d(y)^T}{d(y^{\text{rule}})}\frac{d\left(y^{\text{rule}}\right)^{T^T}}{d(y^{\text{mem}})}*\frac{d(y^{\text{mem}})}{d(\sigma)}$$

The gradient state vector is then a concatenation:

$$h=\left[\frac{d(\omega_{\text{meas}})}{d(w)}\lambda_w,\frac{d(\omega_{\text{meas}})}{d(m)}\lambda_m,\frac{d(\omega_{\text{meas}})}{d(\sigma)}\lambda_\sigma\right]$$

where λ_w,λ_m, and λ_σ are learning rate constants for the weights, means, and sigmas.

The EKF algorithm consists of the following recursive equations built on the state vector x and gradient state vector h (both 21×1 below) and a state covariance matrix P and measurement noise scalar r and state noise vector q:

$$k=(Ph)/\left(r+h^TPh\right)$$

$$x^{\text{next}}=x+k\tilde{z}$$

$$P^{\text{next}}=P-kh^TP+q$$

36.5 Fuzzy PID Control Design-Based Genetic Optimization

A genetic-based hybrid fuzzy-PID controller, which employs a fuzzy-PID controller integrating a classical PID controller, is presented in this section. The fuzzy-PID controller consists of three parallel fuzzy subcontrollers, namely, fuzzy-based proportional controller, fuzzy-based integral controller, and fuzzy-based derivative controller. A genetic optimization technique is used to determine the optimal values of the scaling factors of the output variables of these subcontrollers. These independent controllers are grouped together and integrated with an industrial PID controller to form a hybrid fuzzy-PID controller. Fig. 36.12 shows the architecture of the proposed genetic-based hybrid fuzzy-PID controller. The hybrid fuzzy-PID controller is anticipated to accommodate the robust stabilization and disturbance rejection problems.

36.5.1 Fuzzy-Based Proportional Controller

The first step in designing the controller is to decide which state variables of the drive system can be taken as the input signals to the controller. Both the speed error, $e(k)$, and the delayed feedback control signal, $u_{\text{FP}}(k-1)$, are used as the inputs to the speed controller. The output of the fuzzy-based proportional controllers is the gain, FK_{P}. The linguistic fuzzy variable "$e(k)$" has three sets: positive large (PL), zero (ZE), and negative large (NL), with each set having its own membership function. Furthermore, the linguistic fuzzy variable "$u_{\text{FP}}(k-1)$" also has three sets: positive large (PL), zero (ZE), and negative large (NL), with each set having its own membership function. After specifying the fuzzy sets, it is required to determine the membership functions for these sets. Typical triangular membership functions are utilized for the $e(k)$ and $u_{\text{FP}}(k-1)$. The three fuzzy sets can be symbolized by

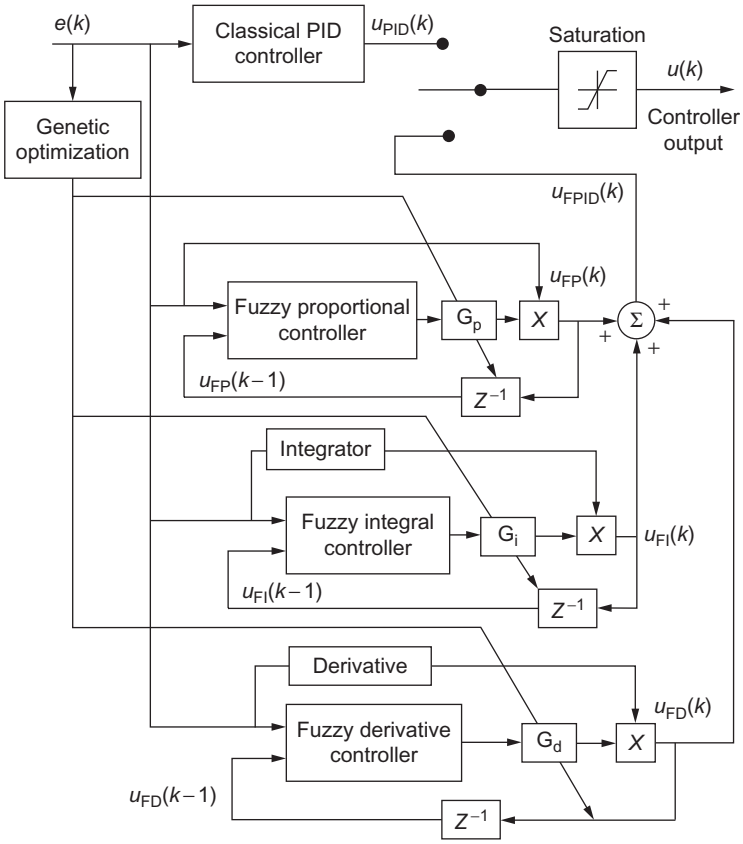


FIG. 36.12 Block diagram of the proposed hybrid fuzzy-PID controller.

$F_i^j, i = 1,2$ and $j = 1,2,3$. Their corresponding membership functions can be symbolized by $\mu F^j(e, u_{\mathrm{FP}}(k-1)), j = 1,2,3$.

The next step in the design of the fuzzy subcontroller is the determination of the fuzzy IF-THEN inference rules. The number of fuzzy rules that are required is equal to the product of the number of fuzzy sets that make up each of the two fuzzy input variables. Thus, a total of nine fuzzy rules are required to relate each possible combination of the two fuzzy input variables to the output membership fuzzy sets. The fuzzy rules ensure that the output of each fuzzy controller enhances the overall speed-tracking performance. Examples of such rules are the following:

IF $e(k)$ is positive large AND $u_{\mathrm{FP}}(k-1)$ is negative large, THEN FK_{P} is positive medium (PM).

IF $e(k)$ is zero AND $u_{\mathrm{FP}}(k-1)$ is zero, THEN FK_{P} is positive small (PS).

IF $e(k)$ is positive large AND $u_{\mathrm{FP}}(k-1)$ is zero, THEN FK_{P} is positive very large (PVL).

In general, a typical fuzzy rule is of the form:

$R^{(k)}$: IF $e(k)$ is F_1^j, and $u_{\mathrm{FP}}(k-1)$ is F_2^l, THEN f_{P} is C_{k}^l for $j = 1\ldots3, l = 1\ldots3, k = 1\ldots9$.

The conjunction of the rule antecedents is evaluated by the fuzzy operation intersection, which is implemented by the min operator. The rule strength represents the degree of membership of the output variable for a particular rule. Defining the rule strength, $\xi_{i,j}$ of a particular rule as $\xi_{i,j} = \min\left(\mu_{F_i}, \mu_{F_j}\right)$ where $i \in [PL, ZE, NL]$ is associated with the fuzzy variable, $e(k)$, and $j \in [PL, ZE, NL]$ is associated with the fuzzy variable, $u_{\mathrm{FP}}(k-1)$. The fuzzy inference engine uses the appropriately designed knowledge base to evaluate the fuzzy rules and produce an output for each rule. Subsequently, the multiple outputs are transformed to a crisp output by the defuzzification interface. Once the aggregated fuzzy set representing the fuzzy output variable has been determined, an actual crisp control decision must be made. The process of decoding the output to produce an actual value for the controller gain FK_{P} is referred to as defuzzification. Thus, a fuzzy-logic controller-based center-average defuzzifier is implemented. The output of fuzzy-based proportional controller is given by $FK_{\mathrm{P}} = f_{\mathrm{P}}(e(k), u_{\mathrm{FP}}(k-1))$, where

$$f_{\mathrm{P}}(e(k), u_{\mathrm{FP}}(k-1)) = \frac{\sum_{1=1}^{9} \mu_{\mathrm{O}^l}\left(\min_{i=1,2}\left(\mu_{\mathrm{F}_i^l}(e(k), u_{\mathrm{FP}}(k-1))\right)\right)}{\sum_{1=1}^{9}\left(\min_{i=1,2}\left(\mu_{\mathrm{F}_i^l}(e(k), u_{\mathrm{FP}}(k-1))\right)\right)}$$

The linguistic fuzzy output variable "FK_{P}" has nine sets: negative very large (NVL), negative large (NL), negative medium (NM), and negative small (NS), zero (ZE), positive small (PS), positive medium (PM), positive large (PL), and positive

very large (PVL). The two fuzzy sets, namely, negative very large (NVL) and positive very large (PVL), are added to enhance the tracking performance. After specifying the fuzzy sets, it is required to determine the membership functions for these sets μ_{O}^{l} for $l=1\ldots9$. The membership function for the fuzzy set-representing zero is a fuzzy singleton. Additionally, the other membership functions are composed of fuzzy singletons within the region defined for the fuzzy output variable. Consequently, the control signal generated by the fuzzy-proportional controller can be written as $u_{\mathrm{FP}}(k)=G_{\mathrm{P}}\{f_{\mathrm{P}}(e(k),u_{\mathrm{FP}}(k-1))\}e(k)$, where G_{P} is the scaling factor that is tuned experimentally using genetic optimization.

36.5.2 Fuzzy-Based Integral Controller

The same technique applied to the fuzzy-based proportional controller is applied to the fuzzy-based integral controller. The controller has two inputs and one output. The inputs to the fuzzy-based controller are (1) the angular speed error, $e(k)$, and (2) the delayed feedback control signal, $u_{\mathrm{FI}}(k-1)$. The controller output is the gain, FK_{I}, of the controller. Three fuzzy sets are defined for the fuzzy linguistic variable "$e(k)$" and three fuzzy sets for the fuzzy linguistic variable "$u_{\mathrm{FI}}(k-1)$." After specifying the fuzzy sets of the two fuzzy variables, the membership functions for these sets are derived. The membership functions are composed of the same fuzzy triangular membership functions allocated for the fuzzy-based proportional controller. Similarly, the number of fuzzy rules that are required is equal to the product of the number of fuzzy sets that make up each of the two fuzzy input variables. Therefore, a total of nine fuzzy rules are introduced. Some of these rules and their significance are explained as follows:

Rule 1: IF $e(k)$ is positive large (PL) AND $u_{\mathrm{FI}}(k-1)$ is positive large (PL), THEN FK_{I} is positive large (PL). This rule implies a general condition when both input signals are positive. Consequently, the output membership function assigned to this rule is a positive value to keep the controller gain within a stable range.

Rule 2: IF $e(k)$ is zero (ZE) AND $u_{\mathrm{FI}}(k-1)$ is positive large (PL), THEN FK_{I} is positive very small (PVS). This rule implies a general condition when the speed error is close to zero and $u_{\mathrm{FI}}(k-1)$ is positive. Therefore, the output membership function assigned to this rule is a small positive value to reduce the control signal variations.

Rule 3: IF $e(k)$ is negative large (NL) AND $u_{\mathrm{FI}}(k-1)$ is positive large (PL), THEN FK_{I} is positive medium (PM). This rule usually deals with the case in which overshoots occur. A medium positive value is assigned in this case to ensure that the overshoot is decreased and prevent oscillations at the same time.

The rule strength represents the degree of membership of the output variable for a particular rule. Similarly, the rule strength, $\xi_{n,m}$ of a particular rule is defined as

$$\xi_{n,m}=\min\left(\mu_{F_n},\mu_{F_m}\right)$$

where $n\in[PL,ZE,NL]$ is associated with the fuzzy variable, $e(k)$, and $m\in[PL,ZE,NL]$ is associated with the fuzzy variable, $u_{\mathrm{FI}}(k-1)$.

The fuzzy inference engine uses the appropriately designed knowledge base to evaluate the fuzzy rules and produce an output for each rule. Subsequently, the multiple outputs are transformed to a crisp output, by the defuzzification interface. A center-average defuzzifier method is used. Thus, the output of fuzzy-based integral controller is given by $FK_{\mathrm{I}}=f_{\mathrm{I}}(e(k),u_{\mathrm{FI}}(k-1)$ where

$$f_{\mathrm{I}}(e(k),u_{\mathrm{FI}}(k-1))=\frac{\sum_{1=1}^{9}\mu_{\mathrm{O}^l}\left(\min_{i=1,2}\left(\mu_{\mathrm{F}_i^l}(e(k),u_{\mathrm{FI}}(k-1))\right)\right)}{\sum_{\mathrm{l}=1}^{9}\left(\min_{i=1,2}\left(\mu_{\mathrm{F}_i^l}(e(k),u_{\mathrm{FI}}(k-1))\right)\right)}$$

After specifying the fuzzy sets for the fuzzy output variable, FK_{I}, the membership functions for these sets are derived. It is important to note that the same fuzzy singleton membership functions are used here. The control signal of the fuzzy-based integral controller is given by

$$u_{\mathrm{FI}}(k)=G_{\mathrm{I}}\{f_{\mathrm{I}}(e,u_{\mathrm{FI}}(k-1))\}\sum_{i=0}^{k}e(i)\Delta t,k=0,1,2,\ldots,$$

where G_{I} is the scaling factor that is tuned experimentally using genetic optimization.

36.5.3 Fuzzy-Based Derivative Controller

The same process applied to fuzzy-based proportional controller and fuzzy-based integral controller is applied to the fuzzy-based derivative controller. The input signals (state variables) to the controller are $e(k)$ and $u_{\mathrm{FD}}(k-1)$. The output of the controller is the gain FK_{D}. After specifying the fuzzy sets and the membership functions for these sets, the triangle membership functions are also used to define the degree of membership. Figs. 36.2 and 36.3 show the membership functions for the fuzzy sets. Similarly, the linguistic fuzzy output variable "FK_{D}" has nine sets: negative very large (NVL), negative large (NL), negative medium (NM), and negative small (NS), zero (ZE), positive small (PS), positive medium (PM), positive large (PL), and positive very large (PVL). Now, it is necessary to find the final controller output. Consequently, the output of fuzzy-based derivative controller is given by $FK_{\mathrm{D}}=f_{\mathrm{D}}(e(k),u_{\mathrm{FD}}(k-1))$, where

$$f_{\mathrm{D}}(e(k),u_{\mathrm{FD}}(k-1))=\frac{\sum_{1=1}^{9}\mu_{\mathrm{O}^l}\left(\min_{i=1,2}\left(\mu_{\mathrm{F}_i^l}(e(k),u_{\mathrm{FD}}(k-1))\right)\right)}{\sum_{\mathrm{l}=1}^{9}\left(\min_{i=1,2}\left(\mu_{\mathrm{F}_i^l}(e(k),u_{\mathrm{FD}}(k-1))\right)\right)}$$

The control signal of the fuzzy-based derivative controller:

$$u_{\mathrm{FD}}(k) = G_{\mathrm{D}} f_{\mathrm{D}}(e(k), u_{\mathrm{FD}}(k-1))\Delta e(k)/\Delta t$$

where G_{D} is a scaling factor that tuned experimentally using genetic optimization.

Finally, the overall output of fuzzy PID was derived as follows:

$$u_{\mathrm{FPID}}(k) = u_{\mathrm{FP}}(k) + u_{\mathrm{FI}}(k) + u_{\mathrm{FD}}(k)$$

Saturation is also incorporated in the hybrid fuzzy-PID controller structure. As such, the final output of proposed controller is

$$\begin{aligned} &u_{\max}(k), u_{\mathrm{FPID}}(k) > u_{\max}(k), \\ &u(k) = u_{\mathrm{FPID}}(k) u_{\min}(k) \le u_{\mathrm{FPID}}(k) \le u_{\max}(k) \\ &u_{\min}(k) u_{\mathrm{FPID}}(k) < u_{\min}(k) \quad (10) \end{aligned}$$

where $u_{\min}$ and $u_{\max}$ are the permitted minimum and maximum inputs to the brushless drive system.

36.6 Classical PID Versus Fuzzy-PID Controller

The classical linear PID controller in its discrete form can be characterized as

$$u_{\mathrm{PID}} = K_{\mathrm{P}} e(k) + K_{\mathrm{I}} \sum_{\mathrm{i}=0}^{k} e(i)\Delta t + K_{\mathrm{D}} \Delta e(k)/\Delta t \quad k = 0, 1, \ldots,$$

where $K_{\mathrm{P}}, K_{\mathrm{I}}$, and K_{D} are constant gains.

This discrete form characterization equation provides a closed-form solution to the proposed fuzzy-PID controller. It can be rewritten as

$$\begin{aligned} u_{\mathrm{FPID}}(k) &= f_{\mathrm{P}}(e, Du_{\mathrm{P}}) G_{\mathrm{P}} e(k) + f_{\mathrm{I}}(e, Du_{\mathrm{I}}) G_{\mathrm{I}} \sum_{i=0}^{k} e(i)\Delta t \\ &\quad + f_{\mathrm{D}}(e, Du_{\mathrm{D}}) G_{\mathrm{D}} \Delta e(k)/\Delta t k = 0, 1, 2, \ldots \\ &= (FK_{\mathrm{P}})_{\mathrm{eq}} e(k) + (FK_{\mathrm{I}})_{\mathrm{eq}} \sum_{i=0}^{k} e(i)\Delta t \\ &\quad + (FK_{\mathrm{D}})_{\mathrm{eq}} \Delta e(k)/\Delta t \quad k = 0, 1, 2, \ldots, \end{aligned}$$

where $(FK_{\mathrm{P}})_{\mathrm{eq}}, (FK_{\mathrm{I}})_{\mathrm{eq}}$, and $(FK_{\mathrm{D}})_{\mathrm{eq}}$ are defined to be the equivalent proportional, integral, and derivative gains to a classical linear PID controller, respectively.

36.7 Genetic-Based Autotuning of Fuzzy-PID Controller

Genetic optimization-based approach is used to ensure the best performance of the proposed fuzzy-PID controller. The genetic optimization imitates the natural evolution process in which the fittest survive and the best genes are propagated to the next generation. A population of chromosomes is evaluated and a fitness value is assigned to each. Each chromosome represents a possible solution for a given problem, and the ones with the higher fitness have a better chance to reproduce. One of the main features is that it could work well for nondeterministic systems, ill-defined systems, and systems that are hard to model. Furthermore, the final performance outcome of the algorithm does not depend highly on the initial choice of chromosomes. When the genetic optimization is applied to control applications, each chromosome represents the set of controller's adjustable parameters, and the fitness value is a quantitative measure of the controller performance. The autotuning consists of the automatic adjustment of these parameters to optimize the controller performance. The genetic optimization combines a stochastic exploratory search with a well-defined cost function to find the solution that fit the problem the best. The cost function that represents the fuzzy-PID controller is defined as follows:

$$J = F(G_{\mathrm{P}}, G_{\mathrm{I}}, G_{\mathrm{D}}),$$

where $G_{\mathrm{P}}, G_{\mathrm{I}}, G_{\mathrm{D}}$ are the output scaling factors of the fuzzy-PID subcontrollers. The function F represents the relationship between the overall performance and the design parameters.

The optimization problem for the fuzzy-PID controller is described as

$$\max(F(G_{\mathrm{P}}, G_{\mathrm{I}}, G_{\mathrm{D}})) = \max(1/J)$$

where F is the fitness function. There are various ways to calculate the overall performance J of the controller, but for simplicity reasons, the mean square error (MSE) performance index was selected.

$$J = \frac{1}{N} \sum_{k=1}^{N} (e(k))^2$$

where N is the length of the evaluation window and $e(k)$ is the error between the reference speed and the actual speed. The fitness of each parameter set or chromosome can be determined as follows:

$$F(G_{\mathrm{P}}, G_{\mathrm{I}}, G_{\mathrm{D}}) = 1 \Big/ \left(\frac{1}{N} \sum_{k=1}^{N} (e(k))^2 \right)$$

Once the fitness function is established, the genetic operators and parameters are defined. The genetic optimization consists

of three basic operators: the crossover, mutation, and reproduction. The parameters are the number of generations, the population size, the probability of crossover, and mutation. In general, an initial population size is defined and evaluated with the fitness function. Once each chromosome has a fitness assigned to it, the reproduction process takes place with those that are more fit having a greater chance to be selected. Then, each of the two operators of crossover and mutation is applied to create the new pool of chromosomes to be evaluated. Crossover occurs when the chromosomes partially exchange their information by interchanging some of their genes. Mutation is the random alteration of a particular section of the chromosome by occasionally changing one or more of the genes that are part of the chromosome. For this optimization task, a crossover factor of 0.3 and a mutation factor of 0.7 were used. Another important aspect of the genetic optimization is the coding of the parameters. Binary coding has been used widely for decades; however, real-coded algorithms are proving useful for a number of applications, and it was chosen to implement the genetic optimization algorithm. One of the difficulties of the real-time implementation is in the simultaneous evaluation of the fitness for all the chromosomes in one generation as a batch data. This problem was overcome by reducing the population size to one and evaluating the fitness function of each chromosome sequentially. The mutation function is applied by increasing or decreasing the value proportional to a uniformly distributed random number between −0.9 and 1. The crossover is implemented with the chromosome that had the higher value for the fitness function and the chromosome being tested in the current generation. A Bernoulli binary set of numbers with probability of 0.5 is used to select the resulting offspring chromosome with a mix of genes from both parent chromosomes. The overall genetic-based autotuning procedure of the fuzzy-PID controller consists of the following steps:

Step 1: Select the control topology of the fuzzy-PID controller in which the outputs of the subcontrollers are used as the FPID gains.

Step 2: Define the characteristics of the fuzzy-PID subcontrollers such as the number of fuzzy sets, membership functions, fuzzy rules, and defuzzification method.

Step 3: Set the genetic optimization parameters, such as the number of generations, the population size, the probability of crossover, and mutation.

Step 4: The last step is the tuning of the parameters, G_P, G_I, and G_D of the fuzzy-PID controller using the genetic optimization procedure.

36.8 Fuzzy and *H*∞ Control Design

36.8.1 Brushless Servo-Motor Drive System

The brushless DC motor used in the section is excited by a three-phase sinusoidal supply and driven from a six-step inverter, which converts a constant voltage to a three-phase voltage with a frequency corresponding instantaneously to the rotor speed. The model of the drive system is used to design the $H\infty$ tracking controller and to simulate its dynamic behavior. However, fuzzy-logic controller does not require mathematical models and has the ability to approximate nonlinear systems. The reader is referred to [16] for details of the dynamic model of the brushless dc motor drive system. For the purpose of discussion, the dynamics of the brushless servomotor drive system can be written in state space form as follows:

$$x^{(n)} = f(x) + Bu + d$$

where $x = \left(x, \dot{x}, \ldots, x^{(n-1)}\right)^T \in R^n$, d is the external disturbance, and $B \neq 0$. Since $B \neq 0$ for $x \in R^n$, the system is controllable in the whole space R^n.

36.8.2 The Fuzzy *H*∞ Control Structure

A hybrid adaptive fuzzy controller is implemented, which employs a fuzzy-logic controller integrating an $H\infty$ tracking controller. The $H\infty$ tracking controller is capable of taking care of the robust stabilization and disturbance rejection problems, while fuzzy-logic controller is used as principle components of the adaptive fuzzy controller. Actually, it is outfitted with an adaptive control law that modifies the parameters of the controller based on a Lyapunov synthesis approach. Fig. 36.13 shows the block diagram of the proposed control structure.

36.8.3 *H*∞ Control Design

The controller objective is to obtain high-performance servo tracking; therefore, the control problem is to force the actual output to follow a predetermined bounded reference trajectory. The tracking performance indicates how closely the servomotor follows a desired position trajectory, velocity trajectory, or acceleration trajectory. For the purpose of discussion, we define the tracking error to be $\overline{\varepsilon} = [\varepsilon, \dot{\varepsilon}]^T$, where ε is the rotor speed error and $\dot{\varepsilon}$ is the acceleration error. Consequently, the motor speed error $\varepsilon = \omega_{ref} - \omega_{act}$ and the acceleration error $\dot{\varepsilon} = \alpha_{ref} - \alpha_{act}$ are used as input variables to the $H\infty$ controller. Here, ω_{act} is the actual speed in rev/s, ω_{ref} is the desired reference speed, α_{ref} is the desired acceleration in rev/s^2, and α_{act} is the calculated acceleration. The acceleration is calculated as the difference in the speed over two successive sampling periods. A block diagram of the $H\infty$ tracking controller is shown in Fig. 36.14. The $H\infty$ control law is defined as [17]

$$u_\infty = -\frac{1}{r_r} B^T P \varepsilon$$

where r_r is a weighting factor and P is the solution of the simplified Riccati-like equation for $P = P^T \geq 0$

$$PA + A^T P = -Q$$

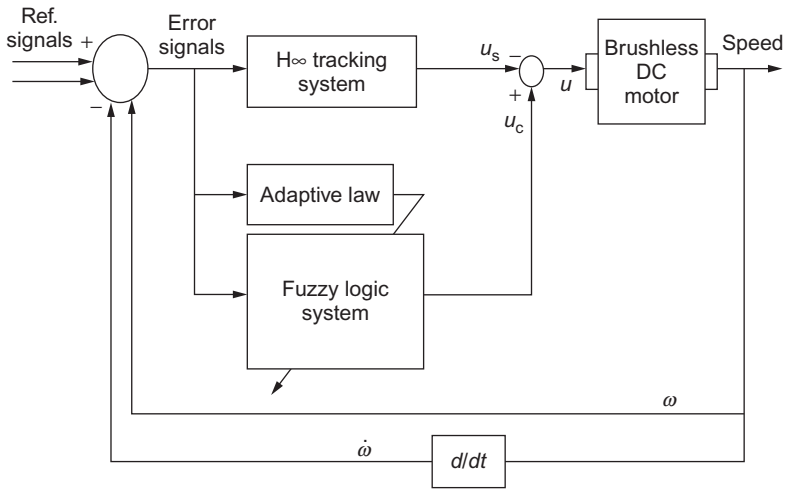


FIG. 36.13 Block diagram of the overall control structure.

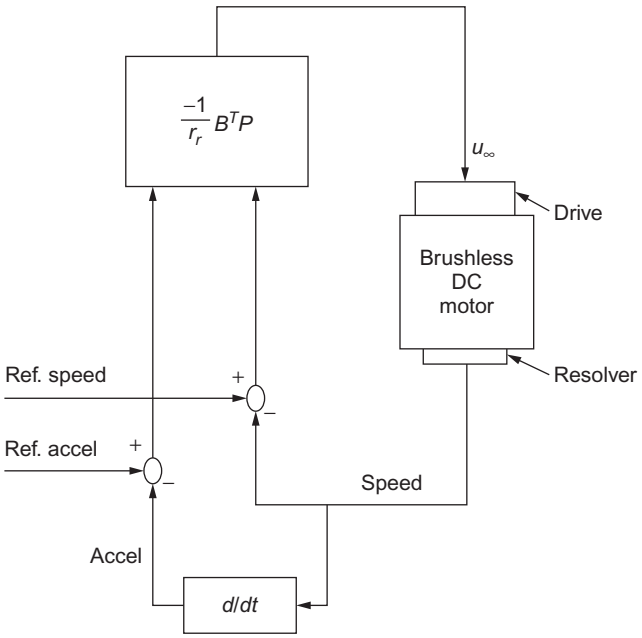


FIG. 36.14 Block diagram of $H\infty$ tracking controller.

The matrices A and B are given by

$$A = \begin{bmatrix} 0 & 1 \\ -k_2 & -k_1 \end{bmatrix} \quad B = \begin{bmatrix} 0 \\ 1 \end{bmatrix}$$

where $k = [k_1, k_2]$ is chosen such that all roots of the polynomial $p^{(S)} = S^n + K_n S^{n-1} + \cdots + k_1$ are in the open left-hand plane.

36.8.4 Fuzzy Logic Control Design

The fuzzy-logic principles with center-average defuzzifier, product inference, and singleton fuzzifier are used as building blocks for the fuzzy controller. A block diagram of the fuzzy control structure is shown in Fig. 36.15. The fuzzy-logic-based controller implemented in this work has two inputs and one output. The inputs are the rotor speed error and the feedback acceleration error, with each of these inputs corresponding to a fuzzy variable.

The output is the fuzzy control decision. The fuzzy variable associated with the rotor speed error signal consists of five fuzzy sets: positive large (PL), positive medium (PM), zero (ZE), negative large (NL), and negative medium (NM). Typical example of the fuzzy membership functions used for the speed is shown in Fig. 36.16. In this way, for any given value of the rotor angle, the degree of membership μ, to which it belongs to each of these sets, can be determined, and a control decision based on this information can be obtained.

Similarly, the acceleration error can be described by a group of partially overlapping fuzzy sets as positive large (PL), positive medium (PM), zero (ZE), negative large (NL), and negative medium (NM), with each set having its own membership function. An example of typical membership functions that make up the fuzzy variable acceleration is shown in Fig. 36.17.

The five fuzzy sets can be symbolized by $F_1^j, i = 1,2$ and $j = 1,2,3\ldots5$. Their membership functions can be symbolized by $\mu F_1^j(x_1), i = 1,2$ and $j = 1,2,3\ldots5$.

36.8.5 Fuzzy Logic Rules

The next step in the design of the fuzzy-logic-based controller is the determination of the fuzzy IF-THEN inference rules. The number of fuzzy rules that are required is equal to the product of the number of fuzzy sets that make up each of the two fuzzy input variables. For the fuzzy controller described here, the input variables representing the rotor speed and its acceleration consist of five fuzzy sets each. Thus, a total of 25 fuzzy rules are required. During each sampling interval that a controller is

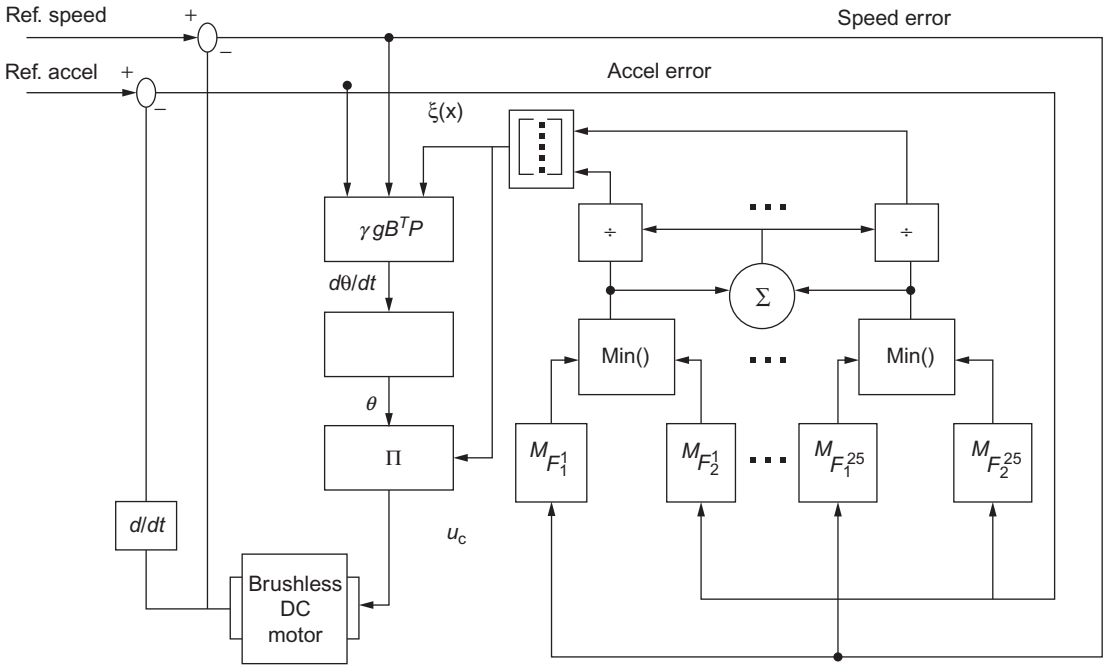


FIG. 36.15 Block diagram of the fuzzy-logic control structure.

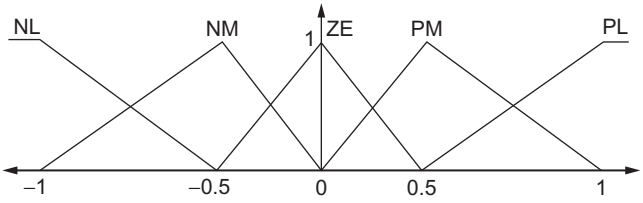


FIG. 36.16 Fuzzy membership functions for the rotor speed error.

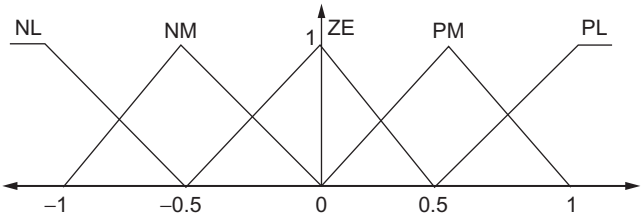


FIG. 36.17 Fuzzy membership functions representing the acceleration error.

calculated, the present value of the degree of membership of the motor speed and its acceleration is calculated for each of the fuzzy sets that make up their respective fuzzy variables. This process is one of the largest computational burdens of the fuzzy-logic control algorithm if each fuzzy set is expected to have some degree of membership for the present input value of the motor speed and its acceleration. This will in addition affect the computational speed at which the fuzzy rules are processed since all the rules have to be evaluated.

Using a triangular membership function for the input variables was very desirable to reduce this computational burden and speed up the process. This ensures that only two fuzzy sets, which are overlapping, will actually have a nonzero degree of membership (Figs. 36.16 and 36.17). With this advantage, the evaluation of the degree of membership in each set is accelerated. This also speeds up the evaluation of the fuzzy rules since only those rules that correspond to nonzero values of membership function need to be evaluated. Hence, for this controller, only four fuzzy rules need to be evaluated during any sampling interval. The fuzzy inference rules have been determined experimentally using the measured responses of the brushless drive servo system. A typical fuzzy rule is of the form:

$[R^{(1)}:]$ IF x_1 is F_1^j, and x_2 is F_2^j, THEN O is G_1^l for $j = 1\ldots5, l = 1\ldots5$.

In general,

$[R^{(k)}:]$ IF x_1 is F_1^j, and x_2 is F_2^j, THEN O is G_k^l for $j = 1\ldots5, l = 1\ldots5, k = 1\ldots25$.

The conjunction of the rule antecedents is evaluated by the fuzzy operation *intersection,* which is implemented by the *min* operator. The rule strength represents the degree of membership of the output variable for a particular rule. Defining the rule strength, $\xi_{i,j}$, of a particular rule as

$$\xi_{i,j} = \min\left(\mu_{F_i^{\text{speed}}}, \mu_{F_j^{\text{accel}}}\right)$$

where $i \in [PL, PM, ZE, NM, NL]$ is associated with the fuzzy variable, *speed*, and $j \in [PL, PM, ZE, NM, NL]$ is associated with

the fuzzy variable, *acceleration*. From above, it is clear that for all the rules where at least one of the degrees of membership in the corresponding fuzzy sets is zero, the output of the *min* operator will be zero, and hence, these rules do not have to be analyzed. The fuzzy inference engine uses the appropriately designed knowledge base to evaluate the fuzzy rules and produce an output for each rule. Subsequently, the multiple outputs are transformed to a crisp output by the defuzzification interface.

36.8.6 Defuzzification

Once the aggregated fuzzy set representing the fuzzy output variable has been determined, an actual crisp control decision must be made. The process of decoding the output to produce an actual value for the control signal is referred to as defuzzification. Thus, a fuzzy-logic controller-based center-average defuzzifier is implemented. The control output can be written in general form:

$$O(x) = \sum_{l=1}^{25} \mu_{O^l} \left(\min_{i=1,2} \left(\mu_{F_i^l}(x) \right) \right) / \sum_{l=1}^{25} \left(\min_{i=1,2} \left(\mu_{F_i^l}(x) \right) \right)$$

which can be written in the form

$$O(x) = \theta^T \xi(x) = \xi^T(x)\theta$$

where

$$\xi^l(x) = \min_{i=1,2} \left(\mu_{F_i^l}(x) \right) / \sum_{l=1}^{25} \left(\min_{i=1,2} \left(\mu_{F_i^l}(x) \right) \right)$$

$\theta = (\mu_{O^1}, \ldots \mu_{O^{25}},)$ is a parameter vector representing the degree of membership of the output, which is tuned online using an adaptation law.

36.8.7 On-Line Adaptation

By using an adaptive law, the fuzzy parameters, θ, can be tuned online based on the Lyapunov synthesis approach. The feedback control law can be expressed as follows [17]:

$$u = \xi^T(x)\theta - u_\infty / g$$

where θ is a vector denoting the parameter estimate of fuzzy-logic controller. The parameter θ is adjusted using the following adaptive law:

$$\dot{\theta} = \gamma \xi(x) g B^T P \varepsilon$$

where γ is an adaptation gain and g is a constant that depends on machine parameters. A block diagram of the hybrid adaptive fuzzy controller is shown in Fig. 36.18.

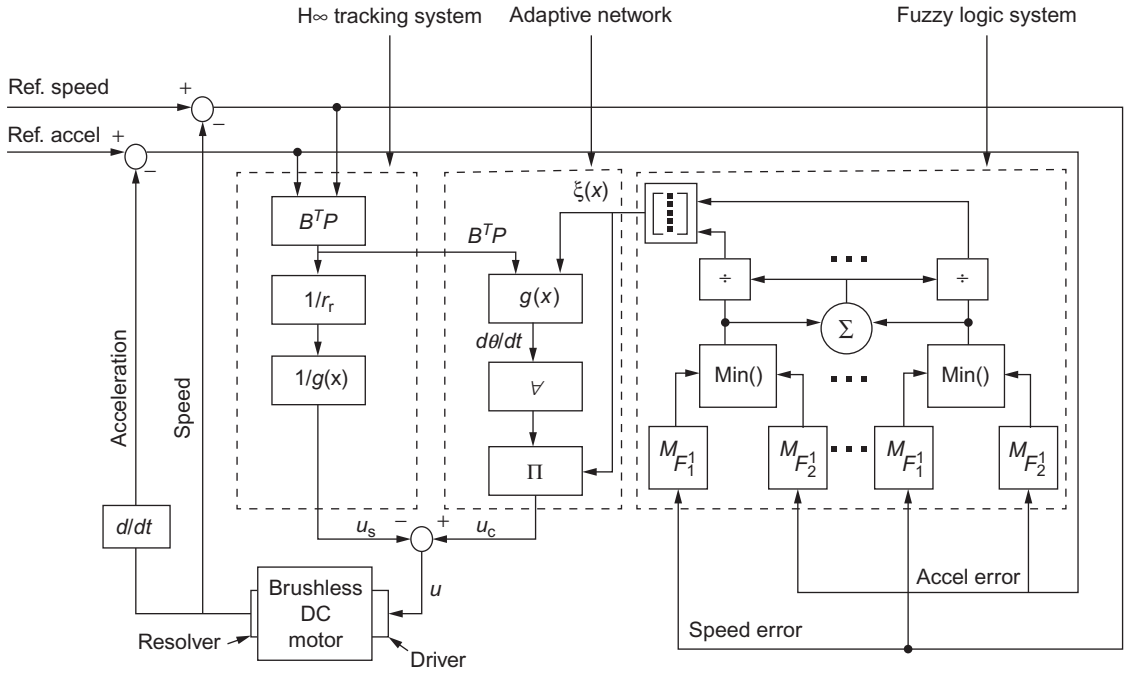


FIG. 36.18 Block diagram of the overall fuzzy- $H\infty$ control structure.

36.9 Fuzzy Control for DC-DC Converters

36.9.1 Background

The DC-DC converters are generally divided into two groups: hard-switching converters and soft-switching converters. In hard-switching converters, the power switches cut off the load current within the turn-on and turn-off times under the hard-switching conditions. The output voltage is controlled by adjusting the on-time of the power switch, which in turn adjusts the width of a voltage pulse at the output. This is known as PWM control. In soft-switching converters, resonant components are used to create oscillatory voltage or current waveforms so that the zero-voltage switching or zero-current switching conditions could be created for the power switches. For many years, control design for converters has been carried out through analog circuits, which limited them to mostly PI controller structure. The PI controllers generally give overshoot in output voltage and high initial current when rise time of response is reduced. Feed-forward types of controllers have also been designed by sensing the input voltage to improve line regulation in applications with a wide range of input voltages and load currents. However, direct sensing of the input voltage through a feed-forward loop may induce large-signal disturbances that could upset the normal duty cycle of the converter. Using human linguistic terms and common sense, several fuzzy-logic controllers have been developed and implemented for the DC-DC converters [18–20]. These controllers have shown promise in dealing with nonlinear systems and achieving voltage regulation in buck converters. Fuzzy-logic control uses humanlike linguistic terms in the form of IF-THEN rules to capture the nonlinear system dynamics. Once in place, the fuzzy rules will not be able to adapt themselves to adequately capture the dynamics and external disturbances of the converter. Although achieving many practical successes, fuzzy control has not been viewed as a rigorous science due to a lack of formal analysis and synthesis techniques. As a result of this, a lot of work has been done to develop adaptive fuzzy controllers and automate the modeling process as much as possible. Recently, the resurgence of interest in ANN has injected a new driving force into fuzzy literature. One of the major features of ANNs is their learning capability. A learning algorithm is usually used to update the nonlinear parameters of the network architecture. A drawback in using an ANN for control is that there is so much freedom in structural implementation choice that it is often difficult to decide how complex a structure is actually necessary for the desired control. Besides, the implementation is not at all intuitive, and the inner workings of the network are very much invisible to the designer. The integration of neural network architectures with fuzzy inference system has resulted in a very powerful strategy known as adaptive network-based fuzzy inference system. Some researchers suggest that neural networks and fuzzy control are in fact special instances of adaptive networks [21,22]. The suggested fuzzy inference system has the advantage that it can not only take linguistic information from human experts but also adapt itself using numerical data to achieve better performance.

36.10 Fuzzy Control Design for Switch-Mode Power Converters

The structure built-up here is a two-input single-output controller. The inputs are the variable voltage error, $e(k)$, and the change in voltage error, $\Delta e(k)$. Consequently, the input to the DC-DC converter would be the duty cycle that is actually the output of the fuzzy controller. The operational structure of the proposed fuzzy controller is shown in Fig. 36.19. It consists of three building blocks: (1) a fuzzification block that expresses quantitative action to qualitative action, (2) fuzzy inference engine that generates the fuzzy rules, and (3) a defuzzification block that articulates qualitative action to quantitative action. Fuzzification translates a numeric value for the error $e(k)$ or change in error $\Delta e(k)$ into a linguistic value such as big or small with a membership grade. Defuzzification takes the fuzzy output of the rules and generates a "crisp" numeric value used as the control input to the DC-DC converter. The controller qualitatively captures the dynamics of the DC-DC converter and executes this qualitative idea in a real-time situation. The DC-DC converter is equipped with a feedback network that provides the error value at the output. The overall architecture of a DC-DC converter topology with the fuzzy controller structure is given in Fig. 36.20. The feedback network consists of a *precision voltage reference* with a nominal voltage of 2.5 V. The 5 and 15 V output potentials are combined in a resistive sampling network in such a way that the output voltage of the network is 2.5 V when the potentials are closed to their nominal magnitudes. This output voltage is then compared internally with the reference of the *precision voltage reference*, and any error difference detected is amplified and fed back. The converter is represented by a "black box" from which we only extract the terminals corresponding to input voltage (V_I), output voltage (V_o), and controlled switch (S). From these measurements, the controller provides a percentage duty-cycle

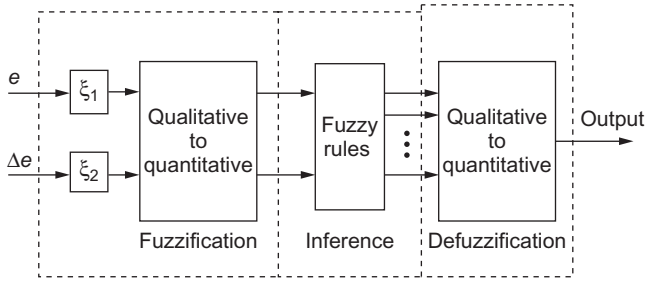


FIG. 36.19 Fuzzy control structure.

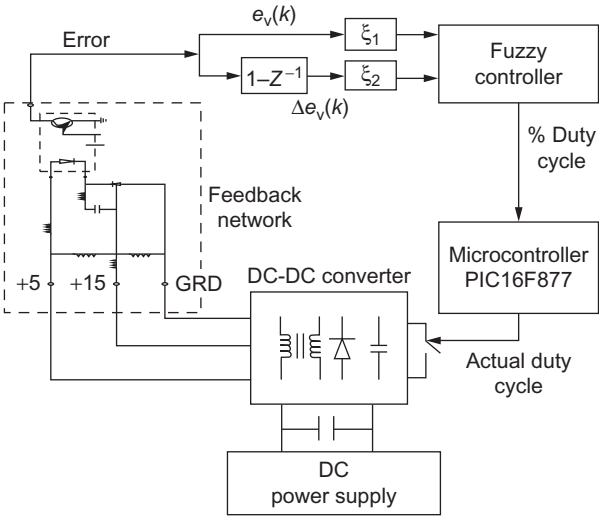


FIG. 36.20 Fuzzy control-based DC-DC converter topology.

signal for a peripheral interface microcontroller PIC16F877, which generates the converters' actual duty cycle.

36.10.1 DC-DC Switch-Mode Power Converter

The DC-DC switch-mode power converter consists of six distinct circuit networks as shown in Fig. 36.21, working together to form a complete DC-to-DC dual-output switch-mode power regulator [23]. The six distinct circuit networks are (1) the bias voltage regulator network, (2) the 100 KHZ clock, (3) the pulse-width modulator (PWM), (4) the power switch driver interface, (5) the feedback error amplifier, and (6) the integrated-magnetic (IM) power stage. In order to implement the proposed adaptive fuzzy-neural-network controller, the converter system shown in Fig. 36.21 was modified by removing the *bias voltage regulator network*, the *100 KHz clock*, and the *pulse-width modulator (PWM)*, which is the core of the control system. The power-stage concept is based on that of a "dual-output forward" configuration operating in a continuous mode of energy storage. When the power MOSFET switch Q1 is turned ON, energy is transferred from the input power source (V_{IN}) to the two secondary sides of the transformer. The voltage potential across the terminals of C1 will be that of the reflected line voltage, namely, $N_{S1} \times V_{IN}/N_P$. The ON time is a fraction of the clock period, and it has to be short and long enough to bring the output to a level above the desired voltage (5 and 15 V). Diodes D1 and D4 conduct allowing the energy transfer to be used to supply 5 and 15 V load power, respectively, and to replenish the energy lost in the "output" inductors during the previous OFF period of Q1. Diodes D2 and D3 do not conduct during this time, since they are reverse-biased.

When Q1 turns OFF, the 5 and 15 V load power is sustained by the energies of the two "inductors" (L1 and L2). The output stored energy, located in two inductors, will then start discharging causing the voltages to drop. Diodes D2 and D3 conduct

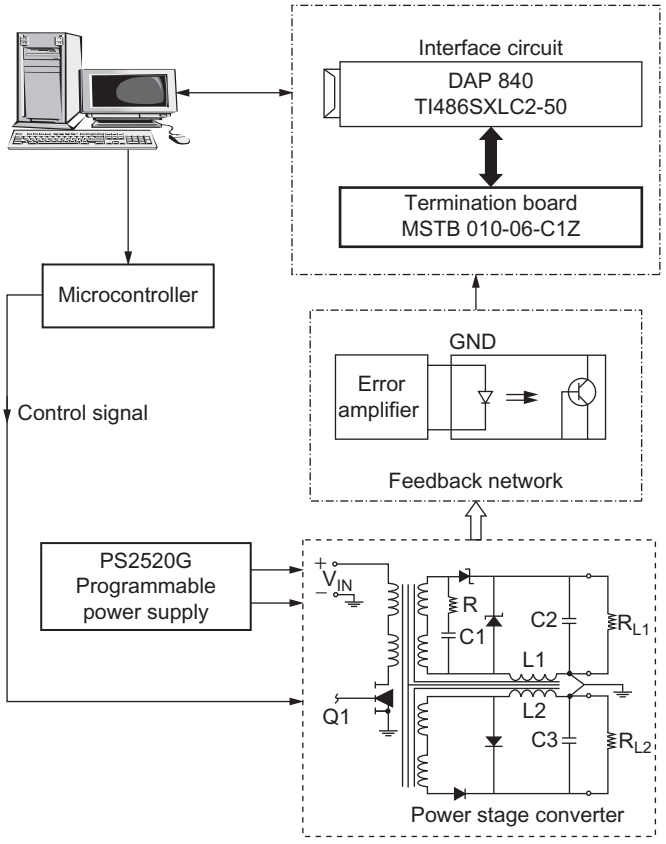


FIG. 36.21 Block diagram of switch-mode DC-DC power converter.

during this time with diodes D1 and D4 forced off. As soon as the voltages go below the desired values, another impulse will be applied on Q1 (Q1 ON), to bring the voltage back upward. Capacitors C2 (0.001 μf) and C3 (100 μf) serve to prevent the dynamic ripple currents in the "inductors" from appearing at the 5 and 15 V load terminals, respectively.

36.11 Optimum Topology of the Fuzzy Controller

The main problem with fuzzy controller generation is related to the definition of its optimum topology such as scaling factors, number of fuzzy sets, shape of the fuzzy sets, and decision-making. This section is devoted to the topology determination of the proposed fuzzy controller structure. Various test cases were performed on the DC-DC converter in order to determine the ranges of membership functions and other system-specific responses of the converter that will help in the design of the linguistic control rules of the proposed controller. The experimental tests were focused on the responses of the DC-DC converter with and without the action of the controller. One other point was to observe how the changes of the control signal and the variations of the error signal with respect to the variations of

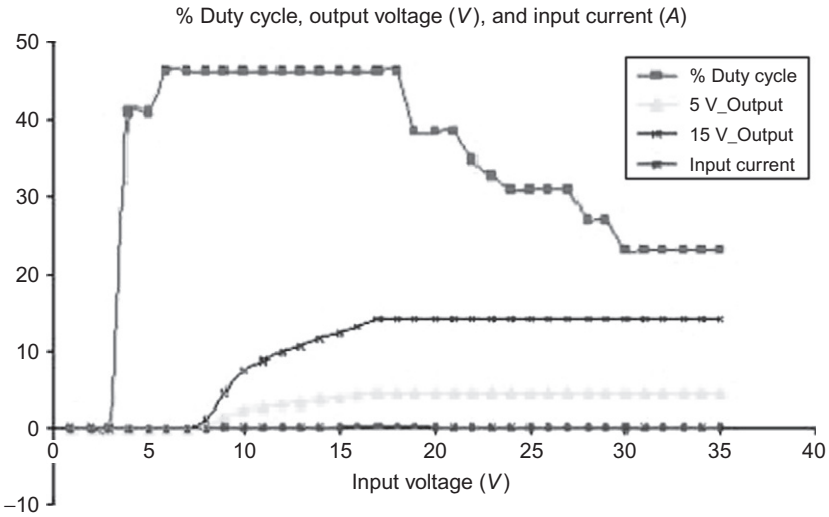


FIG. 36.22 Optimum trajectories of the percentage duty cycle, the output voltage, and the input current with variations in the input voltage.

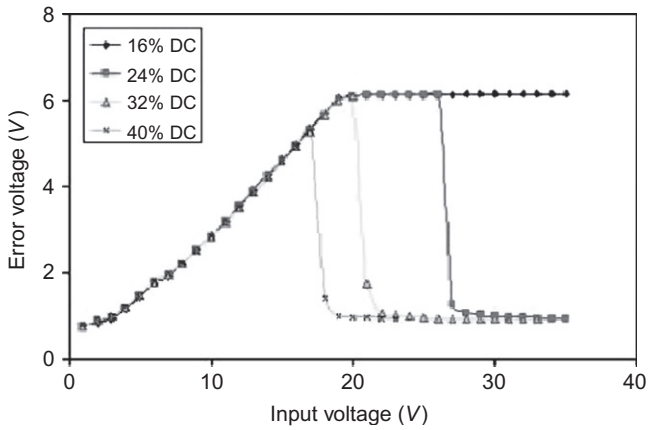


FIG. 36.23 Variations of the error voltage with the control signal at 16%, 24%, 32%, and 40% duty cycle.

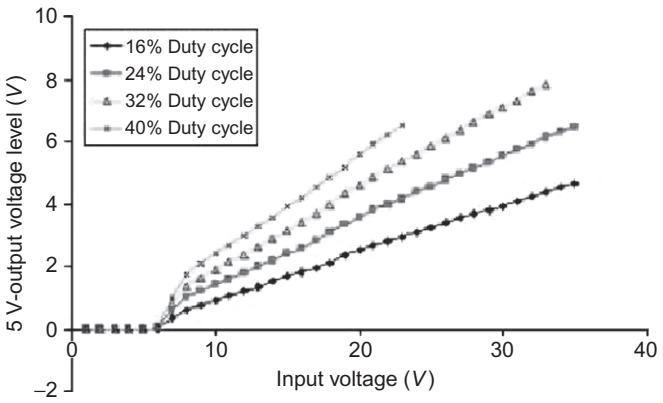


FIG. 36.24 5 V output voltage level tested for different constant control signals.

the input voltage. The various voltage ranges observed in the test cases assisted in choosing the ranges for the input and output membership set. A summary of some of these tests is shown in Figs. 36.22–36.24. Fig. 36.22 shows the optimum trajectories of the duty cycle, the output voltage, and the input current with variations in the input voltage. From Fig. 36.22, when the input voltage increases, the control signal pulses get reduced to maintain the output voltages at their required level. The other information gives the range of the control signal (i.e., 16%–50%) required for the working range of the DC-DC converter. A similar test case was conducted while the error of the system was observed. Fig. 36.23 shows four different test cases of variations of the error voltage and duty cycle with increase in the input voltage plotted together. The figure shows four variations of the error voltage with the control signal at 16%, 24%, 32%, and 40% duty cycle. For the 40% duty-cycle test case, the feedback network becomes active at an input voltage of 18 V. When the duty cycle was reduced to 32%, the feedback network becomes active at around 21 V of the input voltage. At 16% duty cycle, it was realized that the feedback network was not yet active at 36 V of the input voltage. This test case shows that when the feedback network is active, the error voltages are all below 2 V. Fig. 36.23 also gives the actual values of the error voltage and the control signals needed at each stage of the input voltage variations. A general rule from Fig. 36.23 will be "if the error voltage is high (i.e., max 6 V) and the change in error is zero (i.e., very small), then increase the control signal (i.e., duty cycle)." In Fig. 36.24, a 5 V output voltage level was tested for different constant control signals while increasing the input voltage. Four different test cases were conducted for duty-cycle values of 16%, 24%, 32%, and 40%. From the figure, it shows the various voltage levels at which the output voltage gets to the 5 V mark for the different duty cycles. It also shows that without any control, the output voltage will continue to increase without any bound. These experimental observations were in general very helpful in the design of the fuzzy-logic controller.

36.11.1 Membership Functions and Rules Generation

The chief problem of the construction of the fuzzy controller is related to the choice of the regulator parameters. Certainly, there is no systematic procedure for the design of a fuzzy controller (membership functions and rules generation), and this section is devoted to the determination of the fuzzy sets and the linguistic rules. The number of the linguistic sets of the proposed controller has been determined using laboratory experimentation and the responses of the DC-DC converter that have been compared with different numbers of the fuzzy sets. The actual responses have been compared with three, four, five, and seven fuzzy sets. It has been found that the use of more than five linguistic sets does not improve the tracking accuracy of the DC-DC converters but in fact increases the computation time. Consequently, four linguistic sets, positive large (PL), positive small (PS), negative large (NL), and negative small (NS), have been chosen for the input variable voltage error, $e(k)$, and three linguistic sets, positive medium (PM), zero (ZE), and negative medium (NM), have been chosen for that of the change in voltage error, $\Delta e(k)$. Additionally, five linguistic sets, positive large (PL), positive small (PS), zero, negative large (NL), and negative small (NL), have been chosen for the output variable of the fuzzy controller structure. The fuzzy controller utilizes triangular membership functions on the controller input. The triangular membership function is chosen owing to its simplicity. For the change in voltage error, $\Delta e(k)$, the initial values of the premise parameters (the corner coordinates of the triangle) are chosen so that the membership functions are equally spaced along the operating range of each input variable. The scaled input and output membership functions sets are shown in Figs. 36.25 through 36.27. The actual error measured from the feedback network ranges from 0.8 to about 6.0 V, while the control signal ranges from 16% to 50% duty cycle.

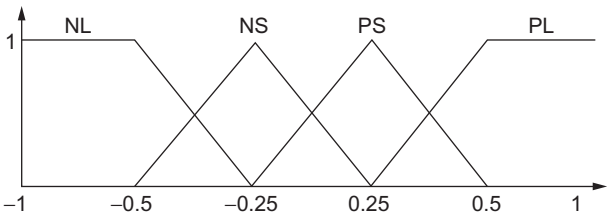


FIG. 36.25 Input membership functions for the error, $e(k)$.

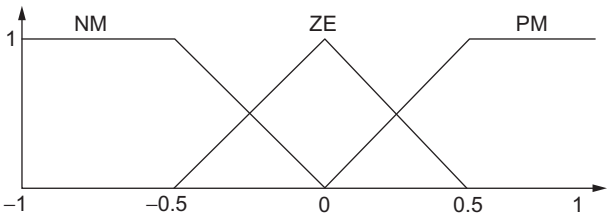


FIG. 36.26 Input membership functions for the change in error, $\Delta e(k)$.

The scaling factors $\xi_1 = 0.167$ and $\xi_2 = 0.01$ were determined using experimental tests in such a way that the normalized inputs $e(k)$ and $\Delta e(k)$ are well adapted to the universe of discourse $[-1,1]$ for any operating point. The linguistic control rules are established considering the dynamic behavior of the DC-DC converter and analyzing the error and its variation. To obtain control decision, the max-min inference method is used. It is based on the minimum function to describe the "AND" operator present in each control rule and the maximum function to describe the "OR" operator.

The output of the fuzzy controller structure is crisp, and thus a combined output fuzzy set must be defuzzified. To express the qualitative action in a quantitative action, the sum-product composition method was used. It calculates the crisp output as the weighted average of the centroids of all output membership functions. The output of the controller can be expressed as

$$O_o = \frac{\left(\sum_m O_m^* a_{Cm} \times b_{Cm}\right)}{\sum_m (O_m^* b_{Cm})}$$

where a_{Cm} and b_{Cm} are the centers and widths of the output fuzzy sets, respectively, for $m = 1,\ldots,5$. The values of the b_{Cm} s were chosen to be unity. This scaled output corresponds to the control signal (percent duty cycle) to be applied to maintain the output voltage at a constant value. Fig. 36.28 represents the normalized output O_o of the proposed fuzzy controller

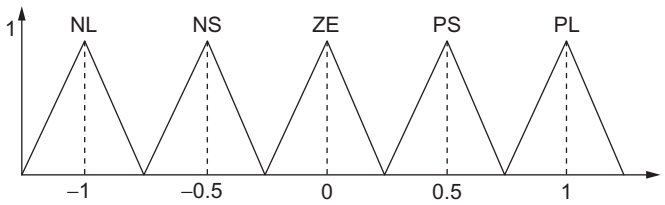


FIG. 36.27 Output membership functions for the control signal.

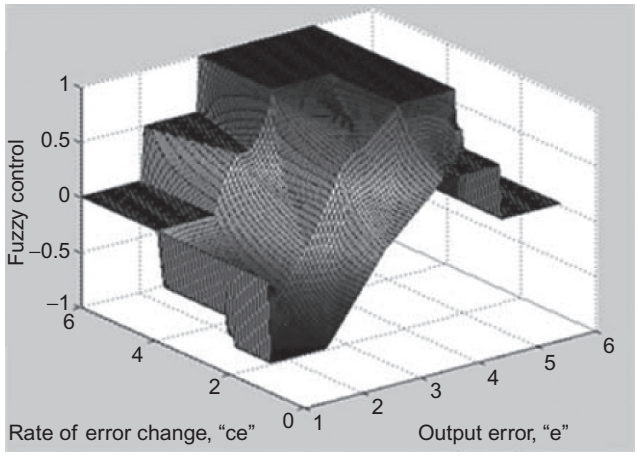


FIG. 36.28 Fuzzy control surface.

structure as a function of the error $e(k)$ and the change of error $\Delta e(k)$. It clearly illustrates the nonlinear characteristics of the proposed fuzzy controller structure.

36.12 Adaptive Network-Based Fuzzy Control System for DC-DC Converters

Adaptive network architecture, ANFIS, and a learning algorithm by which the ANFIS could construct a desired input-output mapping are proposed. The basic structure of a converter topology with adaptive network architecture is given in Fig. 36.29. Both fuzzy-logic principles and learning functions of neural networks are employed together to construct the adaptive fuzzy-network inference system for the control topology. Initially, a basic fuzzy-logic controller is set up utilizing linguistic rules, and then numerical data is used for training the controller. The number of membership functions is chosen so as to cover the entire input space. The converter is represented by a "black box" from which we only extract the terminals corresponding to input voltage (V_i), output voltage (V_o), and controlled switch (S). From these measurements, the ANFIS provides a signal proportional to a percentage duty-cycle signal for a peripheral interface microcontroller, PIC16F877, which generates the converters' actual duty cycle.

36.12.1 Topology of the Neural-Fuzzy Controller (NFC)

The proposed ANFIS is a multilayer neural network-based fuzzy-logic controller. The network architecture is built, such

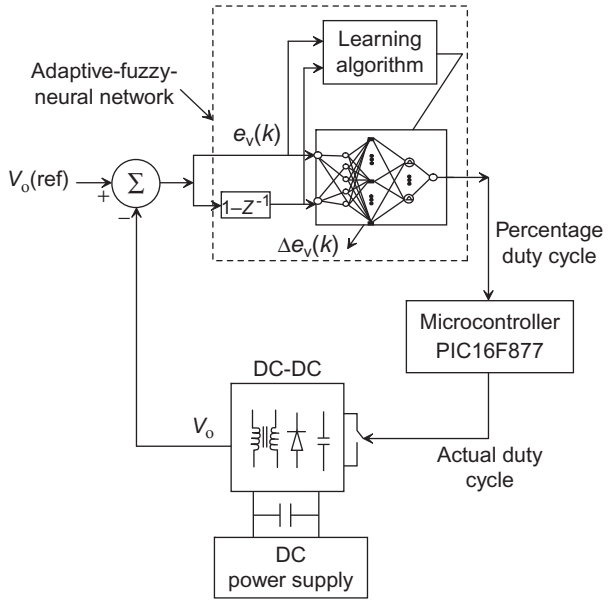


FIG. 36.29 Structure of a converter topology with adaptive network architecture.

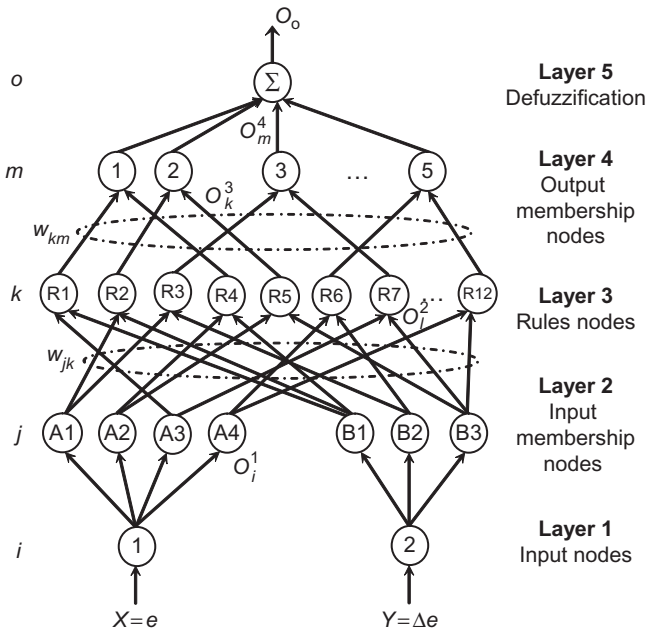


FIG. 36.30 Network architecture-based topology.

that the designer recognizes the internal nodes as they relate to the components of fuzzy controller. The system has a total of five layers. The architecture of the network is shown in Fig. 36.30. The scaled input and output membership functions sets are shown in Figs. 36.3–36.5. The actual error measured from the feedback network ranges from 0.8 to about 6.0 V, while the control signal ranges from 16% to 50% duty cycle.

36.12.1.1 Layer 1: Input Layer

Each node in this layer is an input node, which corresponds to one input variable. These nodes only bypass input signals to the next layer. The input variables are the output voltage error $e(k) = V_o(k) - V_{oref}(k)$ and change in voltage error $\Delta e(k) = [e(k) - e(k-1)]$, respectively. The fuzzy sets proposed for the input variable voltage error, $e(k)$, are positive large (PL), positive medium (PM), positive small (PS), and small (S) and that for the change in voltage error, $\Delta e(k)$, are positive medium (PM), zero (ZE), and negative medium (NM). The output of the neuron i in layer 1 is obtained as

$$O_i^1 = f_i^1\left(\text{net}_i^1\right) = \text{net}_i^1$$

where net_I^1 is the ith input to the node of layer 1, namely, the error and the change in the error.

36.12.1.2 Layer 2: Input Membership Layer

Each node in this layer acts as a linguistic label of one of the input variables in layer 1, that is, the membership value specifying the degree to which an input value belongs to a fuzzy set is determined in this layer. The triangular membership function is chosen owing to its simplicity. For the change in voltage

error, $\Delta e(k)$, the initial values of the premise parameters (the corner coordinates of the triangle) are chosen so that the membership functions are equally spaced along the operating range of each input variable. Due to the nonlinearity in the converter, the triangular membership for the error, $e(k)$, was slightly modified. The weights between the input and membership level are assumed to be unity. The output of neuron j in the second layer can be obtained as follows:

when $(X_i \geq a_j)$ and $(X_i \leq b_j)$

$$O_j^2 = f_j^2\left(\text{net}_j^2\right) = (X_i - a_j)/(b_j - a_j)$$

else when $(X_i \geq b_j)$ and $(X_i \leq c_j)$

$$O_j^2 = f_j^2\left(\text{net}_j^2\right) = (X_i - c_j)/(b_j - c_j)$$

where a_j, b_j, and c_j are the corners of the jth membership function in layer 2 shown in Fig. 36.31 and X_i is the ith input variable to the node of layer 2, which could be either the value of the error or the change in error.

36.12.1.3 Layer 3: Rule Layer

Each node in layer 3 multiplies the incoming signal and outputs the result of the product. The conjunction of the rule antecedents is evaluated by the fuzzy operation *intersection*, which is implemented by the product operator. Consequently, each node of this layer is a rule node that represents one fuzzy control rule. Each node takes two inputs: one from nodes A1–A4 and the other from nodes B1–B3 of layer 2. Nodes A1–A4 define the membership values for the voltage error, and nodes B1–B3 define the membership values for the change in voltage error. Accordingly, there are 12 nodes in layer 3 to form a fuzzy rule base for two input variables, with four linguistic variables for the input *voltage error*, $e(k)$, and three linguistic variables for the input *change in voltage error*, $\Delta e(k)$. The input/output links of layer 3 define the preconditions and the outcome of the rule nodes, respectively. The outcome is the strength applied to the evaluation of the effect defined for each particular rule. The output of neuron k in layer 3 is obtained as

$$O_k^3 = f_k^3\left(\text{net}_k^3\right) = \text{net}_k^3, \text{ where } \text{net}_k^3 = \prod_j w_{jk}^3 y_j^3$$

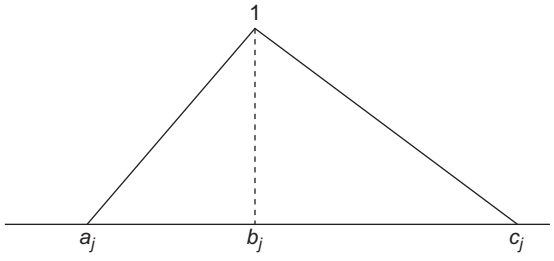


FIG. 36.31 A single membership function.

y_j^3 represents the j th input to the node of layer 3, and w_{jk}^3 is assumed to be unity.

36.12.1.4 Layer 4: Output Membership Layer

Neurons in this layer represent fuzzy sets used in the consequent of fuzzy rules. An output membership neuron receives inputs from the corresponding fuzzy rule neurons and combines them by using the fuzzy operation *union*. This was implemented by the *maximum* function. Layer 4 acts upon the output of layer 3 multiplied by the connecting weights. These link weights represent the output action of the rule nodes evaluated by layer 3. That output is given by

$$O_m^4 = f_m^4\left(\text{net}_{km}^4\right) = \max\left(\text{net}_{km}^4\right)$$

and

$$\text{net}_{km}^4 = O_k^3 w_{km}$$

where the count of k depends on the links from layer 3 to the particular mth output in layer 4 and the link weight w_{km} is the output action of the mth output associate with the kth rule. This level is essential in ensuring the system's stability and allowing a smooth control action.

36.12.1.5 Layer 5: Defuzzification Layer

Layer 5 is the output layer and acts as a defuzzifier. The single node in this layer takes the output fuzzy sets clipped by the respective integrated firing strengths and combines them into a single fuzzy set. The output of the neurofuzzy system is crisp, and thus a combined output fuzzy set must be defuzzified. The sum-product composition method was used. It calculates the crisp output as the weighted average of the centroids of all output membership functions.

$$O_o = f_o^5\left(\text{net}_o^5\right) = \text{net}_o^5$$

and

$$\text{net}_o^5 = \frac{\left(\sum_m O_m^4 \times a_{Cm} \times b_{Cm}\right)}{\sum_m \left(O_m^4 \times b_{Cm}\right)}$$

where a_{Cm} and b_{Cm} for $m = 1, \ldots, 5$ are the centers and widths of the output fuzzy sets, respectively. The values for the b_{Cm}'s were chosen to be unity. This scaled output corresponds to the control signal (percent duty cycle) to be applied to maintain the output voltage at a constant value.

36.12.2 Learning Algorithm

The only weights that are trained are those between layer 3 and layer 4 of Fig. 36.30. The back-propagation network is used to train the weights of this layer. The weights of the neural

network were trained offline before they were used in the experimental setup. The learning algorithm used can be described in the following steps:

Step 1: Calculate the error for the change in the control signal (duty cycle) based on the type of the converter.

$$E_o = T_o - O_o^5$$

where E_o, T_o, and O_o^5 are the output error, the target control signal, and the actual control signal, respectively.

Step 2: Calculate the error gradient.

$$\delta_m = E_o \times f'\left(O_1^4, \ldots, O_m^4\right)$$
$$\Rightarrow \delta_m = \left(T_o - O_o^5\right) \times f'\left(O_1^4, \ldots, O_m^4\right)$$

where

$$f\left(O_1^4, \ldots, O_m^4\right) = \frac{\sum_{j=1}^{m} O_j^4 \times a_{Cj}}{\sum_{j=1}^{m} O_j^4}$$

and the partial derivative of f with respect to O_m^4 is given by

$$f_{O_m^4}{}'\left(O_1^4, \ldots, O_m^4\right) = \frac{\sum_{\substack{j=1 \\ j \neq m}}^{m-1} O_j^4 \times \left(a_{Cm} - a_{Cj}\right)}{\left(\sum_{j=1}^{m} O_j^4\right)^2}$$

where a_{Ci} for $i = 1, \ldots, 5$ are the centers of the output fuzzy sets and O_j^4 is the firing strength from node j in layer 4.

Step 3: Calculate the weight correction

$$\Delta w_{km} = \eta \times \delta_m \times O_k^3$$

to increase the learning rate, the Sejnowski-Rosenberg updating mechanism was used, which takes into account the effect of past weight changes on the current direction of the movement in the weight space. This is given by

$$\Delta w_{km}(t) = \eta \times (1 - \alpha) \times \delta_m \times O_m^3 + \alpha \times \Delta w_{km}(t-1)$$

where α is a smoothing coefficient in the range of 0–1.0 and η is the learning rate.

Step 4: Update the weights.

$$w_{km}(t+1) = w_{km}(t) + \Delta w_{km}(t)$$

where t is the iteration number

The weights linking the rule layer (layer 3) and the output membership layer (layer 4) are trained to capture the system dynamics and therefore minimize the ripples around the operating point. The training results of the link weights are shown in Figs. 36.32 and 36.33.

In the initialization of the weights, wt5 and wt6 in Fig. 36.32 were set to a very small number of 0.001 with the initial assumption that those weights are almost redundant before the training begins. However, the neurofuzzy system was capable of correcting those assumptions. Weight wt5 finally converges to a positive value

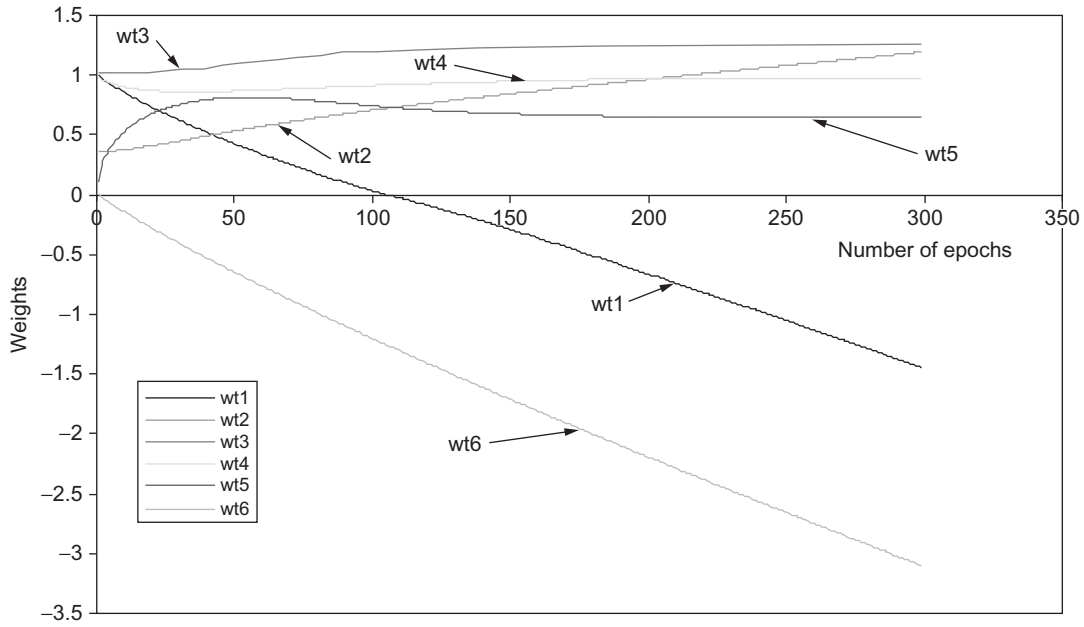


FIG. 36.32 Weight adaptations for the first set of six weights.

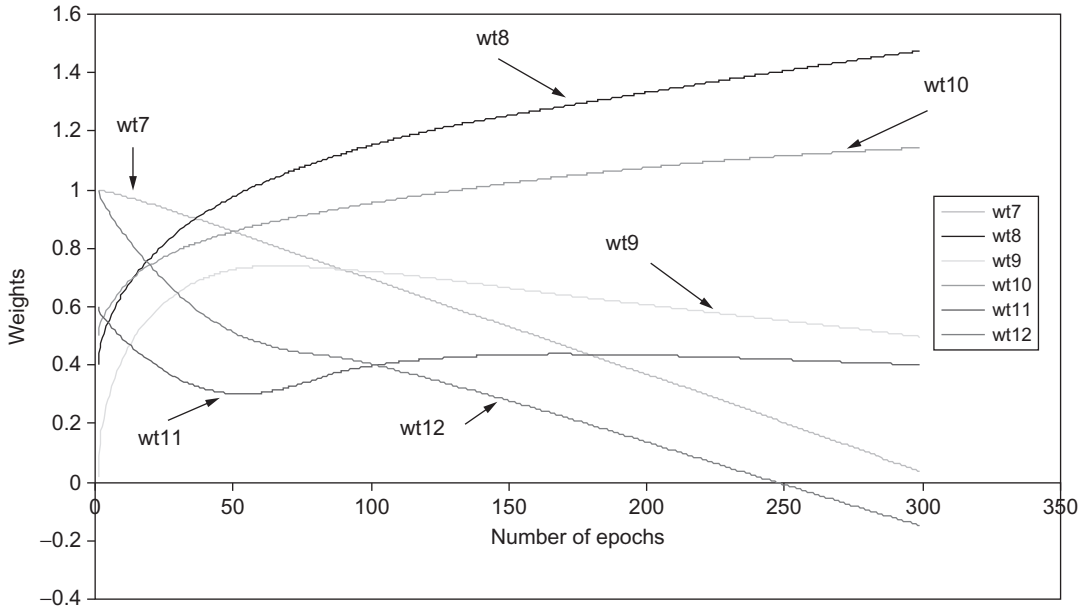


FIG. 36.33 Weight adaptations for the second set of six weights.

that indicates an excitatory rule weight, while wt6 converges to a negative number that is an inhibitory rule weight. Some of the weights change sign during the training process. Weight wt1 was initially set at a positive value but converges to a negative value that makes that rule weight inhibitory.

36.13 Summary

The presence of adaptive control via the EKF learning of the FNN control laws marks an improvement over the FL design. The motor drive over time is subject to experience degradation of mechanical parts or even electric characteristics, and the ability to automatically adapt the control laws to these changes is a feature that a nonadaptive fuzzy controller does not have. A genetic-based FPID controller and its integration with a classical PID in a global control scheme have been developed. Experimental results have shown excellent tracking performance of the proposed hybrid FPID controller and have convincingly demonstrated the usefulness of the FPID controller in high-performance drives with uncertainties. For the H-infinity-based controller, test results have shown that the proposed hybrid controller achieved good tracking performance and stable control, under loading conditions for a number of desired reference trajectories. The ability of the hybrid controller to achieve the tracking process with a high degree of accuracy, even in the presence of random disturbance, was also demonstrated, while the fuzzy application to the DC-DC converter topology showed considerable control performance over a wide range of operating conditions.

Acknowledgments

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References

[1] A. Sant, K.R. Rajagopal, PM synchronous motor speed control using hybrid fuzzy-pi with novel switching functions, IEEE Trans. Magn. 45 (10) (2009) 4672–4675.

[2] B.M. Hohan, A. Sinha, Analytical structure and stability analysis of a fuzzy PID controller, Appl. Soft Comput. 8 (2008) 749–758.

[3] A. Rubaai, M.J. Castro-Sitiriche, A.R. Ofoli, DSP-based laboratory implementation of hybrid fuzzy-pid controller using genetic optimization for high performance motor drives, IEEE Trans. Ind. Appl. 44 (6) (2008) 1977–1986.

[4] Y.-P. Kuo, T.-H.S. Li, GA-based fuzzy PI/PD controller for automotive active suspension system, IEEE Trans. Ind. Electron. 46 (6) (1999) 1051–1056.

[5] B.-G. Hu, G.K.I. Mann, R. Gosine, A systematic study of fuzzy PID controllers—function-based evaluation approach, IEEE Trans. Fuzzy Syst. 9 (5) (2001) 699–712.

[6] H.-X. Li, L. Zhang, K.-Y. Cai, G. Chen, An improved robust fuzzy-PID controller with optimal fuzzy reasoning, IEEE Trans. Syst. Man Cybern. 35 (6) (2005) 1283–1294.

[7] M. Masiala, B. Vafakhah, J. Salmon, A.M. Knight, Fuzzy self-tuning speed control of an indirect field-oriented control induction motor drive, IEEE Trans. Ind. Appl. 44 (6) (2008) 1732–1740.

[8] M. Barut, S. Bogosyan, M. Gokasan, Speed sensorless estimation for induction motors using extended Kalman filters, IEEE Trans. Ind. Appl. 54 (1) (2007) 272–280.
[9] K. Szabat, T. Orlowska-Kowalska, Performance improvement of industrial drives with mechanical elasticity using nonlinear adaptive Kalman filter, IEEE Trans. Ind. Electron. 55 (3) (2008) 1075–1084.
[10] K.K. Ahn, D.Q. Truong, Online tuning fuzzy PID controller using robust extended Kalman filter, J. Process Control 19 (2009) 1011–1023.
[11] D.J. Lary, H.Y. Mussa, Using an extended Kalman filter learning algorithm for feed-forward neural networks to describe tracer correlations, Atmos. Chem. Phys. Discuss. 4 (2004) 3653–3657.
[12] S. Singhal, L. Wu, Training feedforward networks with extended Kalman Filter algorithm, in: Proc. International Conf. ASSP, 1989, pp. 1187–1190.
[13] S.-J. Ho, L.-S. Shu, S.-Y. Ho, Optimizing fuzzy neural networks for tuning PID controllers using an orthogonal simulated annealing algorithm OSA, IEEE Trans. Fuzzy Syst. 14 (3) (2006) 421–434.
[14] I. del Campo, J. Echanobe, G. Bosque, J.M. Tarela, Efficient hardware/software implementation of an adaptive neuro-fuzzy system, IEEE Trans. Fuzzy Syst. 16 (3) (2008) 761–778.
[15] M.N. Uddin, M.A. Rahman, Development and implementation of a hybrid intelligent controller for interior permanent-magnet synchronous motor drives, IEEE Trans. Ind. Appl. 40 (1) (2004) 68–76.
[16] A. Rubaai, R. Kotaru, Neural net based robust controller design for brushless DC motor drives, IEEE Trans. Syst. Man Cybern. 29 (3) (1999) 460–473.
[17] B.S. Chen, C.H. Lee, Y.C. Chang, H ∞ tracking design of uncertain nonlinear SISO systems: adaptive fuzzy approach, IEEE Trans. Fuzzy Syst. 4 (1) (1996) 32–43.
[18] A. Balestrino, A. Landi, L. Sani, CUK converter global control via fuzzy logic and scaling factor, IEEE Trans. Ind. Appl. 38 (2) (2002) 406–413.
[19] E. Vidal, L. Martine, F. Guinjoan, J. Calvente, S. Gomariz, Sliding and fuzzy control of a boost converter using an 8-Bit microcontroller, Proc. IEEE Elect. Pow. Appl. 151 (1) (2004) 5–11.
[20] J. Alvarez, I. Cervantes, G. Espinosa, P. Maya, A. Morales, A stable design of PI control for DC-DC converters with an RHS zero, IEEE Trans. Circuits Syst. 48 (1) (2001) 103–106.
[21] J. Principe, N.R. Euliano, W.C. Lefebvre, Neural and Adaptive Systems, John Wiley & Sons, New York, 2000.
[22] J.S.R. Jang, C. Sun, E. Mizutani, Neuro-Fuzzy and Soft Computing, Prentice Hall, Englewood Cliffs, NJ, 1997.
[23] G.E. Bloom, IMAGINE, a Converter Kit for Exploring the Fascinating World of Integrated-Magnetic Concepts, 1991. San Rafael, **CA**.

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37

Artificial Neural Network Applications in Power Electronics and Electric Drives

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37.1 Introduction

In classical control systems, knowledge of the controlled system (plant) is required in the form of a set of algebraic and differential equations, which analytically relate inputs and outputs. However, these models can become complex, rely on many assumptions, may contain parameters that are difficult to measure, or may change significantly during operation as in the case of the rotor-flux-oriented control (RFOC) induction motor drive. Classical control theory suffers from some limitations due to the assumptions made for the control system such as linearity and time invariance. These problems can be overcome by using artificial intelligence-based control techniques, and these techniques can be used, even when the analytic models are not known. Such control systems can also be less sensitive to parameter variation than classical control systems.

The main advantages of using artificial intelligence-based controllers and estimators are the following:

- Their design does not require a mathematical model of the plant.
- They can lead to improved performance, when properly tuned.
- They can be designed exclusively on the basis of linguistic information available from experts or by using clustering or other techniques.
- They may require less tuning effort than conventional controllers.
- They may be designed on the basis of data from a real system or a plant in the absence of necessary expert knowledge.
- They can be designed using a combination of linguistic- and response-based information.

Generally, the following two types of intelligence-based systems are used for estimation and control of drives, namely:

(a) Artificial neural networks (ANNs)
(b) Fuzzy-logic systems (FLSs)

In different applications in power electronics and electric drives, there are occasions where an output y has to be estimated for an input x. This is generally accomplished with the help of mathematical equations of the system under consideration. Sometimes, it may not be possible to have an accurate mathematical model, or there is no conventional model at all that can be used. In these circumstances, model-free estimators

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are required that can be used either ANNs or fuzzy-logic systems. A mathematical model-based system can operate smoothly when there is no noise in the inputs, but they might fail when the input has noise or if the inputs themselves are uncertain. Also, depending on the complexity of the mathematical model, the computation times can be excessive leading to difficulties for practical implementation.

A conventional function approximator, a neural function estimator, and how these estimators are arrived at are discussed briefly in Section 37.2. It will be shown how neural estimators are used in the estimation of speed, flux, torque, etc. for an induction motor. Some of these estimators are briefly reviewed in Section 37.3. Also, the ANNs have been used for identification and control of stator current in induction motor drives, and these are briefly described in Section 37.4. In addition to their applications to motor drives, they are also used in control of power converters. Some of these applications are discussed in Section 37.5.

37.2 Conventional and Neural Function Approximators

37.2.1 Conventional Approximator

A conventional function approximator should give a good prediction of output data, when a system is presented with a new input data. A conventional function approximator uses a mathematical model of the system as shown in Fig. 37.1A. Sometimes, it is not possible to have an accurate mathematical model of the system, in such a case; mathematical model-free approximators are required, as shown in Fig. 37.1B. A conventional function approximator can easily be replaced by a neural-network-based function approximator.

37.2.2 Neural Function Approximator

The function $y = f(x_1, x_2, \ldots, x_n)$ is the function to be approximated, and $x_1, x_2, x_3, \ldots x_n$ are the n variables (n inputs), and the approximator uses the sum of nonlinear functions $g_1, g_2, g_3, g_4, \ldots, g_i$, where each of the g is nonlinear function of a single variable. Thus,

$$y = f(x_1, x_2, \ldots, x_n) = g_1 + g_2 + g_3 + \cdots + g_{2n+1} = \sum_{i=1}^{2n+1} g_i \tag{37.1}$$

where g_i is a real and continuous nonlinear function that depends only on a single-variable z_i. The output y can also be represented as

$$y = \sum_{j=1}^{n} w_{Mj} x_j = w_{M1} x_1 + w_{M2} x_2 + \cdots w_{Mn} x_n \tag{37.2}$$

These equations can be represented by a network shown in Fig. 37.2. There are n input nodes in the input layer and M hidden nodes in the hidden layer.

Fig. 37.3 shows the schematic diagram of a neural approximation, and Fig. 37.4 shows the technique of its training. The error (e) between the desired nonlinear function (y) and the nonlinear function ($\hat{y}$) obtained by the neural estimator is the input to the learning algorithm for the artificial neural estimator. This type of learning is known as back propagation.

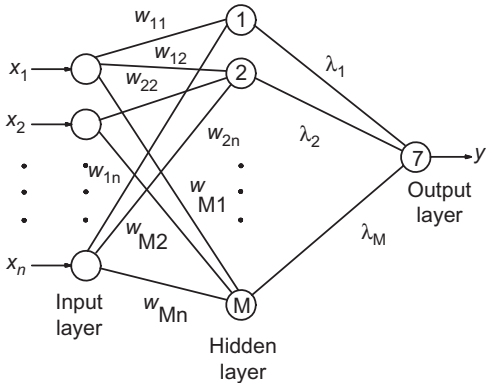


FIG. 37.2 Artificial neural network to generate the required function.

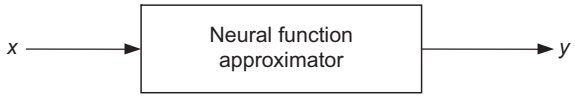


FIG. 37.3 Schematic of a neural function approximator.

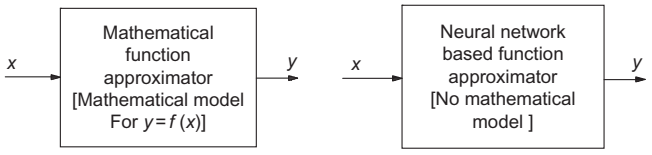


FIG. 37.1 Conventional and neural-network-based function approximators.

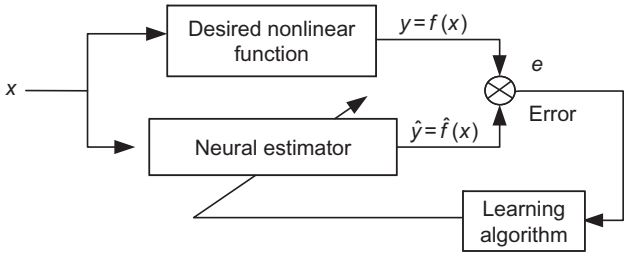


FIG. 37.4 Training of a neural function approximator.

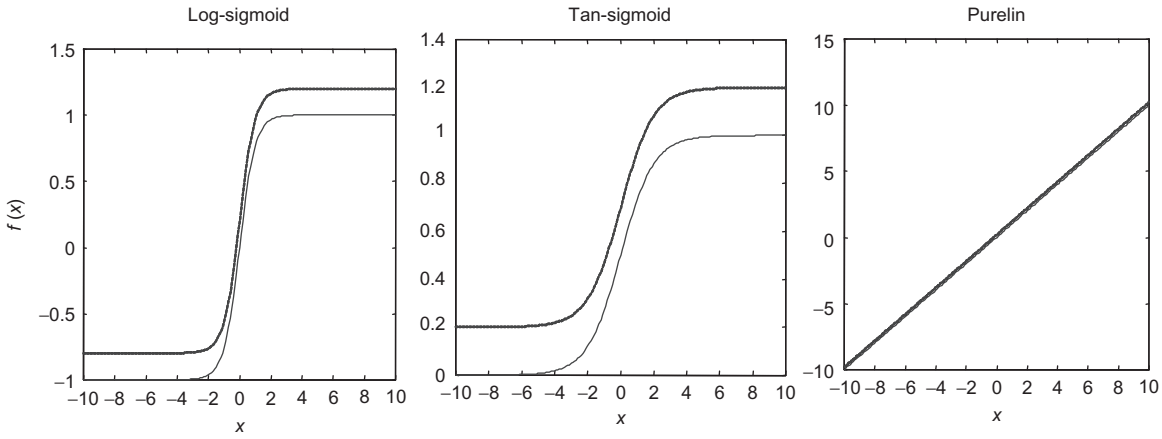


FIG. 37.5 Log-sigmoid, tan-sigmoid, and purelin activation functions.

The output of a single neuron can be represented as

$$a_i = f_i\left\{\sum_{j=1}^{n} w_{ij}x_j(t) + b_i\right\} \tag{37.3}$$

where f_i is the activation function and b_i is the bias. Fig. 37.5 shows a number of possible activation functions in a neuron. The simplest of all is the linear activation function, where the output varies linearly with the input but saturates at ± 1 as shown with a large magnitude of the input. The most commonly used activation functions are nonlinear, continuously varying types between two asymptotic values 0 and 1 or -1 and $+1$. These are, respectively, the sigmoidal function also called log-sigmoid and the hyperbolic tan function also called tan-sigmoid.

The learning process of an ANN is based on the training process. One of the most widely used training techniques is the error back-propagation technique, a scheme that is illustrated in Fig. 37.4. When this technique is employed, the ANN is provided with input and output training data, and the ANN configures its weights. The training process is then followed by supplying with the real input data, and the ANN then produces the required output data.

The total network error (sum of squared errors) can be expressed as

$$E = \frac{1}{2}\sum_{k=1}^{P}\sum_{j=1}^{K}\left(d_{kj} - o_{kj}\right)^2 \tag{37.4}$$

where E is the total error, P is the number of patterns in the training data, k is the number of outputs in the network, d_{kj} is the target (desired) output for the pattern K, and $o_{kj}\left(=y_{kj}\right)$ is the jth output of the kth pattern. The minimization of the error can be arranged with different algorithms such as the gradient descent with momentum, Levenberg-Marquardt, reduced memory Levenberg-Marquardt, and Bayesian regularization.

37.3 ANN-Based Estimation in Induction Motor Drives

Artificial neural networks have found widespread use in function approximation. It has been shown that, theoretically, a three-layer ANN can approximate arbitrarily closely, any nonlinear function, provided that it is nonsingular. Some of the ANN-based estimators reported in the literature for rotor flux, torque, and rotor speed of induction motor drive are discussed in the following section.

37.3.1 Speed Estimation

In general, steady-state and transient analysis of induction motors is done using space-vector theory, with the mathematical model having the parameters of the motor. To estimate the various machine quantities such as stator- and rotor-flux linkages, rotor speed, and electromagnetic torque, the above mathematical model is normally used. However, these machine quantities could be estimated without the mathematical model by using an ANN. Here, no assumptions have to be made about any type of nonlinearity.

As an example, the rotor speed of an induction motor can be estimated from the direct and quadrature-axis stator voltages and currents in the stationary reference frame, as shown in Fig. 37.6. A three-layer feedforward neural network structure with $8 \times 7 \times 1$ (eight input, seven hidden, and one output) is used in this case. The input nodes were selected as equal to the number of input signals and the output nodes as equal to the number of output signals. The number of hidden layer neurons is generally taken as the mean of the input and output nodes. In this speed estimator ANN, seven hidden neurons were selected.

The results of an experiment conducted on a 1.1 kW, 415 V, 3 phase, 4 pole, 50 Hz induction motor is explained in this section. In order to investigate the case of speed estimation using ANN, a rotor-flux-oriented induction motor drive was set up in

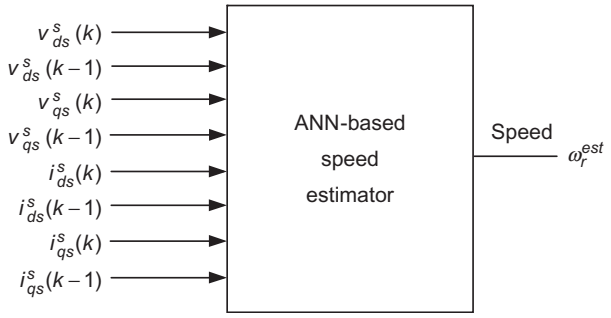


FIG. 37.6 ANN-based speed estimator for induction motor.

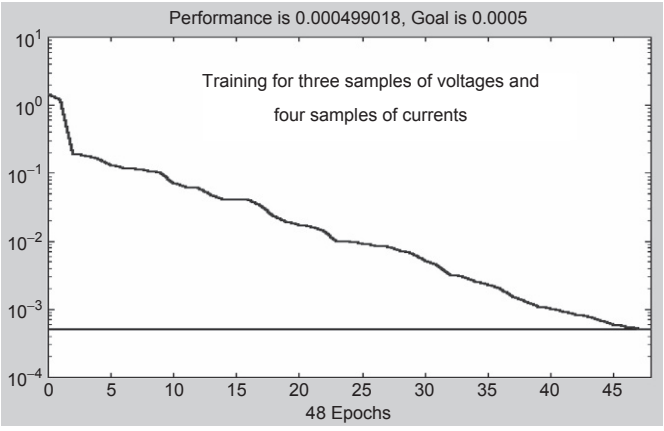


FIG. 37.7 The error plot of $8 \times 7 \times 1$ network training for speed estimation.

the laboratory, where the speed reference was changed in steps of 100 rpm and reversed every time the speed reached 1000 rpm. The load torque on the motor was kept constant at its full load rating. The stator voltages, stator currents, and rotor speed were measured for 5 s, and a data file was generated. The neural network was then trained using the *trainlm* algorithm with this data file. The training of the neural network converged after 48 epochs, and the error plot for this network training is shown in Fig. 37.7. The estimated speed was predicted with the trained neural network, and the result is shown in Fig. 37.8.

The noisy data in the plot are the estimated speed, and the continuous line is the speed measured with the encoder. The speed estimation was found to fail for speeds <100 rpm. If the trained neural network has to predict the speed under the complete range of operation of the drive, the data for training the neural network also have to be taken for the whole range. From this example investigated, it was found that the off-line training of the neural network could not produce satisfactory results, and it can be concluded that these off-line methods are not most suitable for these applications.

Artificial neural networks were also used for the estimation of the rotor speed of an induction motor together with the help of induction motor dynamic model. Though the technique gives a fairly good estimate of the speed, this technique lies more in the adaptive control area than in neural networks. The speed is not obtained at the output of a neural network; instead, the magnitude of one of the weights corresponds to the speed. The four quadrant operation of the drive was not possible for speeds <500 rpm. The motor was not able to follow the speed reference during the reversal for speeds <500 rpm. The drive worked satisfactorily for speeds above 500 rpm. Even though this method does not fall into a true neural network estimator, the results achieved with this type of implementation were very good except for lower speeds.

Alternately, the estimated speed can be made available at the output of a neural network as shown in Fig. 37.9. This speed estimator used a three-layer neural network with five input nodes, one hidden layer, and one output layer to give the estimated speed $\hat{\omega}_r(k)$ as shown in Fig. 37.9. The three inputs to the ANN are a reference model flux λ_r^*, an adjustable model flux $\hat{\lambda}_r$, and $\hat{\omega}_r(k-1)$, the time delayed estimated speed. The multilayer and recurrent structure of the network makes it robust to parameter variations and system noise. The main advantage of their ANN structure lies in the fact that they have used a recurrent structure that is robust to parameter variations and system noise. These authors were able to achieve a speed control error of 0.6% for a reference speed of 10 rpm. The speed control error dropped to 0.584% for a reference speed of 1000 rpm.

37.3.2 Flux and Torque Estimation

The same principle as described in Section 37.3.1 can also be extended for simultaneous estimation of more quantities such as torque and stator flux. When more quantities or variables have to be estimated, the complex ANN has to implement a complex nonlinear mapping.

The four feedback signals required for a direct field-oriented induction motor drive can be estimated using ANNs. A $4 \times 20 \times 4$ multilayer network has been used for the estimation of the rotor-flux magnitude, the electromagnetic torque, and the sine/cosine of the rotor-flux angle. It has been demonstrated both by modeling and experimental results that the above estimated quantities were almost equal to the same quantities computed by a DSP-based estimator. Both the estimated torque and rotor-flux signals using neural network were found to have higher ripple content compared with the DSP-based estimated quantities. It could be concluded that a properly trained ANN could totally eliminate the machine model equations as evident from the results reported.

In another application, an ANN with $5 \times 8 \times 8 \times 2$ structure has been used to estimate the stator flux using the measured induction motor stator variable quantities. After successful training, the ANN was used in a direct field-oriented controlled drive. The rotor flux is computed from the stator flux estimate provided by the ANN and the stator current. This particular

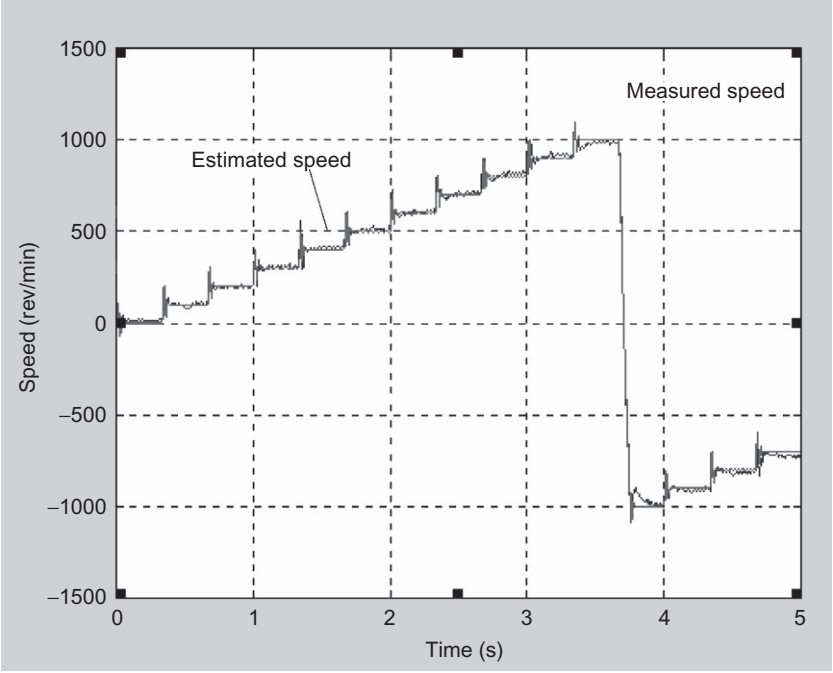


FIG. 37.8 Measured speed versus estimated speed with ANN for induction motor.

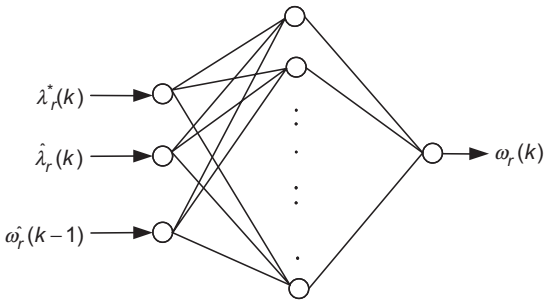


FIG. 37.9 Structure of the neural network for the induction motor speed estimation.

implementation also included an ANN-based decoupler which was used for the indirect field-oriented (IFO) drive. An ANN with a structure of $2 \times 8 \times 8 \times 1$ was used for implementing the mapping between the flux and torque references and the stator current references. The estimated rotor flux using an ANN and a conventional FOC controller was shown to be equal. These authors have used experimental data for the ANN training, and thus, the effect of motor parameters was reduced. The authors were unable to use these estimated fluxes for controlling the induction motor in the experiment. The structure of the ANN used for this estimation is only that of a static ANN. It is preferable to have a dynamic neural network for this purpose.

37.3.3 Rotor Resistance Identification Using ANN

37.3.3.1 Off-Line Trained ANN

The artificial neural network can also be used for the rotor time constant adaptation in indirect field-oriented controlled drives. One of the implementation reported in the literature is shown in Fig. 37.10. There are five inputs to the T_r estimator, namely $v_{ds}^s, v_{qs}^s, i_{ds}^s, i_{qs}^s, \omega_r$. The training signals are generated with step variations in rotor resistance for different torque reference T_e^* and flux command λ_r^*, and the final network is connected in the IFO controller as shown in Fig. 37.10. The rotor time constant was tracked by a proportional integral (PI) regulator that corrects any errors in the slip calculator. The output of this regulator is summed with that of the slip calculator, and the result constitutes the new slip command that is required to compensate for the rotor time constant variation. The major drawback of this scheme is that the final neural network is only an off-line trained neural network with a limited data file obtained from the modeling.

37.3.3.2 On-Line Trained ANN

The limitations of off-line trained ANN are overcome by using an online trained ANN configuration. The method discussed in this section has used an online trained ANN for adaptation of R_r of an induction motor in the RFOC induction motor drive. The error between the desired state variable of an induction

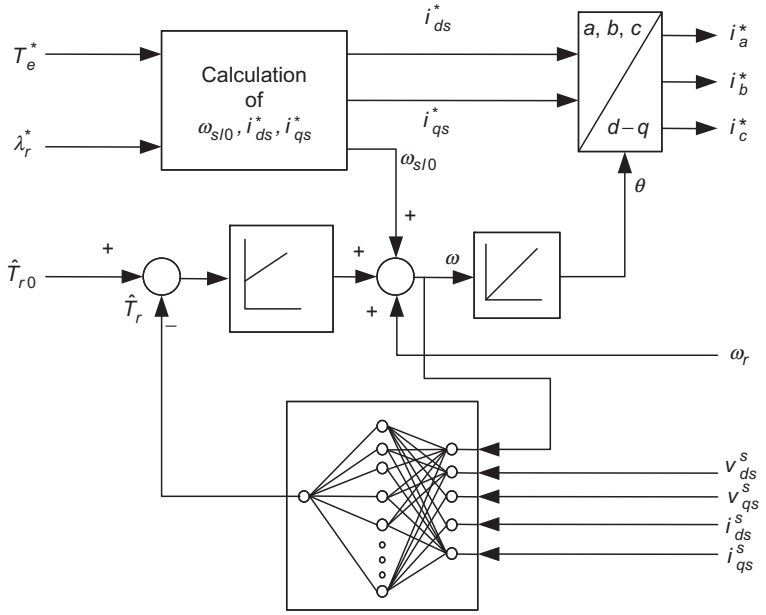


FIG. 37.10 Principle of rotor time constant adaptation.

motor and the actual state variable of a neural model is back propagated to adjust the weights of the neural model, so that the actual state variable tracks the desired value.

The principle of online estimation of rotor resistance (R_r) with multilayer feedforward artificial neural networks using online training has been described in "Multilayer feedforward ANN" section. This technique was then investigated with the help of modeling studies with a 1.1 kW squirrel-cage induction motor (SCIM), described in "Rotor resistance estimation for RFOC using ANN" section. The modeling results are presented in "Modeling results" section. In order to validate the modeling studies, modeling results were compared with those from an experimental setup with a SCIM under RFOC. These experimental results are presented in "Experimental results" section.

Multilayer feedforward ANN

Multilayer feedforward neural networks are regarded as universal approximations and have the capability to acquire nonlinear input-output relationships of a system by learning via the back-propagation algorithm. It should be possible that a simple two-layer feedforward neural network trained by the back-propagation technique can be employed in the rotor resistance identification. The modified technique using ANN proposed in this section can be implemented in real time so that the resistance updates are available instantaneously, and there is no convergence issues related to the learning algorithm. The two-layered neural network based on a back-propagation technique is used to estimate the rotor resistance. Two models of the state variable estimation are used; one provides the actual induction motor output, and the other one gives the neural model output. The total error between the desired and actual state variables is then back propagated as shown in Fig. 37.11, to adjust the weights of the neural model, so that the output of this model coincides with the actual output. When the training is completed, the weights of the neural network should correspond to the parameters in the actual motor.

Rotor resistance estimation for RFOC using ANN

The basic structure of an adaptive scheme described by Fig. 37.11 is extended for rotor resistance estimation of an induction motor as illustrated in Fig. 37.12. Two independent observers are used to estimate the rotor-flux vectors of the induction motor. If the rotor-flux linkages are estimated using the stator voltages and stator currents, they are referred to as *voltage model*, and if the rotor-flux linkages are estimated using the stator currents and rotor speed, they are referred to as *current model*.

The stator flux linkages based on the neural network model in Fig. 37.12 can be represented using Eq. (37.5), which is derived from the sample data models of the combined voltage and current model equations of the induction motor:

$$\overleftarrow{\lambda_r^{s^{nm}}}(k) = W_1X_1 + W_2X_2 + W_3X_3 \tag{37.5}$$

The neural network model represented by Eq. (37.5) is shown in Fig. 37.13, where W_1, W_2, and W_3 represent the weights of the networks and X_1, X_2, and X_3 are the three inputs to the network. If the network shown in Fig. 37.13 has to be used to estimate R_r, where W_2 is already known, then W_1 and W_3 need to be updated.

The weights of the network, W_1 and W_3, are found from training, so as to minimize the cumulative error function E_1:

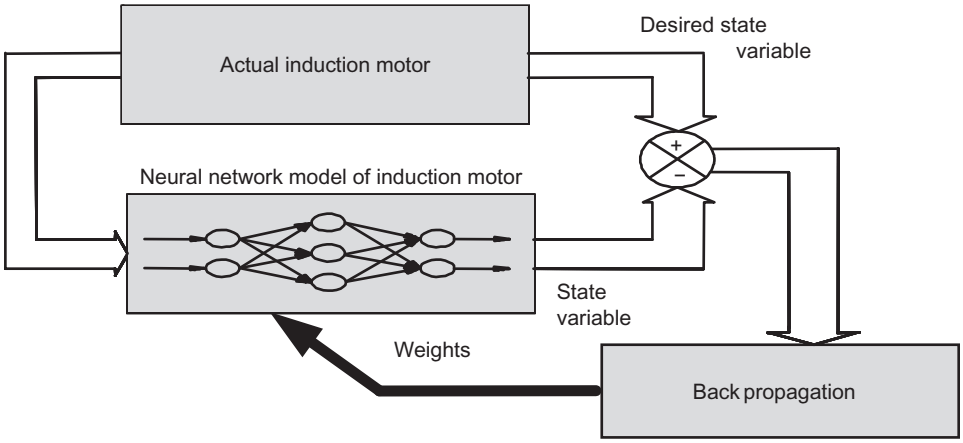


FIG. 37.11 Block diagram of rotor resistance identification using neural networks.

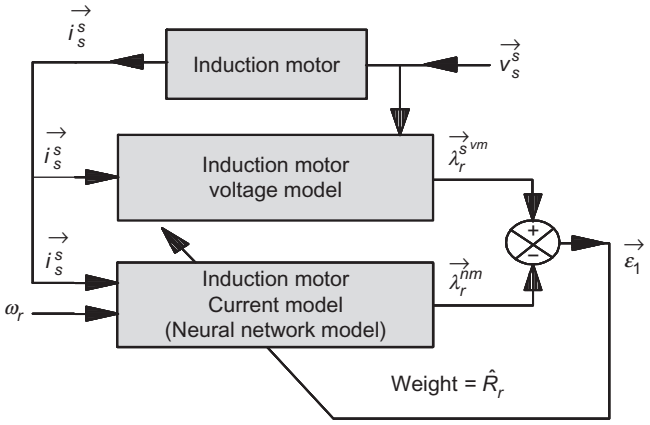


FIG. 37.12 Structure of the neural network system for R_r estimation.

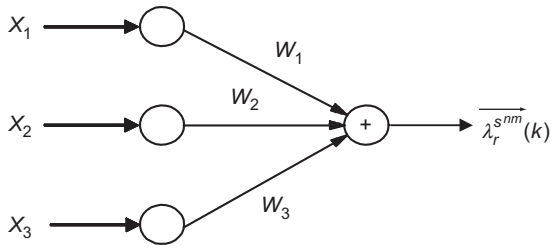


FIG. 37.13 Two-layered neural network model for rotor-flux linkage estimation.

$$E_1 = \frac{1}{2}\vec{\varepsilon}_1^{\,2}(k) = \frac{1}{2}\left\{\overleftarrow{\lambda_r^{s^{vm}}}(k) - \overleftarrow{\lambda_r^{s^{im}}}(k)\right\}^2 \tag{37.6}$$

The weight of the neural network W_1 has to be adjusted using generalized delta rule.

To accelerate the convergence of the error back-propagation learning algorithm, the current weight adjustment has to be supplemented with a fraction of the most recent weight adjustment, as indicated in Eq. (37.7):

$$W_1(k) = W_1(k-1) - \eta_1 \vec{\delta} X_2 + \alpha_1 \Delta W_1(k-1) \tag{37.7}$$

where α_1 is a user-selected positive momentum constant and η_1 is the training coefficient.

The rotor resistance R_r can now be calculated from W_3 from Eq. (37.8) as follows:

$$\hat{R}_r = \frac{L_r W_3}{L_m T_s} \tag{37.8}$$

Modeling results

A schematic diagram showing the implementation of a rotor resistance estimator in RFOC controller for induction motor is shown in Fig. 37.14. The stator voltages and currents are measured to estimate the rotor-flux linkages using the voltage model as shown in this figure. The inputs to the rotor resistance estimator (RRE) are the stator currents, the rotor-flux linkages $\lambda_{dr}^{s^{vm}}$, $\lambda_{qr}^{s^{vm}}$, and the rotor speed ω_r. The estimated rotor resistance $\hat{R}_r$ will then be used in the RFOC controllers for the flux model. The response of the drive together with the rotor resistance estimator OFF is shown in Fig. 37.15 for an abrupt change in R_r of motor, from 6.03 to 8.5 Ω at 0.8 s. The possible changes in the estimated motor torque T_e, the rotor-flux linkage λ_{rd} with this estimator were noted.

Subsequently, the results of the drive were looked at with RRE ON, so that the rotor resistance in the controller R_r' was updated with the estimated rotor resistance $\hat{R}_r$ as shown in Fig. 37.16. The estimated rotor resistance $\hat{R}_r$ has converged to the rotor resistance of the motor R_r within 50 ms.

The response of the drive system with the RRE using ANN is also shown for a practical profile in load torque, speed, and change in R_r. The R_r was increased from 6.03 to 8.5 Ω over a period of 8 s, and the torque and rotor-flux linkage are shown in Fig. 37.17 when the RRE is OFF. For rapid reversals of the drive and variations in load torque, there are significant errors in rotor-flux linkages and thus errors in estimated torques.

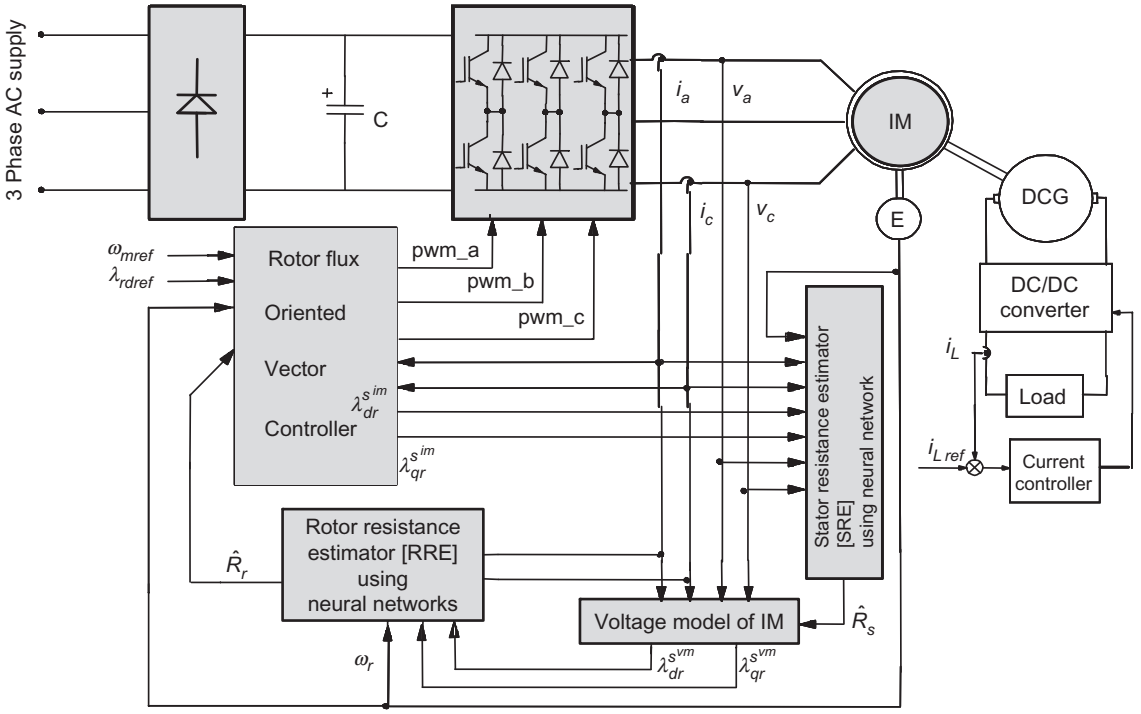


FIG. 37.14 Block diagram of the RFOC induction motor drive with online rotor and stator resistance tracking using ANN.

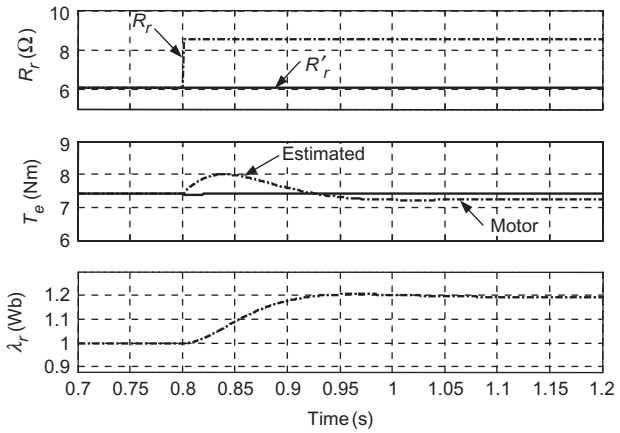


FIG. 37.15 Effect of rotor resistance variation without rotor resistance estimator for 40% step change in R_r —modeling results.

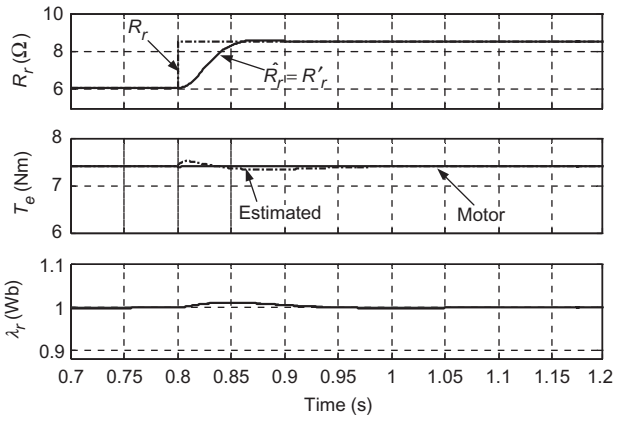


FIG. 37.16 Effect of rotor resistance variation with rotor resistance estimator using ANN for 40% step change in R_r —modeling results.

Subsequently, the RRE block was switched ON, and it can be observed that the rotor resistance estimator was tracking very well even during the worst dynamics in the motor speed and load torques as shown in Fig. 37.18. The estimated rotor resistance $\hat{R}_r$ tracked the actual rotor resistance of the motor R_r throughout except that there was some small error during the reversal of the motor. The rotor-flux linkage λ_{rd} was found to remain constant at 1.0 Wb during this transient condition. The current i_{qs} also remained constant as the torque is now perfectly decoupled.

Experimental results

The practical implementation of the above rotor resistance estimation was found functioning very well in the experimental drive setup. The results of the R_r estimation obtained from the experiment is shown in Fig. 37.19 taken from a heat-run test conducted on an induction motor. As the RRE calculated, the rotor resistance using variables in stationary reference frame, the d-axis rotor-flux linkages of the current model (λ_{dr}^{im}), the voltage model (λ_{dr}^{vm}), and the neural model (λ_{dr}^{nm}), taken at the end of heat run, is also recorded as shown in Fig. 37.20.

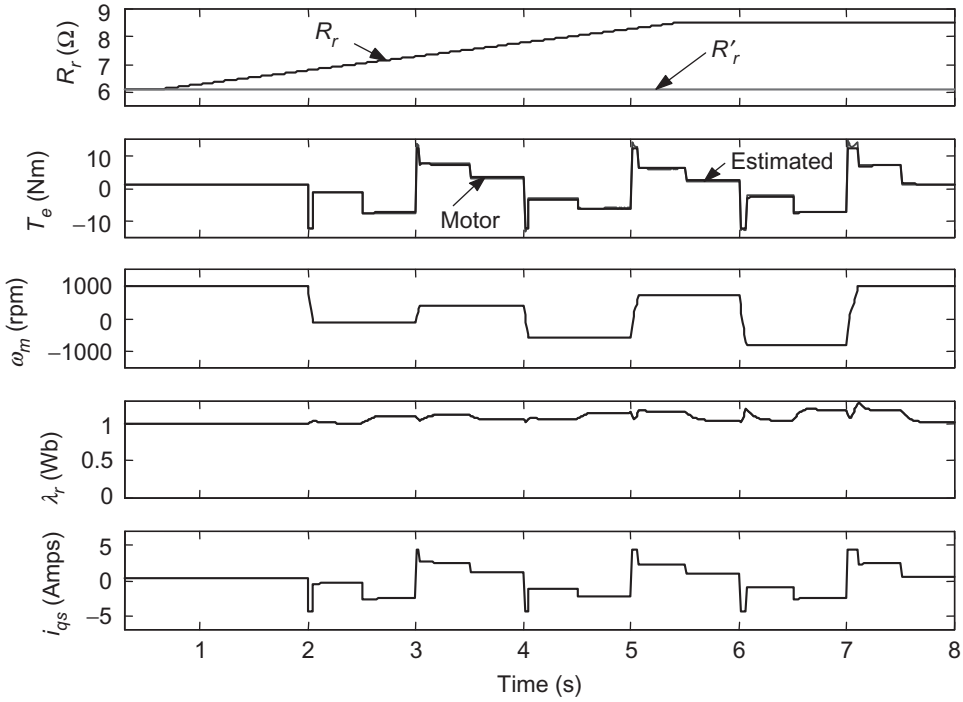


FIG. 37.17 Effect of rotor resistance variation without rotor resistance estimator for 40% ramp change in R_r —modeling results.

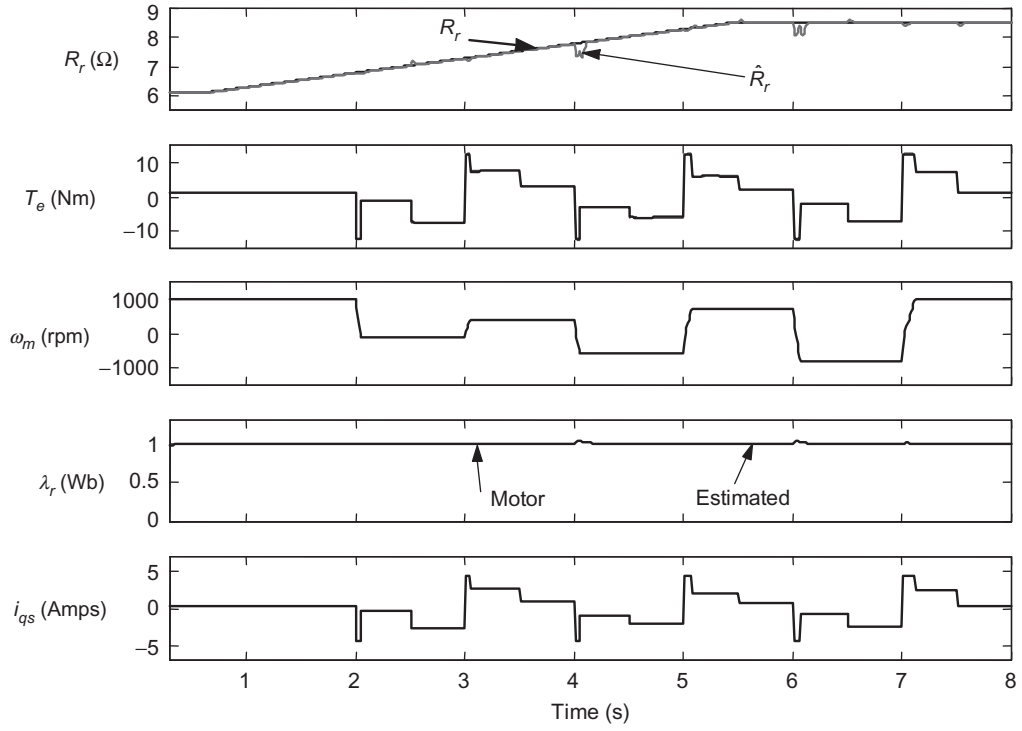


FIG. 37.18 Effect of rotor resistance variation with rotor resistance estimator using ANN for 40% ramp change in R_r —modeling results.

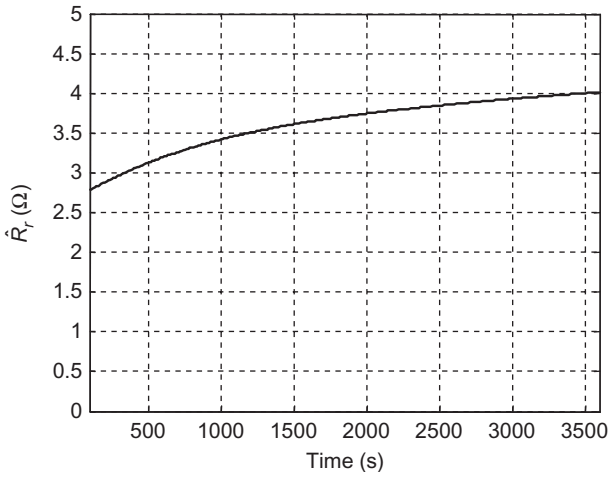


FIG. 37.19 Estimated R_r using ANN—experimental results.

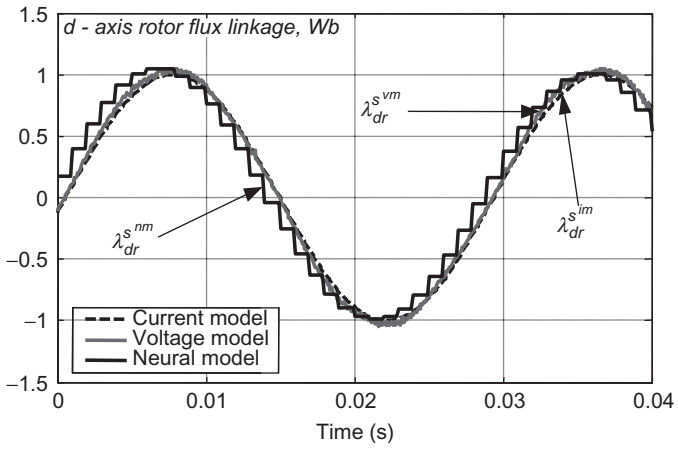


FIG. 37.20 Rotor fluxes estimated during R_r estimation using ANN—experimental results.

37.3.4 Stator Resistance Estimation Using ANN

In this section, the capability of a neural network has been deployed to have online estimator for stator resistance in an RFOC induction motor drive. The stator resistance observer was realized with a recurrent neural network with feedback loops trained using the standard back-propagation learning algorithm. Such architecture with recurrent neural network is known to be a more desirable approach, and the implementation reported in this section confirms this.

The d-axis stator current in the stationary reference frame in the discrete form can be represented using the voltage and current model equations of the induction motor:

$$i_{ds}^{s*}(k) = W_4 i_{ds}^{s*}(k-1) + W_5 \lambda_{dr}^{s\,im}(k-1) + W_6 \omega_r \lambda_{qr}^{s\,im}(k-1) + W_7 v_{ds}^{s}(k-1) \tag{37.9}$$

where, $W_4 = 1 - \frac{T_s}{\sigma L_s}\frac{L_m^2}{L_r T_r} - \frac{T_s}{\sigma L_s} R_s$; $W_5 = \frac{T_s}{\sigma L_s}\frac{L_m}{L_r T_r}$

$W_6 = \frac{T_s}{\sigma L_s}\frac{L_m}{L_r}$; $W_7 = \frac{T_s}{\sigma L_s}$

The weights W_5, W_6, and W_7 are calculated using the induction motor parameters, the rotor speed ω_r, and the sampling interval used in the estimator T_s.

The relationship between stator current and stator resistance is nonlinear that could be easily mapped using a neural network.

When this Eq. (37.9) is represented graphically, it resembles a recurrent neural network as shown in Fig. 37.21. The standard back-propagation learning rule can then be employed for training this neural network. The weight W_4 is the result of training so as to minimize the cumulative error function E_2:

$$E_2 = \frac{1}{2}\vec{e}_2^{\,2}(k) = \frac{1}{2}\left\{ i_{ds}^{s}(k) - i_{ds}^{s*}(k) \right\}^2 \tag{37.10}$$

To accelerate the convergence of the error back-propagation learning algorithm, the current weight adjustment is supplemented with a fraction of the most recent weight adjustment, as indicated in Eq. (37.11):

$$W_4(k) = W_4(k-1) + \eta_2 \Delta W_4(k) + \alpha_2 \Delta W_4(k-1) \tag{37.11}$$

where η_2 is the training coefficient and α_2 is a user-selected positive momentum constant.

Following a similar procedure, the q-axis stator current of the induction motor can be estimated using the discrete form as shown in Eq. (37.12):

$$i_{qs}^{s*}(k) = W_4 i_{qs}^{s*}(k-1) + W_5 \lambda_{qr}^{s\,im}(k-1) - \omega_r W_6 \lambda_{dr}^{s\,im}(k-1) + W_7 v_{qs}^{s}(k-1) \tag{37.12}$$

Equation (37.12) can be represented by a neural network as shown in Fig. 37.22. The weight W_4 is updated with the training based on Eq. (37.12).

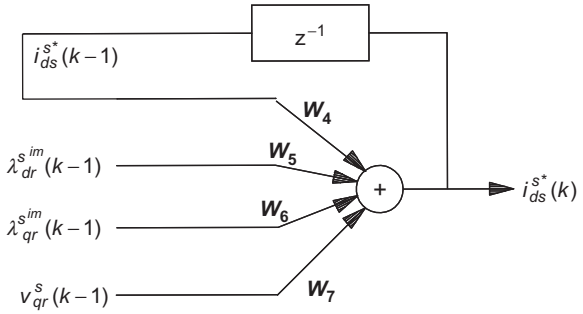


FIG. 37.21 d-Axis stator current estimation using recurrent neural network based on Eq. (37.9).

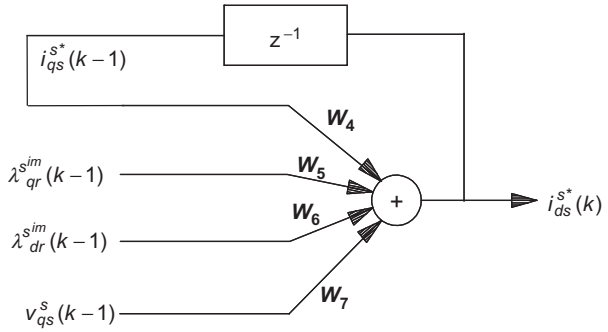


FIG. 37.22 q-Axis stator current estimation using recurrent neural network based on Eq. (37.12).

The stator resistance $\hat{R}_s$ of the induction motor can now be calculated using Eq. (37.13) as follows:

$$\hat{R}_s = \left\{1 - W_4 - \frac{T_s}{\sigma L_s}\frac{L_m^2 \hat{R}_r}{L_r^2}\right\}\frac{\sigma L_s}{T_s} \tag{37.13}$$

The stator resistance of an induction motor can be thus estimated from the stator current using the neural network system as indicated in Fig. 37.23.

37.3.4.1 Modeling Results of Stator Resistance Estimation Using ANN

The block diagram of a rotor-flux-oriented induction motor drive together with stator resistance identification is already shown in Fig. 37.14, where the stator resistance estimation is implemented by the stator resistance estimator (SRE) block.

The stator resistance estimation results are as shown in Fig. 37.24. It has three results (1) without both rotor and stator resistance estimators, (2) with only rotor resistance estimation, and (3) with both rotor and stator resistance estimations. As shown in the figure, both R_r and R_s were increased abruptly by 40% at 1.5 s. It can be seen that the estimated stator resistance $\hat{R}_s$ converges to $\hat{R}_s$ within 200 ms. It can be noted from this figure that the convergence of the stator resistance estimation is not affected by the convergence of the rotor resistance estimator.

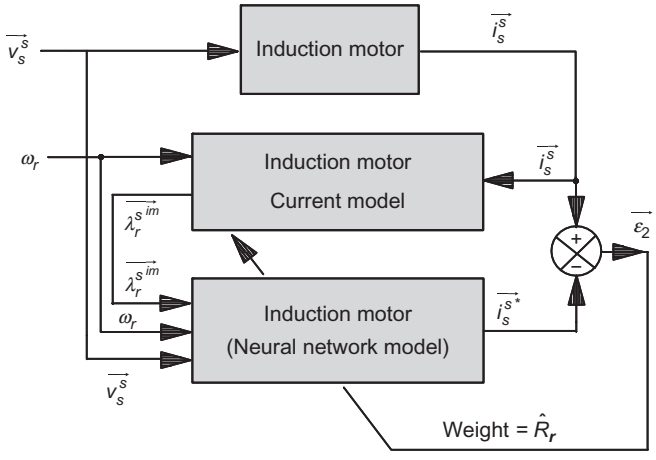


FIG. 37.23 Block diagram of R_s estimation using artificial neural network.

37.3.4.2 Experimental Results of Stator Resistance Estimation Using ANN

The stator resistance estimation algorithm was tested together with the rotor-flux-oriented induction motor drive of Fig. 37.14 implemented in the laboratory. To test the stator resistance estimation, an additional 3.4 Ω per phase was added in series with the induction motor stator, with the motor running at 1000 rev/min and with a load torque of 7.4 Nm.

The estimated stator resistance together with the actual stator resistance is shown in Fig. 37.25. The estimated stator resistance converges to 9.4 Ω within <200 ms.

Fig. 37.26 shows both the measured d-axis stator current and the one estimated by the neural network model. The neural network model output $i_{ds}^{s*}(k)$ follows the measured values $i_{ds}^{s}(k)$, due to the online training of the neural network.

37.4 ANN-Based Controls in Motor Drives

37.4.1 Induction Motor Current Control

Another application of ANN is to identify and control the stator current of an induction motor. In one study, Burton et al. have used a current control strategy outlined by Wishart and Harley to train an ANN to control the induction motor stator currents. They have used a training algorithm named random weight change (RWC) that is reported to be slightly faster than back propagation. In RWC algorithm, the weights are perturbed by a fixed step size and a random sign. This is done for fixed number of trials, and after each trial, the error with the desired output is computed. Finally, the set of weight changes that result in the least error are chosen, and the whole process is repeated until convergence is reached. The modeling results reported in this scheme was excellent. Later, Burton *et al.* presented their practical implementation of this proposed stator current controller with a transputer controller card.

37.4.2 Induction Motor Control

Narendra and Parthasarathy proposed methods for identification and control of dynamic systems using ANNs. Wishart and Harley used the above basic principles to identify and control induction machines. A block diagram of the control scheme is shown in Fig. 37.27. For the induction motor, the nonlinear autoregressive moving average with exogenous input (NARMAX) model for the stationary frame stator current is derived and used for the identification of electromagnetic model. In its

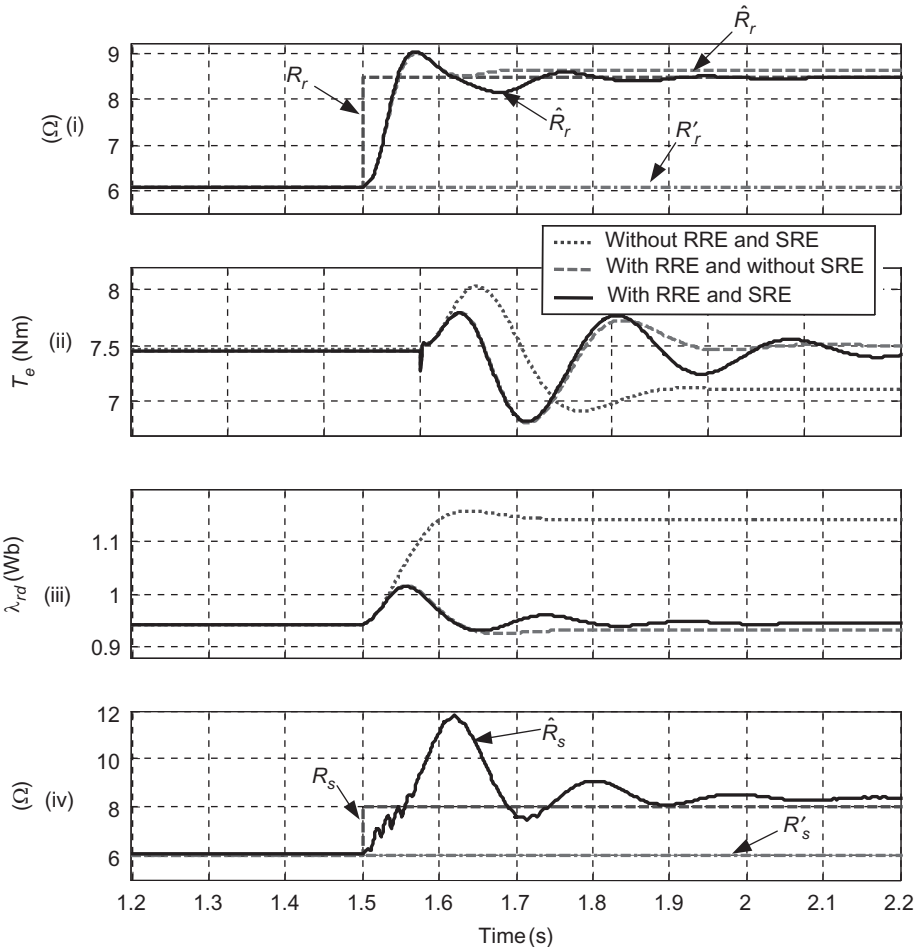


FIG. 37.24 Performance of the drive with and without RRE and SRE using ANN for 40% step change in R_r and R_s, R_r', and R_s' compensated—modeling results.

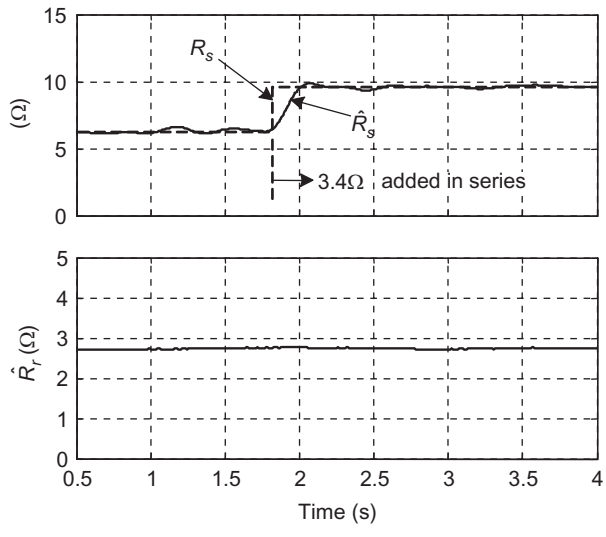


FIG. 37.25 Estimated stator resistance R_s using ANN—experimental results.

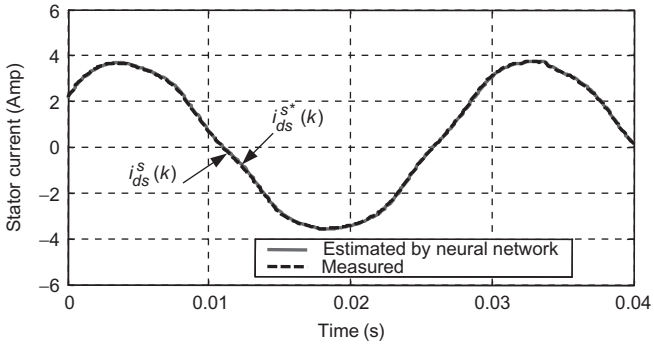


FIG. 37.26 Stator currents in R_s estimation—experimental results.

general form, the NARMAX model represents a system in terms of its delayed inputs and outputs. Random steps in the stator voltage are given for the purpose of identification. The neural network used is of the multilayer back-propagation type, and a quantity based on the rotor time constant is also

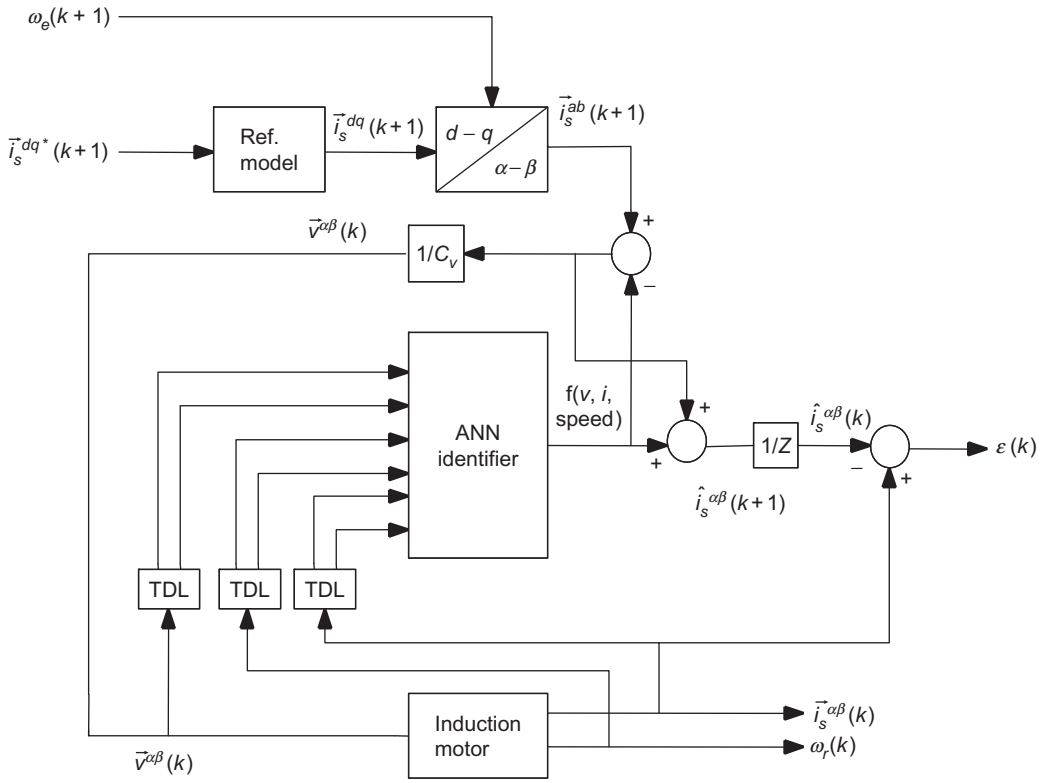


FIG. 37.27 Adaptive current control using ANN proposed by Harley.

computed as an extra weight. As opposed to the regular ANN architecture, this ANN has nonlinearity in the output layer, and the weighted sum of the inputs is used as the output. This gives an estimate of the rotor time constant and makes the system robust against variation of the parameters. Once, the identification is over, the ANN is used for current control. The stator currents predicted by the ANN are used to compute the input voltage for the induction motor, and the ANN output is made to track the reference currents by back propagating the error.

The rotor speed is also controlled in this system by identifying a NARMAX model for the speed increment rather than the absolute value of speed. To simplify the NARMAX model, the load torque is assumed to be a function of the motor speed, as is the case in a fan or pump type of load. For the current control case, the relationship between the control variable (voltage) and the controlled quantity (current) was linear. In the speed control case, this relationship is nonlinear, thus necessitating two ANNs, one for identification of speed and the other for control.

The identification ANN (N_i) predicts the value for the speed increment, which is compared with the actual speed increment, and the error (ε_i) is back propagated through the ANN. A PI controller is used for basic speed control, and the control ANN (N_c) produces the slip frequency, and the difference between the desired speed increment and actual speed increment (ε_c) is back propagated through the ANN. The induction motor drive therefore employs three ANNs as shown in Fig. 37.28.

37.4.3 Efficiency Optimization in Electric Drives

The efficiency improvement of induction motor drives via flux control can be classified into three groups: precomputed flux programs, real-time computation of losses, and online input-output efficiency optimization control. All of these methods target choosing a value of the motor excitation that optimizes the motor-converter losses. The main requirement of an input-output optimization is to achieve the flux optimization in a minimum number of search steps. A constant search step may take too long if the step is too small, or it may bypass the minimum power input if the step is too large. For each mechanical operating point of the motor, it is possible to find a combination of rotor-flux linkage and torque producing current i_q at which the dc-link power P_{dc} to the drive system is minimum.

One of the possible ANN efficiency optimizers reported is shown in Fig. 37.29. An ANN-based search algorithm is employed to operate as an efficiency optimizer. The inputs to the system are the dc power fed into the drive system at instant k and the change in the control variable at the previous instant $\Delta c(k-1)$. The only output is the actual change in control variable $\Delta c(k)$. Appropriate scaling from engineering units to the normalized interval $[-1, 1]$ are implemented by the input and output interfaces, input scaling (IS), and output scaling (OS). The speed signal is used to generate the reference flux $C(k)_0$ corresponding to each speed. The mechanical steady state is

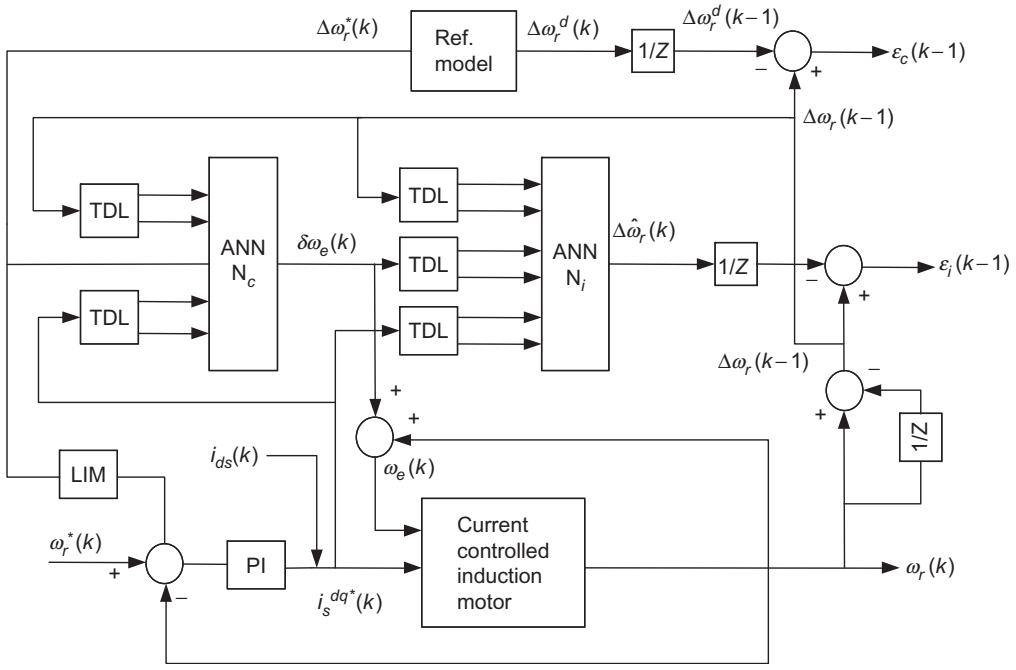


FIG. 37.28 Adaptive speed control of the induction motor using ANN.

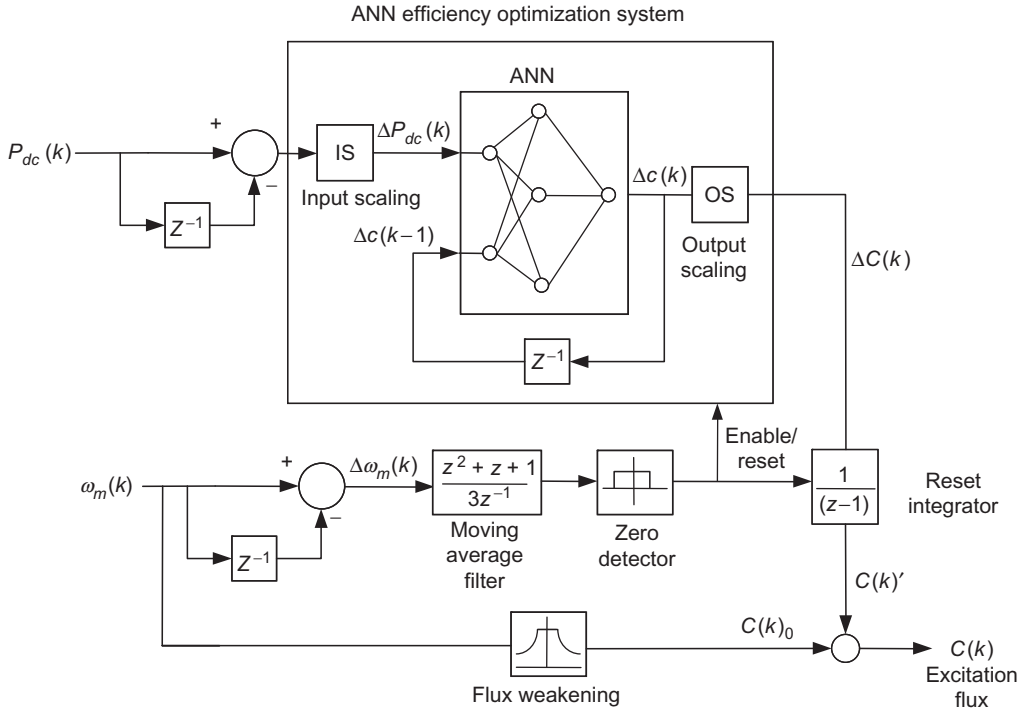


FIG. 37.29 Induction motor efficiency optimizer using ANN.

detected by applying a moving average filtering to the speed variation $\Delta\omega_m$. The ANN efficiency optimizer is enabled only during the mechanical steady state.

37.5 ANN-Based Controls in Power Converters

A feedforward ANN can implement a nonlinear input-output mapping. A feedforward carrier-based pulse-width modulation (PWM) technique, such as space-vector modulator (SVM), can be looked at as a nonlinear mapping where the command phase voltages are sampled at the input and the corresponding pulse-width patterns are established at the output. Fig. 37.30 shows the block diagram of an open-loop V/f-controlled induction motor drive incorporating the proposed ANN-based SVM controller. The command voltage $V_{qs}^*(=V^*)$ is generated from the frequency or speed command, and the angle command θ_e^* is obtained by integrating the frequency, as shown. The output of the modulator generates the PWM patterns for the inverter switches.

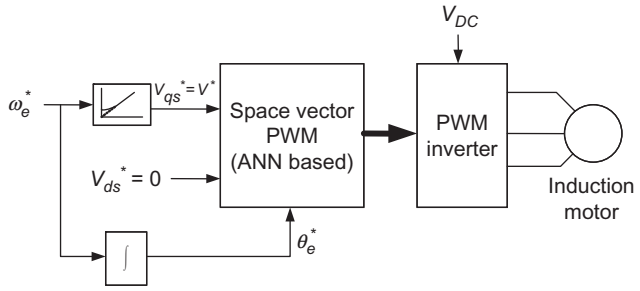


FIG. 37.30 V/f control of induction motor using ANN-based SVM.

The ANN can be conveniently trained off-line with the data generated by calculation of the SVM algorithm. The ANN has inherent learning capability that can give improved precision by interpolation unlike the standard lookup table method. Fig. 37.31 shows such an SVM that can operate during both undermodulation and overmodulation regions linearly extending smoothly up to a square wave. The SVM is implemented using two subnets: angle subnet and amplitude subnet. The subnets use a multiplayer perceptron-type network with sigmoidal-type transfer function. The bias is not shown in the figure. The composite network uses two neurons at the input, 20 neurons in the hidden layer, and four output neurons. The input signal to the angle subnet is θ_e angle that is normalized, and then pulse-width functions at unit amplitude are solved (or mapped) at the output for three phases, as indicated. The amplitude subnet implements the $f(V^*)$ function. The digital words corresponding to the turn-on time are generated by multiplying the angle subnet output with that of the amplitude subnet and then adding the $T_s/4$ bias signal, as shown. The PWM signals are then generated using a single timer. The angle subnet is trained with an angle interval of 2.16 degrees in the range of 0–360 degrees. Due to learning or interpolation

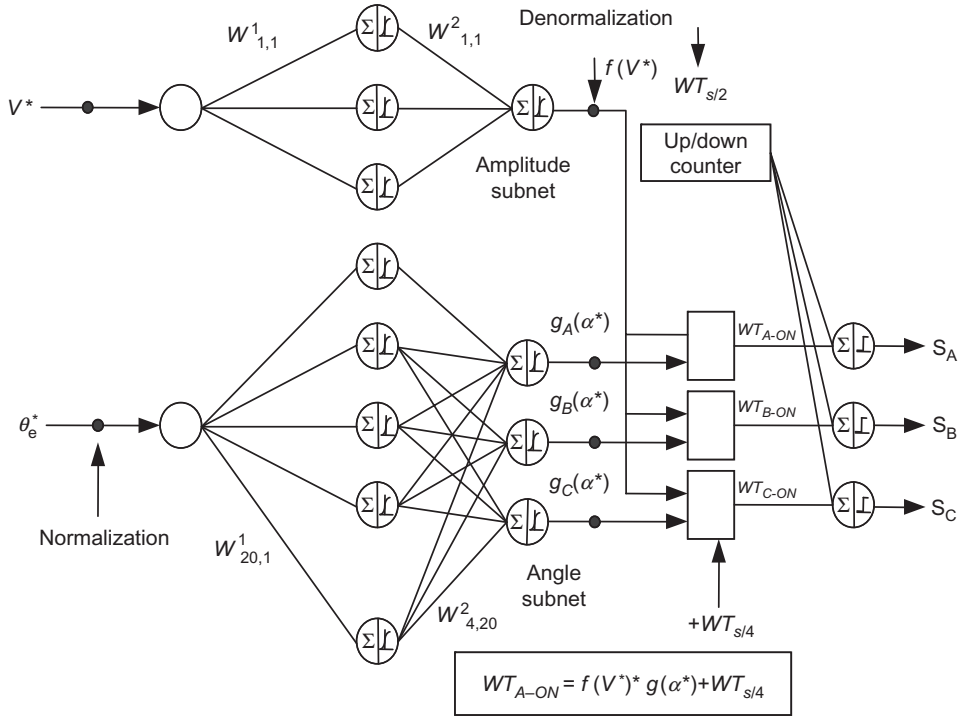


FIG. 37.31 Neural network topology $(2\times20\times4)$ for PWM wave synthesis.

capability, both the subnets will operate higher signal resolution. A sampling interval T_s of 50 µs corresponds to a switching frequency of 20 kHz and a 100 µs that corresponds to 10 kHz.

Further Reading

[1] P. Vas, Artificial Intelligence-Based Electrical Machines and Drives: Application of fuzzy, Neural, Fuzzy-Neural and Genetic-Algorithm—Based Techniques, Oxford University Press, New York, 1999.

[2] B.K. Bose, Modern Power Electronics and AC Drives, Prentice Hall, New Jersey, 2002.

[3] L. Ben-Brahim, S. Tadakuma, A. Akdag, Speed control of induction motor without rotational transducers, IEEE Trans. Ind. Appl. 35 (4) (1999) 844–850.

[4] M.G. Simoes, B.K. Bose, Neural network based estimator of feedback signals for a vector controlled induction motor drive, IEEE Trans. Ind. Appl. 31 (1995) 620–629.

[5] K. Funahashi, On the approximate realization of continuous mappings by neural networks, Neural Netw. 2 (1989) 183–192.

[6] D.T. Pham, X. Liu, Neural Networks for Identification, Prediction and Control, Springer–Verlag, New York, 1995.

[7] M. Wishart, R.G. Harley, Identification and control of induction machines using artificial neural networks, IEEE Trans. Ind. Appl. 31 (3) (1995) 612–619.

[8] K.S. Narendra, K. Parthasarathy, Identification and control of dynamic systems using neural networks, IEEE Trans. Neural Netw. 1 (1) (1990) 4–27.

[9] J.O. Pinto, B.K. Bose, L.E.B. De Silva, M.P. Kazmierkowski, A neural-network based space-vector pwm controller for voltage-fed inverter induction motor drive, IEEE Trans. Ind. Appl. 36 (6) (2000) 1628–1636.

38

Novel AI-Based Soft Computing Applications in Motor Drives

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38.1 Introduction

Solving an optimization problem is one of the common scenarios that occur in most engineering applications. Classical optimization techniques such as linear programming (LP) and nonlinear programming (NLP) are efficient approaches that can be used to solve special cases of optimization problem in power system and motor drive applications. As the complexities of the problem increase, especially with the introduction of parameter uncertainties, more complicated optimization techniques, such as stochastic programming, have to be used. However, these analytic methods are not easy to implement for most of the real-world problems. As a highly nonlinear, nonstationary motor drive system with nonlinear inertia, load, noise, and uncertainties, motor drives can have a large number of operating condition states and parameters. Implementing any of the classical analytic optimization search methods may not be feasible in most of the cases. On the other hand, GA and particle swarm optimization (PSO) search techniques can be an attractive alternative and effective solutions. GA and PSO are stochastically based search techniques that have its roots in artificial life and social psychology and in engineering and computer science. In general, there are two possible optimization techniques based on GA and PSO. These two techniques are the following:

(1) Single-objective optimization (SOO)
(2) Multiobjective optimization (MOO)

The main procedure of the SOO is based on deriving a single-objective function for the optimization search problem. The single-objective function may be combined from several objective functions using weighting factors. The objective function is optimized (either minimized or maximized) using GA or PSO to obtain a single solution. On the other hand, the main objective of the multiobjective (MO) problem is finding the set of acceptable trade-off optimal solutions. This set of

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accepted solutions is called Pareto front. These acceptable solutions give more ability to the user to make an informed decision by seeing a wide range of solutions that are optimum from an "overall" standpoint. Single-objective (SO) optimization may ignore this trade-off viewpoint. This chapter has described the basic concepts of GA and PSO and presents a review of some of the applications of GA and PSO in motor drive-based optimization problems to give the reader some insights of how GA and PSO can serve as acceptable near-optimal solutions to some of the most complicated engineering optimization problems.

38.2 Differences Between GA and PSO and Other Evolutionary Computation Techniques

A comparison between conventional optimization techniques and evolutionary algorithms (like GA and PSO) is presented in Table 38.1 [1]:

- Unlike other random search algorithms, each potential solution (called a particle) is also assigned a randomized velocity and then flown through the problem hyperspace.
- The most striking difference between the PSO and the other evolutionary soft computing algorithms is that PSO chooses the path of cooperation over competition. The other algorithms commonly use some form of decimation, survival of the fittest. In contrast, the PSO population is stable and individuals are not destroyed or created. Individuals are influenced by the best performance of their neighbors. Individuals eventually converge on optimal points in the problem domain.
- The PSO traditionally does not have any genetic operators like crossover between individuals and mutation, and other individuals never substitute particles during the run. Instead, the PSO refines its search by attracting the particles to positions with good solutions.
- Particles update themselves with the internal velocity.
- They also have memory, which is important to the algorithm.
- Compared with GA, the information sharing mechanism in PSO is significantly different. In GAs, chromosomes share information with each other. So the whole population moves like one group toward an optimal area. In PSO, only $\mathbf{g}_{\mathbf{best}}$ or $\mathbf{p}_{\mathbf{best}}$ gives out the information to others. It is a one-way information sharing mechanism. The evolution only looks for the best solution.
- Compared with the GA, the advantages of PSO are that PSO is easy to implement and there are few parameters to adjust.

38.3 Single Objective Genetic Optimization Search Algorithm (SOGA)

GAs are an evolutionary optimization approach that is an alternative to traditional optimization methods. GA is most appropriate for complex nonlinear models where location of the global optimum is a difficult task. It may be possible to use GA techniques to consider problems that may not be modeled as accurately using other approaches.

Therefore, GA appears to be a potentially useful approach. GA is particularly applicable to problems that are large, nonlinear, and possibly discrete in nature, features that traditionally add to the degree of complexity of solution. Due to the probabilistic development of the solution, GA does not guarantee optimality even when it may be reached. However, they are likely to be close to the global optimum. This probabilistic nature of the solution is also the reason they are not contained by local optima. The GA procedure is based on the Darwinian principle of survival of the fittest. An initial population is created containing a predefined number of individuals (or solutions), each represented by a genetic string (incorporating the variable information). Each individual has an associated fitness measure, typically representing an objective value. The concept that fittest (or best) individuals in a population will produce fitter offspring

TABLE 38.1 Comparison between conventional optimization procedures and evolutionary algorithms

Property	Evolutionary	Traditional
Search space	Population of potential solutions	Trajectory by a single point
Motivation	Natural selection and social adaptation	Mathematical properties (gradient, Hessian)
Applicability	Domain independent, applicable to variety of problems	Applicable to a specific problem domain
Point transition	Probabilistic	Deterministic
Prerequisites	An objective function to be optimized	Auxiliary knowledge such as gradient vectors
Initial guess	Automatically generated by the algorithm	Provided by user
Flow of control	Mostly parallel	Mostly serial
CPU time	Large	Small
Results	Global optimum more probable	Local optimum, dependent of initial guess
Advantages	Global search, parallel, speed	Convergence proof
Drawbacks	No general formal convergence proof	Locality, computational cost

is then implemented in order to reproduce the next population. Selected individuals are chosen for reproduction (or crossover) at each generation, with an appropriate mutation factor to randomly modify the genes of an individual, in order to develop the new population. The result is another set of individuals based on the original subjects leading to subsequent populations with better (min or max) individual fitness. Therefore, the algorithm identifies the individuals with the optimizing fitness values, and those with lower fitness will naturally get discarded from the population [2]. Fig. 38.1 shows the general flowchart of the GA algorithm based on total error iterative minimum search. The steps of the GA are depicted as follows:

1. **[Start]** Generate random population of *n* chromosomes (suitable solutions for the problem).
2. **[Fitness]** Evaluate the fitness *f(x)* of each chromosome *x* in the population.
3. **[New population]** Create a new population by repeating following steps until the new population is complete:
   a. **[Selection]** Select two parent chromosomes from a population according to their fitness (the better fitness, the bigger chance to be selected).
   b. **[Crossover]** With a crossover probability cross over the parents to form a new offspring (children). If no crossover was performed, offspring is an exact copy of parents.
   c. **[Mutation]** With a mutation probability, mutate new offspring at each locus (position in chromosome).
   d. **[Accepting]** Place new offspring in a new population.
4. **[Replace]** Use new generated population for a further run of algorithm.
5. **[Test]** If the end condition is satisfied, **stop**, and return the best solution in current population.
   [Loop] Go to step **2**.

GAs can be applied to many scientific, engineering problems, once solutions of a given problem can be encoded to chromosomes in GA and compare the relative performance (fitness) of solutions. An effective GA representation and meaningful fitness evaluation are the keys of the success in GA applications. The appeal of GAs comes from their simplicity and elegance as robust search algorithms and from their power to discover good solutions rapidly for difficult high-dimensional problems. The main advantage of GA is that models that cannot be developed using other solution methods without some form of approximation can be considered in an unapproximated form. The size of the model, that is, number of probabilistic variables, has a significant effect on the speed of solution; therefore, model specification can be crucial. Unlike other solution methods, integer variables are easier to accommodate in GA than continuous variables. This is due to the resulting restricted search space. Further, variable bound values can be applied to achieve similar results. GAs can be used for problem-solving and for modeling when the search space is large, complex, or poorly understood. Domain knowledge is scarce or expert knowledge is difficult to encode to narrow the search space. No mathematical analysis is available and traditional search methods fail.

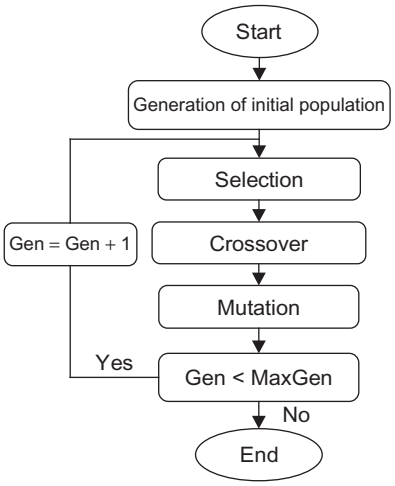


FIG. 38.1 Flowchart for the GA minimizing search algorithm.

38.4 Single Objective Particle Swarm Optimization Search Algorithm (SOPSO)

Particle swarm optimization (PSO) is an evolutionary computational technique (a search method based on a natural system), which was introduced by Kennedy and Eberhart in 1995 [3]. This optimization and search technique models the natural swarm behavior seen in many species of birds returning to roost, group of fish, and swarm of bees, etc. The particle swarm optimization (PSO) may be used to find optimal (or near-optimal) solutions to numerical and qualitative problems [4–8]. PSO methods are inspired by particles moving around in the defined search space. The individuals in a PSO have a position and a velocity. The PSO method remembers the best position found by any particle. Additionally, each particle remembers its own previously best-found position. A particle moves through the specified solution space along a trajectory defined by its velocity, the draw to return to a previous promising search area, and an attraction toward the best location discovered by its close neighbors. Particle swarm optimization has been used for a wide range of search applications and for specific optimization tasks. PSO can be easily implemented in most programming languages and has proved to be both effective and fast when applied to a diverse set of nonlinear optimization problems. PSO has been successfully applied in many areas:

- Function optimization
- Artificial neural network training
- Proportional and integral fuzzy system control
- Other near-optimal search and optimization areas where GA can be applied

38.4.1 Structure of the PSO Particle

The basic structure of any particle in a selected population consists of five components:

- $\vec{x}$ is a vector containing the current location in the solution space. The size of $\vec{x}$ is defined by the number of variables used by the problem that is being solved.
- Fitness is the quality of the solution represented by the vector $\vec{x}$, as computed by a problem-specific evaluation function.
- $\vec{V}$ is a vector containing the velocity for each dimension of $\vec{x}$. The velocity of a dimension is the step size that the corresponding $\vec{x}$ value will change into at the next iteration. Changing the $\vec{V}$ values changes the direction the particle will move through in the search space, causing the particle to make a turn. The velocity vector is used to control the range and resolution of the search.
- P_{best} is the fitness value of the best solution yet found by a particular particle.
- $\vec{P}$ is the copy of the $\vec{x}$ for the location that generated the particle's P_{best}. Jointly, P_{best} and $\vec{x}$ comprise the particle's memory, which is used to control the particle to go back toward a definite search region.
- Each particle is also aware of the current best fitness in the neighborhood for any given iteration. A neighborhood may consist of some small group of particles, in which case the neighborhoods overlap and every particle is in multiple neighborhoods. Particles in a swarm are related socially; that is, each particle is a member of one or more neighborhoods. Each individual tries to emulate the behavior of the best of its neighbors. Each individual can be thought of as moving through the feature space with a velocity vector that is influenced by its neighbors.

38.4.2 Basic Search Method

The position of each particle is represented by XY-axis position, and also, the velocity is expressed by V_{x} (the velocity of X-axis) and V_{y} (the velocity of Y-axis). Modification of the particle position is realized by the position and velocity information. Each particle knows its best value so far **($\mathbf{P_{best}}$)** and its XY position. This information represents the personal experiences of each particle. Moreover, each particle knows the best value so far in the group **($\mathbf{g_{best}}$)** among $\mathbf{P_{bests}}$. This information represents the knowledge of how the other particles around have performed. Namely, each particle tries to modify its position using the following information:

- The current positions (x, y)
- The current velocities (V_{x}, V_{y})
- The distance between the current position and $\mathbf{P_{best}}$
- The distance between the current position and $\mathbf{g_{best}}$

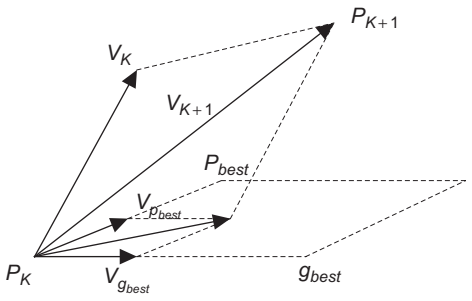


FIG. 38.2 Concept of modification of a searching point by PSO.

This modification can be represented by the concept of velocity. Velocity of each particle can be modified by the following equation:

$$V_{id} = W \times V_{id} + C_1 \times rand_1 \times (P_{id} - X_{id}) + C_2 \times rand_2 \times (P_{gd} - X_{id}) \quad (38.1)$$

where

- V_{id} is the value of dimension d in the velocity vector $\vec{v}$ for particle i.
- C_1 is the cognitive learning selected rate.
- C_2 is the social learning selected rate.
- rand_1 and rand_2 are random values on the range [0.1].
- X_{id} is the current position of particle i along dimension d.
- W is the selected weighting factor.
- P_{id} is the location along dimension d at which the particle previously had the best fitness measure.
- P_{gd} is the current location along dimension d of the neighborhood particle with the best fitness.

The basic concept of the PSO technique lies in accelerating each particle toward its $\mathbf{P_{best}}$ and $\mathbf{g_{best}}$ locations, with a random weighted acceleration at each step, and this is illustrated in Fig. 38.2.
where

P_K is the current position of a particle.
P_{K+1} is its modified position.
V_K is its initial velocity.
V_{K+1} is its modified velocity.
$V_{\text{p}_{\text{best}}}$ is the velocity considering its p_{best} location.
$V_{\text{g}_{\text{best}}}$ is the velocity considering its g_{best} location.

Using the above concept, a certain velocity, which gradually gets close to $\mathbf{P_{best}}$ and $\mathbf{g_{best}}$, can be calculated. The current position (searching point in the solution space) can be modified by the following equation:

$$X_{id} = X_{id} + V_{id} \quad (38.2)$$

38.4.3 PSO Search Algorithm

Fig. 38.3 shows the general flowchart of the PSO algorithm. The main steps in the particle swarm optimization process are described as follows:

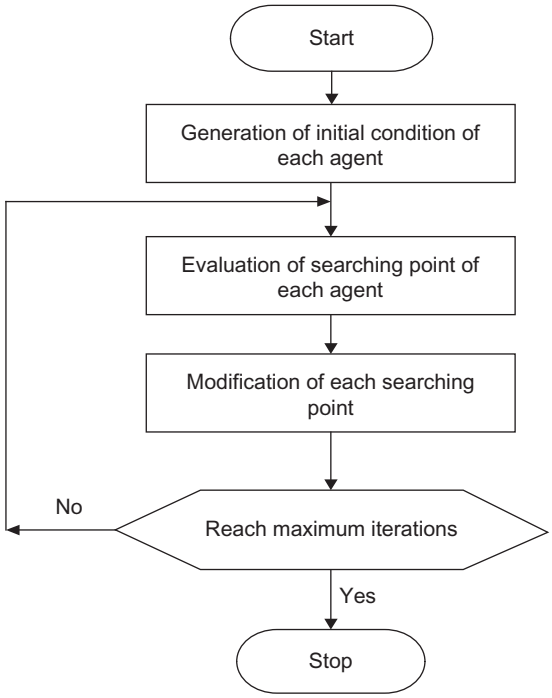


FIG. 38.3 The general flowchart of PSO search algorithm.

1. System initialized with a population of random potential solutions. Each potential solution is assigned a random "velocity" and is called a particle. (It has position in the space, i.e., it is a point in the solution space and it has velocity.) These particles are then "flown" through the search space of potential solutions.
2. Evaluate the fitness of each particle in the swarm.
3. For every iteration, compare each particle's fitness with its previous best fitness (P_{best}) obtained. If the current value is better than P_{best}, then set P_{best} equal to the current value and the P_{best} location equal to the current location in the d-dimensional space.
4. Compare P_{best} of particles with each other and update the swarm global best location with the greatest fitness (g_{best}).
5. The velocity of each particle is changed (accelerated) toward its P_{best} and g_{best}. This acceleration is weighted by a random term. A new position in the solution space is calculated for each particle by adding the new velocity value to each component of the particle's position vector.
6. Repeat steps (2)–(5) until convergence is reached based on some desired single- or multiple-objective criteria.

38.5 Multiobjective Optimization (MOO)

In many real-life applications, multiple and often conflicting objectives need to be satisfied. Satisfying these conflicting objective functions is called multiobjective optimization (MO). For example, to place more functional blocks on a chip while minimizing that chip's area and/or power dissipation is a conflicting objective that needs performing a trade-off analysis [9,10]. The objective of MO optimization is to find a set of acceptable solutions and present them to the user, who will then choose from them. Generally, there are two general approaches to solve multiobjective optimization. The first approach lies in combining the individual objective functions into a single composite function. Determination of a single objective is possible with methods, such as the weighted sum method, but the problem lies in the correct selection of the weights. In practice, it can be very difficult to accurately select these weights, even for someone very familiar with the problem domain. In addition, optimizing a particular solution with respect to a single objective can result in unacceptable results with respect to the other objectives [11,12]. The second general approach is to obtain the optimal solution. There will be a set of optimal trade-offs between the conflicting objectives, but this optimal solution is called Pareto-optimal solution set or Pareto front [13,14]. A Pareto-optimal set is a set of solutions that are nondominated with respect to one another. While moving from one Pareto solution to another, there is always a certain amount of importance in one objective to achieve a certain amount of gain in the other. Generating the Pareto set has several advantages. The Pareto set allows the user to make an informed decision by seeing a wide range of options. The Pareto set contains the solutions that are optimum from an "overall" standpoint. SO optimization may ignore this trade-off viewpoint. This feature is useful since it provides better understanding of this system in which all the consequences of a decision with respect to all the objectives can be explored [9].

The following definitions are used in the proposed multiobjective optimization (MO) search algorithm:

Definition 1 The general MO problem requiring the optimization of N objectives may be formulated as follows:

Minimize

$$\vec{y}=\vec{F}\left(\vec{x}\right)=\left[\vec{f}_1\left(\vec{x}\right),\vec{f}_2\left(\vec{x}\right),\vec{f}_3\left(\vec{x}\right),\ldots,\vec{f}_N\left(\vec{x}\right)\right]^T \quad (38.3)$$

$$\text{subject to } g_j\left(\vec{x}\right)\le 0 \quad j=1,2,\ldots,M \quad (38.4)$$

where

$$\vec{x}^*=\left[\vec{x}_1^*,\vec{x}_2^*,\ldots,\vec{x}_P^*\right]^T\in\Omega \quad (38.5)$$

$\vec{y}$ is the objective vector, the $\vec{g}_i\left(\vec{x}\right)$ represent the constraints, and $\vec{x}^*$ is a P-dimensional vector representing the decision variables within a parameter space Ω. The space spanned by the objective vectors is called the objective space. The subspace of the objective vectors satisfying the constraints is called the feasible space.

Definition 2 A decision vector $\vec{x}_1 \in \Omega$ is said to dominate the decision vector $\vec{x}_2 \in \Omega$ (denoted by $\vec{x}_1 \prec \vec{x}_1$), if the decision vector $\vec{x}_1$ is not worse than $\vec{x}_2$in all objectives and strictly better than $\vec{x}_2$ in at least one objective.

Definition 3 A decision vector $\vec{x}_1 \in \Omega$ is called Pareto-optimal, if there does not exist another $\vec{x}_2 \in \Omega$ that dominates it. An objective vector is called Pareto-optimal, if the corresponding decision vector is Pareto-optimal.

Definition 4 The nondominated set of the entire feasible search space Ω is the Pareto-optimal set. The Pareto-optimal set in the objective space is called Pareto-optimal front.

38.6 Multiobjective Genetic Optimization Search Algorithm (MOGA)

The nondominated sorting genetic algorithm (NSGA) is a multiobjective GA that was developed by Deb et al. [15]. This algorithm has been chosen over a conventional GA for three principal reasons: (a) no need to specify a sharing parameter, (b) a strong tendency to find a diverse set of solutions along the Pareto-optimal front, and (c) the ability to specify multiple objectives without the need to combine them using a weighted sum. The basic idea behind NSGA is the ranking process executed before the selection operation, as shown in Fig. 38.4. This process identifies nondominated solutions in the population, at each generation, to form nondominated fronts [16]; after this, the selection, crossover, and mutation usual operators are performed. In the ranking procedure, the nondominated individuals in the current population are first identified. Then, these individuals are assumed to constitute the first nondominated front with a large dummy fitness value [16]. The same fitness value is assigned to all of them. In order to maintain diversity in the population, a sharing method is then applied. Afterward, the individuals of the first front are ignored temporarily, and the rest of population is processed in the same way to identify individuals for the second nondominated front. A dummy fitness value that is kept smaller than the minimum shared dummy fitness of the previous front is assigned to all individuals belonging to the new front. This process continues until the whole population is classified into nondominated fronts. Since the nondominated fronts are defined, the population is then reproduced according to the dummy fitness values.

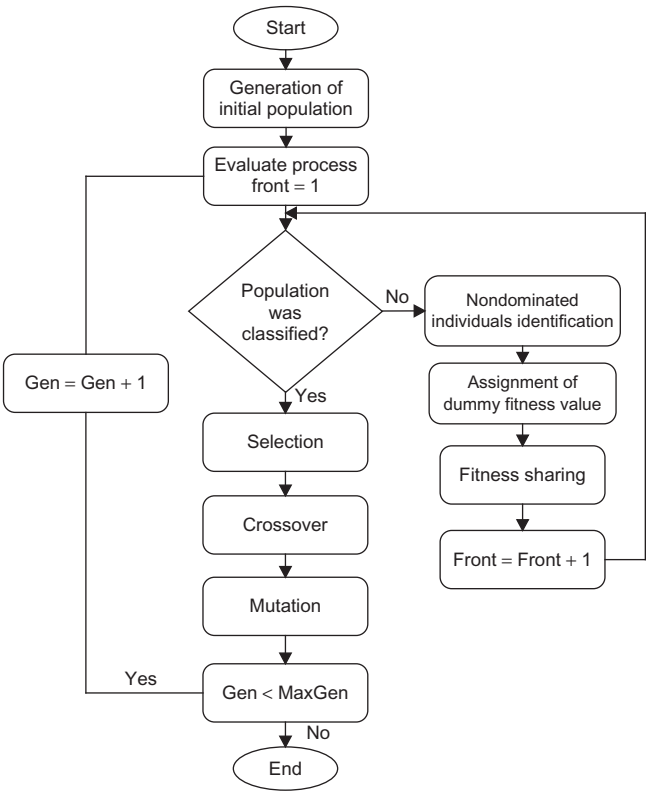


FIG. 38.4 Flowchart of NSGA.

38.7 Multiobjective Particle Swarm Optimization Search Algorithm (MOPSO)

In MOPSO [9–14], a set of particles are initialized in the decision space at random. For each particle i, a position x_i in the decision space and a velocity v_i are assigned. The particles change their positions and move toward the so-far best-found solutions. The nondominated solutions from the last generations are kept in the archive. The archive is an external population, in which the so-far found nondominated solutions are kept. Moving toward the optima (maximum or minimum) is done in the calculations of the velocities as follows:

$$V_{id} = \omega \times V_{id} + C_1 \times rand_1 \times \left(P_{pd} - X_{id}\right) + C_2 \times rand_2 \times \left(P_{rd} - X_{id}\right) \tag{38.6}$$

$$X_{id} = X_{id} + V_{id} \tag{38.7}$$

where $P_{r,d}$, $P_{p,d}$ are randomly chosen from a single global Pareto archive, ω is the inertia factor influencing the local and global abilities of the algorithm, $V_{i,d}$ is the velocity of the particle i in the d-th dimension, and c_1 and c_2 are weights affecting the cognitive and social factors, respectively. r_1 and r_2 are two uniform random functions in the range [0, 1]. According to Eq. (38.7), each particle has to change its position $\mathbf{X_{i,d}}$ toward the position of the two guides $\mathbf{P_{r,d}}$, $\mathbf{P_{p,d}}$ that must be selected from the updated set of nondominated solutions stored in the archive. The particles change their positions during generations until a termination criterion is met. Finding a relatively large set of Pareto-optimal trade-off solutions is possible by running the MOPSO for many generations. Fig. 38.5 shows the flowchart of

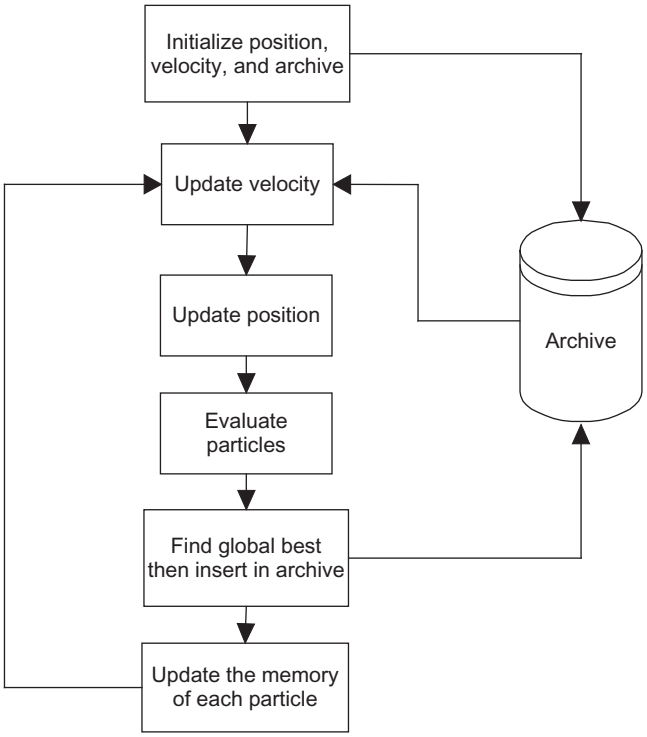


FIG. 38.5 Flowchart of the MOPSO algorithm.

the multiobjective particle swarm optimization (MOPSO). Also, Fig. 38.6 explains the procedure of the multiobjective particle swarm optimization (MOPSO) using pseudocode.

Init Pop(); The particle swarm is initialized with random values corresponding to the ranges of the decision variables. These values are dependent on the test functions.

Init Velocity(); The velocities are initialized with zero values.

Check the feasibility of each particle. If the particle does not satisfy the constraints, then regenerate it.

Evaluate Pop(); The swarm is evaluated using the corresponding objective functions.

Update Fbest(); The fitness vectors are updated (evaluate the multiobjective fitness value of each particle and save it in vector form). As we are dealing with multiobjective optimization, these vectors store the values of each decision variable, whereby the particles obtain the best values in a Pareto sense.

At this stage of the algorithm, these vectors are filled with the results of the initial particle evaluations.

Update Pbest(); Analogously, these values are copied in the pbest vectors.

Insert nodom(); Calculate the multiobjective fitness values of each particle and check its Pareto optimality. Store the nondominated particles in the Pareto archive. If the specific constraint does not exist for the archive, the size of the archive will be unlimited (all nondominated particles are inserted in the grid, i.e., in the external file).

Gbestpos = rnd (0,nodomfileSize); The global gbest particle is randomly selected.

//The flight cycle starts here //

```
1.  MOPSO
2.  {
3.          Init _Pop();
4.          Init _Velocity();
5.          Evaluate_ Pop();
6.          Update_ Fbest();
7.          Update_ Pbest();
8.          Insert_ nodom();
9.          Gbestpos = rnd(0,nodomfileSize)
10.         for (i = 1 to MAXCYCLES)
11.         {
12.             for (j = 0 to MAXPARTICLES)
13.             {
14.                 Update_Velocity();
15.                 Update_Particle();
16.             }
17.             Keeping();
18.             Evaluate_ Pop();
19.             Update_ Fbest();
20.             Update _Pbest();
21.             Insert_ nodom();
22.             Gbestpos = rnd(0,nodomfileSize)
23.         }
24.         Print Statistics();
25.         Generate Outfile();
26. }
```

FIG. 38.6 Pseudocode of the MOPSO.

Update Velocity(); The velocity of each particle is updated, using Eq. (38.6). Two Pareto solutions are chosen randomly for $P_{r,d}$, $P_{i,d}$ from the Pareto archive.

Update Particle(); The position of each particle is also updated using Eq. (38.7).

Keeping(); The keeping operation is carried out to maintain the particles into the allowable range values. Then, the particles are mutated. If the particle does not remain within the feasible solution region, it is discarded and mutated again.

Evaluate Pop(); Update Fbest(); Update Pbest();

The particles are evaluated; the fitness and pbest vector are, if appropriate, updated.

Insert nodom(); As the particles move in the search space because they have changed positions, the dominance of each particle is verified, and, if appropriate, they are inserted in the grid.

(a) Check the Pareto optimality of each particle. If the fitness value of the particle is nondominated when compared with the Pareto-optimal set in the archive, save it into the Pareto archive.

(b) In the Pareto archive, if a particle is dominated by a new one, then discard it.

Gbestpos = rnd(0,nodomfileSize); Then, the new gbest is randomly selected. Two Pareto solutions are chosen randomly for $p_{p;d}$ and $p_{r;d}$ from the Pareto archive.

Repeat the cycle until the number of generations reaches a given n.

// the end of the cycles //

Print Statistics(); Generate Outfile(); Print the statistics and generate an output file, which contains the nondominated particles.

38.8 GA and PSO Applications in Speed Control of Motor Drives

Many areas in power systems require solving one or more nonlinear optimization problems. While analytic methods might suffer from slow convergence and the problem of dimensionality, GA and PSO are known to effectively solve large-scale nonlinear optimization problems [17]. This section provides some motor drives applications that have benefited from the powerful nature of GA and PSO as an optimization techniques. For each application, technical details that are required for applying GA and PSO and the most efficient fitness functions are also discussed. In this section, online energy optimization controllers are proposed for induction motor drives and PMDC motor drives using GA and PSO. In many applications, efficiency optimization of induction motors and PMDC motors represents an important factor of control especially for autonomous electric traction. This section will present some of the applications of GA and PSO in motor drive-based optimization problems to give some insight of how GA and PSO can serve as a solution to some of the most complicated engineering optimization problems [18–43].

38.8.1 Efficient Operation of Induction Motor Drives [18]

Induction motor is a high-efficiency electrical machine when working close to its rated torque and speed. However, at light loads, no balance in between copper and iron losses results considerable reduction in the efficiency. The part load efficiency and power factor can be improved by making the motor excitation adjustment in accordance with load and speed. To implement the above goal, the induction motor should either be fed through an inverter or redesigned with optimization algorithms [19]. This application presents an optimization technique for an efficient controller for the three-phase induction motors. Multiobjective particle swarm optimization (MOPSO) technique is implemented to tackle all the conflicting goals that define the search for the optimality problem. The PSO search deals with two main conflicting objective functions. These conflicting functions are maximizing the operating efficiency of the drive system for a given mechanical load and maximizing the equivalent power factor of the induction motor for start-up and steady-state operations. In addition, the optimization ensures that maximum allowable stator current constraints are not exceeded. The proposed technique are based on the principle that the flux level in a machine can be adjusted to give the required trade-off solution of maximum efficiency and maximum power factor for a given value of speed and load torque. The optimum flux levels are function of the machine load and speed requirements. Simulation results show that considerable efficiency and power factor improvements are achieved using MOPSO when compared with the field-oriented control (FOC) and constant voltage-to-frequency ratio-based control (CVFRC).

For optimal operation, three key objective functions that can affect the motor operation had been chosen. These three objective functions are based on motor efficiency, motor power factor, and motor stator current:

1. Efficiency (to maximize)
2. Power factor (to maximize)
3. Stator current (to minimize)

In addition, the optimization search ensures that all maximum stator current and inrush constraints are not exceeded. Fig. 38.7 is a plot of input power versus stator current. As illustrated in this figure, the stator current and the input power are minimized almost simultaneously. Therefore, in practice, the maximum efficiency (ME) and the minimum stator current (MSC) are not conflicting objective functions. So, when the efficiency is maximized, the stator current is minimized and the torque per ampere is maximized. So, the maximum efficiency and power factor will be considered as the main conflicting objective functions. However, a good operation should represent the right compromise among different objectives, but the problem consists in searching this "compromise." The best tool to optimally solve this problem is represented by the multiobjective approach. This approach allows us to investigate how each single-objective and multiobjective problem affects the

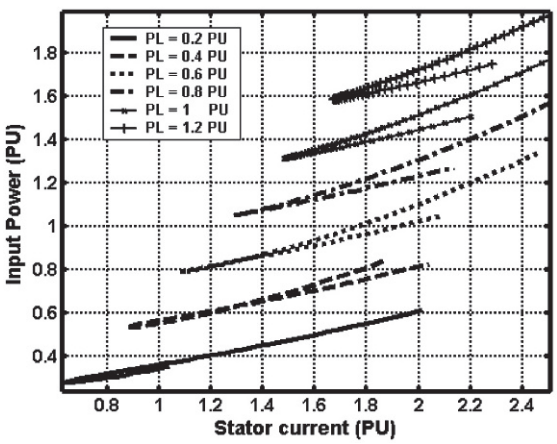


FIG. 38.7 Input power versus stator current at rated speed and various load powers.

results in terms of performance and independent variables and, above all, allows us to have a wide range of alternative solutions among which the operator can choose a better solution. The MOGA and MOPSO algorithms have been applied to optimize the operation of a three-phase, 380 V, 1 hp, 50 Hz, four-pole, squirrel cage induction motor. The block diagram of the optimization process based on PSO is shown in Fig. 38.8. In the proposed controller, the PSO algorithm receives the rotor speed and load torque, and then, the PSO controller determines the slip frequency at which the optimal fitness function occurs at that rotor speed and load torque. As stated before, this part of simulation will consider the maximum efficiency and the maximum power factor (ME and MPF) problem to be solved using multiobjective particle swarm optimization. Fig. 38.9 shows the solution to this problem and shows the Pareto fronts of the problem for different levels of rotor speed $\omega_r = 0.2$, 0.4, 0.8, 1 pu and different levels of load torque $T_L = 0.2$ and 1 pu. Tables 38.2 and 38.3 show the solution limits of the efficiency and the power factor for each operating point using MOGA and MOPSO. This range of solutions that is called the Pareto front enables the operator to choose the best compromise solution. Fig. 38.10 shows the comparison between the constant voltage-to-frequency ratio strategy (CVFRS), the field-oriented control strategy (FOCS), and the available solutions from MOPSO at different levels of load torque and rotor speed $\omega_r = 0.2$ and 1 pu, respectively. The solution that has maximum efficiency is selected from the Pareto front to achieve this comparison. Keep in mind that the operator can choose the compromised solution from the Pareto front depending on the desired efficiency and power factor. It is obvious from Fig. 38.7 that the stator current is minimized using MOPSO. In addition, there is a great improvement in efficiency and power factor using MOPSO when compared with other strategies especially at light loads. It is noted that there is a very poor PF obtained using conventional methods (field-oriented control strategy and constant voltage-to-frequency ratio) especially at light loads. It is obvious from Fig. 38.9 that the efficiency improvement has a noticeable value especially at light loads and rotor speed $\omega_r = 0.2$ pu that can be as high as 80% using CVFRS. This difference decreases to 65% at rotor speed $\omega_r = 1$ pu. On the other hand, the power factor improvement reaches 55% at light load and rotor speed $\omega_r = 0.2$ pu, whereas this improvement reaches to 160% at rotor speed $\omega_r = 1$ pu and light load. The performance difference between the field-oriented control (FOC) and the proposed control strategies MOPSO comes from the chosen value of the slip frequency and the air gap flux for each strategy. For example, at loading condition of rotor speed equal to 0.2 pu and load torques varying from 0.2 to 1 pu, the values of slip frequency based on FOCS vary from 0.01 to 0.042 pu. On the other hand, the values of slip frequency based on MOPSO vary from0.0301 to 0.0524 PU. This difference in slip frequency and air gap flux causes the difference in performance of each control strategy. The difference in the flux level of the (FOCS) controller comes from the choice of the level of the magnetization current command. The command of magnetization current is set to a constant value, which produces rated torque at rated stator flux. At light loads, the constant chosen value of magnetization current fails to choose the optimal flux level. On the other hand, this value yields the optimal flux level at rated loads. The proposed strategies overcome this problem and successfully choosing the optimal flux level especially at light loads.

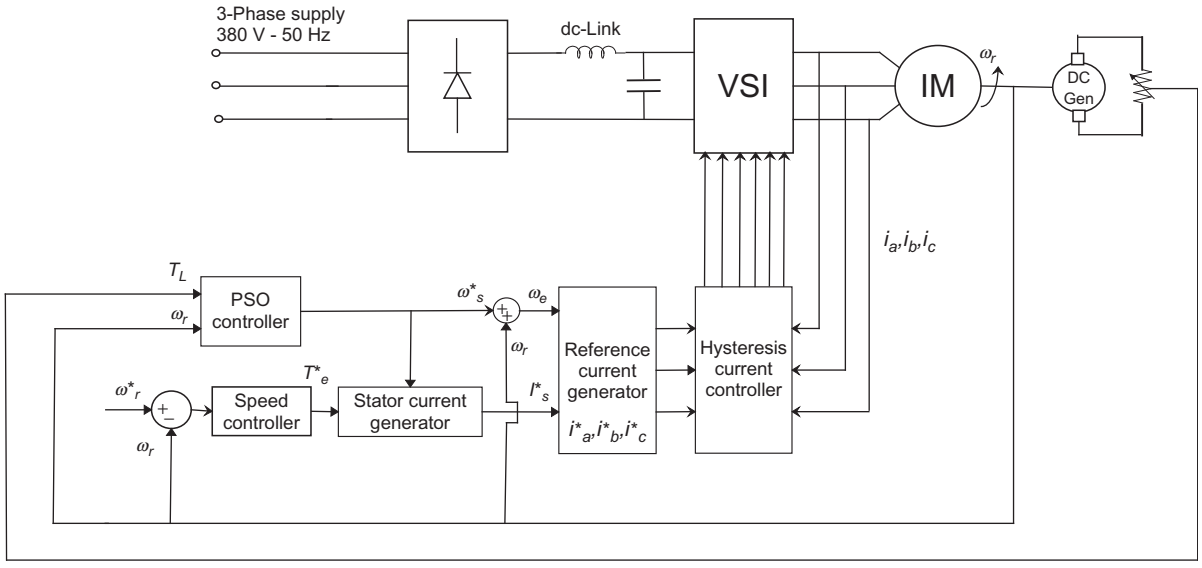


FIG. 38.8 The proposed drive system using PSO based on the loss model controller.

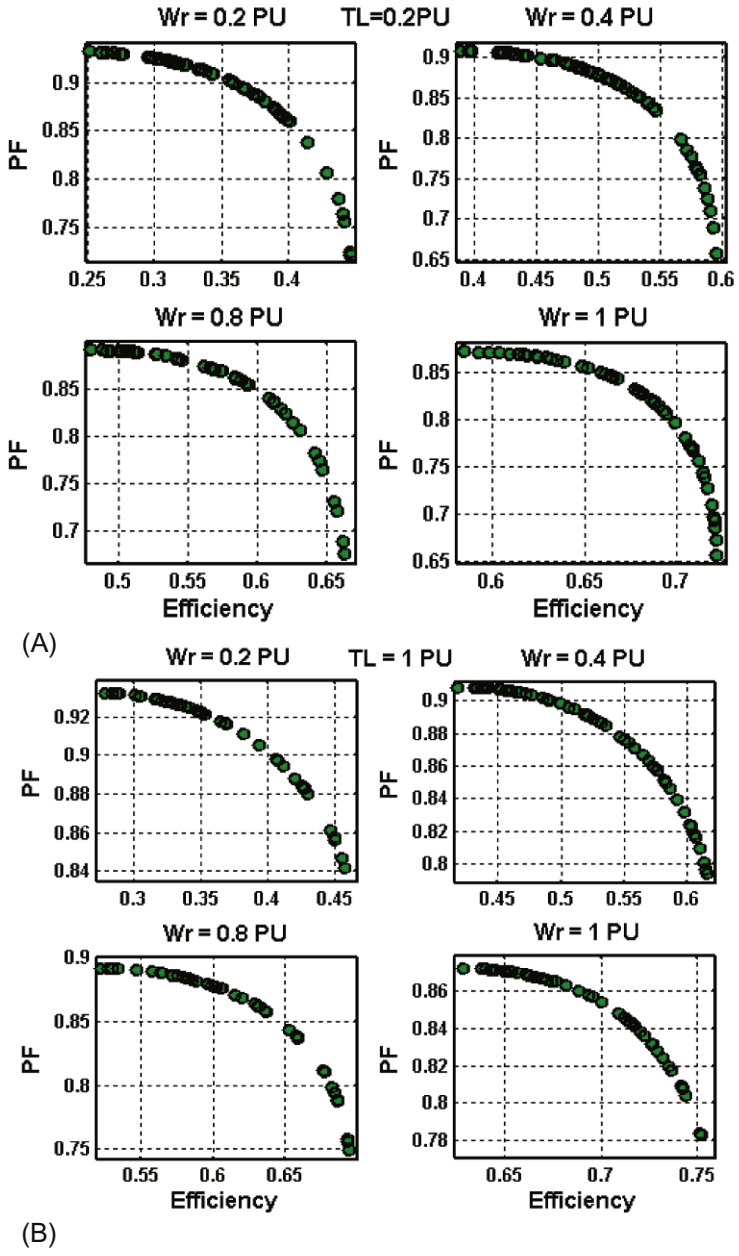


FIG. 38.9 Pareto front of ME and MPF problem for different levels of rotor speed $\omega_r = 0.2$, 0.4, 0.8, 1 pu and different levels of load torque: (A) $T_L = 0.2$ pu and (B) $T_L = 1$ pu.

38.8.2 A Novel Self Regulating Hybrid (PV-FC-Diesel-Battery) Electric Vehicle-EV Drive System [20]

This application presents a number of novel self-regulating triloop error-driven controllers for a hybrid PV-FC-diesel-battery-powered all-wheel drive electric vehicle using four-wheel permanent magnet DC (PMDC) motors, which are modeled to include existing nonlinearities in motor plus load inertia (J) and viscous friction (B). A triloop dynamic error-driven scheme is proposed to regulate motor speed and current and avoid motor overloading/inrush conditions, in addition to motor speed dynamic reference tracking. The proposed triloop dynamic error-driven self-tuned control schemes are utilized to ensure dynamic energy efficiency, control loop decoupling, and grid interface stability while maintaining reference speed tracking capability. The integrated motor drive scheme is fully stabilized using novel FACTS-based green filter compensators that ensure stabilized DC bus voltage, minimal inrush current conditions, and damped load excursions. This application presents a novel comparison of multiobjective particle swarm optimization (MOPSO) and genetic search algorithms MOGA optimization and search

TABLE 38.2 The limits pf the Pareto front of the two conflicting objective functions using MOGA

	Efficiency		Power factor	
T_L (pu)	Minimum	Maximum	Maximum	Minimum
(A)				
$\omega_r = 0.2$ pu				
0.2	0.2554	0.4665	0.9284	0.6650
0.4	0.2486	0.4544	0.9318	0.7091
0.6	0.2521	0.4371	0.9344	0.7780
0.8	0.2510	0.4688	0.9308	0.6578
1	0.2549	0.4539	0.9198	0.6771
(B)				
$\omega_r = 0.4$ pu				
0.2	0.3571	0.5883	0.9010	0.6860
0.4	0.3934	0.6012	0.8862	0.7068
0.6	0.3784	0.5915	0.8963	0.6786
0.8	0.4025	0.5818	0.8871	0.6662
1	0.3794	0.5960	0.9008	0.6547
(C)				
$\omega_r = 0.6$ pu				
0.2	0.4979	0.6859	0.8893	0.7015
0.4	0.4989	0.7099	0.8830	0.6641
0.6	0.5076	0.7053	0.8820	0.7114
0.8	0.5072	0.6948	0.8830	0.6872
1	0.4917	0.7051	0.8868	0.6695
(D)				
$\omega_r = 0.8$ pu				
0.2	0.5301	0.7298	0.8753	0.6707
0.4	0.5270	0.7346	0.8744	0.6340
0.6	0.5251	0.7218	0.8738	0.6520
0.8	0.5299	0.7324	0.8722	0.6127
1	0.5285	0.7115	0.8781	0.7025
(E)				
$\omega_r = 1$ pu				
0.2	0.5964	0.7170	0.8603	0.6899
0.4	0.5937	0.7337	0.8636	0.7032
0.6	0.5952	0.7423	0.8712	0.6599
0.8	0.5921	0.7314	0.8693	0.6919
1	0.5938	0.7366	0.8651	0.6593

TABLE 38.3 The limits pf the Pareto front of the two conflicting objective functions using MOPSO

	Efficiency		Power factor	
T_L (pu)	Minimum	Maximum	Maximum	Minimum
(A)				
$\omega_r = 0.2$ pu				
0.2	0.2521	0.4463	0.9323	0.6806
0.4	0.2647	0.4768	0.9323	0.7184
0.6	0.2742	0.4792	0.9323	0.7705
0.8	0.2702	0.4725	0.9323	0.7741
1	0.278	0.4636	0.9323	0.8165
(B)				
$\omega_r = 0.4$ pu				
0.2	0.3894	0.5957	0.9082	0.6328
0.4	0.4021	.6257	0.9082	0.6647
0.6	0.4154	0.6309	0.9082	0.7033
0.8	0.4335	0.6271	0.9079	0.7271
1	0.4182	0.6195	0.9082	0.7532
(C)				
$\omega_r = 0.6$ pu				
0.2	0.4804	0.6649	0.892	0.6342
0.4	0.4984	0.6937	0.892	0.6375
0.6	0.5132	0.7005	0.892	0.6701
0.8	0.5183	0.699	0.892	0.7224
1	0.523	0.6943	0.892	0.736
(D)				
$\omega_r = 0.8$ pu				
0.2	0.5475	0.7013	0.8806	0.6221
0.4	0.5681	0.7295	0.8806	0.6676
0.6	0.5808	0.7377	0.8805	0.6542
0.8	0.5793	0.7385	0.8806	0.7124
1	0.5776	0.7353	0.8805	0.7165
(E)				
$\omega_r = 1$ pu				
0.2	0.5846	0.7217	0.8722	0.6563
0.4	0.6093	0.7506	0.8722	0.6529
0.6	0.6221	0.7597	0.8722	0.6853
0.8	0.6277	0.7617	0.8722	0.6928
1	0.6283	0.7603	0.8722	0.7257

techniques for online dynamic tuning of the different controllers under varying renewable source conditions and load excursions.

The pressing need to utilize all abundant renewable green energy sources (wind, solar, PV, wave, tidal, fuel cell, biogas, and hybrid) is currently motivated by economic and environmental concerns. The increasing reliance on costly fossil fuels with increasing rate of resource depletion is causing a shift to energy alternatives, clean fuel replacement, and energy displacement of conventional sources to new green renewable, environmentally safe, and friendly counterparts [21,22]. Electric vehicle is one of the solutions for the reduction of the fossil fuel consumption and pollutant emissions of gas, responsible for the greenhouse effect. However, pure battery electric vehicles have shown their own range limitations; because of their size, the vehicle habitability is reduced so as its range. Adding different kinds of power supply in the same vehicle allow taking advantages from their different characteristics [23]. Several types of electric motors may be used for EV propulsion purposes. Earlier traction motors were exclusively dc motors, either series excited or separately excited. Recently, more advanced ac drive systems have found application in EV propulsion using induction motors, permanent magnet synchronous motors, and permanent magnet brushless dc motors [24,25]. The EV-DC motor speed or position control has been realized including conventional PI, PID, fuzzy logic based, nonlinear, adaptive variable structure, model reference adaptive control, artificial neural networks, and feedforward computed torque control strategies [26–28]. The need for an online gains adaptation or a "tunable" control mechanism is highly stressed in the control of any nonlinear systems with unmodeled dynamics. The PSO- and GA-based self-regulating algorithms are utilized to track any reference speed trajectory

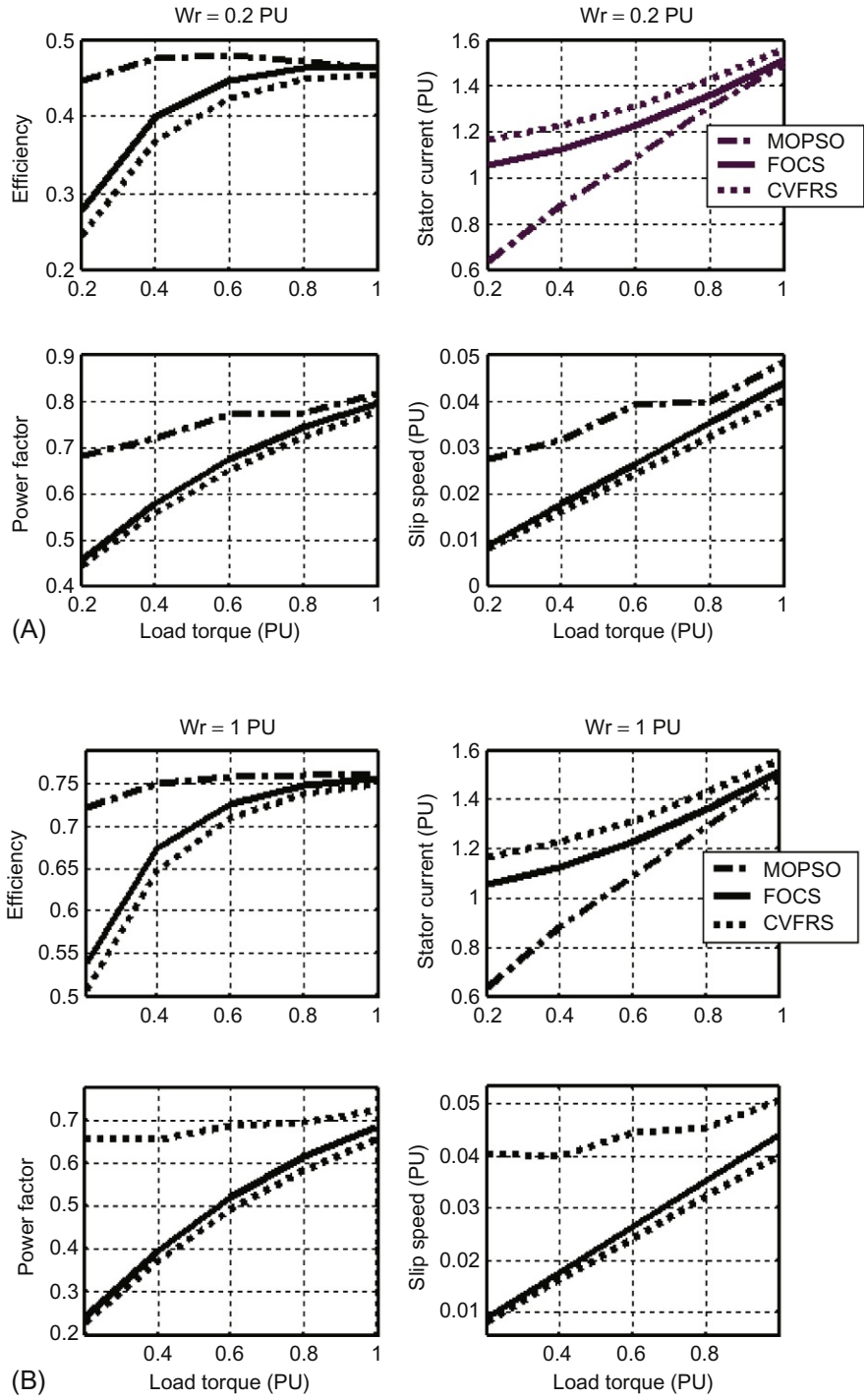


FIG. 38.10 The comparison between CVFRS, FOCS, and MOPSO for different levels of load torque T_L and different levels of rotor speed: (A) $\omega_r = 0.2$ pu and (B) $\omega_r = 1$ pu.

under varying parameter and load conditions. The control system comprises four different controllers used to track speed reference trajectory depicting the motor with minimum over-current, inrush, and ripple conditions. The proposed novel control scheme has been validated for effective dynamic speed reference trajectory tracking and enhanced power utilization.

38.8.2.1 Sample Study AC-DC System

Figs. 38.11 and 38.12 show the proposed the four-wheel electric vehicle drive system scheme with the PV, FC sources, the diesel generator, and the backup battery. The DC compensator scheme developed by the first author is used to ensure stable, efficient, and minimal inrush operation of the hybrid renewable energy

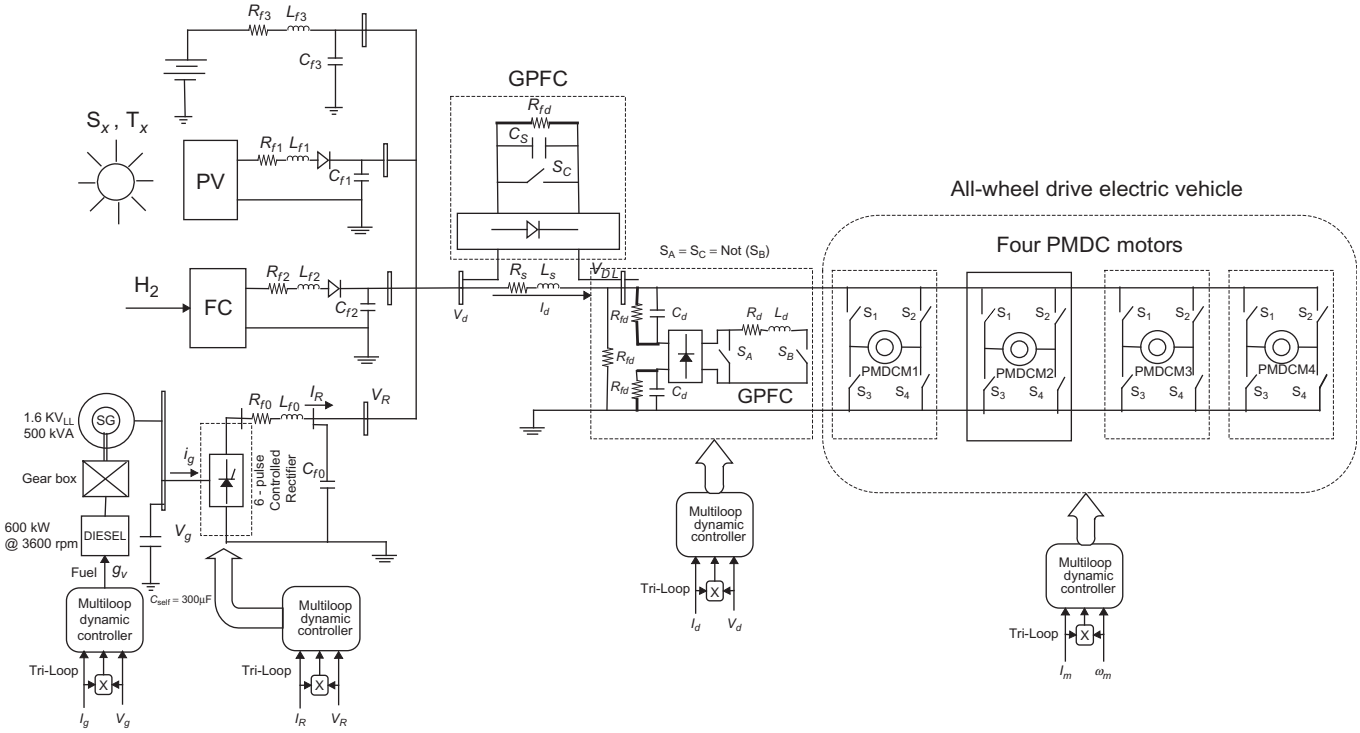


FIG. 38.11 The proposed all-wheel electric vehicle drive system with PV-FC-diesel-battery AC/DC generation.

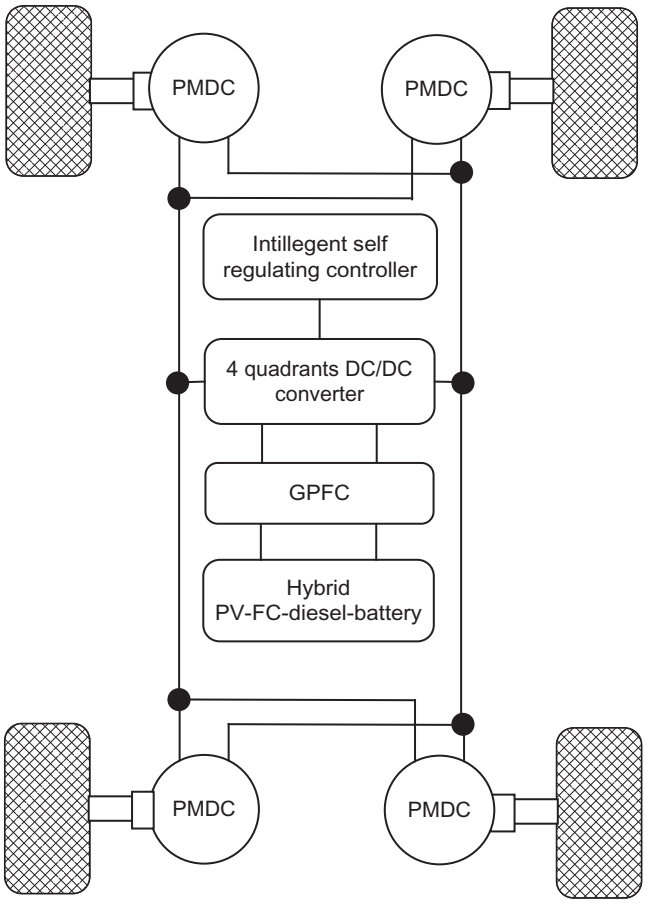


FIG. 38.12 Schematic diagram of a prototype all-wheel drive electric vehicle using four PMDC motors.

scheme. The novel PSO and GA self-tuned multiregulators and coordinated controller are used for the following purposes:

1. Diesel AC generator set with control regulator is based on excess generation and load dynamic matching and stabilization of the common DC collection bus using six-pulse-controlled rectifier.
2. AC/DC power converter regulator to regulate the DC voltage at the diesel engine AC/DC interface and ensure limited inrush conditions and dynamic power matching to reduce current transients and improve utilization at the diesel engine interface AC-DC bus.
3. The DC side green plug filter compensator GPFC-SPWM regulator for pulse-width switching scheme to regulate the DC bus voltage and minimize inrush current transients and load excursions and/or PV and FC nonlinear volt-ampere characteristics. The GPFC device acts as a matching DC-DC interface device between the DC load dynamic characteristics and that of the hybrid main PV, FC, and backup diesel generator set.
4. The permanent magnet DC motor drive with the speed regulator that ensures speed reference tracking with minimum inrush conditions and ensures reduced voltage transients and improved energy utilization.

The unified DC-AC utilization scheme is fully validated using the Matlab/Simulink software environment under normal conditions, DC load excursion, PMDC motor torque changes and the PV, and FC source output variations due to the inherent volt-ampere nonlinear relationship. Other excursion conditions in the diesel engine generator set are also introduced to assess

the control system robustness, effective energy utilization, and speed reference tracking.

Diesel generator set

From an electric system point of view, a diesel-driven AC generator can be represented as a prime mover and generator. Ideally, the prime mover has the capability to supply any power demand up to rated power at constant synchronous frequency. The synchronous generator connected to it must be able to keep the voltage constant at any load condition. The diesel engine kept the operating speed and frequency constant. When power demand fluctuates, the diesel generator could vary its power output via fuel valve regulation and governor control. The synchronous generator must control its output voltage by controlling its excitation current. Thus, the diesel generating system, as an auxiliary source, must be able to control its frequency and its output voltage. The ability of the diesel generator to respond to any frequency changes is affected by the inertia of the diesel gen set, the sensitivity of the governor, and the power capability of the diesel engine. The ability of the AC synchronous generator to control its terminal voltage can be affected by the field-winding time constant, the availability of DC excitation power to supply the field winding, and the time constant of the voltage control loop.

Photo voltaic PV

The equivalent circuit shown in Fig. 38.13 is used to model the PV cells used in the proposed PV array [29]. This model consists of a current source, a resistor, and a reverse parallel connected diode. The PVA model developed and used in Matlab/Simulink environment is based upon the circuit given in Fig. 38.13, in which the current produced by the solar cell is equal to that produced by the current source, minus that which flows through the diode, minus that which flows through the shunt resistor:

$$I = I_L - I_D - I_{SH} \tag{38.8}$$

where I = output current, I_L = photo-generated current, I_D = diode current, and I_{SH} = shunt current. The current through these elements is governed by the voltage across them:

$$V_j = V + IR_S \tag{38.9}$$

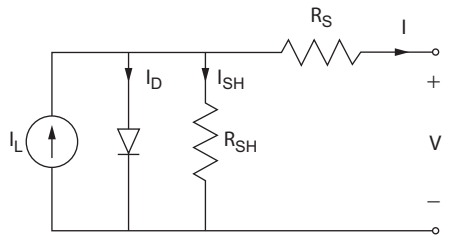


FIG. 38.13 The equivalent circuit of a solar cell.

where V_j = voltage across both diode and resistor R_{SH} (volts), V = voltage across the output terminals (volts), I = output current (amperes), and R_S = series resistance (Ω).

The current diverted through the diode is

$$I_D = I_o\left\{\exp\left[\frac{qV_j}{nkT}\right] - 1\right\} \tag{38.10}$$

where I_0 = reverse saturation current (amperes), n = diode ideality factor (1 for an ideal diode), q = elementary charge, k = Boltzmann's constant, and T = absolute temperature.

The characteristic equation of a solar cell, which relates solar cell parameters to the output current and voltage [30]:

$$I = I_L - I_o\left\{\exp\left[\frac{q(V+IR_s)}{nkT}\right] - 1\right\} - \frac{V+IR_s}{R_{SH}} \tag{38.11}$$

where R_{SH} = shunt resistance (Ω). The I-V curve of an illuminated PV cell has the shape shown in Fig. 38.14 as the voltage across the measuring load is swept from zero to V_{OC}, The power produced by the cell in watts can be easily calculated along the I-V sweep by the equation $P = IV$. At the I_{SC} and V_{OC} points, the power will be zero, and the maximum value for power will occur between the two.

Fuel cell energy system model

Fuel cell stacks were connected in series/parallel combination to achieve the rating desired. Fig. 38.15 shows a simplified diagram of the PEMFC system [31,32]. The FC model here is for a type of PEM, which uses the following electrochemical reaction:

$$H_2 + \frac{1}{2}O_2 \rightarrow H_2O + \text{Heat} + \text{Electrical Energy} \tag{38.12}$$

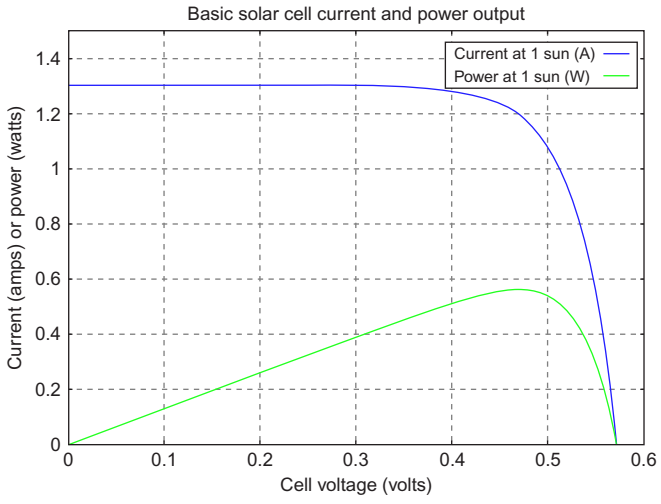


FIG. 38.14 The behavior of a solar cell at particular intensities of solar radiation.

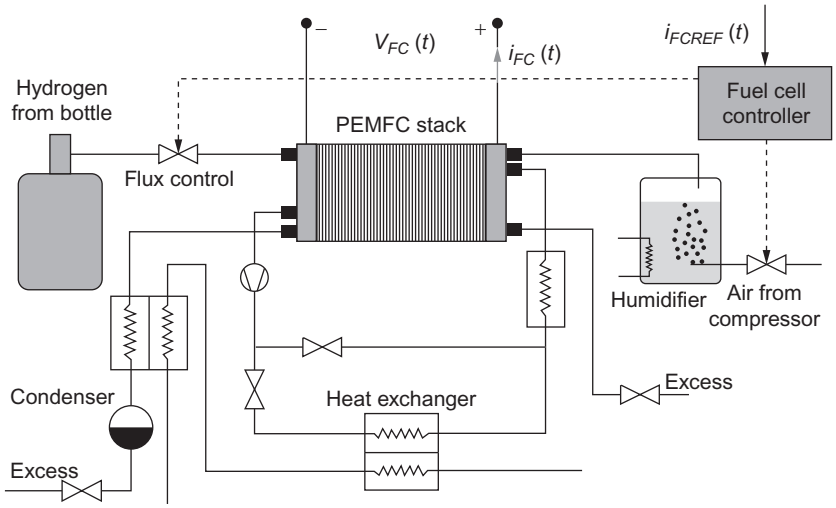


FIG. 38.15 Simplified diagram of the fuel cell PEMFC system.

Fig. 38.16 shows a simulated *V-I* (voltage versus current) polarization curve of a fuel cell [31,32]. As the cell current begins to increase from zero, a sudden drop of the output voltage of the fuel cell is seen. This drop of the cell voltage is due to activation voltage loss. Then, almost a linear decrease of the cell voltage is seen as the cell current increases beyond certain values, as shown in Fig. 38.17, which is a result of the ohmic loss. Finally, the cell voltage drops sharply to zero as the load current approaches the maximum current density that can be generated of the fuel cell. The sharp voltage drop is the effect of the concentration loss in the fuel cell. The fuel cell can be commonly modeled by simple equivalent first-order circuit shown in Fig. 38.10. The open circuit voltage is modified as follows:

$$E_{oc} = N(E_n - A \ln(i_o)) \tag{38.13}$$

where

$$A = \frac{RT}{Z\alpha F} \tag{38.14}$$

where $R = 8.3145$ J/(mol K); $F = 96{,}485$ As/mol; $z =$ number of moving electrons; $E_n =$ Nernst voltage, which is the thermodynamics voltage of the cells and depends on the temperatures and partial pressures of reactants and products inside the stack; and $i_0 =$ exchange current, which is the current resulting from the continual backward and forward flow of electrons from and to the electrolyte at no load. It depends also on the temperatures and partial pressures of reactants inside the stack. α is the

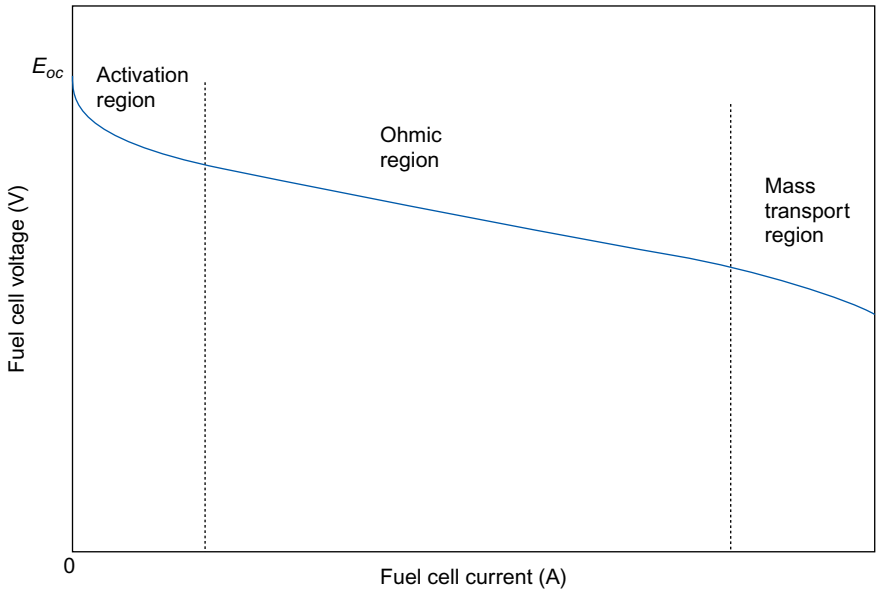


FIG. 38.16 (*V-I*) polarization curve of an SOFC.

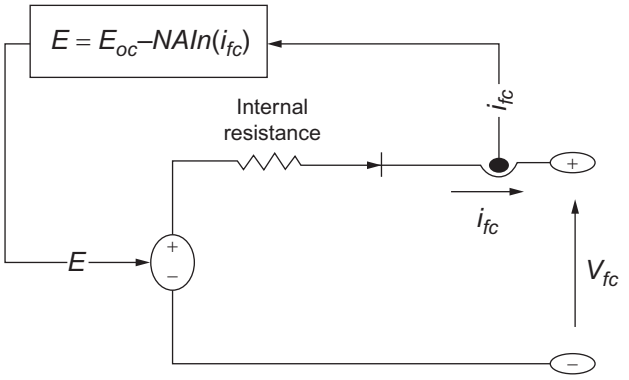


FIG. 38.17 DC-equivalent circuit of an electrochemical fuel cell.

charge transfer coefficient, which depends on the type of electrodes and catalysts used and T is the temperature of operation. The fuel cell voltage V_{FC} is modeled as [31,32]

$$V_{FC} = E_{oc} - V_{\text{Activation loss}} - V_{\text{Ohmic loss}} - V_{\text{Concentrion loss}} \quad (38.15)$$

where

$$V_{Activation\ Loss} = A\log\left(\frac{I_{FC}+i_n}{i_o}\right) \quad (38.16)$$

$$V_{Ohmic\ Loss} = R_m(I_{FC}+i_n) \quad (38.17)$$

$$V_{Concentration\ Loss} = B\log\left(1-\frac{I_{FC}+i_n}{i_L}\right) \quad (38.18)$$

Fuel cell stacks were connected in series/parallel combination to achieve the rating desired. The output of the fuel cell array was connected to a DC bus through a DC/DC converter. The DC bus voltage was kept constant via a DC bus voltage controller.

DC side green plug filter compensator GPFC

The common concerns of power quality are the long-duration voltage variations (overvoltage, undervoltage, and sustained interruptions), short-duration voltage variations (interruption, sags, and swells), voltage imbalance (voltage unbalance), waveform distortion (DC offset, harmonics, interharmonics, notching, and noise), voltage fluctuation (voltage flicker), and power frequency variations [33]. To prevent the undesirable states and to reduce the power consumption, a GPF scheme is used to stabilize the common DC bus.

Dynamic error driven control

The proposed control system developed by first author comprises four subregulators or controllers named as a diesel DC generator set value control regulator, DC side green plug filter compensator GPFC-SPWM regulator, the permanent magnet DC motor drive speed controller, and the AC/DC power converter regulator. Figs. 38.12–38.15 depict the proposed multiloop dynamic self-regulating controllers based on multiobjective optimization search and optimization technique based on soft computing PSO and GA. The global error is the summation of the three loop individual errors including voltage stability, current limiting, and synthesis dynamic power loops. Each multiloop dynamic control scheme is used to reduce a global error based on a triloop dynamic error summation signal and to mainly track a given speed reference trajectory loop error in addition to other supplementary motor current limiting, and dynamic power loops are used as auxiliary loops to generate a dynamic global total error signal that consists of not only the main loop speed error but also the current ripple, overcurrent limit, and dynamic overload power conditions.

The global error signal is input to the self-tuned controllers shown in Figs. 38.18–38.21. The (per unit) three-dimensional-error vector (e_{vg}, e_{Ig}, and e_{pg}) of the diesel engine controller scheme is governed by the following equations:

$$e_{vg}(k) = V_g(k)\left(\frac{1}{1+ST_g}\right)\left(\frac{1}{1+SD}\right) - V_g(k)\left(\frac{1}{1+ST_g}\right) \quad (38.19)$$

$$e_{Ig}(k) = I_g(k)\left(\frac{1}{1+ST_g}\right)\left(\frac{1}{1+SD}\right) - I_g(k)\left(\frac{1}{1+ST_g}\right) \quad (38.20)$$

$$e_{Pg}(k) = I_g(k)\times V_g(k)\left(\frac{1}{1+ST_g}\right)\left(\frac{1}{1+SD}\right) - I_g(k) \times V_g(k)\left(\frac{1}{1+ST_g}\right) \quad (38.21)$$

The total or global error $e_{tg}(k)$ at the AC side scheme at a time instant

$$e_{tg}(k) = \gamma_{vg}e_{vg}(k) + \gamma_{ig}e_{ig}(k) + \gamma_{pg}e_{pg}(k) \quad (38.22)$$

In the same manner, the (per unit) three-dimensional-error vector (e_{vd}, e_{Id}, and e_{pd}) of the GPFC scheme is governed by the following equations:

$$e_{vd}(k) = V_d(k)\left(\frac{1}{1+ST_d}\right)\left(\frac{1}{1+SD}\right) - V_d(k)\left(\frac{1}{1+ST_d}\right) \quad (38.23)$$

$$e_{Id}(k) = I_d(k)\left(\frac{1}{1+ST_d}\right)\left(\frac{1}{1+SD}\right) - I_d(k)\left(\frac{1}{1+ST_d}\right) \quad (38.24)$$

$$e_{Pd}(k) = I_d(k)\times V_d(k)\left(\frac{1}{1+ST_d}\right)\left(\frac{1}{1+SD}\right) - I_d(k) \times V_d(k)\left(\frac{1}{1+ST_d}\right) \quad (38.25)$$

and the total or global error $e_{td}(k)$ for the DC side green plug filter compensator GPFC scheme at a time instant

$$e_{td}(k) = \gamma_{vd}e_{vd}(k) + \gamma_{id}e_{id}(k) + \gamma_{pd}e_{pd}(k) \quad (38.26)$$

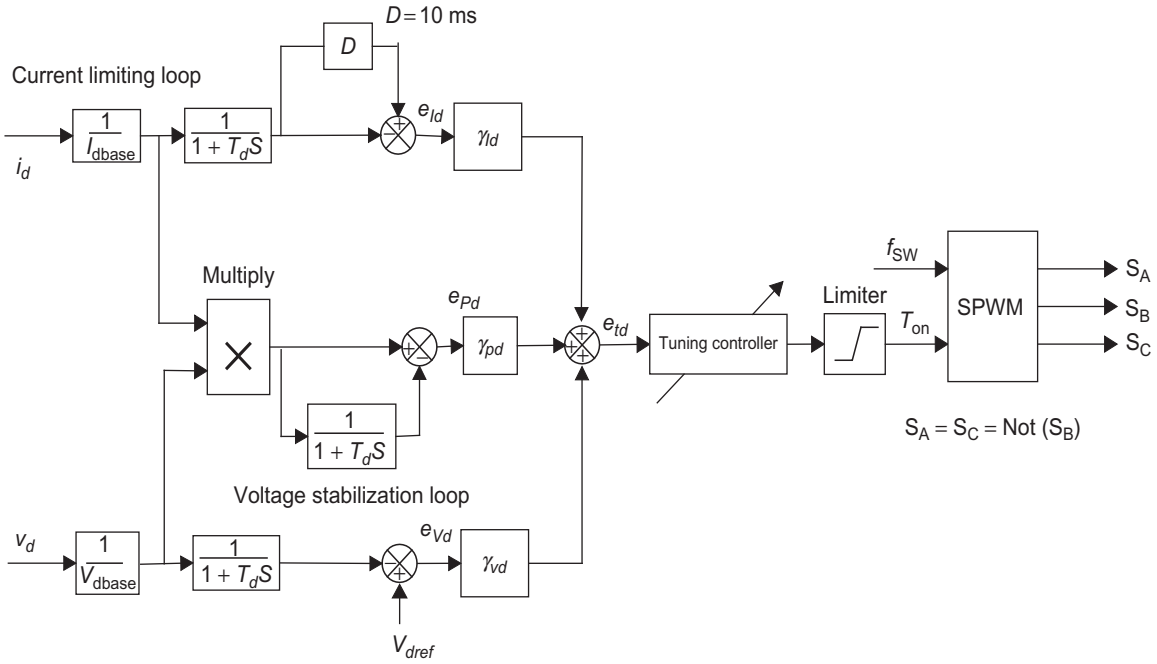


FIG. 38.18 Triloop error-driven self-regulating VSC/SMC/B-B controller for the common DC side GPFC scheme.

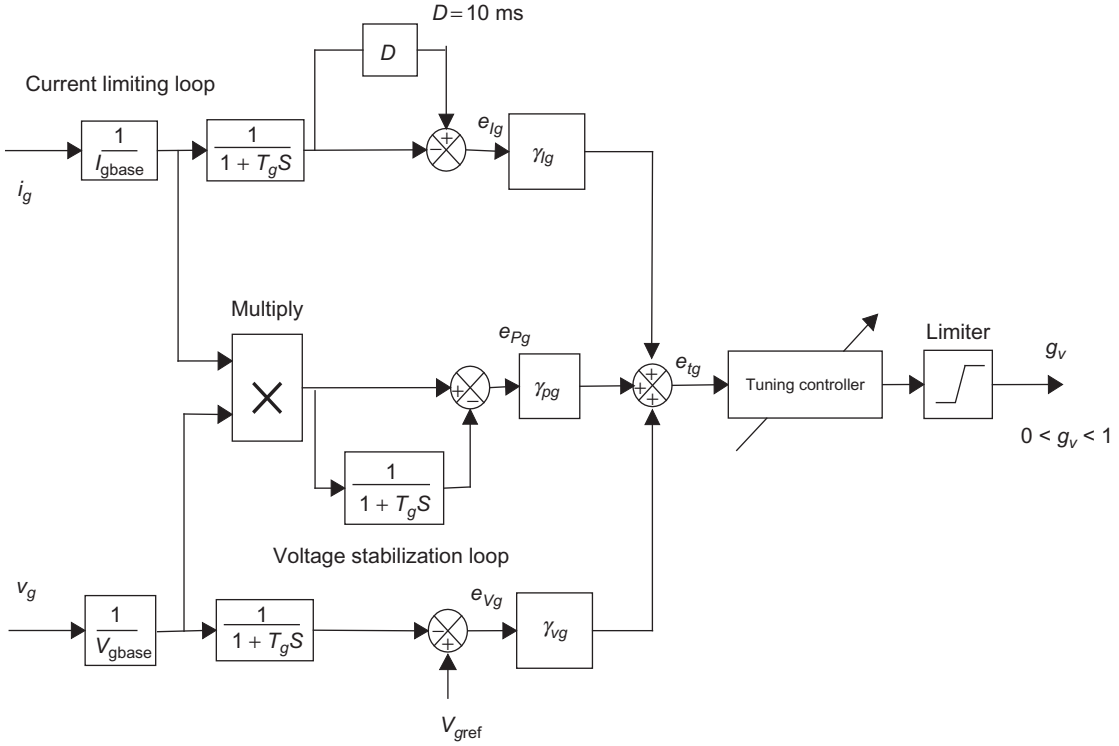


FIG. 38.19 Triloop error-driven self-regulating VSC/SMC/B-B controller for the diesel engine generator set.

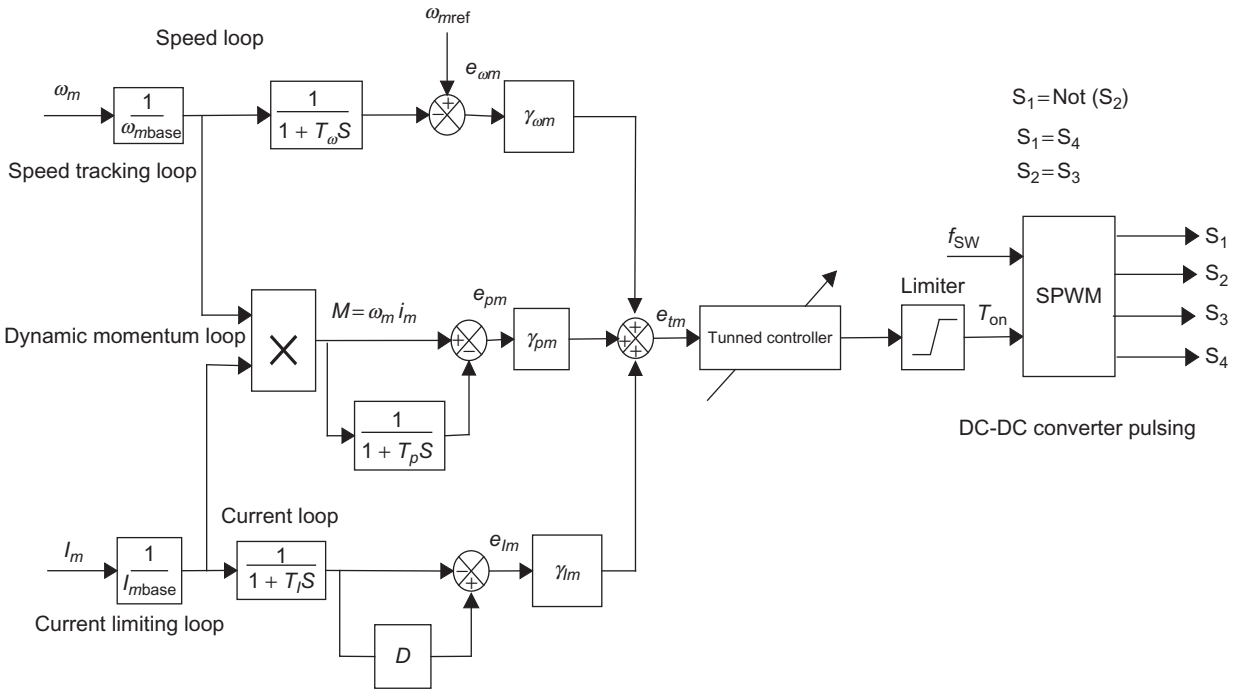


FIG. 38.20 Triloop error-driven self-regulating VSC/SMC/B-B controller for dynamic speed control PMDC motor drive.

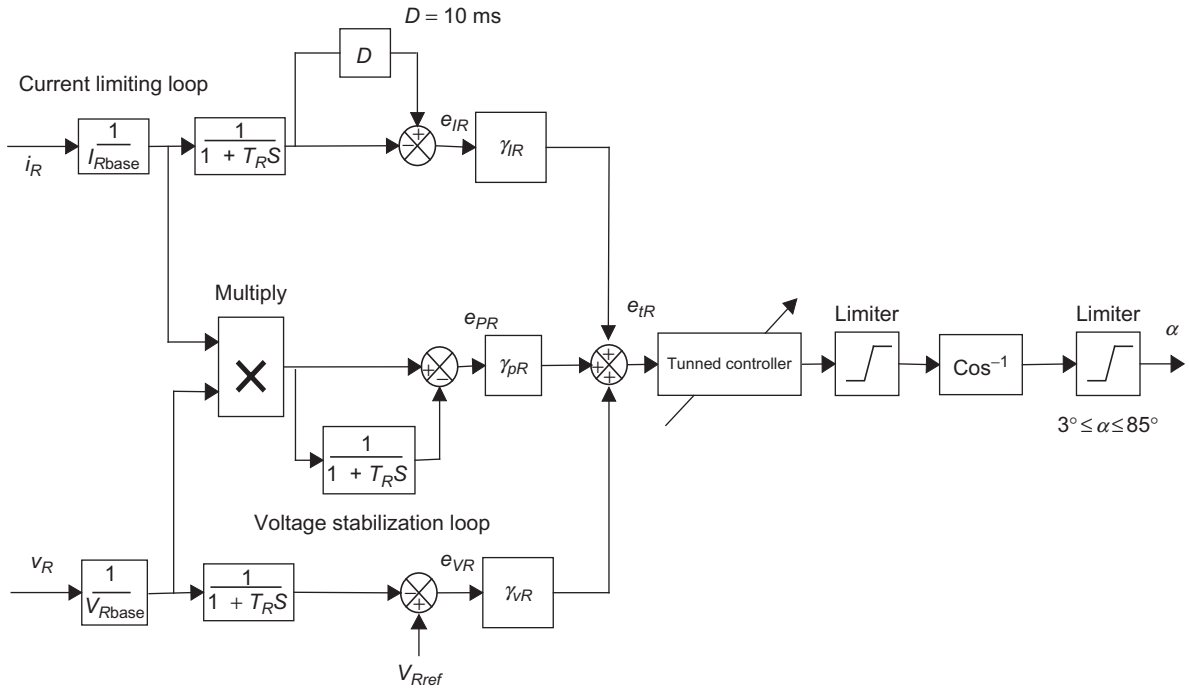


FIG. 38.21 Triloop error-driven self-regulating VSC/SMC/B-B controller firing angle α-controller for diesel AC/DC interface rectifier scheme.

In addition, The (per unit) three-dimensional-error vector (e_{vR}, e_{IR}, and e_{pR}) of the three-phase-controlled rectifier scheme is governed by the following equations:

$$e_{vR}(k) = V_R(k)\left(\frac{1}{1+ST_R}\right)\left(\frac{1}{1+SD}\right) - V_R(k)\left(\frac{1}{1+ST_R}\right) \tag{38.27}$$

$$e_{IR}(k) = I_R(k)\left(\frac{1}{1+ST_R}\right)\left(\frac{1}{1+SD}\right) - I_R(k)\left(\frac{1}{1+ST_R}\right) \tag{38.28}$$

$$e_{PR}(k) = I_R(k) \times V_R(k)\left(\frac{1}{1+ST_R}\right)\left(\frac{1}{1+SD}\right) - I_R(k) \times V_R(k)\left(\frac{1}{1+ST_R}\right) \tag{38.29}$$

The total or global error $e_{tR}(k)$ for the three-phase-controlled converter rectifier scheme at a time instant:

$$e_{tR}(k) = \gamma_{vR}e_{vR}(k) + \gamma_{iR}e_{iR}(k) + \gamma_{pR}e_{pR}(k) \tag{38.30}$$

Finally, the (per unit) three-dimensional-error vector ($e_{\omega m}$, e_{Im}, and e_{pm}) of the PMDC motor scheme is governed by the following equations:

$$e_{\omega m}(k) = \omega_m(k)\left(\frac{1}{1+ST_m}\right)\left(\frac{1}{1+SD}\right) - \omega_m(k)\left(\frac{1}{1+ST_m}\right) \tag{38.31}$$

$$e_{\mathrm{Im}}(k) = I_m(k)\left(\frac{1}{1+ST_m}\right)\left(\frac{1}{1+SD}\right) - I_m(k)\left(\frac{1}{1+ST_m}\right) \tag{38.32}$$

$$e_{Pm}(k) = I_m(k) \times \omega_m(k)\left(\frac{1}{1+ST_m}\right)\left(\frac{1}{1+SD}\right) - I_m(k) \times \omega_m(k)\left(\frac{1}{1+ST_m}\right) \tag{38.33}$$

and the total or global error $e_{tm}(k)$ for the MPFC scheme at a time instant

$$e_{tm}(k) = \gamma_{\omega m}e_{\omega m}(k) + \gamma_{im}e_{im}(k) + \gamma_{pm}e_{pm}(k) \tag{38.34}$$

A number of conflicting objective functions are selected to optimize using the PSO algorithm. These functions are defined by the following:

$$J_1 = \text{Minimize}\left\{\left|e_{tg}\right|, |e_{tR}|, |e_{td}|, |e_{tm}|\right\} \tag{38.35}$$

$$J_2 = \text{Steady state error} = |e_{\omega}(k)| = \left|\omega_{ref}(k) - \omega_m(k)\right| \tag{38.36}$$

$$J_3 = \text{Settling time} \tag{38.37}$$

$$J_4 = \text{Maximum over shoot} \tag{38.38}$$

$$J_5 = \text{Rise time} \tag{38.39}$$

In general, to solve this multiobjective complex optimality search problem, there are two possible optimization techniques based on particle swarm optimization (PSO): single aggregate selected objective optimization (SOO), which is explained, and multiobjective optimization (MOO). The main procedure of the SOO is based on selecting a single aggregate objective function with weighted single-objective parameters scaled by a number of weighting factors. The objective function is optimized (either minimized or maximized) using either GA or particle swarm optimization search algorithm (PSO) methods to obtain a single global or near-optimal solution. On the other hand, the main objective of the multiobjective (MO) problem is finding the set of acceptable (trade-off) optimal solutions. This set of accepted solutions is called Pareto front. These acceptable trade-off multilevel solutions give more ability to the user to make an informed decision by seeing a wide range of near-optimal selected solutions that are feasible and acceptable from an "overall" standpoint. Single-objective (SO) optimization may ignore this trade-off viewpoint, which is crucial. The main advantages of the proposed MOO method are the following: It doesn't require a priori knowledge of the relative importance of the objective functions, and it provides a set of acceptable trade-off near-optimal solutions. This set is called Pareto front or optimality trade-off surfaces. Both SOO and MOO searching algorithms are tested, validated, and compared. The dynamic error-driven controller regulates the controllers' gains using the particle swarm optimization (PSO) and GA to minimize the system total error, the settling time, the rising time, and the maximum overshoot. The proposed dynamic triloop error-driven controller, developed by the first author, is a novel advanced regulation concept that operates as an adaptive dynamic-type multipurpose controller capable of handling sudden parametric changes, load and/or DC source excursions. By using the triloop error-driven controller, it is expected to have a smoother, less dynamic overshoot and fast and more robust speed controller when compared with those of classical control schemes. The proposed general PMDC motor drive model with the novel triloop error-driven controller is fully validated in this application for effective reference speed trajectory tracking under different loading conditions and parametric variations, such as temperature changes, while driving a complex mechanical load with nonlinear parameters and/or torque-speed characteristics.

Self tuned variable structure sliding mode bang-bang VSC/SMC/B-B controller

In the variable structure sliding mode controller scheme, an optimally adaptive and self-tuned variable structure sliding

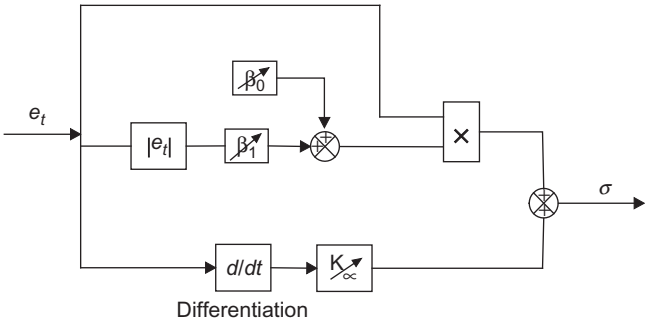


FIG. 38.22 VSC/SMC/B-B controller block diagram.

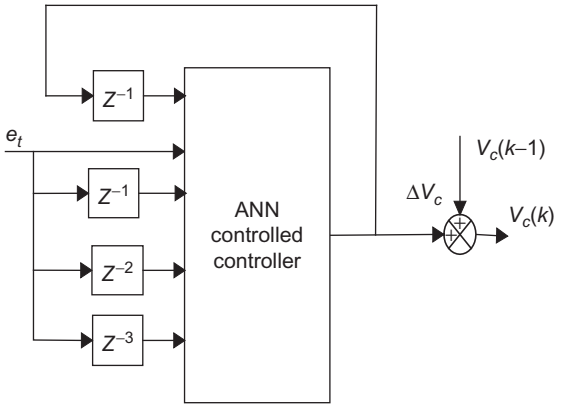


FIG. 38.23 ANN incremental controlled controller block diagram.

mode controller for PMDC motor drive systems using particle swarm optimization technique (PSO) and GA is shown in Fig. 38.22. The slope of the sliding surface is designed as

$$\sigma = \beta e_t + K_\alpha \frac{de_t}{dt} \tag{38.40}$$

With adaptive adjustable error scaling gain,

$$\beta = \beta_0 + \beta_1 |e_t| \tag{38.41}$$

where

$$|e_t| = \sqrt{(\gamma_I e_I)^2 + (\gamma_\omega e_\omega)^2 + (\gamma_V e_V)^2 + \left(\gamma_p e_p\right)^2} \tag{38.42}$$

The system control voltage has the following form in the time domain [33]: the control is an on-off logic; that is, when $\sigma > 0$, $V_c = 1$, and when $\sigma < 0$, $V_c = -1$

The PSO and GA search and optimization are implemented for tuning the various gains β_0, β_1, and α to minimize the selected five conflicting objective functions ($J_1 - J_5$). This test is to verify that the proposed VSC/B-B with adaptive β can maintain the motor speed with nonlinear $J(\omega_m)$ and $B(\omega_m)$ even if the load changes; accordingly, the robustness can be confirmed.

Self tuned artificial neural network controller ANN

The neural network used in this application is the simplest one that uses three layers, which is widely used in the control of the electric machines. Each layer is composed of neurons. Each neuron is connected via weights to the previous layer. The first layer is connected to the input variables. The second one is connected via weights to all the neurons of the previous layer, and the last one is composed of one neuron given the output value. The weights and the biases of the ANN network's are updated to provide that the global error of the system is minimized. The proposed ANN regulator is tuned online using the back-propagation algorithm. The online ANN rule-based algorithm is used to update the ANN network weights and biases to ensure continuous effective dynamic response while keeping the motor inrush current under specified tolerable limits. The input vector with three-layer ANN as shown in Fig. 38.23 is

$$\overline{X} = \{e_t(k), e_t(k-1), e_t(k-2), e_t(k-3), \Delta V_c(k-1)\} \tag{38.43}$$

Self tuned fuzzy logic controller (FLC)

As shown in Fig. 38.24, the FLC system consists of three subsystems, which are the fuzzification, rule base, and defuzzification. Fuzzification subsystem converts the exact inputs to fuzzy values using five membership functions: positive big (PB), positive small (PS), zero (ZZ), negative small (NS), and negative big (NB). The rule base unit processes these fuzzy values with fuzzy rules. The defuzzification unit converts the fuzzy results to exact values. The FLC input values are the global error, e_t, and change in global error, de_t. According to these variables, a rule table is produced in the FLC rule base unit as shown in Table 38.4.

38.8.2.2 Digital Simulation Results

The integrated microgrid for PMDC-driven electric vehicle scheme using the photovoltaic (PV), fuel cell (FC), and backup diesel generation with battery backup renewable generation system performance is compared for two cases, with fixed and self-tuned-type controllers using either GA or PSO. The second case is to compare the performance with artificial neural network (ANN) controller and fuzzy logic controller (FLC) with the self-tuned-type controllers using either GA or PSO. The tuned variable structure sliding mode controller VSC/SMC/B-B has been applied to the speed tracking control of the same EV for performance comparison. There are three different speed references. In the first speed track, the speed increases linearly and reaches the 1 pu at the end of the first 5 s, and then, the reference speed remains speed constant during 5 s. At tenth second, the reference speed decreases with same slope as at the first 5 s. After 15 s, the motor changes the direction and EV increases its speed through the reverse direction. At twentieth second, the reference speed reaches the −1 pu and remains constant speed at the end of twenty-fifth second, and then, the reference speed decreases and

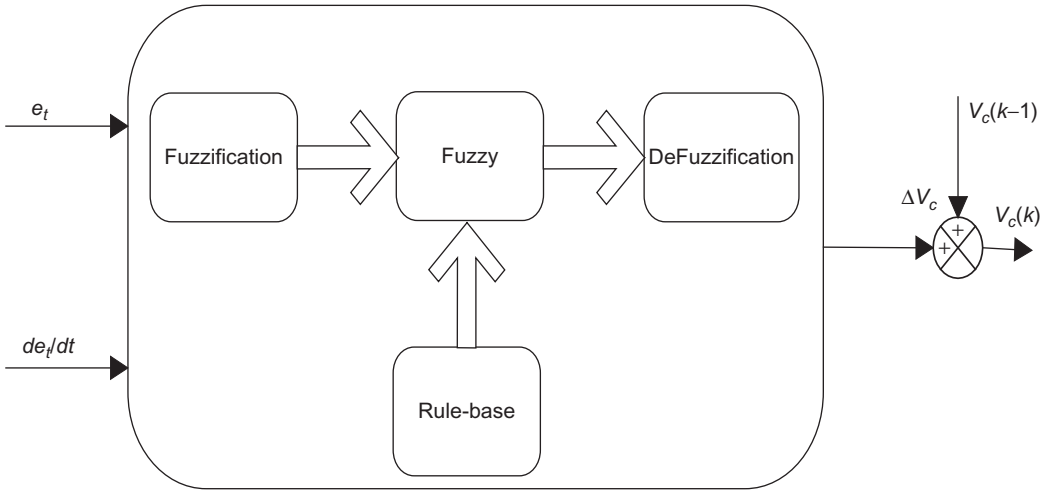


FIG. 38.24 Main structure of the FLC incremental scheme.

TABLE 38.4 Fuzzy rule decision table

	de_t				
e_t	NB	NS	ZZ	PS	PB
NB	NB	NB	NS	NS	ZZ
NS	NB	NS	NS	ZZ	PS
ZZ	NS	NS	ZZ	PS	PS
PS	NS	ZZ	PS	PS	PB
PB	ZZ	PS	PS	PB	PB

becomes zero at thirtieth second. The second reference speed waveform is sinusoidal, and its magnitude is 1 pu, and the period is 12 s. The third reference track is constant speed reference starting with an exponential track. In all references, the system responses have been observed. Matlab/Simulink software was used to design, test, and validate the effectiveness of the integrated microgrid for PMDC-driven electric vehicle scheme using photovoltaic (PV), fuel cell (FC), and backup diesel generation with battery backup renewable generation system with the FACTS devices. The digital dynamic simulation model using Matlab/Simulink software environment allows for low-cost assessment and prototyping, system parameter selection, and optimization of control settings. The use of PSO search algorithm is utilized in online gain adjusting to minimize controller absolute value of total error. This is required before full-scale prototyping that is both expensive and time-consuming. The effectiveness of dynamic simulators brings on detailed submodels selections and tested submodels Matlab library of power system components already tested and validated. The common DC bus voltage reference is set at 1 pu. Digital simulations are obtained with sampling interval Ts = 20 μs. Dynamic responses obtained with GA are compared with the ones resulting from the PSO for the seven proposed self-tuned controllers. The dynamic simulation conditions are identical for all tuned controllers. To compare the global performances of all controllers, the normalized mean-square-error (*NMSE*) deviations between output plant variables and desired values and is defined as

$$NMSE_{V_{\mathrm{DC-bus}}} = \frac{\sum \left(V_{\mathrm{DC-bus}} - V_{\mathrm{DC-bus-ref}}\right)^2}{\sum \left(V_{\mathrm{DC-bus-ref}}\right)^2} \tag{38.44}$$

$$NMSE_{\omega_m} = \frac{\sum \left(\omega_m - \omega_{m-ref}\right)^2}{\sum \left(\omega_{m-ref}\right)^2} \tag{38.45}$$

The digital simulation results validated the effectiveness of both GA- and PSO-based tuned controllers in providing effective speed tracking minimal steady-state errors. Transients are also damped with minimal overshoot, settling time, and fall time. The GA- and PSO-based self-tuned controllers are more effective and dynamically advantageous in comparison with the artificial neural network (ANN) controller, the fuzzy logic controller (FLC), and fixed-type controllers. The self-regulation is based on minimal value of absolute total/global error of each regulator shown in Figs. 38.18–38.21. The control system comprising the three dynamic multiloop error-driven regulators is coordinated to minimize the selected objective functions. SOO obtains a single global or near-optimal solution based on a single-weighted objective function. The weighted single-objective function combines several objective functions using specified or selected weighting factors as follows:

$$\text{weighted objective function} = \alpha_1 J_1 + \alpha_2 J_2 + \alpha_3 J_3 + \alpha_4 J_4 + \alpha_5 J_5 \tag{38.46}$$

where $\alpha_1 = 0.20$, $\alpha_2 = 0.20$, $\alpha_3 = 0.20$, $\alpha_4 = 0.20$, and $\alpha_5 = 0.20$ are selected weighting factors. J_1, J_2, J_3, J_4, and J_5 are the selected objective functions. On the other hand, the MO finds the set of

acceptable (trade-off) optimal solutions. This set of accepted solutions is called Pareto front. These acceptable trade-off multilevel solutions give more ability to the user to make an informed decision by seeing a wide range of near-optimal selected solutions.

Table 38.5 shows the optimal solutions of the main objective functions versus the tuned variable structure sliding mode controller gain-based SOGA and MOGA control schemes. On the other hand, Table 38.6 shows the optimal solutions of the main objective functions versus the tuned variable structure sliding mode controller gain-based SOPSO and MOPSO control schemes. Table 38.7 shows the DC bus behavior comparison using the GA-based tuned variable structure sliding mode controller for the three selected reference tracks. In addition, Table 38.8 shows the system behavior using the PSO-based tuned variable structure sliding mode controller. Figs. 38.25–38.30 show the effectiveness of MOPSO and MOGA search and optimized control gains in tracking the PMDC-EV motor three reference speed trajectories. Comparing the PMDC-EV dynamic response results of the two study cases, with GA and PSO tuning algorithms and traditional controllers with constant controller gain results shown in Table 38.9, ANN controller in Table 38.10 (Figs. 38.31–38.33) and FLC in Table 38.11 (Figs. 38.34–38.36), it is quite apparent that the GA and PSO tuning algorithms highly improved the PMDC-EV system dynamic performance from a general power quality point of view. The GA and PSO tuning algorithms had a great impact on the system efficiency improving it from 0.906631 (constant gains controller), 0.928253 (ANN controller), and 0.937334 (FLC) to around 0.948156 (GA-based tuned controller) and 0.930708 (PSO-based tuned controller) that is highly desired. Moreover, the normalized mean square error ($NMSE\text{-}V_{\text{DC-Bus}}$) of the DC bus voltage is reduced from 0.08443 (constant gains controller), 0.04827 (ANN controller), and 0.03022 (FLC) to around 0.007304 (GA-based tuned controller) and 0.005854 (PSO-based tuned controller). In addition, the normalized mean square error ($NMSE_\omega_m$) of the PMDC motor is reduced from 0.053548 (constant gains controller), 0.02627 (ANN controller), and 0.02016 (FLC) to around 0.0076308 (GA-based tuned controller) and 0.006309 (PSO-based tuned controller). Maximum transient DC voltage over/undershoot (pu) is reduced from 0.054604 (constant gains controller), 0.04186 (ANN controller), and 0.03126 (FLC) to around 0.009302 (GA-based tuned controller) and 0.007259 (PSO-based tuned controller). Maximum transient DC current—over/undershoot (pu) is reduced from 0.087336 (constant gains controller), 0.07355 (ANN controller), and 0.04383 (FLC) to around 0.00292 (GA-based tuned controller) and 0.005987 (PSO-based tuned controller). DC bus voltage (pu) is improved from 0.917020 (constant gains controller), 0.932736 (ANN controller), and 0.94745 (FLC) to around

TABLE 38.5 Selected objective functions versus the tuned variable structure sliding mode controller-based SOGA and MOGA control schemes

	The diesel generator regulator $\begin{bmatrix} K_{\alpha g} \\ \beta_{0g} \\ \beta_{1g} \end{bmatrix}$	The GPFC-DC side regulator $\begin{bmatrix} K_{\alpha d} \\ \beta_{0d} \\ \beta_{1d} \end{bmatrix}$	The PMDC motor regulator $\begin{bmatrix} K_{\alpha m} \\ \beta_{0m} \\ \beta_{1m} \end{bmatrix}$	The α- controller for the converter regulator $\begin{bmatrix} K_{\alpha R} \\ \beta_{0R} \\ \beta_{1R} \end{bmatrix}$	J_1 Minimize the (total error) $\times 10^{-2}$	J_2 Minimize the (steady-state error) (pu) $\times 10^{-2}$	J_3 Minimize the (settling time) (pu) $\times 10^{-2}$	J_4 Minimize the (maximum overshoot) $\times 10^{-2}$	J_5 Minimize the (rise time) $\times 10^{-2}$
SOGA	0.4111	0.6814	0.5376	0.0775	0.4262	0.9659	0.3315	0.6058	0.4274
	7.6052	7.2686	3.7351	2.3320					
	34.4595	18.0903	20.3967	49.4889					
MOGA	0.2438	0.1278	0.5250	0.7085	0.3359	0.1214	0.1330	0.6465	0.5219
	6.7638	9.9706	4.6294	2.0195					
	39.6771	41.6427	29.9333	31.7174					
	0.4171	0.7711	0.0017	0.8023	0.6439	0. 5840	0.8680	0.5505	0.4381
	9.9078	7.3238	7.2307	6.6139					
	42.8415	30.3825	41.9151	33.9013					
	0.0796	0.5655	0.9480	0.5227	0.9325	0.7425	0.1286	0.4502	0.1956
	4.6150	9.8655	8.5251	9.5619					
	14.8331	27.3988	20.8308	27.8837					
	0.5943	0.8238	0.8155	0.3747	0. 6220	0.8159	0.7435	0.3811	0.8706
	2.5467	9.8989	2.4722	5.2401					
	14.8681	13.7004	37.7790	42.9201					
	0.8499	0.9512	0.2953	0.4528	0.8135	0.2985	0.1727	0.4810	0. 7690
	5.2918	2.8911	6.2706	8.2844					
	40.0583	30.3251	45.0299	22.0045					
	0.7103	0.0042	0.3397	0.3788	0.6970	0.7092	0.4680	0.3245	0.8129
	5.8841	9.0935	8.5068	7.4244					
	13.7034	26.9887	27.6030	33.5903					

TABLE 38.6 Selected objective functions versus the tuned variable structure sliding mode controller gains based SOPSO and MOPSO control schemes

	The Diesel generator Regulator $\begin{bmatrix} K_{\alpha g} \\ \beta_{0g} \\ \beta_{1g} \end{bmatrix}$	The GPFC – DC side Regulator $\begin{bmatrix} K_{\alpha d} \\ \beta_{0d} \\ \beta_{1d} \end{bmatrix}$	The PMDC motor Regulator $\begin{bmatrix} K_{\alpha m} \\ \beta_{0m} \\ \beta_{1m} \end{bmatrix}$	the α- controller for the converter Regulator $\begin{bmatrix} K_{\alpha R} \\ \beta_{0R} \\ \beta_{1R} \end{bmatrix}$	J_1 Minimize the (Total Error) $\times 10^{-2}$	J_2 Minimize the (Steady State Error) (PU) $\times 10^{-2}$	J_3 Minimize the (Settling Time) (PU) $\times 10^{-2}$	J_4 Minimize the (Maximum Overshoot) $\times 10^{-2}$	J_5 Minimize the (Rise Time) $\times 10^{-2}$
SOPSO	0.6420	0.8224	0.4837	0.9958	0.6430	0.5063	0.3271	0.2178	0.1942
	3.5994	4.5435	1.5718	4.7632					
	15.9501	45.8496	30.2713	38.4880					
MOPSO	0.9180	0.1091	0.9511	0.2032	0.1188	0.4657	0.8187	0.7850	0.6490
	6.8088	7.1060	5.3405	3.3284					
	41.9628	26.4457	33.8367	26.9778					
	0.7877	0.6885	0.4439	0.4364	0.6431	0.6374	0.4381	0.3956	0.1433
	8.2403	6.4446	9.0896	5.2320					
	33.1334	45.6199	26.3367	19.1299					
	0.2735	0.5283	0.4714	0.6509	0.7553	0.1289	0.5451	0.7768	0.3175
	8.0252	9.0582	4.1808	5.1085					
	25.5645	47.8210	19.7245	49.4370					
	0.6223	0.2945	0.0753	0.5513	0.7700	0.5610	0.5095	0.3739	0.5064
	6.1631	3.5565	5.5806	5.3880					
	35.5179	44.9276	33.6105	40.9104					
	0.7421	0.5091	0.8113	0.5772	0.8056	0.2506	0.4081	0.7742	0.2081
	8.5694	4.4184	3.9733	5.9874					
	17.4213	35.7326	46.4878	27.2446					
	0.8711	0.0135	0.5838	0.7024	0.5603	0.3070	0.6489	0.1938	0.3129
	7.2711	4.0452	8.5443	1.7882					
	17.0029	26.1268	30.2219	17.1486					

TABLE 38.7 DC bus behavior comparison using the GA-based tuned variable structure sliding mode controller VSC/SMC/B-B

	The first speed track	The second speed track	The third speed track
DC bus voltage (pu)	0.964652	0.97417	0.964182
DC bus current (pu)	0.60878	0.614695	0.613914
Maximum transient DC voltage over/undershoot (pu)	0.0085931	0.009302	0.008437
Maximum transient DC current—over/undershoot (pu)	0.002005	0.00292	0.0028122
DC system efficiency	0.9404	0.948156	0.94302
$NMSE_V_{\text{DC-bus}}$	0.0073133	0.007304	0.008248
$NMSE_\omega_m$	0.0074627	0.0076308	0.008558
PMDCM total controller error e_{tm}	0.008187	0.009167	0.007663
DC side GPFC error e_{td}	0.003062	0.004618	0.004337
The diesel engine gen set total controller error e_{tg}	0.0047025	0.005121	0.004377
The diesel engine converter total controller error e_{tR}	0.002879	0.003265	0.002328

TABLE 38.8 DC bus behavior comparison using the PSO-based tuned variable structure sliding mode controller VSC/SMC/B-B

	The first speed track	The second speed track	The third speed track
DC bus voltage (pu)	0.97347	0.974602	0.950341
DC bus current (pu)	0.604077	0.607674	0.605076
Maximum transient DC voltage over/undershoot (pu)	0.0073109	0.007259	0.008571
Maximum transient DC current—over/undershoot (pu)	0.004746	0.005987	0.0047885
DC system efficiency	0.932558	0.930708	0.9327892
$NMSE_V_{\text{DC-bus}}$	0.004941	0.005854	0.0052055
$NMSE_\omega_m$	0.0065287	0.006309	0.007071
PMDCM total controller error e_{tm}	0.005095	0.0048638	0.0052238
DC side GPFC error e_{td}	0.0072358	0.0074294	0.007769
The diesel engine gen set total controller error e_{tg}	0.0069206	0.007013	0.0071823
The diesel engine converter total controller error e_{tR}	0.005167	0.0053836	0.0052152

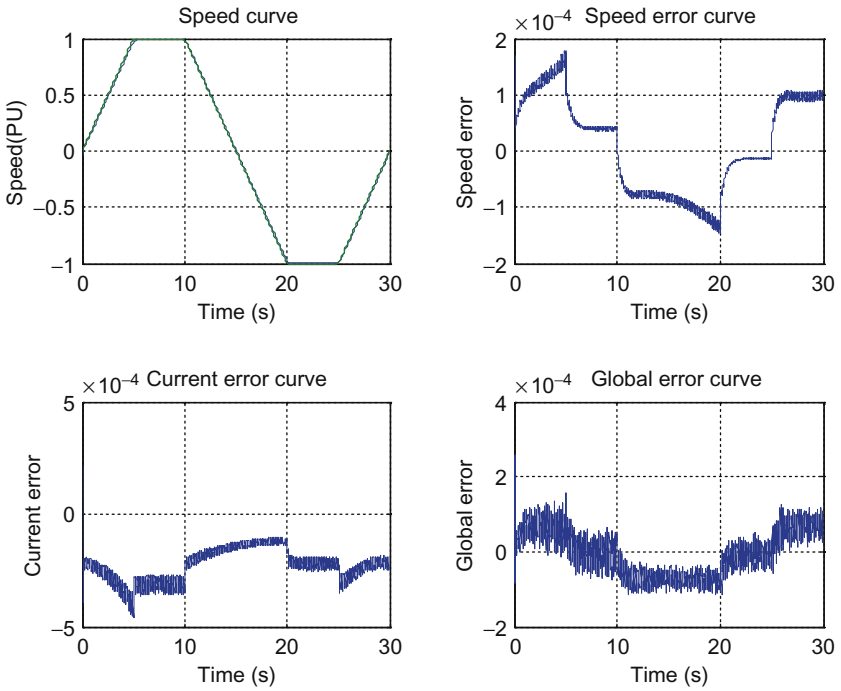


FIG. 38.25 EV-PMDC motor speed response for the first speed track using GA-based tuned triloop variable structure sliding mode controller VSC/SMC/B-B.

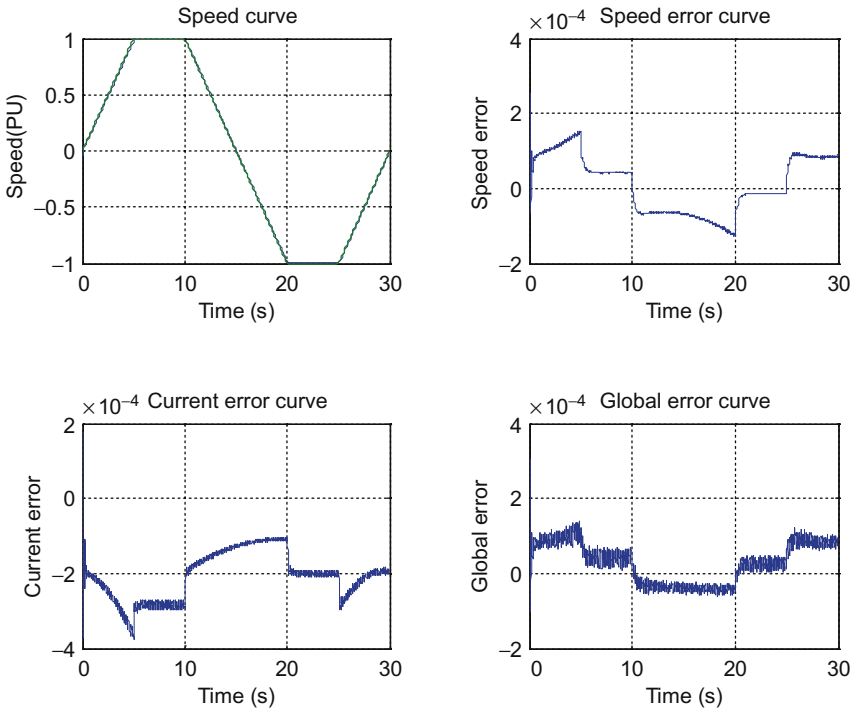


FIG. 38.26 EV-PMDC motor speed response for the first speed track using PSO-based tuned triloop variable structure sliding mode controller VSC/SMC/B-B.

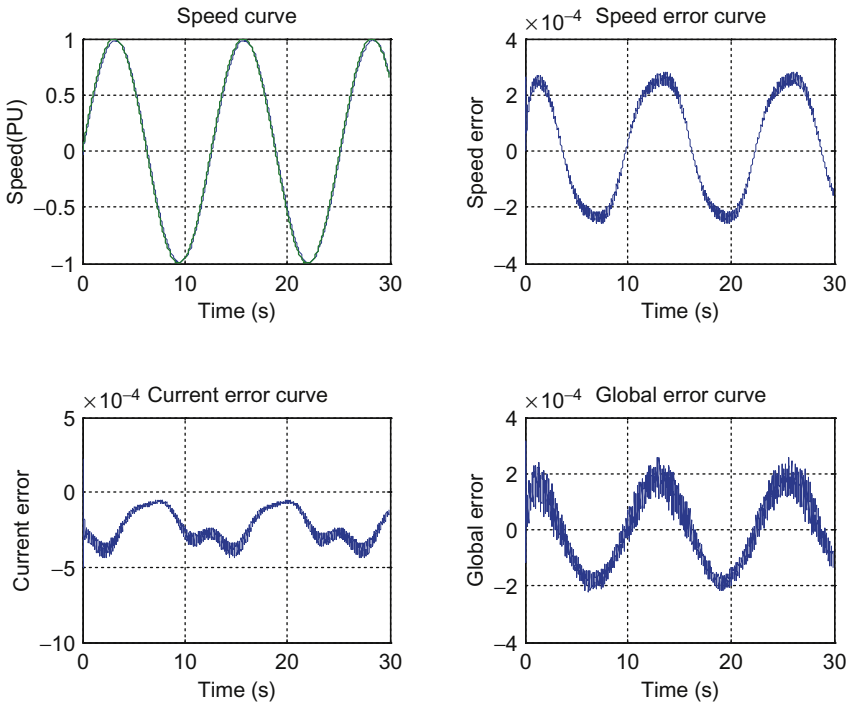


FIG. 38.27 EV-PMDC motor speed response for the second speed track using GA-based tuned triloop variable structure sliding mode controller VSC/SMC/B-B.

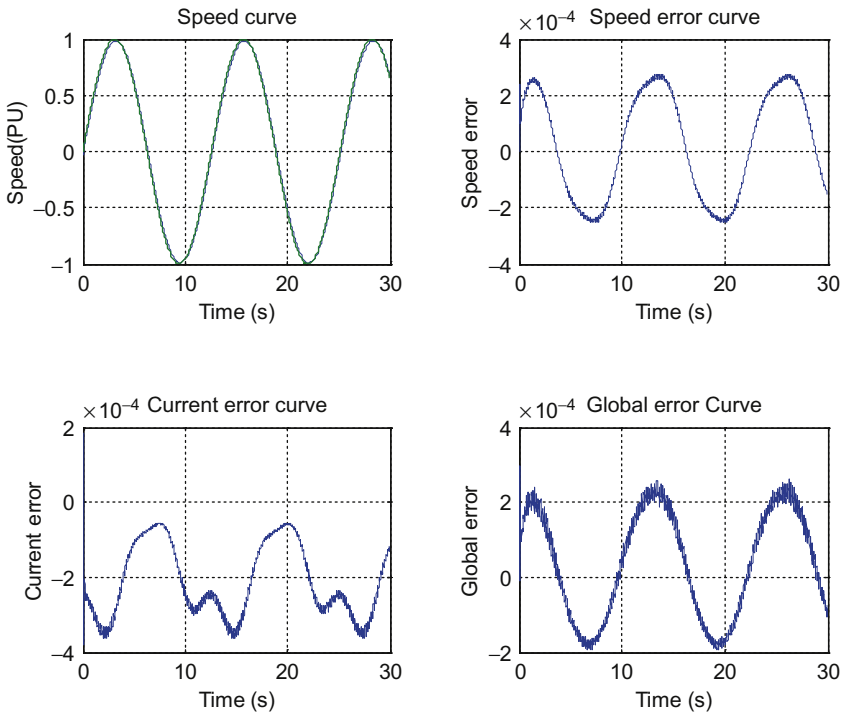


FIG. 38.28 EV-PMDC motor speed response for the second speed track using PSO-based tuned triloop variable structure sliding mode controller VSC/SMC/B-B.

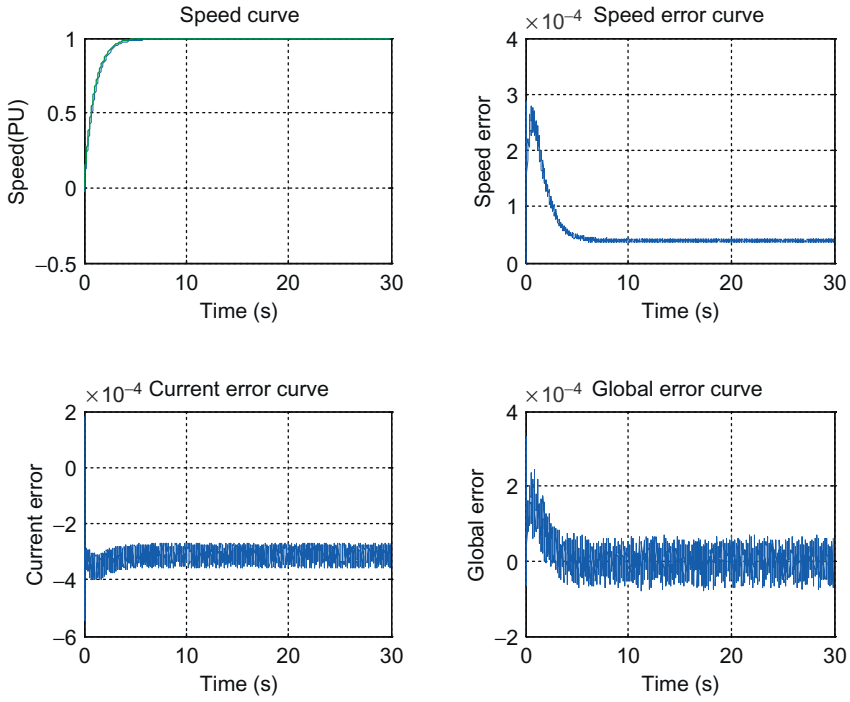


FIG. 38.29 EV-PMDC motor speed response for the third speed track using GA-based tuned triloop variable structure sliding mode controller VSC/SMC/B-B.

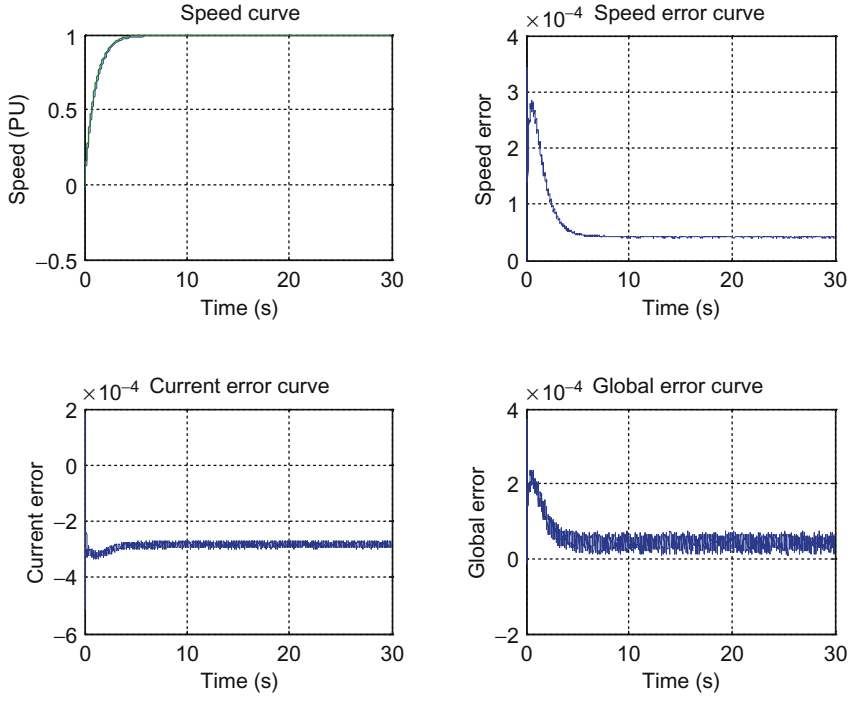


FIG. 38.30 EV-PMDC motor speed response for the third speed track using PSO-based tuned triloop variable structure sliding mode controller VSC/SMC/B-B.

TABLE 38.9 DC bus behavior comparison using the constant parameter variable structure sliding mode controller VSC/SMC/B-B

	The first speed track	The second speed track	The third speed track
DC bus voltage (pu)	0.904060	0.917020	0.895291
DC bus current (pu)	0.76545	0.769594	0.769731
Maximum transient DC voltage over/undershoot (pu)	0.052925	0.054604	0.053089
Maximum transient DC current—over/undershoot (pu)	0.09461	0.087336	0.081906
DC system efficiency	0.885737	0.906631	0.895666
$NMSE_V_{\text{DC-bus}}$	0.09512	0.08443	0.084672
$NMSE_\omega_m$	0.05131	0.053548	0.053953
PMDCM total controller error e_{tm}	0.08521	0.095145	0.09422
DC side GPFC error e_{td}	0.072338	0.70746	0.703462
The diesel engine gen set total controller error e_{tg}	0.062513	0.067513	0.069606
The diesel engine converter total controller error e_{tR}	0.08856	0.086233	0.085740

TABLE 38.10 DC bus behavior comparison using ANN controller

	The first speed track	The second speed track	The third speed track
DC bus voltage (pu)	0.92747	0.932736	0.91131
DC bus current (pu)	0.661466	0.67464	0.64627
Maximum transient DC voltage over/undershoot (pu)	0.0372	0.04186	0.05541
Maximum transient DC current—over/undershoot (pu)	0.08575	0.07355	0.06083
DC system efficiency	0.916100	0.928253	0.926261
$NMSE_V_{\text{DC-bus}}$	0.03439	0.04827	0.05231
$NMSE_\omega_{\text{m}}$	0.03793	0.02627	0.03146
PMDCM total controller error e_{tm}	0.04261	0.04200	0.04639
DC side GPFC error e_{td}	0.02397	0.02416	0.02440
The diesel engine gen set total controller error e_{tg}	0.04437	0.04507	0.05522
The diesel engine converter total controller error e_{tR}	0.03388	0.03978	0.03463

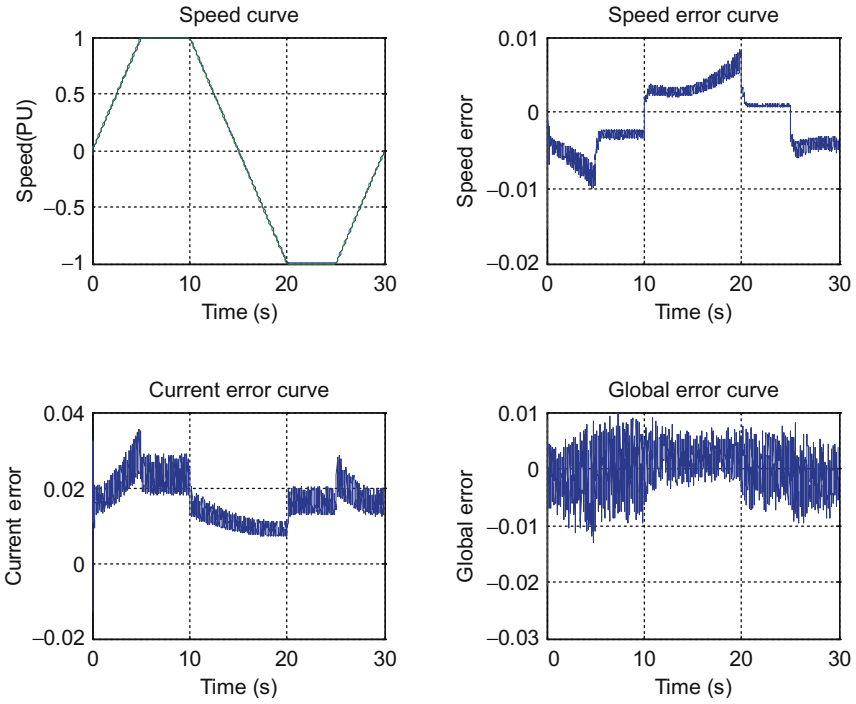


FIG. 38.31 EV-PMDC motor speed response for the first speed track using ANN-based controller.

0.97417 (GA-based tuned controller) and 0.974602 (PSO-based tuned controller). DC bus current (pu) is reduced from 0.769594 (constant gains controller), 0.67464 (ANN controller), and 0.64712 (FLC) to around 0.614695 (GA-based tuned controller) and 0.607674 (PSO-based tuned controller). PMDCM total controller Error (e_{tm}) is reduced from 0.095145 (constant gains controller), 0.04200 (ANN controller), and 0.02154 (FLC) to around 0.009167 (GA-based tuned controller) and 0.0048638 (PSO-based tuned controller). DC side GPFC Error (e_{td}) is reduced from 0.70746 (constant gains controller), 0.03416 (ANN controller), and 0.02416 (FLC) to around 0.004618 (GA-based tuned controller) and 0.0074294 (PSO-based tuned

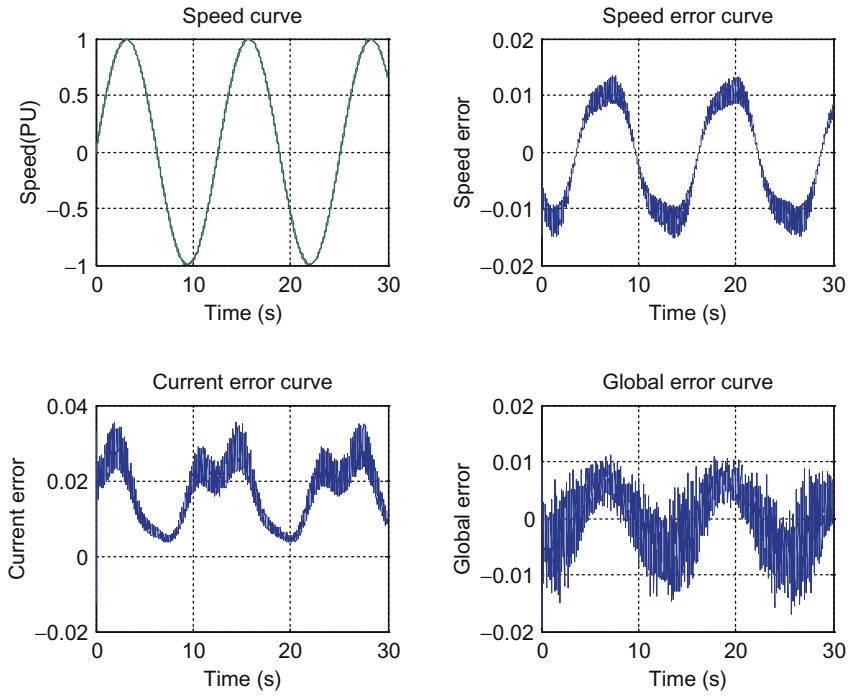


FIG. 38.32 EV-PMDC motor speed response for the second speed track using ANN-based controller.

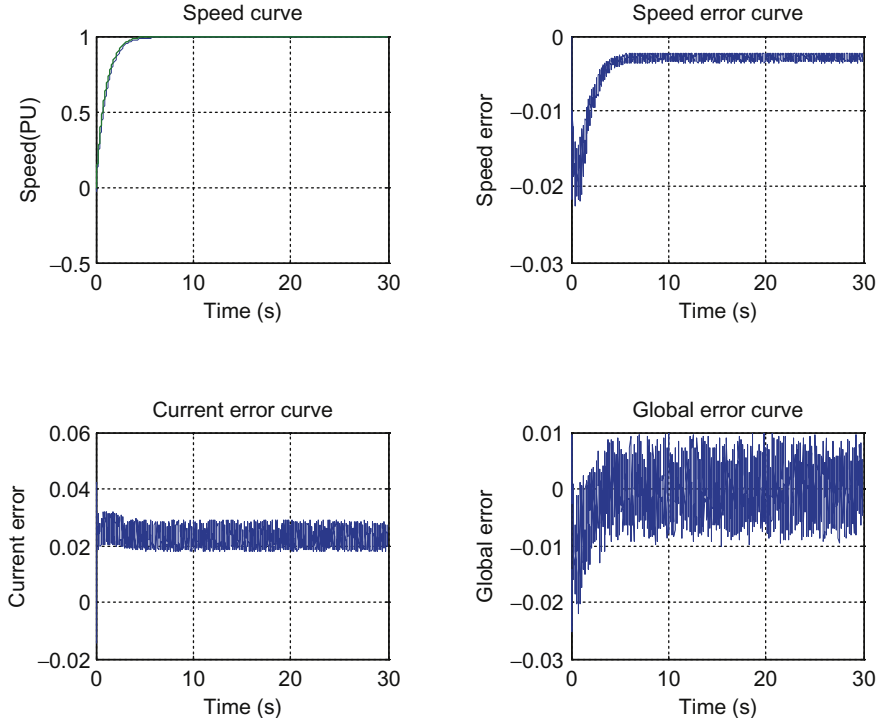


FIG. 38.33 EV-PMDC motor speed response for the third speed track using ANN-based controller.

TABLE 38.11 DC bus behavior comparison using FLC controller

	The first speed track	The second speed track	The third speed track
DC bus voltage (pu)	0.943860	0.94745	0.930581
DC bus current (pu)	0.65611	0.64712	0.630216
Maximum transient DC voltage over/undershoot (pu)	0.03898	0.03126	0.02065
Maximum transient DC current—over/undershoot (pu)	0.05658	0.04383	0.05014
DC system efficiency	0.926459	0.92890	0.937334
$NMSE_V_{\text{DC-bus}}$	0.04193	0.03022	0.02129
$NMSE_\omega_m$	0.0192	0.02016	0.02024
PMDCM total controller error e_{tm}	0.02956	0.02154	0.02852
DC side GPFC error e_{td}	0.06562	0.09179	0.07781
The diesel engine gen set total controller error e_{tg}	0.0337	0.02964	0.02928
The diesel engine converter total controller error e_{tR}	0.02533	0.0260	0.02051

controller). The diesel engine gen set total controller error (e_{tg}) is reduced from 0.067513 (constant gains controller), 0.04507 (ANN controller), and 0.02964 (FLC) to around 0.005121 (GA-based tuned controller) and 0.007013 (PSO-based tuned controller). The diesel engine converter total controller error (e_{tR}) is reduced from 0.086233 (constant gains controller), 0.03978 (ANN controller), and 0.0260 (FLC) to around 0.003265 (GA-based tuned controller) and 0.0053836 (PSO-based tuned controller).

38.8.3 Novel Self Regulating Green Plug/Energy Management/Energy Economizer GP-EM-EE Schemes for Wind Driven Induction Generation

The application presents a novel self-adjusting wind energy utilization scheme using a modified single-phase operation of the three-phase induction generator supplemented by a voltage stabilization switched filter compensation scheme developed by the first author. The series-parallel switched capacitor filter scheme is controlled by a dynamic particle swarm optimization (PSO) and GA error-driven self-adjusting controller to ensure voltage stabilization, minimum impact of the electric load excursions, and wind variations on terminal voltage. The sinusoidal pulse-width modulation complementary switching scheme is dynamically controlled using online minimal global error search that continuously adjusts and modifies the controller gains. The application presents a family of novel switched smart filter compensated devices using green plug/energy management/energy economizer GP-EM-EE devices for small single-phase induction motors used in residential/commercial motor drives used in water pumping, ventilation, air conditioning, compressors, and refrigeration applications. The GP-EM-EE devices are equipped with a dynamic online error-driven optimally tuned controller that ensures improved power factor, reduced feeder losses, stabilized voltage, minimal current ripples, and efficient energy utilization/conservation with minimal impact on the host electric grid security and reliability. The proposed schemes can enhance the power quality and extend induction motor life span by reducing overheating due to inrush currents and

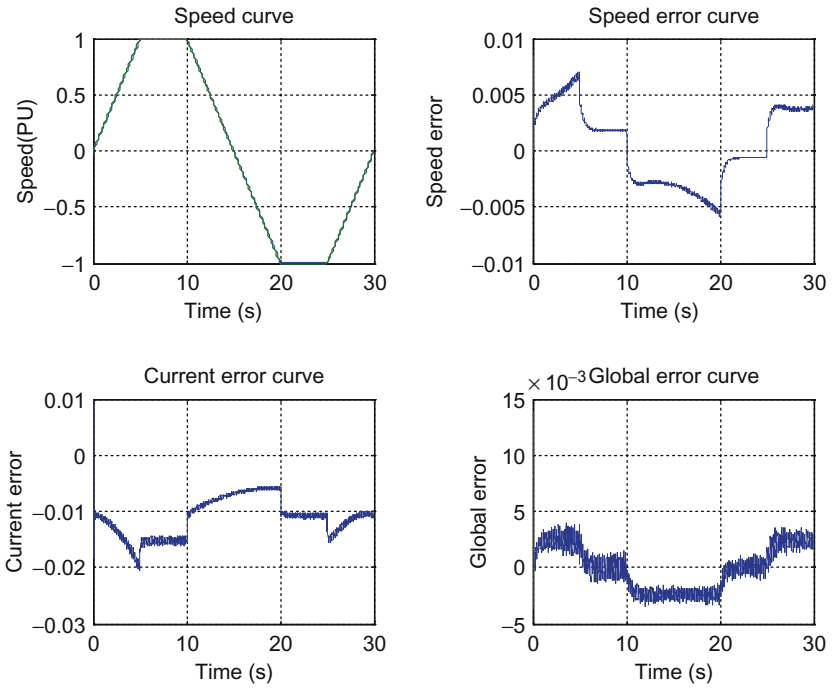


FIG. 38.34 EV-PMDC motor speed response for the first speed track using FLC-based controller.

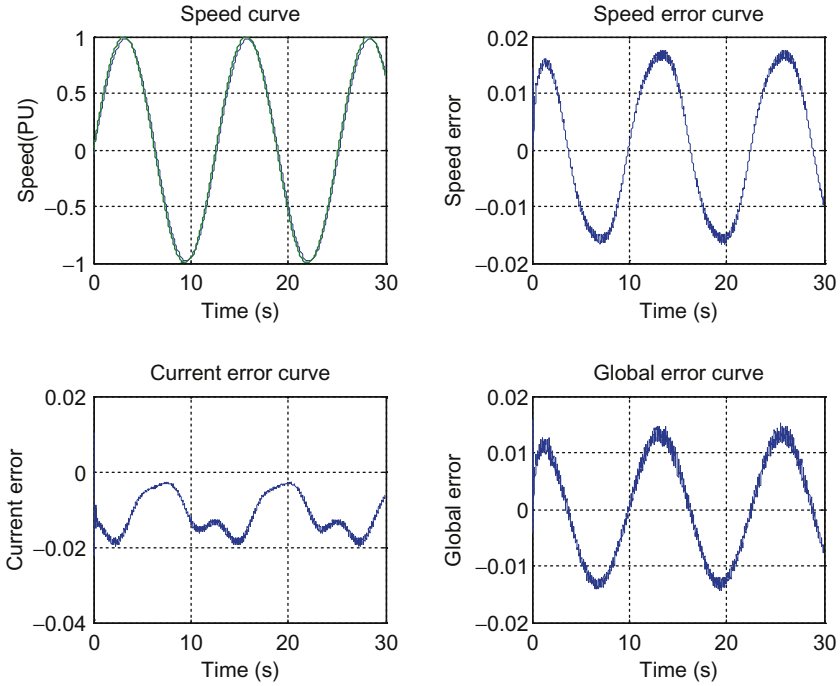


FIG. 38.35 EV-PMDC motor speed response for the second speed track using FLC-based controller.

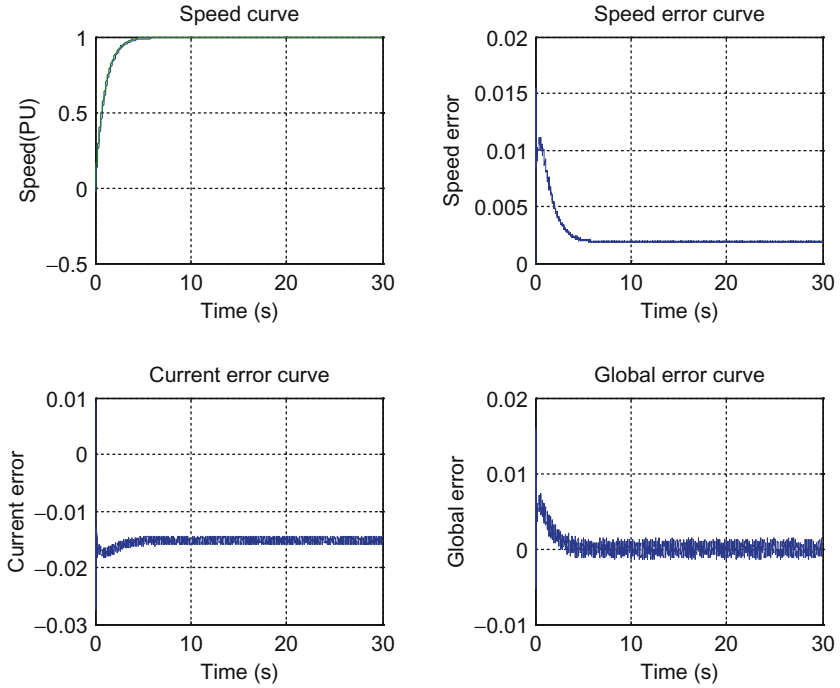


FIG. 38.36 EV-PMDC motor speed response for the third speed track using FLC-based controller.

harmonics. They prevent overheating and possible motor damage. The scheme is suitable for small-scale applications of wind energy utilization in the range from 5 to 25 kVA.

Wind energy conversion systems (WECS) are increasing their number as an environmentally friendly power generation system. Small-sized wind turbine systems in the output power range of 5–25 kVA to be used for the residential houses or small-sized business complex are extending their application fields. There are various advantages of the small-sized wind turbine system. The rotational speed of the smaller sized wind turbines can more rapidly follow the change of the wind speed than the large-scale wind turbines system due to their smaller inertia. This feature contributes higher power generation efficiency of the wind turbines in the case that the wind speed frequently changes [34]. Induction generators are being increasingly utilized in a WECS since they are relatively inexpensive, rigid, and require low maintenance [35]. Small-scale induction motor drives consume over 50% of the total electric energy generated in the developed countries [36]. The electric utility industry and consumers of electric energy around the world are facing new challenges for cutting electric energy cost, improving energy utilization, enhancing energy efficiency, demand-side management, improving supply waveform power quality, reducing safety hazards to personnel, and protecting sensitive computer and automatic data processing networks [37]. There is a mushrooming use of nonlinear electric loads especially in large motor drives, arc furnaces, and power electronic converter loads. All these nonlinear loads are by-products of analog (saturation or limiter-type) or digital (converter, solid-state switching-type) nonlinearities [38]. Nonlinear-type loads cause severe waveform distortion, power quality problem interference, and extra feeder losses due to excessive inrush currents and severe voltage sags. The extended use of power electronic switching conveners and devices in motor drives and process industries such as mining, oil, and gas industries and industrial DC and AC arc-type furnaces has resulted in a polluted grid and unreliable radial distribution/utilization system with serious inherent voltage and power quality problems [39]. These nonlinear-type electric loads are used with ventilation, air conditioning, water pumping, and low-power factor industries such as sewing, printing, shear and press machinery, and food processing plants. These nonlinear loads also fall in the category of inrush or arc-type motorized loads and combined with fluorescent lighting can cause waveform distortion, harmonic interference, and voltage flickering [40–42]. Generally, direct online motor starting is an economic method for starting induction motors. But direct starting will result in severe voltage sags and extra heating. When starting large induction motors, excessive voltage dips result in overheating and loss of motor life expectancy [43].

38.8.3.1 Sample Study Motorized System

Fig. 38.37 depicts the block diagram of the utilization (single-phase induction motor SPIM) and the connection of switched smart filter compensated device using green plug/energy management/energy economizer GP-EM-EE devices and the speed control drive system to the SPIM load. Figs. 38.38 and 38.39 show the proposed triloop dynamic tracking controller to ensure both objectives of (energy/power) saving and power quality enhancement of the supply system current and load bus voltage. The novel PSO and GA self-tuned multiregulators and coordinated controller are used for the following purposes: (1) green plug filter compensator GPFC-SPWM regulator for pulse-width switching scheme to regulate the DC bus voltage and minimize inrush current transients and load excursions and (2) the SPIM drive with the speed regulator that ensures speed reference tracking with minimum inrush conditions and ensure reduced voltage transients and improved energy

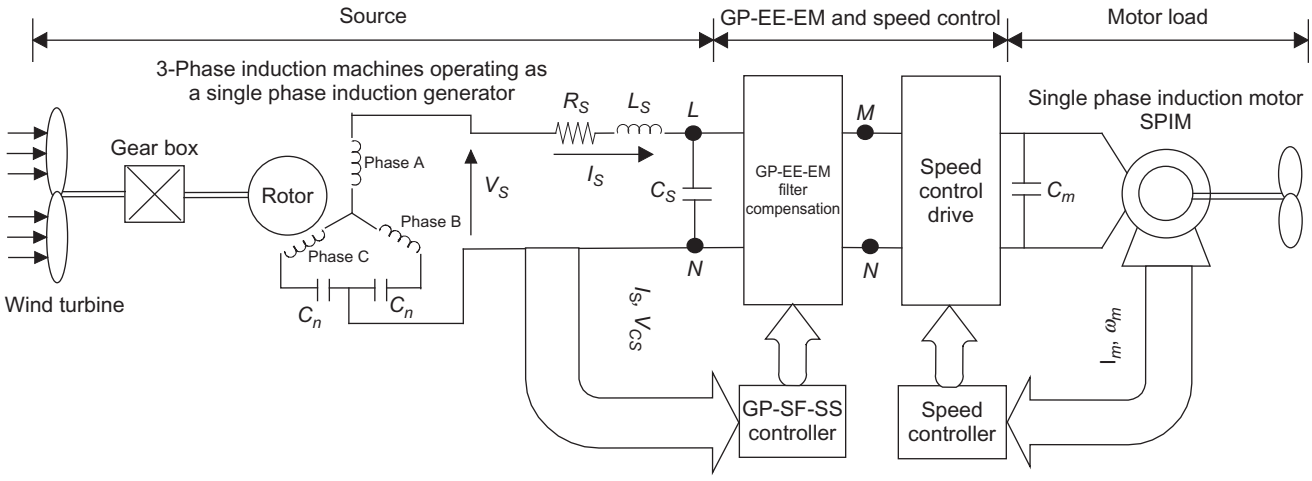


FIG. 38.37 The proposed switched smart filter compensated devices using green plug/energy management/energy economizer GP-EM-EE devices for single-phase induction motor SPIM drive system.

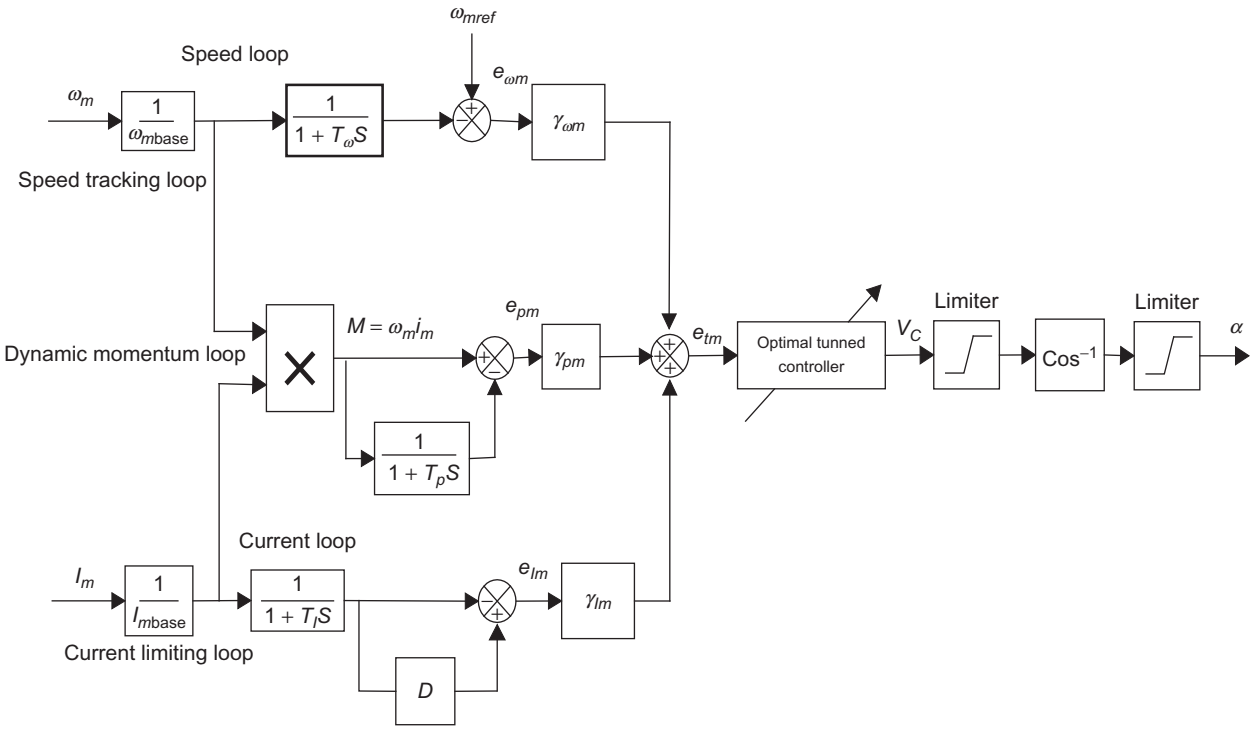


FIG. 38.38 Triloop error-driven self-regulating dynamic controller for control of single-phase induction motor SPIM drive.

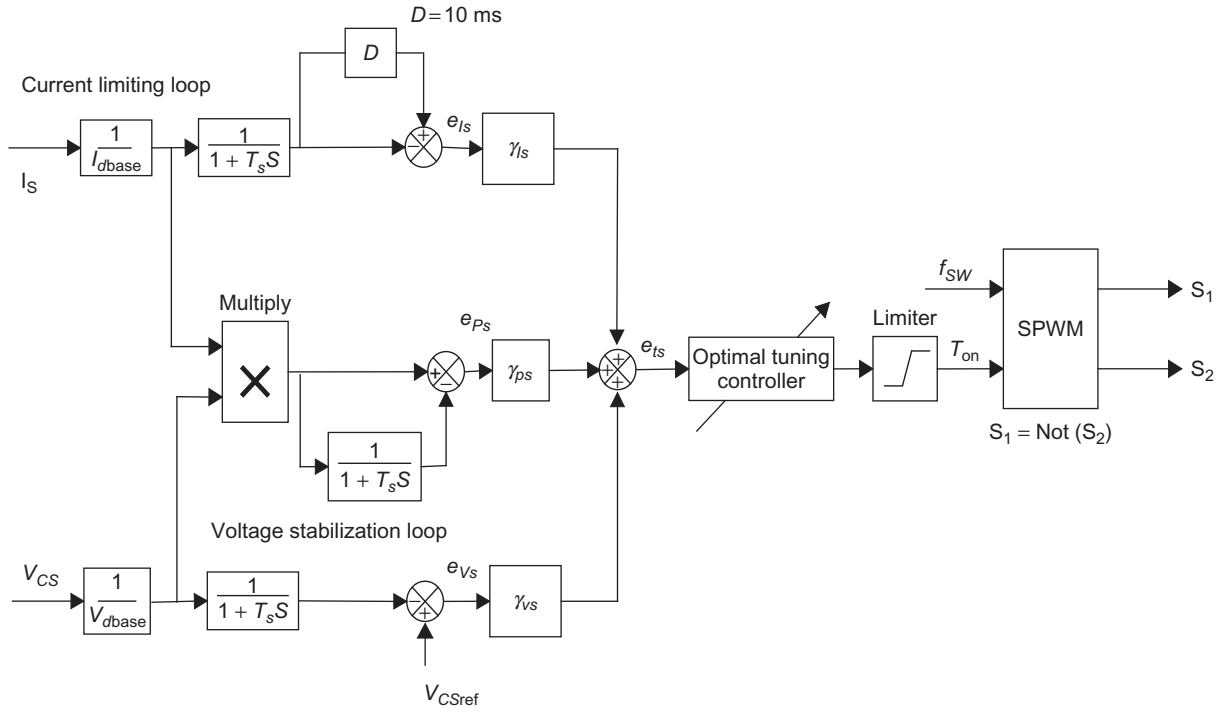


FIG. 38.39 Triloop error-driven self-regulating dynamic controller for the GP-EM-EE scheme.

utilization. Figs. 38.40–38.44 depict the proposed family of switched smart filter compensated devices using green plug/energy management/energy economizer GP-EM-EE devices. All filters objectives can be either (a) harmonic reduction and power quality (PQ) enhancement or (b) electric power/energy savings and dynamic reactive compensation for the single-phase induction motor loads. The proposed utilization scheme is fully validated using the Matlab/Simulink software environment under normal conditions, load excursion, SPIM

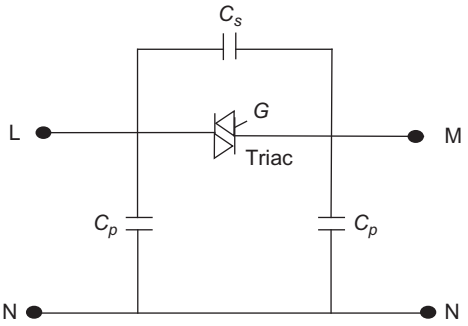


FIG. 38.40 Low-cost switched power filter compensator Scheme A.

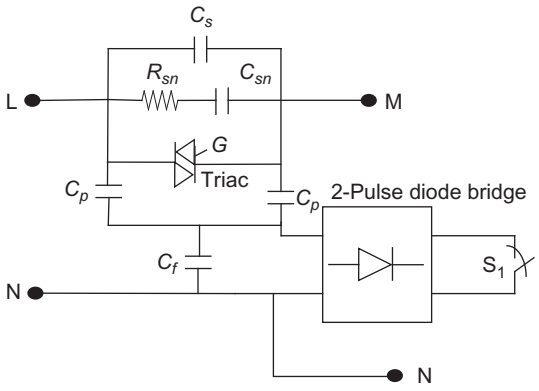


FIG. 38.41 Low-cost switched power filter compensator Scheme B.

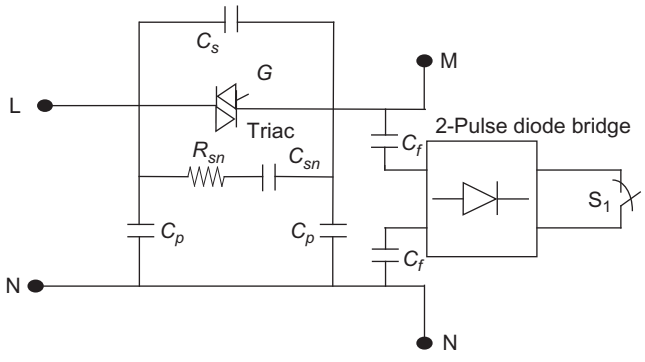


FIG. 38.42 Low-cost switched power filter compensator Scheme C.

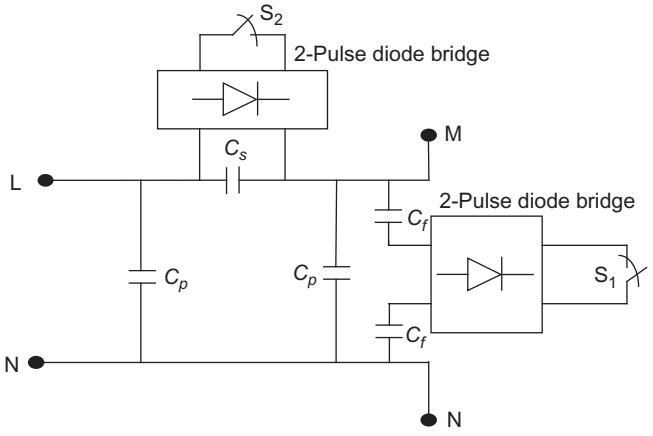


FIG. 38.43 Low-cost switched power filter compensator Scheme D.

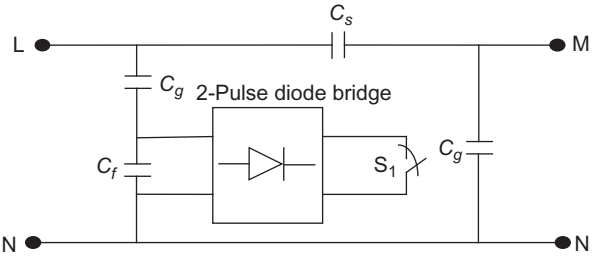


FIG. 38.44 Low-cost switched power filter compensator Scheme E.

motor torque changes to assess the control system robustness, effective energy utilization, and speed reference tracking.

The common concerns of power quality are the long-duration voltage variations (overvoltage, undervoltage, and sustained interruptions), short-duration voltage variations (interruption, sags, and swells), voltage imbalance (voltage unbalance), waveform distortion (DC offset, harmonics, inter-harmonics, notching, and noise), voltage fluctuation (voltage flicker), and power frequency variations. To prevent the undesirable states and to reduce the power consumption, a GPF scheme is used to stabilize the system.

Dynamic error driven control

The proposed control system comprises two subregulators or controllers named as DC side green plug filter compensator GPFC-SPWM regulator and the SPIM drive speed controller. Figs. 38.38 and 38.39 depict the proposed multiloop dynamic self-regulating controllers based on multiobjective optimization search and optimization technique based on soft computing PSO and GA. The global error is the summation of the three loop individual errors including voltage stability, current limiting, and synthesize dynamic power loops. Each multiloop dynamic control scheme is used to reduce a global error based on a triloop dynamic error summation signal and to mainly track a given speed reference trajectory loop error in addition

to other supplementary motor current limiting, and dynamic power loops are used as auxiliary loops to generate a dynamic global total error signal that consists of not only the main loop speed error but also the current ripple, overcurrent limit, and dynamic over load power conditions.

The global error signal is input to the self-tuned controllers shown in Fig. 38.38. The (per unit) three-dimensional-error vector (e_{vs}, e_{Is}, and e_{ps}) of the diesel engine controller scheme is governed by the following equations:

$$e_{vs}(k) = V_s(k)\left(\frac{1}{1+ST_s}\right)\left(\frac{1}{1+SD}\right) - V_s(k)\left(\frac{1}{1+ST_s}\right) \tag{38.47}$$

$$e_{Is}(k) = I_s(k)\left(\frac{1}{1+ST_s}\right)\left(\frac{1}{1+SD}\right) - I_s(k)\left(\frac{1}{1+ST_s}\right) \tag{38.48}$$

$$\begin{aligned} e_{Ps}(k) = {} & I_s(k) \times V_s(k)\left(\frac{1}{1+ST_s}\right)\left(\frac{1}{1+SD}\right) \\ & - I_s(k) \times V_s(k)\left(\frac{1}{1+ST_g}\right) \end{aligned} \tag{38.49}$$

The total or global error $e_{ts}(k)$ for the GP-EM-EE side scheme at a time instant

$$e_{ts}(k) = \gamma_{vs} e_{vs}(k) + \gamma_{is} e_{is}(k) + \gamma_{ps} e_{ps}(k) \tag{38.50}$$

In the same manner, the (per unit) three-dimensional-error vector ($e_{\omega m}$, e_{Im}, and e_{pm}) of the SPIM motor scheme is governed by the following equations:

$$e_{\omega m}(k) = \omega_m(k)\left(\frac{1}{1+ST_m}\right)\left(\frac{1}{1+SD}\right) - \omega_m(k)\left(\frac{1}{1+ST_m}\right) \tag{38.51}$$

$$e_{Im}(k) = I_m(k)\left(\frac{1}{1+ST_m}\right)\left(\frac{1}{1+SD}\right) - I_m(k)\left(\frac{1}{1+ST_m}\right) \tag{38.52}$$

$$\begin{aligned} e_{Pm}(k) = {} & I_m(k) \times \omega_m(k)\left(\frac{1}{1+ST_m}\right)\left(\frac{1}{1+SD}\right) \\ & - I_m(k) \times \omega_m(k)\left(\frac{1}{1+ST_m}\right) \end{aligned} \tag{38.53}$$

and the total or global error $e_{tm}(k)$ for the MPFC scheme at a time instant

$$e_{tm}(k) = \gamma_{\omega m} e_{\omega m}(k) + \gamma_{im} e_{im}(k) + \gamma_{pm} e_{pm}(k) \tag{38.54}$$

A number of conflicting objective functions are selected to optimize using the PSO algorithm. These functions are defined by the following:

$$J_1 = \text{Minimize the total harmonic distortion of the load current } (THDi) \tag{38.55}$$

$$J_2 = \text{Minimize the total harmonic distortion of the load voltage } (THDv) \tag{38.56}$$

$$J_3 = \text{Maximize the electric energy efficiency} \tag{38.57}$$

$$J_4 = \text{Maximize the power factor} \tag{38.58}$$

$$J_5 = \text{Minimize the KWh consumption} \tag{38.59}$$

In general, to solve this complex optimality search problem, there are two possible optimization techniques based on particle swarm optimization (PSO): single aggregate selected objective optimization (SOO), which is explained, and multiobjective optimization (MOO). The main procedure of the SOO is based on selecting a single aggregate objective function with weighted single-objective parameters scaled by a number of weighting factors. The objective function is optimized (either minimized or maximized) using either GA or particle swarm optimization search algorithm (PSO) methods to obtain a single global or near-optimal solution. On the other hand, the main objective of the multiobjective (MO) problem is finding the set of acceptable (trade-off) optimal solutions. This set of accepted solutions is called Pareto front. These acceptable trade-off multilevel solutions give more ability to the user to make an informed decision by seeing a wide range of near-optimal selected solutions that are feasible and acceptable from an "overall" standpoint. Single-objective (SO) optimization may ignore this trade-off viewpoint, which is crucial. The main advantages of the proposed MOO method are the following: It doesn't require a priori knowledge of the relative importance of the objective functions, and it provides a set of acceptable trade-off near-optimal solutions. This set is called Pareto front or optimality trade-off surfaces. Both SOO and MOO searching algorithms are tested, validated, and compared.

The dynamic error-driven controller regulates the controllers' gains using the particle swarm optimization (PSO) and GA to minimize the system total error and the selected objective functions. The proposed dynamic triloop error-driven controller, developed by the first author, is a novel advanced regulation concept that operates as an adaptive dynamic-type multipurpose controller capable of handling sudden parametric changes, load and/or source excursions. By using the triloop error-driven controller, it is expected to have a smoother, less dynamic overshoot and fast and more robust controller when compared with those of classical control schemes.

Self tuned conventional PID controller

Fundamentally, the conventional PID controller comprises three basic control actions. They are simple to implement and they provide good performance. The tuning process of the gains of PID controllers can be complex because it is iterative: first, it is necessary to tune the "proportional" mode, then the "integral," and then add the "derivative" mode to stabilize

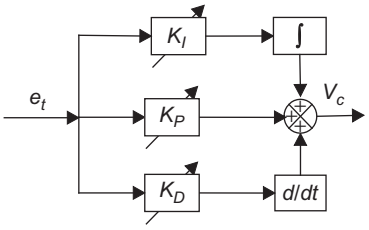


FIG. 38.45 Optimally tuned conventional PID controller block diagram.

the overshoot, then add more "proportional," and so on. The PID controller has the following form in the time domain as shown in Fig. 38.45:

$$u(t) = K_p e(t) + K_i \int_0^t e(t)\,dt + K_d \frac{de(t)}{dt} \tag{38.60}$$

where $e(t)$ is the selected system error, $u(t)$ the control variable, K_p the proportional gain, K_i the integral gain, and K_d is the derivative gain. Each coefficient of the PID controller adds some special characteristics to the output response of the system. Because of this, choosing the right parameters becomes a crucial decision. In this scheme, the triloop error-driven controller is utilized with traditional PID controller. PID controller gains (K_P, K_I, and K_D) are dynamically self-tuned using the PSO and GA dynamic search and optimization criterion based on total error minimization, steady-state error, maximum overshoot, and settling time and rising time.

38.8.3.2 Digital Simulation Results

The family of (GP-EM-EE) devices system performance is compared for two cases; with (as shown in Table 38.12) and without the (GP-EM-EE) devices, the second case is studied with fixed (as shown in Table 38.13) and self-tuned-type controllers using either GA or PSO. In addition, the second case is studied to compare the performance with artificial neural network (ANN) controller (as shown in Table 38.14) and fuzzy logic controller (FLC) (as shown in Table 38.15) with the self-tuned-type controllers using either GA or PSO. The self-tuned-type controllers based either GA or PSO is tuned conventional PID controller and has been applied to the speed tracking control of the same system parameters for performance comparison. Matlab/Simulink software was used to design, test, and validate the effectiveness of the (GP-EM-EE) devices for small motors used in household appliances, washers, dryers, fans, water pumps, ventilation systems, air conditions, and other applications in dispersing machines, actuators, and small converters with induction motor size from 5 to 25 kVA. The digital dynamic simulation model using Matlab/Simulink software environment allows for low-cost assessment and prototyping, system parameter selection, and optimization of control settings. The use of GA and PSO search algorithms is utilized in online gain adjusting to minimize

TABLE 38.12 System behavior without (GP-EM-EE) schemes

	Without (GP-EM-EE)
RMS motor voltage (pu)	0.8578
RMS motor current (pu)	0.8724
Maximum transient voltage over/undershoot (pu)	0.1797
Maximum transient current—over/undershoot (pu)	0.1875
System efficiency	0.7853
NMSE_V	0.4672
*NMSE_*ω_m	0.6476
NMSE_I	0.4238
THDv_Bus L (%)	19.647
THDi_Bus L (%)	20.346
THDv_Bus M (%)	21.675
THDi_Bus M (%)	19.564
Motor power factor	0.7167

TABLE 38.13 System dynamic behavior comparison using the constant parameters conventional PID controller

	GP-EM-EE scheme A	GP-EM-EE scheme B	GP-EM-EE scheme C	GP-EM-EE scheme D	GP-EM-EE scheme E
RMS motor voltage (pu)	0.9762	0.9609	0.9575	0.9735	0.9690
RMS Motor current (pu)	0.7029	0.7008	0.6743	0.7032	0.6821
Maximum transient voltage over/undershoot (pu)	0.0905	0.0734	0.0729	0.0880	0.0846
Maximum transient current—over/undershoot (pu)	0.0701	0.0671	0.0884	0.0716	0.0740
NMSE_V	0.0828	0.0737	0.0781	0.0683	0.0907
*NMSE_*ω_m	0.0809	0.0770	0.0793	0.0749	0.0773
NMSE_I	0.0722	0.0808	0.0852	0.0796	0.0823
THDv_Bus L (%)	7.8228	9.0412	8.7138	8.9321	9.5253
THDi_Bus L (%)	7.3532	8.3315	9.5150	7.7711	9.5659
THDv_Bus M (%)	8.0566	9.4304	9.1032	8.9371	9.2456
THDi_Bus M (%)	10.8589	8.4421	8.6837	8.3050	8.7230
System efficiency	0.8577	0.8749	0.9080	0.9186	0.8579
Motor power factor	0.9082	0.8957	0.8919	0.8721	0.9083
Reduction in kWh consumption (%)	14.4937	14.6854	12.2181	12.6337	12.7710

TABLE 38.14 System dynamic behavior comparison using ANN controller

	GP-EM-EE Scheme A	GP-EM-EE Scheme B	GP-EM-EE Scheme C	GP-EM-EE Scheme D	GP-EM-EE Scheme E
RMS motor voltage (pu)	0.9790	0.9713	0.9620	0.9723	0.9719
RMS motor current (pu)	0.6837	0.6944	0.6839	0.6887	0.7077
Maximum transient voltage over/undershoot (pu)	0.0769	0.0873	0.0795	0.0717	0.0830
Maximum transient current—over/undershoot (pu)	0.0871	0.0673	0.0833	0.0760	0.0869
NMSE_V	0.0790	0.0840	0.0772	0.0742	0.0714
*NMSE_*ω_m	0.0715	0.0833	0.0741	0.0799	0.0704
NMSE_I	0.0837	0.0759	0.0876	0.0874	0.0811
THDv_Bus L (%)	10.4023	7.7359	8.6519	9.1624	9.9567
THDi_Bus L (%)	9.3573	8.9212	8.8588	7.4199	8.8514
THDv_Bus M (%)	8.5408	8.2842	10.4948	10.1231	10.8888
THDi_Bus M (%)	9.3120	7.1241	9.4659	10.3514	10.9988
System efficiency	0.8943	0.9163	0.8749	0.9125	0.8632
Motor power factor	0.8609	0.8715	0.9153	0.8607	0.8734
Reduction in kWh consumption (%)	12.3129	12.0158	14.3858	13.4017	11.8366

TABLE 38.15 System dynamic behavior comparison using the FLC controller

	GP-EM-EE scheme A	GP-EM-EE scheme B	GP-EM-EE scheme C	GP-EM-EE scheme D	GP-EM-EE scheme E
RMS motor voltage (pu)	0.9598	0.9573	0.9627	0.9594	0.9584
RMS motor current (pu)	0.6863	0.6893	0.6917	0.6893	0.6929
Maximum transient voltage over/under shoot (pu)	0.0788	0.0886	0.0867	0.0824	0.0866
Maximum transient current—over/undershoot (pu)	0.0828	0.0751	0.0738	0.0750	0.0797
NMSE_V	0.0844	0.0743	0.0871	0.0805	0.0757
*NMSE_*ω_m	0.0838	0.0800	0.0775	0.0836	0.0818
NMSE_I	0.0860	0.0899	0.0794	0.0881	0.0710
THDv_Bus L (%)	8.2175	8.6528	9.0910	9.9722	8.2990
THDi_Bus L (%)	7.5181	8.8507	8.9451	7.1258	9.7391
THDv_Bus M (%)	9.9806	8.2001	8.1204	9.9178	10.2212
THDi_Bus M (%)	11.0353	8.9716	10.6999	8.8819	10.3043
System efficiency	0.9195	0.8701	0.8880	0.8750	0.8990
Motor power factor	0.9169	0.9049	0.8986	0.8650	0.8628
Reduction in kWh consumption (%)	11.4634	11.4088	13.0202	13.8055	12.4766

controller absolute value of total error. This is required before full-scale prototyping that is both expensive and time-consuming. The effectiveness of dynamic simulators brings on detailed submodels selections and tested submodels Matlab library of power system components already tested and validated. The dynamic simulation conditions are identical for all tuned controllers. To compare the global performances of tuned conventional PID controller, the normalized mean-square-error (*NMSE*) deviations between output plant variables and desired values and is defined as

$$\mathrm{NMSE}_{V_S} = \frac{\sum (V_S - V_{S-\mathrm{ref}})^2}{\sum (V_{S-\mathrm{ref}})^2} \tag{38.34}$$

$$\mathrm{NMSE}_{\omega_m} = \frac{\sum (\omega_m - \omega_{m-\mathrm{ref}})^2}{\sum (\omega_{m-\mathrm{ref}})^2} \tag{38.35}$$

$$\mathrm{NMSE}_{I_s} = \frac{\sum (I_S - I_{S-\mathrm{ref}})^2}{\sum (I_{S-\mathrm{ref}})^2} \tag{38.36}$$

The control system comprises the three dynamic multiloop error-driven regulator is coordinated to minimize the selected objective functions. SOO obtains a single global or near-optimal solution based on a single-weighted-objective function. The weighted single-objective function combines several objective functions using specified or selected weighting factors as follows:

$$\text{weighted objective function} = \alpha_1 J_1 + \alpha_2 J_2 + \alpha_3 J_3 + \alpha_4 J_4 + \alpha_5 J_5 \tag{38.37}$$

where $\alpha_1 = 0.20$, $\alpha_2 = 0.20$, $\alpha_3 = 0.20$, $\alpha_4 = 0.20$, and $\alpha_5 = 0.20$ are selected weighting factors. J_1, J_2, J_3, J_4, and J_5 are the selected

objective functions. On the other hand, the MO finds the set of acceptable (trade-off) optimal solutions. This set of accepted solutions is called Pareto front. These acceptable trade-off multilevel solutions give more ability to the user to make an informed decision by seeing a wide range of near-optimal selected solutions. Table 38.16 shows the system behavior using traditional controllers with constant controller gains for the (GP-EM-EE) schemes. In addition, Table 38.10 shows system behavior comparison using the SOGA-based tuned conventional PID controller, and Table 38.17 shows the system behavior comparison using the MOGA-based tuned conventional PID controller. Finally, Tables 38.18 and 38.19) show system behavior comparison using the SOPSO- and MOPSO-based tuned conventional PID controller, respectively. Comparing the system dynamic response results of the two study cases, with GA and PSO tuning algorithms and traditional controllers with constant controller gain results, ANN controller and FLC, it is quite apparent that the GA and PSO tuning algorithms highly improved the system dynamic performance from a general power quality point of view. The GA and PSO tuning algorithms had a great impact on motor RMS voltage (pu) improving it from 0.8578 (without the (GP-EM-EE) device), 0.9762 (constant gains controller), 0.9790 (ANN controller), and 0.9598 (FLC) to around 0.9804 (SOGA-based tuned controller), 0.9865 (MOGA-based tuned controller), 0.9887 (SOPSO)-based tuned controller, and 0.9852 (MOPSO-based tuned controller). Motor RMS current (pu) is reduced from 0.8724 (without the (GP-EM-EE) device), 0.7029 (constant gains controller), 0.6837 (ANN controller), and 0.6863 (FLC) to around 0.6247 (SOGA-based tuned controller), 0.6304 (MOGA-based tuned controller), 0.6358 (SOPSO)-based tuned controller, and 0.6471 (MOPSO-based tuned controller). Maximum transient motor voltage over/undershoot (pu) is reduced from 0.1797 (without the (GP-EM-EE) device),

TABLE 38.16 System dynamic behavior comparison using the SOGA-based tuned conventional PID controller

	GP-EM-EE scheme A	GP-EM-EE scheme B	GP-EM-EE scheme C	GP-EM-EE scheme D	GP-EM-EE scheme E
RMS motor voltage (pu)	0.9804	0.9810	0.9944	0.9922	0.9799
RMS motor current (pu)	0.6247	0.6237	0.6448	0.6473	0.6428
Maximum transient voltage over/undershoot (pu)	0.0472	0.0569	0.0565	0.0494	0.0380
Maximum transient current—over/undershoot (pu)	0.0431	0.0509	0.0403	0.0542	0.0495
$NMSE_V \times 10^{-1}$	0.0396	0.0591	0.0408	0.0359	0.0531
$NMSE_\omega_m \times 10^{-1}$	0.0458	0.0453	0.0585	0.0595	0.0477
$NMSE_I \times 10^{-1}$	0.0361	0.0564	0.0371	0.0380	0.0533
THDv_Bus L (%)	6.2535	5.8337	3.9023	6.1560	4.7221
THDi_Bus L (%)	4.1530	5.3045	6.4754	4.9912	5.3056
THDv_Bus M (%)	5.7887	3.6631	6.2107	6.3719	3.7171
THDi_Bus M (%)	3.9572	4.7990	6.6102	5.5482	5.7022
System efficiency	95.4132	92.3235	94.2164	95.4236	93.5954
Motor power factor	95.1040	94.4444	92.5749	94.3228	91.4794
Reduction in kWh consumption (%)	18.3913	16.2849	15.9924	18.9718	17.9797

TABLE 38.17 System dynamic behavior comparison using a selected solution from the MOGA Pareto front-based tuned conventional PID controller

	GP-EM-EE scheme A	GP-EM-EE scheme B	GP-EM-EE scheme C	GP-EM-EE scheme D	GP-EM-EE scheme E
RMS motor voltage (pu)	0.9865	0.9775	0.9790	0.9767	0.9939
RMS motor current (pu)	0.6304	0.6289	0.6477	0.6338	0.6252
Maximum transient voltage over/undershoot (pu)	0.0394	0.0371	0.0373	0.0539	0.0365
Maximum transient current—over/undershoot (pu)	0.0533	0.0413	0.0515	0.0486	0.0502
$NMSE_V \times 10^{-1}$	0.0429	0.0582	0.0380	0.0431	0.0564
$NMSE_\omega_m \times 10^{-1}$	0.0608	0.0374	0.0603	0.0590	0.0599
$NMSE_I \times 10^{-1}$	0.0499	0.0597	0.0437	0.0424	0.0372
THDv_Bus L (%)	4.8408	6.6094	3.8605	4.6237	4.0436
THDi_Bus L (%)	4.0103	4.1585	3.9436	5.2812	5.9842
THDv_Bus M (%)	4.9313	6.2074	6.1134	3.6848	5.6249
THDi_Bus M (%)	3.9998	4.3153	6.4326	4.0984	4.2902
System efficiency	95.4882	91.6483	94.5787	93.7556	91.4767
Motor power factor	90.8137	92.1151	95.5633	95.4594	91.8090
Reduction in kWh consumption (%)	16.5388	16.5127	19.0189	20.4335	15.4505

TABLE 38.18 System dynamic behavior comparison using the SOPSO-based tuned conventional PID controller

	GP-EM-EE scheme A	GP-EM-EE scheme B	GP-EM-EE scheme C	GP-EM-EE Scheme D	GP-EM-EE scheme E
RMS motor voltage (pu)	0.9887	0.9831	0.9901	0.9806	0.9809
RMS motor current (pu)	0.6358	0.6449	0.6456	0.6486	0.6446
Maximum transient voltage over/undershoot (pu)	0.0441	0.0431	0.0458	0.0365	0.0429
Maximum transient current—over/undershoot (pu)	0.0412	0.0500	0.0577	0.0421	0.0506
$NMSE_V \times 10^{-1}$	0.0489	0.0389	0.0358	0.0439	0.0448
$NMSE_\omega_m \times 10^{-1}$	0.0608	0.0594	0.0466	0.0593	0.0482
$NMSE_I \times 10^{-1}$	0.0602	0.0599	0.0539	0.0521	0.0575
THDv_Bus L (%)	4.2581	5.2727	5.1959	5.1325	4.8095
THDi_Bus L (%)	5.2433	6.1471	4.2937	4.8437	3.7976
THDv_Bus M (%)	4.5873	6.1412	5.7390	6.3506	3.9065
THDi_Bus M (%)	5.1673	4.9705	4.7114	6.4459	4.1457
System efficiency	95.4999	94.0919	90.9345	93.6876	92.6432
Motor power factor	91.7450	91.5784	91.0446	90.6943	94.6423
Reduction in kWh consumption (%)	15.9691	18.6019	14.9762	16.0446	18.6966

TABLE 38.19 System dynamic behavior comparison using a selected solution from the MOPSO Pareto front-based tuned conventional PID controller

	GP-EM-EE Scheme A	GP-EM-EE Scheme B	GP-EM-EE Scheme C	GP-EM-EE Scheme D	GP-EM-EE Scheme E
RMS motor voltage (pu)	0.9852	0.9830	0.9816	0.9915	0.9847
RMS motor current (pu)	0.6471	0.6407	0.6249	0.6353	0.6278
Maximum transient voltage over/undershoot (pu)	0.0365	0.0449	0.0380	0.0441	0.0359
Maximum transient current—over/undershoot (pu)	0.0563	0.0363	0.0464	0.0365	0.0528
$NMSE_V \times 10^{-1}$	0.0440	0.0498	0.0464	0.0395	0.0373
$NMSE_\omega_m \times 10^{-1}$	0.0513	0.0516	0.0401	0.0460	0.0535
$NMSE_I \times 10^{-1}$	0.0465	0.0410	0.0506	0.0568	0.0581
THDv_Bus L (%)	4.1081	4.1093	5.6076	3.9418	6.4921
THDi_Bus L (%)	5.1378	4.1551	4.5004	4.0566	3.7277
THDv_Bus M (%)	4.3629	6.2371	5.8741	5.7775	4.8263
THDi_Bus M (%)	5.1216	6.6090	6.0487	4.9076	6.5793
System efficiency	90.7467	95.0928	92.4381	94.3056	95.5501
Motor power factor	91.4433	91.4801	92.2403	90.8052	92.4638
Reduction in kWh consumption (%)	16.5328	16.2839	17.9038	15.6451	15.9338

0.0905 (constant gains controller), 0.0769 (ANN controller), and 0.0788 (FLC) to around 0.0472 (SOGA-based tuned controller), 0.0394 (MOGA-based tuned controller), 0.0441 (SOPSO)-based tuned controller, and 0.0365 (MOPSO-based tuned controller). Maximum transient motor current – over/undershoot (pu) is reduced from 0.1875 (without the (GP-EM-EE) device), 0.0701 (constant gains controller), 0.0871 (ANN controller), and 0.0828 (FLC) to around 0.0431 (SOGA-based tuned controller), 0.0533 (MOGA-based tuned controller), 0.0412 (SOPSO)-based tuned controller, and 0.0563 (MOPSO-based tuned controller). Moreover, the normalized mean square error (*NMSE_V*) of the motor voltage is reduced from 0.4672 (without the (GP-EM-EE) device), 0.0828 (constant gains controller), 0.0790 (ANN controller), and 0.0844 (FLC) to around 0.00396 (SOGA-based tuned controller), 0.00429 (MOGA-based tuned controller), 0.00489 (SOPSO)-based tuned controller, and 0.00440 (MOPSO-based tuned controller). In addition, the ($NMSE_\omega_m$) of the SPIM motor is reduced from 0.6476 (without the (GP-EM-EE) device), 0.0809 (constant gains controller), 0.0715 (ANN controller), and 0.0838 (FLC) to around 0.00458 (SOGA-based tuned controller), 0.00608 (MOGA-based tuned controller), 0.00608 (SOPSO)-based tuned controller, and 0.00513 (MOPSO-based tuned controller). The (*NMSE_I*) of the motor current is reduced from 0.4238 (without the (GP-EM-EE) device), 0.0722 (constant gains controller), 0.0837 (ANN controller), and 0.0860 (FLC) to around 0.00361 (SOGA-based tuned controller), 0.00499 (MOGA-based tuned controller), 0.00602 (SOPSO)-based tuned controller, and 0.00465 (MOPSO-based tuned controller). Total

harmonic distortion (THD) (%) of the supply voltage is reduced from 19.647 (without the (GP-EM-EE) device), 7.8228 (constant gains controller), 10.4023 (ANN controller), and 8.2175 (FLC) to around 6.2535 (SOGA-based tuned controller), 4.8408 (MOGA-based tuned controller), 4.2581 (SOPSO)-based tuned controller, and 4.1081 (MOPSO-based tuned controller). THD (%) of the supply current is reduced from 20.346 (without the (GP-EM-EE) device), 7.3532 (constant gains controller), 9.3573 (ANN controller), and 7.5181 (FLC) to around 4.1530 (SOGA-based tuned controller), 4.0103 (MOGA-based tuned controller), 5.2433 (SOPSO)-based tuned controller, and 5.1378 (MOPSO-based tuned controller). THD (%) of the motor voltage is reduced from 21.675 (without the (GP-EM-EE) device), 8.0566 (constant gains controller), 8.5408 (ANN controller), and 9.9806 (FLC) to around 5.7887 (SOGA-based tuned controller), 4.9313 (MOGA-based tuned controller), 4.5873 (SOPSO)-based tuned controller, and 4.3629 (MOPSO-based tuned controller). THD (%) of the motor current is reduced from 21.675 (without the (GP-EM-EE) device), 10.8589 (constant gains controller), 9.3120 (ANN controller), and 11.0353 (FLC) to around 3.9572 (SOGA-based tuned controller), 3.9998 (MOGA-based tuned controller), 5.1673 (SOPSO)-based tuned controller, and 5.1216 (MOPSO-based tuned controller). The system efficiency is improved from 0.7853 (without the (GP-EM-EE) device), 0.8577 (constant gains controller), 0.8943 (ANN controller), and 0.9195 (FLC) to around 95.4132 (SOGA-based tuned controller), 95.4882 (MOGA-based tuned controller), 95.4999 (SOPSO)-based tuned controller, and 90.7467 (MOPSO-based tuned controller). Motor power factor is improved from 0.7167 (without the (GP-EM-EE) device), 0.9082 (constant gains controller), 0.8609 (ANN controller), and 0.9169 (FLC) to around 95.1040 (SOGA-based tuned controller), 90.8137 (MOGA-based tuned controller), 91.7450 (SOPSO)-based tuned controller, and 91.4433 (MOPSO-based tuned controller). Reduction in kWh consumption (%) is reduced from 0.000 (without the (GP-EM-EE) device), 14.4937 (constant gains controller), 12.3129 (ANN controller), and 11.4634 (FLC) to around 18.3913 (SOGA-based tuned controller), 16.5388 (MOGA-based tuned controller), 15.9691 (SOPSO)-based tuned controller, and 16.5328 (MOPSO-based tuned controller).

The application validated the operation of a novel wind-driven squirrel cage induction generator fed from single-phase supply. The scheme utilizes a simple but effective series-parallel switched capacitor filter to ensure dynamic terminal voltage stabilization, effective energy utilization, and minimal impact of electric load switching and dynamic excursions and wind velocity changes. The novel error-driven self-regulating multiloop dynamic controller utilizes random search optimization algorithms using particle swarm optimization (PSO) and GA to continuously search for effective and optimized controllers gains that can cope with specified objective function restrictions of minimum voltage deviations, limited generated current and power excursions due to terminal load changes, and wind velocity excursions and gusting. The application presents a family of novel low-cost green plug electricity saving devices/energy management/energy economizer (GP-EM-EE) devices equipped with a dynamic online error-driven optimally tuned controller. The (GP-EM-EE) are small low-cost energy conservation devices in the form add-on dynamic switched capacitor filter compensator schemes for low horsepower motors used in household appliances, washers, dryers, fans, water pumps, ventilation systems, air conditioners, and other cyclic motorized loads used in dispersing machines, actuators, and small converters with induction motor size from 5 to 25 kVA. The (GP-EM-EE) devices family can be used with all types of small horsepower motors with billions of small motors used in multitude of applications that consumes over 50%–60% of total electric energy generated in the world. The (GP-EM-EE) device can save 10–20% of the electricity cost of operating the small motor over the estimated motor life span of 7–10 years. This translates into millions of dollars in daily electricity savings, reduced electric utility overloading conditions, blackouts, brownouts, and enhanced, secure, and reliable operation with additional sizable power capacity release due to reduced electric demand and feeder losses.

38.9 Conclusion

The chapter covers novel techniques for the dynamic control of industrial motor drives. The use of AI soft computing PSO and GA random search techniques is presented. The specific use of PSO and GA single-objective and multiobjective controller optimization and dynamic gains adjusting is illustrated using three key applications of optimal operation of induction motor drives, hybrid photovoltaic-fuel cell-diesel-battery electric vehicle drive system, and finally, the novel self-regulating green plug-energy management energy economizer schemes developed by the first author as a number of an extended family of modulated power filters, switched capacitor compensators, and dynamic electric energy management devices and system. The control strategies are all based on multiloop error-driven regulation with online dynamic gain adjusting based on PSO and GA search algorithm. The use of AI self-regulating dynamic controllers based on AI soft computing allows meeting a multitude of conflicting objective functions of effective speed reference tracking, minimal losses, efficient utilization, limited inrush currents under parametric variations, supply source excursions, inertia, and mechanical load nonlinear loads. The other added benefit is targeting the use of power electronic devices and switched capacitor compensator/filters in ensuring efficient operation of motors and motor drives especially in future applications using renewable and green energy system.

References

[1] V.G. Gudise, G.K. Venayagamoorthy, Evolving digital circuits using particle swarm, Proceedings of the International Joint Conference on Neural Networks, vol. 1, 20–24 July 1 (2003) 468–472.

[2] L. Davis, Handbooks of Genetic Algorithm, Van Nostrand, Reinhold, New York, 1991.

[3] J. Kennedy, R. Eberhart, Particle swarm optimization, in: Proceedings, IEEE International Conf. on Neural Networks, vol. 4, 1995, pp. 1942–1948.

[4] Y. Shi, R. Eberhart, Empirical study of particle swarm optimization, in: Proceedings of the 1999 Congress on Evolutionary Computation, vol. 3, 1999.

[5] Y. Shi, R. Eberhart, A modified particle swarm optimizer, in: IEEE International Conference on Evolutionary Computation, 1998, pp. 69–73.

[6] R. Eberhart, Y. Shi, Particle swarm optimization: developments, applications and resources, in: Proceedings of the 2001 Congress on Evolutionary Computation, vol. 1, 2001, pp. 81–86.

[7] Y. Shi, R. Eberhart, Parameter selection in particle swarm optimization, in: Proceedings of Seventh Annual Conference on Evolutionary Programming, 1998, pp. 591–601.

[8] Y. Fukuyama, et al., A particle swarm optimization for reactive power and voltage control considering voltage security assessment, IEEE Trans. Power Syst. 15 (4) (2000) 1–11.

[9] P. Ngatchou, A. Zarei, A. El-Sharkawi, Pareto multi objective optimization, in: Intelligent Systems Application to Power Systems, Proceedings of the 13th International Conference on 6–10 Nov. 2005, 2005, pp. 84–89.

[10] A. Berizzi, M. Innorta, P. Marannino, Multiobjective optimization techniques applied to modern power systems, in: IEEE Power Engineering Society Winter Meeting, Jan 28-Feb 1 2001, 2001.

[11] C.A. Coello Coello, M.S. Lechuga Mopso, A proposal for multiple objective particle swarm optimization, in: IEEE Proceedings World Congress on Computational Intelligence, 2003, pp. 1051–1056.

[12] J.E. Fieldsend, S. Singh, A multi-objective algorithm based upon particle swarm optimisation, an efficient data structure and turbulence, in: The 2002 U.K. Workshop on Computational Intelligence, 2002, pp. 34–44.

[13] X. Hu, R. Eberhart, Y. Shi, Particle swarm with extended memory for multiobjective optimization, in: IEEE Swarm Intelligence Symposium, 2003, pp. 193–198.

[14] S. Mostaghim, J. Teich, Strategies for finding good local guides in multi-objective particle swarm optimization, in: IEEE Swarm Intelligence Symposium, 2003, pp. 26–33.

[15] K. Deb, A. Paratap, S. Agarwal, T. Meyarivan, A fast and elitist multiobjective genetic algorithm: NSGA-II, IEEE Trans. Evolut. Comput. 2 (2002) 182–197.

[16] N. Srinivas, K. Deb, Multiobjective optimization using nondominated sorting in genetic algorithms, Tech. Rep. Dept. Mechanical Engineering, Kanpur, India, 1993.

[17] Y. del Valle, G. Kumar Venayagamoorthy, S. Mohagheghi, J.-C. Hernandez, R.G. Harley, Particle swarm optimization: basic concepts, variants and applications in power systems, IEEE Trans. Evol. Comput. 12 (2) (2008) 171–191.

[18] R.H. Abdel Hamid, A.M.A. Amin, R.S. Ahmed, A.A.A. Elgammal, Optimal operation of induction motors based on multi-objective particle swarm optimization (MOPSO), in: The 33rd Annual Conference of the IEEE Industrial Electronics Society November 5–8, 2007, Taipei, Taiwan, 2007.

[19] C. Thanga Raj, S.P. Srivastava, P. Agarwal, Energy efficient control of three-phase induction motor—a review, Int. J. Comput. Electr. Eng. 1 (1) (2009) 61–70.

[20] A.A.A. El-Gammal, A.M. Sharaf, A self regulating particle swarm optimized controller for (PV-FC) battery charging of hybrid electric vehicles, IET Elec. Sys. Transport 2 (2) (2012) 77–89.

[21] R. Billinton, Y. Gao, Multistate wind energy conversion system models for adequacy assessment of generating systems incorporating wind energy, IEEE Trans. Energy Convers. 23 (1) (2008) 163–170.

[22] Weihao Hu, Yue Wang, Weizheng Yao, Jinlong Wu, Hailong Zhang, Zhaoan Wang, An efficient experimental method for high power direct drive wind energy conversion systems, in: Power Electronics Specialists Conference, PESC 2008. IEEE, 15-19 June, 2008, pp. 3955–3959.

[23] M.C. Pera, D. Hissel, J.M. Kauffmann, Fuel cell systems for electrical vehicles, in: Vehicular Technology Conference, VTC Spring, IEEE 55th, vol. 4, 2002, pp. 2097–2102.

[24] N. Parspour, Novel drive for use in electrical vehicles, in: Vehicular Technology Conference, VTC-Spring, IEEE, 1st, vol. 5, 2005, pp. 2930–2933.

[25] A.M. Sharaf, E. Ozkop, I.H. Altas, A hybrid photovoltaic PV array-battery powered EV-PMDC drive scheme, in: Electrical Power Conference, EPC, IEEE Canada, 2007, pp. 37–43.

[26] Z.Q. Zhu, C.C. Chan, Electrical machine topologies and technologies for electric, hybrid, and fuel cell vehicles, in: Vehicle Power and Propulsion Conference, VPPC '08. IEEE, 2008, pp. 1–6.

[27] J.V. Vas, S. Venugopal, V.G. Nair, Control scheme for electrical drive of solar powered vehicles, in: India Conference, INDICON Annual IEEE, vol. 1, 2008, pp. 75–80.

[28] Z.Q. Zhu, D. Howe, Electrical machines and drives for electric, hybrid, and fuel cell vehicles, Proc. IEEE 95 (4) (2007) 746–765.

[29] A. Luque, S. Hegedus, Handbook of Photovoltaic Science and Engineering, John Wiley and Sons, 2003. ISBN 0471491969.

[30] J. Nelson, The Physics of Solar Cells, Imperial College Press, ISBN 978-1-86094-340-9, 2003.

[31] P. Thounthong, S. Rael, B. Davat, Analysis of supercapacitor as second source based on fuel cell power generation, IEEE Trans. Energy Convers. 24 (1) (2009) 247–255.

[32] A. Gebregergis, P. Pillay, D. Bhattacharyya, R. Rengaswemy, Solid oxide fuel cell modeling, IEEE Trans. Ind. Electron. 56 (1) (2009) 139–148.

[33] I.H. Altas, E.O. kop, A.M. Sharaf, A novel PV-powered standalone village electricity utilization fuzzy logic dynamic controller strategy, in: INISTA 2009, International Symposium on INnovations in Intelligent SysTems and Applications, June 29-July 1, 2009, TRABZON, TURKEY, 2009.

[34] K. Fujinami, K. Takahashi, K. Kondo, Y. Sato, A restarting method of an induction motor speed-sensorless vector control system for a small-sized wind turbine power generator system, in: ICEMS 2009. International Conference on Electrical Machines and Systems, 2009, pp. 1–5.

[35] W.-L. Chen, Y.-Y. Hsu, Controller design for an induction generator driven by a variable-speed wind turbine, IEEE Trans. Energy Convers. 21 (3) (2006) 625–635.

[36] B. Zahedi, S. Vaez-Zadeh, Efficiency optimization control of single-phase induction motor drives, IEEE Trans. Power Electron. 24 (4) (2009) 1062–1070.

[37] C. Mademlis, I. Kioskeridis, T. Theodoulidis, Optimization of single-phase induction Motors-part I: maximum energy efficiency control, IEEE Trans. Energy Convers. 20 (1) (2005) 187–195.

[38] M.B. de Rossiter Correa, C.B. Jacobina, E.R.C. da Silva, A.M.N. Lima, Vector control strategies for single-phase induction motor drive systems, IEEE Trans. Ind. Electron. 51 (5) (2004) 1073–1080.

[39] A.M. Sharaf, C. Ciaxia, H. Huang, A smart PWM-modulated power filter for single phase motorized loads, in: IEEE Canadian Conference on Electrical and Computer Engineering, vol. 2, 1998, pp. 778–781.

[40] A.M. Sharaf, P. Kreidi, Dynamic compensation using switched/modulated power filters, in: Canadian Conference on Electrical and Computer Engineering, 2002. IEEE CCECE, vol. 1, 2002, pp. 230–235.

[41] A.M. Sharaf, R. Chalet, A low cost on-off modulated power filter for single phase motorized loads, in: IEEE Canadian Conference on Electrical and Computer Engineering, vol. 2, 1998, pp. 862–865.

[42] A.M. Sharaf, A. Aljankawey, Voltage stabilization using a facts modulated power filter, in: IEEE International Symposium on Industrial Electronics, vol. 3, 2006, pp. 1937–1942.

[43] L. Yang, G.Y. Yang, Z. Xu, Z.Y. Dong, K.P. Wong, X. Ma, Optimal controller design of a doubly-fed induction generator wind turbine system for small signal stability enhancement, IET Gener. Transm. Distrib. 4 (5) (2010) 579–597.



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DSP-Based Control of Variable Speed Drives

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39.1 Introduction

High-performance motor drives are characterized by the need for smooth rotation down to stall, full control of torque at stall, and fast accelerations and decelerations. In the past, variable speed drives employed predominantly dc motors because of their excellent controllability. However, modern high-performance motor drive systems are usually based on three-phase ac motors, such as the ac induction motor (ACIM) or the permanent-magnet synchronous motor (PMSM). These machines have supplanted the dc motor as the machine of choice for variety of applications because of their simple robust construction, low inertia, high power density, high torque density, and good performance at high speeds of rotation.

The vector-control techniques are established for controlling these ac motors, and most modern high-performance drives now implement digital closed-loop current control. In such systems, the achievable closed-loop bandwidths are directly related to the rate at which the computationally intensive vector-control algorithms and associated vector rotations can be implemented in real time. Because of this computational burden, many high-performance drives now use digital signal processors (DSPs) to implement the embedded motor- and vector-control schemes. The DSPs are special microprocessors used where real-time manipulation of large amounts of digital data is required in order to implement complicated control algorithms. The inherent computational power of the DSP permits very fast cycle times and closed-loop current control bandwidths to be achieved.

The complete current control scheme for these machines also requires a high-precision pulse-width modulation (PWM) voltage-generation scheme and high-resolution analog-to-digital (A/D) conversion (ADC) for the measurement of the motor currents. In order to maintain a smooth control of torque to zero speed, rotor position feedback is essential for modern vector controllers. Therefore, many systems include rotor-position transducers, such as resolvers and incremental encoders.

The Texas Instruments TMS320LF2407 DSP Controller (referred to as the LF2407 in this chapter) is a programmable digital controller with a C2xx DSP central processing unit (CPU) as the core processor. The LF2407 contains the DSP core processor and useful peripherals integrated onto a single piece of silicon. The LF2407 combines the powerful CPU with

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on-chip memory and peripherals. With the DSP core and control-oriented peripherals integrated into a single chip, users can design very compact and cost-effective digital control systems.

The LF2407 DSP controller offers 40 million instructions per second (MIPS) performance. This high processing speed of the C2xx CPU allows users to compute parameters in real time rather than lookup approximations from tables stored in memory. This fast performance is well suited for processing control parameters in applications such as notch filters or sensorless motor-control algorithms where a large amount of calculations must be computed quickly.

While the "brain" of the LF2407 DSP is the C2xx core, the LF2407 contains several control-orientated peripherals on board (see Fig. 39.1). The peripherals on the LF2407 make virtually any digital control requirement possible. Their applications range from analog-to-digital conversion to pulse-width modulation (PWM) generation. Communication peripherals make possible the communication with external peripherals,

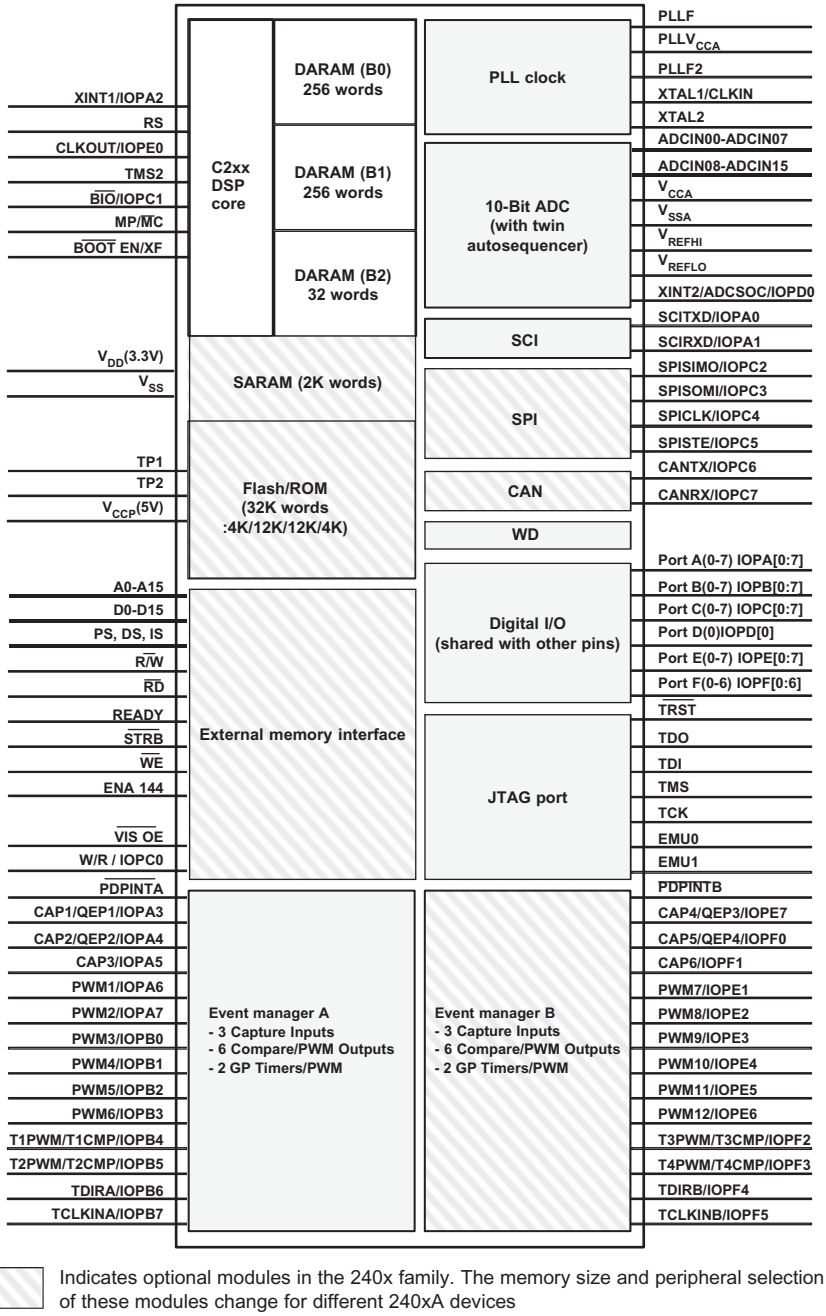


FIG. 39.1 Graphic overview of DSP core and peripherals on the LF2407. Courtesy of Texas Instruments.

personal computers, or other DSP processors. Below is a graphic listing of the different peripherals on board the LF2407 depicted in Fig. 39.1.

We describe here the fundamental principles behind the implementation of high-performance controllers for three-phase ac motors—combining an integrated DSP controller, LF2407, flexible PWM generation, high-resolution A/D conversion, and embedded encoder interface.

39.2 Variable Speed Control of AC Machines

Efficient variable speed control of three-phase ac machines requires the generation of a balanced three-phase set of variable voltages with variable frequency. The variable-frequency supply is typically produced by conversion from dc using power semiconductor devices (typically MOSFETs or IGBTs) as solid-state switches. A commonly used converter configuration is shown in Fig. 39.2A. It is a two-stage circuit, in which the fixed-frequency 50 or 60 Hz ac supply is first rectified to provide the dc-link voltage, V_d, stored in the dc-link capacitor. This voltage is then supplied to an inverter circuit that generates the variable-frequency ac power for the motor. The power switches in the inverter circuit permit the motor terminals to be connected to either V_d or ground.

This mode of operation gives high efficiency because, ideally, the switch has zero loss in both the open and closed positions. By rapid sequential opening and closing of the six switches (Fig. 39.2A), a three-phase ac voltage with an average sinusoidal waveform can be synthesized at the output terminals. The actual output voltage waveform is a pulse-width modulated (PWM) high-frequency waveform, as shown in Fig. 39.2B. In practical, inverter circuits using solid-state switches and high-speed switching of about 20 kHz are possible. Therefore, sophisticated PWM waveforms with fundamental frequencies, nominally in the range of 0–250 Hz, can be generated. The inductive reactance of the motor increases with frequency. Thus, higher-order harmonic currents are very small, and near-sinusoidal currents flow in the stator windings. The fundamental voltage and output frequency of the inverter, as indicated in Fig. 39.2B, are adjusted by changing the PWM waveform using an appropriate controller. When controlling the fundamental output voltage, the PWM process inevitably modifies the harmonic content of the output voltage waveform. A proper choice of modulation strategy can minimize these harmonic voltages and, in result, harmonic losses in the motor.

39.3 General Structure of a Three-Phase AC Motor Controller

Accurate control of any motor drive process may ultimately be reduced to the problem of accurate control of both the torque and speed of the motor. In general, motor speed is controlled directly by measuring the motor's speed or position using appropriate transducers, and torque is controlled indirectly by suitable control of the motor phase currents. Fig. 39.3 shows

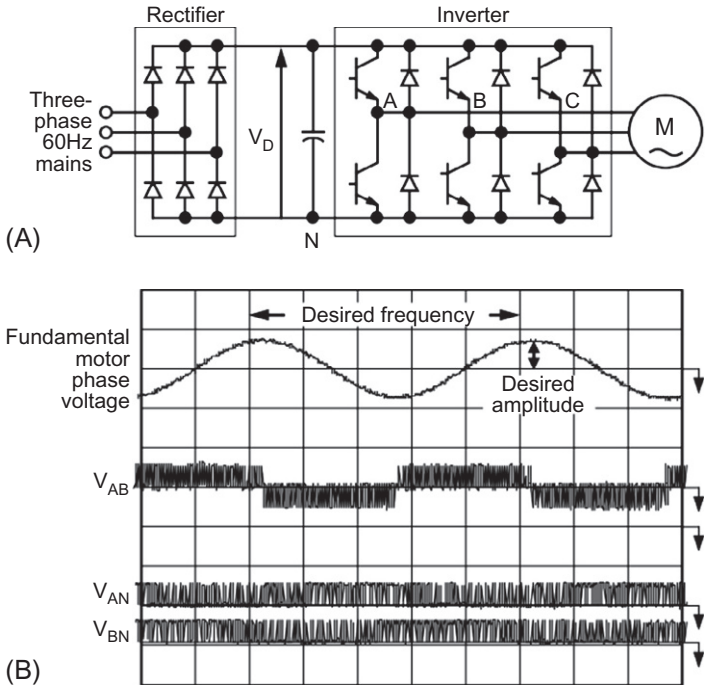


FIG. 39.2 (A) Typical configuration of power converter used to drive three-phase ac motors and (B) typical PWM waveforms in the generation of a variable-voltage, variable-frequency supply for the motor.

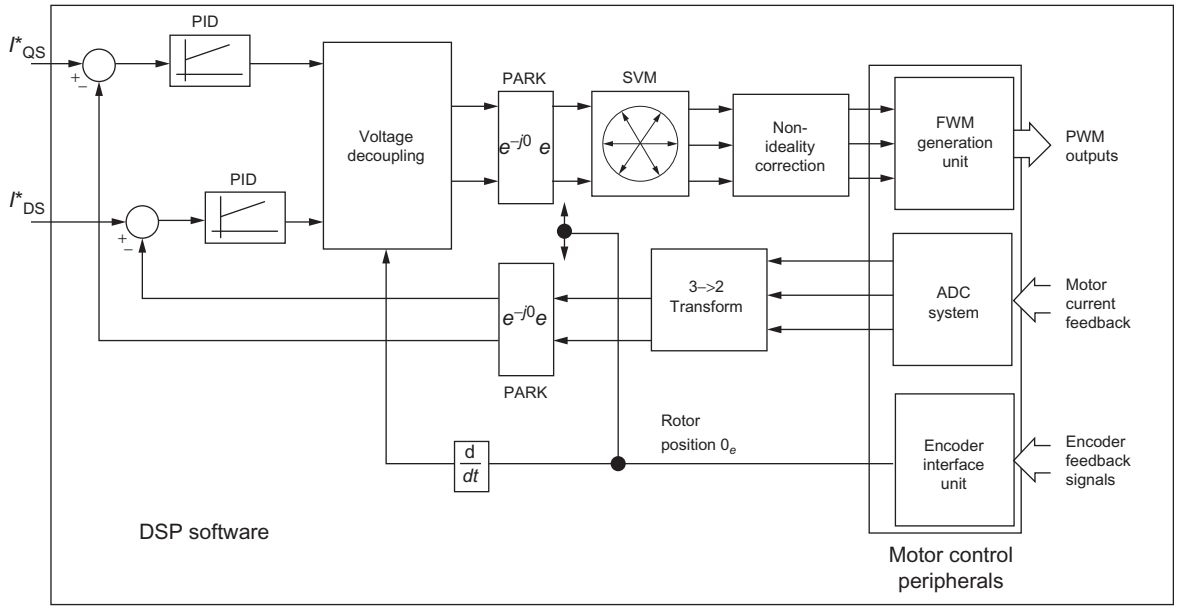


FIG. 39.3 Configuration of typical control system for three-phase ac motor.

a block diagram of a typical synchronous frame current controller for a three-phase motor. The figure also shows the proportioning of tasks between software code modules and the dedicated motor-control peripherals of a motor controller such as the LF2407. The controller consists of two proportional-plus-integral-plus-differential (PID) current regulators that are used to control the motor current vector in a reference frame that rotates synchronously with the measured rotor position.

Sometimes, it may be desirable to implement a decoupling between voltage and speed that removes the speed dependencies and associated axes cross coupling from the control loop. The reference voltage components are then synthesized on the inverter using a suitable PWM strategy, such as space-vector modulation (SVM). It is also possible to incorporate some compensation schemes to overcome the distorting effects of the inverter switching dead time, finite inverter device on-state voltages, and dc-link voltage ripple. The two components of the stator current vector are known as the direct-axis and quadrature-axis components. The direct-axis current controls the motor flux and is usually controlled to be zero with permanent-magnet machines. The motor torque may then be controlled directly by regulation of the quadrature-axis component. Fast, accurate torque control is essential for high-performance drives in order to ensure rapid acceleration and deceleration and smooth rotation down to zero speed under all load conditions.

The actual direct and quadrature current components are obtained by first measuring the motor phase currents with suitable current-sensing transducers and converting them to digital, using an on-chip ADC system. It is usually sufficient to simultaneously sample just two of the motor line currents: since the sum of the three currents is zero, the third current can, when necessary, be deduced from simultaneous measurements of the other two currents. The controller software makes use of mathematical vector transformations, known as Park transformations that ensure that the three-phase set of currents applied to the motor is synchronized to the actual rotation of the motor shaft, under all operating conditions. This synchronism ensures that the motor always produces the optimal torque per ampere—that is, operates at optimal efficiency. The vector rotations require real-time calculation of the sine and cosine of the measured rotor angle, plus a number of multiply-and-accumulate operations. The overall control-loop bandwidth depends on the speed of implementation of the closed-loop control calculations and the resulting computation of new duty-cycle values. The inherent fast computational capability of the 40 MIPS, 16-bit fixed-point DSP core makes it the ideal computational engine for these embedded motor-control applications.

39.3.1 Pulse Width Modulation Generation

In typical ac motor-controller design, both hardware and software considerations are involved in the process of generating the PWM signals that are ultimately used to turn on or off the power devices in the three-phase inverter. In typical digital control environments, the controller generates a regularly timed interrupt at the PWM switching frequency (nominally 10–20 kHz). In the interrupt service routine, the controller software computes new duty-cycle values for the PWM signals used to drive each of the three legs of the inverter. The computed duty cycles depend on both the measured state of the motor (torque and speed) and the desired operating state.

The duty cycles are adjusted on a cycle-by-cycle basis in order to make the actual operating state of the motor follow the desired trajectory.

Once the desired duty-cycle values have been computed by the processor, a dedicated hardware PWM generator is needed to ensure that the PWM signals are produced over the next PWM and controller cycle. The PWM generation unit typically consists of an appropriate number of timers and comparators that are capable of producing very accurately timed signals. Typically, 10- to 12-bit performance in the generation of the PWM timing waveforms is desirable.

Fig. 39.4 shows a typical PWM waveform for a single-leg inverter. In general, there is a small delay required between turning off one power device like A-phase lower device and turning on the complementary power device A-phase upper device. This dead time is required to ensure that the device being turned off has sufficient time to regain its blocking capability before the other device is turned on. Otherwise, a short circuit of the dc voltage could result.

In LF2407, the compare units have been used to generate the PWM signals. The PWM output signal is high when the output of current PI regulation matches the value of T1CNT and is set to low when the timer underflow occurs. The switch states are controlled by the ACTR register. In order to minimize the switching losses, the lower switches are always kept on, and the upper switches are chopped on/off to regulate the phase current.

39.3.2 Analog-to-Digital Conversion Requirements

For the control of high-performance motor drives, fast, high-accuracy, simultaneous-sampling A/D conversion of the measured current values is required. The drives have a rated operation range—a certain power level that they can sustain continuously, with an acceptable temperature rise in the motor and power converter. They also have a peak rating—the ability to handle a current far in excess of the rated current for short periods of time. This allows a large torque to be applied transiently, to accelerate or decelerate the drive very quickly, and then to revert to the continuous range for normal operation. This also means that in the normal operating mode of the drive, only a small percentage of the total input range is being used.

At the other end of the scale, in order to achieve the smooth and accurate rotations desired in these machines, it is wise to compensate for small offsets and nonlinearities such as core saturation and parameter detuning. In any current-sensor electronics, the analog signal processing is often subject to gain and offset errors. Gain mismatches, for example, can exist between the current-measuring systems for different windings. These effects combine to produce undesirable oscillations in the torque. To meet both of these conflicting resolution requirements, modern motor drives use 10-bit A/D converters, depending on the cost/performance trade-off required by the application.

The bandwidth of the system is essentially limited by the amount of time it takes to input information and then perform the calculations. The A/D converters that take many microseconds to convert can produce intolerable delays in the system. A delay in a closed-loop system will degrade the achievable bandwidth of the system, and bandwidth is one of the most important figures of merit in these high-performance drives. Therefore, fast analog-to-digital conversion is a necessity for these applications.

A third important characteristic of the A/D converter used in these applications is timing. In addition to high resolution and fast conversion, simultaneous sampling is needed. In any three-phase motor, it is necessary to measure the currents in the three windings of the motor at exactly the same time in order to get an instantaneous "snapshot" of the torque in the machine. Any time skew (time delay between the measurements of the different currents) is an error factor that is artificially inserted by the means of measurement. Such a nonideality translates directly into a ripple of the torque—a very undesirable characteristic.

The analog-to-digital converter (ADC) on the LF2407 allows the DSP to sample analog or "real-world" voltage signals. The output of the ADC is an integer number that represents the voltage level sampled. The integer number may be used for calculations in an algorithm. The resolution of the ADC is 10 bits, meaning that the ADC will generate a 10-bit number for every conversion it performs. However, the ADC stores the conversion results in registers that are 16-bit wide. The 10 most significant bits are the ADC result, while the least significant bits

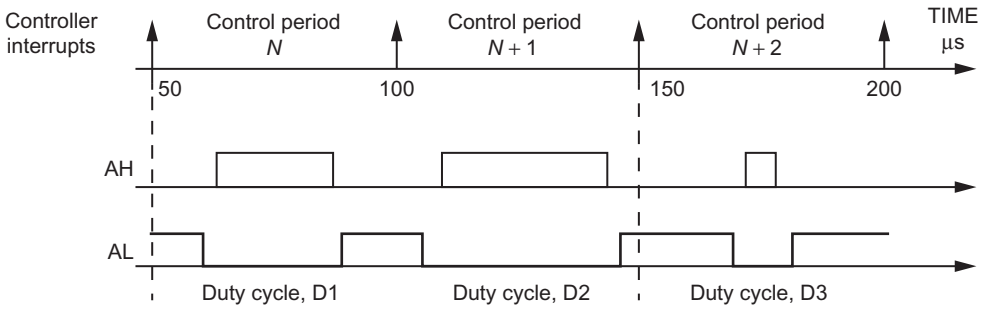


FIG. 39.4 Typical PWM waveforms for a single inverter leg.

(LSBs) are filled with "0"s. There are a total of 16 input channels to the single input ADC. The control logic of the ADC consists of autosequencers, which control the sampling of the 16 input channels to the ADC. The autosequencers control not only which channels (input channels) will be sampled by the ADC but also the order of the channels that the ADC performs conversions on. The two 8-conversion autosequencers can operate independently or cascade together as a "virtual" 16-conversion ADC.

39.3.3 Position Sensing and Encoder Interface Units

Usually, the motor position is measured through the use of an encoder mounted on the rotor shaft. The incremental encoder produces a pair of quadrature outputs (A and B), each with a large number of pulses per revolution of the motor shaft. For a typical encoder with 1024 lines, both signals produce 1024 pulses per revolution. Using a dedicated quadrature counter, it is possible to count both the rising and falling edges of both the A and B signals so that one revolution of the rotor shaft may be divided into 4096 different values. In other words, a 1024-line encoder allows the measurement of rotor position to 12-bit resolution. The direction of rotation may also be inferred from the relative phasing of quadrature signals A and B.

Fig. 39.5 shows the structure of an encoder. It consists of a light source, a radially slotted disk, and the photoelectric sensors. The disk rotates with the rotor. The two photosensors detect the light passing through the slots in the disk. When the light is hidden, a logic "0" is generated by the sensors. When the light passes through the slots of the disk, a logic "1" is produced. These logic signals are shown in Fig. 39.5. By counting the number of pulses, the motor speed can be calculated. The direction of rotation can be determined by detecting the leading signal between signals A and B.

This is all very well, but there is an increasing class of cost-sensitive motor drive applications with lower performance demands that can afford neither the cost nor the space requirements of the rotor position transducer. In these cases, the same motor-control algorithms can be implemented with estimated rather than measured rotor position.

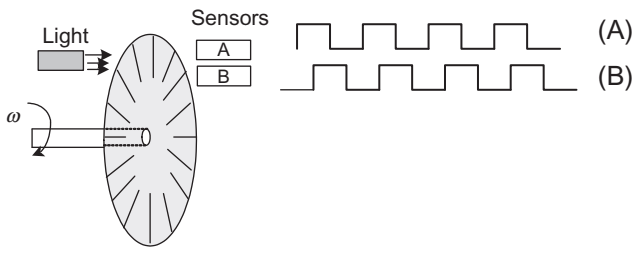


FIG. 39.5 The structure of an optical encoder showing sensor A and B outputs.

The DSP core is quite capable of computing rotor position using sophisticated rotor-position estimation algorithms, such as extended Kalman estimators that extract estimates of the rotor position from measurements of the motor voltages and currents. These estimators rely on the real-time computation of a sufficiently accurate model of the motor in the DSP. In general, these sensorless algorithms can be made to work and the sensored algorithms at medium to high speeds of rotation. But as the speed of the motor decreases, the extraction of reliable speed-dependent information from voltage and current measurements becomes more difficult. In general, sensorless motor control is applicable principally to applications such as compressors, fans, and pumps, where continuous operation at zero or low speeds is not required.

39.3.4 The PI Regulator

An electric drive based on the field-orientated control (FOC) needs two constants as control parameters, the torque component reference i_{qs}^{e*} and the flux component reference i_{ds}^{e*}. The classical PI regulator is well suited to regulate the torque and flux feedback to the desired values. This is because it is able to reach constant references by correctly setting both the proportional term (K_p) and the integral term (K_i), which are, respectively, responsible for the error sensibility and for the steady-state error. The numerical expression of the PI regulatoris as follows:

$$Y_{(k)} = K_p e_{(k)} + K_i e_{(k)} + \sum_{n=0}^{k-1} e_{(n)} \tag{39.1}$$

which is represented in Fig. 39.6.

During normal operation, large reference value variations or disturbances may occur that result in the saturation and overflow of the regulator variables and output. To solve this problem, one solution is to add a correction of the integral component as depicted in Fig. 39.7.

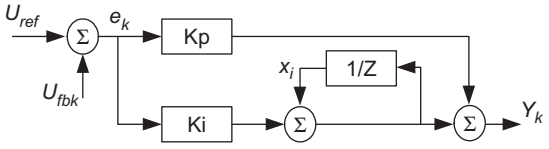


FIG. 39.6 Classical PI regulator structure in discrete domain.

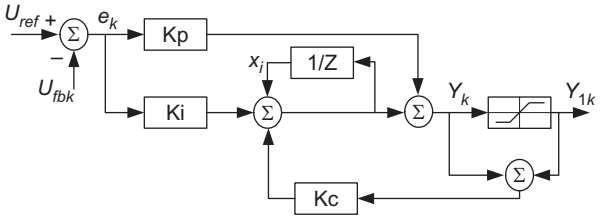


FIG. 39.7 Numerical PI regulator with correction.

The constants K_p, K_i, and K_c, proportional, integral, and integral correction components, respectively, are selected based on the sampling period and on the motor parameters. After defining the DSP-controlled motor drive requirements, in the following, we describe the digital control algorithms for permanent-magnet motors and induction motors.

39.4 DSP-Based Control of Permanent Magnet Brushless DC Machines

Permanent-magnet alternating current (PMAC) motors are synchronous motors that have permanent magnets mounted on the rotor and polyphase, usually three-phase, armature windings located on the stator. Since the field is provided by the permanent magnets, the PMAC motor has higher efficiency than induction- or switched-reluctance motors. The advantages of PMAC motors, combined with a rapidly decreasing cost of permanent magnets, have led to their widespread use in many variable speed drives such as robotic actuators, computer disk drives, appliances, automotive applications, and air-conditioning (HVAC) equipment.

In general, PMAC motors are categorized into two types. The first type of motor is referred to as PM synchronous motor (PMSM). These motors produce a sinusoidal back EMF, shown in Fig. 39.8A, and should be supplied with sinusoidal current/voltage. The PMSM's electronic control and drive system uses continuous rotor position feedback and PWM to supply the motor with the sinusoidal voltage or current. With this, constant torque is produced with very little ripple.

The second type of PMAC motor has a trapezoidal back EMF and is referred to as the brushless DC (BLDC) motor. The back EMF of the BLDC motor is shown in Fig. 39.8B. The BLDC motor requires that quasi-rectangular-shaped currents are fed into the machine. Alternatively, the voltage may be applied to the motor every 120 degrees, with a current limit to hold the currents within the motor's capabilities.

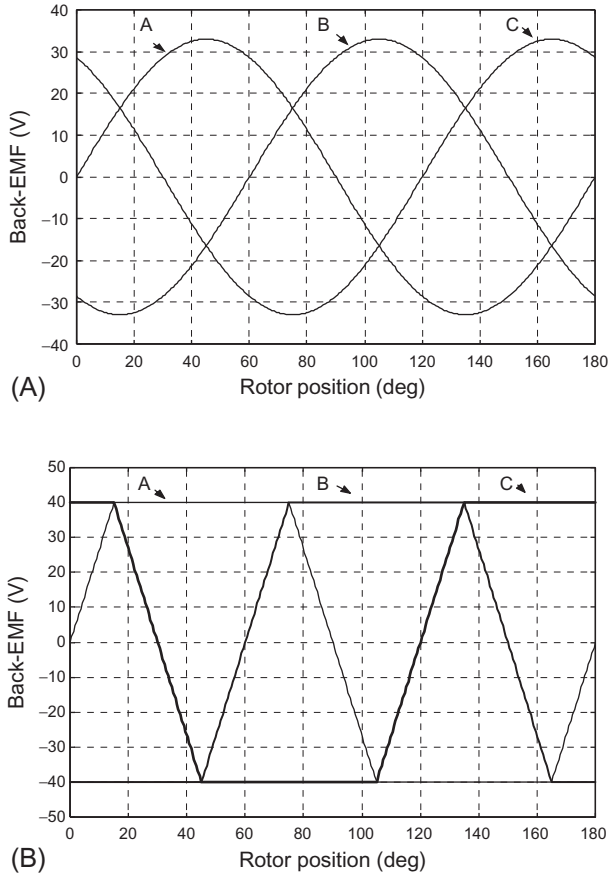


FIG. 39.8 The back EMF of PMAC motors: (A) three-phase back EMF of PMSM and (B) three-phase back EMF of BLDC motors.

39.4.1 Mathematical Model of the BLDC Motor

The phase variables are used to model the BLDC motor due to its nonsinusoidal back EMF and phase current. The terminal voltage equation of the BLDC motor can be written as

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} R+pL_s & 0 & 0 \\ 0 & R+pL_s & 0 \\ 0 & 0 & R+pL_s \end{bmatrix} \cdot \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} \quad (39.2)$$

where v_a, v_b, and v_c are the phase voltages; i_a, i_b, and i_c are the phase currents; e_a, e_b, and e_c are the phase back-EMF voltages; R is the phase resistance; L_s is the synchronous inductance per phase and includes both leakage and armature reaction inductances; and p represents d/dt. The electromagnetic torque is given by

$$T_e = \frac{(e_a i_a + e_b i_b + e_c i_c)}{\omega_m} \quad (39.3)$$

where ω_m is the mechanical speed of the rotor. The equation of motion is

$$\frac{d}{dt}\omega_m = \frac{(T_e - T_L - B\omega_m)}{J} \quad (39.4)$$

where T_L is the load torque, B is the damping constant, and J is the moment of inertia of the rotor shaft and the load.

39.4.2 Torque Generation

From Eq. (39.3), the electromagnetic torque of the BLDC motor is related to the product of the phase back EMF and current. The back EMFs in each phase are trapezoidal in shape and are displaced by 120 electrical degrees with respect to each other in a three-phase machine. A rectangular current pulse is injected into each phase so that current coincides with the crest of the back-EMF waveform; hence, the motor develops

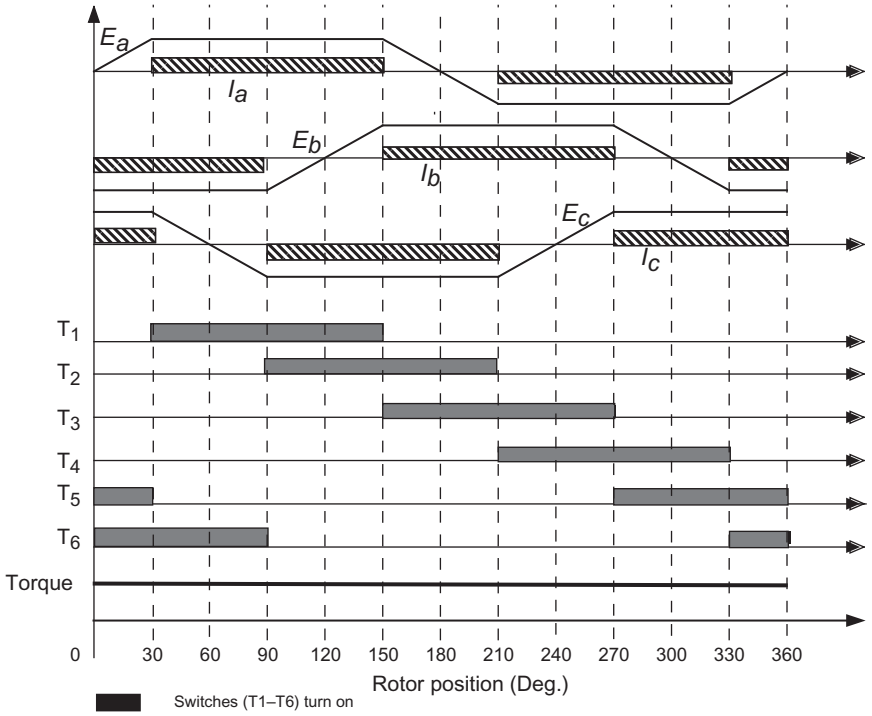


FIG. 39.9 The principle of the six-step current control algorithm. T_1–T_6 are the gate signals; E_a, E_b, and E_c are the motor phase back EMF; and I_a, I_b, and I_c are the motor phase currents.

an almost constant torque. This strategy, commonly called six-step current control, is shown Fig. 39.9. The amplitude of each phase's back EMF is proportional to the rotor speed and is given by

$$E = k\phi\omega_m \tag{39.5}$$

where k is a constant and depends on the number of turns in each phase, φ is the permanent-magnet flux, and ω_m is the mechanical speed. In Fig. 39.9, during any 120 degrees interval, the instantaneous power converted from electric to mechanical, P_o, is the sum of the contributions from two phases in series and is given by

$$P_0 = \omega_m T_e = 2EI \tag{39.6}$$

where T_e is the output torque and I is the amplitude of the phase current. From Eqs. (39.4) and (39.6), the expression for output torque can be written as

$$T_e = 2k\phi I = k_t I \tag{39.7}$$

where K_t is the torque constant. Since the electromagnetic torque is only proportional to the amplitude of the phase current in Eq. (39.7), torque control of the BLDC motor is essentially accomplished by phase current control.

39.4.3 BLDC Motor Control Topology

Based on the previously discussed concept, a BLDC motor drive system is shown in Fig. 39.10. It can be seen that the total

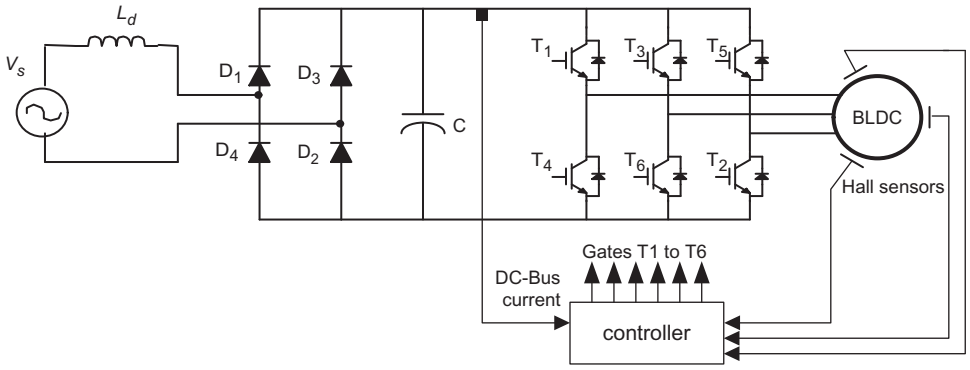


FIG. 39.10 BLDC motor-control system.

drive system consists of the BLDC motor, power electronic converter, sensor, and controller.

The BLDC motors are predominantly surface-magnet machines with wide magnet pole arcs. The stator windings are usually concentrated windings, which produce a square waveform distribution of flux density around the air gap. The design of the BLDC motor is based on the crest of each half cycle of the back-EMF waveform. In order to obtain a smooth output torque, the back-EMF waveform should be wider than 120 degrees electrical degrees. A typical BLDC motor with 12 stator slots and 4 poles on the rotor is shown in Fig. 39.11. The inverter is usually responsible for the electronic commutation and current regulation. For the six-step current control, if the motor windings are Y-connected without the neutral connection, only two of the three-phase currents flow through the inverter in series. This results in the amplitude of the DC-link current always being equal to that of the phase currents. The PWM current controllers are typically used to regulate the actual machine currents in order to match the rectangular current reference waveforms shown in Fig. 39.9. For example, during one 60 degrees interval, when switches T_1 and T_6 are active, phases A and B conduct. The lower switch T_6 is always turned on, and the upper switch T_1 is chopped on/off using either a hysteresis current controller with variable switch frequency or a PI controller with fixed switch frequency.

When T_1 and T_6 are conducting, current builds up in the path as shown in Fig. 39.12A with dashed line. When switch T_1 is turned off, the current decays through diode D_4 and switch T_6 as depicted in Fig. 39.12B. In the next interval, switch T_2 is on, and T_1 is chopped so that phase A and phase C conduct. During the commutation interval, the phase-B current rapidly decreases through the freewheeling diode D_3 until it becomes zero and the phase C current builds up.

From the above analysis, each of the upper switches is always chopped for one 120 degrees interval, and the corresponding lower switch is always turned on per interval. The freewheeling diodes provide the necessary paths for the currents to circulate when the switches are turned off and during the commutation intervals. There are two types of sensors for the BLDC drive system: a current sensor and a position sensor. Since the amplitude of the dc-link current is always equal to the motor phase current in six-step current control, the dc-link current is measured instead of the phase current. Thus, a shunt resistor, which is in series with the inverter, is usually used as the current sensor. Hall-effect position sensors typically provide the position information needed to synchronize the stator excitation with rotor position in order to produce constant torque. Hall-effect sensors detect the change in magnetic field. The rotor magnets are used as triggers for the Hall sensors. A signal-conditioning circuit is needed for noise cancellation in Hall-effect sensor circuits. In six-step current control algorithm, rotor position needs to be detected at only six discrete points in each electric cycle. The controller tracks these six points so that the proper switches are turned on or off for the correct intervals. Three Hall-effect sensors, spaced 120 electrical degrees apart, are mounted on the stator frame. The digital signals from the Hall sensors are then used to determine the rotor position and switch gating signals for the inverter switches.

39.4.4 DSP Controller Requirements

The controller of BLDC drive systems reads the current and position feedback, implements the speed or torque control algorithm, and finally generates the gate signals. The connectivity of the LF2407 in this application is illustrated in Fig. 39.13. Three capture units in the LF2407 are used to detect both the rising and falling edges of Hall-effect signals. Hence, in every 60 electrical degrees of motor rotation, one capture unit interrupt is generated that ultimately causes a change in the gating signals and the motor to move to the next position. One input channel of the 10-bit A/D converter reads the dc-link current. The output pins PWM1–PWM6 are used to supply the gating signals to the inverter.

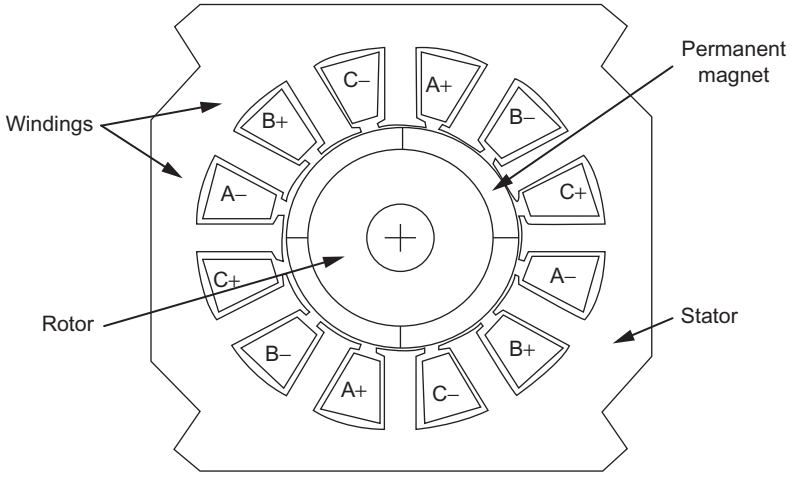


FIG. 39.11 The 4-pole 12-slot BLDC motor.

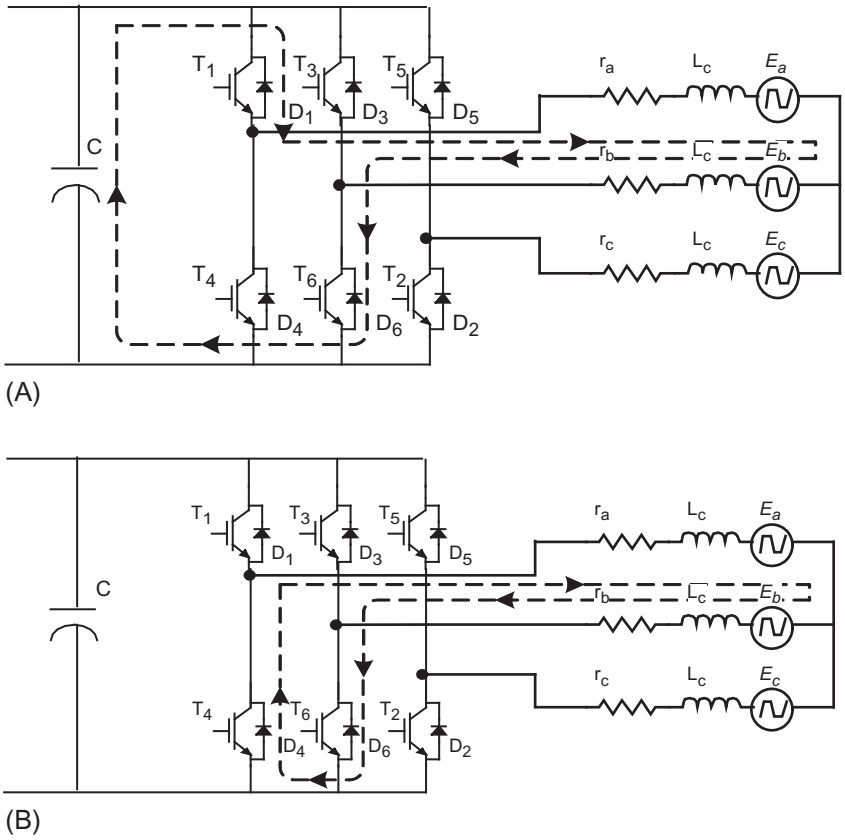


FIG. 39.12 The current path when the switch T_1 (A) turns on and (B) turns off while switch T_6 stays on.

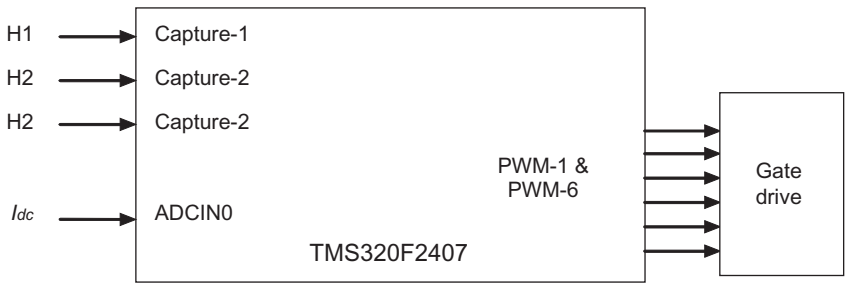


FIG. 39.13 The interface of LF2407.

39.4.5 Implementation of the BLDC Motor Control Algorithm Using LF2407

A block diagram of the BLDC motor-control system is shown in Fig. 39.14. The dashed line separates the software from the hardware components introduced in the previous section. It is necessary to choose hardware components carefully in order to ensure high processing speed and precision in the overall control system. The overall control algorithm of the BLDC motor consists of nine modules:

- Initialization procedure
- Detection of Hall-effect signals
- Speed control subroutine
- Measurement of current
- Speed profiling
- Calculation of actual speed
- PID regulation
- PWM generation
- DAC output

The flowchart of the overall control algorithm is illustrated in Fig. 39.15.

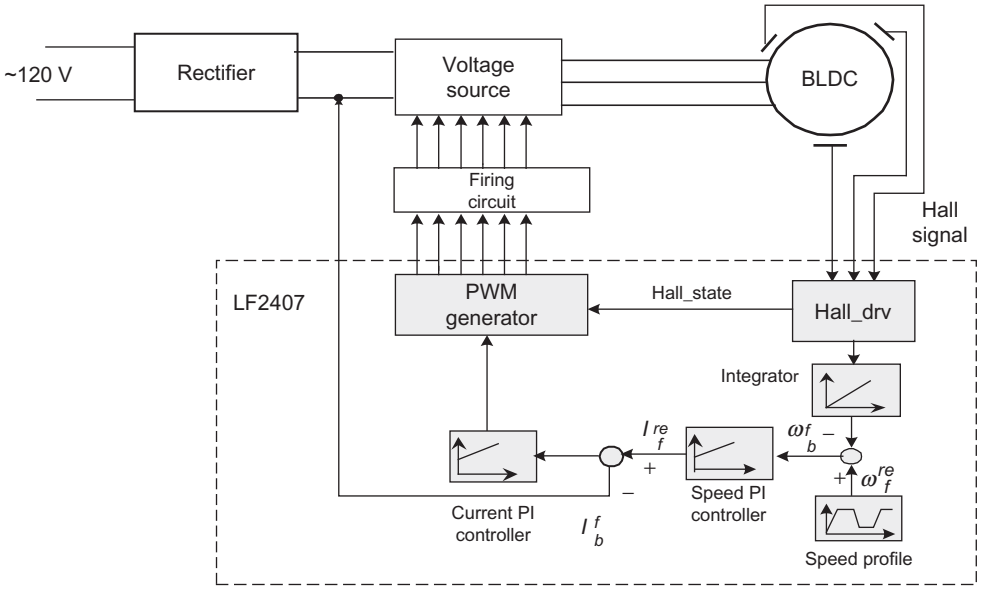


FIG. 39.14 The block diagram of BLDC motor-control algorithm.

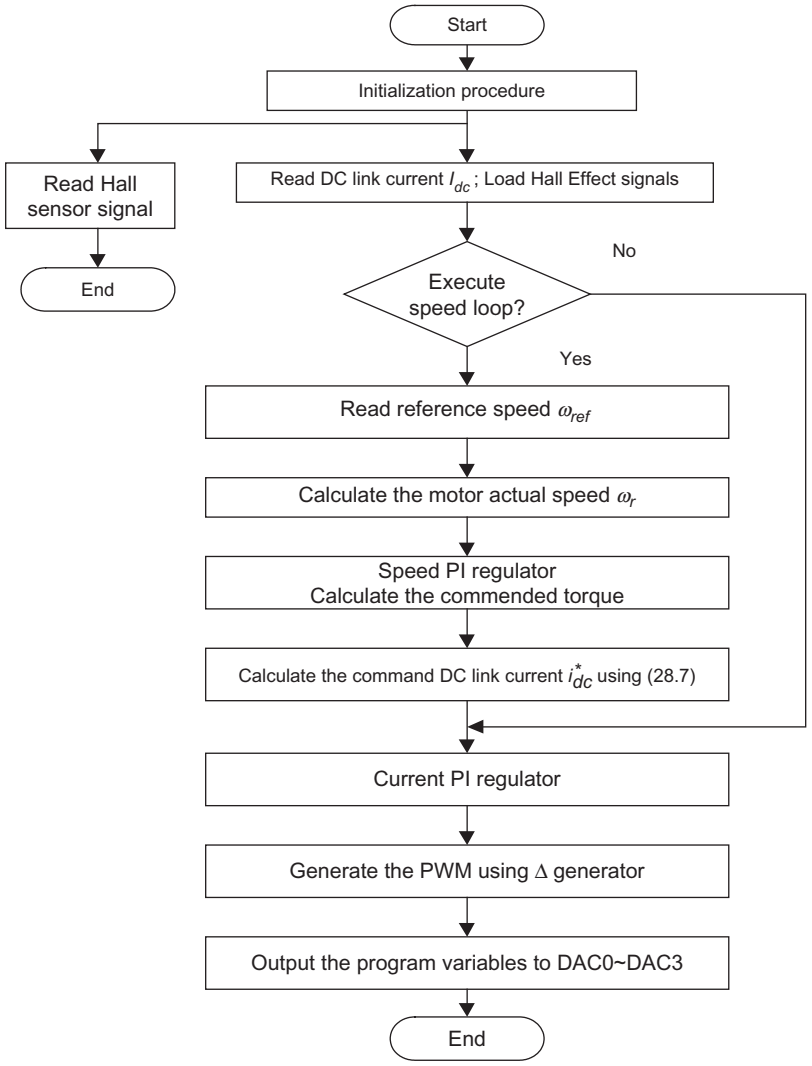


FIG. 39.15 BLDC algorithm flowchart.

39.5 DSP-Based Control of Permanent Magnet Synchronous Machines

As previously described, the permanent-magnet synchronous motor (PMSM) is a PM motor with a sinusoidal back EMF. Compared with the BLDC motor, it has less torque ripple because the torque pulsations associated with current commutation do not exist. A carefully designed machine in combination with a good control technique can yield a very low level of torque ripple (<2% rated), which is attractive for high-performance motor-control applications such as machine tool and servo applications.

In this section, following the same procedures used in the previous section, the principles of the PMSM drive system will be introduced. Later, the control implementation using the LF2407 DSP will be described in detail.

39.5.1 Mathematical Model of PMSM

Fig. 39.16 depicts the simplified three-phase surface-mounted PMSM motor for our discussion. The stator windings, *as-as'*, *bs-bs'*, and *cs-cs'*, are shown as lumped windings for simplicity but are actually distributed around the stator. The rotor has two poles. Mechanical rotor speed and position are denoted as ω_{rm} and θ_{rm}, respectively. Electric rotor speed and position, ω_r and θ_r, are defined as $P/2$ times the corresponding mechanical quantities, where P is the number of poles.

Based on the above motor definition, the voltage equation in the abc stationary reference frame is given by

$$V_{abcs} = R_s i_{abcs} + \frac{d}{dt}\lambda_{abcs} \tag{39.8}$$

where

$$f_{abcs} = [f_{as} f_{bs} f_{cs}]^T \tag{39.9}$$

and the stator resistance matrix is given by

$$R_s = \mathrm{diag}[r_s \quad r_s \quad r_s] \tag{39.10}$$

The flux linkages equation can be expressed by

$$\lambda_{abcs} = L_s i_{abcs} + \lambda'_m \begin{bmatrix} \sin\vartheta_r \\ \sin\left(\vartheta_r - \frac{2\pi}{3}\right) \\ \sin\left(\vartheta_r - \frac{4\pi}{3}\right) \end{bmatrix} \tag{39.11}$$

where λ'_m denotes the amplitude of the flux linkages established by the permanent magnet as viewed from the stator phase windings. Note that in Eq. (39.11), the back EMFs are sinusoidal waveforms that are 120 degrees apart from each other.

The stator self-inductance matrix, L_s, is given as

$$L_s = \begin{Bmatrix} L_{ls} + L_A - L_B\cos 2\theta_r & -\frac{1}{2}L_A - L_B\cos 2(\theta_r - \pi/3) & -\frac{1}{2}L_A - L_B\cos 2(\theta_r + \pi/3) \\ -\frac{1}{2}L_A - L_B\cos 2(\theta_r - \pi/3) & L_{ls} + L_A - L_B\cos 2(\theta_r - 2\pi/3) & -\frac{1}{2}L_A - L_B\cos 2(\theta_r + \pi) \\ -\frac{1}{2}L_A - L_B\cos 2(\theta_r + \pi/3) & -\frac{1}{2}L_A - L_B\cos 2(\theta_r + \pi) & L_{ls} + L_A - L_B\cos 2(\theta_r + 2\pi/3) \end{Bmatrix} \tag{39.12}$$

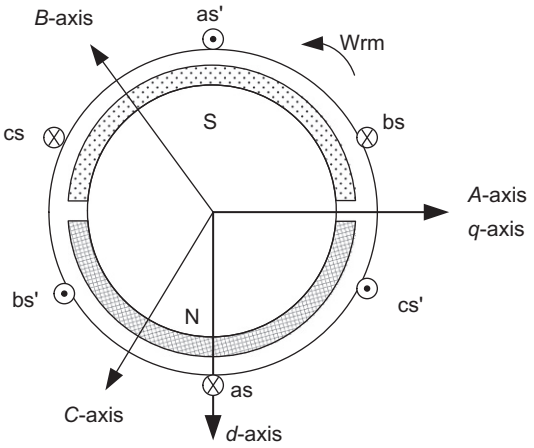


FIG. 39.16 The cross section of PMSM.

The electromagnetic torque may be written as

$$T_e = \frac{P}{2}\left\{\lambda'_m\left[\left(i_{as} - \frac{1}{2}i_{bs} - \frac{1}{2}i_{cs}\right)\cos\theta_r - \frac{\sqrt{3}}{2}(i_{bs} - i_{cs})\sin\vartheta_r\right] + \frac{L_{md} - L_{mq}}{3}\left[\left(i_{as}^2 - \frac{1}{2}i_{bs}^2 - \frac{1}{2}i_{cs}^2 - i_{as}i_{bs} - i_{as}i_{cs} + 2i_{bs}i_{cs}\right)\sin 2\theta_r + \frac{\sqrt{3}}{2}\left(i_{bs}^2 i_{cs}^2 - 2i_{as}i_{bs} + 2i_{as}i_{cs}\right)\cos 2\theta_r\right]\right\} + T_{cog}(\theta_r) \tag{39.13}$$

In Eq. (39.13), $T_{cog}(\theta_r)$ represents the cogging torque, and the d- and q-axes magnetizing inductances are defined by

$$L_{md} = \frac{3}{2}(L_A - L_B)$$

and

$$L_{md} = \frac{3}{2}(L_A + L_B) \tag{39.14}$$

The torque and speed are related by the electromechanical motion equation

$$J\frac{d}{dt}\omega_{rm} = \frac{P}{2}(T_e - T_L) - B_m\omega_{rm} \tag{39.15}$$

where J is the rotational inertia, B_m is the approximated mechanical damping due to friction, and T_L is the load torque.

39.5.2 Mathematical Model of PMSM in Rotor Reference Frame

The voltage and torque equations can be expressed in the rotor reference frame in order to transform the time-varying variables into steady-state constants. The transformation of the three-phase variables in the stationary reference frame to the rotor reference frame is defined as

$$f_{qd0r} = K_r f_{abcs} \tag{39.16}$$

where

$$k_r = \frac{2}{3}\begin{bmatrix} \cos\theta_r & \cos\left(\theta_r - \frac{2\pi}{3}\right) & \cos\left(\theta_r + \frac{2\pi}{3}\right) \\ \sin\theta_r & \sin\left(\theta_r - \frac{2\pi}{3}\right) & \sin\left(\theta_r + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}$$

If the applied stator voltages are given by

$$\begin{cases} V_{as} = \sqrt{2}V_s\cos\theta_{ev} \\ V_{bs} = \sqrt{2}V_s\cos\left(\theta_{ev} = \frac{2\pi}{3}\right) \\ V_{cs} = \sqrt{2}V_s\cos\left(\theta_{ev} + \frac{2\pi}{3}\right) \end{cases} \tag{39.17}$$

then applying Eq. (39.16) to Eqs. (39.8), (39.11), and (39.17) yields

$$v_{qs}^r = r_s i_{qs}^r + \omega_r\lambda_{ds}^r + \frac{d}{dt}\lambda_{qs}^r \tag{39.18}$$

$$v_{ds}^r = r_s i_{ds}^r - \omega_r\lambda_{qs}^r + \frac{d}{dt}\lambda_{ds}^r \tag{39.19}$$

$$\lambda_{qs}^r = L_{qs} i_{qs}^r \tag{39.20}$$

$$\lambda_{ds}^r = L_{ds} i_{ds}^r + \lambda_m^{'r} \tag{39.21}$$

where the q- and d-axes self-inductances are given by $L_{qs} = L_{ls} + L_{mq}$ and $L_{ds} = L_{ls} + L_{md}$, respectively.

The electromagnetic torque can be written as

$$T_e = \frac{3}{2}\frac{P}{2}\left[\lambda_m^{'r} i_{qs}^r + (L_{ds} - L_{qs}) i_{qs} i_{ds}\right] \tag{39.22}$$

From Eq. (39.22), it can be seen that torque is related only to the d- and q-axes currents. Since $L_q \geq L_d$ (for surface-mounted PMSM, both inductances are equal), the second item contributes a negative torque if the flux-weakening control has been used. In order to achieve the maximum torque/current ratio, the d-axis current is set to zero during the constant torque control so that the torque is proportional only to the q-axis current. Hence, this results in the control of the q-axis current for regulating the torque in rotor reference frame.

39.5.3 PMSM Control Topology

Based on the above analysis, a PMSM drive system is developed as shown in Fig. 39.17. The total drive system looks similar to that of the BLDC motor and consists of a PMSM, power electronic converter, sensors, and controller. These components are discussed in detail in the following sections.

The design consideration of the PMSM is to first generate the sinusoidal back EMF. Unlike the BLDC, which needs concentrated windings to produce the trapezoidal back EMF, the stator windings of PMSM are distributed in as many slots per pole

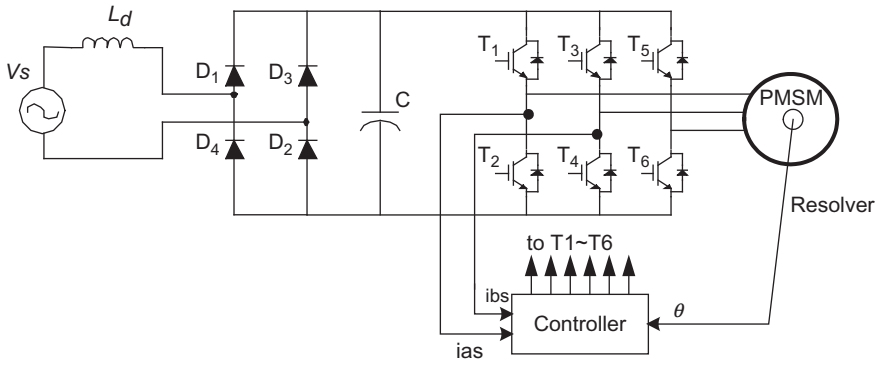


FIG. 39.17 The PMSM speed control system.

as deemed practical to approximate a sinusoidal distribution. To reduce the torque ripple, standard techniques such as skewing and chorded windings are applied to the PMSM. With the sinusoidally excited stator, the rotor design of the PMSM becomes more flexible than the BLDC motor where the surface-mounted permanent magnet is a favorite choice. Besides the common surface-mounted nonsalient pole PM rotor, the salient pole rotors, like inset and buried magnet rotors, are often used because they offer appealing performance characteristics during the flux-weakening region. A typical PMSM with 36 stator slots in stator and 4 poles on the rotor is shown in Fig. 39.18.

Due to the sinusoidal nature of the PMSM, control algorithms such as V/f and vector control, developed for other AC motors, can be directly applied to the PMSM control system. If the motor windings are Y-connected without a neutral connection, three-phase currents can flow through the inverter at any moment. With respect to the inverter switches, three switches, one upper and two lower in three different legs, conduct at any moment as shown in Fig. 39.19. The PWM current control is still used to regulate the actual machine current. Either a hysteresis current controller, a PI controller with sine triangle, or an SVPWM strategy is employed for this purpose. Unlike the BLDC motor, the three switches are switched at any time.

39.5.4 DSP Controller Requirements

The LF2407 is used as the controller to implement speed control of the PMSM system. The interface of the LF2407 is illustrated in Fig. 39.20. Similar to the BLDC motor-control system, three input channels are selected to read the two-phase currents and resolver signal. Because a resolver is used in one case, the quadrature-encoder-pulse (QEP) inputs are not used. The QEP inputs work only with a QEP signal that a rotary encoder supplies. The DSP output pins PWM1–PWM6 are used to supply the gating signals to the switches and form the output of the control part of the system.

39.5.5 Implementation of the PMSM Algorithm Using the LF2407

The block diagram of the PMSM drive system is displayed in Fig. 39.21.

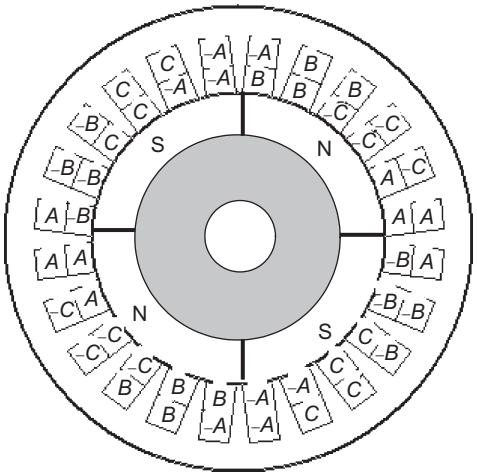


FIG. 39.18 A 4-pole 24-slot PMSM.

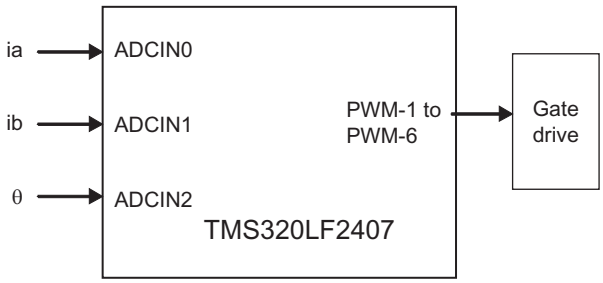


FIG. 39.20 The interface of LF2407.

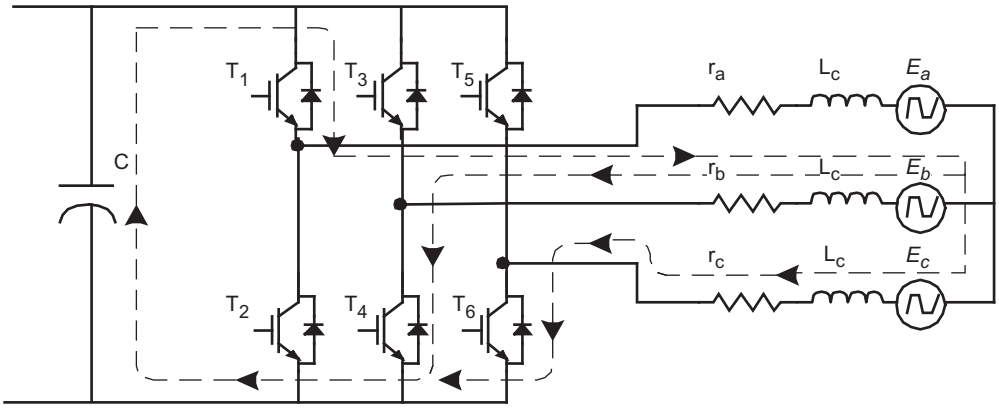


FIG. 39.19 The current path when the three phases are chopped.

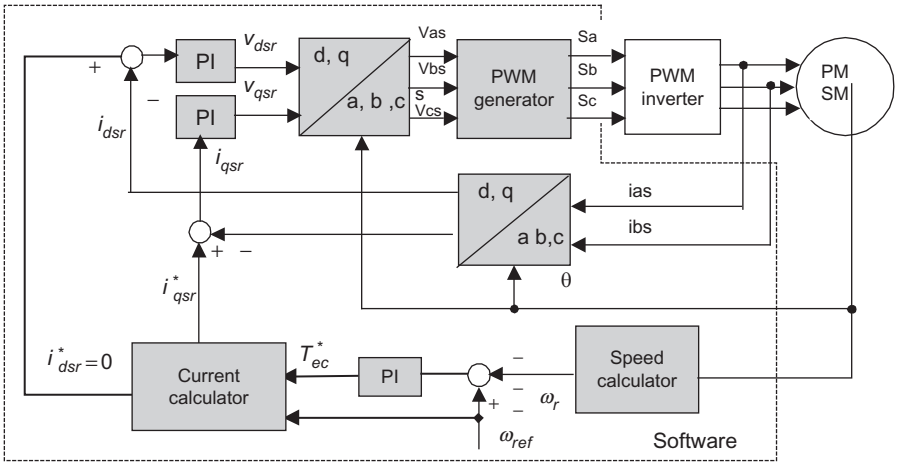


FIG. 39.21 Block diagram of PMSM speed control system.

The flowchart of the developed software is shown in Fig. 39.22. The control program of the PMSM has one main routine and includes four modules:

- Initialization procedure
- DAC module
- ADC module
- Speed control module

In the following section, speed control module is discussed.

39.5.5.1 The Speed Control Algorithm

The requirement for speed control algorithm can be itemized as follows:

- Reading the current and position signal and then generating the commanded speed profile
- Calculating the actual motor speed and transferring the variables in the abc model to the *d-q* model and reverse
- Regulating the motor speed and currents using the vector-control strategy
- Generating the PWM signal based on the calculated motor phase voltages

The PWM frequency is determined by the time interval of the interrupt, with the controlled phase voltages being recalculated every interrupt.

39.6 DSP-Based Vector Control of Induction Motors

For many years, induction motors have been preferred for a variety of industrial applications because of their robust and rugged construction. Compared to dc motors, induction motors are not as easy to control. They typically draw large starting currents, about six to eight times their full-load values, and operate with lagging power factor when loaded. However, with the advent of the vector-control concept for motor control, it is possible to decouple the torque and the flux, thus making the control of the induction motor very similar to that of the dc motor.

The most popular type of induction motor used is the squirrel-cage induction motor. The rotor consists of a laminated core with parallel slots for carrying the rotor conductors, which are usually heavy bars of copper, aluminum, or alloys. One bar is placed in each slot, or rather, the bars are inserted from the end when the semiclosed slots are used. The rotor bars are brazed, electrically welded, or bolted to two heavy and stout short-circuiting end rings, thus completing the squirrel-cage construction. The rotor bars are permanently short-circuited on themselves. The rotor slots are usually not parallel to the shaft but are given a slight angle, called a skew, which increases the rotor resistance due to increased length of rotor bars and an increase in the slip for a given torque. The skew is also advantageous because it reduces the magnetic hum while the motor is operating and reduces the locking tendency or cogging of the rotor teeth.

When the three-phase stator windings are fed by a three-phase supply, a magnetic flux of a constant magnitude rotating at synchronous speed is created in the air gap. Due to the relative speed between the rotating flux and the stationary conductors, an electromagnetic force (EMF) is induced in the rotor in accordance with Faraday's laws of electromagnetic induction. The frequency of the induced EMF is the same as the supply frequency, and the magnitude is proportional to the relative velocity between the flux and the conductors. Therefore, the rotor current develops in the same direction as the flux and tries to catch up with the rotating flux.

39.6.1 Induction Motor Field-oriented Control

The term "vector" control refers to the control technique that controls both the amplitude and the phase of ac excitation voltage. Vector control controls the spatial orientation of the EMF

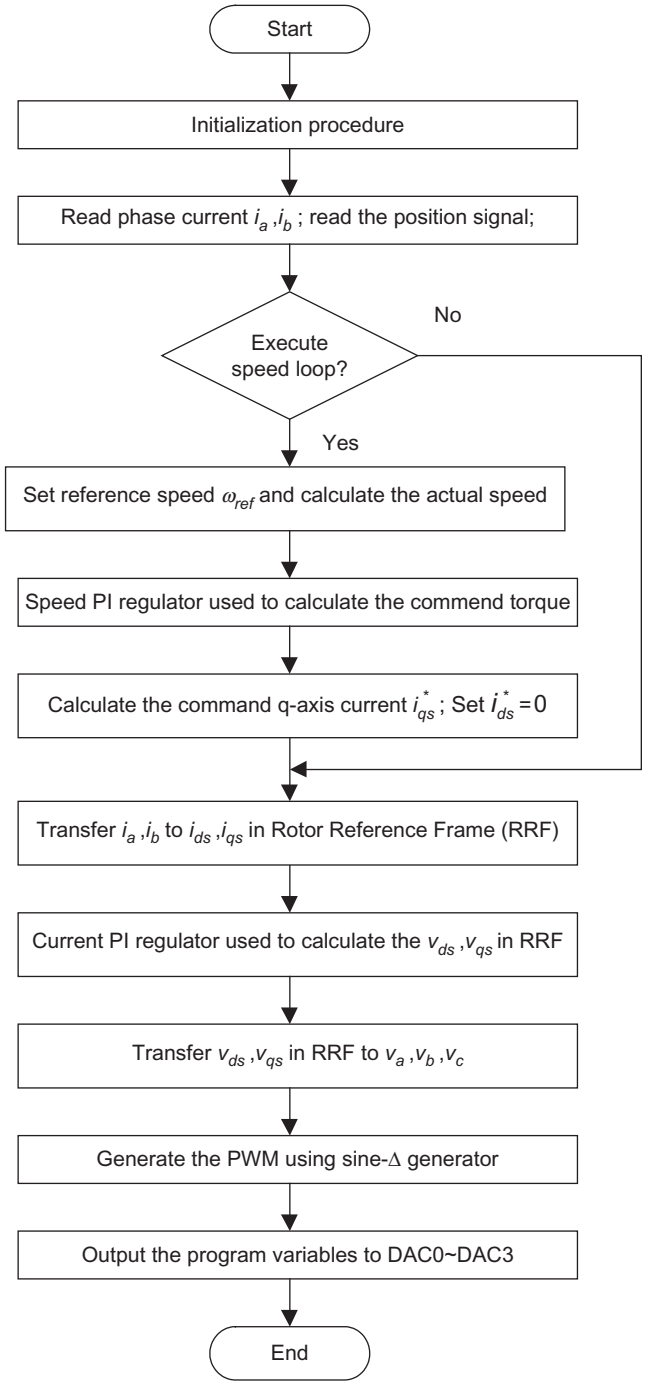


FIG. 39.22 The flowchart of PMSM control system.

in the machine. This has led to the coining of the term FOC, which is used for controllers that maintain a 90 degrees spatial orientation between the critical field components.

The required 90 degrees of spatial orientation between key field components can be compared with the dc motor, where the armature winding magnetic field and the field winding magnetic field are always in quadrature. The objective is to force the control of the induction machine to be similar to the control of a dc motor, that is, torque control. In dc machines, the field and the armature winding axes are orthogonal to one another, making the magnetomotive forces (MMFs) established orthogonal. If the iron saturation is ignored, then the orthogonal fields can be considered to be completely decoupled.

It is important to maintain a constant field flux for proper torque control. It is also important to maintain an independently controlled armature current in order to overcome the effects of the detuning of resistance of the armature winding and leakage inductance. A spatial angle of 90 degrees between the flux and MMF axes has to be maintained in order to limit the interaction between the MMF and the flux. If these conditions are met at every instant of time, the torque will always follow the current.

With vector control, the mechanically robust induction motors can be used in high-performance applications where dc motors were previously used. The key feature of the control scheme is the orientation of the synchronously rotating q-d-0 frame to the rotor flux vector. The d-axis component is aligned with the rotor flux vector and regarded as the flux-producing current component. On the other hand, the q-axis current, which is perpendicular to the d-axis, is solely responsible for torque production.

In order to apply a rotor flux field-orientation condition, the rotor flux linkage is aligned with the d-axis, so the q-axis rotor flux in excitation reference frame λ_{qr}^e will be zero, and the d-axis rotor flux in the excitation reference frame will be the rotor flux, $\lambda_{dr}^e = \hat{\lambda}_r$. Therefore, we have

$$i_{ds}^e = \frac{\lambda_{dr}^e}{L_m} \tag{39.23}$$

$$\omega_{slip} = \frac{r_r}{\hat{\lambda}_r}\left(\frac{L_m}{L_r}\right) i_{qs}^e = \frac{L_m i_{qs}^e}{\tau_r \lambda_r} \tag{39.24}$$

$$T_e = \frac{3}{2}\frac{P}{2}\frac{L_m}{L_r}\hat{\lambda}_d i_{qs}^e \tag{39.25}$$

where τ_r is rotor time constant, L_m magnetizing inductance, L_r, rotor leakage inductance, r_r, rotor resistance, i_{qs}^e q-axis stator current in excitation frame, i_{ds}^e d-axis stator current in excitation frame, and ω_{slip} angular frequency of slip. We can find out that in this case, i_{ds}^e controls the rotor flux linkage and i_{qs}^e controls the electromagnetic torque. The reference currents of the q-d-0 axis (i_{qs}^{e*}, i_{ds}^{e*}) are converted to the reference phase voltages (v_{ds}^{e*}, v_{qs}^{e*}) as the commanded voltages for the control loop. Given the position of the rotor flux and two-phase currents, this generic algorithm implements the instantaneous direct torque and flux control by means of coordinate transformations and PI regulators, thereby achieving accurate and efficient motor control.

It is clear that for implementing vector control, we have to determine the rotor flux position. This usually is performed by measuring the rotor position and utilizing the slip relation to compute the angle of the rotor flux relative to the rotor axis.

Equations (39.23) and (39.24) show that we can control torque and field by i_{ds} and i_{qs} in the excitation frame. However, in the implementation of FOC, we need to know i_{ds} and i_{qs} in the stationary reference frame. So, we have to know the angular position of the rotor flux to transform i_{ds} and i_{qs} from the excitation frame to the stationary frame. By using ω_{slip}, which is shown in Eq. (39.24), and using actual rotor speed, the rotor flux position is obtained:

$$\int_0^t \omega_{slip} dt + \theta_{re}(t) = \theta_r(t) \tag{39.26}$$

where $\theta_{re}(t)$ is electric angular rotor position and $\theta_r(t)$ angular rotor flux position.

The current model takes i_{ds} and i_{qs} as inputs and the rotor mechanical speed and gives the rotor flux position as an output. Fig. 39.23 shows the block diagram of the vector-control strategy in which speed regulation is possible using a control loop.

As shown in Fig. 39.23, two-phase currents are measured and fed to the Clarke transformation block. These projection outputs are indicated as i^s_{ds} and i^s_{qs}. These two components of the current provide the inputs to Park's transformation, which gives the currents in the qds^e excitation reference frame. The i^e_{ds} and i^e_{qs} components, which are outputs of the Park transformation block, are compared with their reference values i^{e*}_{ds}, the flux reference, and i^{e*}_{qs}, the torque reference. The torque command, i^{e*}_{qs}, comes from the output of the speed controller. The flux command, i^{e*}_{ds}, is the output of the flux controller that indicates the right rotor flux command for every speed reference. For i^{e*}_{ds}, we can use the fact that the magnetizing current is usually between 40% and 60% of the nominal current. For operating in speeds above the nominal speed, a field-weakening section should be used in the flux controller section. The current regulator outputs, v^{e*}_{ds} and v^{e*}_{qs}, are applied to the inverse Park transformation. The outputs of this projection are v^e_{ds} and v^s_{qs}, which are the components of the stator voltage vector in the dqs^s orthogonal reference frame. They form the inputs of the space-vector PWM block. The outputs of this block are the signals that drive the inverter.

Note that both the Park and the inverse Park transformations require the exact rotor flux position, which is given by the current model block. This block needs the rotor resistance or rotor time constant as a parameter. Accurate knowledge of the rotor resistance is essential to achieve the highest possible efficiency from the control structure. The lack of this knowledge results in the detuning of the FOC. In Fig. 39.23, a space-vector PWM has been used to emulate v^s_{ds} and v^s_{qs} in order to implement current regulation.

39.6.2 DSP Controller Requirements

The controller of the induction motor-control system is used to read the feedback current and position signals, to implement the speed or torque control algorithm, and to generate the gate signals based on the control signal. Analog controllers or digital signal processors, such as LF2407, can perform these tasks.

The interface of the LF2407 is illustrated in Fig. 39.24. Two quadrature counters detect the rising and falling edges of the encoder signals. Two input channels related to the 10-bit ADC are selected to read the two-phase currents. The pins PWM1–PWM6 output the gating signals to the gate drive circuitry.

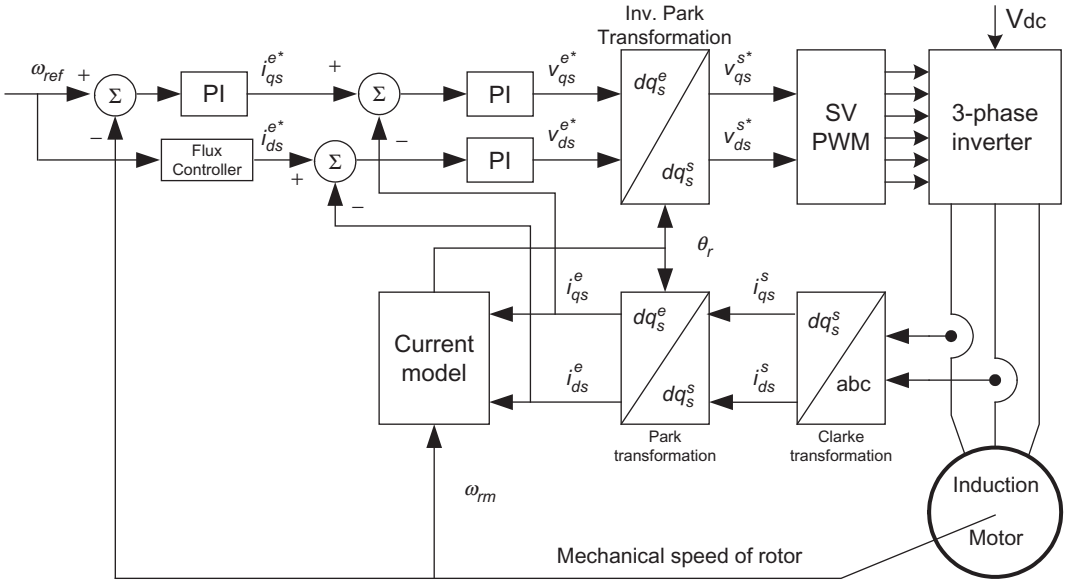


FIG. 39.23 Vector-control algorithm for induction motor.

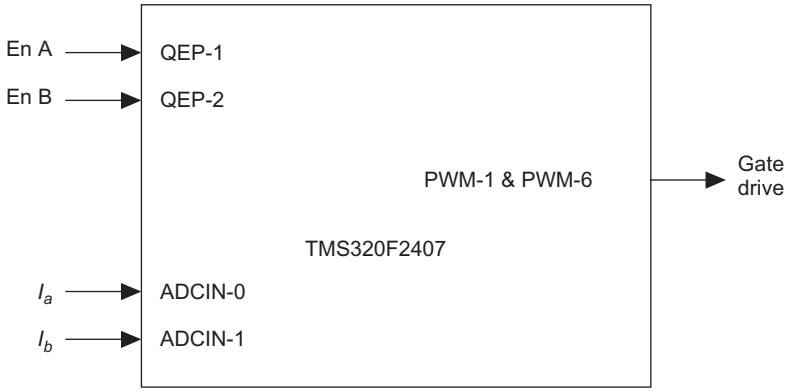


FIG. 39.24 The interface of LF2407.

39.6.3 Implementation of Field-Oriented Speed Control of Induction Motor

Some practical aspects of implementing the block diagram of Fig. 39.24 are discussed in this section and subsections. The software organization, the utilization of different variables, and the handling of the DSP controller resources are described. In addition, the control structure for the per-unit model is presented. Next, some numerical considerations have been made in order to address the problems inherent within the fixed-point calculation. As described, current model is one of the most important blocks in the block diagram depicted in Fig. 39.23. The inputs of this block are the currents and mechanical speed of rotor. In the next sections, technical points that should be considered during current and speed measurement and their scaling are discussed.

39.6.3.1 Software Organization

The body of the software consists of two main modules: the initialization module and the PWM interrupt service routine (ISR) module. The initialization model is executed only once at start-up. The PWM ISR module interrupts the waiting infinite loop when the timer underflows. When the underflow interrupt flag is set, the corresponding ISR is served. Fig. 39.25 shows the general structure of the software. The complete FOC algorithm is executed within the PWM ISR so that it runs at the same frequency as the switching frequency or at a fraction of it. The wait loop could be easily replaced with a user interface.

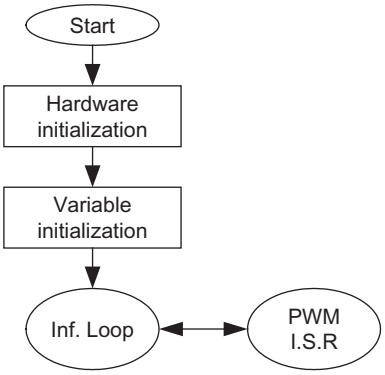


FIG. 39.25 General structure of software.

39.6.3.2 Base Values and Per-Unit Model

It is often convenient to express machine parameters and variables of per-unit quantities. Moreover, the LF2407 is a fixed-point DSP, so using a normalized per-unit model of the induction motor is easier than using real parameters. In this model, all quantities refer to the base values. Base power and base voltage are selected, and all parameters and variables are normalized using these base quantities. Although one might violate this convention from time to time when dealing with instantaneous quantities, the rms values of the rated phase voltage and current are generally selected as the base voltage for the *a-b-c* variables, while the peak value is generally selected as the base voltage for *d-q* variables. The base values are determined from the nominal values by using Eq. (39.27), where I_n, V_n, and f_n are the nominal phase current, the nominal phase-to-neutral voltage, and the nominal frequency in a star-connected induction motor, respectively. The base value definitions are as follows:

$$\begin{aligned} I_b &= \sqrt{2} I_n \\ V_b &= \sqrt{2} V_n \\ \omega_b &= 2\pi f_n \\ \psi_b &= \frac{V_b}{\omega_b} \end{aligned} \tag{39.27}$$

where I_b and V_b are the maximum values of the nominal phase current and voltage, ω_b is the electric nominal rotor flux speed, and ψ_b is the base flux.

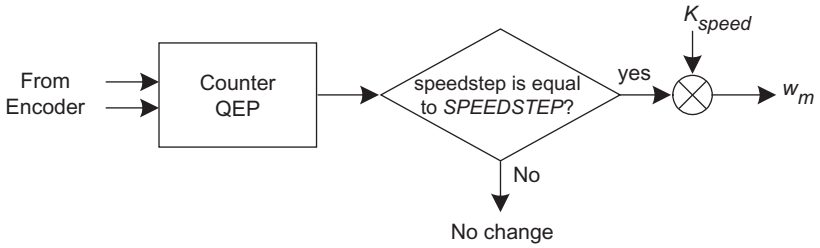


FIG. 39.26 Block diagram of speed feedback calculator.

39.6.3.3 Speed Estimation During High-Speed Region

As previously mentioned, this method is based on counting the number of encoder pulses in a specified time interval. The QEP assigned timer counts the number of pulses and records it in the timer counter register (TxCNT). As the mechanical time constant is much slower than the electric one, the speed regulation loop frequency might be lower than the current loop frequency. The speed regulation loop frequency is obtained in this algorithm by means of a software counter. This counter accepts the PWM interrupt as input clock, and its period is the software variable called SPEEDSTEP. The counter variable is named speedstep. When speedstep is equal to SPEEDSTEP, the number of pulses counted is stored in another variable called n_p, and thus, the speed can be calculated. The scheme depicted in Fig. 39.26 shows the structure of the speed feedback generator.

Assuming that n_p is the number of encoder pulses in one SPEEDSTEP period when the rotor turns at the nominal speed, a software constant K_{speed} should be chosen as follows:

$$01000h = K_{speed} \cdot n_p$$

The speed feedback can then be transformed into a Q4.12 format, which can be used in the control software. In the proposed control system, the nominal speed is 1800 rpm, and SPEEDSTEP is set to 125. The n_p can be calculated as follows:

$$n_p = \frac{1800 \times 64 \times 4}{60} \times \text{SPEEDSTEP} \times T_p = 288 \qquad (39.28)$$

where $T_p = \frac{3}{f_{pwm}} = 3 \times 10^{-4}$ (PWM frequency is 10 kHz, but the program is running at 3333 Hz) and hence K_{speed} is given by

$$K_{speed} = \frac{4096}{288} = 14.22 \Leftrightarrow 0E38h \qquad \text{Q8.8}$$

Note that K_{speed} is out of the Q4.12 format range. The most appropriate format to handle this constant is the Q8.8 format. The speed feedback in Q4.12 format is then obtained from the encoder by multiplying n_p by K_{speed}. The flowchart of speed measurement is presented in Fig. 39.27.

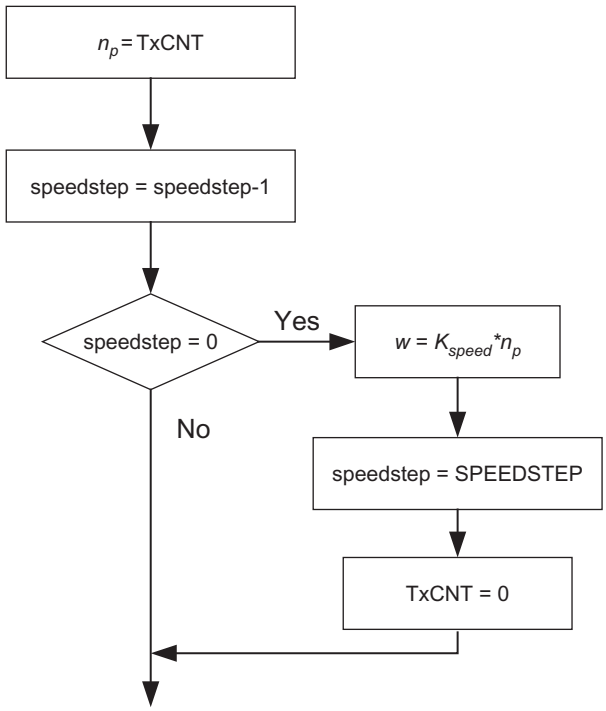


FIG. 39.27 Complete flowchart of speed measurement block during high-speed region.

39.6.3.4 Speed Measurement During Low-Speed Region

To detect the edges of two successive encoder pulses, the developed program can use either the QEP counter or the capture unit input pins. The program has to measure the time between two successive pulses; therefore, it must utilize another GP timer. In this program, timer 3 has been dedicated to the time measurement. During the interrupt service routine of the capture unit or counter QEP, speed can be calculated. To obtain the actual speed of the motor, the appropriate number is divided by the value in the count register of timer 3.

As it can be inferred, at very low speeds, an overflow may occur in timer 3. The counter would then reset itself to zero and start counting up again. This event results in a large error

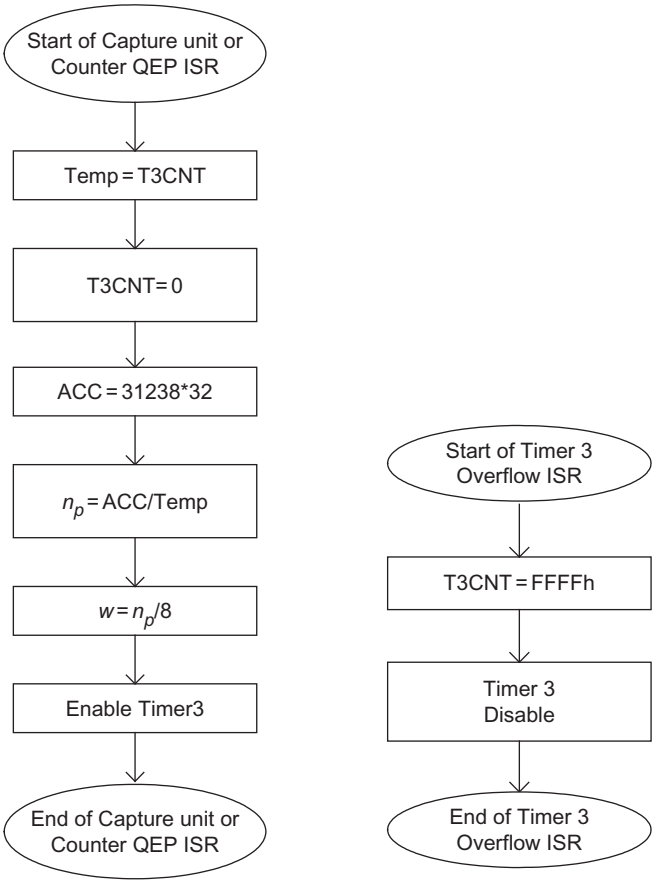


FIG. 39.28 Flowchart of speed measurement at low speed.

in speed measurement. To avoid this event, timer 3 will be disabled in the overflow interrupt service routine. However, this timer is enabled in the capture unit (counter QEP) interrupt.

The flowchart of this implementation is presented in Fig. 39.28.

39.6.3.5 The Current Model

The current model is used to find the rotor flux position. This module takes i_{ds} and i_{qs} as inputs plus the rotor electric speed and then calculates the rotor flux position. The current model is based on Eqs. (39.23) and (39.24). Eq. (39.23) in transient form can be written as

$$\frac{L_r}{r_r L_m}\frac{d\lambda_{dr}}{dt}+\frac{\lambda_{dr}}{L_m}=i_{ds} \tag{39.29}$$

Assume $\lambda_{dr}/L_m = i_m$ where i_m is the magnetizing current; therefore, Eq. (39.29) can be written as follows:

$$T_r\frac{d}{dt}i_m+i_m=i_{ds} \tag{39.30}$$

Rotor flux speed in a per-unit system can be shown by

$$f_s=\frac{1}{\omega_b}\frac{d\theta}{dt}=\omega_{re}+\frac{i_{qs}}{T_r i_m \omega_b} \tag{39.31}$$

where θ is the rotor flux position and $T_r = L_r/r_r$ and ω_{re} are the rotor time constant and rotor electric speed, respectively. The rotor time constant is critical to the correct functionality of the current model. This system outputs the rotor flux speed, which in turn will be integrated to get the rotor flux position. Assuming that $i_{qs_{(k+1)}} \approx i_{qs_{(k)}}$, Eqs. (39.30) and (39.31) can be discretized as follows:

$$\begin{aligned} i_{mr_{(k+1)}} &= i_{mr_{(k)}}+\frac{T_p}{T_r}\left(i_{ds_{(k)}}-i_{mr_{(k)}}\right)\\ f_{S_{(k+1)}} &= n_{(K+1)}+\frac{1}{T_r\omega_b}\frac{i_{qs_{(k)}}}{i_{mr_{(k+1)}}} \end{aligned} \tag{39.32}$$

For example, let the constants T_p/T_r and $1/T_r\omega_b$ be renamed to K_t and K_t, respectively. Here, $L_r = 73.8$ mH, $r_r = 0.73\ \Omega$, and $f_n = 60$ Hz. So for K_t and K_r, we have

$$\begin{aligned} K_r &= \frac{T_p}{T_r}=\frac{(10000/3)^{-1}}{101.09\times10^{-3}}\\ &= 2.967\times10^{-3}\Leftrightarrow 000Ch \end{aligned} \tag{Q4.12}$$

$$\begin{aligned} K_t &= \frac{1}{T_r\omega_b}=\frac{1}{30.232\times10^{-3}\times377}\\ &= 26.237\times10^{-3}\Leftrightarrow 006Bh \end{aligned} \tag{Q4.12}$$

By knowing the rotor flux speed (f_s), the rotor flux position (θ_{cm}) is computed by the integration formula in the per-unit system:

$$\theta_{cm_{(k+1)}}=\theta_{cm_{(k)}}+\omega_b\cdot f_{s_{(k)}}\cdot T \tag{39.33}$$

In Eq. (39.33), let $\omega_b f_s T$ be called θ_{inc}. This variable is the rotor angle variation within one sampling period. Thus, the current model module has three input variables i_{ds}, i_{ds}, and ω_{re} and one output, which is the rotor flux position θ_{cm} represented as a 16-bit integer value. The flowchart of the field-oriented speed control of induction motor is presented in Fig. 39.29. This routine is placed inside the PWM interrupt service routine.

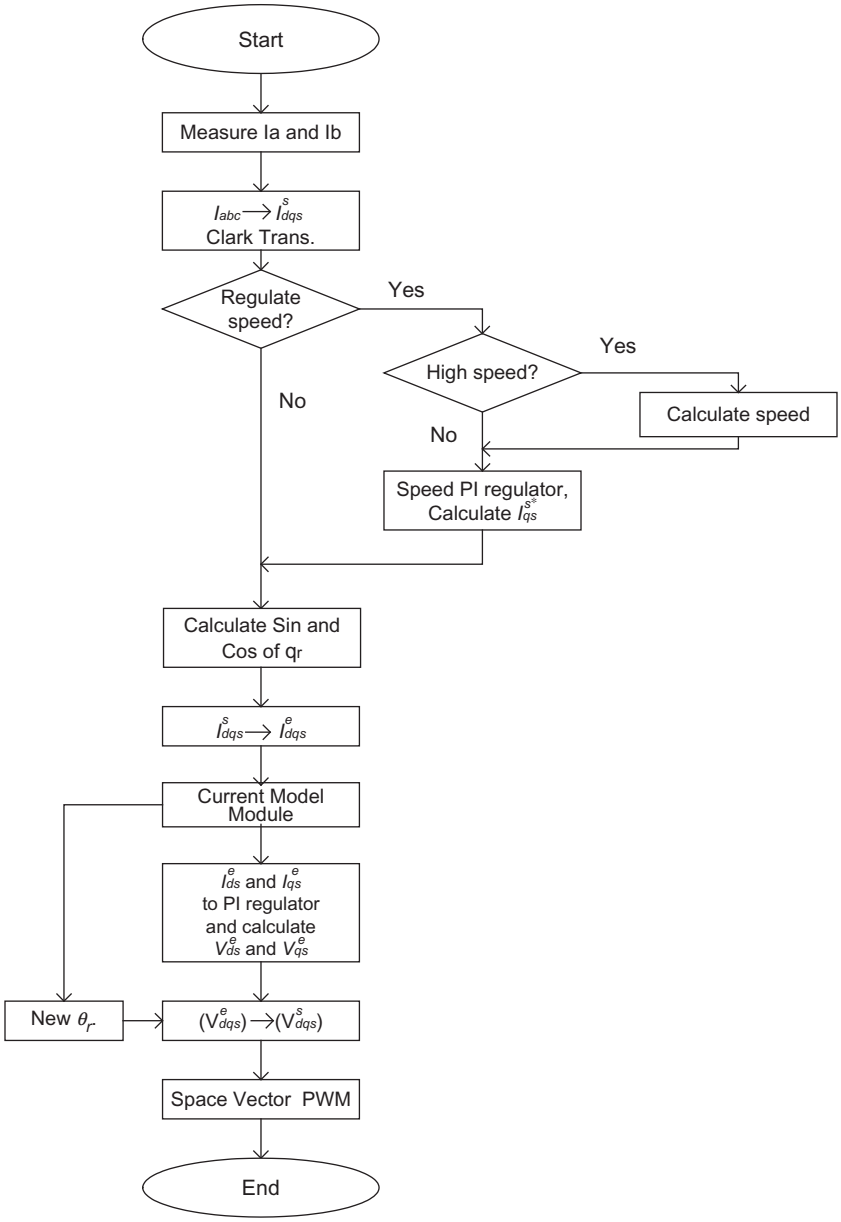


FIG. 39.29 Flowchart of digital implementation of FOC algorithm.

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Predictive Control of Power Electronic Converters

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40.1 Introduction

In recent years, power electronic converters have been involved in many applications from industrial level (motor drives, renewable energy technologies, etc.) to home level (PCs, home appliances, etc.). Therefore, the widespread use of power electronic converters puts their control requirements at the forefront. Traditionally, the control techniques in such converters are supposed to have good dynamic response and high reference tracking accuracy. In addition to these requirements, modern control methods should take into account some technical specifications and constraints to meet national and international standards and grid codes. Although these requirements often can be met with the hardware modifications, this results in extra cost. Thus, this shift in trend has driven the development of more advanced control methods, which should fulfill many control objectives at the same time [1].

One of these control methods is predictive control that has appeared as an attractive solution for the control of power converters due to its fast dynamic response and increased control accuracy [1–3]. Originally, this method was introduced in the process industry, but a very innovative and early paper applied predictive control for power electronics [4]. The main approach is based on the computation of the future system dynamic to calculate optimal actuation variables. Therefore, this technique requires a high amount of calculations, compared with classic control schemes; fortunately, parallel computational capable microprocessors are available in the current market to make possible the implementation of predictive control [5].

Furthermore, predictive control brings considerable benefits to power electronics systems. First of all, concepts are intuitive and easy to understand and implement, it can be applied to a variety of systems, it allows for nonlinearities and constraints to be incorporated into the control law in a straightforward manner, a multivariable case can be considered, and the resulting controller is easy to implement. However, the method requires a high amount of calculations, compared with a classic control scheme; however, the fast microprocessors available today make possible the implementation of predictive control. Generally, the quality of the controller depends on the quality of the model [6].

The aim of this chapter is to provide a comprehensive overview of predictive control and to illustrate its use in power electronic converters. It starts with an overview of predictive control theory. Then, predictive control types are presented along with a description of advantages and disadvantages of each type of predictive control. After that, implementation of MPC for power electronic converters is described. Finally, two case studies are given with simulation and experimental results.

40.2 Theory of Predictive Control

The main idea of the predictive control can be roughly explained as follows: it uses a discrete-time model of the system

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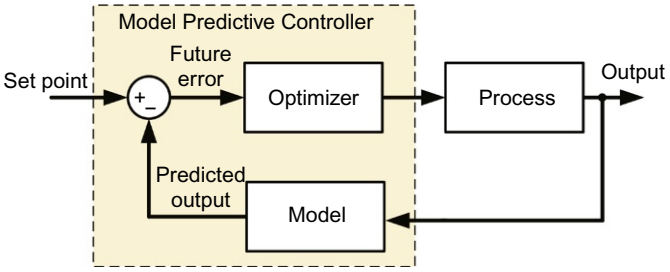


FIG. 40.1 A principle block diagram of predictive control.

to forecast the future behavior of the controlled parameters during a certain time window called a receding horizon. A basic block diagram of this control technique is given in Fig. 40.1 [7]. It can be seen that predictive control consists of two main blocks: model and optimizer. To predict behavior of the system at the next sampling time, the system discrete-time model is used. Then, the future error between predicted output and the reference value is minimized by using predefined cost function in the optimizer. To sum up briefly, the basic idea of MPC can be explained as follows:

- A discrete-time model of the system should be obtained in order to predict system output at the next sampling instant.
- To obtain the optimal actuation, the cost function is used in the optimizer block.

The system prediction model can be defined as state space model as follows:

$$x(k+1) = Ax(k) + Bu(k) \tag{40.1}$$

$$y(k) = Cx(k) + Du(k) \tag{40.2}$$

where $x(k+1)$, $u(k)$, and y(k) are the state variable vector, the input vector, and the output vector, respectively. Furthermore, A is the system matrix, B is the control matrix, C is the output matrix, and D is the feedthrough matrix. The prediction model can be obtained by combining N equations at $k+1$th through $k+N$th instants as follows [8]:

$$\begin{bmatrix} x(k+1) \\ x(k+2) \\ .. \\ x(k+N) \end{bmatrix} = \begin{bmatrix} A \\ A^2 \\ .. \\ A^N \end{bmatrix} x(k) + \begin{bmatrix} B & 0 & 0 & 0 \\ AB & B & 0 & 0 \\ .. & .. & .. & .. \\ A^{N-1}B & A^{N-2}B & .. & B \end{bmatrix} \begin{bmatrix} u(k) \\ u(k+1) \\ .. \\ u(k+N-1) \end{bmatrix} \tag{40.3}$$

This prediction model can be expressed as

$$x(k+1:k+N) = \hat{A}x(k) + \hat{B}u(k:k+N-1) \tag{40.4}$$

$$x(:) = \hat{A}x(k) + \hat{B}u(:) \tag{40.5}$$

A cost function (g) is needed to be determined to select an optimal actuation in the next sampling time. Since the objective of the controller is to guide the system state toward zero from any given initial conditions, the cost function can be defined as follows:

$$\begin{aligned} g &= \|x(:)\|^2 + \lambda\|u(:)\|^2 = \left\|\hat{A}x(k) + \hat{B}u(:)\right\|^2 + \lambda\|u(:)\|^2 \\ &= u(:)^T\left(\hat{B}^T\hat{B} + \lambda I\right)u(:) + u(:)^T\hat{B}^T\hat{A}x(k) + x(k)^T\hat{A}^T\hat{B}u(:) \\ &\quad + x(k)^T\hat{A}^T\hat{A}x(k) \end{aligned} \tag{40.6}$$

where λ is a weighting factor. Taking the derivative of the cost function with respect to $u(:)$ and setting it to zero, one obtains

$$\frac{dg}{du(:)} = 2\left(\hat{B}^T\hat{B} + \lambda I\right)u(:) + 2\hat{B}^T\hat{A}x(k) = 0 \tag{40.7}$$

whose solution is

$$u(:) = -\left[\left(\hat{B}^T\hat{B} + \lambda I\right)^{-1}\hat{B}^T\hat{A}\right]x(k) \tag{40.8}$$

Following the fundamental concept behind predictive control, only the first vector from the array of the optimally predicted future control inputs in Eq. (40.8) is utilized. Hence, the control input vector at the kth time instant can be found to be

$$u(k) = [I \;\; 0 \;\; \ldots \;\; 0]u(:) \tag{40.9}$$

Fig. 40.2 illustrates the working principle of predictive control. The future values of the system states are predicted until a predefined horizon in time $k+$N using the system model and the available measured data until time k. The sequence of the optimal actuation is calculated by minimizing the cost function. This process is repeated taking into account the new measured data for each sampling time [9].

40.3 Types of Predictive Control

The classification of predictive control in power electronic converters can be divided into four main categories, as shown in Fig. 40.3 [10]. The deadbeat control consists of determining which input signal must be applied to the system to ensure the output reaches steady state in the smallest number of time steps. Although deadbeat control requires a modulator, it provides constant switching frequency and requires low computation burden to be implemented in digital platforms. The optimization criterion in the hysteresis-based predictive control is to keep the controlled variable within the boundaries of a hysteresis area, while in the trajectory based, the variables are forced to follow a predefined trajectory. Furthermore, hysteresis-based and trajectory-based predictive controls can be accepted as direct control technique, which means that it doesn't need modulator stage; however, switching frequency is variable. Model predictive control (MPC), which is the most significant predictive control technique for power electronic converters among the others, can be classified in two categories: continuous control set MPC (CCS-MPC) and finite control set

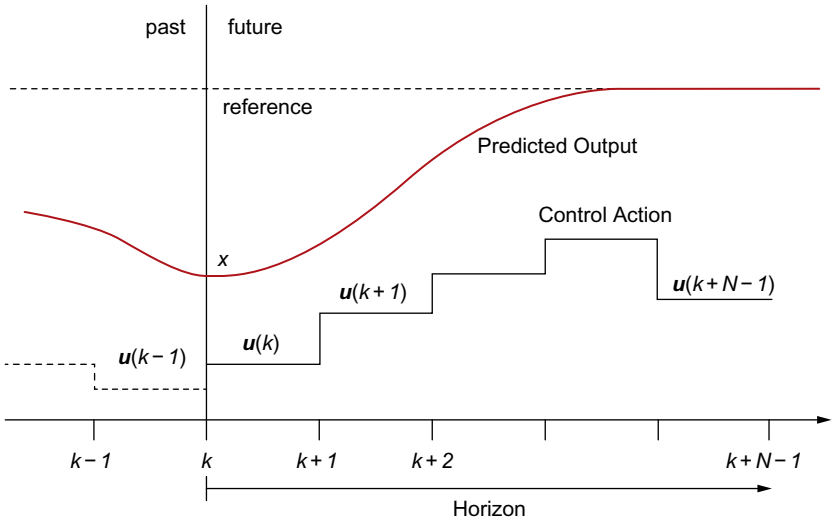


FIG. 40.2 Working principle of predictive control.

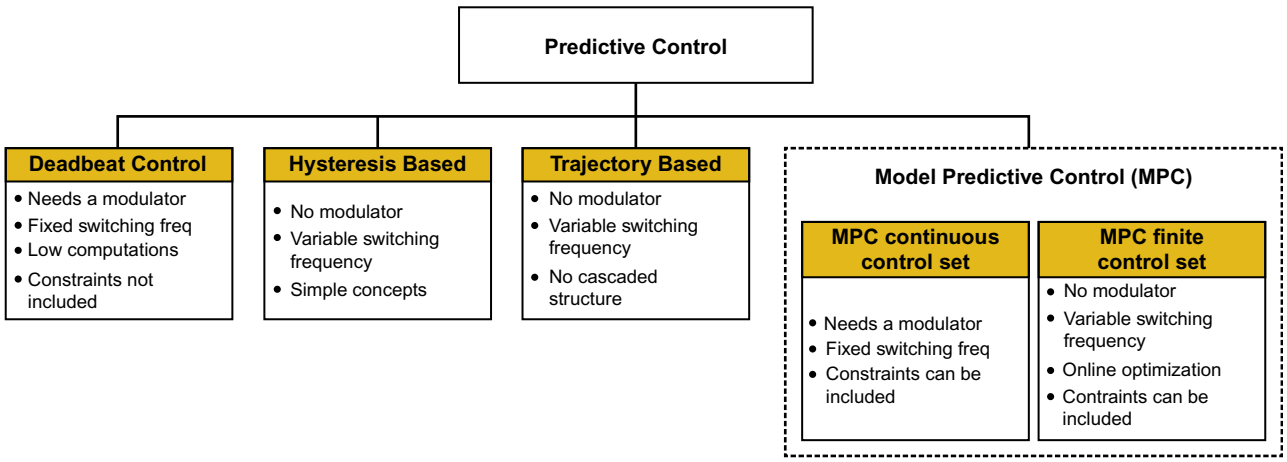


FIG. 40.3 The classification of predictive control techniques.

MPC (FCS-MPC). CCS-MPC requires a modulator to generate the switching states, while in FCS-MPC, the switching state can be generated without modulator stage. In FCS-MPC approach, to solve the optimization problem, the power converters' finite number of switching states is used. To do that, a discrete-time model of the system should be employed to predict the future behavior of the system. Then, an optimal control actuation is selected by the predefined cost function. Although FCS-MPC can generate switching signals without a modulator, switching frequency is variable.

Simplicity and easy implementation concept are the most important advantages of predictive control. Using predictive control technique also allows avoiding the cascaded control structure, which results in fast dynamic response in control. Furthermore, some constraints can be included in the control in order to improve the system performance. Although these advantages can be easily implemented in some predictive control techniques such as MPC, but it is very difficult to add in deadbeat control.

40.4 Model Predictive Control for Power Electronics

In this subsection, the implementation of MPC for power electronic converters will be explained step by step. Although this technique is suitable for all power electronic converters, traditional three-phase three-leg voltage source inverter (VSI) will be taken as an example to explain the MPC idea for power converters.

The block diagram of the MPC for three-phase VSI is shown in Fig. 40.4. This control technique can be summarized by the following steps:

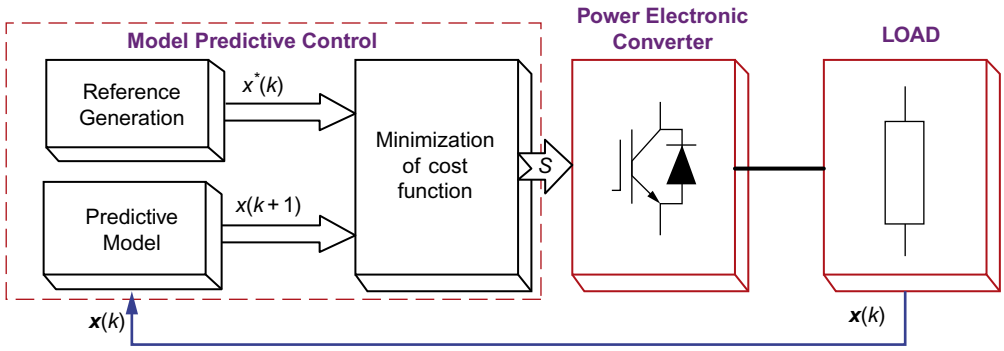


FIG. 40.4 Model predictive control block diagram for three-phase VSI.

- Build a model of the converter and determine the possible switching states.
- Build a model of the load for the predictive model.
- Define a cost function to minimize the error.

40.4.1 Converter Model

The traditional three-phase VSI with *RL* load and VSI equivalent circuits are shown in Fig. 40.5 [11]. As shown, each leg can be represented as a dual-way switch, so only one switch can be active simultaneously in the same leg in order to avoid short circuit. The switching states S_a, S_b, S_c are controlled as follows:

$$S_a = \begin{cases} 1, & \text{if } S_1 \text{ on and } S_4 \text{ off} \\ 0, & \text{if } S_1 \text{ off and } S_4 \text{ on} \end{cases} \tag{40.10}$$

$$S_b = \begin{cases} 1, & \text{if } S_2 \text{ on and } S_5 \text{ off} \\ 0, & \text{if } S_2 \text{ off and } S_5 \text{ on} \end{cases} \tag{40.11}$$

$$S_c = \begin{cases} 1, & \text{if } S_3 \text{ on and } S_6 \text{ off} \\ 0, & \text{if } S_3 \text{ off and } S_6 \text{ on} \end{cases} \tag{40.12}$$

These switching states can be expressed as

$$S = \frac{2}{3}\left(S_a + \mathrm{a}S_b + \mathrm{a}^2 S_c\right) \tag{40.13}$$

where **a** is called as a unitary vector and is equal to $e^{j2\pi/3}$. Finally, the inverter output voltage vector can be defined as a function of the switching state vector ***S*** by

$$\mathrm{v} = V_{dc}\mathrm{S} \tag{40.14}$$

where V_{dc} is the dc-link voltage.

Considering all the possible combinations of the switches (S_a, S_b, S_c), eight switching states and consequently eight voltage vectors can be obtained, as shown in Fig. 40.6. Six of these vectors (v_1–v_6) are defined as active vectors, while the other two (v_0, v_7) are defined as zero vector. Consequently, seven different voltage vectors are obtained as shown in Fig. 40.6.

40.4.2 Discrete-Time Model of Load for Prediction

The equivalent circuit of the three-phase VSI with *RL* load is shown in Fig. 40.7. The continuous-time model of the system can be expressed as

$$\begin{bmatrix} v_{aN} \\ v_{bN} \\ v_{cN} \end{bmatrix} = \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & L \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} + \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} v_{nN} \tag{40.15}$$

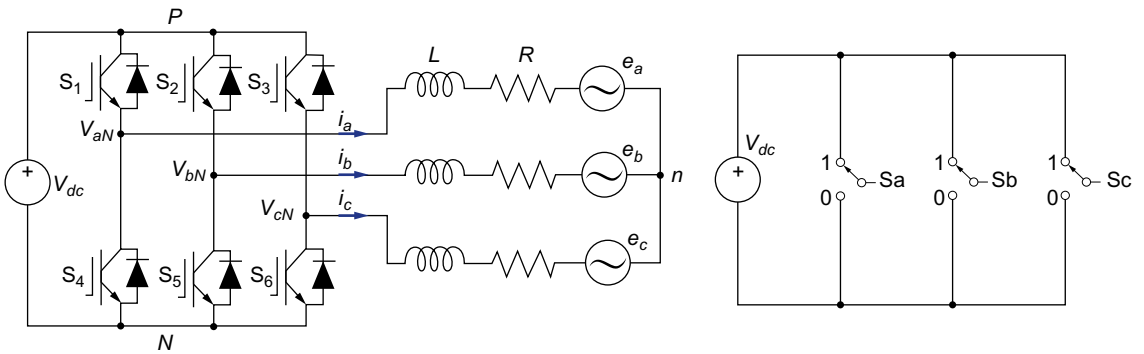


FIG. 40.5 Three-phase three-leg voltage source inverter circuit with *RL* load and its equivalent circuit.

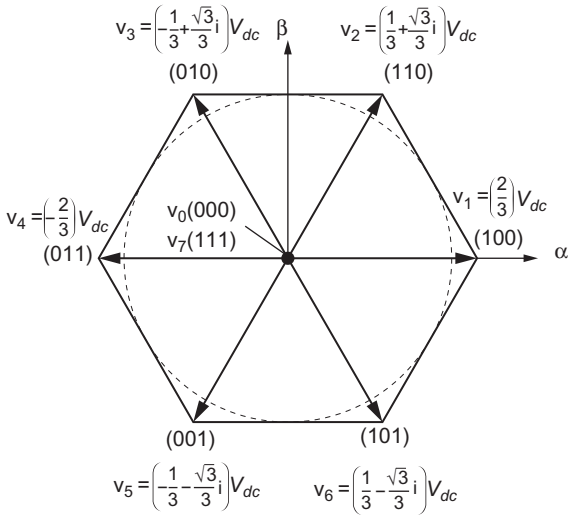


FIG. 40.6 Voltage vectors of the three-phase three-leg inverter.

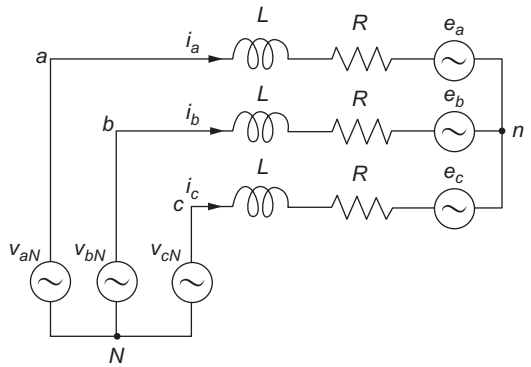


FIG. 40.7 Equivalent circuit of the three-phase VSI with *RL* load.

where R and L are the load resistance and the load inductance, respectively. This equation can be simplified as

$$\mathbf{v} = R\mathbf{i} + L\frac{d\mathbf{i}}{dt} + \mathbf{e} \tag{40.16}$$

where $\mathbf{v}$ is inverter output voltage vector, $\mathbf{i}$ is the load current vector, and $\mathbf{e}$ the load back-emf vector. The derivative of the output current vector can be obtained from

$$\frac{d\mathbf{i}}{dt} = \frac{1}{L}[(\mathbf{v} - \mathbf{e}) - R\mathbf{i}] \tag{40.17}$$

To use mathematical equations in the prediction model, discrete-time equations of the system must be obtained from continuous-time equations. To do that, the general structure of forward-difference Euler equation (40.18) can be used in order to compute the differential equations of the output current [12,13]:

$$\frac{df}{dt} \asymp \frac{f(x_0 + h) - f(x_0)}{h} \tag{40.18}$$

To estimate these variables in the next sampling time, the discretization equation can be defined as

$$\frac{\Delta f(k)}{\Delta t} \asymp \frac{f(k+1) - f(k)}{T_s} \tag{40.19}$$

The continuous-time expression for the i_{abc} is given in (40.17). By substituting (40.19) into (40.17), the discrete-time model of the i_{abc} can be obtained as

$$\mathbf{i}(k+1) = \left(1 - \frac{RT_s}{L}\right)\mathbf{i}(k) + \frac{T_s}{L}(\mathbf{v}(k) - \hat{\mathbf{e}}(k)) \tag{40.20}$$

where $\mathbf{i}(k+1)$ is the predicted output current vector at the next sampling time and $\hat{e}(k)$ denotes the estimated back emf that can be calculated from (40.16) considering the measurements of the load voltage and current with the following expression;

$$\hat{\mathbf{e}}(k-1) = \mathbf{v}(k-1) - \frac{L}{T_s}\mathbf{i}(k) - \left(R - \frac{L}{T_s}\right)\mathbf{i}(k-1) \tag{40.21}$$

where $\hat{e}(k-1)$ is the estimated value of $e(k-1)$.

40.4.3 Cost Function Optimization

The objective of the cost function is to minimize the error between the reference currents ($i_{abc}{}^{*}(k)$) and the predicted output currents ($i_{abc}(k+1)$) at the next sampling time. The cost function can be expressed in orthogonal coordinates as

$$\begin{aligned} g &= \left|i^*_{abc}(k) - i^p_{abc}(k+1)\right| \\ &= \left|i^*_{\alpha}(k) - i^P_{\alpha}(k+1)\right| + \left|i^*_{\beta}(k) - i^P_{\beta}(k+1)\right| \end{aligned} \tag{40.22}$$

where $i^P_{\alpha}(k+1)$ and $i^P_{\beta}(k+1)$ are the real and imaginary parts of the predicted load current vector, while $i^*_{\alpha}(k+1)$ and $i^*_{\beta}(k+1)$ are the real and imaginary parts of the reference load current. To simplify the analysis, it is assumed that the reference current does not change immediately in one sampling time. Thus, $i^*_{abc}(k+1) = i^*_{abc}(k)$ can be considered. On the other hand, this may introduce a one sample delay in the reference tracking, which can be neglected in high sampling frequency conditions. In general, the reference current is generated from an external control loop, for example, maximum power point tracking control loop.

The sketch map of the reference and predicted rotor currents is shown in Fig. 40.8 to illustrate how the proposed MPC strategy works. Here, the measured output current i_a(k) and voltage vectors $\mathbf{v_{0\text{-}7}}$, which are given in Table 40.1, have been evaluated together to estimate the future output current $i_a(k+1)$ values. As shown in Fig. 40.8, there are eight different predicted rotor current values at time $k+1$ and $k+2$. However, it can be seen from the figure that only v_2 and v_3 voltage vectors minimize the error of the output current at $k+1$ and $k+2$ instants, respectively. Thus, voltage vectors that minimize the cost function g are v_2 at $k+1$ and v_3 at $k+2$ are selected. In other words,

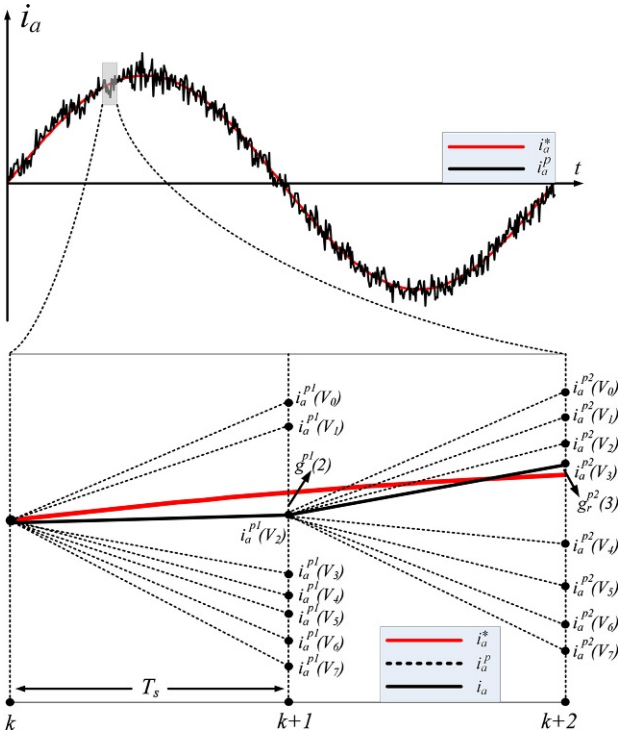


FIG. 40.8 The sketch map of the reference and predicted currents.

TABLE 40.1 Switching states and voltage vectors of three-phase VSI

Switching state	S_a	S_b	S_c	Voltage vector V
0	0	0	0	$\mathbf{V_0}=0$
1	1	0	0	$\mathbf{V}_1=\frac{2}{3}V_{dc}$
2	1	1	0	$\mathbf{V}_2=\frac{1}{3}V_{dc}+j\frac{\sqrt{3}}{3}V_{dc}$
3	0	1	0	$\mathbf{V}_3=-\frac{1}{3}V_{dc}+j\frac{\sqrt{3}}{3}V_{dc}$
4	0	1	1	$\mathbf{V}_4=-\frac{2}{3}V_{dc}$
5	0	0	1	$\mathbf{V}_5=-\frac{1}{3}V_{dc}-j\frac{\sqrt{3}}{3}V_{dc}$
6	1	0	1	$\mathbf{V}_6=\frac{1}{3}V_{dc}-j\frac{\sqrt{3}}{3}V_{dc}$
7	1	1	1	$\mathbf{V}_7=0$

corresponding voltage vector at each sample time is determined by the cost function according to the minimum error or distance between reference and predicted currents. As a result, it can be shown that v_2 and v_3 voltage vectors produce the lowest value of the cost function at $k+1$ and $k+2$ instants, respectively.

40.4.4 Control Algorithm

The MPC algorithm can be implemented as a "*for*" loop to predict future behavior of the system output, minimize the error between the reference and predicted output using predefined cost function, and store the index value of the corresponding switching state [14,15]. The flowchart of the MPC algorithm is given in Fig. 40.9. The control algorithm can be summarized by the following steps:

- Measure the output currents (i_{abc}).
- Estimate the back emf using Eq. (40.21).
- These measured and estimated values are used to predict output currents using the predictive model in Eq.(40.20).
- All predictions are evaluated using the predefined cost function.
- The optimal switching state that corresponds to the optimal voltage vector that minimizes the cost function is selected to be applied at the next sampling time.

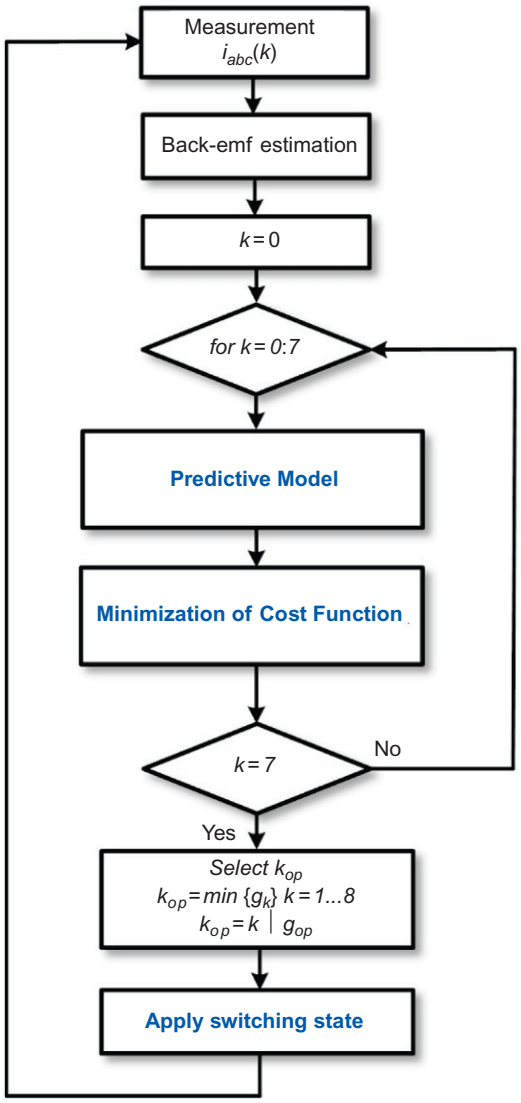


FIG. 40.9 Flowchart of the model predictive control of three-phase VSI.

40.5 MPC Applications in Power Electronic

40.5.1 Three-Level Neutral-Point-Clamped Inverter

Motivated by the aforementioned advantages of MPC and considering the multiobjective control requirements of neutral-point-clamped (NPC) inverter, in this subsection, MPC-based control technique for three-phase NPC inverter is presented. Here, two parameters, the output current and the capacitor voltages, are controlled by the MPC technique. Thus, multiobjective control requirement is solved with simple technique.

A. System Model

The used three-phase NPC inverter topology is illustrated in Fig. 40.10. Each leg of the inverter consists of four power switches with two diodes that allow the output terminal to be connected to the middle point of the split dc-link capacitors. This circuit configuration allows to generate three voltage levels at the output of the inverter according to the neutral point. The switching combinations are given in Table 40.2 [16]. Switching state variable S_x represents the switching state of phase x, with $x = a, b, c$, and it has three possible values denoted by positive, zero, and negative that represent the switching combinations that generate $V_{dc}/2$, 0, and $-V_{dc}/2$, respectively, at the output of the inverter phase.

The NPC inverter applies to the load 19 voltage vectors, which are generated from 27 switching states, as shown in Fig. 40.11 [16]. In addition to these switching states, for this application, one extra switching state is required to ensure shoot-through state. During this state, dc link must be short-circuited by single or multiple inverter legs.

TABLE 40.2 Switching states for one phase of the NPC inverter

S_x	S_{x1}	S_{x2}	S_{x3}	S_{x4}	v_{x0}
+	1	1	0	0	$V_{dc}/2$
0	0	1	1	0	0
−	0	0	1	1	$V_{dc}/2$

The continuous-time expression for the output current (i_o) can be described by the following equation:

$$L\frac{d\mathbf{i}(t)}{dt} = \mathbf{v}(t) - R\mathbf{i}(t) - \mathbf{e}(t) \tag{40.23}$$

where R and L are the load resistance and inductance, respectively, $\mathbf{v}$ is the voltage vector generated by the inverter, $\mathbf{e}$ is the electromotive force of the load, and $\mathbf{i}$ is the load current vector. These vectors are defined as

$$\left.\begin{aligned} \mathbf{v} &= \frac{2}{3}\left(V_a + aV_b + a^2V_c\right) \\ \mathbf{i} &= \frac{2}{3}\left(i_a + ai_b + a^2i_c\right) \\ \mathbf{e} &= \frac{2}{3}\left(e_a + ae_b + a^2e_c\right) \end{aligned}\right\} \tag{40.24}$$

where $a = e^{j(2\pi/3)}$.

B. MPC-based control algorithm

The proposed MPC algorithm applied to the three-level NPC inverter is shown in Fig. 40.12. To predict the output current ($\mathbf{i}_o$) and the capacitor voltages (v_{C1} and v_{C2}) at the next sampling time, discrete-time model of the inverter must be defined. One way to obtain discrete-time models is to use the forward-difference Euler equation due to its simplicity. The derivative form $dx(t)/dt$ is approximated by

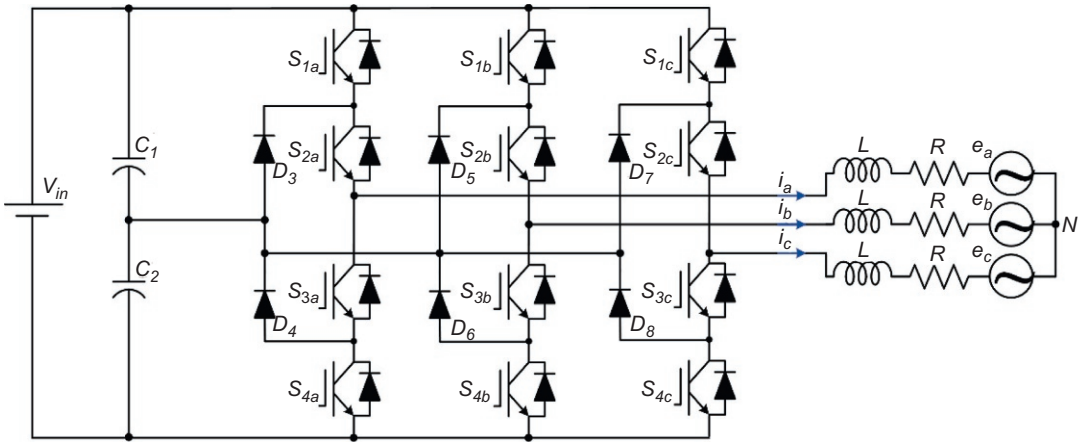


FIG. 40.10 Three-phase three-level NPC inverter topology.

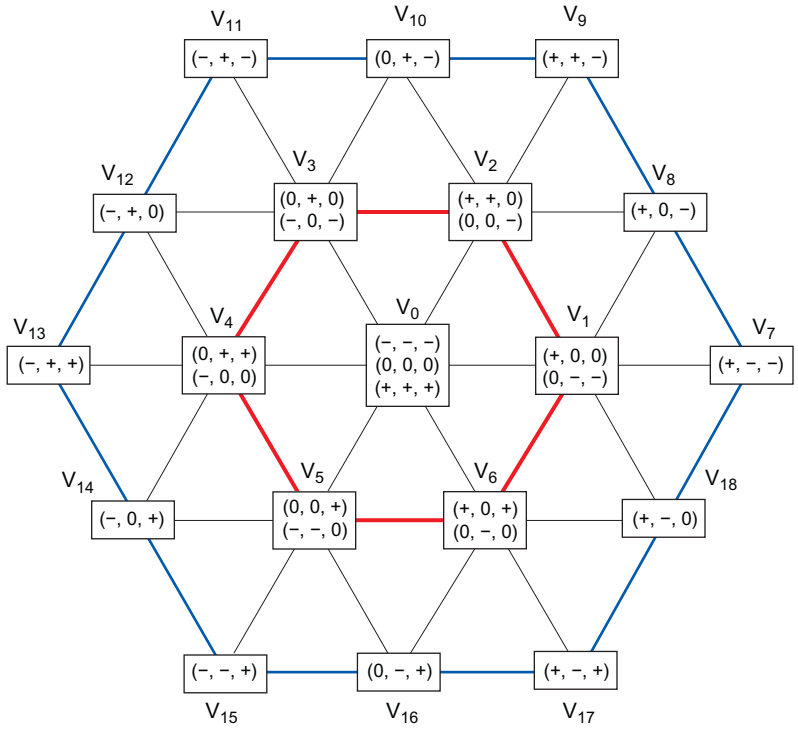


FIG. 40.11 Possible voltage vectors and switching states generated by a three-level NPC inverter.

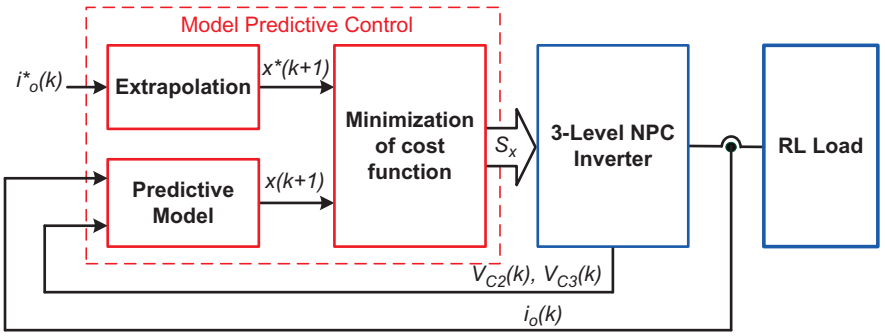


FIG. 40.12 Block diagram of the proposed MPC technique.

$$\frac{dx(k)}{dt} \approx \frac{x(k+1)-x(k)}{T_s} \tag{40.25}$$

where T_s is the sampling time and x is one of the control parameters such as $\mathbf{i}$ and v_{c12}.

By substituting (40.23) into (40.25), the discrete-time model of the output current vector is

$$\mathbf{i}(k+1) = \frac{T_s}{RT_s + L}\left[\frac{L}{T_s}\mathbf{i} + \mathbf{v}(k+1) - \mathbf{e}(k+1)\right] \tag{40.26}$$

where $\mathbf{i}$ $(k+1)$ is the predicted output current vector at the next sampling time.

The current prediction in (40.26) also requires an estimation of the future load back EMF $\mathbf{e}$ (k+1). It can be estimated by using a second-order extrapolation from present and past values. From (40.25) and the output voltage and current, resulting in the following expression:

$$\hat{\mathbf{e}}(k) = \mathbf{v}(k) + \frac{L}{T_s}\mathbf{i}(k-1) - \frac{RT_s + L}{T_s}\mathbf{i}(k) \tag{40.27}$$

where $\hat{e}(k)$ is the estimated value of $\mathbf{e}(k)$.

Furthermore, the discrete-time equations of the capacitor voltage can be expressed by using (40.25):

$$v_{C12}(k+1) = v_{C12}(k) + \frac{T_s}{C} i_{C12}(k) \tag{40.28}$$

where v_{C12}(k+1) is the predicted capacitor voltages, at the next sampling time.

To use reference value in the cost function, this value must be extrapolated to $k+1$ instant. To do that, Lagrange's extrapolation can be used [17]. Once the extrapolated reference values obtained, they are applied in the cost function optimization block as can be seen in Fig. 40.12. To handle the desired control objectives, two terms are required to be defined in the cost function. The terms are responsible for minimizing the error between the reference and predicted values. The defined cost function is

$$g(k+1) = \left|i_\alpha^*(k+1) - i_\alpha(k+1)\right| + \left|i_\beta^*(k+1) - i_\beta(k+1)\right| + \lambda\left|v_{C1}(k+1) - v_{C2}(k+1)\right| \tag{40.29}$$

where λ is the weighting factor.

C. Simulation Results

The simulation of the proposed system was performed using Matlab/Simulink environment. The NPC inverter topology, shown in Fig. 40.10, is used in the simulation. The parameters used in the simulation are summarized in Table 40.3.

The simulation result of steady-state analysis is shown in Fig. 40.13. The reference output currents track their references with high accuracy, while the dc-link voltage is kept balanced by the MPC. Fig. 40.14 shows the simulation result of the transient response of the proposed control technique. The output reference current is step changed from 10 to 15 A. It can be seen that the dc-link voltage remains balanced at 150 V, with small deviations during the transient.

40.5.2 33-Level Input Switched Inverter

The control of multilevel inverters (MIs) is quite challenging and requires a flexible approach to success multiple control objectives. The MPC technique is extremely effective to control MIs due to its considerable advantages over the traditional linear controller. This subsection presents MPC technique for 33-level input switched multilevel inverter (ISMI) to verify MPC's effectiveness in the high-level MI topologies.

TABLE 40.3 System parameters

Parameters	Values
Input DC voltage, V_{DC}	300 V
qZS Network inductance, L_1 and L_2	1 mH
qZS Network capacitance, C_1 and C_2	470 μF
Load resistance, R	10 Ω
Load inductance, L	10 mH
Sampling time, T_s	100 μs

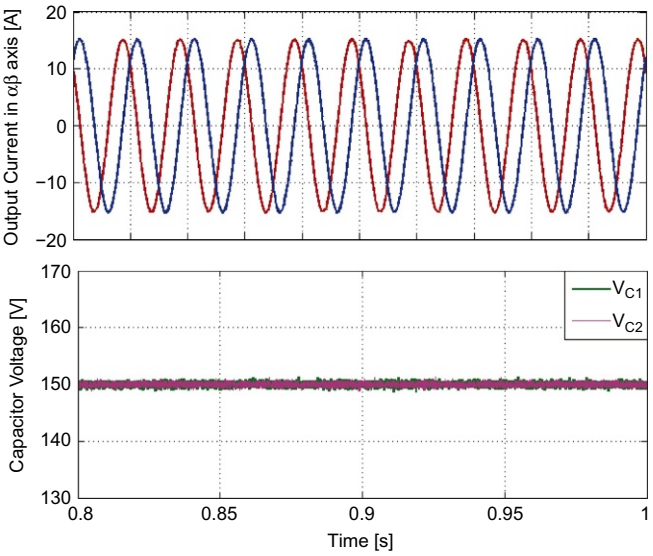


FIG. 40.13 Simulation results of steady-state operation.

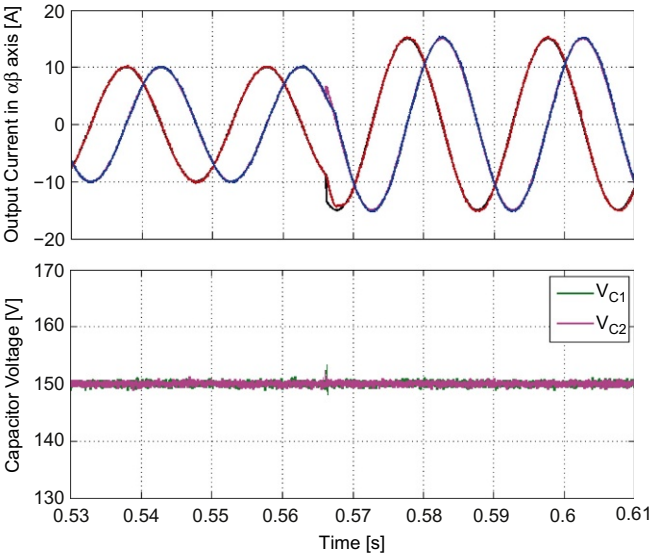


FIG. 40.14 Simulation results of transient response.

A. Overview of the ISMI

The circuit diagram of the single-phase 33-level ISMI with PV generation system is shown in Fig. 40.15 [18]. The ISMI topology has two stages, consisting of the multilevel module and H-bridge inverter. Output voltage level of this topology is given by $N_{level} = 2n+1$, where n represents the number of power legs. In order to obtain 33 voltage level, n should be 16 for this application.

In the first stage, each leg includes two power switches that allow bidirectional current flow. Sixteen capacitors are also employed to divide the dc-link voltage equally to

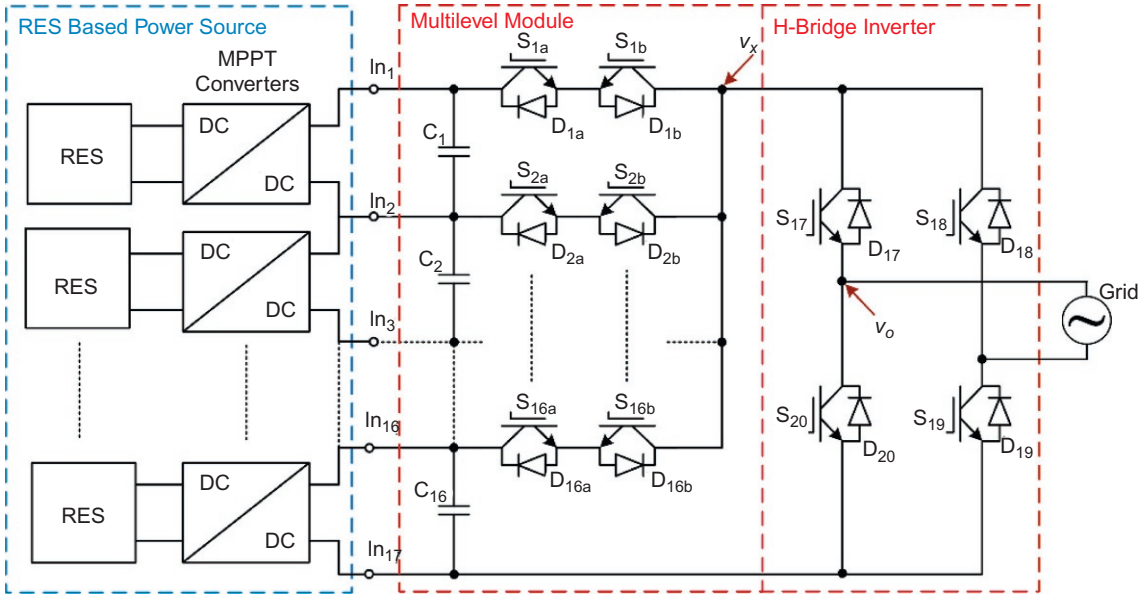


FIG. 40.15 The block diagram of single-phase 33-level ISMI in PV generation system.

V_{dc}/16, as seen in Fig. 40.15. The bidirectional power switches of each leg should be gated on sequentially to obtain desired voltage level. It is noticeable that more than one leg switches cannot be turned on at the same time because input dc source would be short circuit. Moreover, the switching state of the multilevel module is determined by the output current direction and the voltage level of the multilevel module. For example, when the first leg (S_{1ab}) is turned on and other legs are turned off, the output voltage (v_x) of the multilevel module is V_{dc}, the current flows through S_{1a} and D_{1b}. The proposed ISMI has 64 switching states that produce thirty-three voltage levels. However, it should be noted that the voltage level of the multilevel module is only 16 positive levels. Therefore, to obtain positive and negative levels, the traditional H-bridge inverter is employed in the second stage of this topology, as seen in Fig. 40.15. The H-bridge inverter provides voltage gains, which are +1, 0, −1, to ensure positive, zero, and negative voltage on the output. The switching states of 33-level ISMI are given in Table 40.4.

B. MPC-based control algorithm for 33-level ISMI

The block diagram of the MPC strategy applied to the current control for the 33-level grid-connected ISMI is shown in Fig. 40.16. The predictive model of the system needs output current information in order to generate

TABLE 40.4 Switching states of 33-level ISMI

	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}	S_{14}	S_{15}	S_{16}	S_{17}	S_{18}	S_{19}	S_{20}	V_o
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	V_{dc}
1																	0	1	0	1	V_{dc}
2																	0	0	1	1	0
3																	1	1	0	0	0
4	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	$15V_{dc}$/16
5																	0	1	0	1	$15V_{dc}$/16
6																	0	0	1	1	0
7																	1	1	0	0	0
.										.											.
.										.											.
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.										.											.
60	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	V_{dc}/16
61																	0	1	0	1	$-V_{dc}$/16
62																	0	0	1	1	0
63																	1	1	0	0	0

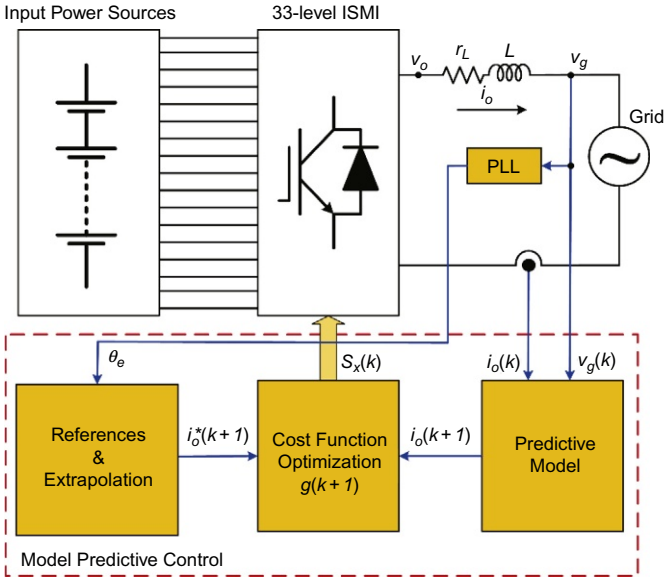


FIG. 40.16 Block diagram of the proposed model predictive control scheme.

reference current. Grid phase angle information is also required to generate reference current in same phase with the grid voltage. In this case, the output current i_o(k) and the grid voltage v_g(k) need to be measured. The phase angle (θ_e) of the reference current is obtained from PLL block. Thus, generated reference current will be in same phase and frequency with the grid voltage.

To control the output current (i_o) of the ISMI, a discrete-time model of the i_o must be defined. To do that, the averaged model of the system, which is defined in (40.30), can be used:

$$\frac{d}{dt}i_o(t) = \frac{-r_L}{L}.i_o(t) + \frac{1}{L}v(t) \tag{40.30}$$

where r_L and L are the resistance and inductance of the filter inductor, respectively, $i_o(t)$ is the average inverter output current, and $v(t)$ is the voltage, averaged in a switching period and applied to the inductor. The voltage on the inductor can be written as $v(t) = v_o(t) - v_g(t)$, where $v_g(t)$ is the grid voltage and $v_o(t)$ is the averaged value of the inverter voltage.

The general solution of the differential equation is

$$i_o(t) = e^{\frac{-r_L}{L}(t-t_0)}i_o(t_0) + \int_{t_0}^{t} e^{\frac{-r_L}{L}(t-\tau)}\frac{1}{L}v(\tau)d\tau \tag{40.31}$$

where lower (t_0) and upper (t) limits of integration can be defined as kT_s and (k+1)T_s, respectively, to obtain discrete-time model with sampling period T_s.

$$i_o(k+1) = e^{\frac{-r_L}{L}T_s}i_o(k) + \frac{1}{L}\int_{kT_s}^{(k+1)T_s} e^{\frac{-r_L}{L}((k+1)T_s-\tau)}v(\tau)d\tau \tag{40.32}$$

where i_o(k) $\equiv i_o$(kT_s). T_s is usually small enough to satisfy ($r_L Ts/L$) <<l; thus, (40.32) can be approximated as

$$i_o(k+1) = e^{\frac{-r_L}{L}T_s}.i_o(k) + \frac{1}{L}\int_{kT_s}^{(k+1)T_s} \left(v_o(\tau) - v_g(\tau)\right)d\tau \tag{40.33}$$

Since $d(t)$ is actualized every sampling period, we can assume that $v_o(t)$ is constant between two sampling instants:

$$v_o(t) = v_o(kT_s) \equiv v_o(k) \tag{40.34}$$

if $t \in$ [kT_s,(k+1)T_s]. On the other hand, as the sampling frequency is much higher than the grid frequency, we can approximate $v_g(t)$ linearly between two sampling instants:

$$v_g(t) \asymp v_g(kT) + \frac{v_g((k+1)T_s) - v_g(kT_s)}{T_s} \tag{40.35}$$

if $t \epsilon$ [kT_s,(k+1)T_s]. Discrete-time model of the output current can be obtained from substituting (40.34) and (40.35) into (40.33):

$$i_o(k+1) = e^{\frac{-r_L}{L}T_s}.i_o(k) + \frac{T_s}{L}\left(v_o(k) - \overline{v}_g(k)\right) \tag{40.36}$$

where $\overline{v}_g(k) = (1/2).\left(v_g(k+1) + v_g(k)\right)$ is the averaged value of the grid voltage between two samples.

The cost function is an important stage of the MPC technique. To minimize the error between the reference and the predicted values in the next sampling time, the cost function must be selected according to specific design criteria. In this study, in order to control the output current, the cost function is defined as

$$g = \left[i_o^*(k+1) - i_o(k+1)\right]^2 \tag{40.37}$$

where i_o*(k+1) is the reference output current and i_o(k+1) is the predicted output current in the next sampling time.

C. Implantation results

To verify the proposed MPC scheme for 33-level ISMI, experimental studies have been carried out for different operating conditions. The parameters of the system are summarized in Table 40.5.

Fig. 40.17A and B shows the experimental results of steady-state performance of the MPC-based current controller under normal and poor grid conditions. The results show that even with poor grid condition, the MPC-based current controller has an excellent steady-state performance.

TABLE 40.5 System parameters

Parameters	Values
Input DC voltage, V_{in}	16*62.5 = 1000 V
dc-link capacitor, C_n	470 μF (each)
Filter inductance, L_f	10 mH
Filter resistance, R_f	0.02 Ω
Nominal output voltage, v_{ln}	800 V max
Sampling time, T_s	50 μs

Fig. 40.18 shows the transient response results of the proposed MPC. The reference current is changed from 30 to 10 A and vice versa in order to observe the response of the proposed control technique. It can be seen that the transient time is very short, controller response is very fast, and the output current tracks its reference with high accuracy.

As the proposed control method is based on the system model, the algorithm is also tested to verify the robustness

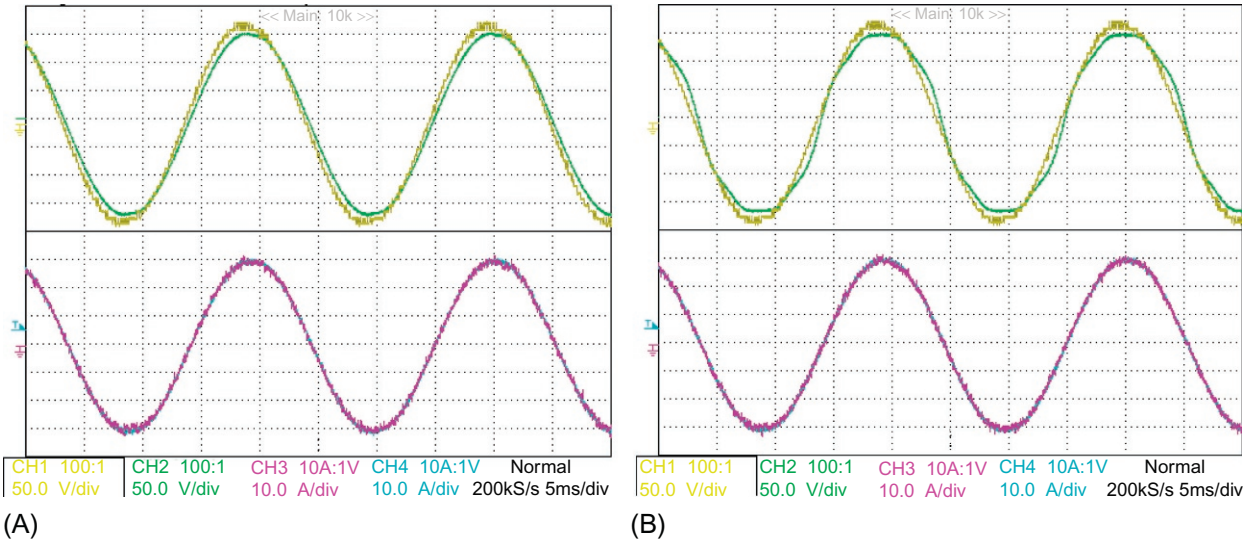


FIG. 40.17 Steady-state results of the proposed algorithm. (A) Normal grid condition. (B) Poor grid condition. CH1, inverter output voltage; CH2, grid voltage; CH3, output current; CH4, reference current.

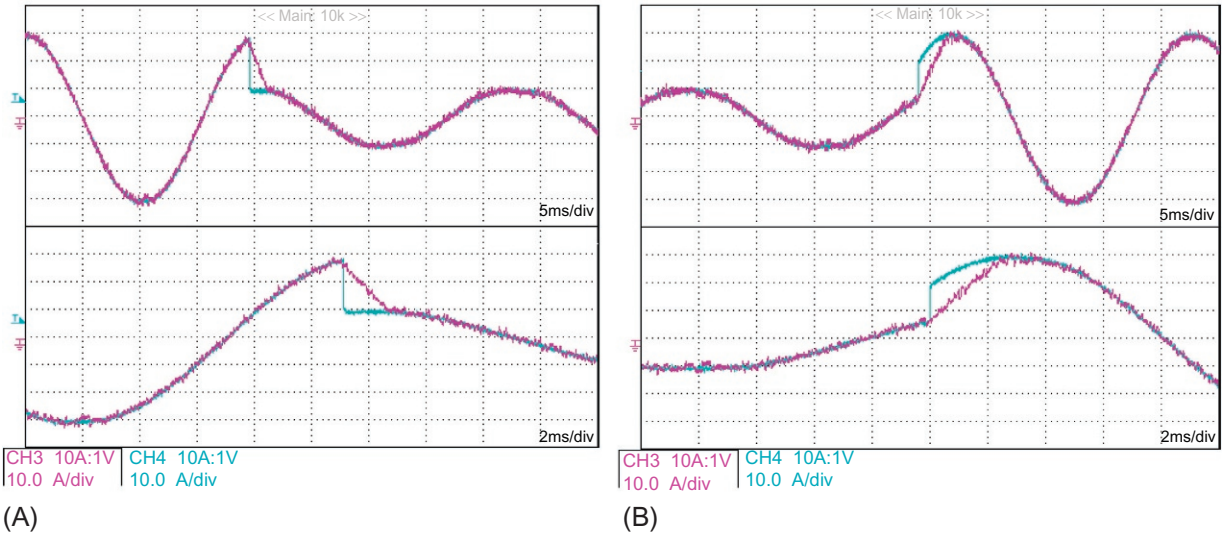


FIG. 40.18 Transient response of the proposed algorithm. (A) Step changes from 30 to 10 A. (B) Step changes from 10 to 30 A. CH3, output current; CH4, reference current.

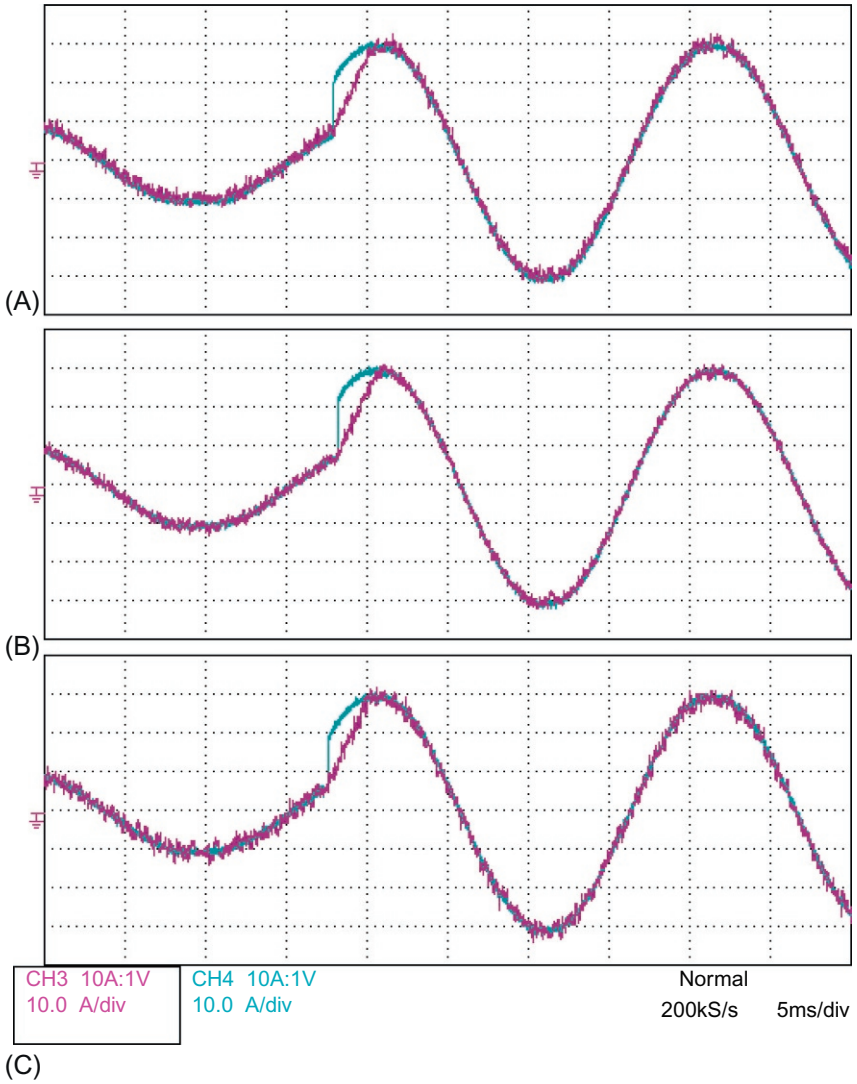


FIG. 40.19 Effect of mismatch filter inductance errors. (A) −50% error $L = 0.5^*L$, (B) no error $L = L$, (C) +50% error $L = 1.5^*L$. CH3, output current; CH4, reference current.

against the mismatch with filter parameter. To do that, the filter inductance (L_f) is consecutively set at 0.5^*L, L, and 1.5^*L, which is the typical case in distributed generation systems where the power system impedance changes randomly. It is remarkable that the new filter inductance value is not entered to the controller. The control algorithm uses a rated filter inductance value ($L = 10$ mH). Results are shown in Fig. 40.19A–C. It is clear that, when the modeled inductance value is smaller than selected value (0.5^*L), the mismatch causes steady-state errors, and when the modeled inductance value is bigger than selected value (1.5^*L), the mismatch causes current oscillation. However, it can be observed from results that the mismatch of the filter model slightly affects the system performance.

Acknowledgment

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References

[1] W. Liuping, C. Shan, Y. Dae, G. Lu, N. Ki, PID and Predictive Control of Electrical Drives and Power Converters Using Matlab/Simulink, Wiley & IEEE Press, 2015. ISBN 97811118339442.

[2] M. Trabelsi, S. Bayhan, S.S. Refaat, H. Abu-Rub, L. Ben-Brahim, Multi-objective model predictive control for grid-tied 15-level packed U cells inverter, in: 18th European Conference on Power

Electronics and Applications (EPE'16 ECCE Europe), Karlsruhe, Germany, 2016, pp. 1–7.
[3] S. Bayhan, H. Abu-Rub, Model predictive sensorless control of standalone doubly fed induction generator, in: 40th Annual Conference of the IEEE Industrial Electronics Society, IECON 2014, 2014, pp. 2166–2172.
[4] J. Holtz, S. Stadtfeld, A predictive controller for the stator current vector of ac machines fed from a switched voltage source, in: IEEE International Power Electronics Conference, Tokyo, 1983, pp. 1665–1675.
[5] M. Trabelsi, S. Bayhan, H. Abu-Rub, L. Ben-Brahim, P. Zanchetta, Finite control set model predictive control for Grid-Tie Quasi-Z-source based multilevel inverter, in: IEEE International Conference on Industrial Technology, ICIT 2016, Taipei, Taiwan, 14–17 March, 2016.
[6] J. Rodriguez, M. Kazmierkowski, J.R. Espinoza, P. Zanchetta, H. Abu-Rub, H.A. Young, C.A. Rojas, State of the art of finite control set model predictive control in power electronics, IEEE Trans. Ind. Inform. 9 (2) (2013) 1003–1016.
[7] P. Cortes, M.P. Kazmierkowski, R.M. Kennel, D.E. Quevedo, J. Rodriguez, Predictive control in power electronics and drives, IEEE Trans. Ind. Electron. 55 (12) (2008) 4312–4324.
[8] B. Kim, N. Washington, H. Yoon, Hysteresis-reduced dynamic displacement control of piezoceramic stack actuators using model predictive sliding mode control, Smart Mater. Struct. 21 (5) (2012) 55–68.
[9] S. Bayhan, M. Mosa, H. Abu-Rub, Model Predictive Control of Impedance Source Inverter, John Wiley & Sons Ltd, 2016. pp. 329–361.
[10] J. Rodriguez, P. Cortes, Predictive Control of Power Converters and Electrical Drives, Wiley & IEEE Press, 2012.
[11] H. Abu-Rub, J. Guzinski, Z. Krzeminski, H.A. Toliyat, Predictive current control of voltage-source inverters, IEEE Trans. Ind. Electron. 51 (3) (2004) 585–593.
[12] J. Rodriguez, J. Pontt, C.A. Silva, P. Correa, P. Lezana, P. Cortes, U. Ammann, Predictive current control of a voltage source inverter, IEEE Trans. Ind. Electron. 54 (1) (2007) 495–503.
[13] S. Bayhan, H. Abu-Rub, O. Ellabban, Sensorless model predictive control of wind-driven DFIG in DC microgrid system, IET Renaw. Power Gen. 10 (4) (2016) 514–521.
[14] V. Yaramasu, M. Rivera, M. Narimani, B. Wu, J. Rodriguez, Model predictive approach for a simple and effective load voltage control of four-leg inverter with an output RL filter, IEEE Trans. Ind. Electron. 61 (10) (2014) 5259–5270.
[15] S. Bayhan, H. Abu-Rub, Model predictive control of Quasi-Z source three-phase four-leg inverter, in: 41st Annual Conference of the IEEE Industrial Electronics Society, Yokohama, Japan, 2015.
[16] S. Bayhan, M. Trabelsi, H. Abu-Rub, Model predictive control of three-phase three-level neutral-point-clamped qZS inverter, in: 6th International Conference on Power Engineering, Energy and Electrical Drives, Bydgoszcz, Poland, 29 June-01 July, 2016.
[17] S. Bayhan, M. Trabelsi, H. Abu-Rub, M. Malinowski, Finite control set model predictive control for a quasi-Z-source four-leg inverter under unbalanced load condition. IEEE Trans. Ind. Electron. 64 (4) (2017) 2560–2569.
[18] S. Bayhan, H. Abu-Rub, M. Rivera, S. Demirbas, Model predictive control of 33-level input switched multilevel inverter for grid-connected PV systems, in: IV. European Conference on Renewable Energy Systems, 28-31 August, Istanbul, Turkey, 2016.

Further Reading

[19] S. Bayhan, M. Trabelsi, H. Abu-Rub, Model Predictive Control of Z-Source Four-Leg Inverter for Standalone Photovoltaic System with Unbalanced Load, in: The Applied Power Electronics Conference & Exposition, Long Beach, US, 2016.
[20] S. Bayhan, H. Abu-Rub, B. Robert, Model predictive control of quasi-Z source four-leg inverter for distributed power generation, IEEE Trans. Ind. Electron. 63 (7) (2016) 4506–4516.
[21] M. Rivera, V. Yaramasu, A. Llor,J. Rodriguez, B. Wu,M. Fadel, Digital predictive current control of a three-phase four-leg inverter, IEEE Trans. Ind. Electron. 60 (11) (2013) 4903–4912.
[22] S. Bayhan, P. Kakosimos, H. Abu-Rub, J. Rodriguez, Model Predictive Control of Five-Level Neutral-Point-Clamped/H-Bridge Quasi-Impedance Source Inverter, in: 41st Annual Conference of the IEEE Industrial Electronics Society, October 23–27, Florence, Italy, 2016.
[23] M. Trabelsi, S. Bayhan, H. Abu-Rub, L. Ben-Brahim, M. Marcos, B. Robert, An effective model predictive control for grid connected packed U cells multilevel inverter, in: Annual IEEE Power and Energy Conference at Illinois, US, PECI 2016, 19–20 February, 2016.
[24] M. Trabelsi, S. Bayhan, K.A. Ghazi, H. Abu-Rub, L. Ben-Brahim, Finite-control-set model predictive control for grid-connected packed-U-cells multilevel inverter, IEEE Trans. Ind. Electron. 63 (11) (2016) 7286–7295.
[25] M. Metry, S. Bayhan, R. Balog, H. Abu-Rub, Model predictive control for maximum power point tracking of single-phase submultilevel inverter for photovoltaic systems, in: Annual IEEE Power and Energy Conference at Illinois, US, PECI 2016, 19–20 February, 2016.

Section VII

Power Quality and EMI Issues

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41

Active Power Filters

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41.1 Introduction

The growing number of power-electronics-based equipment has produced an important impact on the quality of electric power supply. Both high-power industrial loads and domestic loads cause harmonics in the network voltages. At the same time, much of the equipment causing the disturbances is quite sensitive to deviations from the ideal sinusoidal line voltage. Therefore, power quality problems may originate in the system or may be caused by the consumer itself. Moreover, in the last years, the growing concern related to power quality comes from the following:

- Consumers that are becoming increasingly aware of the power quality issues and being more informed about the consequences of harmonics, interruptions, sags, switching transients, etc. Motivated by deregulation, they are challenging the energy suppliers to improve the quality of the power delivered.
- The proliferation of load equipment with microprocessor-based controllers and power electronic devices that are sensitive to many types of power quality disturbances.
- Emphasis on increasing overall process productivity that has led to the installation of high-efficiency equipment, such as adjustable speed drives and power factor correction equipment. This in turn has resulted in an increase in harmonics injected into the power system, causing concern about their impact on the system behavior.

For an increasing number of applications, conventional equipment is proving insufficient for the mitigation of power quality problems. Harmonic distortion has traditionally been dealt with the use of passive LC filters. However, the application of passive filters for harmonic reduction may result in parallel resonances with the network impedance, over compensation of reactive power at fundamental frequency, and poor flexibility for dynamic compensation of different frequency harmonic components.

The increased severity of power quality in power networks has attracted the attention of power engineers to develop dynamic and adjustable solutions to the power quality problems. Such equipment, generally known as active filters, are also called active power line conditioners and are able to compensate current and voltage harmonics and reactive power, regulate terminal voltage, suppress flicker, and improve voltage balance in three-phase systems. The advantage of active filtering is that it automatically adapts to changes in the network and load fluctuations. They can compensate for several harmonic

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orders, and are not affected by major changes in network characteristics, eliminating the risk of resonance between the filter and network impedance. Another plus is that they take up very little space compared with traditional passive compensators.

41.2 Types of Active Power Filters

The technology of active power filter has been developed during the past two decades reaching maturity for harmonic compensation, reactive power, and voltage balance in ac power networks. All active power filters are developed with pulse-width-modulated (PWM) converters (current-source or voltage-source inverters). The current-fed PWM inverter bridge structure behaves as a nonsinusoidal current source to meet the harmonic current requirement of the nonlinear load. It has a self-supported dc reactor that ensures the continuous circulation of the dc current. They present good reliability but have important losses and require higher values of parallel capacitor filters at the ac terminals to remove unwanted current harmonics. Moreover, they cannot be used in multilevel or multistep mode configurations to allow compensation in higher power ratings.

The other converter used in active power filter topologies is the PWM voltage-source inverter (PWM-VSI). This converter is more convenient for active power filtering applications since it is lighter, cheaper, and expandable to multilevel and multistep versions, to improve its performance for high power rating compensation with lower switching frequencies. The PWM-VSI has to be connected to the ac mains through coupling reactors. An electrolytic capacitor keeps a dc voltage constant and ripple-free.

Active power filters can be classified based on the type of converter, topology, control scheme, and compensation characteristics. The most popular classification is based on the topology such as shunt, series, or hybrid. The hybrid configuration is a combination of passive and active compensation. The different active power filter topologies are shown in Fig. 41.1.

Shunt active power filters (Fig. 41.1A) are widely used to compensate current harmonics, reactive power, and load current unbalanced. It can also be used as a static var generator in power system networks for stabilizing and improving voltage profile. Series active power filters (Fig. 41.1B) is connected before the load in series with the ac mains, through a coupling transformer to eliminate voltage harmonics and to balance and regulate the terminal voltage of the load or line. The hybrid

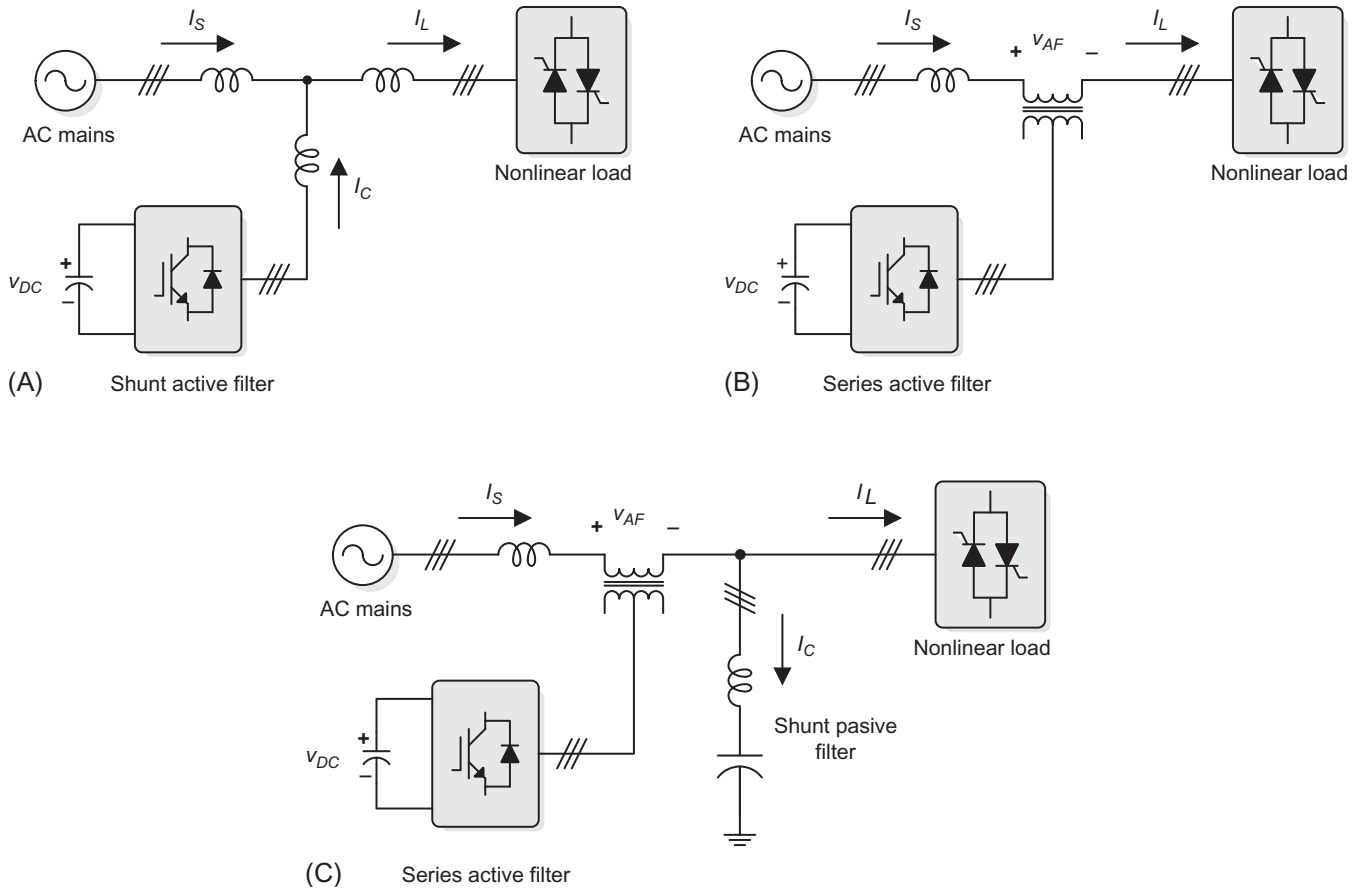


FIG. 41.1 Active power filter topologies implemented with PWM-VSI: (A) shunt active power filter, (B) series active power filter, and (C) hybrid active power filter.

TABLE 41.1 Active filter solutions to power quality problems

Active filter connection	Load on ac supply	AC supply on load
Shunt	Current harmonic filtering Reactive current compensation Current unbalance Voltage flicker	
Series	Current harmonic filtering Reactive current compensation Current unbalance Voltage flicker Voltage unbalance	Voltage sag/swell Voltage unbalance Voltage distortion Voltage interruption Voltage flicker Voltage notching

configuration is a combination of series active filter and passive shunt filter (Fig. 41.1C). This topology is very convenient for the compensation of high-power systems, because the rated power of the active filter is significantly reduced (about 10% of the load size), since the major part of the hybrid filter consists of the passive shunt LC filter used to compensate lower-order current harmonics and reactive power at fundamental frequency.

Due to the operation constraint, shunt or series active power filters can compensate only specific power quality problems. Therefore, the selection of the type of active power filter to improve power quality depends on the source of the problem as can be seen in Table 41.1.

The principles of operation of shunt, series, and hybrid active power filters are described in the following sections.

41.2.1 Shunt Active Power Filters

Shunt active power filters compensate current harmonics by injecting equal but opposite harmonic compensating current. In this case, the shunt active power filter operates as a current source injecting the harmonic components generated by the load but phase shifted by 180 degrees. As a result, components of harmonic currents contained in the load current are canceled by the effect of the active filter, and the source current remains sinusoidal and in phase with the respective phase-to-neutral voltage. This principle is applicable to any type of load considered as a harmonic source. Moreover, with an appropriate control scheme, the active power filter can also compensate the load power factor. In this way, the power distribution system sees the nonlinear load and the active power filter as an ideal resistor. The compensation characteristics of the shunt active power filter are shown in Fig. 41.2.

41.2.2 Power Circuit Topologies

Shunt active power filters are normally implemented with PWM-VSIs. In this type of application, the PWM-VSI operates as a current-controlled voltage source. Traditionally, two-level PWM-VSIs have been used to implement such system connected

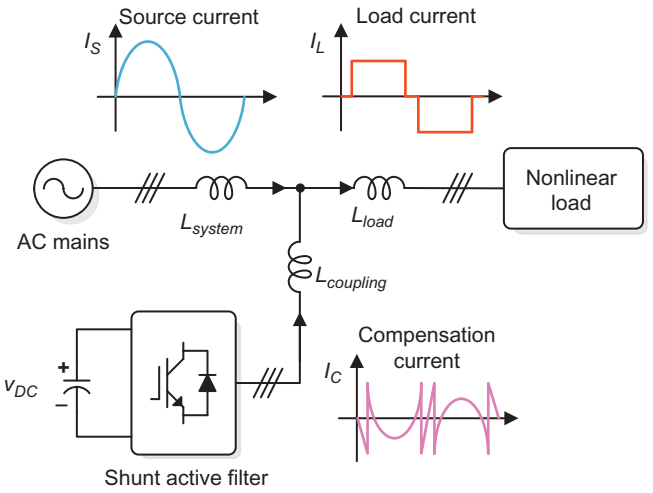


FIG. 41.2 Compensation characteristics of a shunt active power filter.

to the ac bus through a transformer. This type of configuration is aimed to compensate nonlinear load rated in the medium power range (hundreds of kilovolt-amperes) due to semiconductor rated value limitations. However, in the last years, multilevel PWM-VSIs have been proposed to develop active power filters for medium-voltage and higher rated power applications. Also, active power filters implemented with multiple VSIs connected in parallel to a dc bus but in series through a transformer or in cascade have been proposed in the technical literature. The different power circuit topologies are shown in Fig. 41.3.

The use of VSI connected in cascade is an interesting alternative to compensate high-power nonlinear loads. The use of two PWM-VSI with different rated power allows the use of different switching frequencies, reducing switching stresses and commutation losses in the overall compensation system. The power circuit configuration of such a system is shown in Fig. 41.4.

The VSI connected closer to the load compensates for the displacement power factor and lower-frequency current harmonic components (Fig. 41.5B), while the second compensates only high-frequency current harmonic components. The first converter requires higher rated power than the second and can operate at lower switching frequency. The compensation characteristics of the cascade shunt active power filter are shown in Fig. 41.5.

In recent years, there has been an increasing interest in using multilevel inverters for high-power energy conversion, especially for drives and reactive power compensation. The use of neutral-point-clamped (NPC) inverters (Fig. 41.6) allows equal voltage shearing of the series-connected semiconductors in each phase. Basically, multilevel inverters have been developed for applications in medium-voltage ac motor drives and static var compensation. For these types of applications, the output voltage of the multilevel inverter must be able to generate an almost sinusoidal output current. In order to generate a near sinusoidal output current, the output voltage should not contain low-frequency harmonic components.

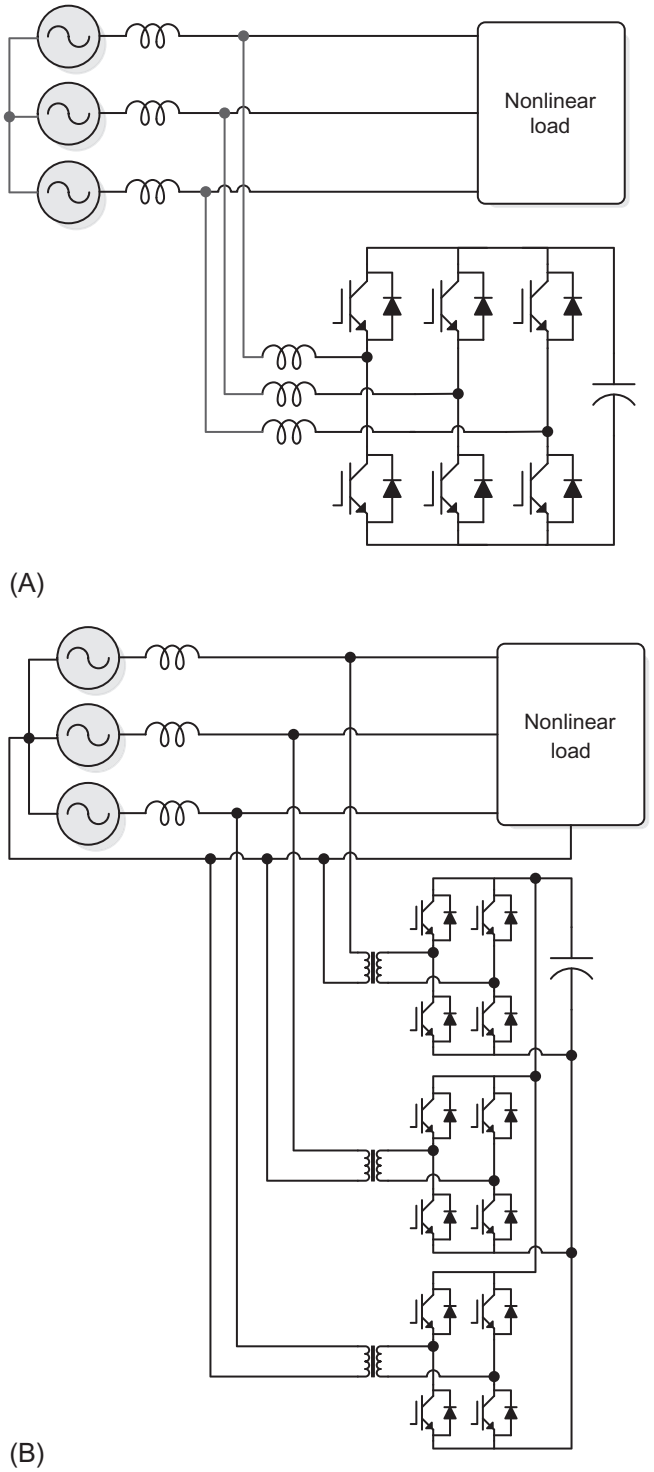


FIG. 41.3 Shunt active power filter topologies implemented with PWM-VSIs: (A) a three-phase PWM unit and (B) three single-phase units in parallel to a common dc bus.

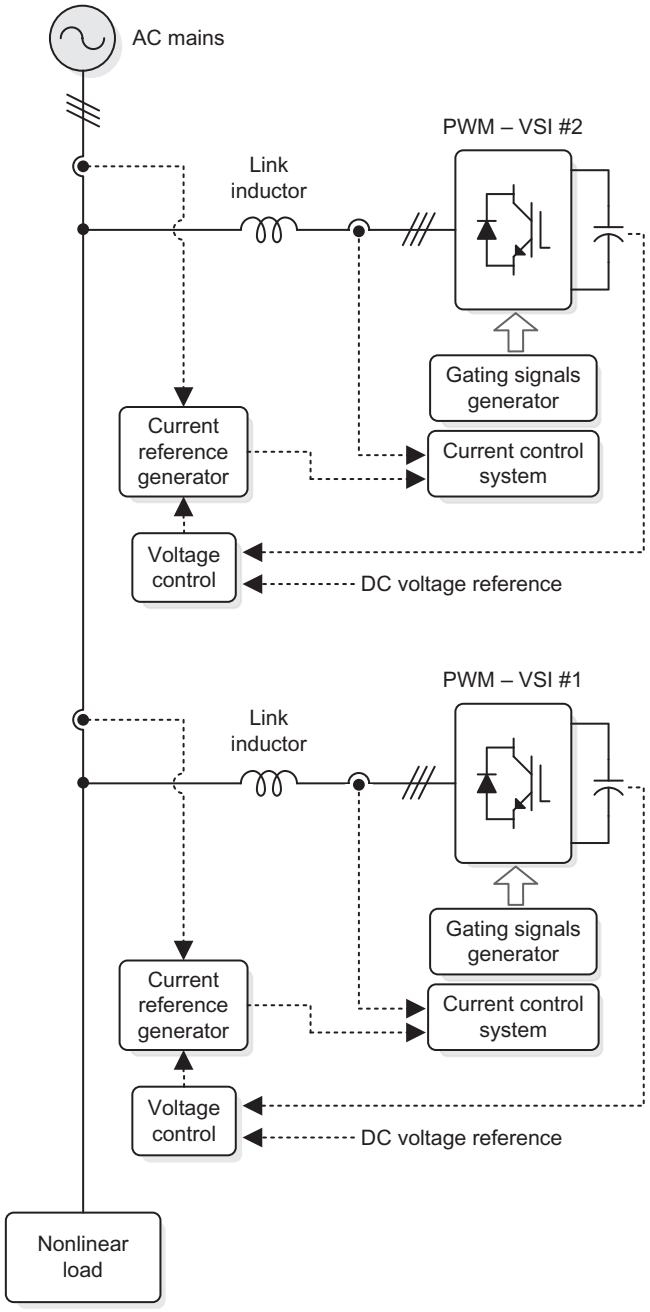


FIG. 41.4 A shunt active power filter implemented with two PWM-VSI connected in cascade.

However, for active power filter applications, the three-level NPC inverter output voltage must be able to generate an output current that follows the respective reference current containing the harmonic and reactive component required by the load. Current and voltage waveforms obtained for a shunt active power filter implemented with a three-level NPC-VSI are shown in Fig. 41.7.

41.2.3 Control Scheme

The control scheme of a shunt active power filter must calculate the current reference waveform for each phase of the inverter, maintain the dc voltage constant, and generate the inverter gating signals. The block diagram of the control scheme of a shunt active power filter is shown in Fig. 41.8.

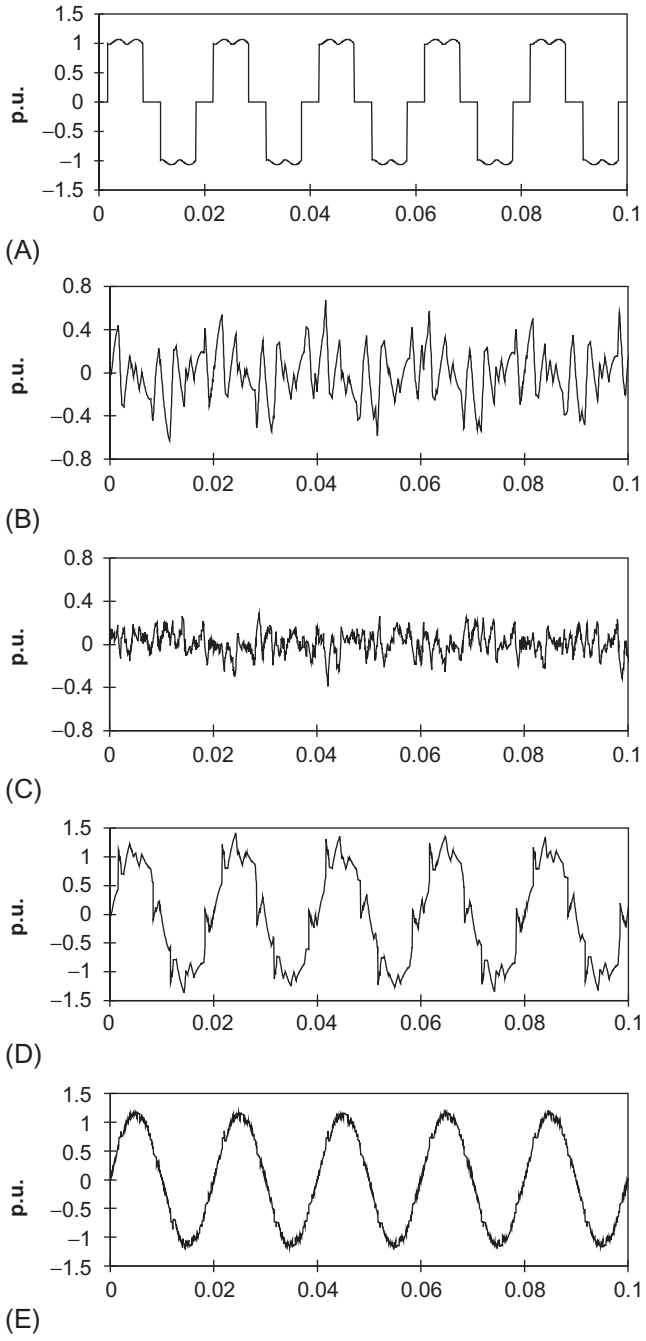


FIG. 41.5 Current waveforms of active power filter implemented with two PWM-VSI in cascade: (A) load current waveform, (B) current waveform generated by PWM-VSI no. 1, (C) current waveform generated by PWM-VSI no. 2, (D) power system current waveform between the two inverters ($THD_i = 13.7\%$), and (E) power system current waveform ($THD_i = 4.5\%$).

The current reference circuit generates the reference currents required to compensate the load current harmonics and reactive power and also try to maintain constant the dc voltage across the electrolytic capacitors. There are many possibilities to implement this type of control, and the most popular of them will be explained in this chapter. Also, the compensation effectiveness of an active power filter depends on its ability to follow with a minimum error and time delay the reference signal calculated to compensate the distorted load current. Finally, the dc voltage control unit must keep the total dc bus voltage constant and equal to a given reference value. The dc voltage control is achieved by adjusting the small amount of real power absorbed by the inverter. This small amount of real power is adjusted by changing the amplitude of the fundamental component of the reference current.

41.2.3.1 Current Reference Generation

There are many possibilities to determine the reference current required to compensate the nonlinear load. Normally, shunt active power filters are used to compensate the displacement power factor and low-frequency current harmonics generated by nonlinear loads. One alternative to determine the current reference required by the VSI is the use of the instantaneous reactive power theory, proposed by Akagi [1], the other one is to obtain current components in *d-q* or synchronous reference frame [2], and the third one is to force the system line current to follow a perfectly sinusoidal template in phase with the respective phase-to-neutral voltage.

Instantaneous reactive power theory

This concept is very popular and useful for this type of application and basically consists of a variable transformation from the *a*, *b*, *c* reference frame of the instantaneous power, voltage, and current signals to the α, β reference frame. The transformation equations from the *a*, *b*, *c* reference frame to the α, β coordinates can be derived from the phasor diagram shown in Fig. 41.9.

The instantaneous values of voltages and currents in the α, β coordinates can be obtained from the following equations:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = [A] \cdot \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = [A] \cdot \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{41.1}$$

where *A* is the transformation matrix, derived from Fig. 41.9 and is equal to

$$[A] = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \tag{41.2}$$

This transformation is valid if and only if $v_a(t) + v_b(t) + v_c(t)$ is equal to zero and also if the voltages are balanced and sinusoidal. The instantaneous active and reactive power in the α, β coordinates are calculated with the following expressions:

$$p(t) = v_\alpha(t) \cdot i_\alpha(t) + v_\beta(t) \cdot i_\beta(t) \tag{41.3}$$

$$q(t) = -v_\alpha(t) \cdot i_\beta(t) + v_\beta(t) \cdot i_\alpha(t) \tag{41.4}$$

It is evident that *p(t)* becomes equal to the conventional instantaneous real power defined in the *a*, *b*, *c* reference frame. However, in order to define the instantaneous reactive power, Akagi

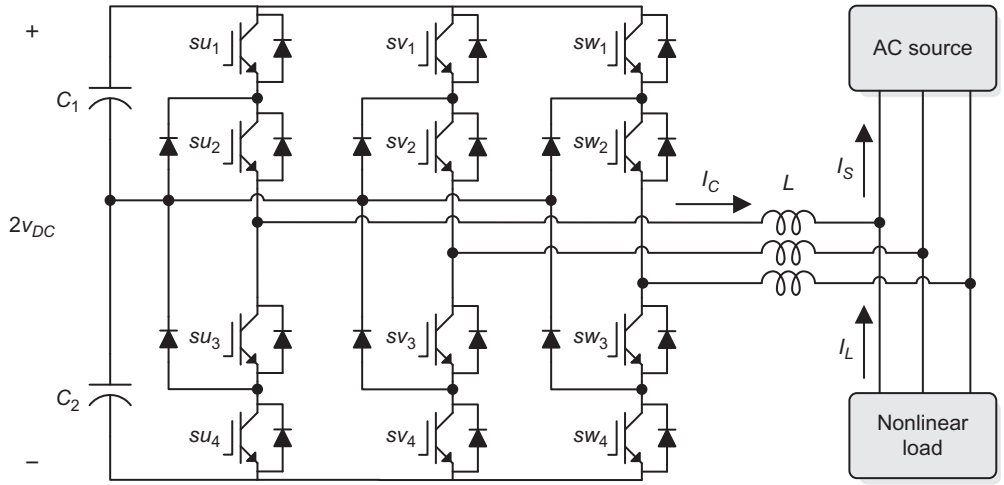


FIG. 41.6 A shunt active power filter implemented with a three-level neutral-point-clamped VSI.

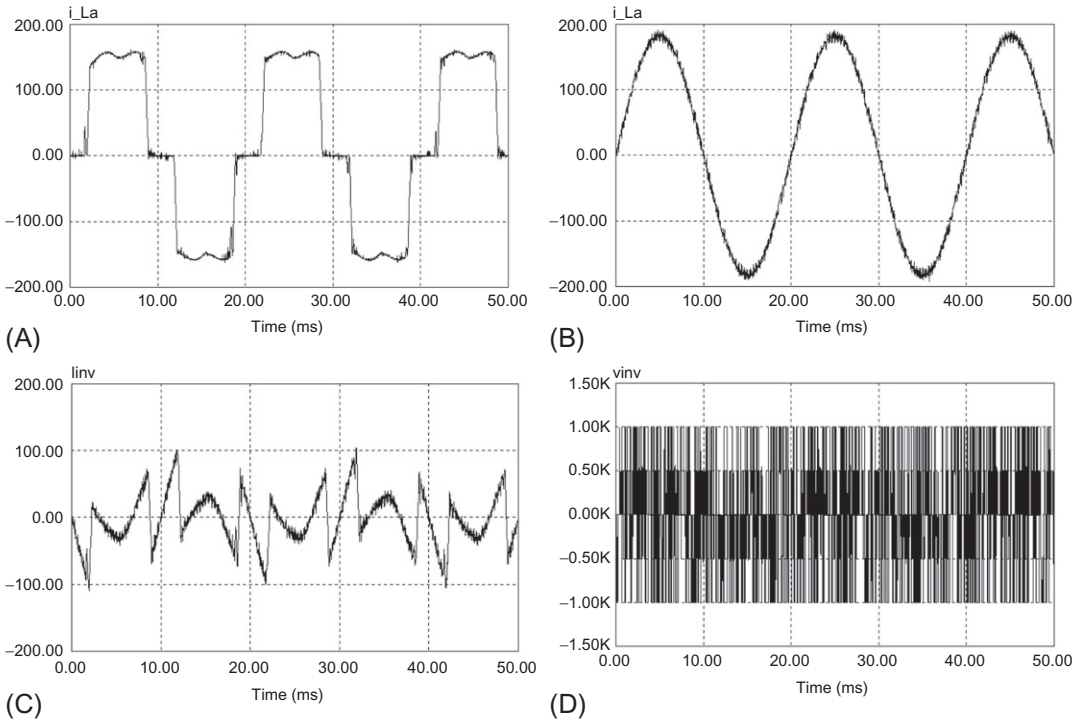


FIG. 41.7 Current and voltage waveforms for a shunt active power filter implemented with a three-level NPC-VSI: (A) load current, (B) compensated system current ($THD_i = 3.5\%$), (C) current generated by the shunt active power filter, and (D) inverter output voltage.

introduces a new instantaneous space vector defined by expression (41.4) or by the vector equation:

$$q = v_\alpha x i_\beta + v_\beta x i_\alpha \tag{41.5}$$

where the vector q is perpendicular to the plane of α, β coordinates, to be faced in compliance with a right-hand rule; v_α is perpendicular to i_β; and v_β is perpendicular to i_α. The physical meaning of the vector q is not "instantaneous power" because of the product of the voltage in one phase and the current in the other phase. On the contrary, $v_\alpha i_\alpha$ and $v_\beta i_\beta$ in Eq. (41.3) obviously mean "instantaneous power" because of the product of the voltage in one phase and the current in the same phase. Akagi named the new electric quantity defined in Eq. (41.5)

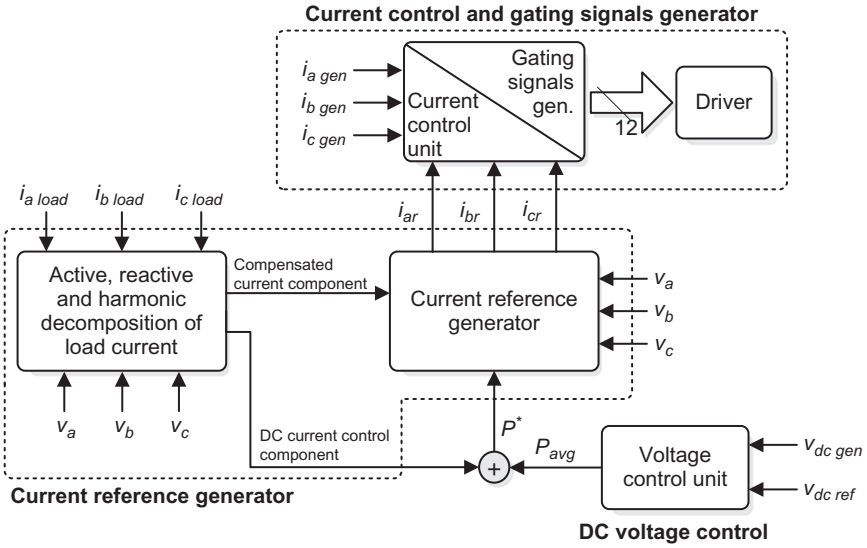


FIG. 41.8 The block diagram of a shunt active power filter control scheme.

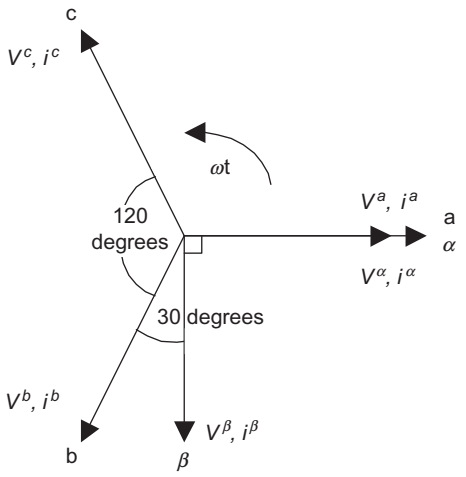


FIG. 41.9 Transformation diagram from the a, b, c reference frame to the α, β coordinates.

"instantaneous imaginary power," which is represented by the product of the instantaneous voltage and current in different axes, but cannot be treated as a conventional quantity.

The expression of the currents in the $\alpha-\beta$ plane, as a function of the instantaneous power, is given by the following equation:

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \cdot \left\{ \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \cdot \begin{bmatrix} p \\ 0 \end{bmatrix} + \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \cdot \begin{bmatrix} 0 \\ q \end{bmatrix} \right\} \equiv \begin{bmatrix} i_{\alpha p} \\ i_{\beta p} \end{bmatrix} + \begin{bmatrix} i_{\alpha q} \\ i_{\beta q} \end{bmatrix} \tag{41.6}$$

and the different components of the currents in the $\alpha-\beta$ plane are shown in the following expressions:

$$i_{\alpha p} = \frac{v_\alpha p}{v_\alpha^2 + v_\beta^2} \tag{41.7}$$

$$i_{\alpha q} = \frac{v_\beta q}{v_\alpha^2 + v_\beta^2} \tag{41.8}$$

$$i_{\beta p} = \frac{v_\beta p}{v_\alpha^2 + v_\beta^2} \tag{41.9}$$

$$i_{\beta q} = \frac{-v_\alpha q}{v_\alpha^2 + v_\beta^2} \tag{41.10}$$

From Eqs. (41.3) and (41.4), the values of p and q can be expressed in terms of the dc components and the ac components, that is,

$$p = \overline{p} + \widetilde{p} \tag{41.11}$$

$$q = \overline{q} + \widetilde{q} \tag{41.12}$$

where

$\overline{p}$ is the dc component of the instantaneous power p and is related to the conventional fundamental active current,

$\widetilde{p}$ is the ac component of the instantaneous power p; it does not have average value and is related to the harmonic currents caused by the ac component of the instantaneous real power.

$\overline{q}$ is the dc component of the imaginary instantaneous power q and is related to the reactive power generated by the fundamental components of voltages and currents.

$\widetilde{q}$ is the ac component of the instantaneous imaginary power q and it is related to the harmonic currents caused by the ac component of instantaneous reactive power.

In order to compensate reactive power (displacement power factor) and current harmonics generated by nonlinear loads, the reference signal of the shunt active power filter must include the values of $\widetilde{p}$, $\overline{q}$, and $\widetilde{q}$. In this case, the reference currents required by the shunt active power filters are calculated with the following expression:

$$\begin{bmatrix} i^*_{c,\alpha} \\ i^*_{c,\beta} \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \cdot \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \cdot \begin{bmatrix} \widetilde{p}_L \\ \overline{q}_L + \widetilde{q}_L \end{bmatrix} \tag{41.13}$$

The final compensating currents including the zero-sequence components in a, b, c reference frame are the following:

$$\begin{bmatrix} i^*_{c,a} \\ i^*_{c,b} \\ i^*_{c,c} \end{bmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} \frac{1}{\sqrt{2}} & 1 & 0 \\ \frac{1}{\sqrt{2}} & \frac{-1}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{-1}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} -i_0 \\ i^*_{c,\alpha} \\ i^*_{c,\beta} \end{bmatrix} \tag{41.14}$$

where the zero-sequence current component i_0 is equal to $\frac{1}{\sqrt{3}}(i_a + i_b + i_c)$. The block diagram of the circuit required to generate the reference currents defined in Eq. (41.14) is shown in Fig. 41.10.

The advantage of instantaneous reactive power theory is that real and reactive power associated with fundamental components are dc quantities. These quantities can be extracted with a low-pass filter. Since the signal to be extracted is dc, filtering of the signal in the $\alpha - \beta$ reference frame is insensitive to any phase-shift errors introduced by the low-pass filter, improving compensation characteristics of the active power filter. The same advantage can be obtained by using the *synchronous reference frame method*, proposed in [2]. In this case, transformation from a, b, c axes to d-q synchronous reference frame is done.

Effects of the low-pass filter design characteristics in compensation performance: A Butterworth filter is normally used due to the adequate frequency response. A second-order filter offers an appropriate relation between the transient response and the required attenuation characteristic. Higher-order filters achieve better filtering characteristic, but the settling time is increased. Since the low-pass filter cannot eliminate completely the low-frequency harmonic contained in the p and q signals, the shunt active power filter cannot compensate the entire low-frequency harmonic contained in the load current. Normally, the cutoff frequency is equal to 127 Hz with an attenuation factor of 15 dB for the first ac component to be eliminated, which means an 82.2% attenuation of the fifth and seventh harmonic components (Fig. 41.11). The expression that relates the system line current harmonic distortion with the LPF cutoff frequency and load power factor is shown in Eq. (41.15):

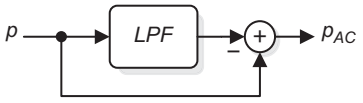


FIG. 41.11 The low-pass filter block diagram used to extract the ac component of p.

$$THD_{isys} = \frac{\sqrt{\sum_{h=6k}^{\infty} \frac{1}{(f_n/f_c)^4 + 1} \left[\left(\left(h^2+1\right)/\left(h^2-1\right) \right) - \left(1/\left(h^2-1\right)\right) \cos(2\varphi) \right]}}{\cos(\varphi)} \tag{41.15}$$

with $k = 1, 2, 3, \ldots$ and f_h is the frequency of the harmonic component of order h and f_c is the LPF cutoff frequency.

Fig. 41.12 shows the total harmonic distortion (THD) in the line currents introduced by the second-order Butterworth filtering characteristics, as a function of the cutoff frequency and considering a 50 Hz ac mains frequency. The harmonic distortion of the compensated line current depends on the load displacement power factor, as shown in Eq. (41.15). If the cutoff frequency of the low-pass filter is changed, the active power filter compensation performance is affected and the transient response of the control scheme.

Effects of the supply voltage distortion in compensation performance: One of the most important characteristics of the instantaneous imaginary power concept is that in order to obtain the current reference signal required to compensate reactive and harmonic current components, the system phase-to-neutral voltages are used. In general, purely sinusoidal voltages

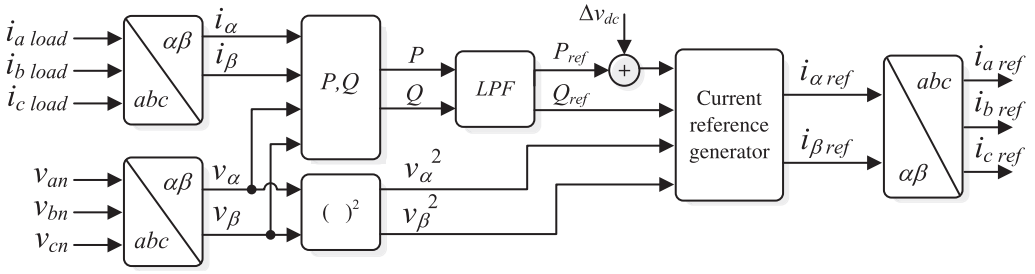


FIG. 41.10 The block diagram of the current reference generator using p-q theory.

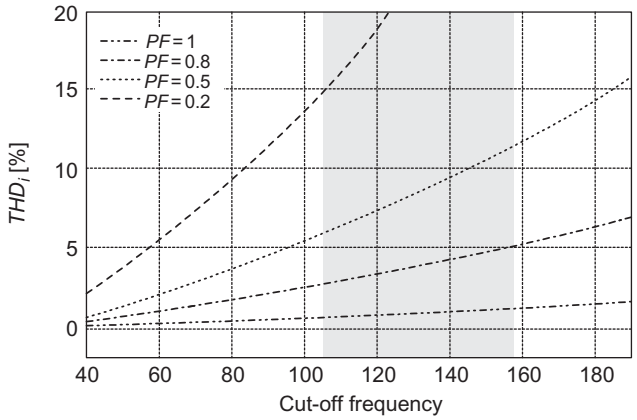


FIG. 41.12 Harmonic distortion of the compensated line current as a function of the low-pass filter cutoff frequency, $PF = \cos(\varphi)$.

are considered in previously reported analysis. In case voltage is purely sinusoidal, the dc components of p and q in the α–β plane are related with the fundamental components in the real a, b, c reference system. This is not the case if the system voltages are distorted or unbalanced, as it is demonstrated below.

It is assumed that the supply voltages have harmonic distortion, and these are represented by

$$\begin{aligned} v_a(t) &= V_1 \cos(\omega t) + V_h \cos[h(\omega t - \delta_h)] \\ v_b(t) &= V_1 \cos\left(\omega t - \frac{2\pi}{3}\right) + V_h \cos\left[h\left(\omega t - \delta_h - \frac{2\pi}{3}\right)\right] \\ v_c(t) &= V_1 \cos\left(\omega t + \frac{2\pi}{3}\right) + V_h \cos\left[h\left(\omega t - \delta_h + \frac{2\pi}{3}\right)\right] \end{aligned} \tag{41.16}$$

Since the harmonic voltage component introduces a dc component in p and q, compensation performance of the shunt active power filter is reduced, as shown in Fig. 41.13. The larger the harmonic distortion in the system voltage is, the active power filter performance is more affected.

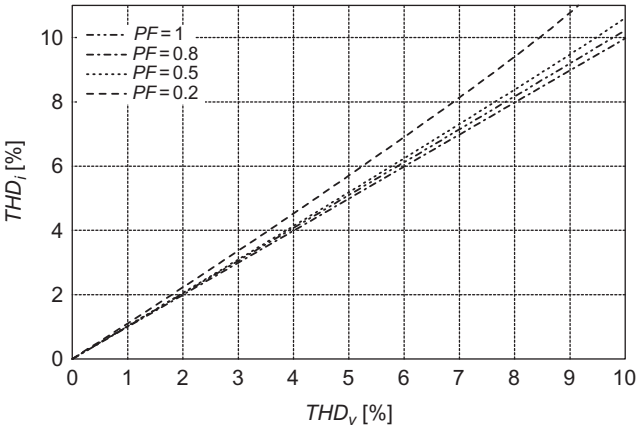


FIG. 41.13 Harmonic distortion in the compensated line current as a function of the harmonic distortion in the system voltages, $PF = \cos(\varphi)$.

Effects of the supply voltage unbalance in compensation performance: Voltage unbalance also affects the active power filter compensation performance. In this analysis, the phase-to-neutral voltages of the ac supply are equal to

$$\begin{aligned} v_a(t) &= V_1 \cos(\omega t) \\ v_b(t) &= V_1(1+m) \cos\left(\omega t - \frac{2\pi}{3}\right) \\ v_c(t) &= V_1(1-m) \cos\left(\omega t + \frac{2\pi}{3}\right) \end{aligned} \tag{41.17}$$

with $0 < m < 1$.

If the low-pass filter is considered as ideal and the active filter follows exactly the current references, the compensated supply current (phase a) is

$$\begin{aligned} i_{Sa} = & I_1 \cos(\varphi) \cos(\omega t) + \frac{\sqrt{3}}{3} m [I_1 \sin(\varphi) \cos(3\omega t) \\ & + I_1 \cos(3\omega t - \varphi)] \end{aligned} \tag{41.18}$$

In this case, the active power filter is not able to fully compensate the system line current, since compensation performance depends on the voltage unbalance magnitude.

The unbalance is defined as a function of the positive and negative-sequence component as

$$\begin{aligned} V_{a1} &= \frac{1}{3}\left[V_a + a^2 V_b + a V_c\right] \\ V_{a2} &= \frac{1}{3}\left[V_a + a V_b + a^2 V_c\right], \quad a = 1\angle 120 \text{ degrees} \\ \text{Unbalance} &= \frac{|V_{a2}|}{|V_{a1}|} = \frac{\sqrt{3}}{3} m \end{aligned} \tag{41.19}$$

The harmonic distortion is equal to

$$THD_i = \frac{\sqrt{3}}{3} m \tag{41.20}$$

The relation between line current harmonic distortion and voltage unbalance is shown in Fig. 41.14.

Effects of the time delay introduced by the dsp in compensation performance: If a DSP is used to derive the reference generation signals, a time delay, T, associated with the processing time is introduced in the calculation of the reference signals. Considering a simultaneous sampling, the ac mains compensated line current with an ideal low-pass filter in the control scheme (phase a) is

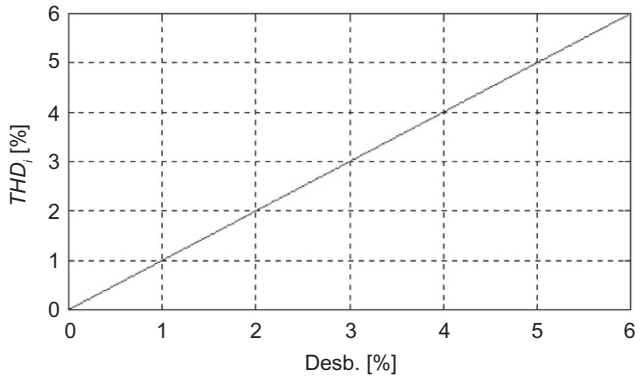


FIG. 41.14 Harmonic distortion in the compensated line current as a function of the system voltages unbalance.

$$\begin{aligned} i_{Sa} =& I_1 \cos(\omega t)[\cos(\varphi) + \sin(\omega T)] + \Delta V_{DC} \cos(\omega t) \\ &+ \sum_{n=2k-1}^{\infty} I_n[1 - \cos(n\omega T)] \cos[n(\omega t - \varphi)] \\ &+ \sum_{n=2k-1}^{\infty} I_n \sin(n\omega T) \sin[n(\omega t - \varphi)] \end{aligned} \tag{41.21}$$

The time delay introduced by the DSP affects the compensation performance, especially when fast changes are present in the load current. Nevertheless, when T is small ($T > 50$ s), the effect in compensation performance is negligible.

In four-wire systems, unbalances in the load current also affect the generation of the adequate current reference signal that will assure high-performance active power filter compensation. This assumption can be proved by considering the following load currents:

$$\begin{aligned} i_{La} &= I_1 \cos(\omega t - \varphi) + \sum_{n=2k-1}^{\infty} I_n \cos[n(\omega t - \varphi)] \\ i_{Lb} &= I_1(1 + l) \cos\left(\omega t - \varphi - \frac{2\pi}{3}\right) \\ &+ \sum_{n=2k-1}^{\infty} I_n(1 + l) \cos\left[n\left(\omega t - \varphi - \frac{2\pi}{3}\right)\right] \\ i_{Lc} &= I_1(1 - l) \cos\left(\omega t - \varphi + \frac{2\pi}{3}\right) \\ &+ \sum_{n=2k-1}^{\infty} I_n(1 - l) \cos\left[n\left(\omega t - \varphi + \frac{2\pi}{3}\right)\right] \\ i_{LN} &= i_{La} + i_{Lb} + i_{Lc} \end{aligned} \tag{41.22}$$

with $0 < l < 1$, $k = 1, 2, 3, \ldots$

Eq. (41.23) shows the presence of low-frequency even harmonics in the active power expression introduced by the load current unbalanced. These low-frequency current components force to reduce the cutoff frequency of the low-pass filter, close to 100 Hz, which affects the transient response of the active power filter:

$$\begin{aligned} p = \frac{3}{2} V_1 \Bigg[& I_1 \cos(\varphi) + \sum_{n=2k-1}^{\infty} I_n \cos[(n+1)\omega t - n\varphi] \\ & + \sum_{m=2k-1}^{\infty} I_m \cos[(m-1)\omega t - m\varphi] \Bigg] \quad \text{with} \quad k = 1, 2, 3, \ldots \end{aligned} \tag{41.23}$$

Synchronous reference frame algorithm

The block diagram of a current reference generator that uses the synchronous reference frame algorithm is shown in Fig. 41.15.

In this case, the real currents are transformed into a synchronous reference frame [2]. The reference frame is synchronized with the ac mains voltage and is rotating at the same frequency. The transformation is defined by

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ \sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{41.24}$$

As for the instantaneous reactive power theory, d and q terms are composed by a dc and multiple ac components, such as $i_d = i_{ddc} + i_{dac}$ and $i_q = i_{qdc} + i_{qac}$. The compensation reference signals are obtained from the following expressions: $i_{dref} = -i_{dac}$ and $i_{qref} = -i_{qdc} - i_{qac}$. The compensated currents generated by the shunt active power filter are obtained from Eq. (41.25):

$$\begin{bmatrix} i_{aref} \\ i_{bref} \\ i_{cref} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & 1 & 0 \\ \frac{1}{\sqrt{2}} & -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} -1 & 0 & 0 \\ 0 & \cos(\omega t) & -\sin(\omega t) \\ 0 & \sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} i_0 \\ i_{dref} \\ i_{qref} \end{bmatrix} \tag{41.25}$$

One of the most important characteristics of this algorithm is that the reference currents are obtained directly from the load currents without considering the source voltages. This is an

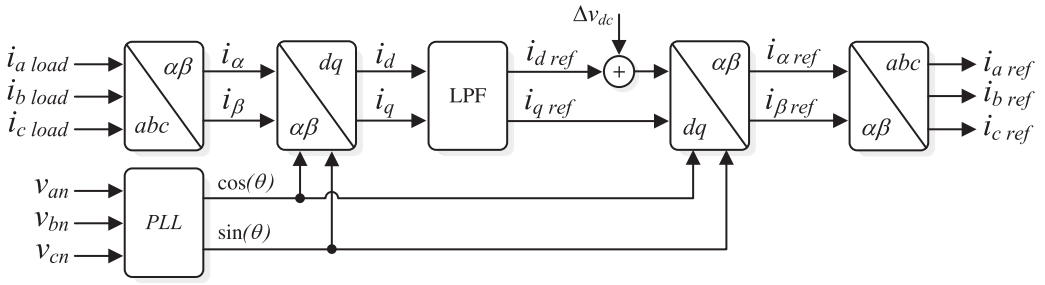


FIG. 41.15 The circuit block diagram required to obtain current reference waveforms using the synchronous reference frame theory.

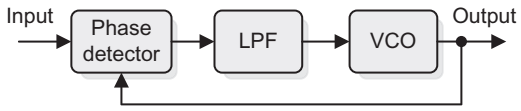


FIG. 41.16 The PLL circuit block diagram.

important advantage since the generation of the reference signals is not affected by voltage unbalance or voltage distortion, therefore increasing the compensation robustness and performance. However, in order to transform from the $\alpha-\beta$ plane to the d-q synchronous reference frame, sine and cosine signals synchronized with the respective phase-to-neutral voltages are required. A phase-locked loop (PLL) per each phase, as the one shown in Fig. 41.16, must be used.

Since the algorithm used to obtain the reference current presents the same mathematical procedure and operations that the ones required in the instantaneous reactive power concept, the effects introduced by the filter and DSP time delay are similar. Unbalanced load currents generate a different harmonic spectrum in the synchronous reference frame, and low-order harmonic components appear in the reference signal. In order to separate these uncharacteristic low-frequency current components, the cutoff frequency of the low-pass filter must be reduced.

Peak detection method

There are other possibilities to generate the current reference signal required to compensate reactive power and current harmonics. Basically, all the different schemes try to obtain the current reference signals that include the reactive components required to compensate the displacement power factor and the current harmonics generated by the nonlinear load. Fig. 41.17 shows another scheme used to generate the current reference signals required by a shunt active power filter. In this case, the ac current generated by the inverter is forced to follow the reference signal obtained from the current reference generator. In this circuit, the distorted load current is filtered, extracting the fundamental component, i_{l1}. The band-pass filter is tuned at the fundamental frequency (50 or 60 Hz), so that the gain attenuation introduced in the filter output signal is zero and the phase-shift angle is 180 degrees. Thus, the filter output current is exactly equal to the fundamental component of the load current but phase shifted by 180 degrees. If the load current is added to the fundamental current component obtained from the second-order band-pass filter, the reference current waveform required to compensate only harmonic distortion is obtained. In order to provide the reactive power required by the load, the current signal obtained from the second-order band-pass filter I_{l1} is synchronized with the respective phase-to-neutral source voltage (see Fig. 41.17) so that the inverter ac output current is forced to lead the respective inverter output voltage, thereby generating the required reactive power and absorbing the real power necessary to supply the switching losses and also to maintain the dc voltage constant.

The real power absorbed by the inverter is controlled by adjusting the amplitude of the fundamental current reference waveform, I_{l1}, obtained from the reference current generator. The amplitude of this sinusoidal waveform is equal to the amplitude of the fundamental component of the load current plus or minus the error signal obtained from the dc voltage control unit. In this way, the current signal allows the inverter to supply the current harmonic components, the reactive power required by the load, and to absorb the small amount of active power necessary to cover the switching losses and to keep the dc voltage constant (Fig. 41.18).

The main characteristic of this method is the direct derivation of the compensating component from the load current, without the use of any reference frame transformation [1,2]. Nevertheless, this technique presents a low-frequency oscillation problem in the active power filter dc bus voltage. To improve this technique, a modification of the previous scheme (Fig. 41.17) is shown in Fig. 41.19. The scheme is necessary for each phase. The expression for i_{Ma} is

$$i_{Ma}=\frac{I_1\cos(\varphi)}{2}+\frac{I_1\cos(2\omega t-\varphi)}{2}+\sum_{n=2k-1}^{\infty}\frac{I_n}{2}\{\cos[(n-1)\omega t-n\varphi]+\cos[(n+1)\omega t-n\varphi]\} \tag{41.26}$$

with $k=1, 2, 3,\ldots$

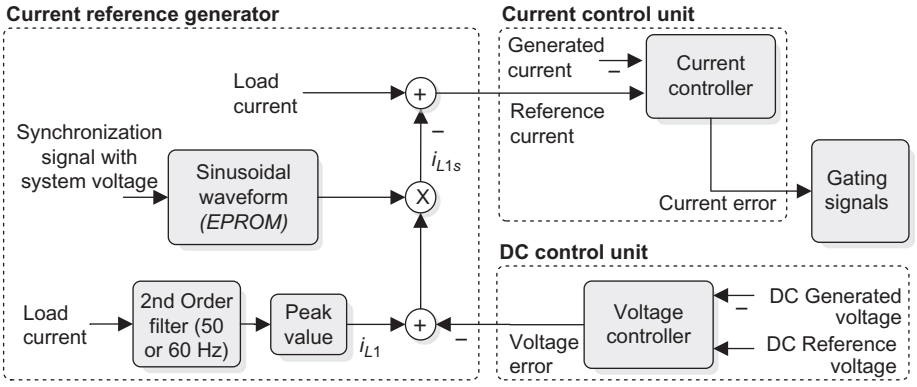


FIG. 41.17 The block diagram of an active power filter control scheme that does not use the instantaneous reactive power concept.

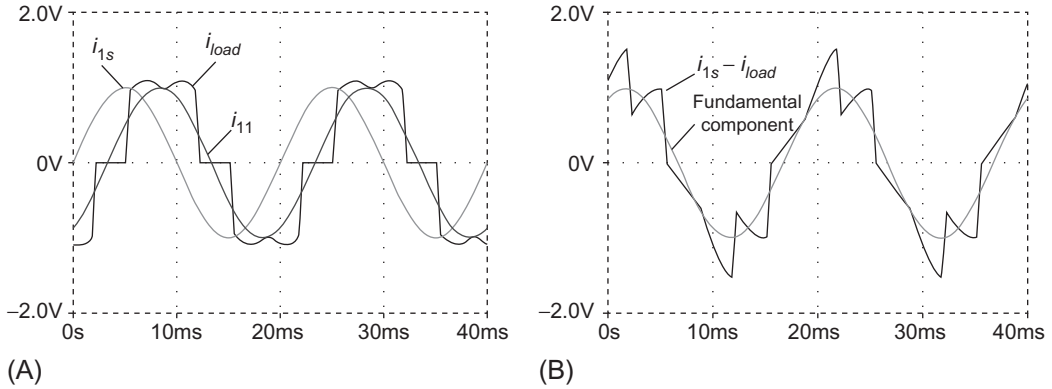


FIG. 41.18 The procedure for the generation of the current reference waveform: (A) the load current i_{load}, its fundamental component, i_{l1}, and the fundamental current component synchronized with the respective phase-to-neutral source voltage, i_{ls}, and (B) the synchronized fundamental current signal minus the load current, $i_{ls} - i_{load}$, and its fundamental component.

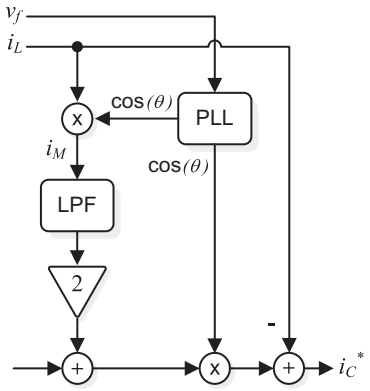


FIG. 41.19 Modified version of the original peak detection method.

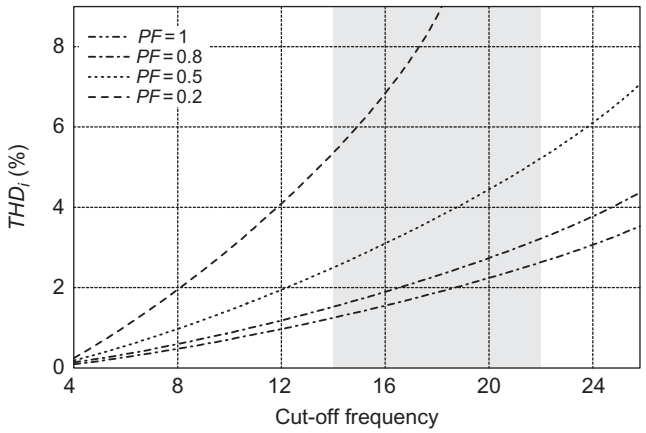


FIG. 41.20 Harmonic distortion of the system line current as a function of the cutoff frequency of the low-pass filter and the load displacement power factor.

Fig. 41.20 shows the current harmonic distortion introduced by the low-pass filter used in the control scheme and the associated cutoff frequency. The current distortion of the compensated current depends on the phase angle of the fundamental load current component.

The supply voltage has no effect on the reference current generation. Synchronization with the ac mains voltage is the important issue in this scheme and in the synchronous reference frame theory. Unbalanced loads do not affect the reference generation. Nevertheless, the method cannot achieve active power balance in four-wire systems. The control circuit implementation of the peak detection method is simple and does not require complex calculation, so the processing time on a DSP is lower than the required in the two previous implementations, ($T < 10$ s). The use of this method minimizes the distortion introduced on current harmonics.

Technical comparison of the three different techniques: In order to validate the effectiveness of the proposed analysis, a common industrial system is considered. The results are obtained using the previous equations and Matlab simulation results. The DSP delay introduced is using the processing time according to the DSP ADSP2187. The parameters considered are

$$THD_{iL} = 29\%$$
$$THD_V = 5\%$$
$$\cos(\varphi) = 0.87$$
$$\text{Unbalance} = 3\%$$

Table 41.2 shows the numeric results.

Table 41.3 shows a comparison of the three different techniques analyzed. The effects of the nonideal conditions are described for each technique.

In conclusion, it can be mentioned that the compensation performance of the different techniques is similar under ideal conditions, but under the presence of unbalanced and voltage

TABLE 41.2 Results of the considered case

Technique	THD_{iS}(%)	FP	Transient delay t_d (ms)
PQ	8.2	0.99	18.1
DQ	3.1	0.99	18.1
DPVM	2.3	0.99	56.8

TABLE 41.3 Comparison of the techniques

Parameter	PQ	SRF	PDM
Load *PF* required to achieve full compensation	$PF > 0.3$	$PF > 0.3$	$PF > 0.2$
Harmonic distortion voltage effect on the compensated current	$THD_i \approx THD_v$	0	0
Unbalanced voltage effect	$THD_i \approx$ Unbalance	0	0
Dynamic response under load changes (in function of f_c, $t_d = 5\tau$)	Fast (load balanced)	Fast (load balanced)	Slow
Capability of load balance	Yes (It is necessary to reduce cutoff frequency f_c)	Yes (it is necessary to reduce cutoff frequency f_c)	No
DSP delay time introduced	Minimum	Minimum	≈ 0

distortion, the synchronous reference frame algorithm presents the best performance, since it is insensitive to voltage perturbations. It is fundamental to consider adequately the cutoff frequency in the filter used to extract the ac component in the different techniques. If the frequency is changed, the compensation performance is affected as well as the transient response of the control scheme. In four-wire systems, unbalance in the load current also affects the generations of the adequate current reference. Unbalanced load currents generate a different harmonic spectrum in the dc reference frame, and low-order harmonic components appear in the reference signal; then, the cutoff frequency of the filter must be reduced.

41.2.3.2 Current Modulator

The effectiveness of an active power filter depends basically on the design characteristics of the current controller, the method implemented to generate the reference template and the modulation technique used. Most of the modulation techniques used in active power filters are based on PWM strategies. In this chapter, four of these methods, whose characteristics are their simplicity and effectiveness, are analyzed: periodical sampling control, hysteresis band control, triangular carrier control, and vector control. The first three methods have been tested with different waveform templates sinusoidal, quasisquare, and rectifier compensation current and were compared in terms of the harmonic content and distortion at the same switching frequency [3]. The analysis shows that for sinusoidal current generation the best method is triangular carrier, followed by hysteresis band and periodical sampling. For other types of references, however, one strategy may be better than the others. Also, it was shown that each control method is affected in a different way by the switching time delays present in the driving circuitry and in the power semiconductors.

Periodical sampling

The periodical sampling method switches the power transistors of the converter during the transitions of a square-wave clock of fixed frequency (the sampling frequency). As shown in Fig. 41.21, this type of control is very simple to implement since it requires a comparator and a D-type flip-flop per phase. The main advantage of this method is that the minimum time between switching transitions is limited to the period of the sampling clock. However, the actual switching frequency is not clearly defined.

Hysteresis band

The hysteresis band method switches the transistors when the current error exceeds a fixed magnitude: the hysteresis band. As can be seen in Fig. 41.22, this type of control needs a single comparator with hysteresis per phase. In this case, the switching frequency is not determined, but it can be estimated.

Triangular carrier

The triangular carrier method, shown in Fig. 41.23, compares the current error with fixed-amplitude and fixed-frequency

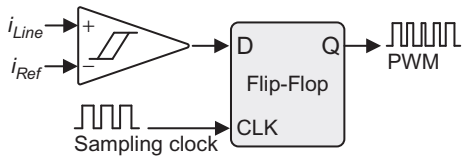


FIG. 41.21 Control modulator block for periodical sampling method.

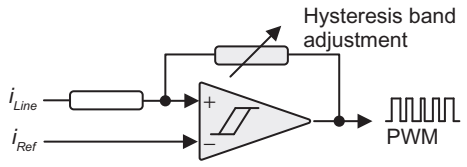


FIG. 41.22 Control modulator block for hysteresis band.

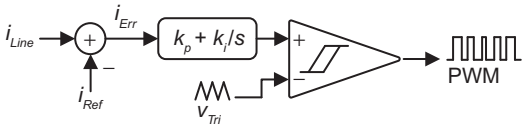


FIG. 41.23 Control modulator block for triangular carrier method.

triangular wave (the triangular carrier). The error is processed through a proportional-integral (PI) gain stage before the comparison with the triangular carrier takes place. As can be seen, this control scheme is more complex than the periodical sampling and hysteresis band. The values for the PI control gain k_p and k_i determine the transient response and steady-state error of the triangular carrier method. It was found empirically that the values for k_p and k_i shown in Eqs. (41.27) and (41.28) give a good dynamic performance under transient- and steady-state operating conditions:

$$k_p^* = \frac{(L + L_o) \cdot \omega_c}{2V_{dc}} \tag{41.27}$$

$$k_i^* = \omega_c k_p^* \tag{41.28}$$

where $L + L_o$ is the total series inductance seen by the converter; ω_c is the triangular carrier frequency, whose amplitude is 1 V peak-peak; and V_{dc} is the dc supply voltage of the inverter.

Vector control technique

This current control technique proposed in [4] divides the $\alpha - \beta$ reference frame of currents and voltages in six regions, phase shifted by 30 degrees (Fig. 41.24); identifies the region where the current vector error Δi is located; and selects the inverter output voltage vector V_{inv} that will force Δi to change in the opposite direction, keeping the inverter output current close to the reference signal.

Fig. 41.25 shows the single-phase equivalent circuit of the shunt active power filter connected to a nonlinear load and to the power supply.

The equation that relates the active power filter currents and voltages is obtained by applying Kirchhoff law to the equivalent circuit shown in Fig. 41.25:

$$V_{inv} = L\frac{di_{gen}}{dt} + E_0 \tag{41.29}$$

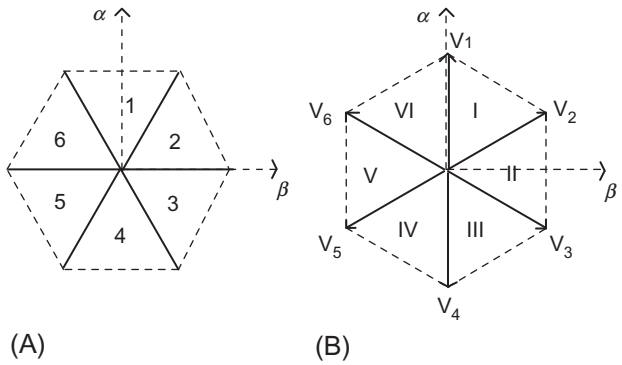


FIG. 41.24 The hexagons defined in the $\alpha - \beta$ reference frame by the current control scheme: (A) the hexagon defined by the inverter output current vector and (B) the hexagon defined by the inverter output voltage vector.

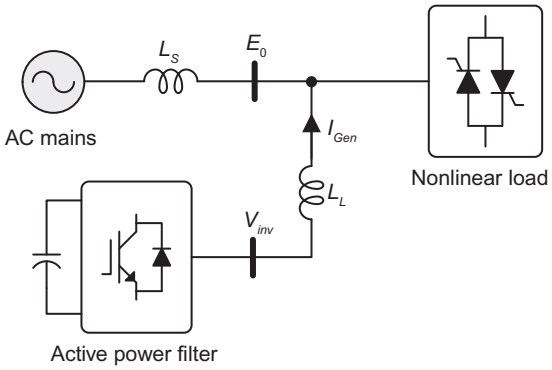


FIG. 41.25 The single-phase equivalent circuit of a shunt active power filter connected to the power system.

The current error vector Δi is defined by the following expression:

$$\Delta i = i_{ref} - i_{gen} \tag{41.30}$$

where i_{ref} represents the inverter reference current vector defined by the instantaneous reactive power concept. By replacing Eq. (41.30) in Eq. (41.29),

$$V_{inv} = L\frac{d}{dt}\left(i_{ref} - \Delta i\right) + E_0 \Rightarrow L\frac{d\Delta i}{dt} = L\frac{di_{ref}}{dt} + E_0 - V_{inv} \tag{41.31}$$

If $E = L\left(di_{ref}/dt\right) + E_0$, then Eq. (41.31) becomes

$$L\frac{d\Delta i}{dt} = E - V_{inv} \tag{41.32}$$

Eq. (41.32) represents the active power filter state equation and shows that the current error vector variation $d\Delta i/dt$ is defined by the difference between the fictitious voltage vector E and the inverter output voltage vector V_{inv}. In order to keep $d\Delta i/dt$ close to zero, V_{inv} must be selected near E_0.

The selection of the inverters' gating signals is defined by the region in which Δi is located and by its amplitude. In order to improve the current control accuracy and associate time response, depending on the amplitude of Δi, the following actions are defined:

- If $\Delta i \leq \delta$, the gating signals of the inverter are not changed.
- If $h \leq \Delta i \leq \delta$, the inverter gating signals are defined following mode a.
- If $\Delta i > h$, the inverter gating signals are defined following mode b.

where δ and h are reference values that define the accuracy and the hysteresis window of the current control scheme.

Mode a: Small changes in $\Delta i (h \leq \Delta i \leq \delta)$

The selection of the inverter switching mode a can be explained with the following example. Assuming that the voltage vector E

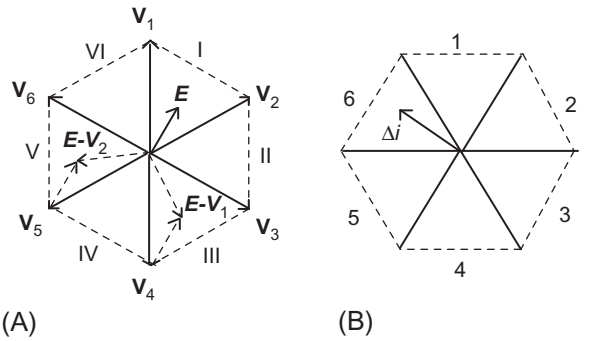


FIG. 41.26 Selection of the inverter switching pattern according to the region where Δi and E are located: (A) the regions where $Ld\Delta i/dt$ is located and (B) the region where Δi is located.

is located in region I (Fig. 41.26A) and the current error vector Δi is in region 6 (Fig. 41.26B), the inverter voltage vectors, V_{inv}, located closest to E are V_1 and V_2. The vectors $E - V_2$ and $E - V_1$ define two vectors $Ld\Delta i/dt$, located in regions III and V, respectively, as shown in Fig. 41.26A, so in order to reduce the current vector error Δi, $Ld\Delta i/dt$ must be located in region III. Thus, the inverter output voltage has to be equal to V_1. In this way, Δi will be forced to change in the opposite direction reducing its amplitude faster. By doing the same analysis for all the possible combinations, the inverter switching modes for each location of Δi and E can be defined (Table 41.4).

V_k represents the inverter switching functions defined in Table 41.5.

Mode b: Large changes in Δi ($\Delta i > h$)

If Δi becomes larger than h in a transient state, it is necessary to choose the switching mode in which the $d\Delta i/dt$ has the largest opposite direction to Δi. In this case, the best inverter output voltage V_{inv} corresponds to the value located in the same region of Δi.

The switching frequency may be fixed by controlling the time between commutations and not applying a new switching pattern if the time between two successive commutations is lower than a selected value ($t = 1/2f_c$).

Fig. 41.27 shows the block diagram of the inverter vector current control scheme implemented in a microcontroller. In Fig. 41.27, $^*E$ represents the region where the vector E is located, $^*\Delta i$, the region of Δi, k_1 keeps the same value of k (no commutation in the inverter), k_2 selects the new inverter output voltage from Table 41.4, and k_3 selects V_{inv} in the same region of Δi.

TABLE 41.4 Inverter switching modes

E region	Δi Region					
	1	2	3	4	5	6
I	V_1	V_2	V_2	$V_0 - V_7$	$V_0 - V_7$	V_1
II	V_2	V_2	V_3	V_3	$V_0 - V_7$	$V_0 - V_7$
III	$V_0 - V_7$	V_3	V_3	V_4	V_4	$V_0 - V_7$
IV	$V_0 - V_7$	$V_0 - V_7$	V_4	V_4	V_5	V_5
V	V_6	$V_0 - V_7$	$V_0 - V_7$	V_5	V_5	V_6
VI	V_1	V_1	$V_0 - V_7$	$V_0 - V_7$	V_6	V_6

TABLE 41.5 Relationship between switching function and inverter output voltage

k	Switch on phase a	Switch on phase b	Switch on phase c	Inverter output voltage V_k
0	4	6	2	0
1	1	6	2	$\frac{2}{3}V_{dc}$
2	1	3	2	$\frac{2}{3}V_{dc}e^{j\pi/3}$
3	4	3	2	$\frac{2}{3}V_{dc}e^{j2\pi/3}$
4	4	3	5	$\frac{2}{3}V_{dc}e^{j\pi}$
5	4	6	5	$\frac{2}{3}V_{dc}e^{j4\pi/3}$
6	1	6	5	$\frac{2}{3}V_{dc}e^{j5\pi/3}$
7	1	3	5	0

41.2.3.3 Control Loop Design

Active power filters based on self-controlled dc bus voltage require two control loops, one to control the inverter output current and the other to regulate the inverter dc voltage. Different design criteria have been presented in the technical literature; however, a classic design procedure using a PI controller will be presented in this chapter. In general, the design procedure for the current and voltage loops is based on the respective time-response requirements. Since the transient response of the active power is determined by the current control loop, its time response has to be fast enough to follow the current reference waveform closely. On the other hand, the time response of the dc voltage does not need to be fast and is selected to be at least 10 times slower than the current control loop time response. Thus, these two control systems can be decoupled and designed as two independent systems.

A PI controller is normally used for the current and the voltage control loops since it contributes to zero steady-state error in tracking the reference current and voltage signals, respectively.

Design of the current control loop

The design of the current control loop gains depends on the selected current modulator. In the case of selecting the triangular carrier technique, to generate the gating signals, the error between the generated current and the reference current is processed through a PI controller, and then, the output current error is compared with a fixed-amplitude and fixed-frequency triangular wave (Fig. 41.23). The advantage of this current modulator technique is that the output current of the converter has well-defined spectral line frequencies for the switching frequency components.

Since the active power filter is implemented with a voltage-source inverter, the ac output current is defined by the inverter

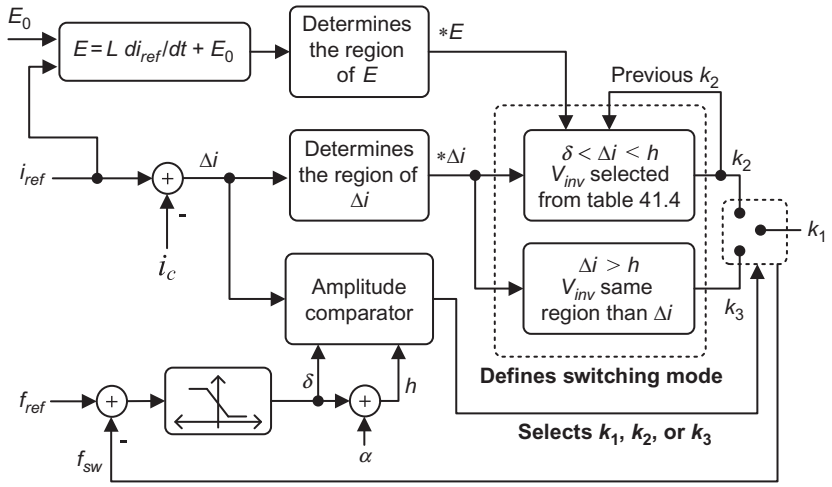


FIG. 41.27 The current control block diagram.

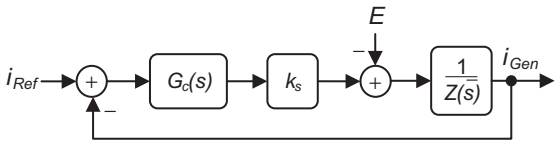


FIG. 41.28 The block diagram of the current control loop.

ac output voltage. The block diagram of the current control loop for each phase is shown in Fig. 41.28 where

E	phase-to-neutral source voltage,
$Z(s)$	impedance of the link reactor,
K_s	gain of the converter, and
$Gc(s)$	gain of the controller.

The values of K_s and $Gc(s)$ are given in Eqs. (41.33) and (41.34):

$$K_s = \frac{V_{dc}}{2\xi} \tag{41.33}$$

$$G_c(s) = K_p + \frac{K_i}{s} \tag{41.34}$$

From Fig. 41.27 and Eq. (41.34), the following expression is obtained:

$$I_{gen} = \frac{\left[K_s\left(K_p + (K_i/s)\right)\right]/(R_r + sL_r)}{1 + \left[K_s\left(K_p + (K_i/s)\right)/(R_r + sL_r)\right]} I_{ref} - \frac{1/(R_r + sL_r)}{1 + \left(K_s\left(K_p + K_i/s\right)/(R_r + sL_r)\right)} E \tag{41.35}$$

The characteristic equation of the current loop is given by

$$1 + \frac{\left(K_p s + K_i/s\right)}{s(R_r + sL_r)} \tag{41.36}$$

The analysis of the characteristic equation proves that the current control loop is stable for all values of K_p and K_i. Also, this analysis shows that K_p determines the speed response and K_i defines the damping factor of the control loop. If K_p is too big, the error signal can exceed the amplitude of the triangular waveform, affecting the inverter switching frequency, and if K_i is too small, the gain of the PI controller decreases, which means that the generated current will not be able to follow the reference current closely. The active filter transient response can be improved by adjusting the gain of the proportional part (K_p) to equal one and the gain of the integrator (K_i) to equal the frequency of the triangular waveform.

DC voltage control loop

Voltage control of the dc bus is performed by adjusting the small amount of real power flowing into the dc capacitor, thus compensating for the conduction and switching losses. The voltage loop is designed to be at least 10 times slower than the current loop, hence the two loops can be considered decoupled. The dc voltage control loop needs not to be fast, since it only responds for steady-state operating conditions. Transient changes in the dc voltage are not permitted and are taken into consideration with the selection criteria of the appropriate electrolytic capacitor value.

41.2.4 Power Circuit Design

The selection of the ac link reactor and the dc capacitor values affects directly the performance of the active power filter. Static var compensators implemented with voltage-source inverters present the same power circuit topology, but for this type of application, the criteria used to select the values of L_r and C are different. For reactive power compensation, the design of the synchronous link inductor, L_r, and the dc capacitor, C, is performed based on harmonic distortion constrain. That is, L_r must reduce the amplitude of the current harmonics generated by the inverter, while C must keep the dc voltage ripple factor below a given value. This design criteria cannot be

applied in the active power filter since it must be able to generate distorted current waveforms. However, L_r must be specified so that it keeps the high-frequency switching ripple of the inverter ac output current smaller than a defined value.

41.2.4.1 Design of the Synchronous Link Reactor

The design of the synchronous link reactor depends on the current modulator used. The design criteria presented in this section are based considering that the triangular carrier modulator is used. The design of the synchronous reactor is performed with the constraint that for a given switching frequency the minimum slope of the inductor current is smaller than the slope of the triangular waveform that defines the switching frequency. In this way, the intersection between the current error signal and the triangular waveform will always exist. In the case of using another current modulator, the design criteria must allow an adequate value of L_r in order to ensure that the di/dt generated by the active power filter will be able to follow the inverter current reference closely. In the case of the triangular carrier technique, the slope of the triangular waveform, λ, is defined by

$$\lambda = 4\xi f_t \tag{41.37}$$

where ξ is the amplitude of the triangular waveform, which has to be equal to the maximum permitted amount of ripple current, and f_t is the frequency of the triangular waveform (i.e., the inverter switching frequency). The maximum slope of the inductor current is equal to

$$\frac{di_L}{dt} = \frac{V_{an} + 0.5V_{dc}}{L_r} \tag{41.38}$$

Since the slope of the inductor current (di_L/dt) has to be smaller than the slope of the triangular waveform (λ) and the ripple current is defined, from Eqs. (41.37) and (41.38), as

$$L_r = \frac{V_{an} + 0.5V_{dc}}{4\xi f_t} \tag{41.39}$$

41.2.4.2 Design of the DC Capacitor

Transient changes in the instantaneous power absorbed by the load generate voltage fluctuations across the dc capacitor. The amplitude of these voltage fluctuations can be controlled effectively with an appropriate dc capacitor value. It must be noticed that the dc voltage control loop stabilizes the capacitor voltage after a few cycles, but is not fast enough to limit the first voltage variations. The capacitor value obtained with this criteria is bigger than the value obtained based on the maximum dc voltage ripple constraint. For this reason, the voltage across the dc capacitor presents a smaller harmonic distortion factor. The maximum overvoltage generated across the dc capacitor is given by

$$V_{C\max} = \frac{1}{C}\int_{\theta_1/\omega}^{\theta_2/\omega} i_C(t)dt + V_{dc} \tag{41.40}$$

where $V_{C\max}$ is the maximum voltage across the dc capacitor, V_{dc} is the steady-state dc voltage, and $i_c(t)$ is the instantaneous dc bus current. From Eq. (41.40),

$$C = \frac{1}{\Delta V}\int_{\theta_1/\omega}^{\theta_2/\omega} i_C(t)dt \tag{41.41}$$

Eq. (41.41) defines the value of the dc capacitor, C, that will maintain the dc voltage fluctuation below ΔV p.u. The instantaneous value of the dc current is defined by the product of the inverter line currents with the respective switching functions. The mean value of the dc current that generates the maximum overvoltage can be estimated by

$$\int_{\theta_1/\omega}^{\theta_2/\omega} i_C(t)dt = I_{inv}\int_{\theta_1/\omega}^{\theta_2/\omega} [\sin(\omega t) + \sin(\omega t + 120 \text{ degrees})]dt \tag{41.42}$$

In this expression, the inverter ac current is assumed to be sinusoidal. These operating conditions represent the worst case.

41.2.5 Technical Specifications

The standard specifications of shunt active power filters are the following:

- Number of phases: three phases and three wires or three phases and four wires (in case neutral currents need to be compensated)
- Input voltage: 200, 210, 220 ± 10%, 400, 420, 440 ± 10%, 6600 ± 10%
- Frequency: 50/60 Hz ± 5%
- Number of restraint harmonic orders: 2nd–25th
- Harmonic restraint factor: 85% or more at the rated output
- Type of rating: continuous
- Response: 1 ms or less

For shunt active power filter, the harmonic restraint factor is defined as $[1 - (I_{H_2}/I_{H_1})] \times 100\%$, where I_{H_1} is the harmonic currents flowing on the source side when no measure is taken for harmonic suppression and I_{H_2} is the harmonic currents flowing on the source side when harmonics are suppressed using an active filter.

41.3 Series Active Power Filters

Series active power filters were introduced by the end of the 1980s [5] and operate mainly as a voltage regulator and harmonic isolator between the nonlinear load and the utility system. The series-connected active power filter is more preferable to protect the consumer from an inadequate supply voltage quality. This type of approach is specially recommended for the compensation of voltage unbalances, voltage distortion,

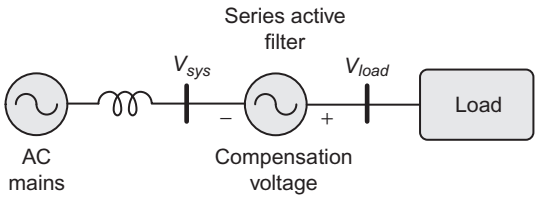


FIG. 41.29 The series active power filter operating as a voltage compensator.

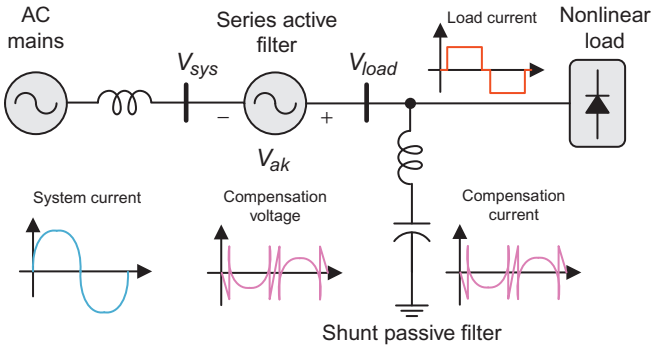


FIG. 41.30 Combination of series active power filter and passive filter for current harmonic compensation.

and voltage sags from the ac supply and for low-power applications represents an economically attractive alternative to UPS, since no energy storage (battery) is necessary and the overall rating of the components is smaller. The series active power filter injects a voltage component in series with the supply voltage and therefore can be regarded as a controlled voltage source, compensating voltage sags and swells on the load side (Fig. 41.29).

If passive LC filters are connected in parallel to the load, the series active power filter operates as a harmonic isolator forcing the load current harmonics to circulate mainly through the passive filter rather than the power distribution system (hybrid topology) (Fig. 41.30). The main advantage of this scheme is that the rated power of the series active power filter is a small fraction of the load kilovolt-ampere rating, typically 5%. However, the rated apparent power of the series active power filter may increase, in case voltage compensation is required.

41.3.1 Power Circuit Structure

The topology of the series active power filter is shown in Fig. 41.31. In most cases, the power circuit configuration is based on a three-phase PWM voltage-source inverter connected in series with the power lines through three single-phase coupling transformers. For certain type of applications, the three-phase PWM voltage-source converter can be replaced by three single-phase PWM inverters. However, this type of approach requires more power components, which increases the cost.

In order to operate as a harmonic isolator, a parallel LC filter must be connected between the nonlinear loads and the coupling transformers (Fig. 41.30). Current harmonic and voltage compensation are achieved by generating the appropriate voltage waveforms with the three-phase PWM voltage-source inverter, which are reflected in the power system through three

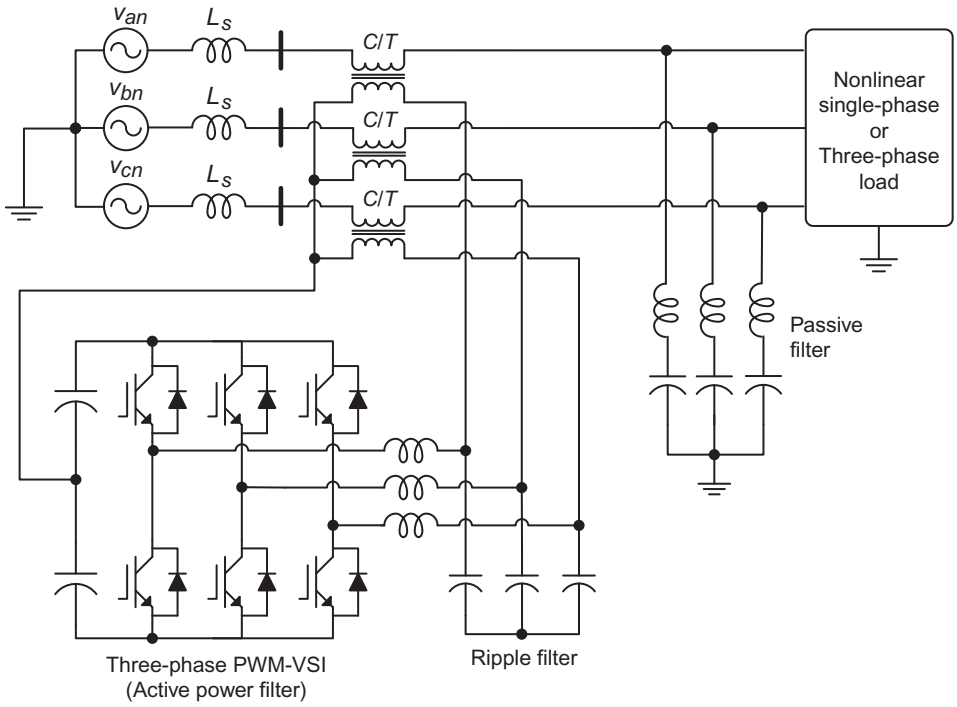


FIG. 41.31 The series active power filter topology.

coupling transformers. With an adequate control scheme, series active power filters can compensate for current harmonics generated by nonlinear loads, voltage unbalances, voltage distortion, and voltage sags or swells at the load terminals. However, it is very difficult to compensate the load power factor with this type of topology. In four-wire power distribution systems, series active power filters with the power topology can also compensate the current harmonic components that circulate through the neutral conductor.

41.3.2 Principles of Operation

Series active power filters compensate current system distortion caused by nonlinear loads by imposing a high-impedance path to the current harmonics, which forces the high-frequency currents to flow through the LC passive filter connected in parallel to the load (Fig. 41.30). The high impedance imposed by the series active power filter is created by generating a voltage of the same frequency that the current harmonic component needs to be eliminated. Voltage regulation or voltage unbalance can be corrected by compensating the fundamental frequency positive, negative, and zero-sequence voltage components of the power distribution system (Fig. 41.29). In this case, the series active power filter injects a voltage component in series with the supply voltage and therefore can be regarded as a controlled voltage source, compensating voltage regulation on the load side (sags or swells) and voltage unbalance. Voltage injection of arbitrary phase with respect to the load current implies active power transfer capabilities that increases the rating of the series active power filter and in most cases requires an energy storage element connected in the dc bus. Voltage and current waveforms shown in Figs. 41.32–41.34 illustrate the compensation characteristics of a series active power filter operating with a shunt passive filter.

41.3.3 Power Circuit Design

The power circuit topology of the series active power filter is composed by the three-phase PWM voltage-source inverter, the second-order resonant LC filters, the coupling transformers, and the secondary ripple frequency filter (Fig. 41.30). The design characteristics for each of the power components are described below.

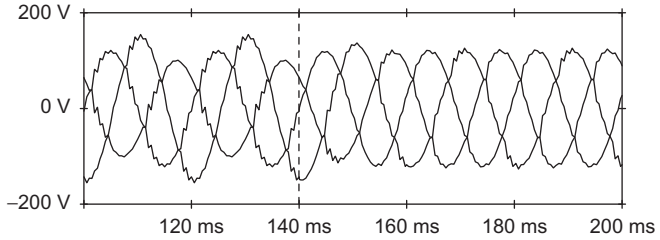


FIG. 41.32 Load voltage waveforms for voltage unbalance compensation. Phase-to-neutral voltages at the load terminals before and after series compensation. (Compensation starts at 140 ms, current harmonic compensator not operating.)

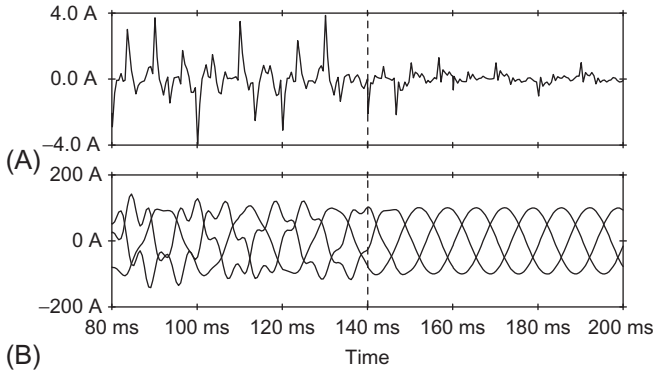


FIG. 41.33 System current waveforms for current harmonic compensation: (A) neutral current flowing to the ac mains before and after compensation and (B) line currents flowing to the ac mains before and after compensation. (Voltage unbalance compensator is not operating.)

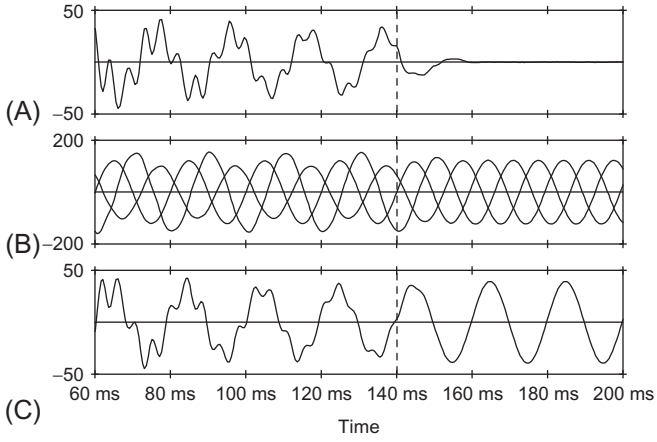


FIG. 41.34 Load voltages and system currents for voltage unbalance and current harmonic compensation, before and after compensation: (A) power system neutral current, (B) phase-to-neutral load voltages, and (C) power system line current.

41.3.3.1 PWM Voltage-Source Inverter

Since series active power filter can compensate voltage unbalance and current harmonics simultaneously, the rated power of the PWM voltage-source inverter increases compared with other approaches that compensate only current harmonics, since voltage injection of arbitrary phase with respect to the load current implies active power transfer from the inverter to the system. Also, the transformer leakage inductance entails fundamental voltage drop and apparent power, which has to be supported by the inverter, reducing the series active filter inverter rating available for harmonic and voltage compensation. The rated apparent power required by the inverter can be obtained by calculating the apparent power generated in

the primary of the coupling transformers. The voltage reflected across the primary winding of each coupling transformer is defined in Eq. (41.43):

$$V_{series} = \left[K_1^2 \left\{ \sum_{k \neq 1} I_{sk}^2 \right\}^{1/2} + K_2^2 \{ V_2 + V_0 \}^2 \right]^{1/2} \tag{41.43}$$

where V_{series} is the root-mean-square voltage across the primary winding of the coupling transformer. Eq. (41.43) shows that the voltage across the primary winding of the transformer is defined by two terms. The first one is inversely proportional to the quality factor of the passive LC filter, while the second one depends on the voltage unbalance that needs to be compensated. K_1 depends on the LC filter values, while K_2 is equal to one. The current flowing through the primary winding of the coupling transformer, due to the harmonic currents (Eq. 41.44), can be obtained from the equivalent circuit shown in Fig. 41.35:

$$I_{sk} = \frac{Z_{fk} I_{lk}}{Z_{fk} + Z_{sk} + K_1} \tag{41.44}$$

where $V_{series} = -K_1 I_{sk}$. The fundamental component of the primary current depends on the amplitude of the negative- and zero-sequence component of the source voltage due to the system unbalance.

41.3.3.2 Coupling Transformer

The purpose of the three coupling transformers is not only to isolate the PWM inverters from the source but also to match the voltage and current ratings of the PWM inverters with those of the power distribution system. The total apparent power required by each coupling transformer is one-third the total apparent power of the inverter. The turn ratio of the current transformer is specified according to the inverter dc bus voltage, K_1 and V_{ref}. The correct value of the turn ratio "a" must be specified according to the overall series active power filter performance. The turn ratio of the coupling transformer must be optimized through the simulation of the overall active power filter, since it depends on the values of different related parameters. In general, the transformer turn ratio must be high in order to reduce the amplitude of the inverter output current and to reduce the voltage induced across the primary winding. Also, the selection of the transformer turn ratio influences the performance of the ripple filter connected at the output of the PWM inverter. Taking into consideration all these factors, in general, the transformer turn ratio is selected equal to 1:20.

41.3.3.3 Secondary Ripple Filter

The design of the ripple filter connected in parallel to the secondary winding of the coupling transformer is performed following the method presented by Akagi in [6]. However, it is important to notice that the design of the secondary ripple filter depends mainly on the coupling transformer turn ratio and the current modulator used to generate the inverter gating signals. If the triangular carrier is used, the frequency of the triangular waveform has to be considered in the design of the ripple filter. The ripple filter connected at the output of the inverter avoids the induction of the high-frequency ripple voltage generated by the PWM inverter switching pattern at the terminals of the primary winding of the coupling transformer. In this way, the voltage applied in series to the power system corresponds to the components required to compensate voltage unbalanced and current harmonics. The single-phase equivalent circuit is shown in Fig. 41.36.

The voltage reflected in the primary winding of the coupling transformer has the same waveform as that of the voltage across the filter capacitor. For low-frequency components, the inverter output voltage must be almost equal to the voltage across C_{fr}. However, for high-frequency components, most of the inverter output voltage must drop across L_{fr}, in which case the voltage at the capacitor terminals is almost zero. Moreover, C_{fr} and L_{fr} must be selected in order not to exceed the burden of the coupling transformer. The ripple filter must be designed for the carrier frequency of the PWM voltage-source inverter. To calculate C_{fr} and L_{fr}, the system equivalent impedance at the carrier frequency, Z_{sys}, reflected in the secondary must be known. This impedance is equal to

$$Z_{sys(secondary)} = a^2 \cdot Z_{sys(primary)} \tag{41.45}$$

For the carrier frequency, the following design criteria must be satisfied:

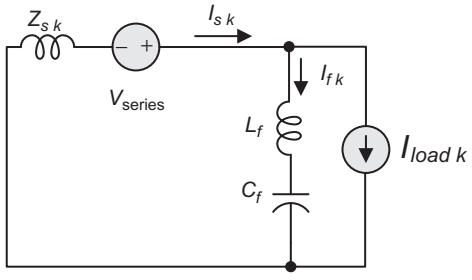


FIG. 41.35 The equivalent circuit of the series active power filter for harmonic components.

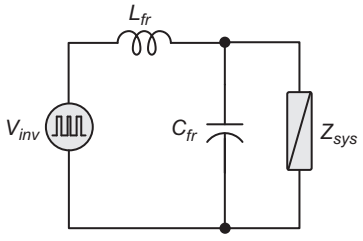


FIG. 41.36 The single-phase equivalent circuit of the inverter output ripple filter.

(i) $X_{Cfr} \ll X_{Lfr}$ to ensure that at the carrier frequency most of the inverter output voltage will drop across L_{fr}

(ii) X_{Cfr} and $X_{Lfr} \ll Z_{sys}$ to ensure that the voltage divider is between L_{fr} and C_{fr}

The small-rated LC passive filter exhibits a high-quality-factor circuit because of the high impedance on the output side. Oscillation between the small-rated inductor and capacitor may occur, causing undesirable high-frequency voltage across the ripple filter capacitor, which is reflected in the primary winding of the coupling transformer generating high-frequency current to flow through the power distribution system. It is important to note that this oscillation is very difficult to eliminate through the design and selection of the L_{fr} and C_{fr} values. However, it can be eliminated with the addition of a new control loop. The cause of the output voltage oscillation is explained with the help of Fig. 41.37. The transfer function $G_p(s)$ between the input voltage $V_i(s)$ and the output voltage $V_C(s)$ is given by the following equation:

$$G_p(s) = \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{41.46}$$

where $\omega_n = \sqrt{1/L_{fr}C_{fr}}$ and $\xi = r_L/2\sqrt{C_{fr}/L_{fr}}$.

Normally, the damping factor ξ is smaller than one, causing the voltage oscillation across the capacitor ripple filter, C_{fr}. Generally, relatively low impedance loads are connected to the output terminals of voltage-source PWM inverters. In these cases, the quality factor of the LC filter can be low, and the oscillation between the inductor L_{fr} and the capacitor C_{fr} is avoided [7].

41.3.3.4 Passive Filters

Passive filters connected between the nonlinear load and the series active power filter play an important role in the compensation of the load current harmonics. With the connection of the passive filters, the series active power filter operates as a harmonic isolator. The harmonic isolation feature reduces the need for precise tuning of the passive filters and allows their design to be insensitive to the system impedance and eliminates the possibility of filter overloading due to supply voltage harmonics. The passive filter can be tuned to the dominant load current harmonic and can be designed to correct the load displacement power factor.

However, for industrial loads connected to stiff supply, it is difficult to design passive filters that can absorb a significant part of the load harmonic current, and therefore, its effectiveness deteriorates. Specially, for compensation of diode rectifier type of loads, where a small kilovolt-ampere passive filter is required, it is difficult to achieve the required tuning to absorb significant percentage of the load harmonic currents. For this type of application, the passive filter cannot be tuned exactly to the harmonic frequencies because they can be overloaded due to the system voltage distortion and/or system current harmonics.

The single-phase equivalent circuit of a passive LC filter connected in parallel to a nonlinear current source and to the power distribution system is shown in Fig. 41.38. From this figure, the design procedure of this filter can be derived. The harmonic current component flowing through the passive filter i_{fh} and the current component flowing through the source i_{sh} are given by the following expressions:

$$i_{fh} = \frac{Z_s}{Z_s + Z_f} i_h; \quad i_{sh} = \frac{Z_f}{Z_s + Z_f} i_h \tag{41.47}$$

At the resonant frequency, the inductive reactance of the passive filter is equal to the capacitive reactance of the filter, that is,

$$2\pi frL = \frac{1}{2\pi frC} \tag{41.48}$$

Therefore, the resonant frequency of the passive filter is equal to

$$fr = \frac{1}{2\pi\sqrt{LC}} \tag{41.49}$$

The passive filter bandwidth is defined by the upper and lower cutoff frequency, at which values the filter current gain is −3 dB, as shown in Fig. 41.39.

The magnitude of the passive filter impedance as a function of the frequency is shown in Fig. 41.40.

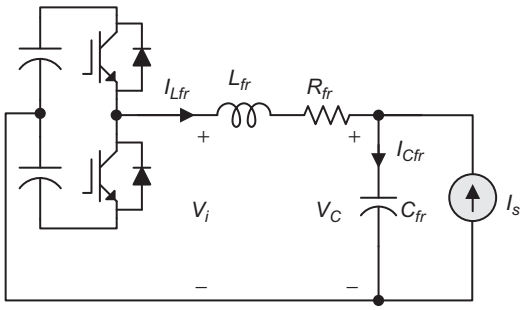


FIG. 41.37 Single-phase equivalent circuit of series active power filter connected to the ripple filter.

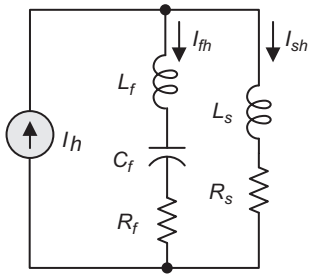


FIG. 41.38 The single-phase equivalent circuit of the passive filter connected to a nonlinear load.

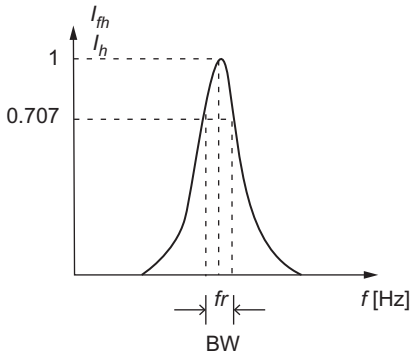


FIG. 41.39 The passive filter bandwidth.

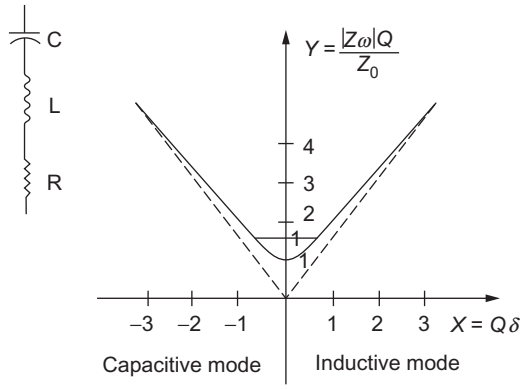


FIG. 41.40 The frequency response of the passive LC filter.

At the resonant frequency, the passive filter magnitude is equal to the resistance. If the resistance is zero, the filter is in short circuit. The quality factor of the passive filter is defined by the following expression:

$$Q = \frac{\omega_n L}{R} \tag{41.50}$$

It is important to note that the operation of the series active power filter with off-tuned passive filter has an adverse impact on the inverter power rating compared with the normal case. The more off-tuned the passive filter, the more rated apparent power is required by the series active power filter.

41.3.3.5 Protection Requirements

Short circuits in the power distribution system generate large currents that flow through the power lines until the circuit breaker operates clearing the fault. The total clearing time of a short circuit depends on the time delay imposed by the protection system. The clearing time cannot be instantaneous due to the operating time imposed by the overcurrent relay and by the total interruption time of the power circuit breaker. Although power system equipment, such us power transformers and cables, are designed to withstand short-circuit currents during at least 30 cycles, the active power filter may suffer severe damage during this short time. The withstand capability of the series active power filter depends mainly on the inverter power semiconductor characteristics.

Since the most important feature of series active power filters is the small-rated power required to compensate the power system, typically 10%–15% of the load rated apparent power, the inverter semiconductors are rated for low values of blocking voltages and continuous currents. This makes series active power filters more vulnerable to power system faults.

The block diagram of the protection scheme described in this section is shown in Fig. 41.41. It consists of a varistor connected in parallel to the secondary winding of each coupling transformer and a couple of antiparallel thyristors [8]. A special circuit detects the current flowing through the varistors and generates the gating signals of the antiparallel thyristors. The protection circuit of the series active power filter must protect only the PWM voltage-source inverter connected to the secondary of the coupling transformers and must not interfere with the protection scheme of the power distribution system. Since the primary of the active power filter coupling transformers is connected in series to the power distribution system, they operate as current transformers, so that their secondary windings cannot operate in open circuit. For this reason, if a short circuit is detected in the power distribution system, the PWM voltage-source inverter cannot be disconnected from the secondary of the current transformer. Therefore, the protection scheme must be able to limit the amplitude of the currents and voltages generated in the secondary circuits. This task is performed by the varistors and by the magnetic saturation characteristic of the transformers.

The main advantages of the series active power filter protection scheme described in this section are the following:

(i) It is easy to implement and has a reduced cost.
(ii) It offers full protection against power distribution short-circuit currents.
(iii) It does not interfere with the power distribution system.

When short-circuit currents circulate through the power distribution system, the low saturation characteristic of the

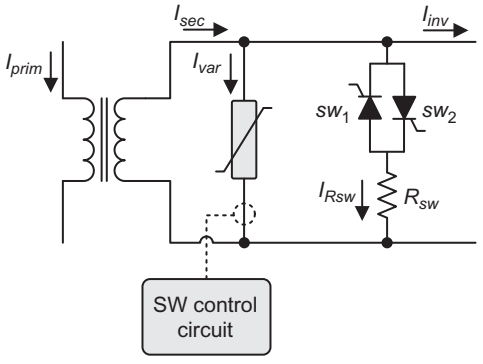


FIG. 41.41 The series active power filter protection scheme.

transformers increases the current ratio error and reduces the amplitude of the secondary currents. The larger secondary voltages induced by the primary short-circuit currents are clamped by the varistors, reducing the amplitude of the PWM voltage-source inverter currents. After a few cycles of duration of the short circuit, the PWM voltage-source inverter is bypassed through a couple of antiparallel thyristors, and at the same time, the gating signals applied to the PWM voltage-source inverter are removed. In this way, the PWM voltage-source inverter can be turned off. The principles of operation and the effectiveness of the protection scheme are shown in Fig. 41.42.

The secondary short-circuit currents will circulate through the antiparallel thyristors and the varistors until the fault is cleared by the protection equipment of the power distribution system.

By using the protection scheme described in this subsection, the voltage and currents reflected in the secondary of the coupling transformers are significantly reduced. When short-circuit currents circulate through the power distribution system, the low saturation characteristic of the coupling transformers increases the current ratio error and reduces the amplitude of the secondary voltages and currents. Moreover, the saturated high secondary voltages induced by the primary short-circuit currents are clamped by the varistors, reducing the amplitude of the PWM voltage-source inverter ac currents. Once the secondary current exceeds a predefined reference value, the PWM voltage-source inverter is bypassed through a couple of antiparallel thyristors, and then, the gating signals applied to the PWM voltage-source inverter are removed. The effectiveness of the protection scheme is shown in Fig. 41.43.

By increasing the current ratio error due to the magnetic saturation, the energy dissipated in the secondary of the coupling transformer is significantly reduced. The total energy dissipated in the varistor for the different protection conditions is shown in Fig. 41.44.

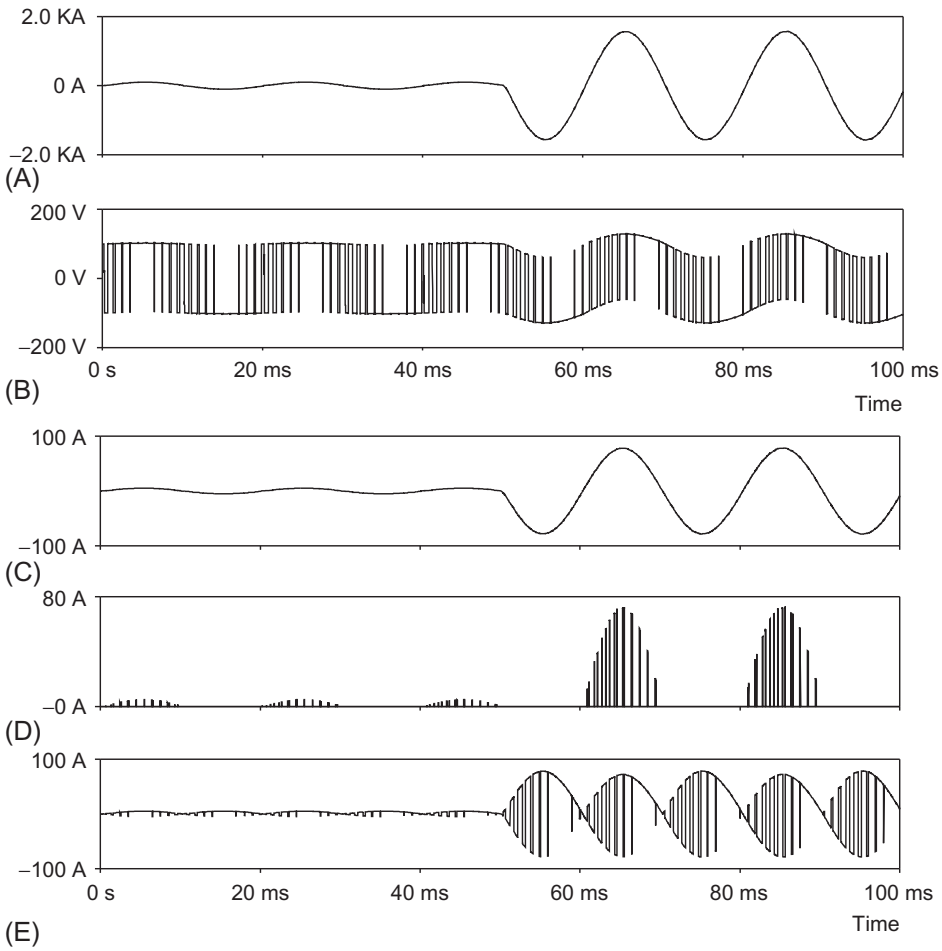


FIG. 41.42 Current waveforms of the series active power filter during a three-phase short circuit in the power distribution system set at 50 ms: (A) power distribution system line current, (B) current transformer secondary voltage, (C) inverter ac current, (D) current through an inverter leg, and (E) inverter dc bus current.

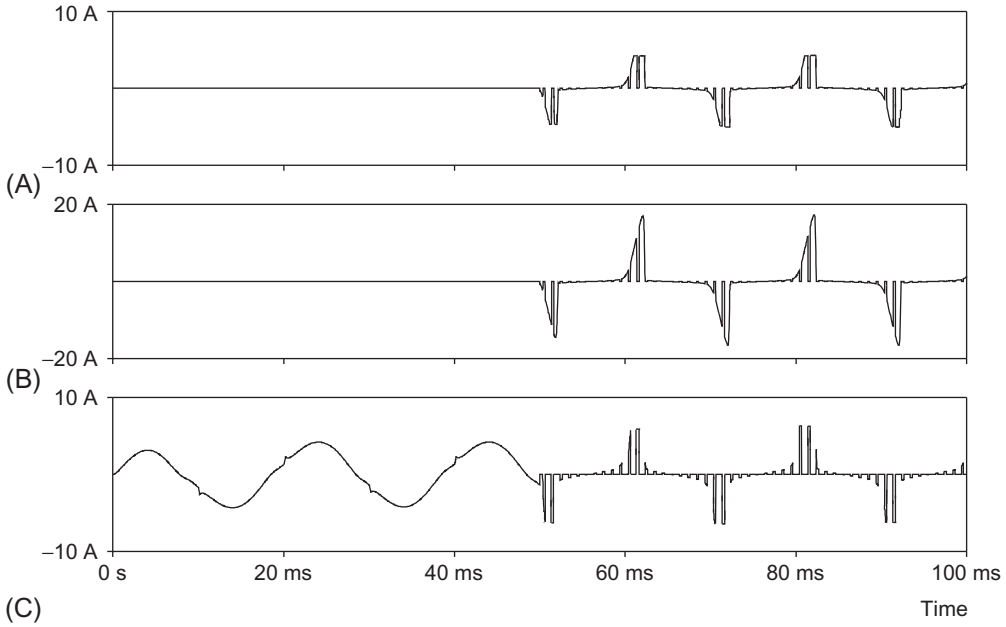


FIG. 41.43 Current waveforms for a line-to-line short circuit in the power distribution system. The protection scheme is implemented with the varistor, a couple of antiparallel thyristors, and a coupling transformer with low saturation characteristic: (A) current through the varistor, (B) current through the thyristors, and (C) inverter ac current.

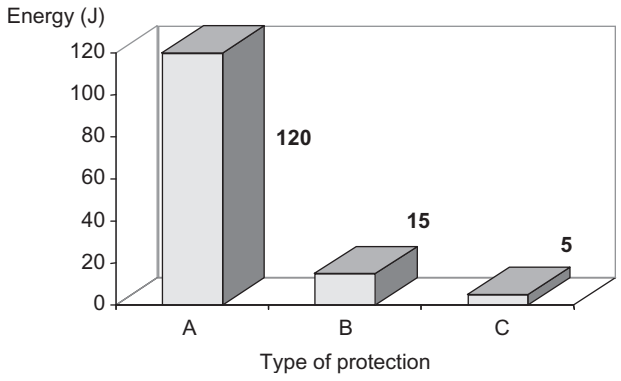


FIG. 41.44 The total energy dissipated in the varistor during the power system short circuit for different protection schemes implementations: (A) only with the varistor used, (B) the varistor is connected in parallel to a bidirectional switch, and (C) with the complete protection scheme operating (including the coupling transformer with low saturation characteristics).

41.3.4 Control Issues

The block diagram of a series active power filter control scheme that compensates current harmonics and voltage unbalance simultaneously is shown in Fig. 41.45.

Current and voltage reference waveforms are obtained by using the Park transformation (instantaneous reactive power theory) voltage unbalance that is compensated by calculating the negative- and zero-sequence fundamental components of the system voltages. These voltage components are added to the source voltages through the coupling transformers compensating the voltage unbalance at the load terminals. In order to reduce the amplitude of the current flowing through the neutral conductor, the zero-sequence components of the line currents are calculated. In this way, it is not necessary to sense the current flowing through the neutral conductor.

41.3.4.1 Reference Signals Generator

The compensation characteristics of series active power filters are defined mainly by the algorithm used to generate the reference signals required by the control system. These reference signals must allow current and voltage compensation with minimum time delay. Also, it is important that the accuracy of the information contained in the reference signals allows the elimination of the current harmonics and voltage unbalance present in the power system. Since the voltage and current control schemes are independent, the equations used to calculate the voltage reference signals are the following:

$$\begin{bmatrix} v_{a0} \\ v_{a1} \\ v_{a2} \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} . \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{41.51}$$

The voltages v_a, v_b, and v_c correspond to the power system phase-to-neutral voltages before the current transformer. The reference voltage signals are obtained by making the positive-sequence component, v_{a1}, zero and then applying

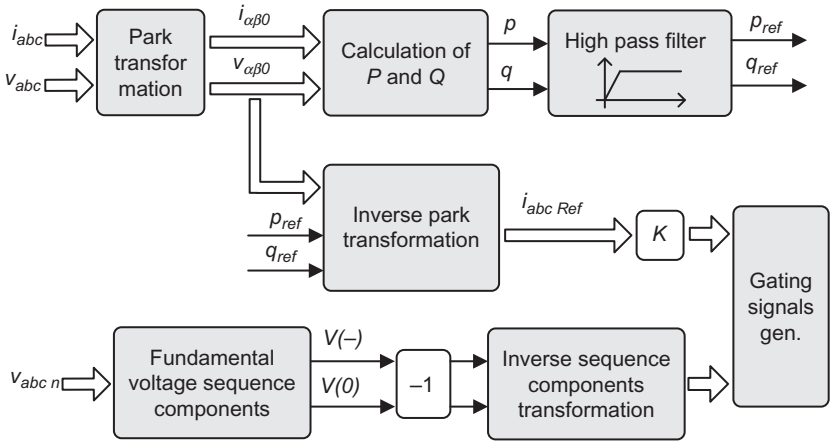


FIG. 41.45 Compensation scheme for voltage unbalance correction.

the inverse of the Fortescue transformation. In this way, the series active power filter compensates only voltage unbalance and not voltage regulation. The reference signals for the voltage unbalance control scheme are obtained by applying the following equations:

$$\begin{bmatrix} v_{refa} \\ v_{refb} \\ v_{refc} \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \cdot \begin{bmatrix} -v_{ao} \\ 0 \\ -v_{a2} \end{bmatrix} \tag{41.52}$$

In order to compensate current harmonics generated by the nonlinear loads, the following equations are used:

$$\begin{bmatrix} i_{aref} \\ i_{bref} \\ i_{cref} \end{bmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} 1 & 0 \\ \frac{-1}{2} & \frac{\sqrt{3}}{2} \\ \frac{-1}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix}^{-1} \begin{bmatrix} p_{ref} \\ q_{ref} \end{bmatrix} + \frac{1}{\sqrt{3}} \begin{bmatrix} i_0 \\ i_0 \\ i_0 \end{bmatrix} \tag{41.53}$$

where i_0 is the fundamental zero-sequence component of the line current and is calculated using the Fortescue transformation Eq. (41.50):

$$i_0 = \frac{1}{\sqrt{3}}(i_a + i_b + i_c) \tag{41.54}$$

In Eq. (41.40), p_{ref}, q_{ref}, v_α, and v_β are defined according to the instantaneous reactive power theory. In order to avoid the compensation of the zero-sequence fundamental frequency current, the reference signal i_0 must be forced to circulate through a high-pass filter generating a current i_0' that is used to create the reference signal required to compensate current harmonics. Finally, the general equation that defines the references of the PWM voltage-source inverter required to compensate voltage unbalance and current harmonics is the following:

$$\begin{bmatrix} V_{refa} \\ V_{refb} \\ V_{refc} \end{bmatrix} = K_1 \left\{ \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ \frac{-1}{2} & \frac{\sqrt{3}}{2} \\ \frac{-1}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix}^{-1} \begin{bmatrix} P_{ref} \\ q_{ref} \end{bmatrix} + \frac{1}{\sqrt{3}} \begin{bmatrix} i_0' \\ i_0' \\ i_0' \end{bmatrix} \right\} + K_2 \left\{ \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \cdot \begin{bmatrix} -v_{a0} \\ 0 \\ -v_{a2} \end{bmatrix} \right\} \tag{41.55}$$

where K_1 is the gain of the coupling transformer that defines the magnitude of the impedance for high-frequency current components and K_2 defines the degree of compensation for voltage unbalance, ideally K_2 equals 1.

41.3.4.2 Gating Signals Generator

This circuit provides the gating signals of the three-phase PWM voltage-source inverter required to compensate voltage unbalance and current harmonic components. The current and voltage reference signals are added, and then, the amplitude of the resultant reference waveform is adjusted in order to increase the voltage utilization factor of the PWM inverter for steady-state operating conditions. The gating signals of the inverter are generated by comparing the resultant reference signal with a fixed-frequency triangular waveform. The triangular waveform helps to keep the inverter switching frequency constant (Fig. 41.46).

A higher voltage utilization of the inverter is obtained if the amplitude of the resultant reference signal is adjusted for the steady-state operating condition of the series active power filter. In this case, the reference current and reference voltage waveforms are smaller. If the amplitude is adjusted for transient operating conditions, the required reference signals will have a

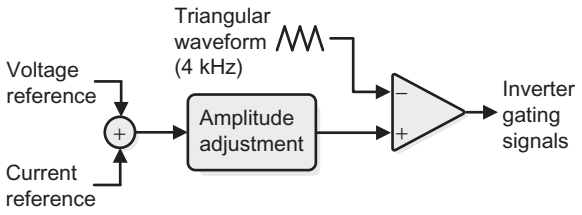


FIG. 41.46 The block diagram of the gating signal generator.

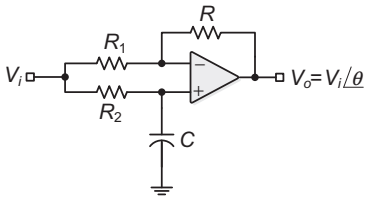


FIG. 41.48 The all-pass filter used as a phase shifter.

larger value, creating a higher dc voltage in the inverter and defining a lower voltage utilization factor for steady-state operating conditions. The inverter switching frequency must be higher in order not to interfere with the current harmonics that need to be compensated.

41.3.5 Control Circuit Implementation

Since the control scheme of the series active power filter must translate the current harmonic components that need to be compensated in voltage signals, a proportional controller is used. The use of a PI controller is not recommended since it would modify the reference waveform and generate new current harmonic components. The gain for proportional controller depends on the load characteristics, and its value fluctuates between one and two.

Another important element used in the control scheme is the filter that allows to generate p_{ref} and q_{ref} (Fig. 41.35). The frequency response of this filter is very important and must not introduce any phase shift or attenuation to the low-frequency harmonic components that must be compensated. A high-pass first-order filter tuned at 15 Hz is adequate. This corner frequency is required when single-phase nonlinear loads are compensated. In this case, the dominant current harmonic is the third. An example of the filter that can be used is shown in Fig. 41.47.

The operator "a" required to calculate the sequence components of the system voltages (Fortescue transformation) can be obtained with the all-pass filter shown in Fig. 41.48.

The phase shift between V_o and V_i is given by the following expression:

$$\theta = 2\arctan\left(2\pi f R_2 C\right) \tag{41.56}$$

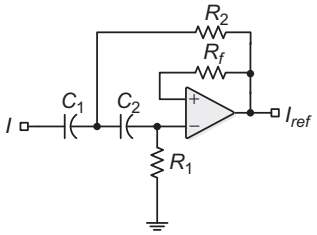


FIG. 41.47 The first-order high-pass filter implemented for the calculation of p_{ref} and q_{ref} ($C_1 = C_2 = 0.1\,\mu F$, $R_1 = R_f = 150\,k\Omega$, and $R_2 = 50\,k\Omega$).

Since the phase shift is negative, the operator "a" is obtained by using an inverter (180 degrees) and then by tuning $\theta = -60$ degrees. The operator "a^2" is obtained by phase shifting V_i by -120 degrees. V_i is synchronized with the system phase-to-neutral voltage V_{an}.

41.3.6 Experimental Results

The viability and effectiveness of series active power filters used to compensate current harmonics was proved in an experimental setup of 5 kVA. Current waveforms generated by a nonlinear load and using only passive filters and the combination of passive and the series active power filter are shown in Figs. 41.49 and 41.50.

These figures show the effectiveness of the series active power filter, which reduces the overall *THD* of the current that flows through the power system from 28.9% (with the operation of only the passive filters) to 9% with the operation of the passive filters with the active power filter connected in series. The compensation of the current that flows through the neutral conductor is shown in Fig. 41.51.

41.4 Hybrid Active Power Filters

Hybrid topologies composed of passive LC filters connected in series to an active power filter have already been proposed by the end of the 1980s [2,5,6,9,10]. Hybrid topology improves significantly the compensation characteristics of simple passive filters, making the use of active power filter available for high-power applications, at a relatively lower cost. Moreover, the compensation characteristics of already installed passive filters can be significantly improved by connecting a series active power filter at its terminals, giving more flexibility to the compensation scheme. Most of the technical disadvantages of passive filters described before can be effectively attenuate if an active power filter is connected in series to the passive approach as shown in Fig. 41.52.

The hybrid active power filter topology is shown in Fig. 41.52. The active power filter is implemented with a three-phase PWM voltage-source inverter operating at fixed switching frequency and connected in series to the passive filter through a coupling transformer. Basically, the active power filter forces the utility line currents to become sinusoidal and in

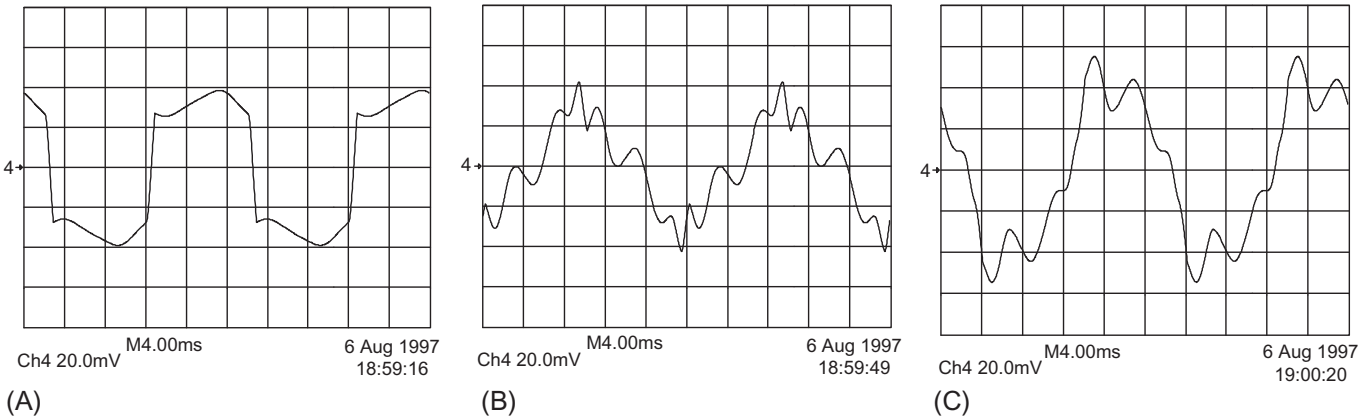


FIG. 41.49 Experimental results without the operation of the series active power filter: (A) load current, (B) current flowing through the passive filter, and (C) current through the power supply.

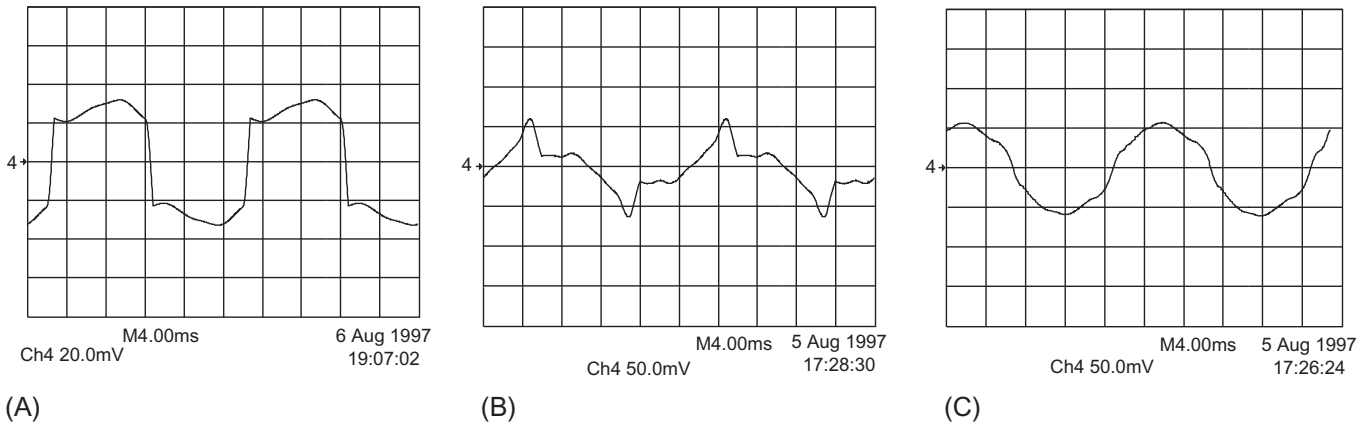


FIG. 41.50 Experimental results with the operation of the series active power filter: (A) load current, (B) current flowing through the passive filter, and (C) current through the power supply.

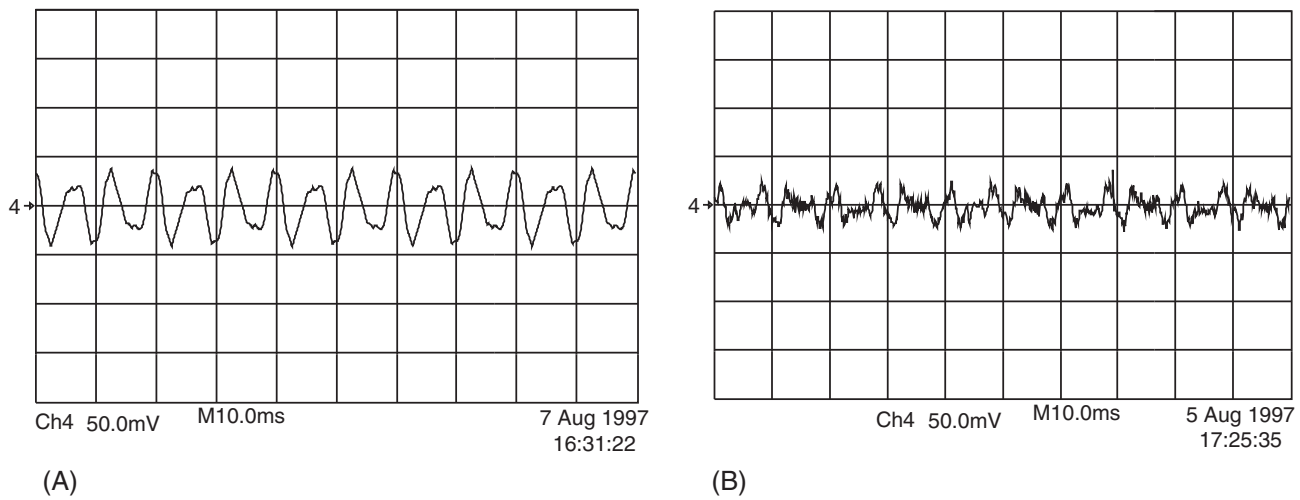


FIG. 41.51 Experimental results of neutral current compensation: (A) current flowing through the neutral without the operation of the series active power filter and (B) current flowing through the neutral with the operation of the active power filter.

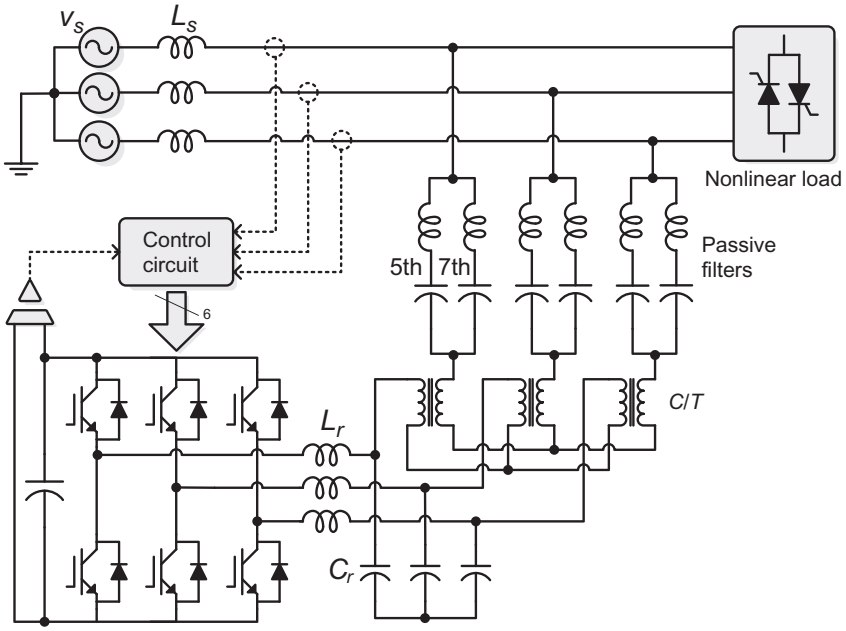


FIG. 41.52 The hybrid active power filter configuration.

phase with the respective phase-to-neutral voltage, improving the compensation characteristics of the passive filter.

41.4.1 Principles of Operation

Since the active power filter is connected in series to the passive filter through a coupling transformer, it imposes a voltage signal at its primary terminals that forces the circulation of current harmonics through the passive filter, improving its compensation characteristics, independently of the variations in the selected resonant frequency of the passive filter. The block diagram of the proposed control scheme shown in Fig. 41.53 consists of three modules: the dc voltage control, the voltage reference generator, and the inverter gating signal generator.

The voltage reference waveform required by the inverter control scheme is obtained by adjusting the amplitude of a

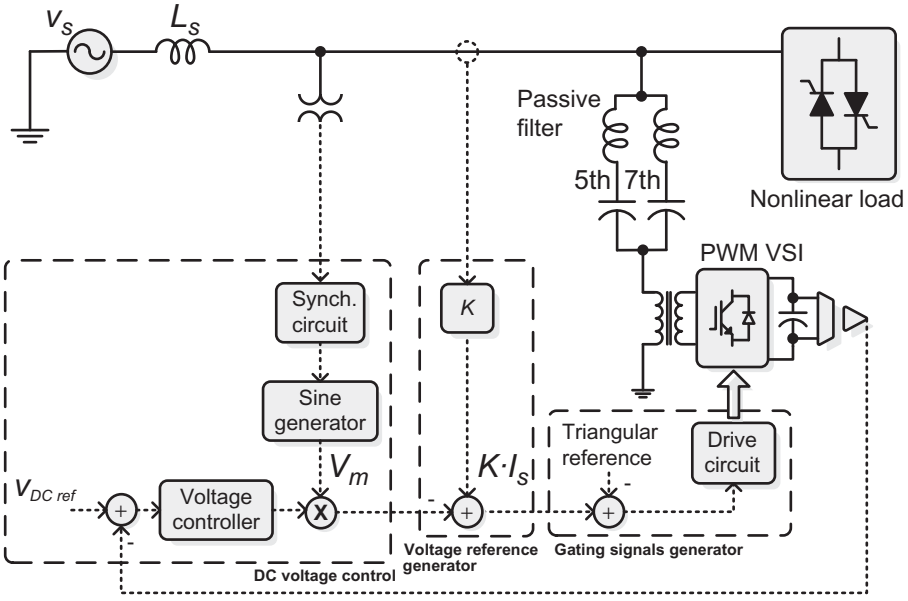


FIG. 41.53 The hybrid active power filter topology and associated control scheme.

sinusoidal reference waveform in phase with the respective phase-to-neutral voltage and then subtracting the respective ac line current (Fig. 41.53). The sinusoidal reference signal can be obtained from the voltage system (in case of low voltage distortion), or it can be generated from an EPROM synchronized with the respective phase-to-neutral voltage. The amplitude of this reference waveform controls the inverter dc voltage and the ac mains displacement power factor. The inverter dc voltage varies according with the amount of real power absorbed by the inverter, while the ac mains power factor depends on the amount of reactive power generated by the hybrid filter, which can be controlled by changing the amplitude of the fundamental component of the inverter output voltage.

The principles of operation for current harmonic and power factor compensation are explained with the help of the single-phase equivalent circuit shown in Fig. 41.54. In the current harmonic compensation mode, the active filter improves the filtering characteristic of the passive filter by imposing a voltage harmonic waveform at its terminals with an amplitude value equals to

$$V_{Ch} = K \cdot I_{Sh} \tag{41.57}$$

where I_{Sh} is the harmonic content of the line current to be compensated and K is the active power filter gain. If the ac mains voltage is purely sinusoidal, the ratio between the harmonic component of the nonlinear load current and the harmonic component of the ac line current (attenuation factor) is obtained from Fig. 41.54A and is equal to

$$\frac{I_{Sh}}{I_{Lh}} = \frac{Z_F}{K + Z_F + Z_S} \tag{41.58}$$

Eq. (41.58) shows that the filtering characteristics of the hybrid topology (I_{Sh}/I_{Lh}) depend on the value of the passive filter equivalent impedance, Z_F. Moreover, since the tuned factor, δ, and the quality factor, Q, can modify the filter bandwidth and the passive filter harmonic equivalent impedance (Fig. 41.55), their values must be carefully selected in order to maintain the compensation effectiveness of the hybrid topology. In particular, a high value of the quality factor, Q, defines a large bandwidth of the passive filter, improving the compensation characteristics of the hybrid topology. On the other hand, a low value in the quality factor and/or a large value in the tuned factor increases the required voltage generated by the active power filter necessary to keep the same compensation effectiveness, which increases the active power filter rated power.

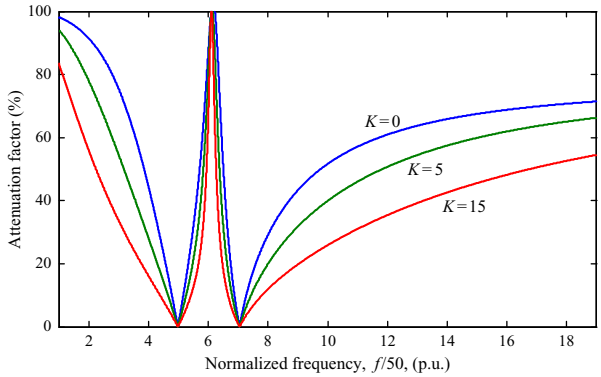


FIG. 41.55 The attenuation factor of the line current harmonics for different frequency values.

Fig. 41.55 shows how the active power filter gain, K, in Eq. (41.57) affects the harmonic attenuation factor of the line currents. The attenuation factor of the line current harmonics expressed in percentage is obtained from Eq. (41.59) and is shown in Fig. 41.56, for a power distribution system with two passive filters tuned at fifth and seventh harmonics.

$$THD_i = \frac{\sqrt{\sum_{h=2} [I_{Lh} \cdot (Z_F/(Z_S + Z_F + K))]^2}}{I_{S1}} \tag{41.59}$$

Eq. (41.59) indicates that the total harmonic distortion of the line current decreases if K increases. In other words, a better hybrid filter compensation is obtained for larger values of voltage harmonic components generated by the active power filter. Also, it is shown that the compensation capability of the hybrid

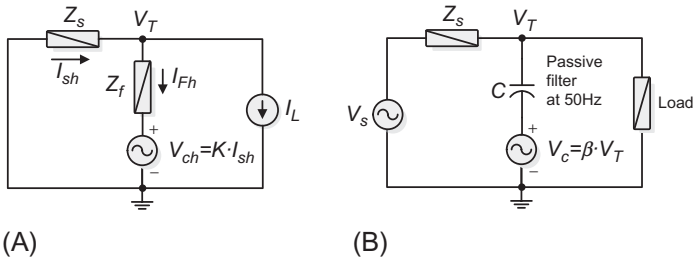


FIG. 41.54 Single-phase equivalent circuits of the hybrid active power filter scheme: (A) for current harmonic compensation and (B) for displacement power factor compensation.

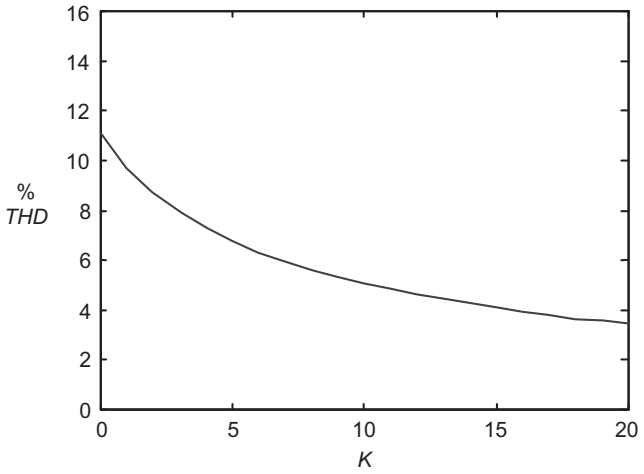


FIG. 41.56 System line current *THD* vs *K* factor.

filter depends on the compensation characteristic of the passive filter, that is, the filter impedance value and tuned frequency will affect the active filter rated power required to satisfy the system line current compensation requirements.

Displacement power factor correction can be achieved by controlling the voltage drop across the passive filter capacitor. In order to do that, a voltage at fundamental frequency is generated at the inverter ac terminals, with an amplitude equals to

$$V_C = \beta \cdot V_T \tag{41.60}$$

Displacement power factor control can be achieved since at fundamental frequency the passive filter equivalent impedance is capacitive. The reactive power generated by the passive filter is obtained by changing the voltage imposed by the active power filter across the passive filter capacitor terminals. The passive filter fundamental current component is defined by the following expression:

$$i_F = C\frac{d}{dt}(v_T - \beta v_T) = (1-\beta)C\frac{dv_T}{dt} = C_\gamma \beta \frac{dv_T}{dt} \tag{41.61}$$

Eq. (41.61) proves that the equivalent capacitance at fundamental frequency $C\gamma$ can be modified by changing β. The reactive power generated by the active filter is β times the reactive power generated by the passive filter and can be defined by

$$Q_\gamma = V_C \cdot I_F = \beta V_T I_F \tag{41.62}$$

Eq. (41.62) shows that if $\beta > 0$, the active power filter generates a voltage at fundamental frequency in phase with V_T, reducing the reactive power that flows to the load. If $\beta < 0$, the active power filter generates a voltage at fundamental frequency phase shifted by 180 degrees with respect to V_T, increasing the reactive power that flows to the load. In other words, by selecting a β positive or negative, the hybrid topology can generate or absorb reactive power at fundamental frequency, compensating for leading or lagging displacement power factor of the nonlinear load. This is achieved by changing the voltage across the passive filter capacitor C_F.

41.4.2 The Hybrid Filter Compensation Performance

The design characteristics of the passive filters have an important influence on the compensation performance of the hybrid topology. The tuned frequency and quality factor of the passive filter directly influence the compensation characteristics of the hybrid topology. If these two factors are not properly selected, the rated power of the active filter must be increased in order to get the required compensation performance. The tuned factor, δ, in per unit with respect to the resonant frequency is defined by Eq. (41.63):

$$\delta = \frac{\omega - \omega_n}{\omega_n} \tag{41.63}$$

Here, δ defines the magnitude in which the passive filter resonant frequency changes due to the variations in the power system frequency and modifications in the values of the passive filter parameters L and C. The values of L and C can change due to aging conditions, temperature, or design tolerances. The tuning factor, δ, can also be defined as

$$\delta = \frac{\Delta f}{f_n} + \frac{1}{2}\left(\frac{\Delta L}{L_n} + \frac{\Delta C}{C_n}\right) \tag{41.64}$$

The quality factor, Q, of the passive filter is defined by Eq. (41.65):

$$Q = \frac{X_0}{R} \tag{41.65}$$

where X_0 is equal to

$$X_0 = \omega_n L = \frac{1}{\omega_n C} = \sqrt{\frac{L}{C}} \tag{41.66}$$

The passive filter quality factor, Q, defines the ratio between the passive filter reactance with respect to its resistance. In order to have a passive filter low impedance value in a limited frequency bandwidth, defined by the maximum expected changes of the rated power system frequency, it is necessary to reduce X_0 or increase the passive filter resistance R, reducing the value of Q. However, if R increases, the equivalent impedance of the passive filter at the resonant frequency will increase, with the associated power losses, increasing the overall passive filter operational cost. On the other hand, the larger the value of Q, the lower is the passive filter equivalent impedance at the resonant frequency, increasing the currents harmonic components across the filter, at the resonant operating point.

41.4.2.1 Effects of the Power System Equivalent Impedance

The influence of the power system equivalent impedance on the hybrid filter compensation performance is related with its effects on the passive filter, since if the system equivalent impedance is lower than the passive filter equivalent impedance at the resonant frequency, most of the load current harmonics will flow mainly to the power distribution system. In order to compensate this negative effect on the hybrid filter compensation performance, K must be increased, as shown in Eq. (41.57), increasing the active power filter rated power.

Fig. 41.57 shows how the system equivalent impedance affects the relation between the system current *THD* with the active filter gain, K, in a power distribution system with passive filters tuned at the fifth and seventh harmonics. If Z_s decreases, the current system *THD* increases, so in order to keep the same compensation performance of the hybrid scheme, the active power filter gain, K, must be increased. On the other hand, if Z_s is high, it is not necessary to increase K in order to ensure a low *THD* value in the system current.

41.4.2.2 Effects of the Passive Filter Quality Factor

The quality factor, Q, defines the passive filter bandwidth. A passive filter with a high quality factor, Q, presents a larger bandwidth and better compensation characteristics. Eq. (41.67) defines the quality factor value in terms of the passive filter parameters L, R, and C. This equation shows that if R or C decreases, Q increases, and the filter bandwith becomes larger, improving the hybrid scheme compensation characteristics:

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}} \tag{41.67}$$

Although by decreasing R or C the passive filter quality factor is improved, each element produces a different effect in the hybrid filtering behavior. For example, by increasing R, the filter equivalent impedance at the resonant frequency becomes bigger, affecting the current harmonic compensation characteristics at this specific frequency.

Fig. 41.58 illustrates how the system current *THD* changes with different values of C while keeping the filter tuned factor, δ, constant. It is important to note that the larger the value of C, the better is the compensation characteristic of the hybrid scheme. An appropriate value of C must be selected, since C cannot be increased too much. If C is too big, the fundamental component of the filter current will increase, overloading the hybrid filter and generating a large amount of reactive power to the power distribution system. A similar analysis is made for the value of the resistance, showing the results in Fig. 41.59.

41.4.2.3 Effects of the Passive Filter Tuned Factor

The tuned factor, δ, is defined in Eq. (41.63). This factor affects the hybrid scheme performance especially at the passive filter

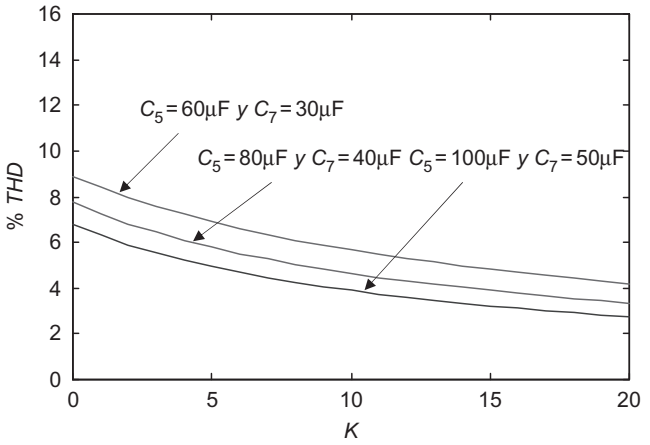


FIG. 41.58 *THD* of the system line current vs the K factor for different values of filter capacitor.

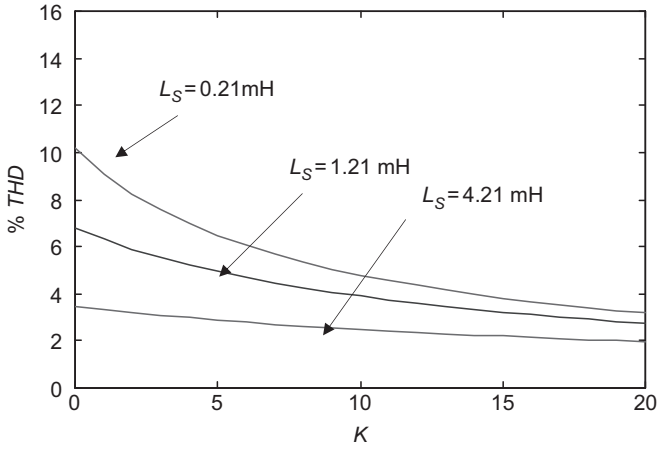


FIG. 41.57 Relation between the *THD* of the line current vs the active power filter gain, K, for different values of the system equivalent impedance.

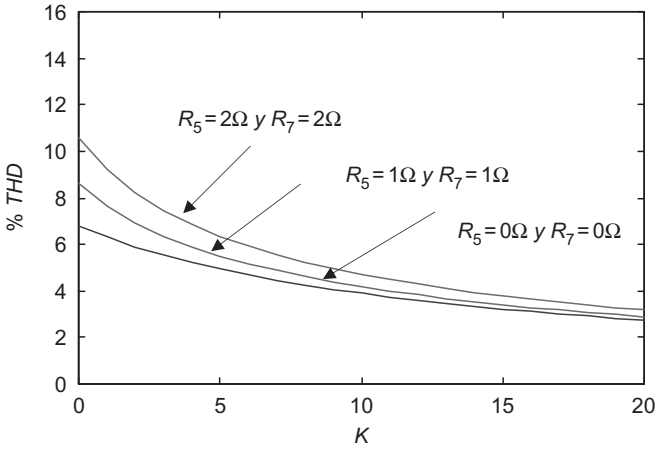


FIG. 41.59 *THD* of the system line current vs the K factor for different values of filter resistor.

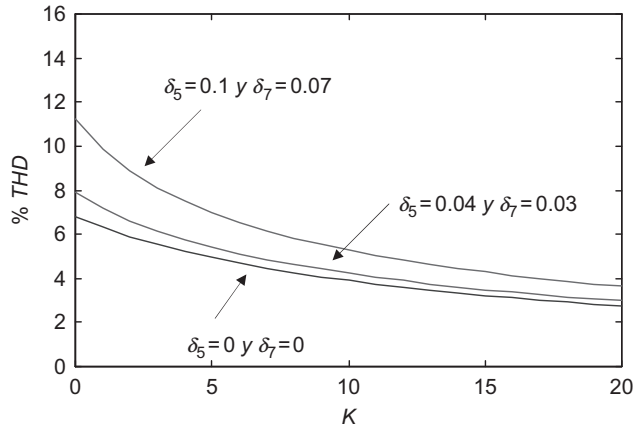


FIG. 41.60 *THD* of the system line current vs the *K* factor for different values of tuned factor.

resonant frequency, since δ defines the changes in the system frequency, affecting the value of the passive filter resonant frequency. Fig. 41.60 shows how the system current *THD* changes with respect to the active power filter gain, *K*, for different values of passive filter tuned factors. The larger the value of δ, the filtering performance of the hybrid filter becomes worst.

41.4.3 Experimental Results

A laboratory prototype using IGBT switches was implemented and tested in the compensation of a six-pulse controlled rectifier. The inverter was operated at 4 kHz switching frequency. Steady-state experimental results are illustrated in Figs. 41.61 and 41.62.

In case resonance is generated between the passive filter and system equivalent reactance, the system current *THD* increases to 60%. By connecting the active power filter, the line current *THD* is reduced to 4.9%, as shown in Figs. 41.63 and 41.64.

41.5 Predictive Control in Active Power Filters

Traditionally, active power filters have been controlled using pretuned controllers, such as PI-type or adaptive, for the current and for the dc voltage loops. PI controllers must be designed based on the equivalent linear model, while predictive controllers use the nonlinear model, which is closer to real operating conditions. Providing an accurate model is used, a predictive controller improves the performance of the active power filter, especially during transient operating conditions, because it can quickly follow the current reference signal while maintaining a constant dc voltage.

Fig. 41.65 shows the equivalent circuit of a shunt APF application. One advantage of using model-based predictive control in active power filter applications is that the power converter model and parameter are well-known or can be easily determined. These parameters are obtained from the converter output ripple filter (Z_f) and the power system equivalent impedance (Z_s). The former is known from the design stage of the active power filter, and the latter can be determined using well-known standard procedures of calculation or online estimation.

41.5.1 Predictive Current Control

The block diagram of the proposed digital predictive current control scheme is shown in Fig. 41.66. This control scheme

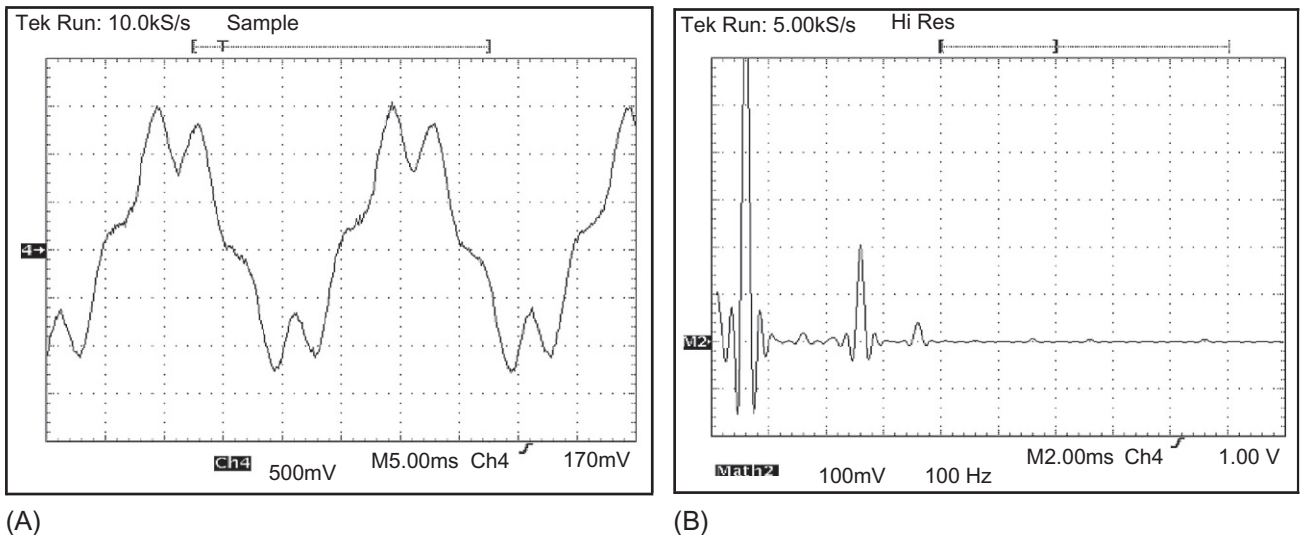


FIG. 41.61 Experimental ac line current waveform with passive filtering compensation: (A) line current waveform (*THD* = 24%) and (B) line current frequency spectrum.

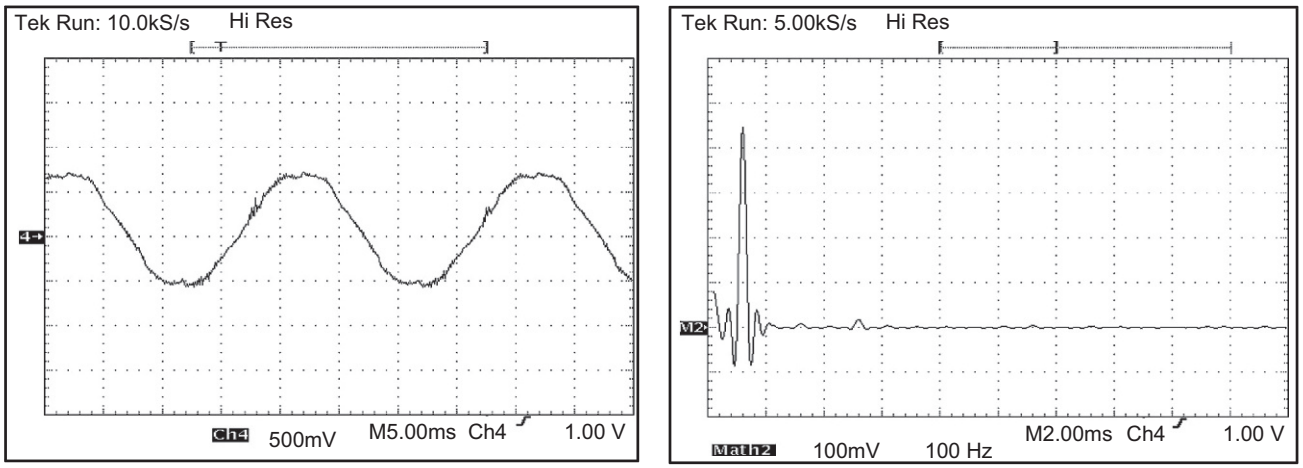


FIG. 41.62 Experimental ac line current waveform with hybrid filter compensation: (A) line current waveform ($THD = 6.3\%$) and (B) associated frequency spectrum.

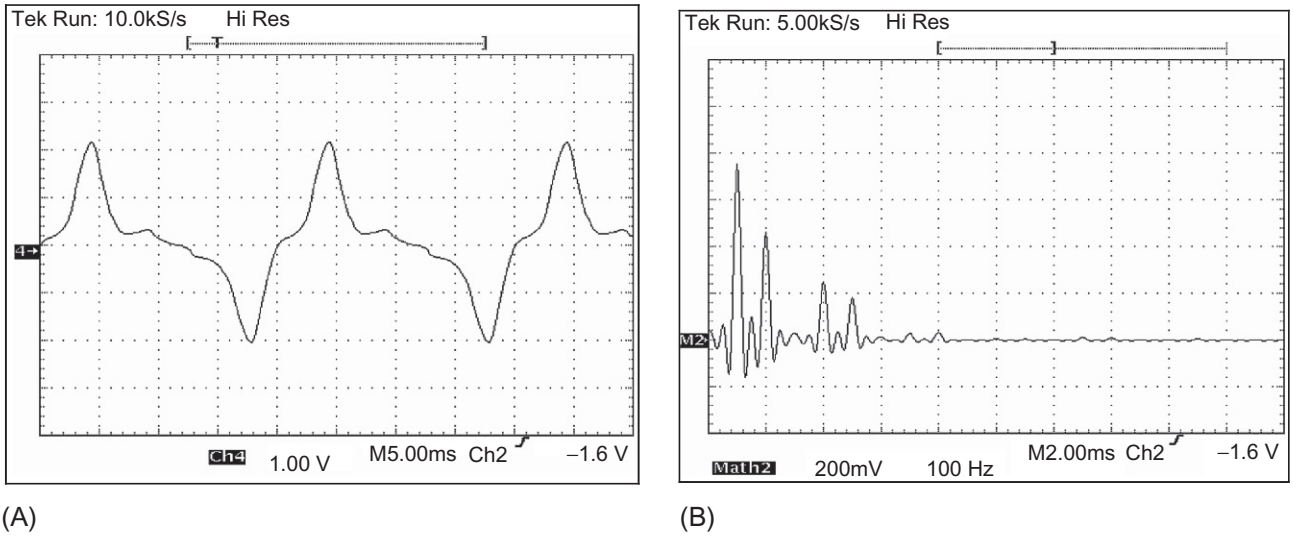


FIG. 41.63 Experimental ac line current waveform for resonant compensation: (A) line current waveform ($THD = 60\%$) and (B) associated frequency spectrum.

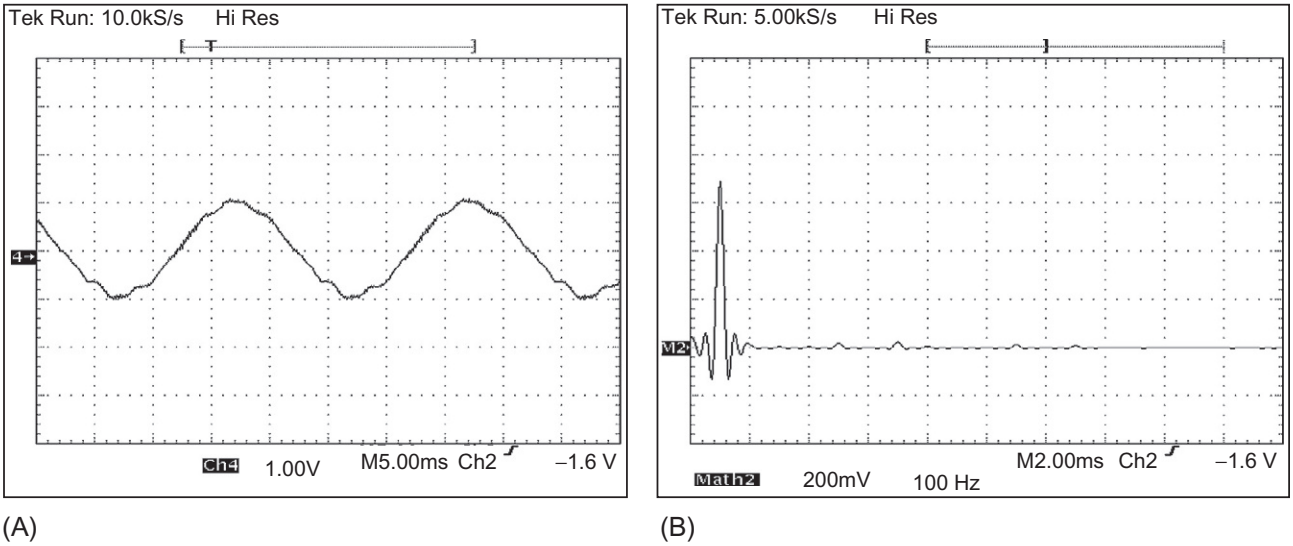


FIG. 41.64 Experimental ac line current waveform with hybrid topology compensation: (A) line current waveform ($THD = 4.9\%$) and (B) associated frequency spectrum.

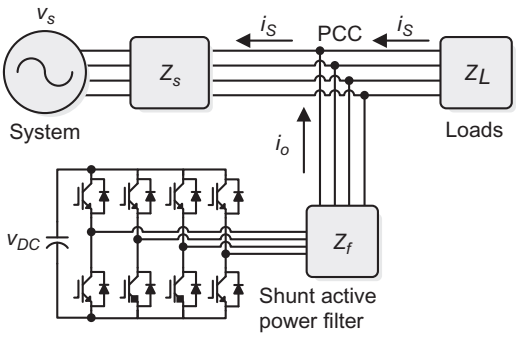


FIG. 41.65 Three-phase equivalent circuit of the proposed shunt APF.

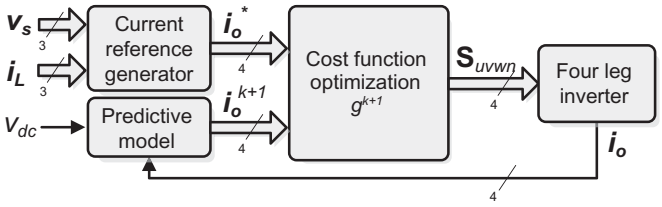


FIG. 41.66 Block diagram of the proposed predictive current control.

entails an optimization algorithm that is implemented in a microprocessor. Consequently, the analysis has to be developed using discrete mathematics in order to consider additional restrictions such as time delays and approximations. The essence of model-based predictive control is the use of the model of the system to be controlled to predict the future state of some of its variables. The controller then, according to a predefined optimization criterion, selects the optimum switching pattern that has to be applied to the power converter in order for it to achieve the future state with minimum error. The predictive control algorithm can be implemented with three main blocks, as shown in Fig. 41.66.

41.5.1.1 Current Reference Generator

This unit is designed to generate the required current reference that is used to compensate the undesirable load current components. In this case, the system voltages, the load currents, and the dc voltage converter are measured, while the neutral output current and neutral load current are generated directly from these signals.

41.5.1.2 Prediction Model

The converter model is used to predict the output converter current. Since the controller operates in discrete time, both the controller and the system model must be represented in a discrete-time domain. The discrete-time model consists of a recursive matrix equation that represents this prediction system. This means that for a given sampling time T_s, knowing the converter switching states and control variables at instant kT_s, it is possible to predict the next states at any instant $[k+1]$ T_s. Due to the first-order nature of the state equations that describe the model in (41.68) and (41.69), a sufficiently accurate first-order approximation of the derivative is considered:

$$v_o = v_{xn} - R_{eq} i_o - L_{eq} \frac{di_o}{dt} \tag{41.68}$$

$$v_{xn} = S_x - S_n v_{dc}\,, x = u, v, w, n. \tag{41.69}$$

Therefore, the 16 possible output current predicted values can be obtained from (41.68) as

$$i_o[k+1] = \frac{T_s}{L_{eq}}(v_{xn}[k] - v_o[k]) + \left(1 - \frac{R_{eq} T_s}{L_{eq}}\right) i_o[k] \tag{41.70}$$

41.5.1.3 Cost Function

In order to select the optimal switching state that must be applied to the power converter, the 16 predicted values obtained for $i_o[k+1]$ are compared with the reference using a cost function g, as follows:

$$\begin{aligned} g[k+1] = &\left(i_{ou}^*[k+1] - i_{ou}[k+1]\right)^2 \\ &+ \left(i_{ov}^*[k+1] - i_{ov}[k+1]\right)^2 \\ &+ \left(i_{ow}^*[k+1] - i_{ow}[k+1]\right)^2 \\ &+ \left(i_{on}^*[k+1] - i_{on}[k+1]\right)^2 \end{aligned} \tag{41.71}$$

The output current (i_o) is equal to the reference (i_o^*) when $g=0$. Therefore, the optimization goal of the cost function is to achieve a g-value close to zero. During each sampling state, the voltage vector v_{xn} that minimizes the cost function is found and then applied to the converter in the next sampling state.

41.5.2 Current Reference Generator

A dq-based current reference generator scheme is used to obtain the active power filter current reference signals (see "Synchronous Reference Frame Algorithm" section). This scheme presents a fast and accurate signal-tracking capability. This characteristic avoids voltage fluctuations that deteriorate the current reference signal affecting compensation performance. The current reference signals are obtained from the corresponding load currents as shown in Fig. 41.67. The cutoff frequency of the LPF used in this example is 20 Hz.

The current that flows through the neutral of the load is compensated by injecting the same instantaneous value obtained from the phase currents but with a phase shift of 180 degrees as shown in (41.72):

$$i_{on}^* = -(i_{Lu} + i_{Lv} + i_{Lw}) \tag{41.72}$$

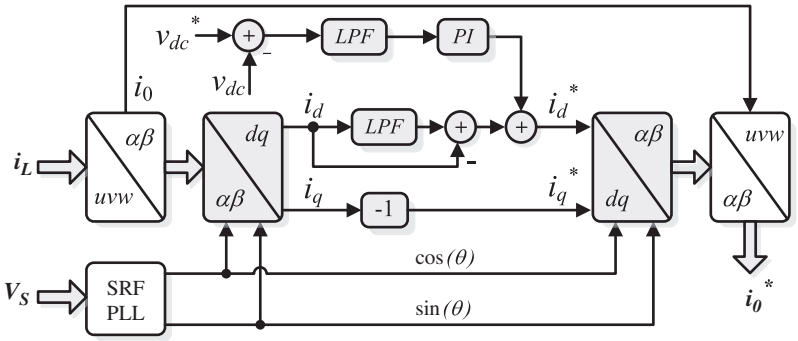


FIG. 41.67 A *dq*-based current reference generator block diagram.

41.5.3 DC Voltage Control

The dc voltage converter is controlled with a traditional PI controller. This is an important issue in the evaluation, since the cost function (41.71) is designed using only current references, in order to avoid the use of weighting factors. Generally, these weighting factors are obtained experimentally, and they are not well defined when different operating conditions are required. Additionally, the slow dynamic response of the voltage across the electrolytic capacitor does not affect the current transient response. For this reason, the PI controller represents a simple and effective alternative for the dc voltage control.

The dc voltage remains constant (with a minimum value of $\sqrt{6}v_{s(rms)}$) until the active power absorbed by the converter decreases to a level where it is unable to compensate for its losses. The active power absorbed by the converter is controlled by adjusting the amplitude of the active power reference signal i_e, which is in phase with each phase voltage. The equivalent closed-loop transfer function of the given system with a PI controller is

$$\frac{v_{dc}}{i_e} = \frac{\frac{\omega_n^2}{a}(s+a)}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{41.73}$$

Since the time response of the dc voltage control loop does not need to be fast, a damping factor $\zeta = 1$ and a natural angular speed $\omega_n = 2\pi 100$ rad/s are used to obtain a critically damped response with minimal voltage oscillation. The corresponding integral time $T_i = 1/a$ and proportional gain K_p can be calculated as

$$\zeta = \sqrt{\frac{3}{8}\frac{K_P v_s \sqrt{2} T_i}{C_{dc} v_{dc}^*}} \tag{41.74}$$

$$\omega_n = \sqrt{\frac{3}{2}\frac{K_P v_s \sqrt{2}}{C_{dc} v_{dc}^* T_i}} \tag{41.75}$$

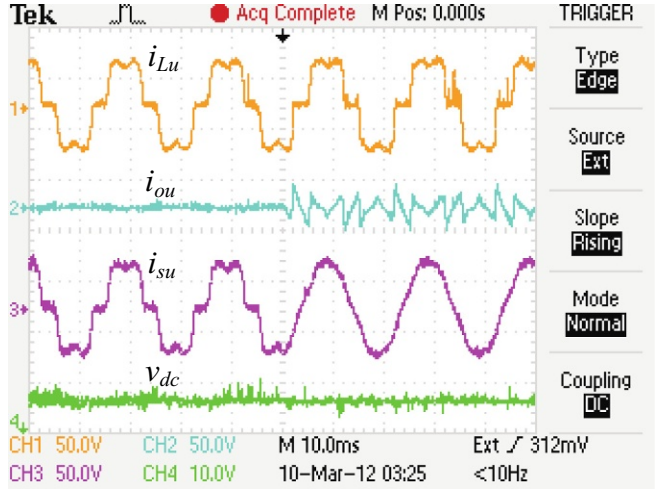
41.5.4 Performance Evaluation

The compensation effectiveness of the active power filter is corroborated in a 2 kVA experimental setup. In order to verify the effectiveness of the current harmonic compensation, a six-pulse rectifier was selected as a nonlinear load. A step load change was applied to evaluate the transient response of the dc voltage loop. Finally, an unbalanced load was used to validate the performance of the neutral current compensation. The proposed predictive control algorithm was programmed using an S-function block that allows simulation of a discrete model that can be easily implemented in a real-time interface (RTI) on the dSPACE DS1103 R&D control board. The complete control loop is executed by the controller every 20 μs, while the selected switching state is available at 16 μs. An average switching frequency of 4.64 kHz is obtained.

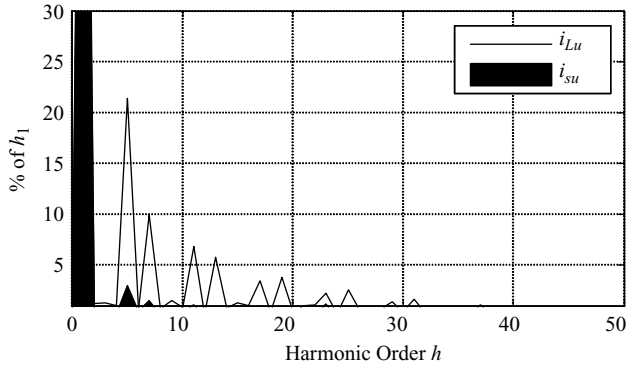
Fig. 41.68 shows the transient response of the compensation scheme. Fig. 41.68A shows that the line current becomes sinusoidal when the active power filter starts compensating and the dc voltage behaves as expected. Fig. 41.68B indicates that the total harmonic distortion of the line current (THDi) is reduced from 27.1% to 4.5%. This is a consequence of the good tracking characteristic of the current references, as shown in Fig. 41.68D.

In Fig. 41.69, the transient response of the active power filter under a step load change is shown. In this case, a step load change is applied from 0.6 to 1.0 p.u. The line currents remain sinusoidal, and the dc voltage returns to its reference with a typical transient response of an underdamped second-order system (maximum overshoot of 5% and two grid cycles of settling time).

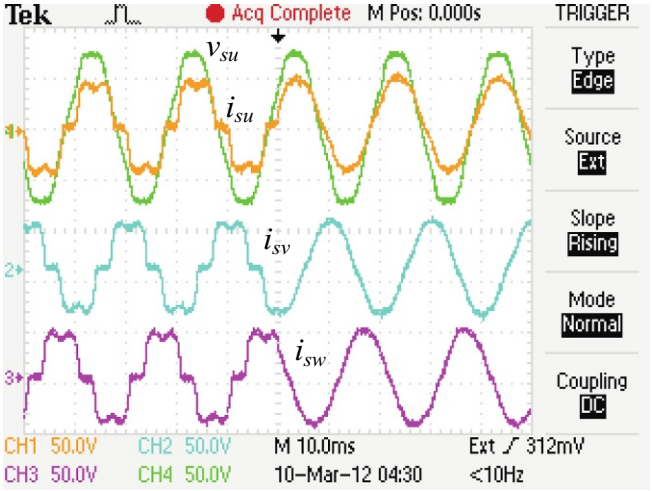
Finally, the load connected to phase u was increased from 1.0 to 1.3 p.u. The corresponding waveforms are shown in Fig. 41.70. Fig. 41.70A shows that the active filter is capable of compensating the current in the neutral conductor with a fast transient response. Moreover, Fig. 41.70B shows that the system neutral current ion is effectively compensated and eliminated and system currents remain balanced even if an 11% current imbalance is applied.



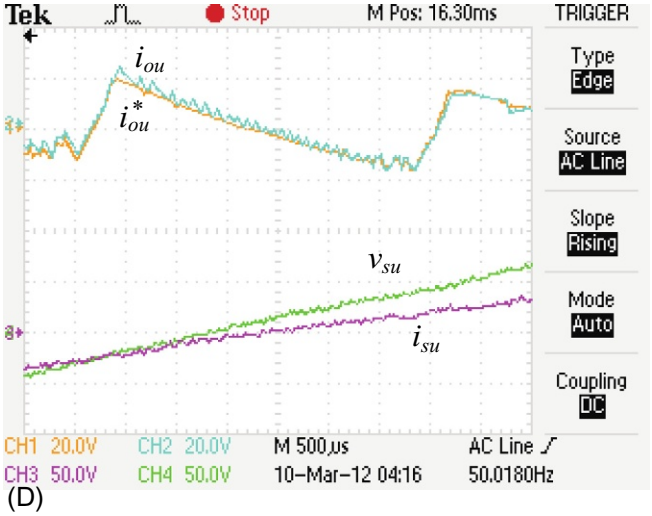
(A)



(B)



(C)



(D)

FIG. 41.68 Experimental waveforms of transient response after the connection of the APF. (A) Load current i_{Lu}, active power filter current i_{ou}, dc voltage converter v_{dc}, and system current i_{su}. (B) Frequency spectrum of the load and system currents. (C) System voltage and currents, v_{su} and i_{su}, i_{sv}, and i_{sw}. (D) Detailed view of the tracking characteristic of the APF current i_{ou}.

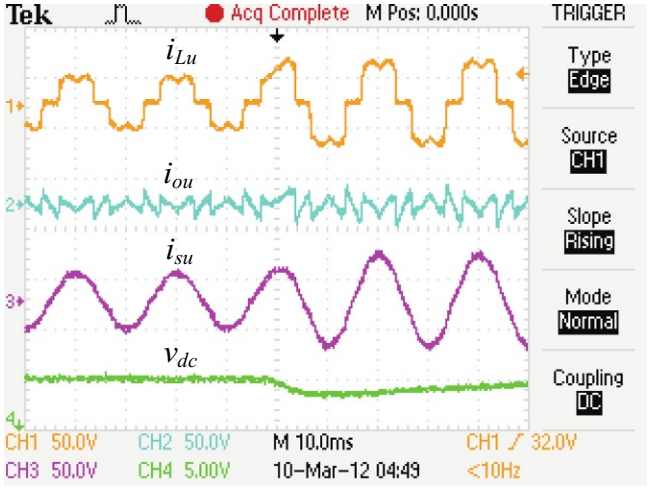


FIG. 41.69 Experimental results for step load change (0.6–1.0 p.u.). Load current i_{Lu}, active power filter current i_{ou}, system current i_{su}, and dc voltage converter v_{dc}.

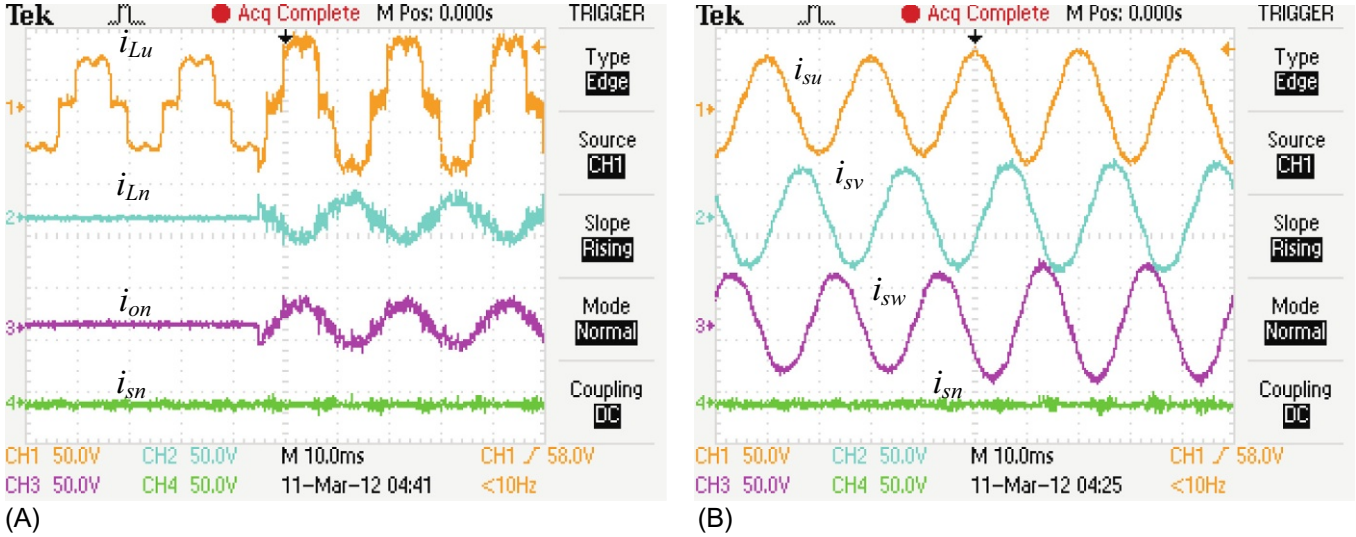


FIG. 41.70 Experimental results for step unbalanced phase u load change (1.0–1.3 p.u.). (A) Load current i_{Lu}, load neutral current i_{Ln}, active power filter neutral current i_{on}, and system neutral current i_{sn}. (B) System currents i_{su}, i_{sv}, i_{sw}, and i_{sn}.

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References

[1] H. Akagi, Y. Kanazawa, A. Nabae, Instantaneous reactive power compensators comprising switching devices without energy storage components, IEEE Trans. Ind. Appl. IA-20 (3) (1984) 625–630.

[2] S. Bhattacharya, D. Divan, Design and implementation of a hybrid series active filter system, in: Power Electronics Specialists Conference, 1995. PESC '95 Record., 26th Annual IEEE, vol. 1, 1995, pp. 189–195. vol. 1.

[3] J. Dixon, S. Tepper, L. Moran, Practical evaluation of different modulation techniques for current-controlled voltage source inverters, IEE Proc. Electr. Power Appl. 143 (4) (1996) 301–306.

[4] A. Nabae, S. Ogasawara, H. Akagi, A novel control scheme for current-controlled PWM inverters, IEEE Trans. Ind. Appl. IA-22 (4) (1986) 697–701.

[5] F.Z. Peng, H. Akagi, A. Nabae, A new approach to harmonic compensation in power systems-a combined system of shunt passive and series active filters, IEEE Trans. Ind. Appl. 26 (6) (1990) 983–990.

[6] F.Z. Peng, H. Akagi, A. Nabae, Compensation characteristics of the combined system of shunt passive and series active filters, IEEE Trans. Ind. Appl. 29 (1) (1993) 144–152.

[7] T. Tanaka, K. Wada, H. Akagi, A new control scheme of series active filters, in: Presented at the IPEC, 1995, pp. 376–381.

[8] L.A. Moran, I. Pastorini, J. Dixon, R. Wallace, A fault protection scheme for series active power filters, IEEE Trans. Power Electron. 14 (5) (1999) 928–938.

[9] H. Fujita, T. Yamasaki, H. Akagi, A hybrid active filter for damping of harmonic resonance in industrial power systems, IEEE Trans. Power Electron. 15 (2) (2000) 215–222.

[10] S. Fukuda, T. Endoh, Control method for a combined active filter system employing a current source converter and a high pass filter, IEEE Trans. Ind. Appl. 31 (3) (1995) 590–597.

Further Reading

[1] Z.X. Zou, K. Zhou, Z. Wang, M. Cheng, Frequency-adaptive fractional-order repetitive control of shunt active power filters, IEEE Trans. Ind. Electron. 62 (3) (2015) 1659–1668.

[2] T.L. Lee, Y.C. Wang, J.C. Li, J.M. Guerrero, Hybrid active filter with variable conductance for harmonic resonance suppression in industrial power systems, IEEE Trans. Ind. Electron. 62 (2) (2015) 746–756.

[3] P. Kanjiya, V. Khadkikar, H.H. Zeineldin, Optimal control of shunt active power filter to meet IEEE Std. 519 current harmonic constraints under nonideal supply condition, IEEE Trans. Ind. Electron. 62 (2) (2015) 724–734.

[4] D. Das, R.P. Kandula, J.A. Muñoz, D. Divan, R.G. Harley, J. E. Schatz, An Integrated controllable network transformer-hybrid active filter system, IEEE Trans. Ind. Appl. 51 (2) (2015) 1692–1701.

[5] P. Acuña, L. Morán, M. Rivera, R. Aguilera, R. Burgos, V. G. Agelidis, A single-objective predictive control method for a multivariable single-phase three-level NPC converter-based active power filter, IEEE Trans. Ind. Electron. 62 (7) (2015) 4598–4607.

[6] W.R.N. Santos, et al., The transformerless single-phase universal active power filter for harmonic and reactive power compensation, IEEE Trans. Power Electron. 29 (7) (2014) 3563–3572.

[7] S. Rahmani, A. Hamadi, K. Al-Haddad, L.A. Dessaint, A combination of shunt hybrid power filter and thyristor-controlled reactor for power quality, IEEE Trans. Ind. Electron. 61 (5) (2014) 2152–2164.

[8] P. Acuña, L. Morán, M. Rivera, J. Dixon, J. Rodriguez, Improved active power filter performance for renewable power generation systems, IEEE Trans. Power Electron. 29 (2) (2014) 687–694.

[9] Q.N. Trinh, H.H. Lee, An advanced current control strategy for three-phase shunt active power filters, IEEE Trans. Ind. Electron. 60 (12) (2013) 5400–5410.
[10] J.E. Hernandez, R.P. Kandula, F.C. Lambert, D. Divan, A practical directional third harmonic hybrid active filter for medium-voltage utility applications, IEEE Trans. Ind. Appl. 49 (6) (2013) 2674–2683.
[11] M. Angulo, D.A. Ruiz-Caballero, J. Lago, M.L. Heldwein, S. A. Mussa, Active power filter control strategy with implicit closed-loop current control and resonant controller, IEEE Trans. Ind. Electron. 60 (7) (2013) 2721–2730.
[12] J. Liu, P. Zanchetta, M. Degano, E. Lavopa, Control design and implementation for high performance shunt active filters in aircraft power grids, IEEE Trans. Ind. Electron. 59 (9) (2012) 3604–3613.
[13] C.S. Lam, W.H. Choi, M.C. Wong, Y.D. Han, Adaptive DC-link voltage-controlled hybrid active power filters for reactive power compensation, IEEE Trans. Power Electron. 27 (4) (2012) 1758–1772.
[14] A. Bhattacharya, C. Chakraborty, S. Bhattacharya, Parallel-connected shunt hybrid active power filters operating at different switching frequencies for improved performance, IEEE Trans. Ind. Electron. 59 (11) (2012) 4007–4019.
[15] H. Akagi, K. Isozaki, A hybrid active filter for a three-phase 12-pulse diode rectifier used as the front end of a medium-voltage motor drive, IEEE Trans. Power Electron. 27 (1) (2012) 69–77.
[16] P. Acuña, L. Moran, J. Dixon, Current harmonics compensation for electrolytic processes using a series active scheme, IET Power Electron. 5 (8) (2012) 1254–1261.
[17] E.C. dos Santos, C.B. Jacobina, J.A.A. Dias, N. Rocha, Single-phase to three-phase universal active power filter, IEEE Trans. Power Deliv. 26 (3) (2011) 1361–1371.
[18] A. Bhattacharya, C. Chakraborty, A shunt active power filter with enhanced performance using ANN-based predictive and adaptive controllers, IEEE Trans. Ind. Electron. 58 (2) (2011) 421–428.
[19] A. Varschavsky, J. Dixon, M. Rotella, L. Moran, Cascaded nine-level inverter for hybrid-series active power filter, using industrial controller, IEEE Trans. Ind. Electron. 57 (8) (2010) 2761–2767.
[20] A. Prasai, J. Sastry, D.M. Divan, Dynamic capacitor (D-CAP): an integrated approach to reactive and harmonic compensation, IEEE Trans. Ind. Appl. 46 (6) (2010) 2518–2525.
[21] J.M. Maza-Ortega, J.A. Rosendo-Macias, A. Gomez-Exposito, S. Ceballos-Mannozzi, M. Barragan-Villarejo, Reference current computation for active power filters by running DFT techniques, IEEE Trans. Power Deliv. 25 (3) (2010) 1986–1995.
[22] H. Akagi, R. Kondo, A transformerless hybrid active filter using a three-level pulsewidth modulation (PWM) converter for a medium-voltage motor drive, IEEE Trans. Power Electron. 25 (6) (2010) 1365–1374.
[23] A. Luo, Z. Shuai, Z.J. Shen, W. Zhu, X. Xu, Design considerations for maintaining DC-side voltage of hybrid active power filter with injection circuit, IEEE Trans. Power Electron. 24 (1) (2009) 75–84.
[24] P. Flores, J. Dixon, M. Ortuzar, R. Carmi, P. Barriuso, L. Moran, Static var compensator and active power filter with power injection capability, using 27-level inverters and photovoltaic cells, IEEE Trans. Ind. Electron. 56 (1) (2009) 130–138.
[25] V.F. Corasaniti, M.B. Barbieri, P.L. Arnera, M.I. Valla, Hybrid active filter for reactive and harmonics compensation in a distribution network, IEEE Trans. Ind. Electron. 56 (3) (2009) 670–677.
[26] M. Aredes, H. Akagi, E.H. Watanabe, E.V. Salgado, L. F. EncarnaÇÃo, Comparisons between the p–q and p–q–r theories in three-phase four-wire systems, IEEE Trans. Power Electron. 24 (4) (2009) 924–933.
[27] H. Akagi, T. Hatada, Voltage balancing control for a three-level diode-clamped converter in a medium-voltage transformerless hybrid active filter, IEEE Trans. Power Electron. 24 (3) (2009) 571–579.
[28] G. Superti-Furga, G. Todeschini, Discussion on instantaneous p #x2013; q strategies for control of active filters, IEEE Trans. Power Electron. 23 (4) (2008) 1945–1955.
[29] H.A. Ramos-Carranza, A. Medina, G.W. Chang, Real-time shunt active power filter compensation, IEEE Trans. Power Deliv. 23 (4) (2008) 2623–2625.
[30] J. Mahomar, L. Moran, J. Guzman, J. Dixon, A new mathematic algorithm to analyze power distribution systems with active compensation and nonlinear loads, IEEE Trans. Power Deliv. 23 (4) (2008) 2535–2544.
[31] T.L. Lee, P.T. Cheng, H. Akagi, H. Fujita, A dynamic tuning method for distributed active filter systems, IEEE Trans. Ind. Appl. 44 (2) (2008) 612–623.
[32] R.S. Herrera, P. SalmerÓn, H. Kim, Instantaneous reactive power theory applied to active power filter compensation: different approaches, assessment, and experimental results, IEEE Trans. Ind. Electron. 55 (1) (2008) 184–196.
[33] B.S. Chen, G. JoÓs, Direct power control of active filters with averaged switching frequency regulation, IEEE Trans. Power Electron. 23 (6) (2008) 2729–2737.
[34] M.T. Bina, A.K.S. Bhat, Averaging technique for the modeling of STATCOM and active filters, IEEE Trans. Power Electron. 23 (2) (2008) 723–734.
[35] L. Asiminoaei, F. Blaabjerg, S. Hansen, P. ThØgersen, Adaptive compensation of reactive power with shunt active power filters, IEEE Trans. Ind. Appl. 44 (3) (2008) 867–877.
[36] L. Asiminoaei, E. Aeloiza, P.N. Enjeti, F. Blaabjerg, Shunt active-power-filter topology based on parallel interleaved inverters, IEEE Trans. Ind. Electron. 55 (3) (2008) 1175–1189.
[37] W. Tangtheerajaroonwong, T. Hatada, K. Wada, H. Akagi, Design and performance of a transformerless shunt hybrid filter integrated into a three-phase diode rectifier, IEEE Trans. Power Electron. 22 (5) (2007) 1882–1889.
[38] B.N. Singh, B. Singh, A. Chandra, P. Rastgoufard, K. Al-Haddad, An improved control algorithm for active filters, IEEE Trans. Power Deliv. 22 (2) (2007) 1009–1020.
[39] M.I.M. Montero, E.R. Cadaval, F.B. Gonzalez, Comparison of control strategies for shunt active power filters in three-phase four-wire systems, IEEE Trans. Power Electron. 22 (1) (2007) 229–236.
[40] R.S. Herrera, P. Salmeron, Instantaneous reactive power theory: a comparative evaluation of different formulations, IEEE Trans. Power Deliv. 22 (1) (2007) 595–604.
[41] S.A. Gonzalez, R. Garcia-Retegui, M. Benedetti, Harmonic computation technique suitable for active power filters, IEEE Trans. Ind. Electron. 54 (5) (2007) 2791–2796.
[42] H. Fujita, H. Akagi, Voltage-regulation performance of a shunt active filter intended for installation on a power distribution system, IEEE Trans. Power Electron. 22 (3) (2007) 1046–1053.
[43] L. Asiminoaei, C. Lascu, F. Blaabjerg, I. Boldea, Performance improvement of shunt active power filter with dual parallel topology, IEEE Trans. Power Electron. 22 (1) (2007) 247–259.
[44] B. Singh, V. Verma, An indirect current control of hybrid power filter for varying loads, IEEE Trans. Power Deliv. 21 (1) (2006) 178–184.

[45] M.E. Ortuzar, R.E. Carmi, J.W. Dixon, L. Moran, Voltage-source active power filter based on multilevel converter and ultracapacitor DC link, IEEE Trans. Ind. Electron. 53 (2) (2006) 477–485.
[46] B.R. Lin, C.H. Huang, Implementation of a three-phase capacitor-clamped active power filter under unbalanced condition, IEEE Trans. Ind. Electron. 53 (5) (2006) 1621–1630.
[47] P.T. Cheng, T.L. Lee, Distributed active filter systems (DAFSs): a new approach to power system harmonics, IEEE Trans. Ind. Appl. 42 (5) (2006) 1301–1309.
[48] S. Kim, P.N. Enjeti, A new hybrid active power filter (APF) topology, IEEE Trans. Power Electron. 17 (1) (2002) 48–54.
[49] B. Singh, K. Al-Haddad, A. Chandra, A review of active filters for power quality improvement, IEEE Trans. Ind. Electron. 46 (5) (1999) 960–971.
[50] T. Thomas, K. Haddad, G. Joos, A. Jaafari, Design and performance of active power filters, IEEE Ind. Appl. Mag. 4 (5) (1998) 38–46.
[51] S. Bhattacharya, T.M. Frank, D.M. Divan, B. Banerjee, Active filter system implementation, IEEE Ind. Appl. Mag. 4 (5) (1998) 47–63.
[52] H. Akagi, Control strategy and site selection of a shunt active filter for damping of harmonic propagation in power distribution systems, IEEE Trans. Power Deliv. 12 (1) (1997) 354–363.
[53] H. Fujita, S. Tominaga, H. Akagi, Analysis and design of a DC voltage-controlled static VAr compensator using quad-series voltage-source inverters, IEEE Trans. Ind. Appl. 32 (4) (1996) 970–978.
[54] V.B. Bhavaraju, P.N. Enjeti, An active line conditioner to balance voltages in a three-phase system, IEEE Trans. Ind. Appl. 32 (2) (1996) 287–292.
[55] T. Tanaka, H. Akagi, A new method of harmonic power detection based on the instantaneous active power in three-phase circuits, IEEE Trans. Power Deliv. 10 (4) (1995) 1737–1742.
[56] L.A. Moran, J.W. Dixon, R.R. Wallace, A three-phase active power filter operating with fixed switching frequency for reactive power and current harmonic compensation, IEEE Trans. Ind. Electron. 42 (4) (1995) 402–408.
[57] M. Aredes, E.H. Watanabe, New control algorithms for series and shunt three-phase four-wire active power filters, IEEE Trans. Power Deliv. 10 (3) (1995) 1649–1656.
[58] A. Campos, G. Joos, P.D. Ziogas, J.F. Lindsay, Analysis and design of a series voltage unbalance compensator based on a three-phase VSI operating with unbalanced switching functions, IEEE Trans. Power Electron. 9 (3) (1994) 269–274.
[59] H. Akagi, Trends in active power line conditioners, IEEE Trans. Power Electron. 9 (3) (1994) 263–268.
[60] E.H. Watanabe, R.M. Stephan, M. Aredes, New concepts of instantaneous active and reactive powers in electrical systems with generic loads, IEEE Trans. Power Deliv. 8 (2) (1993) 697–703.
[61] L. Moran, P.D. Ziogas, G. Joos, A solid-state high-performance reactive-power compensator, IEEE Trans. Ind. Appl. 29 (5) (1993) 969–978.

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42

EMI Effects of Power Converters

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42.1 Introduction

The term "electromagnetic interference" (EMI) refers to the disturbance in operation of an engineering system due to an electromagnetic impact of the same system or other systems. Conducted electric noise and radiated electromagnetic noise are typical culprits. Watching TV during work hours in industrial centers of Western Europe in the late 1960s was virtually impossible, due to operation of large dc drives and inadequate efforts to fight the EMI threat. Today, proliferation of power electronic converters and communication devices makes EMI mitigation as important as ever, because of the high and growing number of both the potential perpetrators and victims of EMI. To ensure electromagnetic compatibility (EMC), various EMI norms have been established. The issue of EMI is closely linked to that of susceptibility of an electronic circuit to external disturbances. Considering a multicircuit system, if each constituent circuit does not emit above-limit EMI and is immune to below-limit EMI, then each circuit is electromagnetically compatible with the system.

The institution historically entrusted with development of international EMC standards is Comité International Special des Perturbations Radioelectriques (CISPR), founded in 1933, and now forming part of International Electrotechnical Commission (IEC). Drawing on CISPR expertise, numerous other international and national organizations issue norms pertaining to various aspects of EMC. Specific EMI limits are set for internal use by individual countries and organizations, such as armed forces or large corporations. Manufacturers of electric apparatus and systems must comply with the EMC standards to have an access to the market.

In this chapter, EMI effects of power electronic converters are illustrated, and basic terms and units are introduced. EMI measurement techniques and preventive measures are described, and EMC standardization efforts are examined.

42.2 Power Converters as Sources of EMI

The switch-mode operation of power electronic converters results in rippled currents. Also, rapid changes of the switched voltages induce currents in parasitic (stray) capacitances that couple the converter with other closely spaced circuits. Distorted currents drawn from the power grid produce distorted voltage drops generating pervasive voltage noise. In general, the voltage disturbances can be divided into three classes: (1) noise, (2) short-duration impulses superimposed on the mains voltage, and (3) transients.

Electromagnetic disturbances travel by conduction on wiring (conducted EMI), radiation in space (radiated EMI), and intercircuit capacitive or inductive coupling. Below 10 MHz, the EMI spreads mainly by conduction, whereas at higher frequencies mostly by radiation. The frequency range of 0.15–30 MHz occupies an important place in EMC norms because it covers the radio and TV broadcast. According to those norms, in that range, it is the conducted EMI that must be measured and suppressed, whereas measurements of the radiated EMI are required only under special circumstances. Power electronic equipment typically produces EMI that is broadband and contained within a frequency range from the operating frequency to several megahertz. Recently, the very

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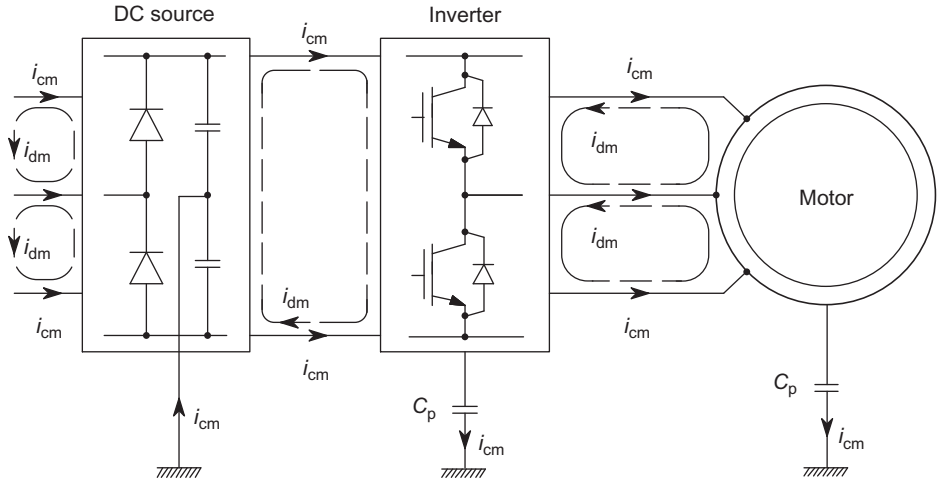


FIG. 42.1 AC drive system with PWM voltage-source inverter.

low-frequency range of 10–150 kHz has been receiving an increased attention. Consequently, with respect to most power electronic converters, it is the conducted EMI that is considered a major nuisance.

Conducted EMI appears in the form of common-mode (CM) and differential-mode (DM) voltages and currents. These two modes are illustrated in Fig. 42.1, which depicts an adjustable-speed ac drive with a PWM voltage-source inverter. CM currents, i_{cm}, flow to the ground through parasitic capacitances, C_p, whereas DM currents, i_{dm}, flow only in the wires of the system. Considering the two-wire dc line supplying the inverter, the rms CM voltage, $V_{cm(2)}$, is defined as

$$V_{cm(2)} = \frac{V_1 + V_2}{2} \tag{42.1}$$

and the rms DM voltage, $V_{dm(2)}$, as

$$V_{dm(2)} = V_1 - V_2 \tag{42.2}$$

where V_1 and V_2 are line-to-ground voltages of the two wires. The rms CM and DM currents, $I_{cm(2)}$ and $I_{dm(2)}$, are defined as

$$I_{cm(2)} = I_1 + I_2 \tag{42.3}$$

$$I_{dm(2)} = \frac{I_1 - I_2}{2} \tag{42.4}$$

For the three-wire supply and load ac lines, the rms CM voltage, $V_{cm(3)}$, and current, $I_{cm(3)}$, are defined as

$$V_{cm(3)} = \frac{V_1 + V_2 + V_3}{3} \tag{42.5}$$

$$I_{cm(3)} = I_1 + I_2 + I_3 \tag{42.6}$$

where subscript "3" applies to the third wire. The DM voltage and current, if measured with respect to ac wires 1 and 2, are defined by Eqs. (42.2) and (42.4) as for the two-wire system.

To illustrate EMI generation by PWM power converters, a typical waveform of output current of the inverter in Fig. 42.1 is shown in Fig. 42.2. The fundamental sine wave dominates, but the high-frequency current ripple is also observable. As seen in Fig. 42.3, numerous clusters of higher harmonics appear in the frequency spectrum of the current. Their locations coincide with multiples of the switching frequency (here 2 kHz), which, as in all PWM converters, is much higher than the fundamental frequency (here 9 Hz) of the ac output (or input) voltage.

The range of frequency in Fig. 42.3 is narrow (24 kHz). A wide-range frequency spectrum of current of another inverter is shown in Fig. 42.4. It can be seen that the harmonics become progressively less prominent when the frequency increases. This observation justifies the already mentioned focus on the frequencies below 30 MHz.

The fast ON-OFF and OFF-ON state transition of switches, whose switching times are typically in the order of a fraction of microsecond, also causes EMI. It is due to the high dv/dt ratios, which generate transient charge currents in the inter-wire capacitances of cables, intrawinding capacitances of transformers and p-n junctions of power diodes. Transient circuit-to-ground currents through parasitic capacitances also produce EMI. If not filtered out, the transients appear in current waveforms as spikes on top of the fundamental sinusoid. The circuit-to-ground current spikes constitute CM emissions, whereas the ripple current and periodic current spikes, coincident with the switching pattern of the converter, comprise DM emissions.

Power electronic converters tend to generate current-related interference at their input, injecting noise to the power grid, and voltage-related interference at their outputs. It may disturb operation of communication and control systems in proximity to the converter. Considering the popular low-power dc-to-dc converters, the flyback and buck converters produce particularly noisy input currents because the semiconductor switch

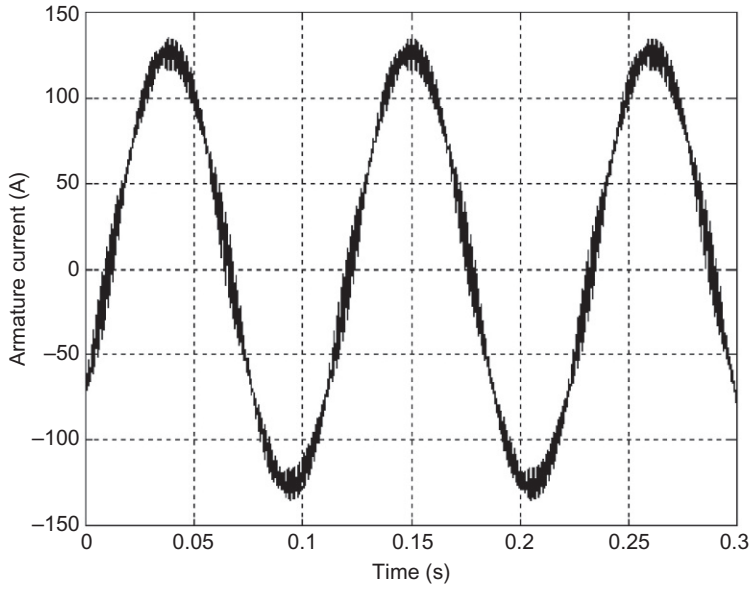


FIG. 42.2 Waveform of output current of PWM voltage-source inverter.

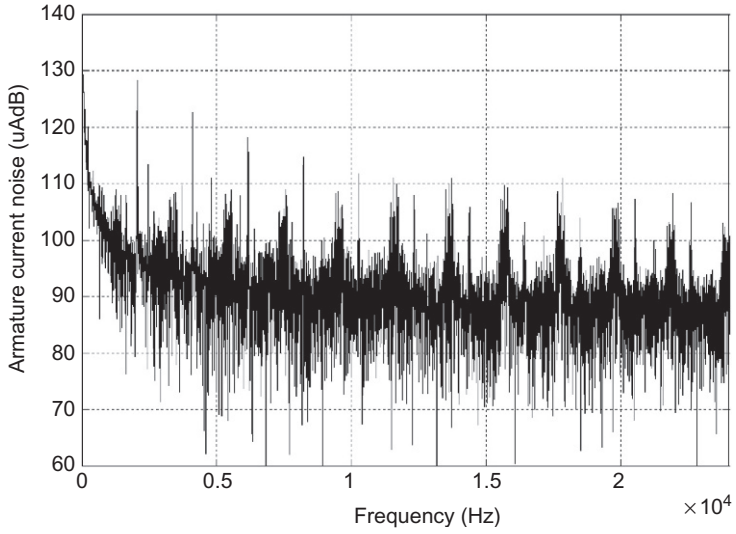


FIG. 42.3 Frequency spectrum of current in Fig. 42.2.

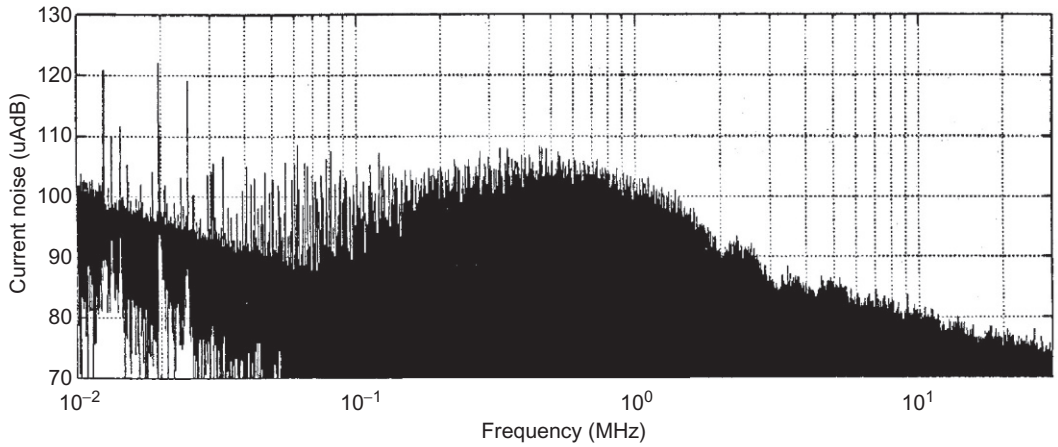


FIG. 42.4 Wide-range frequency spectrum of inverter current.

is directly in series with the input power line. In conjunction with the finite source impedance, the EMI from dc-to-dc converters conducted by the line can cause disturbance of operation of system operating from a common power bus. Disturbances can also be caused by emissions radiated from converters with very high switching frequencies. The radiated EMI is most often a magnetic field, due to the typically low voltages and high currents involved, but electric fields can sometimes also be a nuisance, especially with respect to the own control circuitry of the converter. Power lines can also radiate EMI produced by the current noise drawn from converters.

42.3 Measurements of Conducted EMI

Mitigation of conducted EMI is of major practical importance in power electronic systems. Therefore, the topic of EMI measurements in this chapter is limited to the 10 kHz–30 MHz frequency range. The related terms, units, instruments, and techniques are subsequently described. Concerning the radiated interference, the reader is referred to one of many publications covering the radio-frequency (RF) aspects of EMC, for example [1–5].

The basic quantity of a signal is power. Because of the potentially wide magnitude ranges involved, the decibel (dB) system is often used in which 1 W serves as the reference. In the dB system, signal power, $P_{(\mathrm{dBW})}$, expressed in dBW, is calculated from the power in watts, $P_{(\mathrm{W})}$, as

$$P_{(\mathrm{dBW})} = 10\log P_{(\mathrm{W})}\,\mathrm{dBW} \tag{42.7}$$

If milliwatts, mW, often abbreviated as "m," is considered; then

$$P_{(\mathrm{dBm})} = P_{(\mathrm{dBW})} + 30\,\mathrm{dBm} \tag{42.8}$$

However, in EMI measurements, it is voltage that is commonly used, and voltage probes are employed. Power is proportional to the square of voltage. Thus, taking 1 V as reference, voltage in the logarithmic scale, $V_{(\mathrm{dbV})}$, is defined as

$$V_{(\mathrm{dBV})} = 20\log V_{(\mathrm{V})}\,\mathrm{dBV} \tag{42.9}$$

In practice, the reference voltage is usually 1 μV, and

$$V_{(\mathrm{dB}\mu\mathrm{V})} = 20\log V_{(\mu\mathrm{V})}\,\mathrm{dB}\mu\mathrm{V} = V_{(\mathrm{dBV})} + 120\,\mathrm{dB}\mu\mathrm{V} \tag{42.10}$$

If the commonly used resistance of 50 Ω is employed in the measurements, conversions of $P_{(\mathrm{dBm})}$ into $V_{(\mathrm{dB}\mu\mathrm{V})}$ and vice versa can be made from the equation:

$$V_{(\mathrm{dB}\mu\mathrm{V})} + P_{(\mathrm{dBm})} = 107 \tag{42.11}$$

Current probes for EMI measurements are used when limits on conducted EMI are expressed in units of current. Denoting the terminal-pair transfer impedance of a current probe by Z_{T}, current expressed in dBμA, is given by

$$I_{(\mathrm{dB}\mu\mathrm{A})} = V_{(\mathrm{dB}\mu\mathrm{V})} - Z_{\mathrm{T}(\mathrm{dB}\Omega)} \tag{42.12}$$

where

$$Z_{(\mathrm{dB}\Omega)} = 20\log Z_{(\Omega)}\,\mathrm{dB}\Omega \tag{42.13}$$

To characterize broadband coherent (continuous spectrum) signals, an amplitude density function, A, is used in place of a discrete amplitude measure. The so-called broadband unit is 1 V/Hz. In EMC techniques, the 1 μV/MHz unit is more convenient. The conversion equations are

$$A_{(\mathrm{dB}\mu\mathrm{V/MHz})} - A_{(\mathrm{dBV/Hz})} = 240 \tag{42.14}$$

and

$$V_{(\mathrm{dB}\mu\mathrm{V})} - A_{(\mathrm{dB}\mu\mathrm{V/MHz})} = 20\log B_{(\mathrm{MHz})} \tag{42.15}$$

where $B_{(\mathrm{MHz})}$ is the measurement bandwidth, usually 9 kHz, that is, 0.009 MHz.

Conducted emissions are measured using EMI receivers, which usually measure voltage from an appropriate probe. Basically, the EMI receiver is a tunable voltmeter; its block diagram is shown in Fig. 42.5. Modern EMI receivers cover extremely wide frequency ranges, for example, from 9 kHz to 18 GHz.

To allow comparison of EMI measurement results, precise specifications for the detector have been established. The most common types are peak, quasi-peak, and average detectors. They are based on RC circuits having different charging and discharging time constants. It must be mentioned that the displays are usually calibrated to the rms value of an equivalent sinusoidal signal, whereas the actual detector often measures a different characteristic of the culprit noise.

Measurement of the peak EMI is important because of the ubiquity of impulsive sources and sensitivity of many types

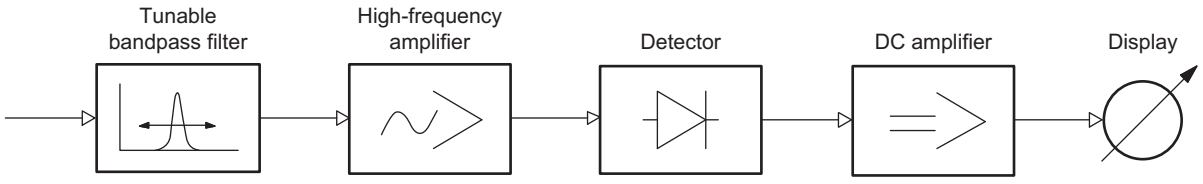


FIG. 42.5 Block diagram of EMI receiver.

of electronic circuits to impulses. The peak detectors have a short charging time constant, in the order of a fraction of microsecond, and a very long discharging time constant, in the order of tens of seconds. The quasi-peak detectors, strongly recommended by CISPR, have been primarily developed to emulate the human ear acting as a broadcast disturbance sensor. The charging and discharging time constants are 1 and 160 ms, respectively. The average detector is characterized by a long integration time constant, in the order of a second. For the 0.15–30 MHz frequency range, CISPR requires that an EMI measuring instrument have a 9 kHz bandwidth of the filter at 6 dB (from −5 to +4 kHz from the central frequency value) and that the measurement accuracy for a sinusoidal signal be less than 2 dB.

To increase the accuracy within wide ranges of the frequency and magnitude of signals, modern EMI receivers have several measuring channels. Each channel contains an independent quasi-peak detector, and the saturation and threshold levels of individual channels differ from each other. Output signals of the detectors are added in a circuit operating the display.

For comparability of EMI measurements, an interface circuit is inserted between the EMI source and the mains. This circuit is called a line impedance stabilization network (LISN) or artificial mains. The LISN produces a standard load impedance for the EMI source and filters out high-frequency disturbances on the mains, which could distort measurement results. An example of single-phase LISN recommended by CISPR 16—a publication devoted to proper EMI testing—is shown in Fig. 42.6. In the equipment under test (EUT) block, the positive and negative line terminals are denoted by P and N, respectively, whereas grounded terminal is denoted by G. The load resistance, R_L, specified by CISPR 16 is 50 Ω. The switch, S, allows transition from the CM to DM measurements. Three-phase LISNs are also available. Refer to the manual of a given LISN for operating instructions.

For quick qualitative EMI measurements, for example, when developing an EMI filter, a spectrum analyzer can be employed. A direct view of the interference levels over a wide frequency range is very convenient. The frequency axis can be switched to a linear or logarithmic scale, whereas the magnitude is usually displayed in dBm. True peak and average detectors are available. Spectrum analyzers are rms calibrated, so that the reading is correct for sinusoidal waveforms only, such as discrete harmonics of the measured noise. For impulse disturbances, correct peak values are obtained. For broadband measurements, corrections must be made to convert the true peak to quasi-peak and to account for the difference in measurement bandwidths. For help, refer to the manual of a given spectrum analyzer.

Technical details of EMI measurements for EMC compliance are too vast, a topic to be fully covered here. The reader is referred to such authoritative sources as the already mentioned CISPR publication 16 and books [1–6].

42.4 EMI Filters

EMI generated in power electronic systems usually exceeds the allowable levels, so it must be reduced. The most common means of EMI mitigation are low-pass filters, often called radio-frequency (RF) filters. They are installed on the input and output sides of power converters. The filters are simple capacitive (C) or inductive-capacitive (LC) circuits. Resistors are sometimes added to dampen possible resonances caused by converters with high switching frequencies.

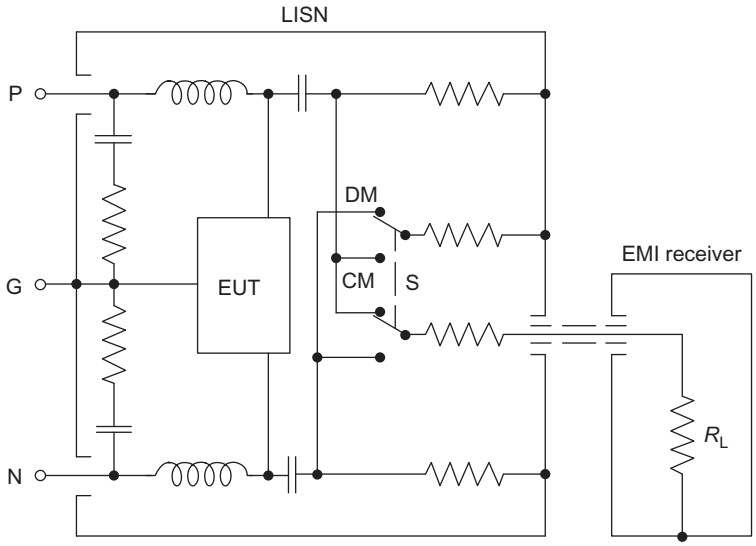


FIG. 42.6 Simplified circuit diagram of a LISN.

Choke coils are employed as the inductive components of the filters. They are usually single-layer solenoid structures with relatively low coefficients of inductance. In the case of CM EMI filters, two or three windings are placed on the same closed iron core. The windings are so arranged that the coil impedance for the CM noise is high, but that for the load current and DM noise is low. A single-phase CM choke coil is shown in Fig. 42.7. Again, letters P, N, and G denote the positive, negative, and ground terminals of the mains. It can be seen that magnetomotive forces $\mathcal{F}_L$ and $\mathcal{F}_{dm}$ produced by the load current i_L and DM noise current i_{dm} in the upper and lower parts of the coil cancel each other. As a result, the magnetic flux Φ_{cm12} in the core is generated only by magnetomotive forces $\mathcal{F}_{cm1}$ and $\mathcal{F}_{cm2}$ produced by the CM noise currents i_{cm1} and i_{cm2}.

Capacitors employed in EMI filters must have low parasitic series inductance, low dielectric and ohmic losses, and stable capacitance versus frequency characteristics. Paper, metalized paper, polystyrene, and ceramic capacitors are widely used. The so-called multifunction ceramic (MFC) capacitors can suppress the high-frequency noise and absorb impulse-type transients. According to their electric connection mode, capacitors in power line filters can be classified as X and Y capacitors, the former posing no threat of electric shock to personnel, even in the case of a breakdown. Y capacitors are typically used for attenuation of the CM noise in power line filters, but they require stricter safety standards and higher reliability than X capacitors.

To reduce the parasitic inductance, contributed mostly by the leads, the so-called feedthrough capacitors have been developed for use in EMI filters. The wire conducting the load current passes through the capacitor structure, instead of the capacitor being connected between it and the ground. This is illustrated in Figs. 42.8 and 42.9. Fig. 42.8A shows the structure of the feedthrough capacitor, and its electric symbol is shown in Fig. 42.8B. Fig. 42.9A shows that in a conventional capacitor, the parasitic inductances, L_p, of the leads are in series with the capacitance, C. The total inductance is thus $2L_p$. In contrast, as seen in Fig. 42.9B, in the feedthrough capacitor, lead inductances are connected in parallel to each other, so that the total inductance is $L_p/2$.

From the very beginning of modern power electronics, capacitors have been employed in the so-called snubbers. In the simplest embodiment, a snubber circuit consists of a capacitor with a resistor connected in series to dampen possible resonance with parasitic inductances. The snubber is placed across a semiconductor power switch to improve the switching conditions and keep the switch within its safe operating area. Snubbers reduce the EMI, which is particularly strong when the switch turns off and interrupts the load current.

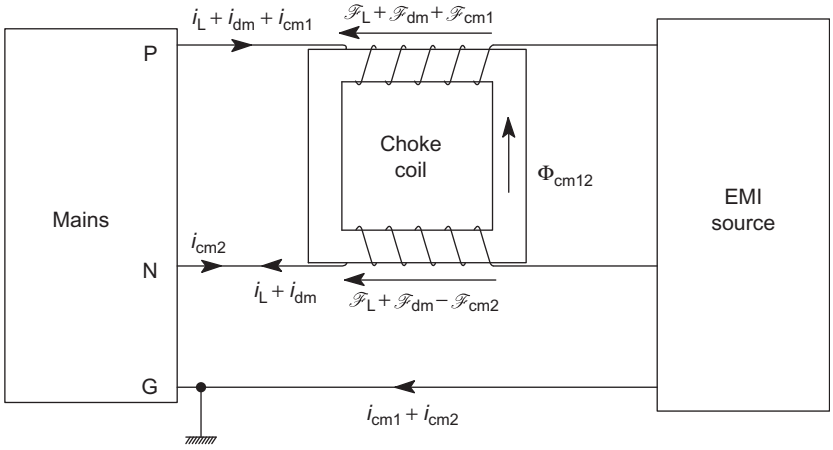


FIG. 42.7 Single-phase CM choke coil.

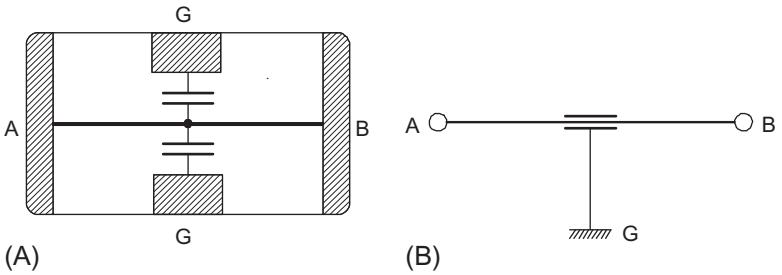


FIG. 42.8 Feedthrough capacitor: (A) structure and (B) electric symbol.

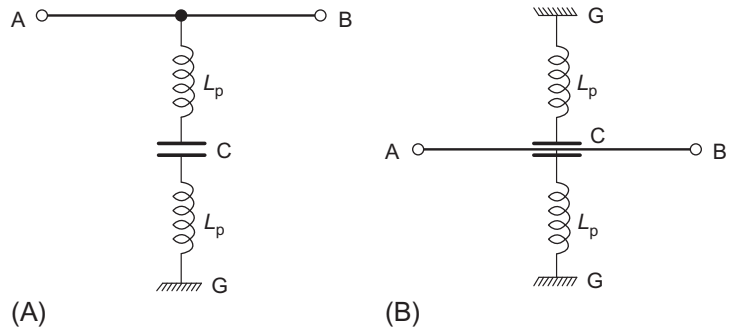


FIG. 42.9 Parasitic inductances of the leads: (A) conventional capacitor and (B) feedthrough capacitor.

Noise suppression capacitors connected to various other points in a power electronic system are also widely used, although they do not mitigate the EMI as effectively as LC filters with choke coils. Capacitive filters most often appear at the input and output of power electronic converters. They can be connected between lines or line to ground.

Basic topologies of low-pass LC filters are illustrated in Fig. 42.10. It must be stressed that EMI filters must be placed in all wires of a power electronic system. Most common configurations are shown in Fig. 42.11 for a two-wire system. The filters attenuate both the CM and DM conducted EMI. An extension of the T-type filter on a three-wire system is shown in Fig. 42.12. Similar extension can be made with respect to the other topologies of filters.

An example arrangement of the CM and DM EMI filters in the ac drive system of Fig. 42.1 is shown in Figs. 42.13 and 42.14, respectively. In the actual system, both types of filters are installed, and the two separate circuit diagrams have been used for an instructional purpose only.

The main parameter of EMI filters is the insertion loss (IL). For a given frequency, f, IL can be determined by measuring the voltage, V_G, of a sinusoidal signal generator and then connecting the filter to the generator and measuring the voltage, V_F, at the filter's output. Then,

$$\mathrm{IL} = 20\log\left(\frac{V_G}{V_F}\right)\mathrm{dB} \tag{42.16}$$

The insertion loss is usually given as an IL(f) graph with logarithmic coordinates. For filter design, the two-port network theory is employed, using the transmission, A, parameters expressing the dynamic relations between the input and output variables of a two-port network. Specifically,

$$\begin{bmatrix} V_1(s) \\ I_1(s) \end{bmatrix} = \begin{bmatrix} A_{11}(s) & A_{12}(s) \\ A_{21}(s) & A_{22}(s) \end{bmatrix} \begin{bmatrix} V_2(s) \\ I_2(s) \end{bmatrix} \tag{42.17}$$

where V_1 denotes the input (EMI-source side) voltage of the network, I_1 is the input current, V_2 is the output voltage, and I_2 is the output current, whereas s denotes the Laplace variable (complex frequency). The transmission parameters are defined as

$$A_{11}(s) = \frac{V_1(s)}{V_2(s)}\Big|I_2 = 0 \tag{42.18}$$

$$A_{12}(s) = \frac{V_1(s)}{I_2(s)}\Big|V_2 = 0 \tag{42.19}$$

$$A_{21}(s) = \frac{I_1(s)}{V_2(s)}\Big|I_2 = 0 \tag{42.20}$$

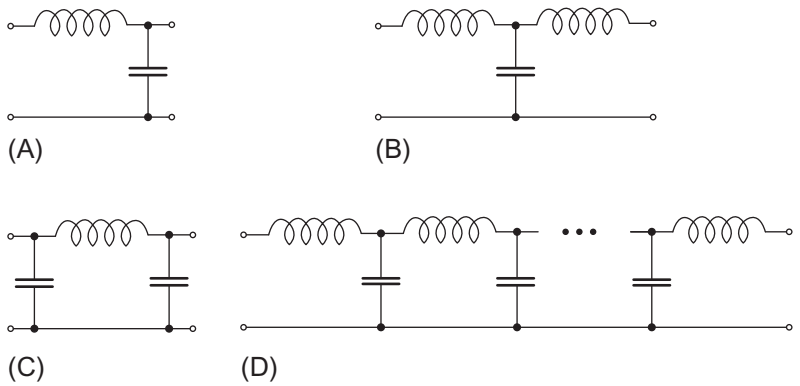


FIG. 42.10 Basic topologies of low-pass LC filters: (A) inverted gamma (Γ'), (B) pi (Π), (C) tee (T), and (D) multistage.

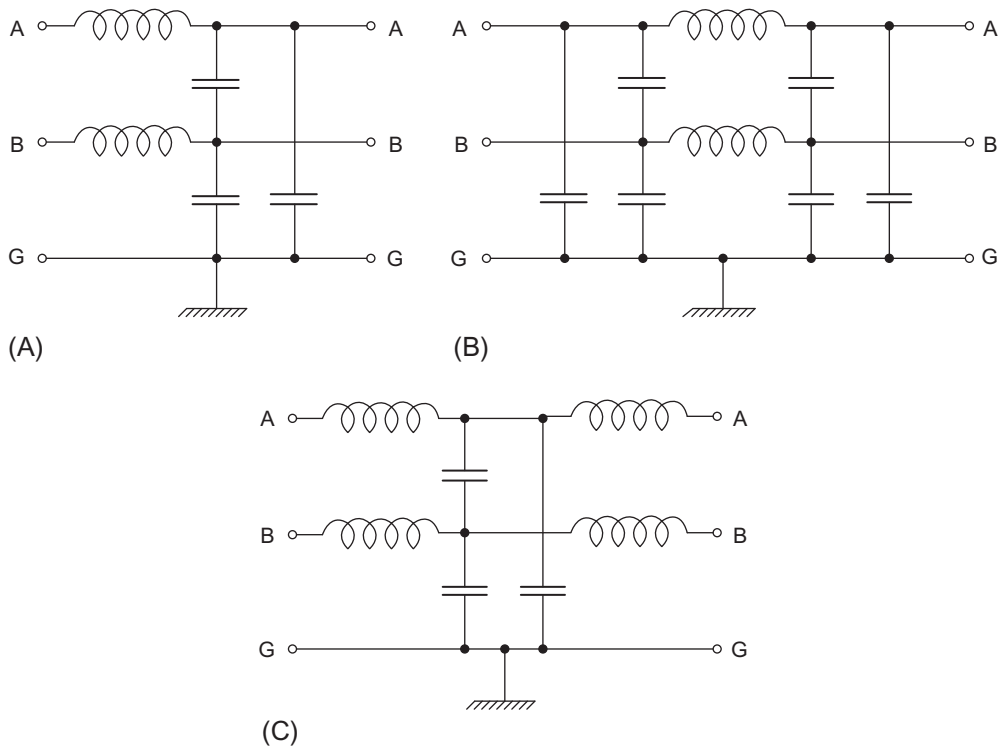


FIG. 42.11 EMI filters in a two-wire power electronic system: (A) inverted gamma (Γ′), (B) pi (*Π*), and (C) tee (T).

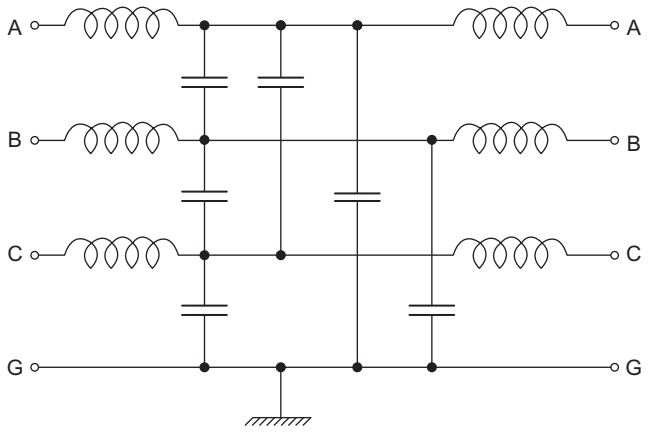


FIG. 42.12 T-type EMI filter in a three-wire power electronic system.

$$A_{22}(s) = \frac{I_1(s)}{I_2(s)} \Big| V_2 = 0 \tag{42.21}$$

Once the transmission parameters for a given filter are determined using the transient analysis of its circuit, the insertion loss can be found from the following equation:

$$\mathrm{IL}(f) = 20\log \left| \frac{[A_{21}(j\omega)Z_\mathrm{L}(j\omega) + A_{22}(j\omega)Z_\mathrm{S}(j\omega) + A_{11}(j\omega)Z_\mathrm{L}(j\omega), + A_{11}(j\omega)]}{Z_\mathrm{S}(j\omega) + Z_\mathrm{L}(j\omega)} \right| \tag{42.22}$$

where $\omega = 2\pi f$. Then, the IL(f) graph can be plotted, as illustrated in Fig. 42.15 for an actual commercial EMI filter.

The insertion loss is approximately proportional to the total inductance and capacitance (total LC) and square of the frequency. Because of the cost and size associated with the total LC value of the filter, an optimal filter is the one with a minimum total LC value, which still mitigates the EMI sufficiently to satisfy the pertaining norm. A difficulty in optimizing the EMI filter design consists in the mismatched impedance conditions under which the filters operate. From the point of view of a manufacturer of the filters, the source and load impedances are unknown. However, from the user's viewpoint, estimating the source and load impedances allows for better selection of the filter configuration. Specifically, for low source and load impedance, the "T" filter is recommended. The "*Π*" configuration is best for high source and load impedance, whereas for low source and high load impedance, the "Γ′" (LC) filter is preferred. Finally, for high source and low load impedance, the "*Γ*" (CL) topology is favored. If possible, multiple-stage filter topologies should be employed.

Practical design of EMI filters is complicated by the fact that there are no ideal inductors and capacitors. Considering the equivalent electric circuit of an inductor in Fig. 42.16A and that of a capacitor in Fig. 42.16B, it can be seen that at very high frequencies, the impedance of the parasitic components, marked by the subscript "p," may dominate that of the main component. Thus, the reactance of the parasitic capacitance, C_p, of the inductor can make the overall impedance to decrease with the frequency, and the reactance of the parasitic

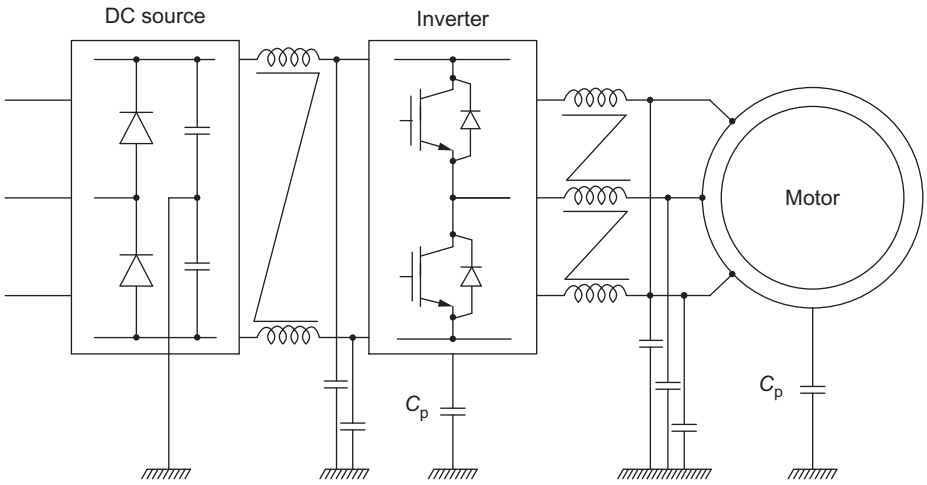


FIG. 42.13 Placement of CM EMI filters in the drive system of Fig. 42.1.

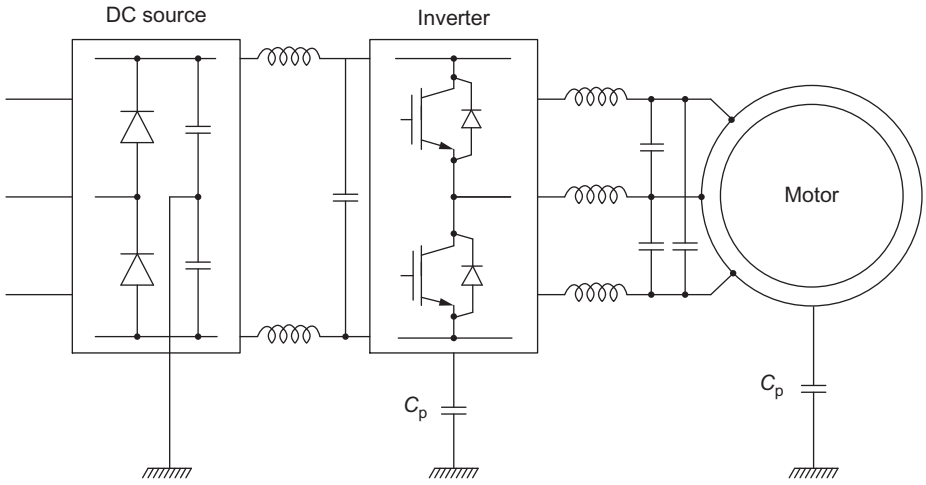


FIG. 42.14 Placement of DM EMI filters in the drive system of Fig. 42.1.

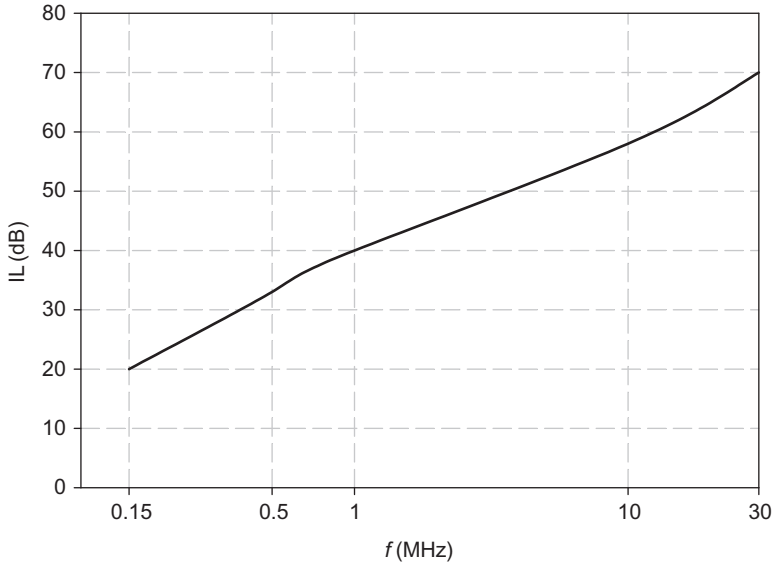


FIG. 42.15 An example insertion loss versus frequency graph for an EMI filter.

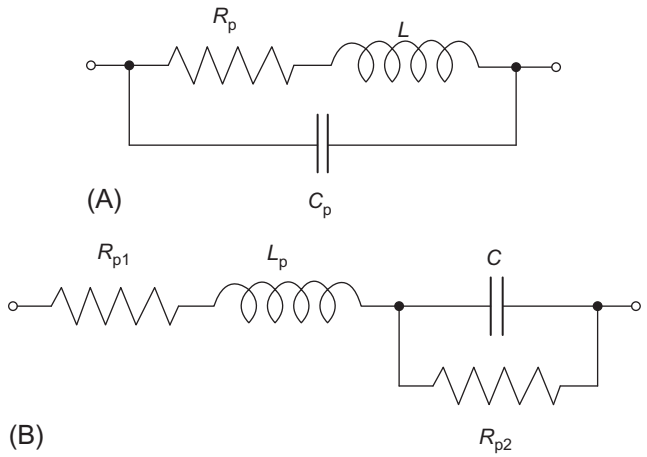


FIG. 42.16 High-frequency equivalent circuits of (A) capacitor and (B) inductor.

inductance, L_p, of the capacitor can make the overall impedance of the capacitor to increase. That is why manufacturers of EMI filters and their components go to great lengths to minimize the parasitics.

In the common case of power electronic converters fed from the grid, the so-called power line filter is installed between the grid and converter. It protects the converter and its load from external disturbances and, vice versa, screens out the grid from EMI generated in the converter. Voltage impulses originated within the grid are particularly hazardous for the converter, and varistors are used in the filter to attenuate the impulses. An example of commercial power line filter is shown in Fig. 42.17. In the drive system in Fig. 42.1, the filter would be connected to the three-phase input terminals of the dc source (rectifier).

Numerous vendors offer a variety of power line and EMI filters with a wide range of voltage and current ratings. Thus, designers of power converters and converter-fed systems have a choice of quality products, without the need for designing their own filters. Useful details of the process of EMI filters design can be found in [7,8].

Active EMI filters, although very effective, are less common than the passive filters described because of their increased complexity and cost. They are based on the feedback principle, generating currents that neutralize the noise currents. In the dc-to-dc converters, they are also employed to limit inrush currents, for example, during the so-called hot swapping, when a faulty electronic board is replaced without interrupting operation of the system. In certain three-phase systems with power converters such as ac drives, the CM voltage noise, apart from producing external interference, causes internal problems, for example, accelerated wear of bearings. The so-called CM voltage cancellers are one of the means to mitigate those problems. Such a voltage canceller in the drive system of Fig. 42.1 is shown in Fig. 42.18.

42.5 Random Pulse Width Modulation

Suppression of the low-frequency noise originating from the PWM operating mode of most power converters is particularly difficult. As already pointed out in Section 42.1, the noise, mostly harmonics of the voltages and currents, appears in the frequency spectra as harmonic clusters around multiples of the switching frequency, f_{sw}. As seen in Fig. 42.3, the highest magnitudes of the harmonics appear at the lower end of the frequency range, while the insertion loss of EMI filters progressively increases with the frequency, as shown in Fig. 42.15. Thus, at low frequencies, effectiveness of the filters decreases. Increasing the total LC value helps, but it results in corresponding increase of the cost and bulk of the filters. Therefore, mitigation of harmonics by means of special PWM strategies is the best solution for filter minimization.

Most of the commercial PWM power converters are characterized by a fixed switching frequency, f_{sw}, defined here as a reciprocal of the switching period, T_{sw}. The switching period constitutes the length of a switching interval, which houses pulses of switching variables of the converter, one pulse per variable. Duty ratio of a given pulse varies from 0 to 1; that is, the width (duration) of the pulse is in the range of $0 - T_{sw}$. It has been demonstrated in many publications, for example, [9] that

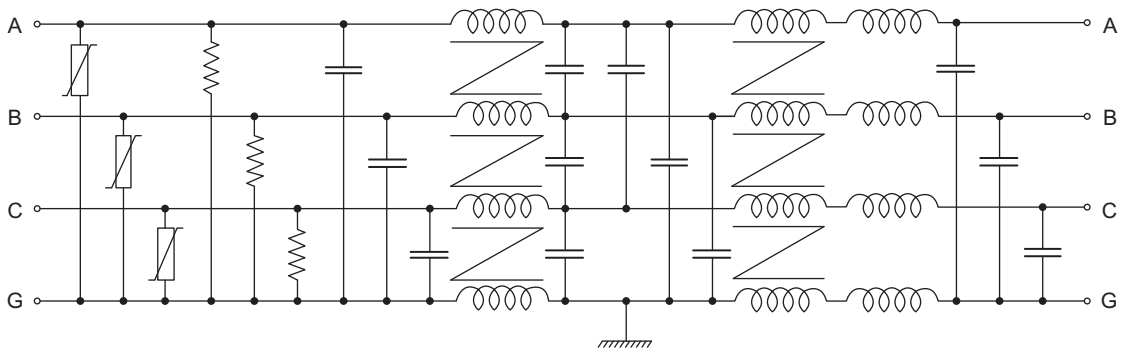


FIG. 42.17 Power line filter.

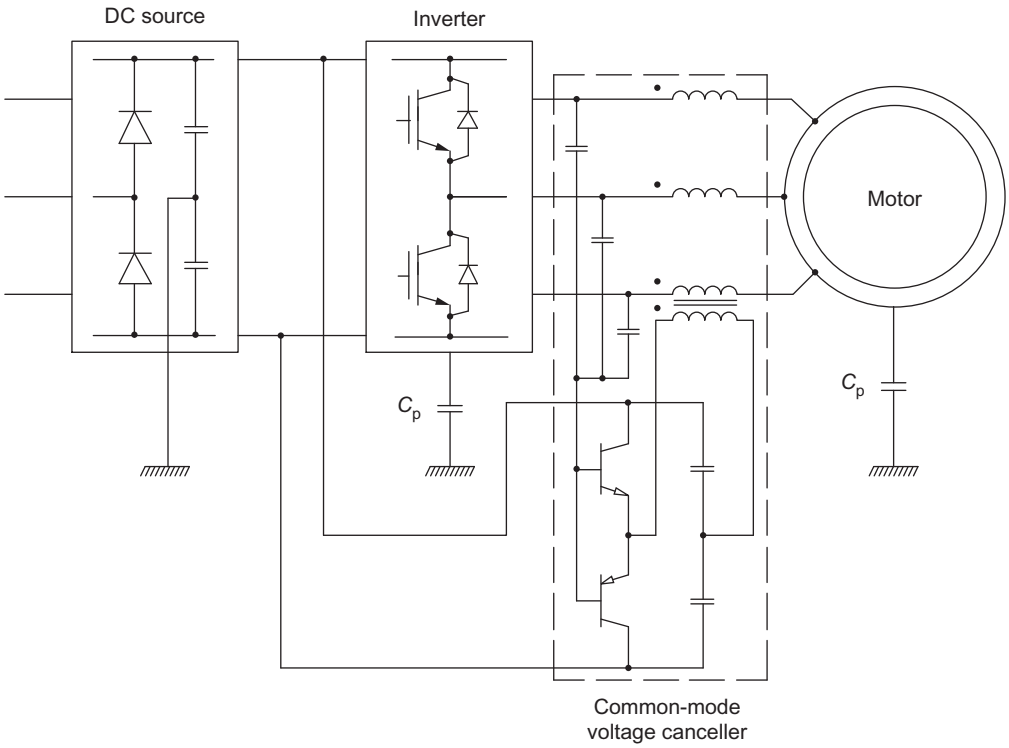


FIG. 42.18 Common-mode voltage canceller.

if individual switching periods are randomly varied, then the discrete harmonic power (watts) of spectra of the voltages and currents of the converter is transferred to continuous power spectral density (watts/hertz). This strategy of random pulse-width modulation (RPWM) results in significant mitigation of both the acoustic and electromagnetic noise associated with the current harmonics [10,11]. Accumulated experience and theoretical considerations show that varying T_{sw} from 0.5 to 1.5 of the average switching period, $T_{sw,ave}$, is sufficient. Thus, the nth switching period is determined as

$$T_{sw,n} = (r_n + 0.5)T_{sw,ave} \tag{42.23}$$

where r_n is a uniform-probability random number in the 0–1 range.

For convenience, in practical digital modulators for PWM converters, the switching cycles coincide with the sampling cycles of the modulator, that is, $f_{sw} = f_{smp}$, where f_{smp} denotes the sampling frequency (not to be confused with the much higher clock frequency). Consequently, the varying switching rate is associated with identically varying sampling rate. When a single digital system performs more tasks than just PWM, the random sampling rate is a disadvantage. For instance, in a control system, the sampling rate defines the control bandwidth, and it is selected at a specific trade-off level. Therefore, an RPWM technique with a fixed sampling rate but variable switching frequency is more practical. Fig. 42.19 illustrates (A) the most common, nonrandom PWM technique with

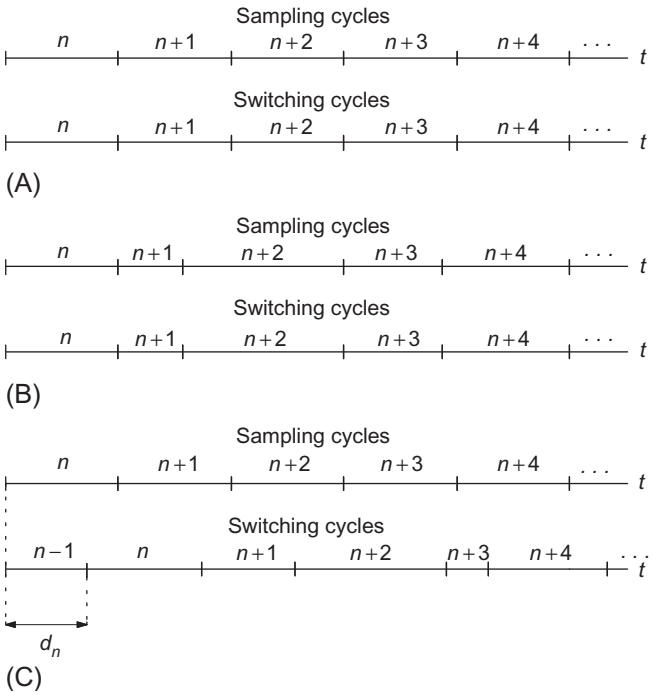


FIG. 42.19 Illustration of PWM techniques: (A) fixed-period and coinciding sampling and switching cycles, (B) randomly varied and coinciding sampling and switching cycles, and (C) fixed-period sampling cycles and variable-period switching cycles (VD-RPWM).

fixed-period and coinciding sampling and switching cycles; (B) RPWM with randomly varied and coinciding sampling and switching cycles; and (C) RPWM with fixed sampling periods and randomly varied switching periods, subsequently referred to as variable-delay RPWM (VD-RPWM).

As seen in Fig. 42.19C, the switching cycles in the VD-RPWM method are delayed with respect to the corresponding sampling cycles by a randomly varied time delay, d. The value of d for the nth switching cycle is calculated as

$$d_n = r_n T_{\text{smp}} \tag{42.24}$$

where $T_{\text{smp}} = 1/f_{\text{smp}}$ denotes the sampling period. When in two consecutive switching cycles, denoted by k and $k+1$, r_{k} is close to 1, and $r_{\text{k}+1}$ is close to 0; the second, $k+1$, switching cycle may be too short; that is, its length, $T_{\text{sw},k+1}$, may be lower than the minimum allowable length, $T_{\text{sw,min}}$. Therefore, in case of such occurrence, $T_{\text{sw},k+1}$ is set to $T_{\text{sw,min}}$, or another value of r_{k} is selected. As a result, the switching periods vary from T_{min} to $2T_{\text{smp}}$. The average switching period, $T_{\text{sw,ave}}$, equals the sampling period, T_{smp}.

Any PWM strategy based on the concept of switching cycles can be employed within the RPWM method. For instance, the popular space-vector modulation can be used in three-phase voltage-source inverters. As long as the average switching period is sufficiently short, the quality of output current is similar to that in a converter with a fixed switching frequency having the same period. An example spectrum of the output current of a voltage-source inverter controlled using the VD-RPWM is shown in Fig. 42.20. It is the same converter whose current spectrum, with fixed-period PWM, was shown in Fig. 42.3. The noise suppression by 10 dBμA is easily observable. A spectrum corresponding to that in Fig. 42.4 is shown in Fig. 42.21. Here, the EMI mitigation, by about 20 dBμA, is even stronger.

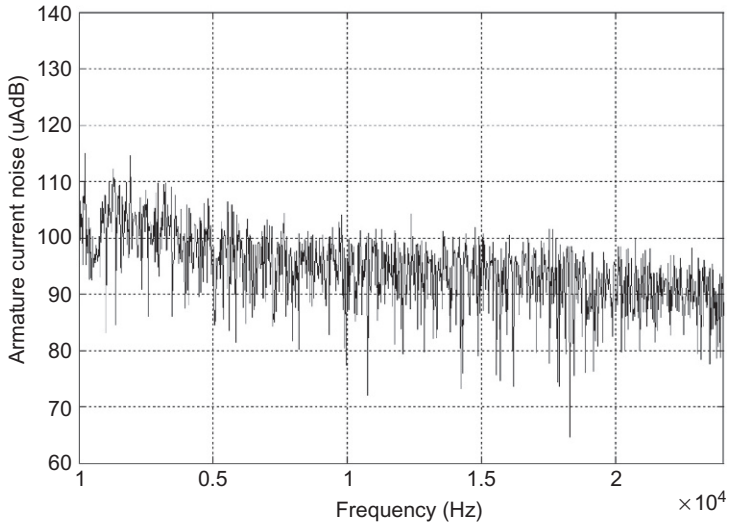


FIG. 42.20 Frequency spectrum of output current of a voltage-source inverter with VD-RPWM.

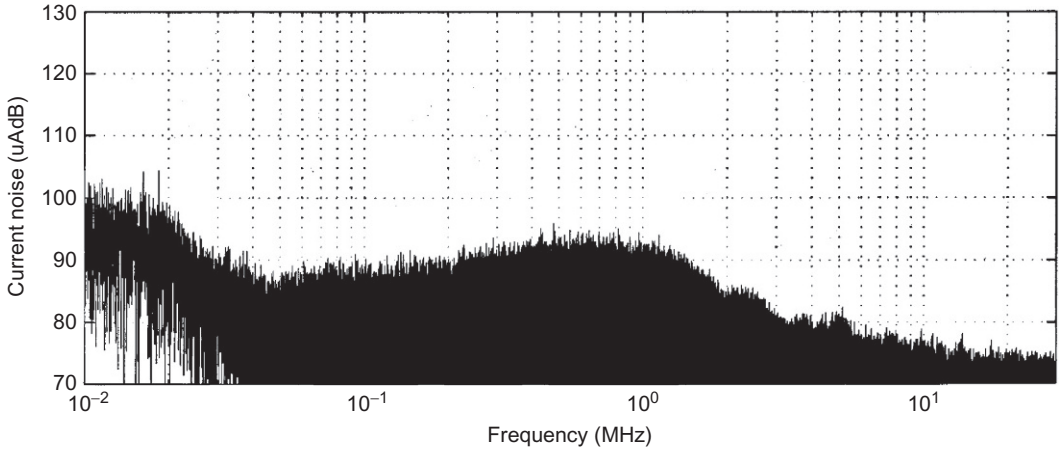


FIG. 42.21 Wide-range frequency spectrum of inverter current with VD-RPWM.

Although RPWM is not a perfect tool for EMI mitigation, it effectively eliminates high harmonics of the input and output currents and output voltages in PWM power converters. The EMI filters are usually still needed for the suppression of transients, impulses, and high-frequency noise. However, their total LC value can be greatly reduced. The RPWM technique with random switching and sampling periods is a little more effective than the VD-RPWM because of the somewhat greater freedom of randomization, and it is recommended for converters whose pulse-width modulator operates independently of the rest of the system.

It is worth mentioning that PWM techniques have been developed that reduce the CM noise in three-phase inverters by elimination (or significant reduction) of the so-called zero states, in which all the three-phase terminals are clamped by the inverter switches to one of the dc buses. Other solutions involve addition of a fourth leg to the inverter or use of multilevel inverters.

42.6 Other Means of Noise Suppression

In addition to filters and PWM methods, means of mitigation of EMI effects in systems with power electronic converters include grounding, shielding, and minimization of electromagnetic coupling. When skillfully used, they can significantly reduce the EMI and circuit susceptibility at a low extra cost.

Effects of grounding on the EMI must be considered in the context of the whole system employing power electronic converters. Grounding of electric equipment has historically been based on the requirements of safe and reliable power distribution, maximum protection against overvoltages (including lightning strikes and electrostatic buildup), and safe-touch conditions for personnel during ground faults. The so-called safety ground (green wire in the United States) protects personnel and equipment by conducting fault current, operating a circuit breaker or fuse, and limiting the voltage to ground during faults. This type of grounding can be termed low-frequency grounding. The earth ground is made using buried rods, plates, or grids. Note that the ground wiring for lightning protection must be isolated from other grounding conductors, and the lightning current may not pass through any circuit breaker or fuse. Considering the drive system in Fig. 42.1 and assuming the "Y" connection of the secondary windings of the supplying transformer, the neutral of the transformer can be ungrounded, directly grounded, or connected to the ground through a resistor. Each of these arrangements has advantages and disadvantages, but the resistance-grounded system has gained the greatest popularity because the line-to-ground faults do not cause immediate shutdown of the system. Proper selection of the grounding resistance allows sufficient limitation of the ground fault currents and the voltage to ground to avoid equipment failures.

The high-frequency grounding, which should be considered separately from the low-frequency scheme, has a strong impact on the CM EMI. The general rule for proper high-frequency grounding design is to understand the CM noise path and to reroute the noise away from the sensitive electronics. A single-point grounding scheme is theoretically the best, although the existence of many stray system-to-ground capacitances makes it practically a multipoint grounding above certain frequencies. Physical capacitors are often used to augment the stray capacitances, for example, between the chassis and the grounding wire, to reduce the CM noise voltage. High-power parts of a system should be connected the closest to the single-point ground, with the most sensitive circuits the furthest from it.

Most practical systems with power converters include cables, for example, those connecting the inverter to the motor in the drive in Fig. 42.1. The cables act as antennas for the radiated EMI, and they are receptors in the electromagnetic coupling. Shielding the cables significantly reduces those unwanted phenomena. Such types of cables as the aluminum-armor or braided-shield ones offer very good protection from EMI. In particular, they prevent interference with sensitive equipment by providing an isolated and predictable metallic path for the CM noise. The shield is usually bonded with the ground wire at both ends of the cable. For industrial installations, such as drive systems in a factory, use of grounded steel conduits to carry cables is a convenient and effective solution. Shielding can also be applied to other than cables, parts of the electronic circuitry, such as circuit enclosures.

As illustrated in Fig. 42.22, the electromagnetic noise coupling can be capacitive (electric field) or inductive (magnetic field). The noise source voltage is denoted by v_n, and the stray capacitance, C_{12}, and mutual inductance, M_{12}, link wires 1 and 2 transmitting noise from the source. The coupling capacitances and inductances should therefore be minimized. The simplest, but not always practical, approach is to increase the distances between noise sources and receivers. Shielding is a good protection from electromagnetic noise coupling, and the unshielded leads extending beyond the shield should be possibly short [12].

Electromagnetic noise coupling can also be minimized by proper circuit geometry. The potential noise source should not be placed in parallel to the potential noise receiver. Perpendicular placement is best. Twisting two interconnecting wires helps as well because currents in individual wires flow in opposite directions, producing magnetic fields that cancel each other.

EMI reduction techniques should also be considered at the printed circuit board (PCB) level. Proper grounding, power distribution, and interconnection techniques, depending on whether the PCB contains analog or digital circuitry, improve immunity to both the internal and external noise sources. This highly specialized topic extends the tutorial scope of this publication.

A thorough compendium of various means of EMI mitigation in inverter-fed ac drive systems can be found in [12]. It should be stressed that EMI suppression techniques should be considered in early stages of the design. Otherwise, the

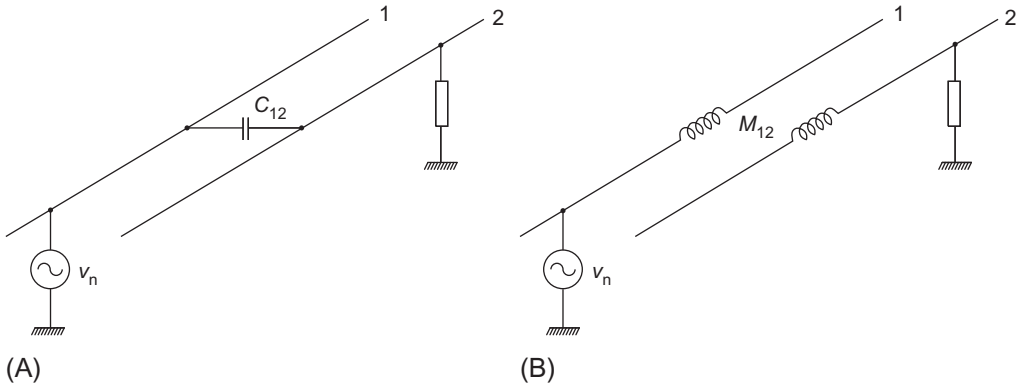


FIG. 42.22 Electromagnetic coupling: (A) capacitive and (B) inductive.

designed system would be likely to have serious and expensive to fix noise problems.

42.7 EMC Standards

The number of institutions involved in regulations and recommendations that concern EMI is quite large, and to an average person, the issue of EMC standards can be somewhat confusing. EMC is defined as the ability of equipment to function satisfactorily in its electromagnetic environment without introducing intolerable disturbances to anything in that environment. EMC requirements entail two major items: emissions and susceptibility or its opposition—the immunity. Electromagnetic disturbance is any phenomenon that may degrade the performance of a device or system or adversely affect the living and inert matter. The term "EMI" pertains to that performance degradation. It is worth mentioning that in the colloquial engineering language, EMI is often meant as emissions and EMC as immunity, which is inexact. In the important US military standard, MIL-STD 461, the emissions and immunity requirements are referred to as conducted/radiated emissions (CE/RE) and conducted/radiated susceptibility (CS/RS).

In the United States, it is the Federal Communications Commission (FCC) that sets the general EMC requirements, but medical products are regulated by the Food and Drug Administration (FDA). The FCC rules and regulations, title 47, part 15, subpart B concerns *any unintentional radiator (device or system) that generates and uses timing pulses at a rate in excess of 9000 pulses (cycles) per second and uses digital techniques.* Clearly, that mandatory requirement applies to almost every product that employs a microprocessor. It is illegal to sell or advertise for the sale of any product regulated under part 15, subpart B until its emissions have been measured and found to be in compliance. Products regulated by part 15, subpart B are divided in two classes. Class A devices are those marketed for use in commercial applications, whereas the domestic applications belong to class B. As illustrated in Fig. 42.23, class B limits are more stringent than those for class A products, and the class B administrative *certification* process is more rigorous than the class A *verification* process. The American National Standards Institute (ANSI) standard C63.4 defines the required emission test procedures. However, there are no FCC regulations pertaining to product immunity to electromagnetic fields.

EMC requirements for products used by the US military are listed in the already mentioned MIL-STD-461. This standard is applicable to a wide range of systems, from power tools to computer workstations. Unlike the FCC regulations, MIL-STD-461 specifies limits for both the emissions and immunity. The ANSI and Institute of Electrical and Electronics Engineers (IEEE) also publish EMC standards, as do, for internal use, private organizations, such as the Society of Automotive Engineers (SAE) and automobile manufacturers.

Under provisions of the General Agreement on Tariffs and Trade (GATT) and its successor, the World Trade Organization (WTO), member countries are obliged to adopt international standards for national use. With respect to the EMC, international standards are primarily developed by the International Electrotechnical Commission (IEC) and its International Special Committee on Radio Interference (CISPR); both were already mentioned in the introduction to this chapter. The series of IEC standards, IEC 61000-1 through IEC 61000-6, covers all aspects of EMC. The FCC standards are harmonized to IEC standards, as are the European Norms (EN) used in the European Union (EU). Some specific EMC standards have also been published by the International Organization for Standardization (ISO).

In 1992, the EU eliminated internal borders, necessitating a common system for establishing EMC standards and accreditation, testing, and certification procedures. The "new approach" and "global approach" have been initiated; their goal are to include EU directives into national laws of EU states, harmonize national standards with the European standards, and ensure validity of test reports and conformity certificates between all member states.

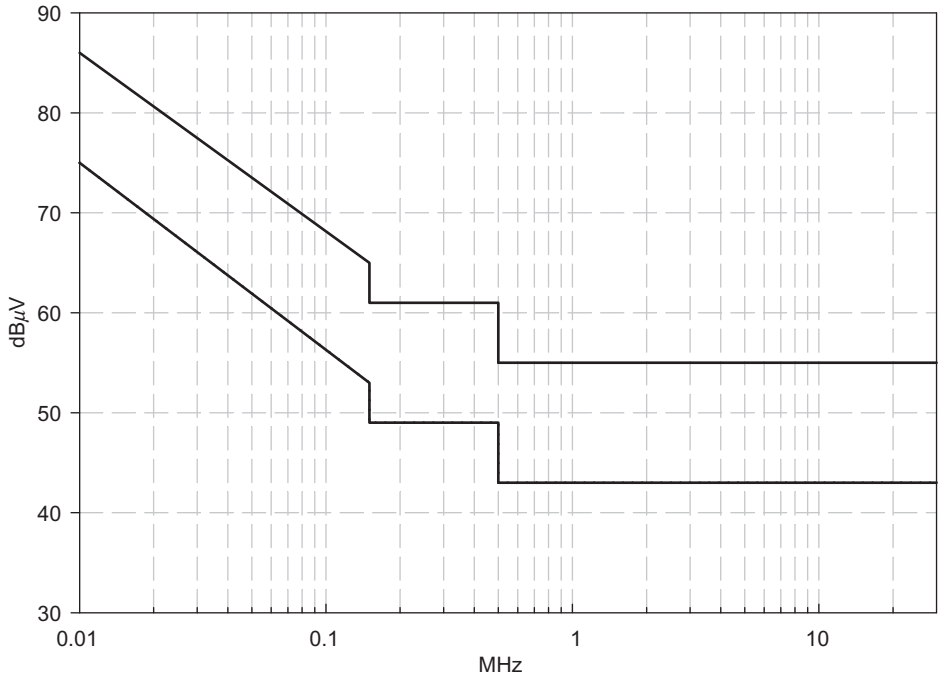


FIG. 42.23 FCC conducted emissions limits. Upper trace, class A, and lower trace, class B.

According to the "new approach," technical contents have been removed from the European directives and entrusted to the European standard bodies, which are Comitè Europèen de Normalization (CEN), Comitè Europèen de Normalization Electrotechnique (CENELEC), and European Telecommunication Standards Institute (ETSI). The key European directive 89/336/EEC "electromagnetic compatibility" gives only a general definition of the *essential protection requirements* for all electric and electronic equipment and systems while referring to CENELEC and ETSI standards for technical details. The "global approach" requires every product on the European market to have the permanent "CE" marking, which indicates that the affixer declares and takes full responsibility of the conformity to all applicable European directives.

The EMC directive 89/336/EEC sets up emission and immunity requirements. It defines (a) components, (b) systems, and (c) installations. The directive applies only to components performing direct function and to the systems. Standards referred to the directive are divided into basic standards, generic standards, and product standards. The basic standards define general EMC requirements and testing procedures, without specifying any limit values or assessment criteria. Generic standards specify the requirements for products in specific electromagnetic environments. For instance, EN 50081-1 applies to emissions in residential, commercial, and light industrial equipment, including power supplies for industrial equipment, and EN 50081-2 to emissions in industrial environments. Respective immunity norms are EN 50082-1 and EN 50082-2. Product standards address EMC requirements for certain products and product families, such as household appliances, information technology equipment, or generic light industrial equipment; various European norms are employed as the product standards.

The IEC 555-2 (EN 60555-2), IEC 1000-3-2 (EN 61000-3-2), and IEC 1000-3-4 are emission standards for low-frequency harmonics, closely associated with operation of power electronic converters. Voltage fluctuations and flicker (*impression of unsteadiness of visual sensation induced by a light stimulus whose luminance or spectral distribution fluctuates in time*) emission limits are defined in IEC 555-3 (EN 555-3), IEC 1000-3-3 (EN 61000-3-3), and IEC 1000-3-5. IEC 61000-4-7 and IEC 61000-4-15 define the required instrumentation for EMI measurements. Radio-frequency conducted and radiated emissions are dealt with in EN 55011, EN 55014, and EN 55022, whereas CISPR 16 is the basic standard for radio-interference measurements. Finally, IEC 1000-4-1 through IEC 1000-4-12 are immunity standards.

EMC standards are continuously being developed and revised. Therefore, it is important to keep track of standards' publication dates (DoP) and dates of withdrawal (DoW) of conflicting earlier standards. Temporary EN standards are called ENV. Numerous Internet resources are available, in particular:

- American National Standards Institute (ANSI)
- Canadian Standards Association
- Electronic Industries Association (EIA)
- European Telecommunications Standards Institute (ETSI)
- Federal Communications Commission (FCC)

- IEEE Standards Association
- International Electrotechnical Commission (IEC)
- International Organization for Standardization (ISO)
- National Institute of Standards and Technology (NIST)
- NSSN, A National Resource for Global Standards
- Society of Automotive Engineers (SAE)
- Standards Australia
- VCCI (Japanese EMC Regulation and Certification)
- Verband Deutscher Elektrotechniker e. V. (VDE–German standards)

For more EMC information links, go to http://www.dbtechnology.co.uk/links.htm and https://en.wikipedia.org/wiki/List_of_common_EMC_test_standards. A comprehensive treatment of contemporary EMC issues in power electronic and power distribution systems can be found in [13,14].

References

[1] D.A. Weston, Electromagnetic Compatibility: Principles and Applications, third ed., CRC Press, Boca Raton, FL, 2016.
[2] K.L. Kaiser, Electromagnetic Compatibility Handbook, CRC Press, Boca Raton, FL, 2005.
[3] P.G. Andre, K. Wyatt, EMI Troubleshooting Cookbook for Product Designers, SciTech Publishing, Edison, NJ, 2014.
[4] C.R. Paul, Introduction to Electromagnetic Compatibility, second ed., John Wiley, Hoboken, NJ, 2009.
[5] H.W. Ott, Electromagnetic Compatibility Engineering, second ed., John Wiley, Hoboken, NJ, 2009.
[6] F. Cost, E. Laboure, Electromagnetic Compatibility in Power Electronics, John Wiley, Hoboken, NJ, 2014.
[7] R.L. Ozenbaugh, EMI Filter Design, second ed., Marcel Dekker, New York, 2001.
[8] M.J. Nave, Power Line Filter Design for Switched-Mode Power Supplies, Van Nostrand Reinhold, New York, 1991.
[9] R.L. Kirlin, M.M. Bech, A.M. Trzynadlowski, Analysis of power and power spectral density in PWM inverters with randomized switching frequency, IEEE Trans. Ind. Electron. 49 (2) (2002) 486–499.
[10] M. Vilathgamuwa, J. Deng, K.J. Tseng, EMI suppression with switching frequency modulated DC-DC converters, IEEE Ind. Appl. Mag. 5 (6) (1999) 27–33.
[11] A.M. Trzynadlowski, M. Zigliotto, M.M. Bech, Random pulse width modulation quiets motors, reduces EMI, PCIM Power Electron. Syst. Mag. (1999) 55–58.
[12] X.C. Tong, Advanced Materials and Design for Electromagnetic Interference Shielding, CRC Press, Boca Raton, FL, 2009.
[13] G.L. Skibinski, R.J. Kerkman, D. Schlegel, EMI emissions of modern PWM AC drives, IEEE Ind. Appl. Mag. 5 (6) (1999) 47–80.
[14] L. Rosetto, P. Tenti, A. Zuccato, Electromagnetic compatibility issues, IEEE Ind. Appl. Mag. 5 (6) (1999) 34–46.

Further Reading

[1] F. Lattarulo, Electromagnetic Compatibility in Power Systems, Elsevier, Amsterdam, 2007.

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Power Electronics Standards

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43.1 Introduction

Famous admiral Rickover often made the point that what was needed to get things done in the world of technology was engineering more than science. He also said: "Engineering is a profession which affects the material basis of everyone's life. To practice a profession one must have acquired mastery of an academic discipline as well as a technique for applying this special knowledge to the problems of everyday life. A profession is therefore intellectual in content, practical in application."

Dr. Henry Petroski, specialist in failure analysis and professor of civil engineering at Duke University, put it in these words: "Engineers are not superhuman. That they make mistakes is forgivable; that they catch them is imperative. Thus it is the essence of modern engineering not only to be able to check one's own work but also to have one's work checked and to be able to check the work of others."

As in any rapidly advancing technology, power electronics standards are the risk mitigation tool, which allow using collective practical experience of many generations of engineers. Knowledge of the standards accelerates acceptance of power electronics and allows doing things right from the first time. Typically, standards formulate what is required and should be considered leaving to user decisions how requirements of the standards are implemented.

43.2 General Review of Power Electronics Standards

All power electronics standards are application-specific and could be categorized as follows:

1. Recommended professional engineering standards developed by engineering societies, manufacturing associations, and testing laboratories
2. Mandatory regulation standards developed or adapted by country or local authorities for operation of power electronics in their area of jurisdiction
3. End user- or customer-specific standards mutually agreed by user and manufacturer.

The major international developers of power electronics engineering standards are the Institute of Electrical and Electronics Engineers (IEEE), International Electrotechnical Commission (IEC), National Electrical Manufacturers Association (NEMA), and Underwriters Laboratories (UL). Each standard organization has its own procedures for developing standards:

- IEEE Working Groups develop standards through a consensus development process, which brings together volunteers representing varied viewpoints and interests to achieve the final product. These standards are approved only when a 75% consensus is reached. IEEE standards

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are creating technical base for customer's selection and acceptance of products and the technical base for codes, rules, and regulations by different enforcing and regulating authorities.
- IEC technical committees by specialists from participating countries develop IEC standards expressing an international consensus of opinion on the relevant subjects from all interested IEC National Committees having equal voting rights. Each participating country is responsible for enforcement of standards.
- NEMA technical committees of representatives from members of association develop NEMA standards. NEMA members are responsible for compliance with standards.
- UL specialists develop UL standards with inputs from manufacturers and consumers. Compliance with standards required for power electronics products liability insurance or by end users and consumers.

There are many standards for power electronics components, but the list of power electronics standards as an equipment is relatively short:

- IEEE Std 1100 (Emerald Book), IEEE Recommended Practice for Powering and Grounding Electronic Equipment
- IEEE Std 1303 Guide for Static Var Compensator Field Tests
- IEEE Std 1409 Guide for Application of Power Electronics for Power Quality Improvement on Distribution Systems Rated 1 kV Through 38 kV
- IEEE Std 1566 IEEE Standard for Performance of Adjustable Speed AC Drives Rated 375 kW and Larger
- IEEE Std 1515 IEEE Recommended Practice for Electronic Power Subsystems: Parameter Definitions, Test Conditions, and Test Methods
- IEEE Std. 1573 IEEE Recommended Practice for Electronic Power Subsystems: Parameters, Interfaces, Elements, and Performance
- IEEE Std 1585 IEEE Guide for the Functional Specification of Medium Voltage (1–35 kV) Electronic Series Devices for Compensation of Voltage Fluctuations
- IEEE Std 1662-2008 Guide for the Design and Application of Power Electronics in Electrical Power Systems on Ships
- IEEE Std 1676 IEEE Guide for Control Architecture for High Power Electronics (1 MW and Greater) Used in Electric Power Transmission and Distribution Systems
- IEEE Std 1688 Standard for requirements for the Control of Electromagnetic Interference Characteristics of Replaceable Electronic Modules
- IEC 60146, Semiconductor converters—Basic requirements: Part 1-1: Line Commutated converters and Part 1-2: Self-commutated semiconductor converters including d. c. converters
- IEC 61800 all parts, Adjustable speed electrical power drive systems
- ANSI/UL 347A Medium Voltage Power Conversion Equipment
- ANSI/UL 508C-2008 Power Conversion Equipment
- ANSI/UL 61800-5 all parts, Adjustable Speed Electrical Power Drive Systems
- NEMA Standards Publication ICS 1.1 Safety Guidelines for the Application, Installation, and Maintenance of Solid-State Control
- NEMA ICS 7.2 Application Guide for AC Adjustable Speed Drive Systems
- NEMA Standards Publication IC 10 Industrial Control and Systems Part 2: Static AC Transfer Equipment
- UL 1008S Standard for Solid-State Transfer Switches

43.3 Examples of IEEE Power Electronics Standards

43.3.1 IEEE Std 1662-2016 "Recommended Practice for the Design and Application of Power Electronics in Electrical Power Systems"

This standard was sponsored by the Industrial Applications Society (IAS) and cosponsored by the Power Electronics Society (PELS). The standard recommends that power electronics equipment should do the following:

- Take self-protection actions regardless of the status of communications by reflexive actions to maintain continuity of power.
- Respond to internal and downstream faults.
- Sustain communications and ability to perform control actions following a loss of input voltage to permit detection, isolation, and system reconfiguration following a casualty condition.
- Latch parameter values at the time of the fault and communicate status to higher-level outside controllers.
- Interact with other power electronics equipment for power flow management and fault handling.
- High-resistance grounding preferable on the source side of isolated and otherwise ungrounded three-wire, three-phase distribution systems with voltages over 1000 V and aggregated power above 1.5 MW.
- PE should have a minimum efficiency of 95% (5% total losses) at rated load condition. PE should be provided with an overload rating of 150% for 1 min.

Three sets of test recommended to be conducted on power electronics equipment:

- Type test—Test of one or more devices made to a certain design to demonstrate that the design meets certain specifications.

- Production test—A test conducted on every unit of equipment prior to shipment.
- Commissioning test—A test conducted when the equipment is installed to verify correct operation.

43.3.2 IEEE Std 1676-2010 "Guide for Control Architecture for High Power Electronics (1 MW and Greater) in Electric Power Transmission and Distribution Systems"

This standard sponsored by the IEEE Power Engineering Society (PES) recommends the use of Power Electronics Building Block (PEBB) concept in electric power systems. It recommends PEBB multilayer control architecture and states, for example:

- The interface between layers should be designed to enable layer modularity such that replacement of any layer should not induce modifications in other layers.
- The communication speed requirements at the lowest or hardware layer are the greatest and decline with each higher control layer.
- In order to preserve the hierarchical architecture, horizontal communication between layers should be avoided.
- It is also recommended that each converter have its own independent switch control to serve its hardware control.

43.3.3 IEEE Std 1826-2012 "IEEE Standard for Power Electronics Open System Interfaces in Zonal Electrical Distribution Systems Rated Above 100 kW"

This standard was sponsored by the Industrial Applications Society (IAS) and cosponsored by the Power Electronics Society (PELS). The standard applies in cases where power electronics is the interface between the zones and extends application of IEEE Standards 1662 and 1676. It states that each power electronics device attached to the power bus shall meet following criteria:

1. Each device shall conform to standard control and power interfaces.
2. Each device shall have functionality that lets it "play well" with other power electronics devices including having the same protection and safety features.
3. Each device shall be capable of information exchange and reconfiguration of the system in response to load demands, changes of the mission, or new technologies insertion.

Any standard is always available from standard publishers.

43.4 Conclusions

- The best definition of the importance of standards is the famous saying by Admiral Rickover: "You have to learn from the mistakes of others. You won't live long enough to make them all yourself."
- Standards establish baseline for customer's selection and acceptance of products.
- Standards are collective practical experience of many generations of engineers. They are the best tools to avoid mistakes and do things right from the first attempt.
- Standards are risk reduction in applying new power electronics technologies by combining established industrial practices with the latest innovations and modern analytic tools.
- Standards are best defense from outrageous regulators demands and frivolous lawsuits.
- The latest editions of any standard are always available from the standard publisher.

Further Reading

[1] IEEE Std. 1662-2016 Recommended Practice for Design and Application of Power Electronics in Electrical Power Systems.
[2] IEEE Std. 1566-2015, Standard for Performance of Adjustable Speed AC Drives Rated 375 kW and Larger.
[3] IEEE 1826-2012, Standard for Power Electronics Open System Interfaces in Zonal Electrical Distribution Systems Rated Above 100 kW.
[4] IEEE Std 1676-2010, Guide for Control Architecture for High Power Electronics (1 MW and Greater) Used in Electric Power Transmission and Distribution Systems.
[5] Yuri Khersonsky, Standards for Ships and Oil Platforms, IEEE Industry Applications Magazine, Jan/Feb 2016.
[6] Yuri Khersonsky, PEBB Concept and the IEEE Power Electronics Standards, IEEE International Symposium on Industrial Electronics, Bari, Italy, 4–7 July 2010.
[7] Yuri Khersonsky, IEEE Power Electronics Standards-the necessary tools for every power electronics engineer, Applied Power Electronics Conference APEC 2010, Palm Spring, CA, February 26, 2010.
[8] Yuri Khersonsky, Role of standards in Power Electronics Rap session presentation, APEC 2008, Feb 24–28, 2008, Austin TX.

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Section VIII

Simulation and Packaging

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44

Computer Simulation of Power Electronics and Motor Drives

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44.1 Introduction

This chapter shows how power electronics, electric motors, and drives can be simulated with modern spice-based software simulation tools. The focus will be on LTspice, which is widely used and available for free download for all contemporary (2016) Windows 7, 8, and 10 PCs. The LTspice examples have been developed for the current LTspice IV version of the software [1]. LTspice lends itself especially well to simulations of switch-mode power electronics circuits since it was designed to support Linear Technologies' family of products. This product line includes a large number of switch-mode power conversion parts. This manifests itself in the stability of the simulator during switching transitions. The author found the use of these examples is very beneficial in an educational environment, since the examples can be shared with students to enhance their understanding of the lecture material. The concepts and examples presented here can also be used for serious professional work. In fact, the author has used these tools with great success in many research projects. In addition to LTspice, PTC Mathcad [2] has been used to derive and present the underlying equations. Equations created in Mathcad look as perfect as in the best typesetting software, but they can also be evaluated numerically and manipulated symbolically to derive additional equations and to validate the underlying theory.

The software examples have been developed to illustrate advanced techniques for the simulation of power electronics and motor drives but not to teach the basic features of LTspice. For that, the reader shall be referred to the online documentation [1]. In addition, it is assumed that the reader is familiar with the basics of power electronics and electric machines, specifically AC induction machines. For a review, the reader shall be referred to [3] for power electronics and [4,5] for induction machines.

44.2 Use of Simulation Tools for Design and Analysis

It is appropriate to reflect upon the value of simulations and its place in the design and analysis process before any in-depth discussion of specific simulation examples. Computer simulations enable engineers to study the behavior of complex and powerful systems without actually building or operating them. Simulations therefore have a place in the analysis of existing equipment and the design of new systems. In addition, computer simulations enable engineers to safely study high-power circuits including abnormal operating conditions without actually creating such conditions in a real environment.

However, even the most advanced simulation software cannot perfectly represent all effects in real hardware. The accuracy of the results depends on the accuracy of the component models and the proper identification and inclusion of parasitic circuit elements such as parasitic inductance, capacitance, and mutual coupling. Discrepancies between simulation and experimental results often occur if the underlying assumptions for the device model have been exceeded. For example, an attempt to model transformer inrush with a transformer model that assumes linear magnetics would not yield useful results.

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In particular, the precise prediction of voltage and current traces during fast switching transitions in power electronics circuits has been proven to be difficult. To obtain useful results, extensive experimental validation, advanced device models (and the values for their parameters!), and detailed knowledge of parasitic elements, including the ones associated with the packaging of the circuit elements, are necessary. Therefore, the exact prediction of waveforms during switching transitions shall be excluded from the discussions in this chapter. Consequently, the author prefers to measure parameters such as voltage rise and fall times and over- and undershoot on actual circuitry in the laboratory.

Sometimes, users of spice-based simulators claim that the simulations of power electronics circuits with steep signal transitions are difficult due to convergence problems. However, with the proper techniques of gate signal generation, we can simulate just about any given circuit with little or no convergence problems in many spice-based tools. In addition, if convergence problems are avoided, simulations run much faster and larger numbers of individual transitions can be studied. This is achieved by generating gate signals using dependent sources with mathematical functions that produce switching signals that are differentiable throughout the transition. Being able to run simulations with a large number of transitions fast and without convergence problems gives a lot of insight into the cycle-by-cycle and the system level behavior of a power electronics circuit. An excellent application for these cycle-by-cycle simulations is the development and verification of control strategies for the power semiconductors in power electronics circuits.

Dependent voltage and current sources included in LTspice can be used to study large and complex systems like field-oriented (also called vector) control of induction machines if the proper mathematical control functions are used. Details are given below. In the examples for vector control of induction motors, the power electronics inverter is replaced with a dependent voltage source that represents the short-term average (filtering away the high-frequency voltage components associated with the switching frequency) of the output of a three-phase inverter. These examples represent system level simulations, which could have also been done using programs like MatLab/Simulink. However, circuit simulation software also provides the option of studying actual circuit level details in complex systems. To demonstrate this capability, the start-up of an induction motor, fed by a three-phase inverter with actual switch-mode operation, is presented.

In all modeling cases, the user needs to define the goal of the simulation effort. In other words, the user must answer the question "What information shall be obtained through the simulation of the circuit or system?" The user must then select the appropriate simulation software and the appropriate models. This process requires a detailed understanding of the properties and limitations of the device models and the sensitivity of the results to the limitations of the models. In order to obtain such an understanding, it is often recommended and necessary to perform numerous simulation test runs, carefully scrutinize the results, and compare them with measured data, results from other simulation packages, or otherwise known facts.

44.3 Simulation of Power Electronics Circuits With LTspice

The first example of a power electronics circuit is a step-down (also called buck) converter with synchronous rectification. For the purpose of synchronous rectification, the diode, which connects the inductor to ground in the regular circuit, is replaced with a power MOSFET transistor. The benefit of this circuit is that the power MOSFET represents a purely resistive channel in the on state. This channel does not have a residual, current independent, voltage drop like the p-n junction of a diode. Therefore, the voltage drop across the MOSFET can be much lower than what can be achieved with diodes. The results are reduced losses and increased efficiency. To achieve this, the lower MOSFET must be turned on whenever the upper MOSFET is turned off.

Fig. 44.1 shows a simulation setup for a synchronous buck converter. This converter steps down from 12 V input voltage to 3.3 V at the output. As mentioned before, the key element of this example is the circuit for the generation of the gate-drive signals for the MOSFETs. The basic principle of the operation of the gate-drive circuit is the well-known carrier-based scheme [3], where a control voltage is compared with a triangular carrier with fixed amplitude. The dependent voltage source *tri* on the left border of Fig. 44.1 generates the triangular carrier. Eq. (44.1) shown below gives the closed form equation for the triangular carrier wave. The output range of the function shown in Eq. (44.1) is between 0.0 and 1.0:

$$E_{\mathrm{tri}}(t) := \frac{1}{2} + \frac{1}{\pi} \cdot a\sin\left(\sin\left(2 \cdot \pi \cdot F_{\mathrm{SW}} \cdot t\right)\right) \tag{44.1}$$

For the generation of the gate-drive signals, the carrier wave is compared with a control signal that can have values between 0.0 and 1.0, corresponding to a duty cycle input between 0% and 100%. Dependent voltage sources *E_PWMa* and *E_PWMb* in Fig. 44.1 generate the PWM signals for the MOSFETs *M1* and *M2*, which are included in the LTspice library. A hyperbolic tangent function is used to create a PWM waveform with smooth transitions to aid in convergence. Fig. 44.2 shows a plot of a hyperbolic tangent function to illustrate the concept. The *Gain* parameter is used to steepen the curve to resemble realistic PWM signal transitions. In Fig. 44.2, the *Gain* is varied between 1 and 5. In the control functions for *E_PWMa* and *E_PWMb*, the factor 15 in front of the tanh function generates an output voltage that varies between −15 and +15 V. Note the inverse polarities on the inputs of sources *Dr1* and *Dr2* generate the complementary gate-drive signals.

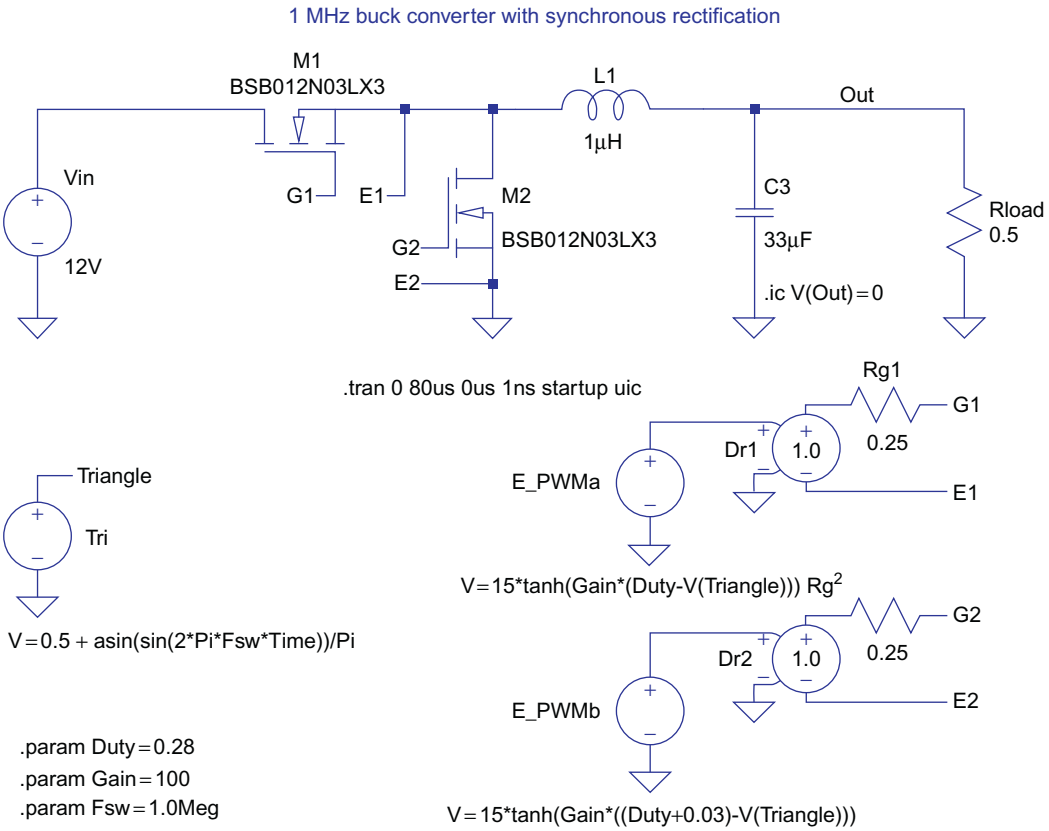


FIG. 44.1 LTspice simulation setup for a synchronous buck converter.

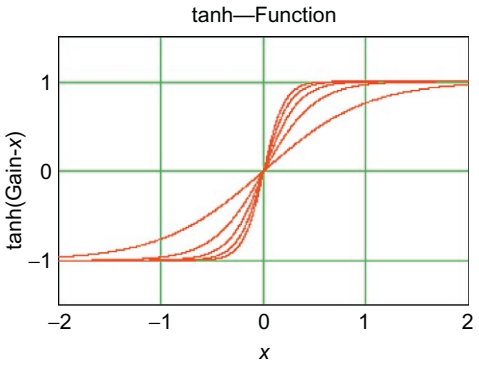


FIG. 44.2 Plot of a hyperbolic tangent function used to generate smooth PWM signals.

Careful inspection of Fig. 44.1 shows that 3% duty cycle *0.03* is added to generate the gate-drive signal of the lower (synchronous rectification) MOSFET to create some blanking time between the drive signals and avoid cross conduction between the MOSFETs *M1* and *M2*.

Fig. 44.3 shows the calculated voltage and current traces for the synchronous buck converter. The top-level pane shows the generated triangle carrier. It has a frequency (Fsw; see parameter statement in Fig. 44.1) of 1.0 MHz. The graph below the triangle signal shows the inductor current and the current in the load resistor. The bottom trace shows the capacitor voltage, which has a steady-state value of 3.3 V.

In addition to the cycle-by-cycle simulation of a DC-DC converter, it is also possible to use a time-averaged replacement for the MOSFET transistors used in the circuit in Fig. 44.1. In fact, a common time-averaged model can be used for the buck, the boost, the buck-boost, and the Cuk converter as long as they operate with continuous inductor current. The time-averaged model has the advantage that it can run much faster since it does not have to follow each switching transition. It is also possible to perform DC and AC sweep analyses. A DC sweep would sweep the duty cycle over a wide range and show the output voltage as a function of the duty cycle. An AC sweep analysis would sweep the frequency of an AC signal, which is superimposed on top of the duty cycle bias signal. The AC sweep allows the study of the behavior of the converter, including a feedback control system, in the frequency domain for traditional stability analysis and system tuning. A detailed description of this time-averaged modeling technique, including detailed examples, is given in [6].

To illustrate the capabilities of the LTspice simulation program, the next example shows a complete three-phase inverter using six power MOSFETs. This circuit is shown in Fig. 44.4.

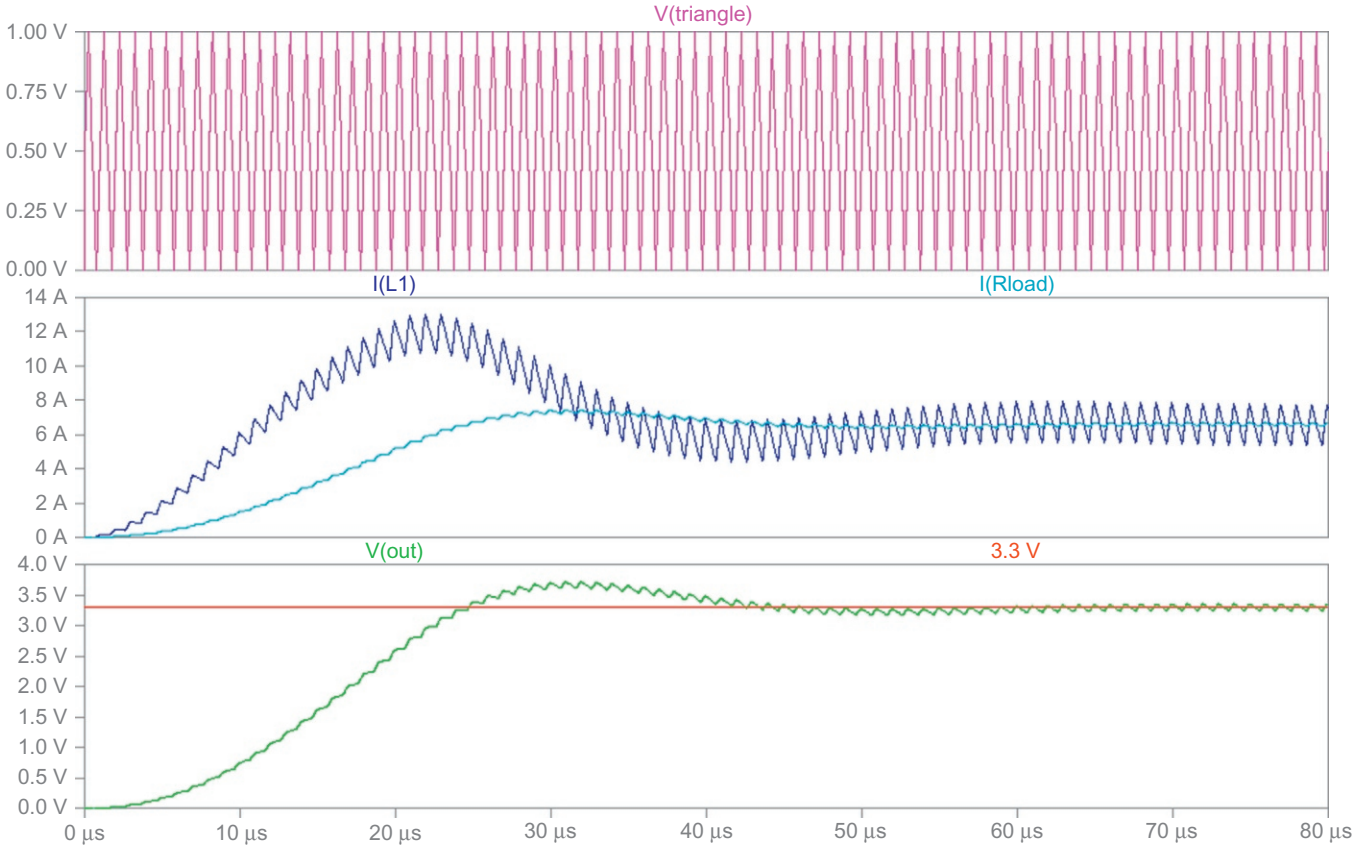


FIG. 44.3 Output waveforms for the synchronous buck converter.

Such an inverter needs antiparallel diodes connected across each power semiconductor to ensure that the load current can flow continuously. These diodes are often called freewheeling diodes. Here, the freewheeling diodes are an integral part of every power MOSFETs (body diodes) and are therefore not visible. The inverter drives a three-phase load, which represents the 5 hp induction motor used later. The R and L values represent rated load conditions. The load is connected to the inverter output terminals via labels (A,B,C).

Due to the number of elements involved, the circuit for the gate-drive signal generation is contained in a custom part named *PWM1*. Custom parts like this can easily be generated using the "Hierarchy—Create a New Symbol" menu path in the LTspice schematic editor. Double-clicking on the part reveals the associated subcircuit that is shown in Fig. 44.5. The arrow-shaped symbols on the right side of Fig. 44.5 named *G1*, *E1*, *G2*, etc. are called interface ports and are the outputs of the gate-drive circuit to the MOSFETs. These interface ports provide the connection between the subcircuit and the ports of the custom part. These ports on the custom part are created using the "Edit—Add Pin/Port" menu path in the LTspice schematic editor. The arrow-shaped symbols on the left side of Fig. 44.5 are inputs for the fundamental output frequency and the modulation index. The names of these ports in the subcircuit (must!) correspond to the names of the ports of the custom symbol.

The circuit shown in Fig. 44.5 is similar to the gate-drive generation circuit discussed before. As in the PWM generation circuitry shown in Fig. 44.1, a triangular carrier is compared with a reference signal. In this case, three reference signals, one for each phase, are compared with 3 PWM sources (*E_PWM_A*, *E_PWM_B*, and *E_PWM_C*) to create the gate-drive signals for all three phases. Again, the factor 15 in front of the tanh functions generates an output voltage that varies between −15 and +15 V for driving the gates of the MOSFETs. Here, the triangular carrier signal is symmetrical with respect to the time axis and covers the range from −1.0 to 1.0. The closed form expression for the triangular carrier is given by Eq. (44.2):

$$E_{\text{tri}}(t) := \frac{2}{\pi} \cdot a\sin\left(\sin\left(2 \cdot \pi \cdot F_{\text{SW}} \cdot t + \frac{\pi}{2}\right)\right) \tag{44.2}$$

The three reference signals are sinusoidal signals with equal amplitude and a relative phase shift of 120°. For linear modulation, the amplitude range of the reference signals is limited to the amplitude of the triangular carrier, for example, 1 V. The ratio of the reference wave amplitude and the (fixed) carrier amplitude is called amplitude modulation ratio *Mod*. In the

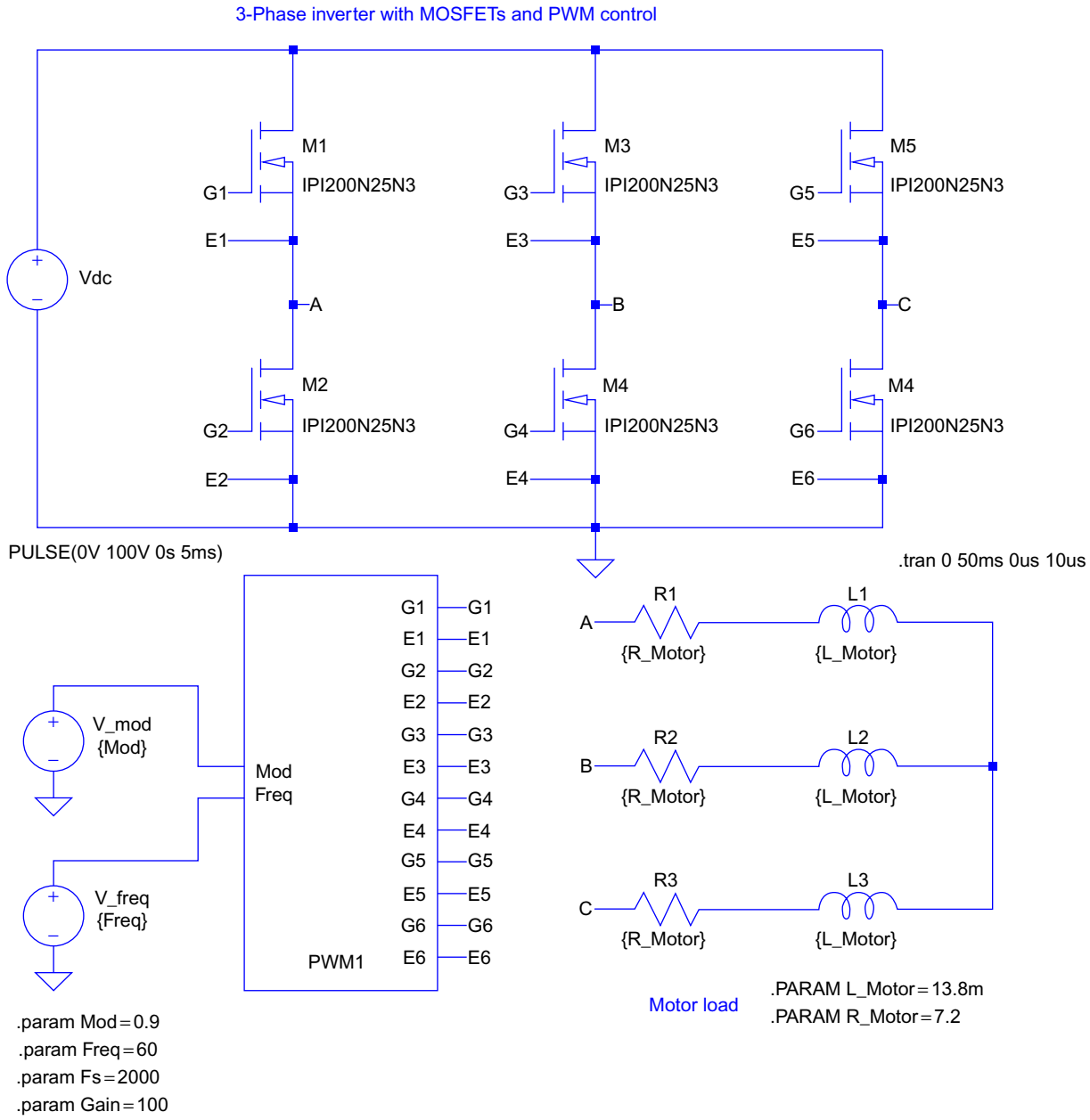


FIG. 44.4 Circuit for a three-phase inverter with MOSFETs.

circuit shown in Fig. 44.4, *Mod* has a value of 0.9. This value is defined by a parameter symbol at the top level and therefore represents a global parameter, which is visible throughout all levels of the hierarchy. The amplitude of the phase-to-neutral voltage of each inverter leg is equal to half of *Vdc* (shown in Fig. 44.4) multiplied with the amplitude modulation ratio. The frequency and wave shape of the phase-to-neutral voltage of each phase leg is equal to the reference waveform if the high-frequency components resulting from the carrier wave are filtered away. Each inverter leg can be viewed as a power amplifier for its reference voltage. In fact, in drive applications, inverters are often called "servo-amplifiers." The load typically reacts only to the low-frequency components of the inverter output voltage. The high-frequency components, which include the triangular carrier frequency (also called switching frequency) and its harmonics, are typically "just a blur" for the load. These are especially true in recent times, where switching frequencies of 20 kHz and above are possible. As an added benefit, audible noise is avoided at these frequency levels.

The complementary sources *Dr1/Dr2*, *Dr3/Dr4*, and *Dr5/Dr5* in combination with the gate resistors will generate the control voltages for the transistor pairs of each leg. Using this circuitry will ensure that during switching transitions in each

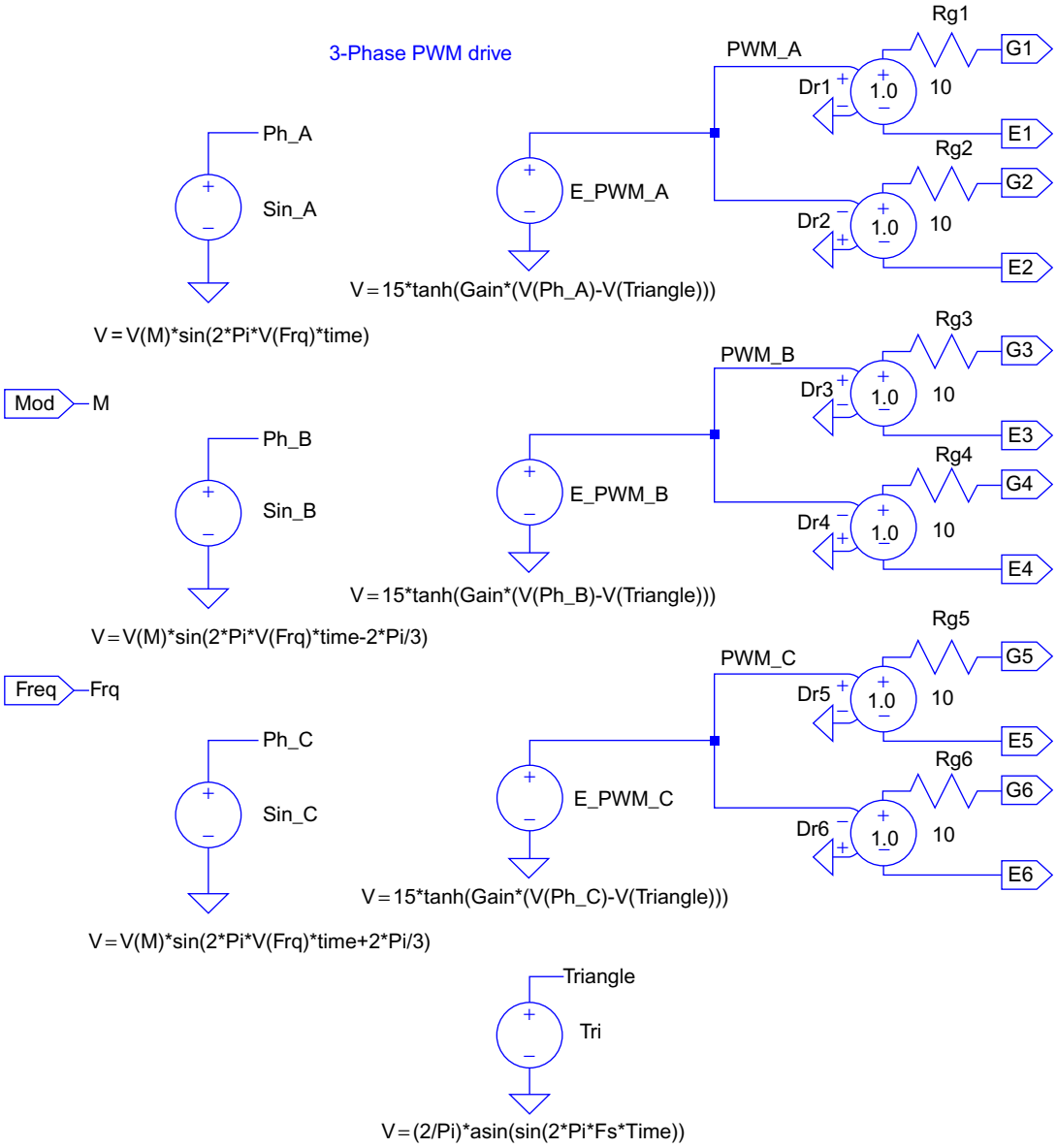


FIG. 44.5 PWM generation subcircuit for a three-phase MOSFET inverter.

phase leg, the gate voltage of the transistor that is turning off will fall below the turn-on threshold before the gate voltage of the transistor that is turning on reaches that threshold. Therefore, a shoot through, meaning a short circuit between the positive and negative bus, is avoided.

Fig. 44.6 shows the simulation results for the three-phase inverter. The timescale is slightly stretched, to better show the details of the PWM signals. The line-to-line voltage V_{AB} and the load current in all three phases are shown. Due to the inductors contained in the load, the current cannot instantaneously change and follow the PWM signal. Therefore, the load currents are almost pure sinusoids with very little ripple. This is representative of the real line currents in induction motors.

Fig. 44.7 shows an example where the MOSFETs in Fig. 44.4 have been replaced with insulated gate bipolar transistors (IGBTs). The spice model of the particular IGBTs shown here is included on the right side of the schematic. Note that freewheeling diodes are needed, if IGBTs are used. The freewheeling diodes carry the load current when the IGBTs are turned off to provide a continuous path for the current. This is very important, since the load can have a substantial inductive component. Whenever the diodes are conducting, energy flows momentarily back to the source. In the case of power MOSFETs, the diodes (often called body diodes) are an integral part of the device. In the symbol graphic of LTspice, these body diodes are not shown for MOSFETs. For this circuit, the gate-drive circuit and the results are the same as for the

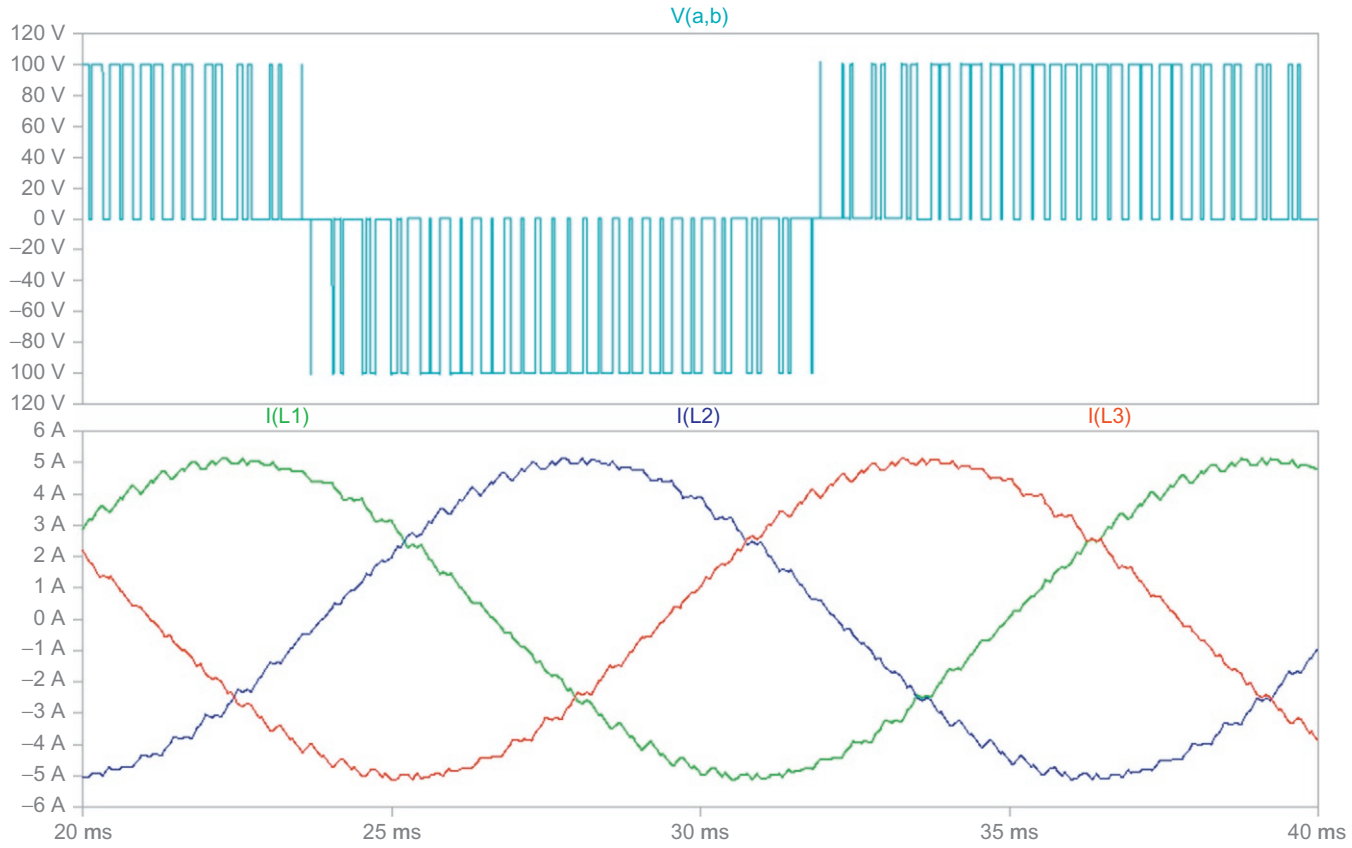


FIG. 44.6 Output waveforms of the three-phase inverter with MOSFETs.

three-phase inverter with power MOSFETs. This circuit returns the same results than the one shown in Fig. 44.6 except that the simulation runs a lot longer (minutes rather than seconds) due to the complexity of the IGBT models.

44.4 Simulations of Power Electronic Circuits and Electric Machines

In the following, the start-up of an induction motor, fed by a three-phase inverter similar to the ones shown in Figs. 44.4 and 44.7, is presented. For this purpose, the simple passive load in Figs. 44.4 and 44.7 has been replaced by a complete dynamic model of an induction motor. Also, the MOSFETs or IGBTs from Figs. 44.4 and 44.7, respectively, have been replaced by generic voltage-controlled switches. This will increase the simulation speed even more dramatically compared with the case with IGBTs with very little effect on accuracy since this simulation is meant to study the start-up behavior of an induction motor. For this and further discussions, it is assumed that the reader is familiar with the theory of induction machines and in particular their dynamic behavior. A number of excellent references are given at the end of this chapter [4,5,7,8]. The induction motor symbol represents the electromechanical model of an induction motor. The model is suitable for studies of electric and mechanical transients and steady-state conditions. The output pin on the motor shaft represents the mechanical output. The voltage on this pin represents the mechanical angular velocity using the relation 1 V = 1 rad/s. In addition, any current drawn from or fed into this terminal represents applied motor or generator torque according to the relation 1 A = 1 N m. Due to these definitions, the electric power associated with the voltage of the motor shaft (with respect to ground) is identical to the mechanical power. Following the well-known theory, the induction motor model has been derived for a two-phase (direct and quadrature, D, Q) equivalent motor. Attached to the motor is a bidirectional two-phase to three-phase converter module. This module is voltage and current invariant. This means that the voltage and current levels in the two-phase and the three-phase machine are equal. Consequently, the power in the two-phase machine is only two-thirds of the power in the three-phase circuit. This is accounted for in the calculation of the electromagnetic torque (factor 3/2; see Eq. (44.4)). The internally generated torque can be monitored on the output labeled *Torque* on top of the sleeve around the motor shaft. The linear load in Fig. 44.8 is a symbol that represents an appropriately

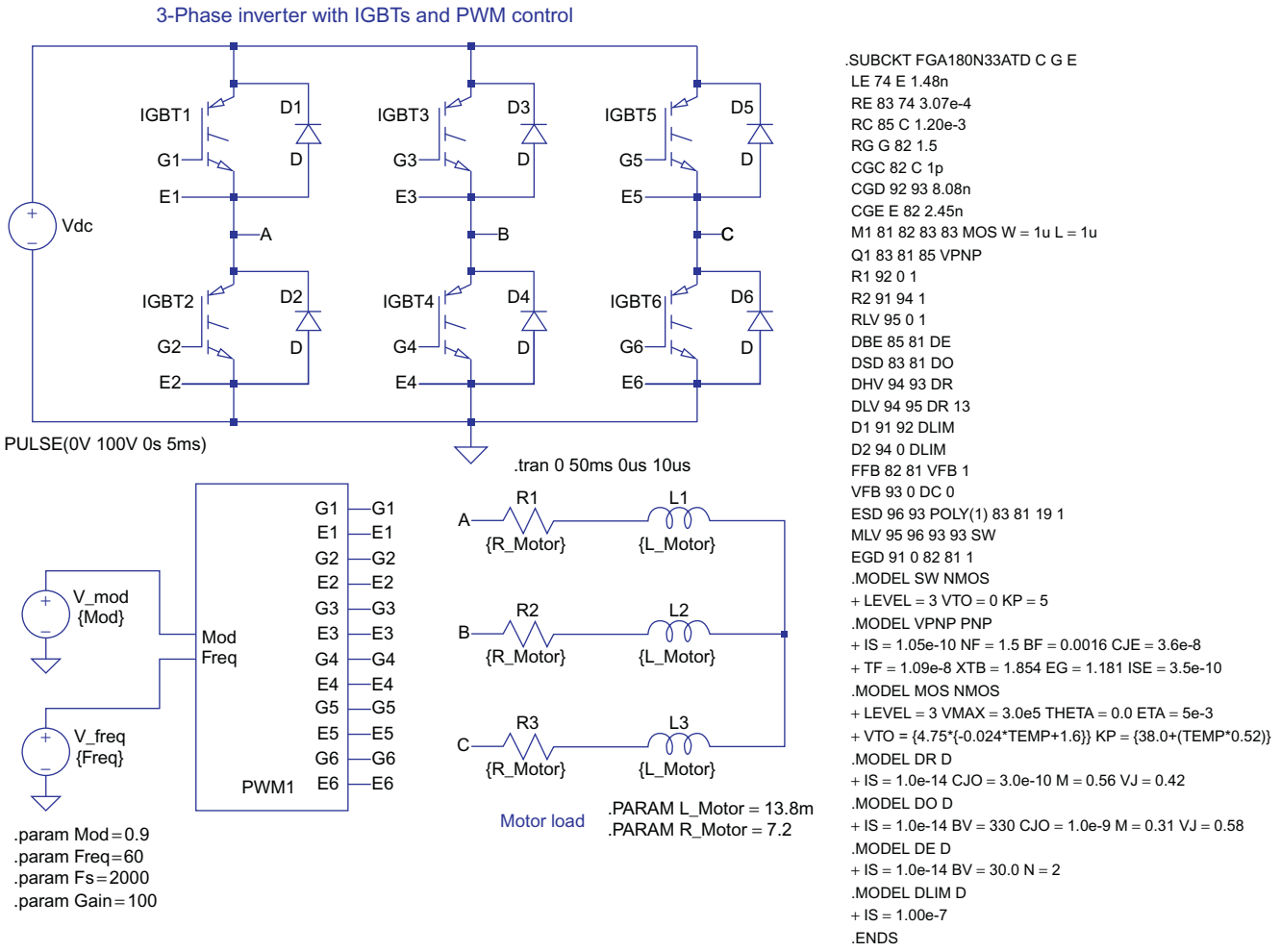


FIG. 44.7 Three-phase inverter circuit with IGBTs.

sized resistor to the ground representing rated power that is 5 hp for this example.

In Fig. 44.8, the motor is represented by a custom symbol called *induction machine*. The symbol can be easily created using the "Hierarchy—Create a New Symbol" menu path in the LTspice schematic editor. The editor provides standard graphic elements (lines, rectangles, circles, etc.) so that professional-looking symbols can easily be created.

Double-clicking on the motor symbol reveals the associated subcircuit that implements its function. This subcircuit is shown in Fig. 44.9. The left part of this subcircuit represents the electric model. The electric model calculates the stator and rotor currents, with the stator voltages and the mechanical speed of the machine being input parameters. However, it is also possible without any changes to feed stator currents (with controlled current sources) into the D and Q inputs. This option is useful for vector control applications, which are discussed later.

The equation system for the electric model of a two-phase induction machine is given by Eq. (44.3). The theory for this equation system is derived in [4,5,7,8]. The equation system and the model are formulated for the stationary reference frame. This reference frame assumes that the frame of the machine is stationary and the voltages and currents of the rotor are equivalent AC values with stator frequency.

From machine theory, we know that the actual rotor currents have slip frequency. Another reference frame is the synchronous (also called excitation) reference frame. In this reference frame, the stator of a fictitious machine is assumed to rotate with synchronous speed. The advantage of this reference frame is that the input frequency is zero (DC), which makes it easy to derive the principle of vector control by extending the theory of DC machines to AC machines:

$$\begin{bmatrix} V_d \\ V_q \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} R_{stat}+pL_s & 0 & pL_m & 0 \\ 0 & R_{stat}+pL_s & 0 & pL_m \\ pL_m & \omega_e L_m & R_{rot}+pL_r & \omega_e L_r \\ -\omega_e L_m & pL_m & -\omega_e L_r & R_{rot}+pL_r \end{bmatrix} \begin{bmatrix} I_{sd} \\ I_{sq} \\ I_{rd} \\ I_{rq} \end{bmatrix}$$

$$L_s = L_m + L_{s1} \qquad L_r = L_m + L_{r1} \quad p = \frac{d}{dt} \tag{44.3}$$

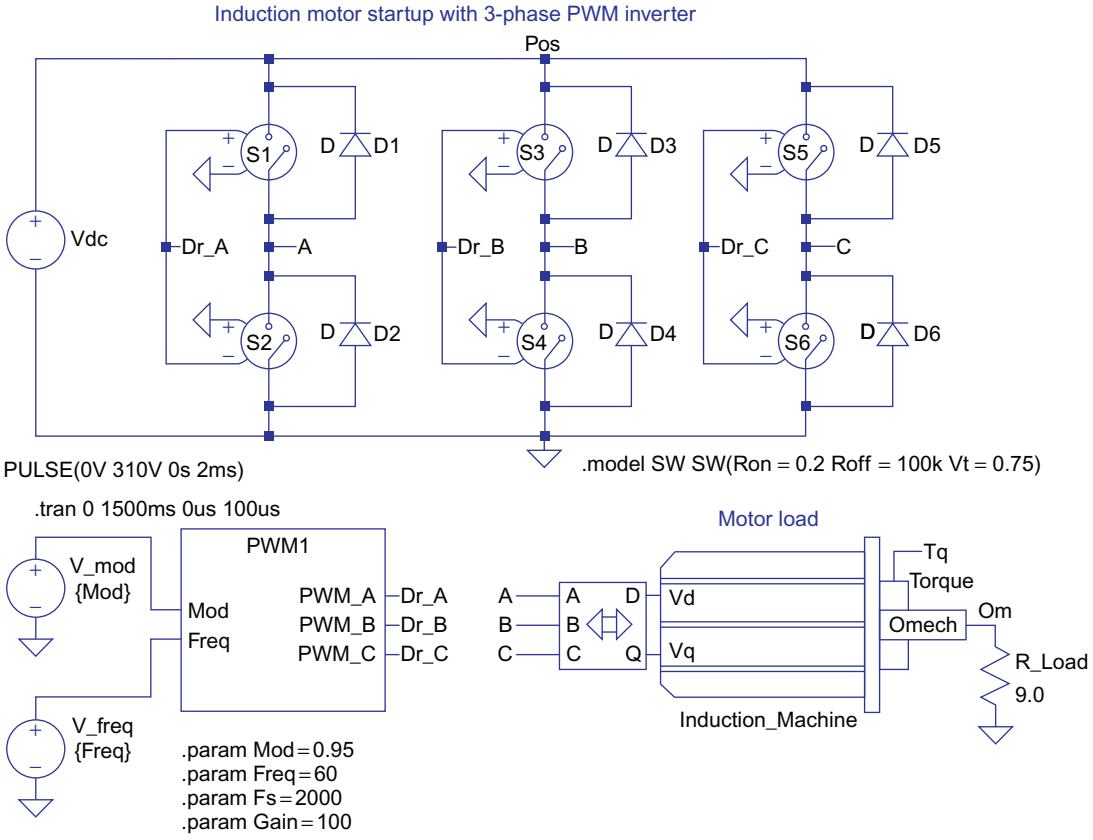


FIG. 44.8 Induction motor start-up with three-phase inverter circuit.

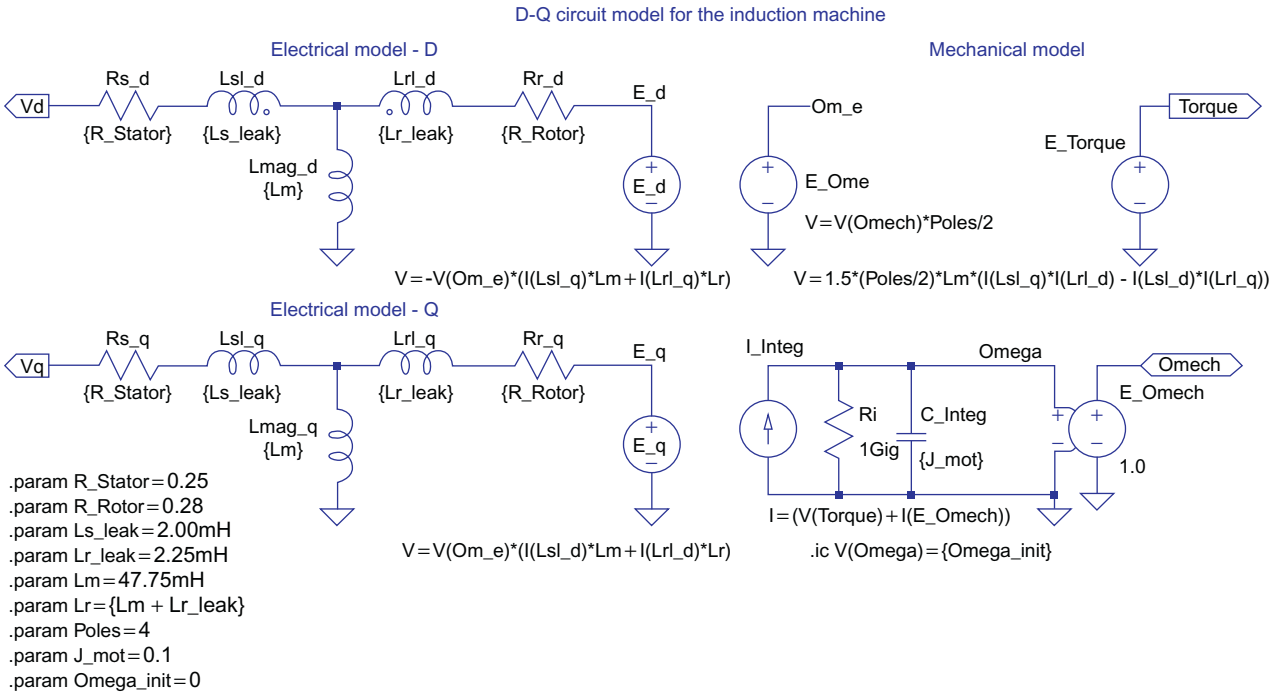


FIG. 44.9 Subcircuit for induction motor model.

In typical implementations of vector control using digital signal processors (DSPs), the synchronous reference frame is used internally to calculate the reference values for the currents in the D- and Q-axis. These values are then transformed to the stationary reference frame in an additional step. Sometimes, still other reference frames are used, and it is possible to generate a universal electric model with a reference frame speed input. This model could then be used for any reference frame.

The electric model in Fig. 44.9 implements the equation system shown in Eq. (44.3). The circuit closely resembles the well-known T-equivalent circuit for the steady-state analysis of induction machines. Two instances of the T-equivalent circuit are necessary to implement the two-phase (D, Q) model. The right part of the schematic in Fig. 44.9 represents the mechanical model. This circuitry calculates the internally generated electromagnetic torque, using the rotor and stator currents as input values. The equation for the internal electromagnetic torque of the induction machine is given by Eq. (44.4) [4,5,7,8]. The factor 3/2 accounts for the fact that the real motor is a three-phase machine. The generated torque is used to calculate the angular acceleration of the motor shaft considering the load torque and the moment of inertia. Integration of the angular acceleration yields the rotor speed, which is used in the electric model:

$$T = \frac{3}{2}\frac{P}{2} L_m \left(I_{sq} I_{rd} - I_{sd} I_{rq}\right) \tag{44.4}$$

Since almost all induction machines are three-phase machines, it is often desirable to have a machine model with a three-phase input. Therefore, a bidirectional two-phase to three-phase converter module, which can be attached to the motor, has been developed. A subcircuit for this module is shown in Fig. 44.10.

This circuit is truly bidirectional, meaning that the circuit can be fed with voltage or current sources from either side. The equation system for this voltage and current-invariant transformation is given by Eq. (44.5). This transformation is sometimes called "Clark" or "ABC-DQ" transformation. The voltage V_0 in Eq. (44.5) denotes a zero-sequence voltage, which is assumed to be zero and not implemented in the subcircuit shown in Fig. 44.10. This voltage would only have nonzero values for unbalanced conditions. An interesting detail of the subcircuit in Fig. 44.10 is the addition of high-value resistors on each input. These resistors provide a small current path from the three-phase input to the ground and ensure stable operation if the module is fed with current sources;

$$\begin{bmatrix} V_d \\ V_q \\ V_o \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ 0 & \sqrt{3} & -\sqrt{3} \\ 1 & 1 & 1 \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}$$
$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \frac{1}{2}\begin{bmatrix} 2 & 0 & 2 \\ -1 & \sqrt{3} & 2 \\ -1 & -\sqrt{3} & 2 \end{bmatrix}\begin{bmatrix} V_d \\ V_q \\ V_o \end{bmatrix} \tag{44.5}$$

Fig. 44.11 shows the result for the start-up of the induction motor for the circuit of Fig. 44.8. The motor is a 5 hp, 208 V, 4-pole machine. The detailed parameters are shown in Table 44.1. The PWM generation was derived from the example shown in Fig. 44.4. The top trace in Fig. 44.11 shows the mechanical angular velocity with a scale of 1 V = 1 rad/s. The middle trace shows the developed electromagnetic torque, including the level for the rated steady-state torque (20 N m as commanded by the load in Fig. 44.8) and the zero level. This graph shows the typical oscillatory torque production of the induction machine for an uncontrolled line start. The scale for this graph is 1 V = 1 N m. The bottom trace of Fig. 44.11 shows the input current for phase A.

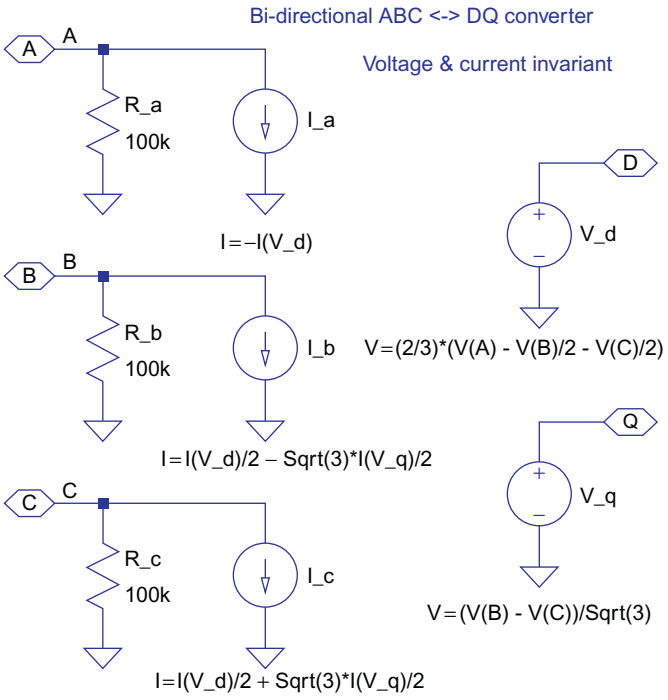


FIG. 44.10 Subcircuit for the ABC-DQ transformation module.

It is evident that the current trace is an almost perfect sinusoid, despite the fact that the input voltage is a PWM waveform. Also, the trace for the torque shows only a small high-frequency ripple. The reason is, of course, that the motor windings are inductive and represent a low-pass filter for the applied voltages. Nevertheless, recent research suggests that filtering the output voltage of the inverter is advantageous anyway, because it significantly reduces the voltage stress on the windings and suppresses displacement currents through the bearings [9].

44.5 Simulations of AC Induction Machines Using Field Oriented (Vector) Control

The following examples will demonstrate the use of LTspice for simulations of field-oriented control (FOC) of AC induction machines. Again, it is assumed that the reader is familiar with the basics of induction machine theory. Often times, FOC is



FIG. 44.11 Induction motor start-up with three-phase inverter circuit.

TABLE 44.1 List of all attributes used for the 5 hp, 208 V, 4-pole induction motor

Attributes
R_Stator = 0.25 Ω
R_Rotor = 0.28 Ω
Ls_leak = 2.00 mH
Lr_leak = 2.25 mH
Lm = 47.75 mH
Ls = Lm + Ls_leak
Lr = Lm + Lr_leak
kT = 1.5*(Poles/2)*Lm/Lr
Tau_r = Lr/R_Rotor
Sigma = 1 − Lm*Lm/(Ls*Lr)
Poles = 4
J_mot = 0.1 kg m^2
Omega_init = 0

also called vector control, and both expressions can be used interchangeably. The theory of vector control is described in detail in [4,7,8]. The idea was originally proposed in the 1960s by Hasse and Blaschke, working at the Technical University of Darmstadt [10]. The author had the privilege of taking one of Prof. Hasse's classes on machine control as an undergraduate student. The basic idea of FOC is to inject currents into the stator of an induction machine such that the magnetic flux level and the production of electromagnetic torque can be independently controlled and the dynamics of the machine resembles that of a separately excited DC machine. The previously discussed two-phase model for the induction machine is very helpful for studies of vector control and shall be used in all examples. If a two-phase induction motor model for the synchronous (or excitation) reference frame is used, the similarities between the control of a separately excited DC machine and vector control of an AC induction machine will be most evident. In this case, the D input corresponds to the field excitation input of the DC machine, and both inputs are fed with DC current. Assuming unsaturated machines, the current into the D input of the induction machine or the field current in the DC machine directly controls the flux level. The Q input of the induction machine would correspond to the armature winding input of the DC machine, and again, both inputs would receive DC current. These currents would directly control the production of electromagnetic torque with a linear relation (constant k_T) between the current level and the torque level. Furthermore, the Q component of the current would not change the flux level established by the D component (no cross coupling). To make such a simulation work, it would finally be necessary to calculate the slip value that corresponds to the commanded torque and use this value to calculate the speed of the synchronous reference frame of the machine model.

Of course, this is very interesting from an academic standpoint, and the author uses this example in a semester-long lecture on machines and drives. However, it should again be noted that a machine represented by a model with a synchronous reference frame would have a stator, which rotates with synchronous speed. Of course, this is not realistic, and therefore, it is more interesting to generate a simulation example that uses the previously discussed motor model for the stationary reference frame. This motor must be supplied with AC voltages and currents with a frequency determined mostly by the rotor speed and to a small extent (slip value) by the commanded torque. We still compute DC values representing the commanded flux and torque, but we transform these DC values to appropriate AC values. In the following example, we will assume that we can measure the actual rotor speed with a sensor. For this purpose, many types of sensors are available on the market. If we add the slip speed to the measured rotor speed, we obtain the synchronous speed for the given operating point. We determine the slip speed from the torque command. With this synchronous speed, we can transform the DC flux and torque command values from the synchronous reference frame to the stationary reference frame. We accomplish this by using a rotational transformation according to the matrix equations in Eq. (44.6). This rotational transformation is also called "Park" transformation. As shown in Eq. (44.6), the transformation is bidirectional, and the product of the transformation matrices yields the unity matrix:

$$\begin{bmatrix} V_{Dout} \\ V_{Qout} \end{bmatrix} = \begin{bmatrix} \cos(\rho) & -\sin(\rho) \\ \sin(\rho) & \cos(\rho) \end{bmatrix} \begin{bmatrix} V_{Din} \\ V_{Qout} \end{bmatrix}$$
$$\begin{bmatrix} V_{Dout} \\ V_{Qout} \end{bmatrix} = \begin{bmatrix} \cos(\rho) & \sin(\rho) \\ -\sin(\rho) & \cos(\rho) \end{bmatrix} \begin{bmatrix} V_{Din} \\ V_{Qout} \end{bmatrix} \tag{44.6}$$
$$\begin{bmatrix} \cos(\rho) & -\sin(\rho) \\ \sin(\rho) & \cos(\rho) \end{bmatrix} \begin{bmatrix} \cos(\rho) & \sin(\rho) \\ -\sin(\rho) & \cos(\rho) \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$$

For the following discussion, we shall define the transformation that produces AC values from DC inputs as a positive vector transformation and the reverse operation consequently a negative vector transformation. The matrix equation for the positive vector transformation is shown on the left side of Eq. (44.6). The negative transformation is very useful to extract DC values from AC voltages and currents for diagnostic and feedback control purposes. Both rotational transformations use the angle, α, in the equations. This angle can be interpreted as the momentary rotational displacement angle between two Cartesian coordinate systems, one containing the input values and the other the output values. This angle is obtained by integration of the angular velocity with which the coordinate systems are rotating (typically the synchronous speed).

In summary, we replaced a theoretical motor model using a synchronous reference frame by a reference frame transformation of the supply voltages and currents. In fact, modern DSPs are capable to perform both the Clark and the Park transformations in both directions at very high speeds. These DSPs are well supported with proved reference designs, including free software examples.

Fig. 44.12 shows the top level of a simulation example that implements vector control for an induction machine with a stationary reference frame model. The motor model and the associated subcircuits (Fig. 44.9) are identical to the ones used for the circuit shown in Fig. 44.8. As discussed above, the actual speed of the rotor is used as an input signal for the control unit. This scheme is known as indirect vector control and represents one of the most often used control methods. The symbol for the controller uses the same parameters as the motor. This is necessary to achieve correct field orientation. In real systems, the controller must be told or somehow determine the machine parameters. The machine parameters are contained in *.param* statements. If these *.param* statements are used at the top level of the hierarchy, they are global to the simulation, but if they are contained in a subcircuit, they are local to that subcircuit. Here, the vector controller and the induction motor

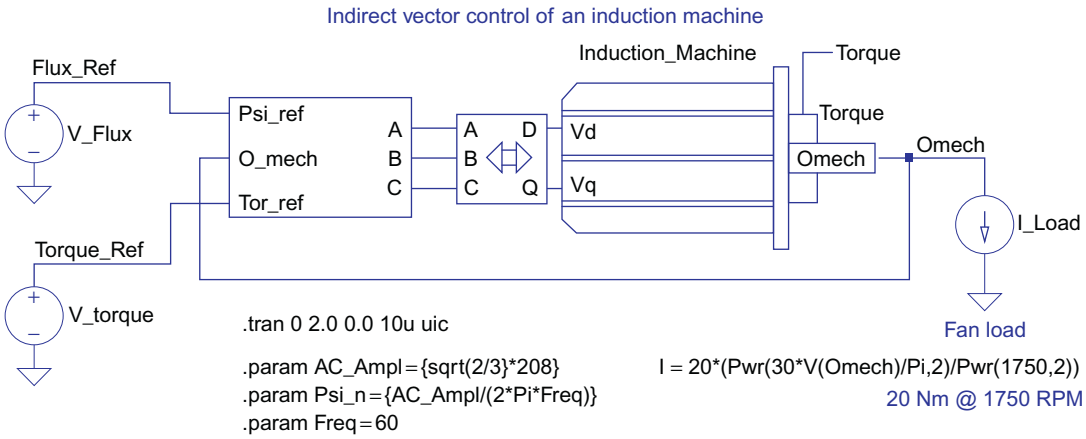


FIG. 44.12 Top-level circuit for indirect vector control of induction motors.

both have local parameters, which enables us to study the influence of parameter mismatch on the performance of the control.

Fig. 44.12 shows a dependent current source that represents a fan load for the motor. The current of this source represents the load torque and is proportional to the square of the mechanical speed of the motor shaft. That speed is represented by the voltage on the *Omech* terminal. The controlling equation is scaled such that the load draws the rated torque (20 A = 20 N m) at rated speed (1750 RPM). In this fashion, many more mechanical properties and devices can be modeled. For example, a mechanical flywheel is simply represented by a capacitor to the ground. Due to the scaling factors for the angular velocity and the torque, a flywheel with $J = 1$ kg m^2 would be a capacitor with a value of $C = 1$ F. The compliance of a driveshaft (elastic twisting by the applied torque) can be modeled by a series inductor. By including both capacitors and inductors, effects like mechanical resonance can be included in a model.

Fig. 44.13 shows the subcircuit for the vector control unit. The central part is a vector rotator for positive direction. This element transforms the DC reference values for the flux (D-axis) and the torque (Q-axis) to the stationary reference frame. The input angle for the vector rotator is the integral of the synchronous angular velocity. The signal called *Omech* is the measured rotor speed. The subcircuit for the vector rotator is shown in Fig. 44.14.

This speed is multiplied with the number of pole pairs (*poles*/2) to obtain the electric angular velocity. Then, the slip value (see Eq. (44.7) for slip frequency calculation for vector

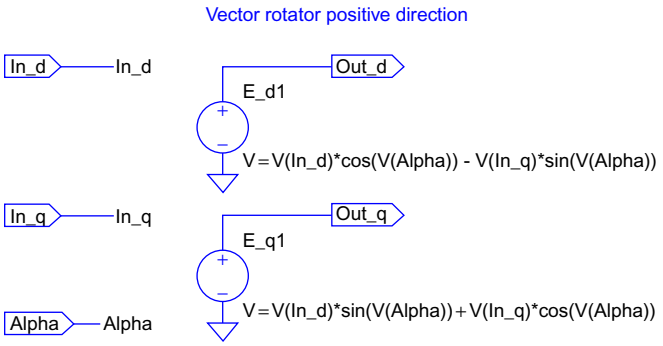


FIG. 44.14 Schematic for subcircuit for vector rotator.

control) appropriate to the torque command is added, and the resulting signal is routed through an integrator to generate the input angle for the vector rotator.

In the D-axis, a differentiator function *DDT(V(Id_ref))* is used in a compensation element (see Eq. (44.8) for D-axis reference current for vector control) that assures that the actual flux in the machine follows the commanded signal without delay. The input and output values of the vector rotator are voltage signals that correspond 1:1 to current signals. (In a real controller, the currents are typically scaled values in the memory of a DSP.) The vector controller calculates the appropriate currents that need to be injected into the machine to perform as desired. The currents are then transformed into three-phase values using the equations of (44.5) and fed into three voltage

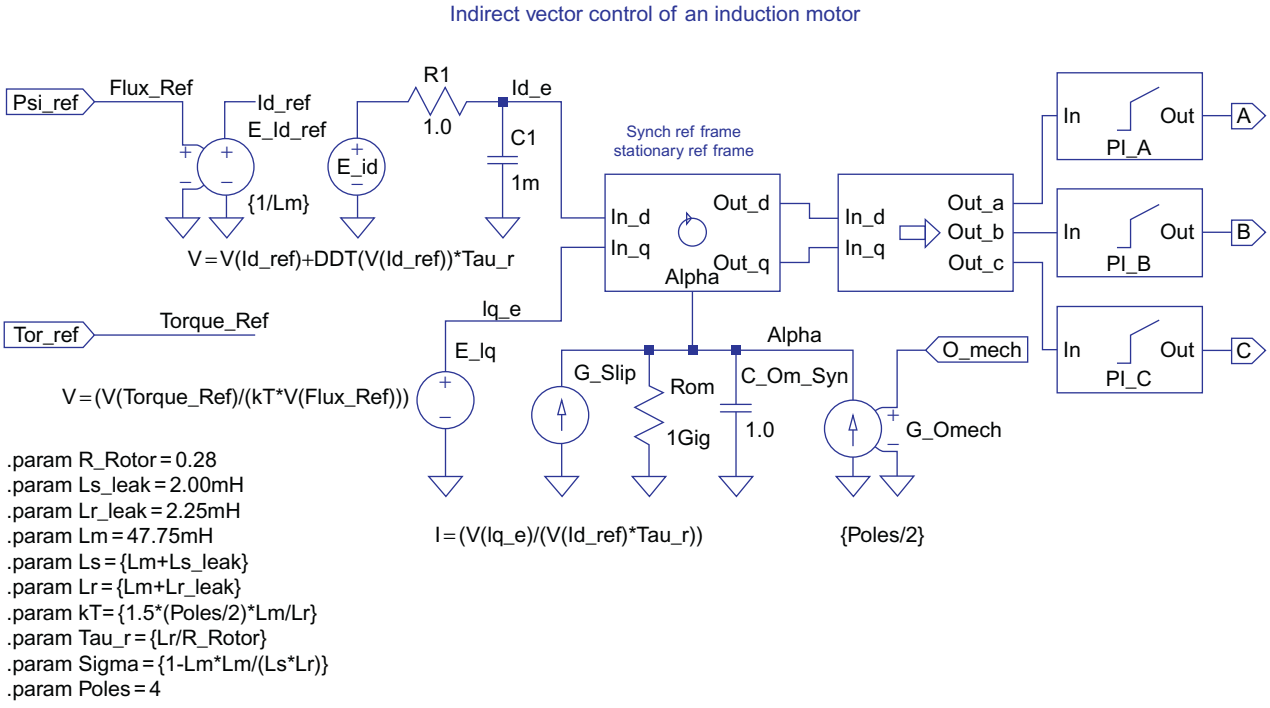


FIG. 44.13 Subcircuit for indirect vector control of induction motors.

sources with PI current loop feedback that represents a realistic implementation using a voltage-source PWM inverter. Alternatively, the PI current loops could be replaced with ideal current sources that are available in LTspice:

$$\omega_{slip} = L_m \frac{I_{sq}}{\tau_r \lambda_{rd}} \tag{44.7}$$

$$I_{sd} = \frac{(\lambda_{rd} + \tau_r \lambda_{rd} p)}{L_m} = \frac{1 + \tau_r p}{L_m} \lambda_{rd} \quad p = \frac{d}{dt} \tag{44.8}$$

Fig. 44.15 shows the results obtained for the circuit shown in Fig. 44.12 with perfect tuning of the vector controller. Perfect tuning means that the controller precisely knows all motor parameters at all times (including resistance changes due to heating of the windings). The two traces in the pane at the top of Fig. 44.15 represent the traces for the D and Q input signals of the vector rotator. The upper trace in the bottom pane of Fig. 44.15 shows the reference value for the flux scaled by a factor of 50. It is evident that the flux level is being changed at the same time when 20 N m of torque is commanded (and produced). This proves that with exact tuning the torque and the flux can be independently controlled, which is true for correct FOC. Below the trace for the flux reference are the traces for the torque reference and the actual torque, which are perfectly on top of each other. This provides the easiest way to judge the quality of the correct field orientation.

The center pane shows the trace for the mechanical angular velocity. It can be seen that the machine accelerates whenever torque is developed and slows down due to the load when the torque command is driven to zero.

Fig. 44.16 is an example of the results obtained from a detuned vector controller. The circuit is identical to the circuit in Fig. 44.12, except for the fact that the rotor resistance value in the controller was increased to 125%, which is thought to be attributed to heating of the rotor bars. It is obvious that the traces for the commanded and the actually produced torque are no longer identical. This is especially true, during times when the flux is changing. Detuning is actually a real problem in industrial vector control applications. Detuning is caused by the fact that the machine parameters are not precisely known to begin with and/or are changing during the operation of the machine. The values of the winding resistance are most commonly increasing due to heating of the machine during operation at high load.

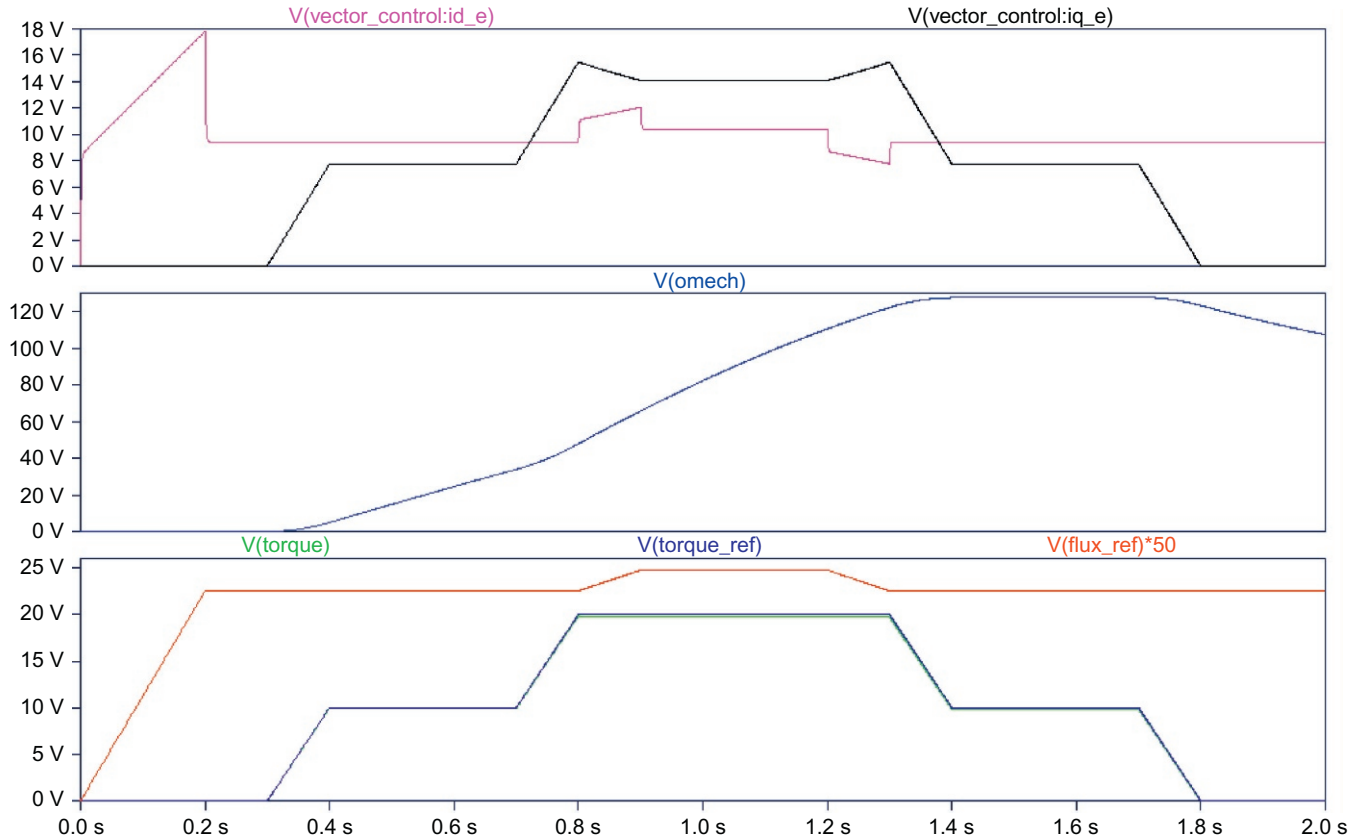


FIG. 44.15 Results for indirect vector control with perfect tuning.

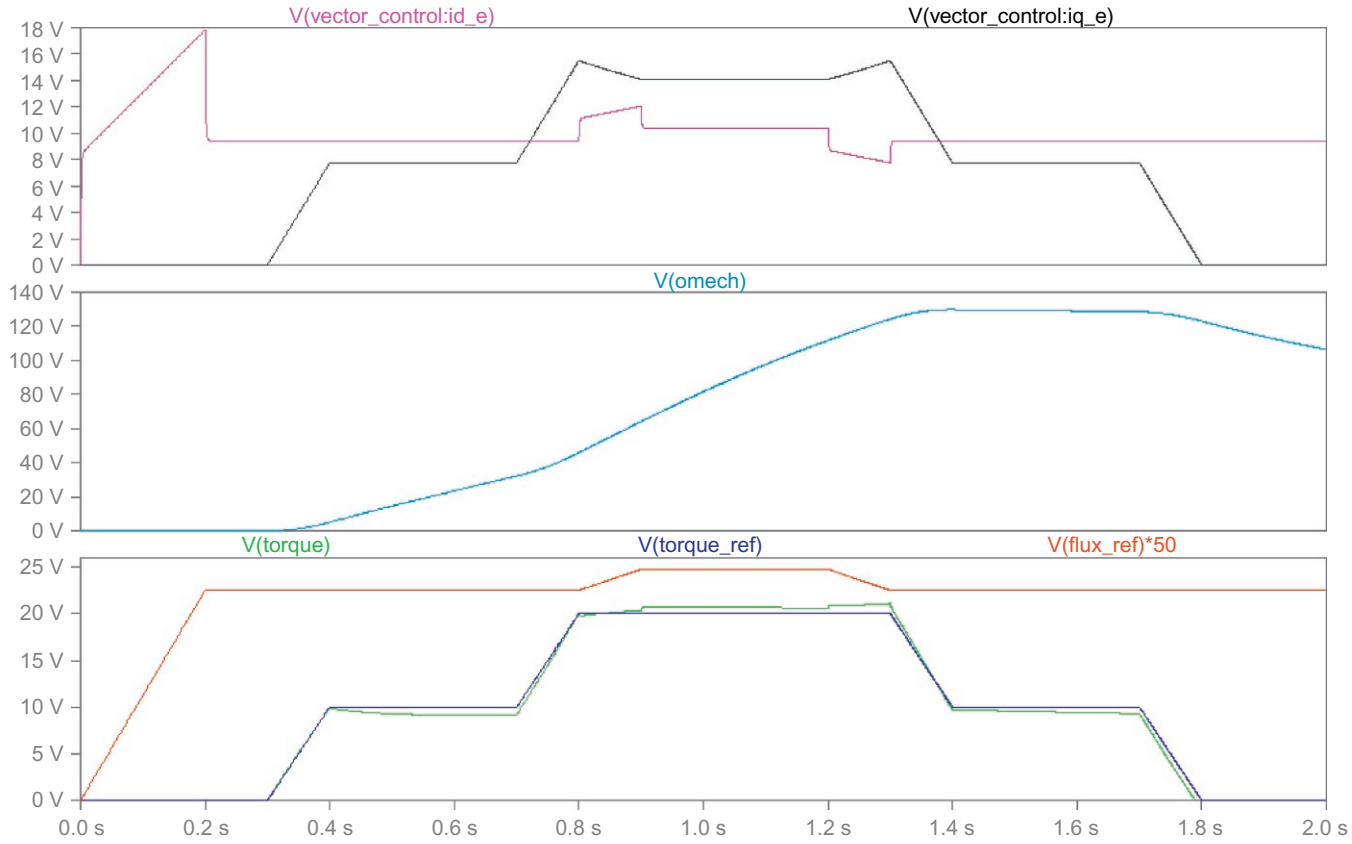


FIG. 44.16 Results for indirect vector control with 125% rotor resistance resulting in imperfect tuning.

44.6 Simulation of Sensorless Vector Control Using LTspice

In the previous example, the advantages of vector control have been shown. However, for the implementation of the control scheme, a sensor for the mechanical speed was used. This poses a problem for applications where a vector drive is to be retrofitted into existing equipment. The motor installation may not easily allow the installation of a mechanical speed sensor. Therefore, engineers have thought to replace the mechanical speed sensor with a speed observer, which is a mathematical model that is evaluated by the control processor (typically a DSP), which is also performing the standard vector control computations. The algorithm for the observer uses the measured stator voltages and currents for the D- and Q-axes as input parameters. It also relies on the knowledge of the machine model and on the correct machine parameters (rotor and stator resistance, mutual and leakage inductance, etc.). The following example shows a vector control implementation using a speed observer. The vector controller has been derived from the previous example shown in Fig. 44.13. However, the speed sensor signal was replaced by a speed observer. Careful examination of the derivation [4] of the speed observer reveals that it is easier to calculate the synchronous angular velocity, which is ultimately desired, than the angular velocity of the rotor. Therefore, the observer was modified, and the calculation of the rotor speed and the subsequent addition of the slip speed were foregone. The speed observer used here basically solves the D, Q equation system of the induction machine shown in Eq. (44.3), with the only difference that some of the dependent variables are now independent and vice versa. In addition to the synchronous angular velocity, the observer provides the values of the rotor flux, which could be used in the D-axis signal path.

Fig. 44.17 shows the top level of a simulation project for sensorless vector control. The top view of this circuit is very similar to the circuit for the indirect vector control represented by Fig. 44.12 except for the missing motor-speed feedback. The model for the motor and the motor's parameters are precisely the same as in the example for the indirect vector control. Double-clicking the control block reveals the associated subcircuit, which is shown in Fig. 44.18. As mentioned before, this subcircuit is similar to the subcircuit for the indirect vector control. However, the signal from the motor-speed sensor is replaced by the speed observer. In our case, the speed observer directly provides the synchronous angular velocity. Therefore,

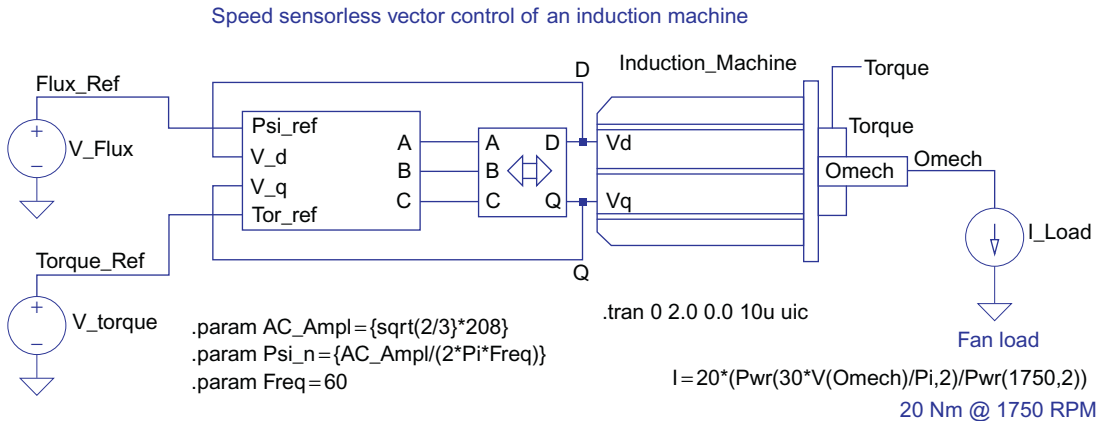


FIG. 44.17 Top level of simulation circuit for sensorless vector control.

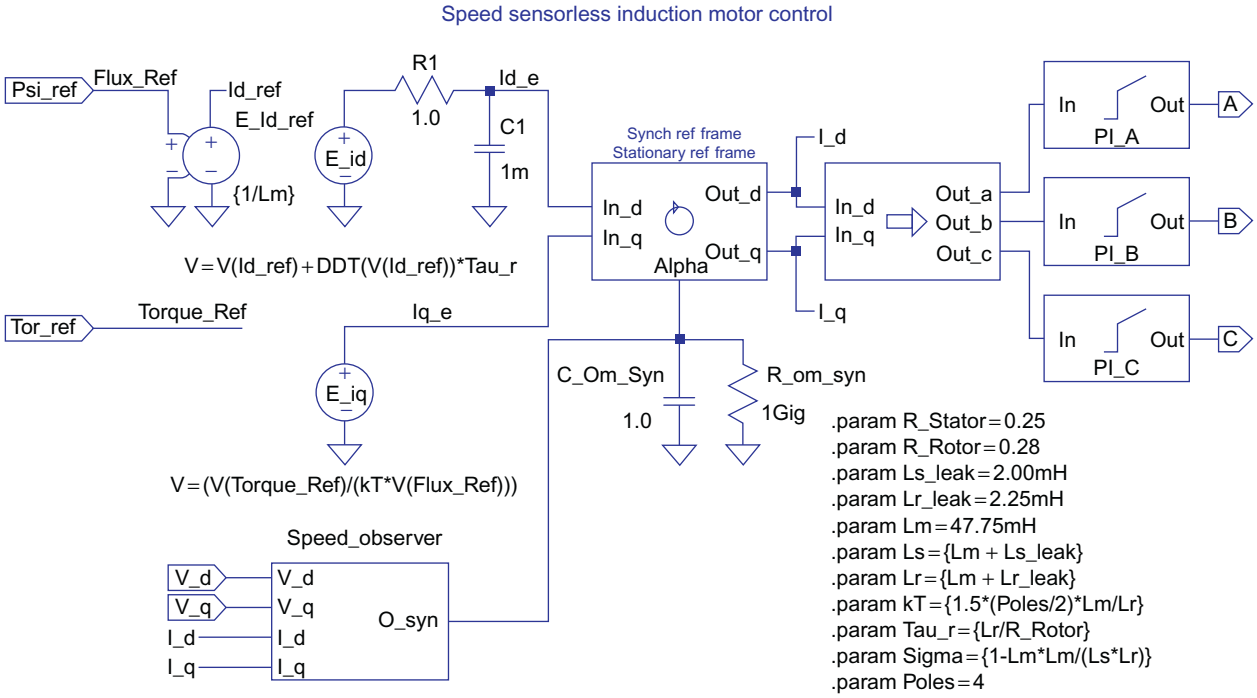


FIG. 44.18 Subcircuit for sensorless vector controller.

it is not necessary to calculate the slip speed and add it to the rotor speed to obtain the synchronous speed.

Fig. 44.19 shows the subcircuit for the speed observer. The speed observer uses the stator voltages and currents for the D- and Q-axis as input variables. After subtracting the voltage drop across the winding resistance and the leakage inductance of the stator from the stator input voltage and scaling the result by *Lr/Lm*, the observer calculates the D and Q components of the rotor flux by integration. Since the input values are in the stationary reference frame, so are the results. The observer also calculates the magnitude of the rotor flux (Eq. (44.9)) and then calculates the synchronous angular velocity (Eq. 44.10) by evaluating the rate of change of the ratio of the D and Q components. The mathematical relationships are given by Eqs. (44.9) and (44.10) [4]:

$$p\begin{bmatrix}\lambda_{rd}\\ \lambda_{rq}\end{bmatrix}=\frac{L_r}{L_m}\left[\begin{bmatrix}V_{sd}\\ V_{sq}\end{bmatrix}-\begin{bmatrix}R_s+\sigma L_s p & 0\\ 0 & R_s+\sigma L_s p\end{bmatrix}\begin{bmatrix}I_{sd}\\ I_{sq}\end{bmatrix}\right] \qquad (44.9)$$

$$\sigma=\left[1-\frac{L_m^2}{(L_r L_s)}\right] \quad \sigma=\text{Leakage factor}$$

$$\frac{d}{dt}a\tan\left(\frac{\lambda_{rq}(t)}{\lambda_{rd}(t)}\right)=\omega_s=\frac{\left(\frac{d}{dt}\lambda_{rq}(t)\lambda_{rd}(t)-\lambda_{rq}(t)\frac{d}{dt}\lambda_{rd}(t)\right)}{\left(\lambda_{rd}(t)^2+\lambda_{rq}(t)^2\right)} \qquad (44.10)$$

Fig. 44.20 shows the output for the speed sensorless vector control project as it presents itself in the LTspice waveform display for perfect tuning of the speed observer. A comparison of the traces for the torque and the torque command (they are

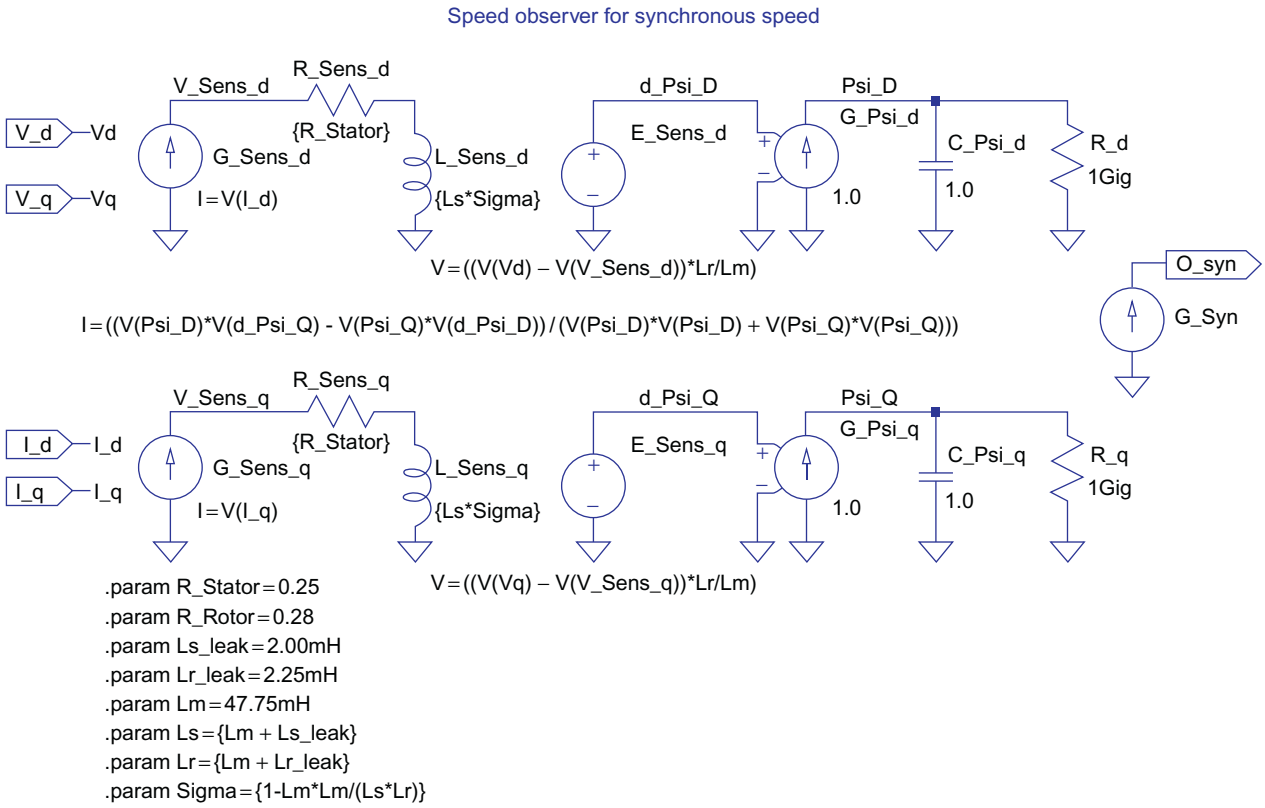


FIG. 44.19 Subcircuit for speed observer for sensorless vector controller.

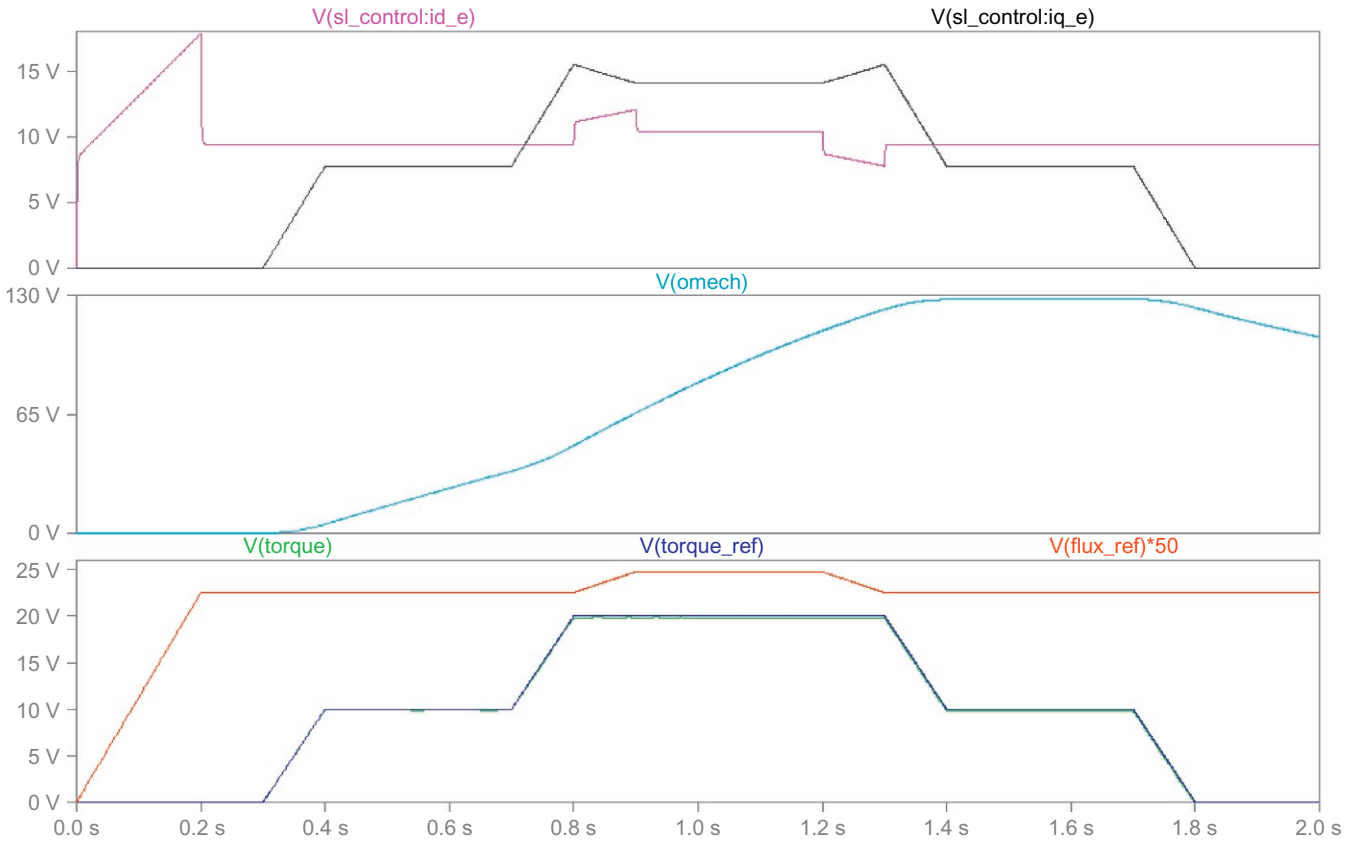


FIG. 44.20 Simulation results for sensorless vector control with perfect observer tuning.

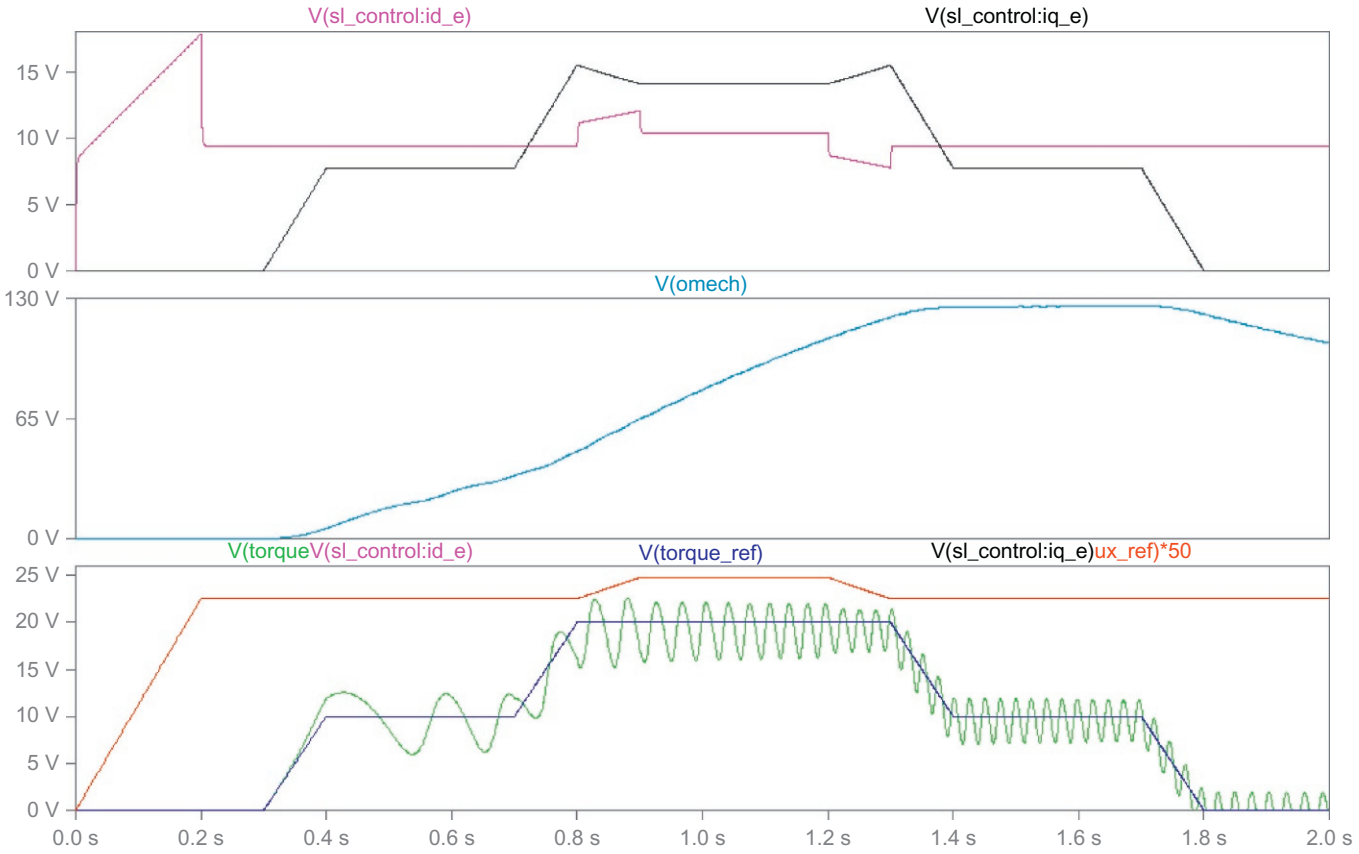


FIG. 44.21 Simulation results for sensorless vector control with detuned stator resistance.

perfectly on top of each other) shows that the scheme works extremely well. It even works for a start from zero speed, which is typically not the case in real systems. The reason is that the uncertainties of the winding resistance values (note that they change with temperature) create errors in observers like this one. The problem is worst at low speeds, because at low speeds and associated low stator frequencies, the uncertain winding resistance represents the largest part of the total machine impedance.

Fig. 44.21 shows the output for the speed sensorless vector control example with increased values for the stator resistance (0.28 Ω instead of 0.25 Ω). A comparison of the traces for the torque and the torque command now shows that the control does not work well in this case. This confirms that at low speeds including zero speed, an actual speed sensor is required for proper field-oriented control.

44.7 Conclusions

In this chapter, the capabilities of LTspice [1] have been used to simulate a number of examples from the power electronics, machines, and drive area. The advantage of LTspice is that it is based on the almost universal spice simulation language, which can be seen as the worldwide de facto standard for circuit simulation. The reader should always validate any model before it is used for critical engineering decisions. It was pointed out in the introduction that model validation often means verification that the limitations of the model are not exceeded.

In addition to the detailed examples, some general guidelines on the uses of simulation for analysis and design have been developed. All tested simulations yielded excellent results. The simulation time for each project shown was typically less than a minute on a contemporary (2016) PC. The author hopes that the reader has gotten an insight and appreciation of the power of modern circuit simulation codes and some useful ideas and inspirations for projects of his/her own.

References

[1] Linear Technology, 1630 McCarthy Blvd., Milpitas, CA 95035-7417, LTspice IV, http://www.linear.com/designtools/software/. Accessed February 23, 2017.

[2] PTC, 140 Kendrick Street, Needham, MA 02494, USA, http://www.ptc.com/engineering-math-software/mathcad Accessed February 23, 2017.

[3] N. Mohan, T. Undeland, W. Robbins, Power Electronics, Converters, Applications, and Design, second ed., John Wiley & Sons, New York, ISBN: 0-58408-8, 1995.

[4] A.M. Trzynadlowski, The Field Orientation Principle in Control of Induction Motors, Kluwer Academic Publishers, Inc., Boston, MA, ISBN: 0-7923-9420-8, 1994.
[5] P.C. Krause, O. Wasynczuk, S.D. Sudhoff, Analysis of Electric Machinery, IEEE Press, Hoboken, NJ, ISBN: 0-7803-1101-9, 1995.
[6] M.G. Giesselmann, Averaged and cycle by cycle switching models for buck, boost, buck-boost and cuk converters with common average switch model, in: Proceedings of the 32nd Intersociety Energy Conversion Engineering Conference, IECEC-97, Honolulu, Hawaii, July 27–Aug. 01, 1997, 1997.
[7] D.W. Novotny, T.A. Lipo, Vector Control and Dynamics of AC Drives, Oxford Science Publications, New York, NY, ISBN: 0-856439-2, 1996.
[8] P. Vas, Vector Control of AC Machines. Monographs in Electrical and Electronic Engineering, Oxford Science Publications, vol. 22, Clarendon Press/Oxford University Press, Oxford/New York, ISBN: 0-859370-81990.
[9] A. Von Jouanne, D. Rendusara, P. Enjeti, W. Gray, Filtering techniques to minimize the effect of long motor leads on PWM inverter fed AC motor drive systems. IEEE Trans. Ind. Appl. 32 (4) (1996) 919–926, http://dx.doi.org/10.1109/28.511650.
[10] K. Hasse, Zur Dynamik Drehzahlgeregelter Antriebe mit Stromrichter gespeisten Asynchron-Kurzschlussläufermachinen (On the Dynamics of Adjustable Speed Drives with converter-fed Squirrel Cage Induction Machines), Ph.D. Dissertation, Technical University of Darmstadt, 1969.

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Design for Reliability of Power Electronic Systems

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45.1 Introduction

Due to the foreseen exhaustion of fossil-based energies, many countries are turning to the renewable energy technologies [1,2]. Among those, wind and solar photovoltaic (PV) systems have attracted more attentions in the past decades [2]. However, the incompatibility of renewable sources and loads requires an intermediate processing stage, which is typically achieved by power electronics [2–4,4a]. In conventional electric systems (e.g., motor drive systems), the role of power electronics is also obvious, as they are heavily involved in controlling the loads—motors. That is, the power electronic technology is the key to optimal energy harvesting and also friendly energy system integration. Moreover, this technology is developing with new and emerging power devices [5,6] with extraordinary performances in terms of switching speed and efficiency. In all, power electronics will be extensively used in many applications in the future.

In practice, the design of power electronic systems is mainly cost-driven, and thus there are three major concerns: power density, efficiency, and reliability [7,8]. Efficiency improvements can be achieved through developing power-lossless topologies (also, including soft-switching techniques) and advancing the power semiconductor devices. As an intuitive way, minimizing the number of conversion stages can contribute to high efficiencies. Notably, the topological simplification also has adverse impacts (e.g., the leakage current issue in transformerless PV inverters), which thus requires new dedicated control strategies. Alternatively, the latest advancements in power semiconductor technologies, for example, wide bandgap power devices like silicon carbide (SiC) transistors, offer much room to improve the efficiency of power electronic systems [6–10]. For instance, as reported in [11–13], the PV power electronic systems with wide bandgap devices have achieved a remarkable efficiency of above 99%, meaning that very few losses exist. The high-efficiency performance has boosted the PV market, where commercial PV inverters employing new devices are available. Furthermore, the wide bandgap power semiconductors feature a high-switching frequency operation capability, and thus, incorporating soft-switching techniques can further improve the efficiency [14].

As discussed above, higher power density and efficiency of power electronic systems are relatively achievable. However, according to a survey [15], the power electronic converter itself has become one of the most fragile parts in the entire system. For instance, in that study, the unscheduled maintenance events due to power electronics account for 37% of the total events in a utility-scale PV power plants, as shown in

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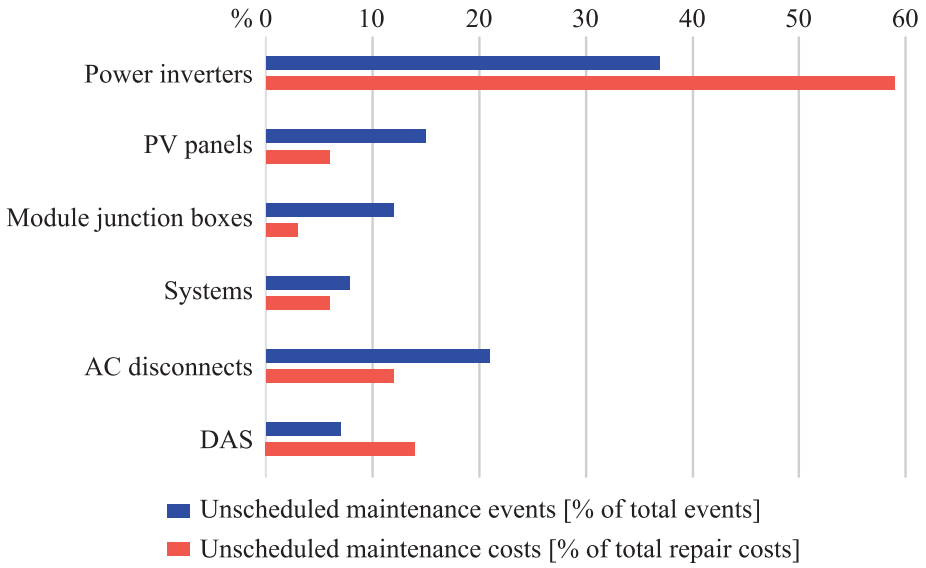


FIG. 45.1 Five years of real-field experience in failures of a utility-scale PV power plants (data acquisition systems (DAS)) [15].

Fig. 45.1. Those unscheduled maintenance events require human intervention (system repairing or maintenance), thus affecting the overall production and the maintenance costs, as observed in Fig. 45.1. In the end, the cost of PV energy will go up drastically due to the high failure rate of power inverters in PV systems. Hence, as aforementioned, high reliability of power electronics is in urgent need on top of efficiency.

As for reliability, more challenging issues should be addressed [16–23]. Prediction in lifetime of the power electronics is the first task so that the reliability can be taken as a performance factor in the design phase of power electronic systems, which is referred to as the design for reliability (DfR) [24–26]. In the past, the statistical analysis has been the dominant approach for lifetime prediction, where the reliability models (typically, constant failure rates) of subsystems are defined. For instance, a handbook—MIL-HDBK-217 F [27]—has been widely adopted to predict the lifetime of electronic equipment for decades. However, in this handbook, the models are outdated, and the associated failure rates are considered as constants. Thus, this handbook has been revoked. It is also worth to point out that the predicted lifetime or reliability based on this handbook has limited or no direct guiding value for the system design [28]. It is difficult to use the predicted reliability data to design new products or systems with higher reliability, not to mention the control to enhance the reliability performance. With the still increasing demands for high reliability, the analysis approach has to be shifted to the physics-of-failure (PoF) analysis [19–22], where the root causes, failure mechanisms, and mission profiles are in focus [20,29,30]. This (i.e., the PoF-based DfR) enables more predictable and controllable power electronic systems with high reliability.

In light of the above discussion, this chapter briefly discusses the mainstream power electronic converters for wind and PV power systems. More importantly, the DfR approach is explained in detail, including a short description of the failure mechanisms. Case studies on a 6-kW single-phase grid-connected PV inverter system have been provided to better illustrate the DfR approach considering mission profiles. Finally, concluding remarks and discussions on future research trends in the reliability of power electronics are provided.

45.2 Power Electronic Converters and Mission Profiles

Design and operation of power electronic systems for both wind and PV power systems are strongly dependent on the grid requirements. Fig. 45.2 shows the general demands for grid-connected PV and wind power systems, where the power electronic system is the key component, acting as “the brain” of the entire system. The objectives of those power electronic systems are to manage the power demand from the local operators and end customers [31,32]. A very common requirement is to transfer the PV and wind energy to the grid, according to its inherent characteristics (i.e., applying maximum power point tracking techniques). Other specific demands can be summarized as (a) reliable/secure power supply; (b) high efficiency, low cost, small volume, and effective protection; (c) control of active and reactive power injected into the grid; (d) dynamic grid support (e.g., fault ride-through operation); and (e) system monitoring and communication. In all, as the core of power conversion systems, the reliability of power electronic systems is of strong concern. In the following, some of the state-of-the-art power electronic converter solutions for wind and PV systems are introduced.

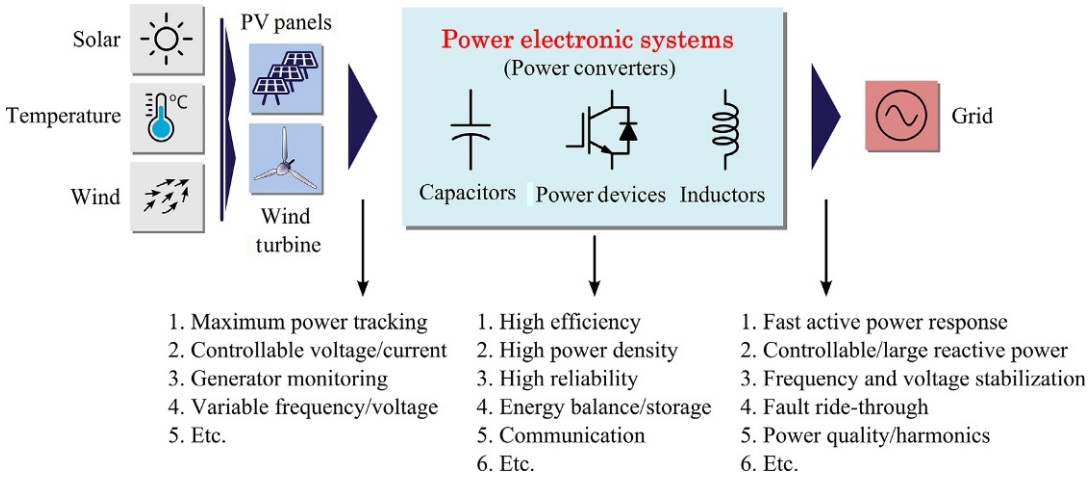


FIG. 45.2 Demands for grid-connected PV and wind power systems at different stages in the system.

45.2.1 Power Electronic Converters for Wind Power Systems

According to the types of generator, power electronics, speed controllability, and the way in which the aerodynamic power is limited, the wind-turbine system (WTS) designs can be categorized into four types:

- Fixed speed wind turbine (WT) systems
- Partial variable speed WT with variable rotor resistance
- Variable speed WT with partial-scale frequency converter
- Variable speed WT with full-scale power converter

Among those configurations, the latter two shown in Fig. 45.3 currently dominate the markets, which will be further employed in future wind power systems. As observed in Fig. 45.3 and aforementioned, the power electronic converters are very important, and they have various power ratings. In the past, the doubly fed induction generator (DFIG) with partial-scale power electronic converters was the most favorable concept (see Fig. 45.3A). However, the synchronous generator (SG) or asynchronous generator (AG) with full-scale power electronic converters (see Fig. 45.3B) has taken over today's wind power markets [33,34].

For the power electronic converters, there are many ways to configure. The most commonly adopted three-phase converter is the two-level voltage source converter (2L-VSC), as shown in Fig. 45.4. The popularity of this converter topology lies in its structural and control simplicity. However, the continuous increase in power capacity of an individual wind turbine [35,36] highly stressed the 2L-VSC and thus leading to a lower efficiency. From this standpoint, the multilevel converter technology is getting more and more attentions in wind power applications, since they can achieve more output voltage levels,

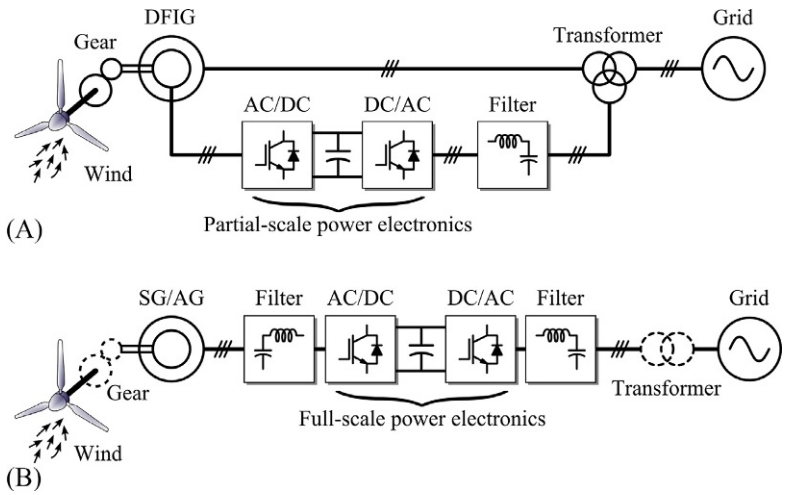


FIG. 45.3 Two dominant power-electronic-based WTS configurations: (A) partial-scale back-to-back power-converter-based wind turbine system with a doubly fed induction generator (DFIG) and (B) full-scale back-to-back power-converter-based wind turbine system with a synchronous or asynchronous generator (SG/AG).

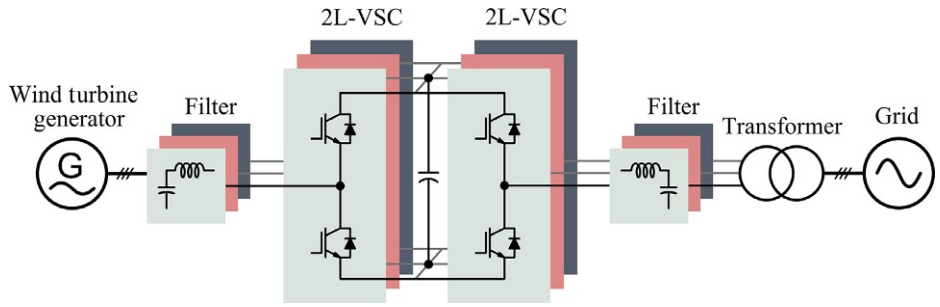


FIG. 45.4 Two-level VSC back-to-back (2L-VSC BTB) power electronic converters for wind turbine power systems.

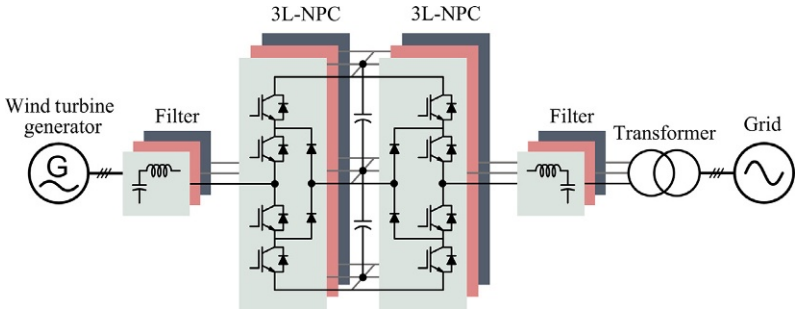


FIG. 45.5 Three-level neutral-point-clamped back-to-back (3L-NPC BTB) converter for wind turbine power systems.

higher voltage, and larger output power [33–37]. Fig. 45.5 shows the power converter schematics of the most successfully commercialized multilevel converter, that is, the three-level neutral-point-clamped (3L-NPC) converter. As mentioned, the 3L-NPC enables the use of smaller filters (reduced system volume), while the major drawback is the unequal power loss distribution. This in return may challenge the reliability of the entire power electronic converter system. To tackle this issue, multicell converter topologies by connecting converter cells in parallel or in series are developed and also commercially adopted in practice (e.g., Gamesa and Siemens) [38,39].

45.2.2 Power Electronic Converters for PV Power Systems

According to the state-of-the-art technologies, there are certain concepts [26,39a] to organize and deliver the PV power to the grid, as shown in Fig. 45.6. Each of the concepts consists of a couple of power electronic converters (e.g., dc-dc converters and dc-ac inverters) that are configured in different structures, depending on the applications and power ratings. For instance, modular PV converters (Fig. 45.6A) of small volume and high scalability are commonly adopted in small energy conversion systems. However, in order to connect modular PV converters to the grid, high conversion ratio dc-dc converters may be required, or a dc grid is necessary (see Fig. 45.6A and B). In contrast, string, multistring, or central inverters can directly be connected to the grid and they are developed as shown in Fig. 45.6B and C. Nevertheless, when compared with wind power systems, the PV utilization is still at a residential level with lower power ratings. Hence, string and multistring inverters with the exemplified configuration of Fig. 45.6B are dominant on the markets, and the single-phase connection is more often to see [40,41].

Fig. 45.7 exemplifies a single-phase grid-connected PV system with an LCL filter, where a full-bridge inverter has been employed. Additionally, to have a higher efficiency, transformerless PV inverters are preferred [40]. However, the side effects (e.g., leakage currents) brought by the removal of isolation transformers have to be addressed. Although single-phase configurations are more common, increasing demands in power and voltage also push the ratings of PV systems higher, as demonstrated in Fig. 45.6. Those large PV power plants, rated over tens and even hundreds of megawatts (MW), adopt many central inverters with the power rating of up to 900 kW. A typical large-scale PV power plant is shown in Fig. 45.8, in which the traditional three-phase full-bridge inverter can be adopted. Notably, the cables and power devices may have to bear large currents, and seen from this point, multilevel power electronic converter technologies might be more promising to large-scale PV systems [42–44]. In that case, disconnecting a large amount of dc currents is yet challenging.

45.2.3 Mission Profiles for Power Electronic Converters

A mission profile is normally referred to as a simplified representation of relevant conditions under which the system is operating [45,46]. As a result, the mission profiles for power electronic converters determine the loading of power electronic

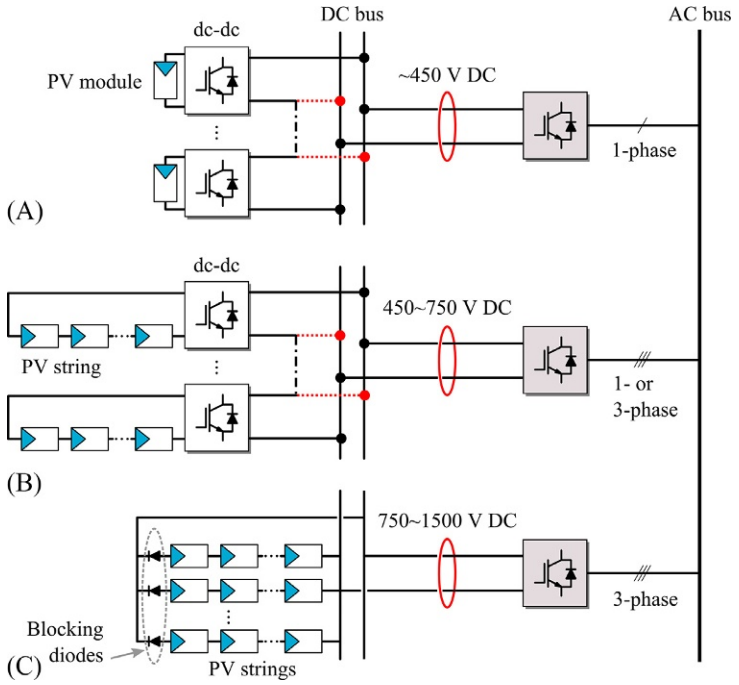


FIG. 45.6 Different grid-connected photovoltaic conversion systems: (A) module converters (low-power applications); (B) string or multi-string inverters (medium-power applications), where the dc-dc converters are optional; and (C) central inverters (high-power applications, e.g., commercial and utility-scale systems).

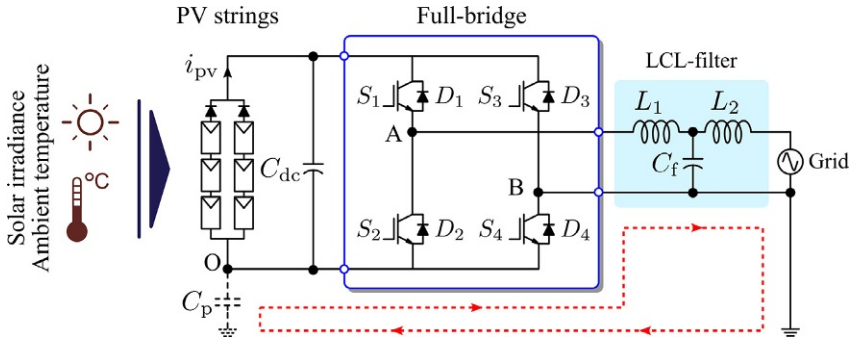


FIG. 45.7 Single-phase single-stage transformerless full-bridge string inverter with an LCL filter, where i_{pv} represents the PV output current and C_p is the parasitic capacitor between the PV panels (strings) and the ground. The dashed line with arrows indicates possible leakage currents circulating through the parasitic capacitor C_p.

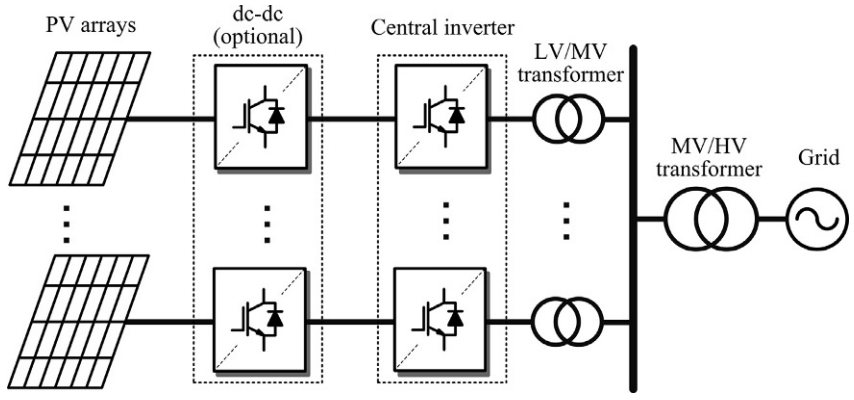


FIG. 45.8 Typical large-scale PV power plant based on central inverters for utility applications in the MW range (low voltage (LV); medium voltage (MV); high voltage (HV)).

components, and thereby, they are closely related to the cost and reliability performances. In renewable energy applications, the mission profiles are relatively tough: they need to withstand a large amount of power (even up to a few MWs) and perform a series of complicated functions required from the grid, and meanwhile, they also operate under harsh environments like day-night temperature swings, dust, vibration, humidity, and salty ambience. Moreover, the operating hours for wind turbines can be up to 120,000 h, and for a PV inverter, they might be operating 80,000 h in a 20-year life span [19,20]. Notably, today, even longer operation hours are discussed. In this section, typical mission profiles for wind and PV applications are exemplified, including wind speed, solar irradiance level, and ambient temperature.

45.2.3.1 Wind Speed

As the input of the entire wind power system, the wind energy quantified by the wind speed is an important factor that can determine the design, control, maintenance, energy yield, and eventually also the system cost. During the construction and design phases, assumptions have to be made about the wind conditions that the wind turbines will be exposed to. Typically, wind classes are used that are determined by three parameters—the average wind speed, extreme 50-year gust, and turbulence. Because the loading of power electronic converters are mainly caused by wind speed level and its variations, the knowledge of the wind class is of crucial importance for the reliability calculation and performances. The commonly adopted classifications of wind conditions are from an IEC standard [47]. Fig. 45.9 shows the distribution under different wind classes, where the Weibull function is used to describe the distribution characteristics.

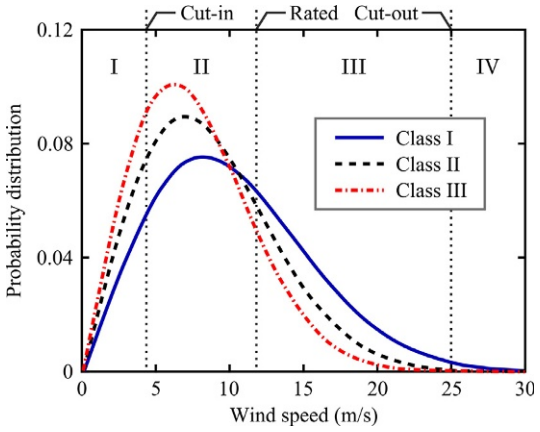


FIG. 45.9 Distributions of the wind speeds under different wind classes and operation of wind turbines (region I, no power generation below cut-in wind speed; region II, maximum power point tracking generation; region III, constant power generation; and region IV, no power generation above cut-out wind speed) [47].

Additionally, a field-recorded annual wind speed profile is illustrated in Fig. 45.10 [48], which is based on 1-h averaged at 80-m hub height for a wind farm located near Germany with the latitude of 54.25° and the longitude of 8.20°. The shown wind speed belongs to the IEC class I—high with an average wind speed of 8.5–10 m/s. It can be seen in Fig. 45.10 that the wind speed fluctuates significantly. Without proper controls of the mechanical and electrical parts, the fluctuations may be transferred to the grid and cause grid stability problems. Moreover, the power electronic components may suffer from largely cyclical loadings and thus accelerating the degradation and challenging the lifetime. As a result, the roughness class and fluctuation of wind speeds should be considered in the control and design of the power electronics for wind power systems [34].

45.2.3.2 Solar Irradiance

Wind speeds directly affect the power outputs of wind power systems, while solar irradiance level and ambient temperature are determining the output power of PV power systems. Actually, the mission profile (i.e., solar irradiance and ambient temperature) is a reflection of the intermittent nature of the solar PV energy, and consequently, it has an inherent relationship with the entire system performance. Figs. 45.11 and 45.12 show annual solar irradiance and ambient temperature profiles for PV systems in Aalborg, Denmark, respectively. It can be observed that both the solar irradiance level and the ambient temperature vary significantly through a year. It is thus required to develop dedicated MPPT control

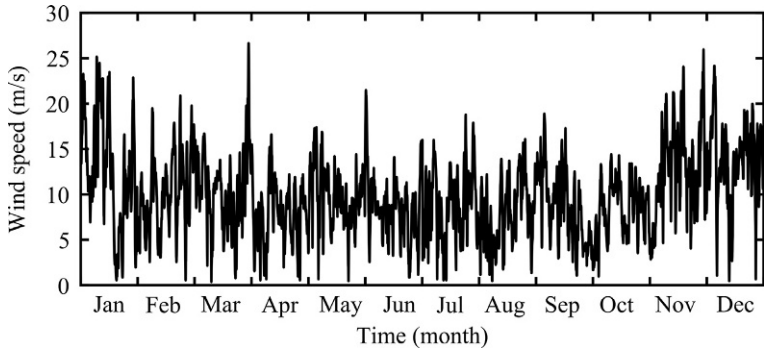


FIG. 45.10 One-year wind speed profile at a wind farm near Germany (recorded at 80-m height and 1-h averaged).

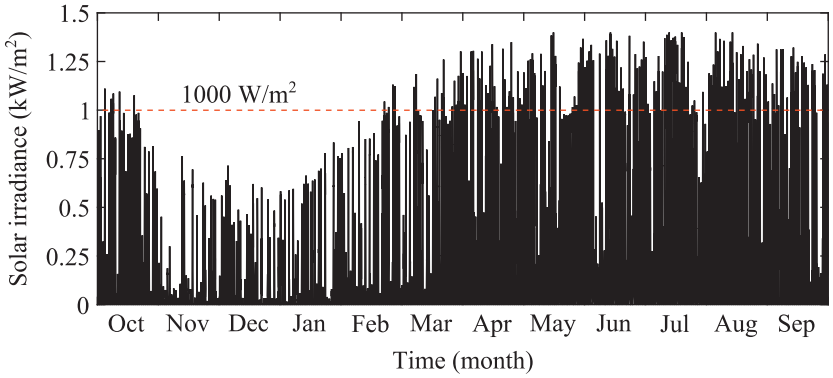


FIG. 45.11 Yearly solar irradiance level from recorded data (5 min per sampling data) for PV systems.

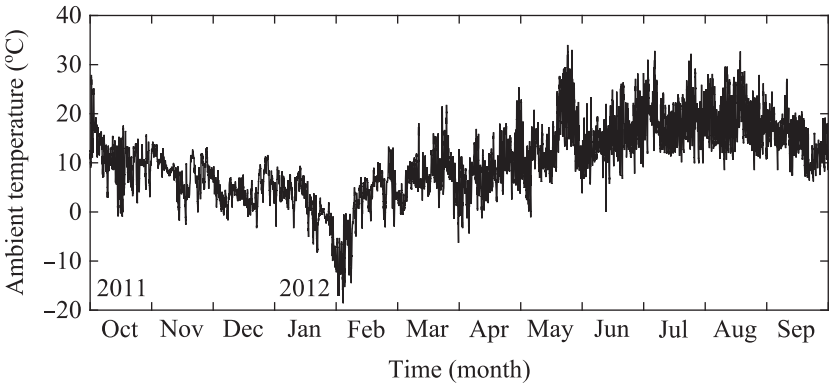


FIG. 45.12 Yearly ambient temperature profile from recorded data (5 min per sampling data) for PV systems.

systems in order to increase the energy yield. Moreover, like the case for wind power systems, the resultant fluctuating power from a PV power system may incur stability issues—especially when the PV penetration is getting larger and larger.

45.2.3.3 Ambient Temperature

In many applications, the power electronic systems are exposed to a harsh environment, where the ambient temperature is also time-varying, as shown in Fig. 45.12. The ambient temperature variation inevitably imposes thermal stresses on the power electronic systems, and thus, the reliability is affected by the ambient temperature. For PV power systems, as mentioned previously, the ambient temperature also affects the power outputs. Consequently, those aspects related to mission profiles have to be carefully considered in the control and design phases of power electronic systems.

45.3 Design for Reliability (DfR) of Power Electronic Systems

As discussed in Section 45.2, the power electronic system is the core of the energy conversion or processing system. Hence, the design of the entire system is centered on the power electronic systems, including power density, efficiency, and reliability. All those considered parameters aim to further reduce the cost but increase the manufacturability. For the design of high power density and high efficiency, technological achievements are dictated by topological innovations and semiconductor advancements, as mentioned at the beginning of this chapter.

To design a power electronic system with a specific reliability target, a top-down reliability allocation to the component level is necessary. Fig. 45.13 shows a typical architecture to illustrate this concept. The failure causes of a power electronic system could be hardware, software, and human errors. While this chapter focuses on the hardware reliability, the failure from software and human errors can be considered according to the software reliability modeling and the field operation experiences in human error rates. A certain level of the reliability budget should be allocated for the software failure and human errors accordingly. For the hardware part, there are long-term degradation related wear-out failures and single-event-related catastrophic failures. The wear-out failure of power electronic components usually can be modeled based on long-term operation conditions and their respective lifetime models, which contribute partially to the failure events. The single-event-related catastrophic failure does have associated failure mechanisms, while it is difficult to predict accurately by models. Instead, it can be obtained based on field operation experiences of the products or similar products. An ideal design is to avoid

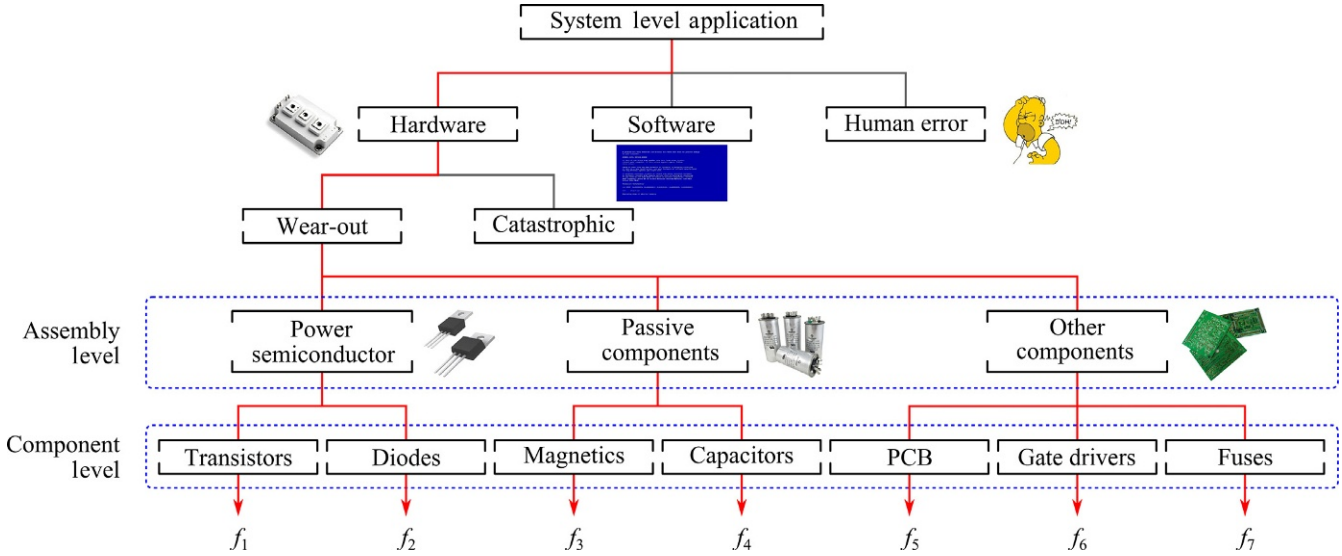


FIG. 45.13 From system-level reliability specification to component-level reliability design budgets (printed circuit board (PCB); f_k stands for failures with k being 1, 2, 3, ..., 7).

any wear-out failure of power electronic components within the specified service life of the power electronic system of interest. However, it is usually not feasible due to both design cost constraints and component property uncertainties to a certain degree. Based on the budgets for software failures, human errors, single-event-related catastrophic failures, and the system-level reliability target, the reliability design budget of hardware assemblies associated with wear-out failure mechanisms can be determined. The component-level reliability design target can then be allocated. The wear-out failure mechanisms of key power electronic components and the lifetime prediction methods have been well discussed in [20]. As an example, Section 45.4 demonstrates how to size the IGBT power devices to achieve a specific reliability target.

Fig. 45.14A shows the influencing factors in the design and operation phases of power electronic systems, where it can be observed that the design involves many factors. More important, it is seen in Fig. 45.14A that unexpected failures will occur during the operation, resulting in costly maintenance [24]. Accordingly, the design of high reliability is becoming mission critical in power electronic systems, as it is the key parameter affecting the levelized cost of energy (LCOE) [49,50]:

$$\mathrm{LCOE} = \frac{C_{\mathrm{int}} + C_{\mathrm{cap}} + C_{\mathrm{o\&m}}}{E_{\mathrm{annual}}} \tag{45.1}$$

where C_{int} is the initial development cost, C_{cap} represents the capital cost, $C_{\mathrm{o\&m}}$ indicates the operational and maintenance cost, and E_{annual} denotes the average annual energy production in the lifetime cycle of the system. More specifically, a power electronic system of high reliability will reduce the cost for operational and maintenance and also increase the service time (i.e., more energy production). Eventually, the cost of energy is lowered.

In order to lower the unscheduled maintenance cost, potential failures should be anticipated as early as possible and input into the design flow. This initiates a more promising solution to improving the reliability of power electronic systems, as shown in Fig. 45.14B, being the DfR approach. The inclusion of reliability enables a quick identification of design flaws or weakness and thus feeds back to the design for corrections (e.g., reselection of components). After a few iterations, the reliability demands can be fulfilled before the installation/construction of the power electronic system. As a consequence, significant cost reduction in the design phase and shorter development cycles can be attained while also targeting for higher reliability. Clearly, the failures or downtimes of the designed power electronic systems are predictable, demonstrated in Fig. 45.14B.

It should be pointed out that the reliability prediction is the first task for the DfR process, and it involves in multiple disciplines from the PoF point of view. Fig. 45.15 depicts the detailed reliability evaluation process of the DfR approach, which shows that the reliability analysis has three major tasks:

- Failure identification
- Stress analysis and strength modeling
- Reliability mapping.

More specifically, the critical components and the major failure mechanisms of power electronics are identified through physics analysis and real-field experience. Accordingly, the corresponding stresses and the ability of power electronic components to withstand the stresses are tested and modeled. Finally, counting algorithms and statistical distributions are adopted to map the stress and strength information to the reliability metrics of the power electronic system. The reliability indicators can be direct performances like the B_x lifetime, robustness, and failure probability or indirect performances [24]. Here, the B_x lifetime indicates the time by which x percent of a population of the system under study will have failed.

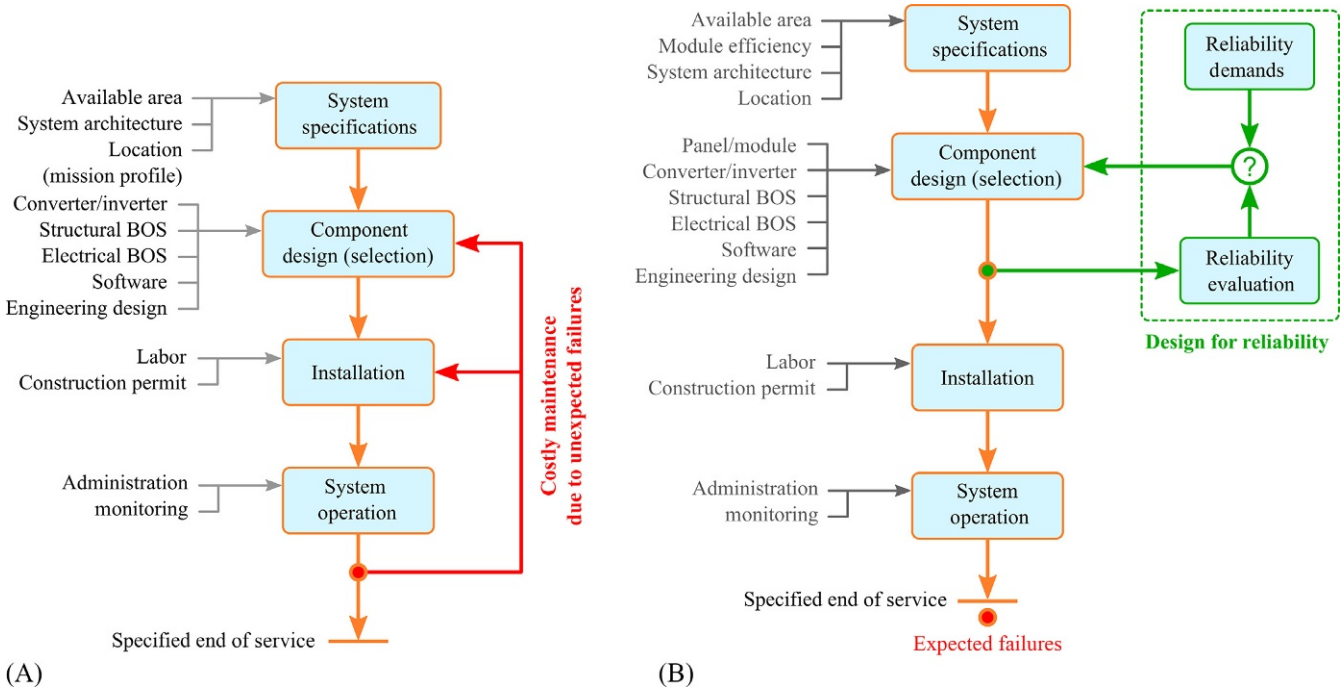


FIG. 45.14 Factors considered in the design and operation phases of power electronic systems (e.g., PV systems; balance of system (BOS)): (A) conventional design and (B) with reliability demands.

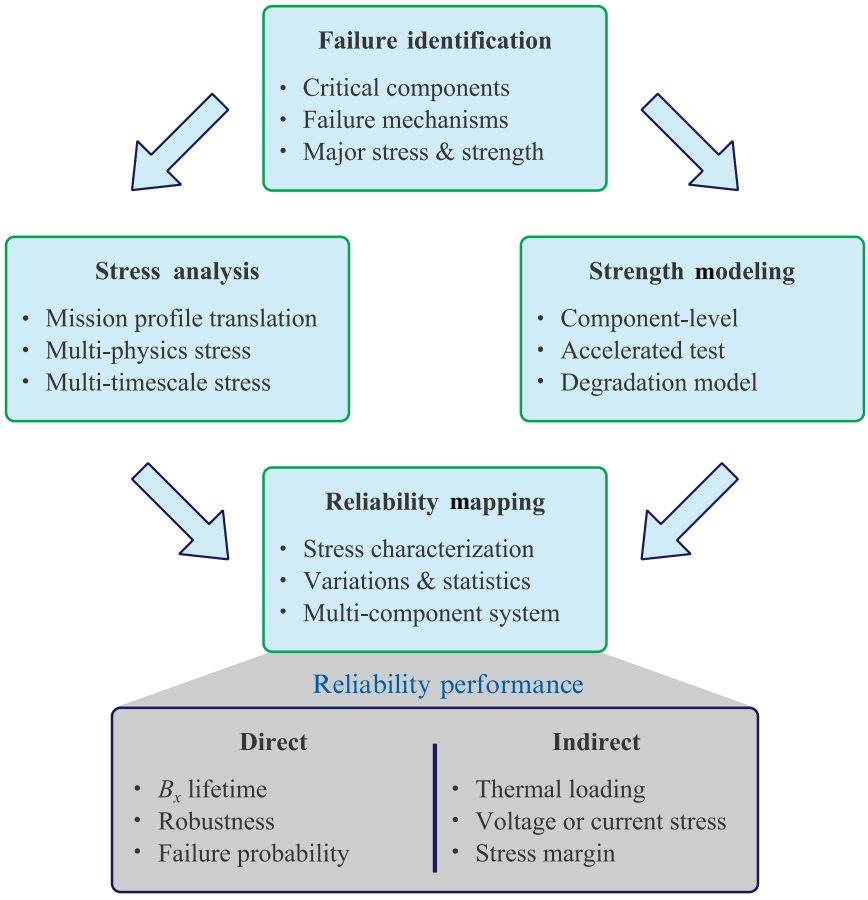


FIG. 45.15 Reliability prediction process of the design for reliability (DfR) approach for power electronic systems, where the B_x lifetime indicates the time by which x percent of a population of the evaluated system will have failed.

For a specific power electronic system, the DfR approach included in the Fig. 45.14 and the reliability predication process detailed in Fig. 45.15 enable analyzing the power converter candidates in terms of reliability. Here, the failure mechanisms have to be identified first. As discussed in [20], for power electronic converters, the major failures are related to the temperature in power devices. Nevertheless, on condition that the failure mechanisms are identified, it is possible to directly translate mission profiles into thermal loading on the power electronic components of the selected candidates. As a result, the reliability is obtained and can be compared with the demand. The process is further summarized as follows:

- Mission profile translation
- Thermal loading interpretation
- Lifetime model of power devices
- Monte Carlo reliability assessment
- System-level reliability analysis

which is also discussed in detail in the following.

45.3.1 Mission Profile Translation

In the DfR approach, the knowledge of the power converter operating conditions during the entire operation is essential [20,51]. In this respect, a mission profile of the power electronic converters, which represents the operating condition of the system, is needed. Then, the mission profiles have to be translated into thermal loading of power electronic systems (e.g., junction temperature variations of the devices), which can be done in the following way.

Once the mission profiles are obtained, the power production of the power electronic system can be estimated considering the electrical characteristic model. Taking into account the conversion efficiency, the power losses dissipated in the power devices can be estimated. Notably, this loss calculation is usually implemented with a lookup table (LUT), in order to assist the long-term simulation (e.g., an annual mission profile). In that case, the power losses are calculated for a certain set of operating conditions (e.g., the input power from 0 to 100% of the rated power), and the power losses under other operating conditions can be interpolated from the constructed LUT. Then, the thermal model of the power devices in the power electronic converter is required in order to obtain the device junction temperature loading.

45.3.2 Thermal Loading Interpretation

By applying the previous process, the junction temperature of the power electronic device T_j under a specific mission profile can be obtained. However, the device junction temperature is usually an irregular loading profile, due to the dynamics of mission profiles (e.g., the solar irradiance and ambient temperature for PV power systems). Thus, a cycle-counting algorithm such as a rainflow analysis is usually employed, in order to divide the irregular thermal loading cycle into several regular thermal loading cycles [52]. By doing so, the information such as the mean junction temperature T_{jm}, the cycle amplitude ΔT_j, and the cycle period t_{on} can be obtained, which can then be applied to the lifetime (degradation) model of the selected power electronic devices of the converter candidates.

45.3.3 Lifetime Model of Power Devices

Any component in a power electronic system (e.g., power semiconductors and capacitors) can cause failures of the entire system. In that regard, it leads to a complicated analysis, as the components may have a cross effect of the reliability on each other. For simplicity, only the temperature-related failure mechanisms of the power device are considered. In fact, the power device has been reported as one of the most critical components in power electronic systems [15,16]. Hence, it is a natural thought to consider temperature-related lifetime models [53,54].

Normally, the lifetime of the power device is expressed by considering the life consumption (LC), which indicates how much life of the device has been consumed (or damaged) during operations. The LC is calculated by using the Miner's rule as [52]

$$\text{LC} = \sum_i \frac{n_i}{N_{fi}} \tag{45.2}$$

where n_i is the number of cycles (obtained from the thermal loading interpretation) for a certain T_{jm}, ΔT_j, and $t_{\text{on,}}$ and N_{fi} is the number of cycles to failure calculated at that specific stress condition. For instance, if the number of cycles n_{i} is counted from an annual mission profile, the LC calculated in (45.2) will represent a yearly LC of the power device. When the LC accumulates to unity, the power electronic device is considered to reach its end of life, and the lifetime for the single power electronic device is predicted.

45.3.4 Monte Carlo Reliability Assessment

Actually, the lifetime prediction of the power device obtained from (45.2) can be taken as an ideal case, where all the power devices fail at the same rate. In reality, there are uncertainties in the time to failure of the power devices, mainly introduced by parametric variations in the lifetime model and changes in the stresses. Therefore, it is more common to express the lifetime prediction in terms of statistical values (e.g., using the probability of failures), rather than the fixed values. In order to do so, a Monte Carlo analysis should be performed, which is aimed to introduce variations in the system parameters, and simulate the

result with a large number of samples. With the large enough number of samples, the results will converge to the expected value.

This approach can be employed for estimating the power devices lifetime [55–57]. In this method, all the parameters in the lifetime model have to be modeled by a distribution function with a certain range of variations. Then, following the Monte Carlo simulation approach, a certain number of samples from each parametric distribution are randomly taken to calculate the lifetime of the power electronic device. Accordingly, a set of results is obtained, which can then be represented with a certain distribution function (e.g., Weibull distribution) [58]. The probability density function (PDF) of this lifetime prediction result is usually referred to as a lifetime distribution (failure distribution) $f(x)$, while its cumulative distribution function (CDF) is considered as an unreliability function $F(x)$. Eventually, the B_x lifetime can be obtained from the unreliability function of the power electronic device.

45.3.5 System-Level Reliability Analysis

A power electronic system usually has many power devices, and each power electronic device has its own unreliability function $F(x)$. In order to perform the system-level reliability assessment, the reliability block diagram of the entire system should be constructed [16]. The reliability block diagram represents how the reliability of components in the system interacts with each other. For a system with n components and the entire power electronic system cannot function if any of the n components fails, the total unreliability of system $F_{\text{tot}}(x)$ can be calculated as

$$F_{tot}(x) = 1 - \prod_{n} (1 - F_n(x)) \tag{45.3}$$

where $F_n(x)$ is the unreliability function of the n-th component. Once the total unreliability function of the inverter system $F_{\text{tot}}(x)$ is obtained, the B_x lifetime of the entire power electronic system can be estimated in a similar way as it has been done for a single power electronic component. However, it should be pointed out that the system-level reliability analysis approach (i.e., the reliability block diagram) can be applied to any power electronic system. For different converter topologies, the reliability block diagram may be different from (45.3), depending on the number of power devices and their operational principles.

Following the above steps, the reliability of a power electronic system can be predicted, and then, it can be compared with the design target (i.e., the reliability demand). This DfR flow especially includes the reliability in the design and thus avoids slow and expensive feedbacks or iterations. From this standpoint, the DfR approach can significantly accelerate the power electronic system design, while maintaining lower design costs and also better reliable products.

45.4 Case Study

In the DfR approach, the reliability target (i.e., the reliability demand) has to be specified at the beginning of the design phase, as shown in Fig. 45.14B. The reliability target is considered as a design objective, which should be fulfilled in the end of the design process. Following the diagram in Fig. 45.14B, the DfR approach is demonstrated on a single-phase 6 -kW PV power system referring to Fig. 45.7. To recap, the entire DfR flow for the PV power electronic system is represented in Fig. 45.16. As the PV power production is mainly affected by the solar irradiance level and the ambient temperature conditions, these two parameters are considered as the mission profile of the PV power electronic system, as also shown in Fig. 45.16. In the case study, the mission profiles in Figs. 45.11 and 45.12 are adopted. The targeted lifetime for the power electronic system is above 25 years. Three power electronic devices with the rated current of 15, 30, and 50 A from leading manufacturers are selected for comparison.

45.4.1 Mission Profile Translation

From the given mission profile, the PV power production (P_{pv}) can be determined by using the PV panel electrical characteristic model. Then, the actual input power seen by the PV inverter (P_{in}) is obtained by taking the MPPT algorithm efficiency (η_{MPPT}) into account. In order to estimate the power losses in the power devices (P_{loss}), a PV inverter loss model is employed. This can be obtained by considering the switching losses and conduction losses of the power devices in the inverter. After that, the thermal model of the power devices can be applied in order to obtain the junction temperature profile of the power devices (T_j) during the entire operation, which is implemented by using an LUT, as mentioned previously, in order to enable a long-term mission profile translation (e.g., yearly mission profiles) [59]. Fig. 45.17 summarizes the above process.

As an example (for the 600 V/30 A device), one of the translated thermal loading profiles under the mission profile (Figs. 45.11 and 45.12) is shown in Fig. 45.18. The cycle amplitude ($\triangle T_j$) and the mean junction temperature (T_{jm}) are presented in Fig. 45.18A and B, respectively. The impact of the mission profile can be observed in Fig. 45.18 from the thermal loading of the power device, where the cycle amplitude profile follows the variation in the solar irradiance profile (i.e., part of the mission profile). The long-term variation in the mean junction temperature has the similar tendency as the ambient temperature profile in Fig. 45.12 with a short-term variation imposed by the variation in the solar irradiance profile in Fig. 45.11.

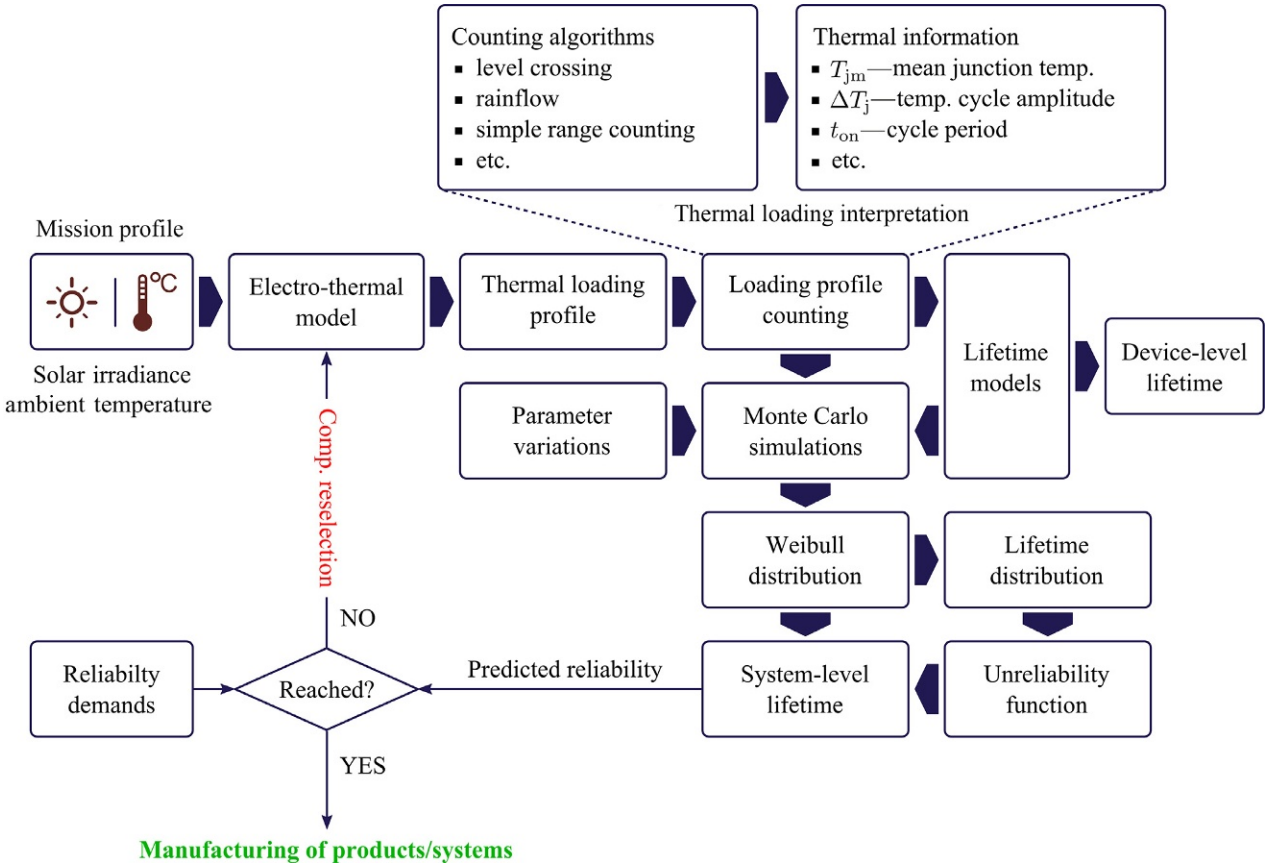


FIG. 45.16 Complete DfR structure for the power electronic systems in PV applications.

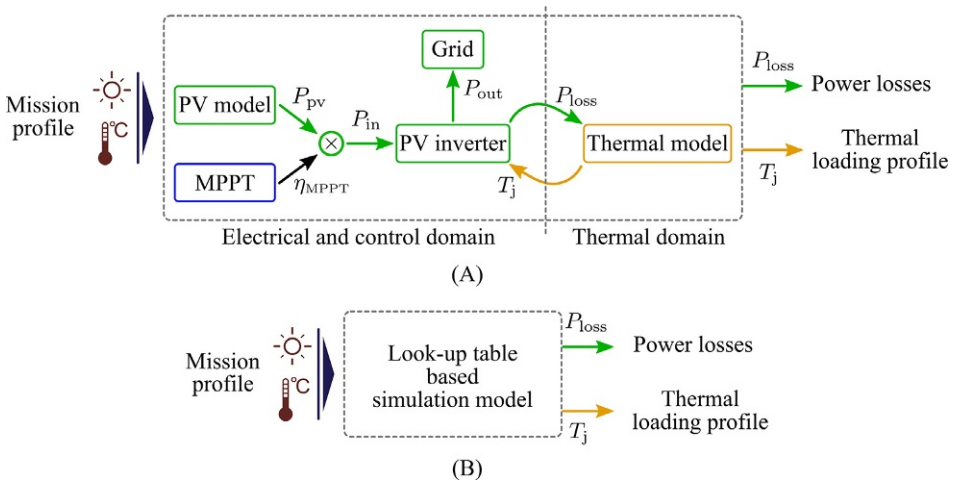


FIG. 45.17 Mission profile translation to power losses P_{loss} and thermal loading T_j: (A) for short-term mission profiles and (B) for long-term mission profiles.

45.4.2 Thermal Loading Interpretation

The junction temperature profile shown in Fig. 45.18 reflects the impact of mission profiles on the thermal loading of the power electronic system. However, it provides limited qualitative information about the thermal loading of the power devices, as the cycle amplitude ($\triangle T_j$) and the mean value of the junction temperature (T_{jm}) are an irregular profile due to the mission profile dynamics. In other words, it

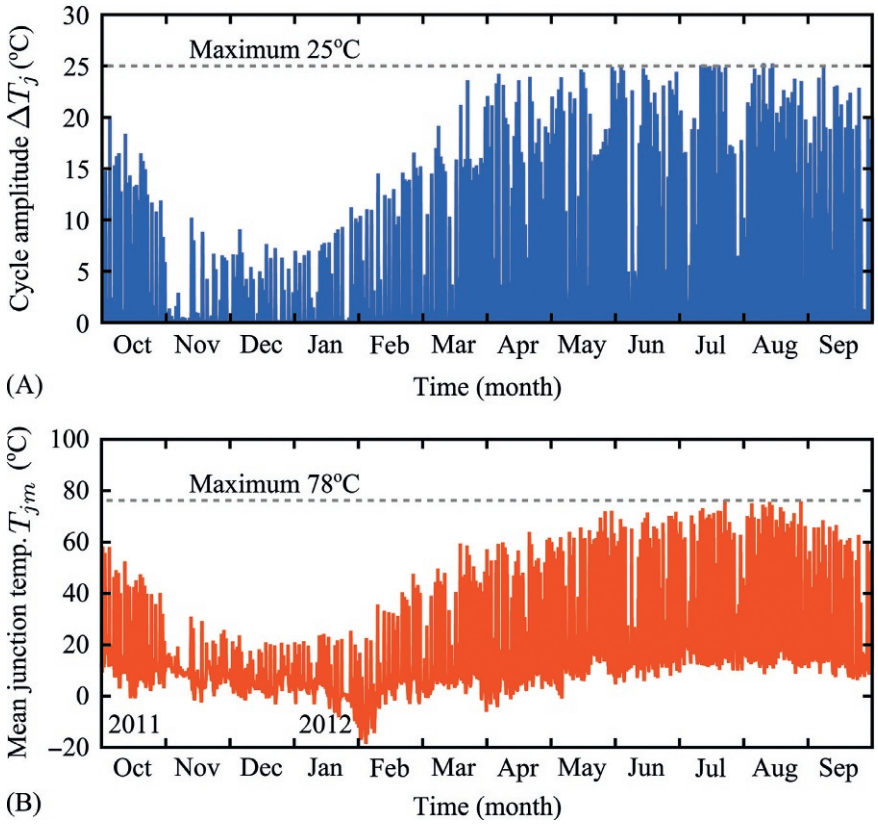


FIG. 45.18 Thermal loading of the power device in the single-phase full-bridge PV inverter under a yearly mission profile: (A) cycle amplitude and (B) mean junction temperature.

cannot be directly applied to an empirical lifetime model. Thus, a cycle-counting algorithm such as rainflow analysis is normally employed in order to divide the irregular profile into several regular thermal cycles [52]. With this analysis, the qualitative information such as the number of cycles n_i at a certain cycle amplitude $\triangle T_j$, mean junction temperature T_{jm}, and cycle period t_{on} can be obtained and applied to the lifetime model. Details of the rainflow algorithm can be found in [30,60,61].

45.4.3 Lifetime Model of Power Devices

The lifetime model of the interested power component is required for the lifetime prediction. In the case study, the lifetime of the power electronic systems (devices) is considered. Several lifetime models of the power electronic devices, components, or modules have been developed. A recently developed IGBT lifetime model that considers the thermal cycle period t_{on} is adopted [53], and it is expressed as

$$N_f = A \times (\Delta T_j)^{\alpha} \times (ar)^{\beta_1 \Delta T_j + \beta_0} \times \left[\frac{C + (t_{\text{on}})^{\gamma}}{C+1}\right] \times \exp\left(\frac{E_a}{k_b \times T_{\text{jm}}}\right) \times f_d \quad (45.4)$$

where N_f, $\triangle T_j$, T_{jm}, and t_{on} are defined previously. The other parameters are constants that are given in Table 45.1. Using the interpreted thermal loading information and (45.4), the LC of the power electronic components can be obtained according to (45.2). When the LC is accumulated to unity, the power electronic device reaches its end of life, as mentioned previously.

45.4.4 Monte Carlo Reliability Assessment

The reliability metric is usually expressed in terms of statistical values, rather than a fixed value obtained previously, due

TABLE 45.1 Parameters of the lifetime model of an IGBT module [53]

Parameter	Value	Experimental Condition
A	3.4368×10^{14}	
α	-4.923	$64 \le \triangle T_j \le 113$ K
β_1	-9.012×10^{-3}	
β_0	1.942	$0.19 \le ar \le 0.42$
C	1.434	
γ	-1.208	$0.07 \le t_{\text{on}} \le 63$ s
f_d	0.6204	
E_a	0.06606 eV	$32.5 \le T_j \le 122$ °C
k_B	8.6173324×10^{-5} eV/K	

to the uncertainties in the lifetime prediction. The uncertainties can be introduced by the component-parametric variations (e.g., due to the manufacturing process), lifetime-parametric variations (e.g., due to the test data), and variations in the stresses (e.g., variations in the PV power production due to the PV panel aging). In order to include the impact of those uncertainties into the lifetime prediction, a Monte Carlo analysis is employed [26,62], according to the flow shown in Fig. 45.16.

In the Monte Carlo analysis, variations are introduced to the lifetime model of (45.4) and also the stressors, where the parameters can be modeled with a certain distribution function (e.g., a normal distribution), as illustrated in Fig. 45.19. Following the Monte Carlo approach, a large set of populations are taken randomly from the distribution in Fig. 45.19 and applied to the lifetime model. Therefore, the lifetime distribution (or time-to-failure distribution) can be obtained and fitted with a specific distribution function. Normally, the lifetime distribution of the wear-out failure follows the Weibull distribution, and the Weibull probability density function (Weibull PDF) is shown in Fig. 45.20A. Notably, it is also possible to analyze the influence of an individual parametric variation by using the sensitivity study. This can be used for identifying the crucial parameter that limits the lifetime of the component (which may be redesigned). For instance, a controlled cooling unit may be required, if the lifetime is sensitive to the mean junction temperature.

From the lifetime distribution (i.e., the Weibull PDF), the reliability of one single power device (e.g., component level) can be determined by considering the CDF of the lifetime distribution. The Weibull CDF distribution (Weibull CDF) shown in Fig. 45.20B is referred to as the unreliability function, as it represents the percentage of failure population overtime. The B_x lifetime can be obtained from the unreliability function. For instance, the B_1 and B_{10} lifetime of the power device, which indicates the time when 1% and 10% of the population have failed, are the commonly used reliability metrics.

45.4.5 System-Level Reliability Analysis

In many cases, the system under consideration consists of several components, where each component has its own unreliability function. The B_x lifetime of one single component may not accurately reflect the B_x lifetime of the overall power electronic system. Thus, the system-level reliability assessment is performed using the reliability block diagram. For the full-bridge PV inverter shown in Fig. 45.7, the system-level reliability block diagram consists of a series connection of four components, as the failure of any power device (e.g., S_1, S_2, S_3, or S_4) will lead to the loss of functionality of the entire power electronic system. Thus, according to (45.3), the system-level unreliability function can be calculated as

$$F_{\text{sys}}(x) = 1 - \prod_{n=1}^{4} (1 - F_n(x)) \tag{45.5}$$

where $F_{\text{sys}}(x)$ is the system-level unreliability function and $F_n(x)$ is the component-level unreliability function of the n-th component. The system-level unreliability function of the PV inverter (e.g., four devices) is shown in Fig. 45.20B, where it can be noticed that the system-level unreliability is in general higher than the component-level unreliability (i.e., $F_{\text{sys}}(x) \geq F_n(x)$), resulting in the lower B_x lifetime for the system level.

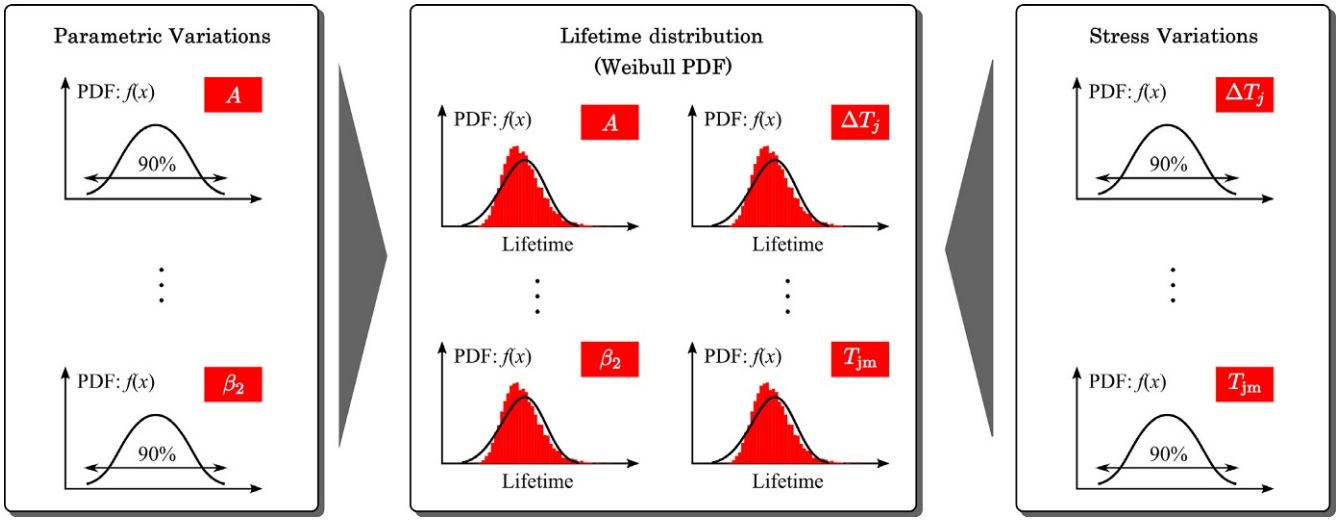


FIG. 45.19 Sensitivity analysis of the parametric variations by using the Monte Carlo analysis (probability density function (PDF)).

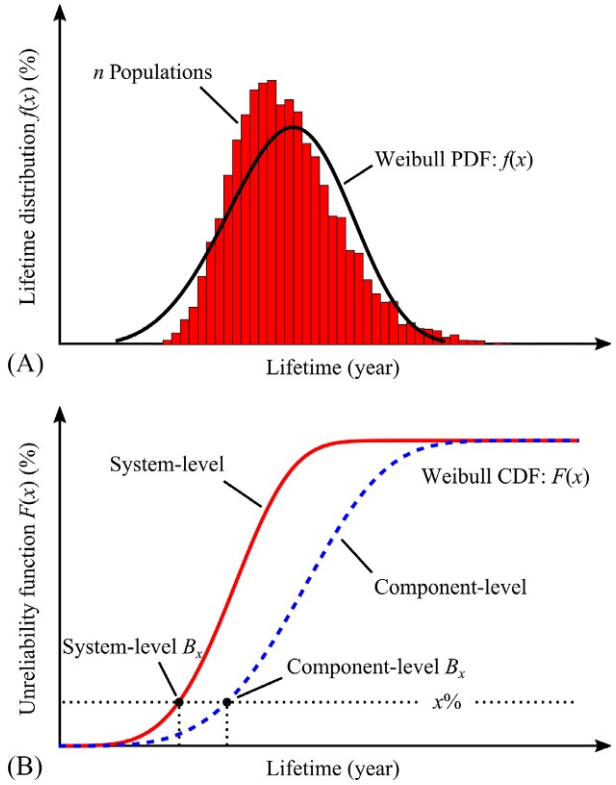


FIG. 45.20 Results from the Monte Carlo simulation (probability density function (PDF) and cumulative distribution function (CDF)): (A) lifetime distribution of one single power device (i.e., the Weibull PDF) with n populations and (B) unreliability function (i.e., the Weibull CDF) of one single power device (component level) and full-bridge inverter with four power devices (system level).

45.4.6 Design for Reliability (DfR) Results

The reliability analysis is carried out with three selected power devices following the above. As specified in the reliability target, the system-level lifetime of the PV power electronic system should be higher than 25 years. This is the benchmark for selecting the most suitable power electronic device among the three candidates. The DfR results are shown in Fig. 45.21. The lifetime distribution of each device obtained from the Monte Carlo analysis is shown in Fig. 45.21A, where it can be seen that the lifetime distribution of the three power electronic devices shows significant difference. A majority of the population with the 15-A power devices fail after 10 years of operation, while most of the population with the 30- and 50-A power devices can survive after 100 and 250 years of operation, respectively. However, it should be noted that in such cases other parameters will determine the lifetime. Additionally, the ratings of the two devices are over designed compared with the rating of the system under study (i.e., 6-kW). Both lead to the relatively long lifetime.

Based on the lifetime distribution in Fig. 45.21A, the unreliability function can be obtained, as it is shown in Fig. 45.21B, where the B_x lifetime is also indicated. For example, it can be seen from Fig. 45.21B that the system-level B_1 lifetime of the PV inverter is 2 years if the 15-A power devices are selected. This means that the power electronic system with 15-A power devices did not meet the reliability target of 25 years under the given mission profile. On the other hand, the PV inverter with 30- and 50-A power devices has the system-level B_1 lifetime of 30 and 61 years, respectively. Therefore, either the 30- or 50-A power device can be used in the full-bridge power electronic system that fulfills the reliability target. In most cases, the cost of the power devices with the current rating of 30 A will be lower than that of the 50-A power devices. Thus, the 30-A power electronic device is considered to be the most suitable candidate to be used in the PV power system in order to achieve the system-level B_1 lifetime higher than 25 years. However, it is also worth mentioning that the predicted lifetime is relatively long, since there are many other factors influencing the reliability. In this case study, only the failure mechanism related the junction temperature is considered. To improve the reliability prediction, more failure mechanisms as well as possible coupling effects should be taken into account. It in return may make the analysis become more complicated. Nevertheless, the above demonstrates a way to lifetime prediction, and thus enables the DfR in power electronic systems.

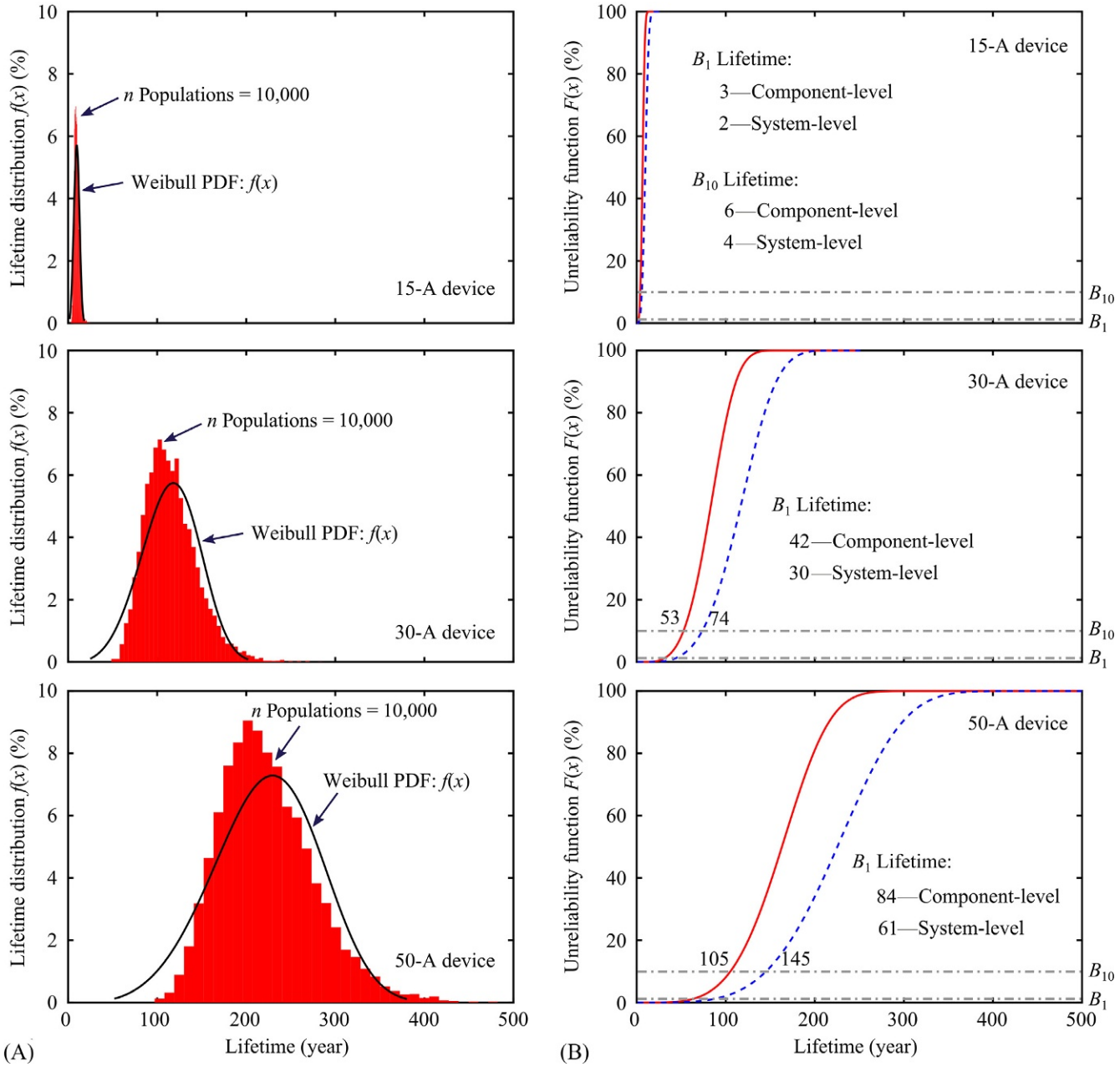


FIG. 45.21 Design for reliability (DfR) results of the power electronic system for single-phase PV applications obtained from the Monte Carlo simulation with 10,000 populations: (A) lifetime distribution of one single power device (i.e., the Weibull PDF function) and (B) unreliability function (i.e., the Weibull CDF function) of one single power device (component level) and full-bridge inverter with four power devices (system level). Note that there are other factors leading to the so long lifetime.

45.5 Summary

The reliability demands for power electronic systems have been identified in this chapter. The state of the art in power electronic converters for wind and PV power systems have been briefly reviewed, from which it is known that the power electronic systems play a vital role in the power conversion. The conventional design of power electronic systems focuses on power density and efficiency. However, the power electronic system is also one of the most life-limiting parts, and thus, the reliability should be included in the design phase, being the design for reliability (DfR) approach, as demonstrated in this chapter. Multidisciplinary efforts in component physics, reliability engineering, system engineering, and power electronics are necessary to implement the DfR approach. Many challenges still exit in mission profile modeling, lifetime modeling, reliability data in software, human errors, single-event catastrophic failures, and reliability-oriented design tools as

discussed in [20]. Other relevant studies related to this chapter have been collectively presented in [63], which provides an overview of the recent advancements in the area of reliability of power electronic converter systems and also reliability testing.

References

[1] International Renewable Energy Agency (IRENA). 2016. Renewable capacity statistics 2016. Tech. Rep., pp. 1–56, Apr. 2016. Last retrieved on Nov. 26, 2016. [Online]. Available: http://www.irena.org/DocumentDownloads/Publications/IRENA_RE_Capacity_Statistics_2016.pdf.

[2] F. Blaabjerg, D.M. Ionel, Y. Yang, H. Wang, Renewable energy systems technology overview and perspectives, in: F. Blaabjerg, D. Ionel (Eds.), Renewable Energy Devices and Systems with Simulations in MATLAB and ANSYS, Chapter 1, CRC Press LLC, 2017, pp. 1–16.

[3] F. Blaabjerg, K. Ma, Y. Yang, Power electronics—the key technology for renewable energy systems, in: Proceedings of EVER, 2014, pp. 1–11.

[4] J.M. Carrasco, L.G. Franquelo, J.T. Bialasiewicz, E. Galvan, R.C. Portillo Guisado, M.A.M. Prats, J.I. Leon, N. Moreno-Alfonso, Power-electronic systems for the grid integration of renewable energy sources: a survey, IEEE Trans. Ind. Electron. 53 (4) (2006) 1002–1016.

[4a] F. Blaabjerg, Z. Chen, S.B. Kjaer, Power electronics as efficient interface in dispersed power generation systems, IEEE Trans. Power Electron. 19 (5) (2004) 1184–1194.

[5] J.D. van Wyk, F.C. Lee, On a future for power electronics, IEEE J. Emerg. Sel. Top. Power Electron. 1 (2) (2013) 59–72.

[6] J.C. Balda, A. Mantooth, Power-semiconductor devices and components for new power converter developments: a key enabler for ultra-high efficiency power electronics, IEEE Power Electron. Mag. 3 (2) (2016) 53–56.

[7] M. Kasper, D. Bortis, G. Deboy, J. W. Kolar, Design of a highly efficient (97.7%) and very compact (2.2 kW/dm^3) isolated AC-DC telecom power supply module based on the multi-cell ISOP converter approach, IEEE Trans. Power Electron. 32 (10) (2017) 7750–7769.

[8] D. Bortis, D. Neumayr, J.W. Kolar, ηρ-Pareto optimization and comparative evaluation of inverter concepts considered for the GOOGLE Little Box Challenge, in: Proceedings of IEEE COMPEL, Trondheim, 2016, pp. 1–5.

[9] R. Khazaka, L. Mendizabal, D. Henry, R. Hanna, Survey of high temperature reliability of power electronics packaging components, IEEE Trans. Power Electron. 30 (5) (2015) 2456–2464.

[10] J. Colmenares, D.P. Sadik, P. Hilber, H.P. Nee, Reliability analysis of a high-efficiency SiC three-phase inverter, IEEE J. Emerg. Sel. Top. Power Electron. 4 (3) (2016) 996–1006.

[11] B. Burger, D. Kranzer, Extreme high efficiency PV-power converters, in: Proceedings of EPE - ECCE Europe, 2009, pp. 1–13.

[12] M.H. Todorovic, F. Carastro, T. Schuetz, R. Roesner, L. Stevanovic, G. Mandrusiak, et al., SiC MW PV inverter, Proceedings of PCIM Europe, 2016, pp. 1–8.

[13] Y. Furusho, K. Fujii, 1-MW solar power conditioning system with boost converter using all-SiC power module, in: Proceedings of CIPS, 2016, pp. 1–5.

[14] M. Kasper, R.M. Burkart, G. Deboy, J.W. Kolar, ZVS of Power MOSFETs Revisited, IEEE Trans. Power Electron. 31 (12) (2016) 8063–8067.

[15] L.M. Moore, H.N. Post, Five years of operating experience at a large, utility-scale photovoltaic generating plant, Prog. Photovolt.: Res. Appl. 16 (3) (2008) 249–259.

[16] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, P. Tavner, An industry-based survey of reliability in power electronic converters, IEEE Trans. Ind. Appl. 47 (3) (2011) 1441–1451.

[17] Y. Song, B. Wang, Survey on reliability of power electronic systems, IEEE Trans. Power Electron. 28 (1) (2013) 591–604.

[18] S. Yang, D. Xiang, A. Bryant, P. Mawby, L. Ran, P. Tavner, Condition monitoring for device reliability in power electronic converters: a review, IEEE Trans. Power Electron. 25 (11) (2010) 2734–2752.

[19] H. Wang, M. Liserre, F. Blaabjerg, Toward reliable power electronics: challenges, design tools, and opportunities, IEEE Ind. Electron. Mag. 7 (2) (2013) 17–26.

[20] H. Wang, M. Liserre, F. Blaabjerg, P. de Place Rimmen, J. B. Jacobsen, T. Kvisgaard, J. Landkildehus, Transitioning to physics-of-failure as a reliability driver in power electronics, IEEE J. Emerg. Sel. Top. Power Electron. 2 (1) (2014) 97–114.

[21] H. Oh, B. Han, P. McCluskey, C. Han, B.D. Youn, Physics-of-failure, condition monitoring, and prognostics of insulated gate bipolar transistor modules: a review, IEEE Trans. Power Electron. 30 (5) (2015) 2413–2426.

[22] L. Yang, P.A. Agyakwa, C.M. Johnson, Physics-of-failure lifetime prediction models for wire bond interconnects in power electronic modules, IEEE Trans. Device Mat. Rel. 13 (1) (2013) 9–17.

[23] S.V. Dhople, A. Davoudi, A.D. Domínguez-García, P.L. Chapman, A unified approach to reliability assessment of multiphase dc-dc converters in photovoltaic energy conversion systems, IEEE Trans. Power Electron 27 (2) (2012) 739–751.

[24] Y. Yang, V.S. Sularea, K. Ma, F. Blaabjerg, Advanced design tools for the reliability of power electronics—case studies on a photovoltaic (PV) system, in: Proceedings of IECON, 2015, pp. 2828–2833.

[25] X. Shi, A.M. Bazzi, Solar photovoltaic power electronic systems: design for reliability approach, in: Proceedings of EPE-ECCE Europe, 2015, pp. 1–8.

[26] Y. Yang, A. Sangwongwanich, F. Blaabjerg, Design for reliability of power electronics for grid-connected photovoltaic systems, CPSS Trans. Power Electron. Appl. 1 (1) (2016) 92–103.

[27] U.S. Department of Defense, MIL-HDBK-217F—Military Handbook for Reliability Prediction of Electronic Equipment. Department of Defense, Washington DC, USA, Dec. 1991.

[28] C. Jais, B. Werner, D. Das, Reliability predictions—continue reliance on a misleading approach, in: Proceedings of RAMS, 2013, pp. 1–6.

[29] Y. Song, B. Wang, Evaluation methodology and control strategies for improving reliability of HEV power electronic system, IEEE Trans. Veh. Technol. 63 (8) (2014) 3661–3676.

[30] X. Ma, Y. Guo, L. Wang, W. Ji, Exploration of the reliability of automotive electronic power steering system using device junction electrothermal profile cycle, IEEE Access 4 (2016) 7054–7062.

[31] R. Teodorescu, M. Liserre, P. Rodriguez, Grid Converters for Photovoltaic and Wind Power Systems, Wiley, Hoboken, NJ, USA, 2011.

[32] F. Blaabjerg, R. Teodorescu, M. Liserre, A.V. Timbus, Overview of control and grid synchronization for distributed power generation systems, IEEE Trans. Ind. Electron. 53 (5) (2006) 1398–1409.

[33] F. Blaabjerg, K. Ma, Future on power electronics for wind turbine systems, IEEE J. Emerg. Sel. Top. Power Electron. 1 (3) (2013) 139–152.

[34] F. Blaabjerg, K. Ma, Wind energy systems. Proc. the IEEE (2017) 1–19, early access, http://dx.doi.org/10.1109/JPROC.2017.2695485.

[35] M. Liserre, R. Cardenas, M. Molinas, J. Rodriguez, Overview of multi-MW wind turbines and wind parks, IEEE Trans. Ind. Electron. 58 (4) (2011) 1081–1095.
[36] K. Ma, F. Blaabjerg, Multilevel converters for 10 MW wind turbines, in: Proceedings of EPE'11, Aug. 30, 2011–Sept. 1, 2011, pp. 1–10.
[37] J. Rodriguez, S. Bernet, P.K. Steimer, I.E. Lizama, A survey on neutral-point-clamped inverters, IEEE Trans. Ind. Electron. 57 (7) (2010) 2219–2230.
[38] B. Andresen, J. Birk, A high power density converter system for the Gamesa G10x 4.5 MW Wind turbine, in: Proceedings of EPE, 2007, pp. 1–7.
[39] R. Jones, P. Waite, Optimised power converter for multi-MW direct drive permanent magnet wind turbines, in: Proceedings of EPE, 2011, pp. 1–10.
[39a] F. Blaabjerg, Y. Yang, D. Yang, X. Wang, Distributed power-generation systems and protection, Proc. IEEE 105 (7) (2017) 1311–1331.
[40] Y. Yang, F. Blaabjerg, Overview of single-phase grid-connected photovoltaic systems, Electr. Power Compo. Sys. 43 (12) (2015) 1352–1363.
[41] N.A. Rahim, R. Saidur, K.H. Solangi, M. Othman, N. Amin, Survey of grid-connected photovoltaic inverters and related systems, Clean Technol. Environ. Policy 14 (4) (2012) 521–533.
[42] B. Xiao, L. Hang, J. Mei, C. Riley, L.M. Tolbert, B. Ozpineci, Modular cascaded H-bridge multilevel PV inverter with distributed MPPT for grid-connected applications, IEEE Trans. Ind. Appl. 51 (2) (2015) 1722–1731.
[43] M.R. Islam, Y. Guo, J. Zhu, A multilevel medium-voltage inverter for step-up-transformer-less grid connection of photovoltaic power plants, IEEE J. Photovoltaics 4 (3) (2014) 881–889.
[44] H. Nademi, A. Das, R. Burgos, L.E. Norum, A new circuit performance of modular multilevel inverter suitable for photovoltaic conversion plants, IEEE J. Emerg. Sel. Top. Power Electron. 4 (2) (2016) 393–404.
[45] M. Ciappa, Lifetime prediction on the base of mission profiles, Microelectron. Reliab. 45 (9–11) (2005) 1293–1298.
[46] F. Chan, H. Calleja, Reliability estimation of three single-phase topologies in grid-connected PV systems, IEEE Trans. Ind. Electron. 58 (7) (2011) 2683–2689.
[47] IEC Standard, Wind turbines—part I: design requirements, IEC 61400-1, third ed., (2005).
[48] K. Ma, M. Liserre, F. Blaabjerg, T. Kerekes, Thermal loading and lifetime estimation for power device considering mission profiles in wind power converter, IEEE Trans. Power Electron. 30 (2) (2015) 590–602.
[49] C. Kost, J.N. Mayer, J. Thomsen, N. Hartmann, C. Senkpiel, S. Philipps, et al., Levelized cost of electricity renewable energy technologies, Tech. Rep., Fraunhofer Institute for Solar Energy Systems ISE, 2013. Last retrieved on Nov. 27, 2016. [Online]. Available: https://www.ise.fraunhofer.de/en/publications/veroeffentlichungen-pdf-dateien-en/studien-und-konzeptpapiere/study-levelized-cost-of-electricity-renewable-energies.pdf.
[50] M. Woodhouse, R. Jones-Albertus, D. Feldman, R. Fu, K. Horowitz, D. Chung, et al., The role of advancements in solar photovoltaic efficiency, reliability, and costs, Tech. Rep. (NREL/TP-6A20-65872), National Renewable Energy Laboratory (NREL) of the U.S. Department of Energy, May 2016. Last retrieved on Nov. 27, 2016. [Online]. Available: http://www.nrel.gov/docs/fy16osti/65800.pdf.
[51] M. Musallam, C. Yin, C. Bailey, M. Johnson, Mission profile-based reliability design and real-time life consumption estimation in power electronics, IEEE Trans. Power Electron. 30 (5) (2015) 2601–2613.
[52] H. Huang, P.A. Mawby, A lifetime estimation technique for voltage source inverters, IEEE Trans. Power Electron. 28 (8) (2013) 4113–4119.
[53] U. Scheuermann, R. Schmidt, P. Newman, Power cycling testing with different load pulse durations, in: Proceedings of PEMD, 2014, pp. 1–6.
[54] I.F. Kovacevic, U. Drofenik, J.W. Kolar, New physical model for lifetime estimation of power modules, in: Proceedings of IPEC—ECCE ASIA, 2010, pp. 2106–2114.
[55] P.D. Reigosa, H. Wang, Y. Yang, F. Blaabjerg, Prediction of bond wire fatigue of IGBTs in a PV inverter under a long-term operation, IEEE Trans. Power Electron. 31 (10) (2016) 7171–7182.
[56] Y. Shen, H. Wang, Y. Yang, P.D. Reigosa, F. Blaabjerg, Mission profile based sizing of IGBT chip area for PV inverter applications, in: Proceedings of PEDG, 2016, pp. 1–8.
[57] D. Zhou, H. Wang, F. Blaabjerg, S.K. Kaer, D. Blom-Hansen, System-level reliability assessment of power stage in fuel cell application, in: Proceedings of ECCE, 2016, pp. 1–8.
[58] ZVEI, How to measure lifetime for robustness validation—step by step, Rev. 1.9, 2012, Last retrieved on Jul. 14, 2017. [Online]. Available:https://www.zvei.org/fileadmin/user_upload/Presse_und_Medien/Publikationen/2013/Oktober/How_to_Measure_Lifetime_for_Robustness_Validation_-_Step_by_Step/Robustness-Valdiation-Step-by-Step.pdf.
[59] Y. Yang, H. Wang, F. Blaabjerg, K. Ma, Mission profile based multi-disciplinary analysis of power modules in single-phase transformer-less photovoltaic inverters, in: Proceedings of EPE, 2013, spp. 1–10.
[60] L.R. GopiReddy, L.M. Tolbert, B. Ozpineci, J.O.P. Pinto, Rainflow Algorithm-Based Lifetime Estimation of Power Semiconductors in Utility Applications, IEEE Trans. Ind. Appl. 51 (4) (2015) 3368–3375.
[61] M. Musallam, C.M. Johnson, An efficient implementation of the rainflow counting algorithm for life consumption estimation, IEEE Trans. Rel. 61 (4) (2012) 978–986.
[62] K. Ma, H. Wang, F. Blaabjerg, New approaches to reliability assessment: using physics-of-failure for prediction and design in power electronics systems, IEEE Power Electron. Mag. 3 (4) (2016) 28–41.
[63] H. Chung, H. Wang, F. Blaabjerg, M. Pecht, Reliability of power electronic converter systems, the Institution of Engineering and Technology (IET), (2015). ISBN 978-1-84919-901-8.

46

Thermal Modeling and Analysis of Power Electronic Components and Systems

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46.1 Introduction

In the field of power electronics, most of the challenges arise from the thermal management and our ability to predict the behavior of circuits under varied and extreme temperature conditions. It is particularly important in power electronics to understand the effects of temperature as this fundamentally affects so many aspects of the design from component values to tolerances, reliability, performance, and robustness. This chapter will therefore focus on understanding how to model and analyze thermal models relating to power electronic components and systems.

Heat is transported by three main mechanisms, conduction, convection, and radiation [1], and all three mechanisms can be important in power electronics, although the first two are generally the most significant. Heat transport occurs in three dimensions, which can make detailed analysis difficult; therefore one objective in modeling thermal behavior in power electronic systems is to reduce the problem to a simpler level and make it easier for the designer to get approximate but sufficiently accurate answers to design questions. A particular issue for the power electronics designer is that not only is the thermal behavior a requirement to accurately model the system but also is the interdependence with the device behavior. Power devices contribute heat due to losses and switching behavior, and this also contributes to self-heating effects that fundamentally affect their behavior. In some devices, this can become a serious problem. In power electronic circuits, there are also significant effects due to the variability of passive components such as resistance, capacitance, and magnetic components due to temperature, and these must all be taken into account when understanding the overall circuit behavior in this context. Finally, the environment temperature will also have a major impact on the performance of the power electronic circuit, and an effective and efficient approach is required to modeling such thermal effects.

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46.2 Background

Modeling and simulation of thermal effects has been at the heart of power electronics for many years, with engineers attempting to understand fundamental device behavior needing to understand specific thermal behavior to provide model parameters that would accurately reflect the true model behavior [2,3]. Using simple thermal resistance and capacitance models (discussed in more detail later in this chapter) either integrated in the device models [4] or extending the SPICE simulator to include thermal effects directly in the models [5], the use of equivalent "lumped element" models has been used for more than 25 years to improve our understanding of temperature and its effect on semiconductor device operation. This has been a particular issue for the bipolar device community due to the "thermal runaway" characteristics of these devices; however, the use of similar techniques by the power electronics community has become common [6]. This is still an ongoing research issue primarily due to the difficulty of accurately obtaining thermally dependent parameters for the device and package thermal circuit and also making empirical measurements that can confirm the validity of the approach. In this chapter, we will look at some techniques that can be applied to modeling thermal behavior and some approaches to implement some form of modeling to understand at least the basic thermal behavior of power electronic devices and systems.

46.3 Semiconductor Device Modelling

Simulation Program with Integrated Circuit Emphasis (SPICE) building block models exist for diodes and MOSFETs in most circuit simulators already, but they were generally designed for low-voltage and small current integrated circuit applications as the name of the program suggests. They do not (usually) have bulk effects or dynamic thermal behavior, which is essential for power electronics. Like any semiconductor device power diode, MOSFETS and IGBTs are highly nonlinear and depend fundamentally on temperature. If we consider the humble diode equation (46.1),

$$i_d = I_{SAT}\left(e^{\frac{V_d}{nV_T}} - 1\right) \tag{46.1}$$

Eq. (46.1) relates the diode current in a nonlinear fashion to the diode voltage where I_{SAT} is the saturation current, V_d is the junction voltage, $V_T = kT/q$ is the thermal voltage, and n is the emission coefficient. It is obvious that the thermal voltage depends directly on the temperature. This type of approach has been used in SPICE (and other circuit simulators for many years), where the simulator temperature is defined as a global variable and used in semiconductor device models, with the assumption being that the circuit will be in a thermal steady state and this can be defined precisely by the designer. In some simulators, such as SABER, the temperature can be defined hierarchically so that a circuit or even device can have a unique temperature, but this is still effectively static. A breakthrough was to make the temperature of the device a dynamic variable that could be modeled using a thermal circuit at the same time as the electric circuit, and by using electric analogies, the integrated device behavior could be made more accurate.

Another key issue with the modeling power devices was to take a different approach to that of the low-power IC designers and to create models of power devices such as diodes, MOSFETs, and IGBTs that were more appropriate to this context. This was the "lumped-charge" approach [7], and this model handles the forward and reverse recovery characteristics much better than the basic low-voltage model. It has been implemented in Saber for more than 20 years, and the general approach has been extended to a wide variety of power semiconductor models [8] and to other simulators such as Modelica [9].

Often, power electronics designers do not understand the detail of model that is required to solve their design problem, and this relates directly to the implementation of a thermal model too. This can be encapsulated in a series of questions such as the following:

- Do you need a detailed physics model?
- Do you need cycle by cycle accuracy?
- Can you characterize the data well enough to achieve the accuracy?

These questions (and the answers to them) will often dictate the type of model to be used and the resulting complexity of system to analyze.

46.4 Magnetic Components

Magnetic components that include a nonlinear ferrite core are some of the most difficult to model in a power electronic system. The nonlinear BH curve that defines the magnetic behavior of the inductors and transformers in a power electronic system has a profound effect on the behavior of the system as a whole. It is also highly thermally dependent, and therefore, it is useful to be able to model this.

A basic BH curve is shown in Fig. 46.1, and this illustrates the effect of high magnetic field strength (causing saturation) and the remanence effect that leads to hysteresis. This is difficult enough to model without thermal effects (e.g., see the Jiles-Atherton approach [10–12]), and this has been implemented in most circuit simulators; however, the problem for power electronic circuit designers is that the BH curve can vary with temperature as shown in Fig. 46.2.

This can be managed in a simulation model by not only including a thermal pin, in a similar manner to the power semiconductor devices, but also making it self-heating to take into account eddy currents or losses that contribute to the overall thermal behavior [13].

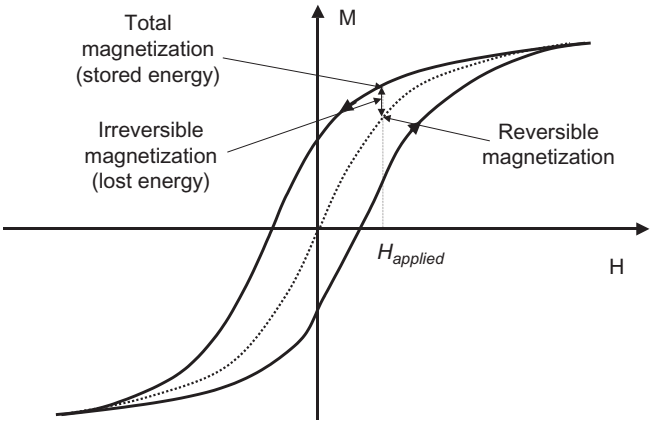


FIG. 46.1 Basic magnetic material BH curve.

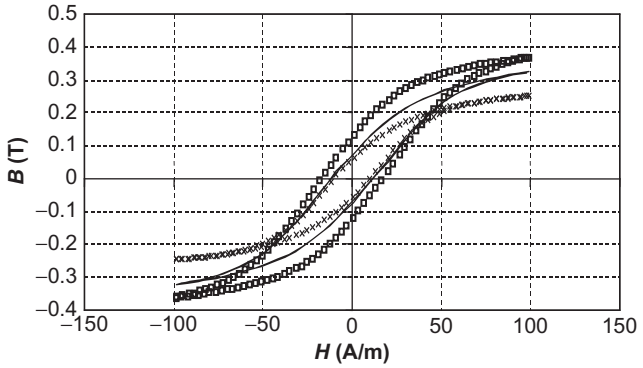


FIG. 46.2 BH curve temperature variation (□ = 27°C, − = 95°C, and × = 125°C).

In order to understand the methods of integrating thermal behavior into power electronic circuits, it is useful to first review the principles in thermal modeling.

46.5 Thermal Conduction

The conduction of heat through materials is by far the simplest transport mechanism to analyze. The transport of heat with conduction is described by the Fourier heat equation given in Eq. (46.1):

$$\frac{\delta T}{\delta t} = \frac{\sigma_\theta}{d\rho c} \times \nabla^2 T \tag{46.2}$$

where ρ is the density and c is the specific heat. The heat flux (power flow per unit area) can be found at any point using Eq. (46.3):

$$Q_\theta = -\sigma_\theta \nabla T \tag{46.3}$$

As with all partial differential equations, the solution of the Fourier equation can only be performed exactly for a few

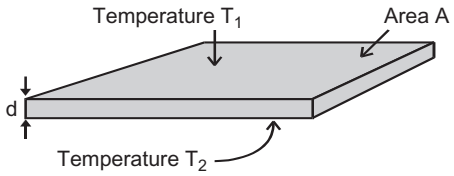


FIG. 46.3 Block of material for thermal conduction.

simple sets of boundary and initial conditions. Solutions can be found numerically or using approximate methods if we consider the conduction of heat through a square plate of area A and thickness d as shown in Fig. 46.3.

The two surfaces are at uniform temperatures T_1 and T_2. If it is the case that $d \ll A$, then we can make the assumption that the heat loss from the edges may be neglected and the resulting heat flow is in one dimension. The heat flow through the plate can therefore be calculated using Eq. (46.4):

$$P_\theta = \frac{(T_1 - T_2) \times A \times \sigma_\theta}{d} \times W \tag{46.4}$$

where σ_θ is the thermal conductivity. Notice the use of the subscript θ to emphasize that both the power and conductivity are thermal. Eq. (46.4) is often written in the form shown in Eq. (46.5):

$$P_\theta = \frac{(T_1 - T_2)}{R_\theta} \tag{46.5}$$

where R_θ is the *thermal resistance* of the plate, given by Eq. (46.6):

$$R_\theta = \frac{d}{A \times \sigma_\theta} \text{ K/W} \tag{46.6}$$

It is useful to see that the magnitude of thermal resistances for commonly used materials (in this case assuming a plate of area 10^{-4} m^2 (1 cm × 1 cm) and thickness 1 mm) is shown in Table 46.1.

TABLE 46.1 Thermal conductivity and resistance of a range of materials

Material	Thermal conductivity (W/K/m)	Thermal resistance (K/W)
Aluminum	217	0.046
Copper	394	0.025
Gold	291	0.034
Lead	34.3	0.29
Tin	63	0.16
PCB (FR4)	0.3	33
Alumina	27.6	0.36
Diamond	630	0.016
Silicon	150	0.067
GaN	130	0.077
Silicon carbide	500	0.02

Table 46.1 is interesting in that as we might expect, copper is an extremely good conductor; however, it is particularly interesting to look at three common materials for power electronic devices, silicon, gallium nitride, and silicon carbide. They all have excellent thermal properties; however, silicon carbide is particularly good making it advantageous for power electronic applications where thermal management is crucial.

The equation for conduction of heat has the same form as Ohm's law, making it easy to draw a direct analogy between the thermal and electric resistance equations:

$$P_\theta = \frac{\Delta T}{R_\theta} \Leftrightarrow I = \frac{\Delta V}{R} \tag{46.7}$$

The analogy is drawn that P is equivalent to I, T is equivalent to V, and R_θ is equivalent to R. T in the thermal model is defined as an *across* variable, that is, only differences between points are specified. This means that as for voltage, there must be a reference node. This is usually the ambient temperature, T_a. P is a through variable in the same that in an electric circuit, current must flow around a closed loop.

46.6 Convection

Convection is the process by which heat is transferred from a solid surface to a nonsolid, such as air or water. The convection process involves the motion of the fluid relative to the solid surface and the processes by which heat is transferred across the interface.

There are two main forms of convection, *natural* or *free* convection, where the motion of the fluid is produced by the change in density with temperature, and *forced* convection, where the motion is generated by an external mechanism, a fan or a pump.

Convection is most effective where the hot surface is vertical. The air is heated by the plate and rises by the "chimney effect." Forced airflow parallel to the plate will increase heat transfer. Heat transfer will depend on surface area, height, and temperature difference (Fig. 46.4). The process of convection is complex and not readily amenable to analysis; therefore, empirical methods have been developed, allowing models to be created based on these measurements.

46.7 Radiation

The final concept of heat transfer is radiation. In this context, radiation refers to the transfer of heat by electromagnetic radiation. The basic equation for heat transfer by radiation is the Stefan-Boltzmann law that is given in Eq. (46.8):

$$P_{rad} = 5.7 \times 10^{-7}\left(T^4 - T_a^4\right) \times E \times A \tag{46.8}$$

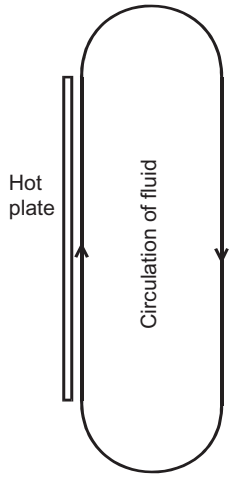


FIG. 46.4 Convection concept of fluid circulation.

where T is the absolute temperature of the radiating surface (K), T_a is the ambient temperature of the surrounding objects (K), A is the area (m^2), and E is a constant known as the emissivity. The emissivity may vary from as low as 0.05 for polished aluminum to 0.9 for black oxidized aluminum.

In order to put the power loss by radiation into context, consider a 1 cm^2 black anodized aluminum plate. The plate is at a temperature of 373 K, and the ambient temperature is at 323 K.

Taking into account the heat loss from both sides of the plate, the power loss is given by Eq. (46.9):

$$P = 5.7 \times 10^{-7} \times 0.8 \times 10^{-4} \times \left(373^4 - 323^4\right) \times 2 = 0.87 \text{ W} \tag{46.9}$$

With a heat sink using natural convection, radiation will play a role in removing heat. The difference between a shiny aluminum heat sink and the same sink anodized black is of order 5%–25%, and the advantage rises with temperature.

Now, we have covered the basics of thermal behavior; we can investigate how to implement useful models for inclusion in power electronic circuits.

46.8 Steady State Thermal Circuit Modeling

For the thermal circuit model to be of use, it must be possible to define the temperature at well-defined points that are defined as the nodes of the thermal circuit. It must also be possible to define the heat flux and thermal resistance between these points, which implies that we therefore have a *lumped* model. At this stage, we are considering the steady state only, where the temperatures have stabilized into an equilibrium condition.

It is essentially the same as describing an electric circuit in terms of nodes connected by electric components, which is valid as long as it is not necessary to consider distributed effects

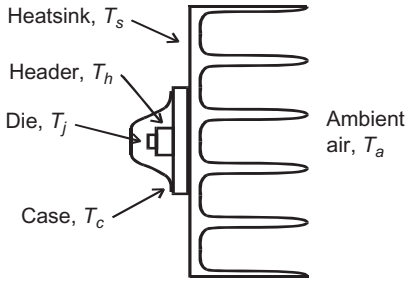


FIG. 46.5 Transistor bolted to a heat sink.

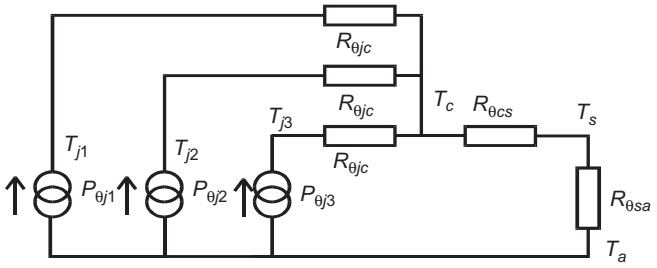


FIG. 46.7 Several transistors mounted on the same heat sink.

(such as a transmission line). The lumped components in the thermal circuit are generally less well defined than their electric counterparts, due to the uncertainty in characterization of the thermal parameters and approximations made to obtain the parameters.

If we consider the example of a transistor that is bolted to a heat sink, as shown in Fig. 46.5, we can see that there are five temperatures to consider in this model, starting from the junction temperature of the device (T_j), the header temperature (T_h), the case temperature (T_c), the heat sink (T_s), and finally the ambient temperature (T_a).

The heat flow into the thermal circuit from the device is the power dissipation (in watts) from the power device, which is analogous to current in the electric domain. At this point, the obvious question is how do we model this thermal circuit in such a way that we can calculate all the intermediate temperatures based on a power dissipation value from the power transistor? We can represent each of the individual thermal elements as a thermal resistance connected in series with a thermal heat source as shown in Fig. 46.6.

In this example, the thermal circuit has been represented by four resistors with five nodes. In practice, R_{qjh} and R_{qhc} would not readily be measured separately and so would be grouped together as R_{qjc}, a parameter measured by the manufacturer. The heat-sink supplier would specify R_{qsa}, and the contact resistance between case and heat sink would depend on mounting method surface conditions. The junction temperature can be estimated using Eq. (46.10):

$$T_j = \left(R_{\theta jh} + R_{\theta jc} + R_{\theta cs} + R_{\theta sa}\right) \times P_{\theta j} + T_a \tag{46.10}$$

and the heat-sink temperature can also be estimated from Equation (46.11):

$$T_s = R_{\theta sa} \times P_{\theta j} + T_a \tag{46.11}$$

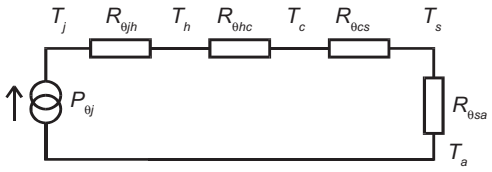


FIG. 46.6 Equivalent thermal circuit of power device and heat sink.

This lumped approach starts to become very effective when the situation becomes more complex as it can be easily modeled using SPICE or other circuit simulators, such as the case when there are several devices mounted on the same heat sink as shown in Fig. 46.7.

This circuit can quickly be solved and the resulting heatsink temperature estimated.

46.9 Dynamic Thermal Circuit Modeling

So far, only steady-state thermal circuits have been considered. There are however many situations where it is required to model the transient behavior, such as when the dynamic electric behavior changes (say under peak inrush current conditions or a failure current). When heat is applied to an object, the temperature will increase at a rate determined by the heat input and the *thermal capacity* of the object. Although the scenario has moved from steady state to dynamic, the assumption is still being made that a single temperature may be assigned to the object, that is, a lumped model rather than a distributed one. This will not necessarily be the case, but it is a necessary assumption for the lumped component model. Generally, some kind of average temperature will be used. The thermal capacity of a lumped component of the thermal circuit is given by Eq. (46.12):

$$C_\theta = m \times c_s \tag{46.12}$$

where m is the mass of the component and c_s the specific heat of the material. In terms of the circuit model, the thermal capacity is analogous to an electric capacitor. A transistor on a heat sink may therefore be represented by Fig. 46.8.

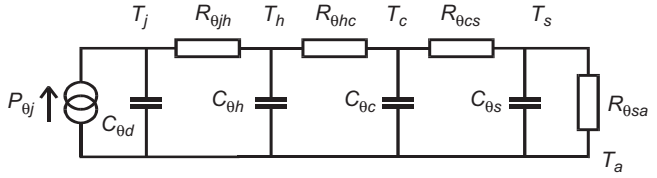


FIG. 46.8 Adding thermal capacitance to the thermal model.

This model is useful, but there are still issues to resolve. If we consider the heat sink, a thermal capacity $R_{\theta s}$ has been ascribed to it, and this is relatively well defined. In the model, the temperature drop across the heat sink itself has been neglected. The thermal resistances either side of the capacitor are interface resistances, with no significant thermal capacity. Similarly, the case presents a relatively large thermal capacity but little thermal resistance. The header and the die however are different. Here, they have both been considered as two lumped components. This is not a very good assumption as in reality the thermal resistance and thermal capacity in both header and die are distributed.

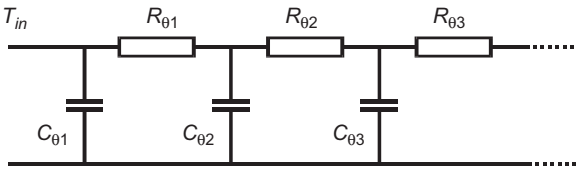


FIG. 46.9 Thermal ladder network.

46.10 Approximating Distributed Thermal Behaviour Using Ladder Networks

One solution to the problem of approximating a distributed thermal network is to use a thermal ladder network. The thermal resistance is divided into n sections of R_θ/n and the capacitance into n capacitances of value C_θ/n. This is exactly the same problem that arises in distributed electric networks (such as transmission lines), and the same approach may be taken as shown in Fig. 46.9. However, it should be noted that there is no obvious equivalent to an inductance in the thermal domain.

46.11 Transient Thermal Impedance

The ladder network approach is useful but is a hard work to analyze. A simpler approach is needed and that approach is the transient thermal impedance. When considering active devices mounted on a heat sink, the external part can be adequately described by the simple thermal resistance—thermal capacity concept. The problem area is the internal behavior of the device. The central idea is to replace the internal thermal resistance by a thermal impedance that depends on the temporal variation of the power dissipated. The objective is to accurately estimate the maximum junction temperature.

A typical data sheet graph (for the International Rectifier IRF 450 n-type power MOSFET in a modified TO-3 package, a 500 V 12 A device) of thermal impedance is shown in Fig. 46.10, with the thermal impedance plotted against the pulse duration on the x-axis and the family of curves showing how the duty ratio affects the effective thermal impedance, normalized to the thermal resistance. For this device, the thermal resistance is found on the data sheet as the parameter R_{thJC} and is 0.83°C/W, and the junction to ambient thermal resistance is 30°C/W. (For comparison, a TO-240 package—device is denoted by IRFM450—has a junction to ambient thermal resistance of 48°C/W.)

The starting point is the response of the junction temperature to a unit step of input power, when the case temperature is constant. The temperature after a time t is the equivalent of the maximum temperature reached by the junction for a single

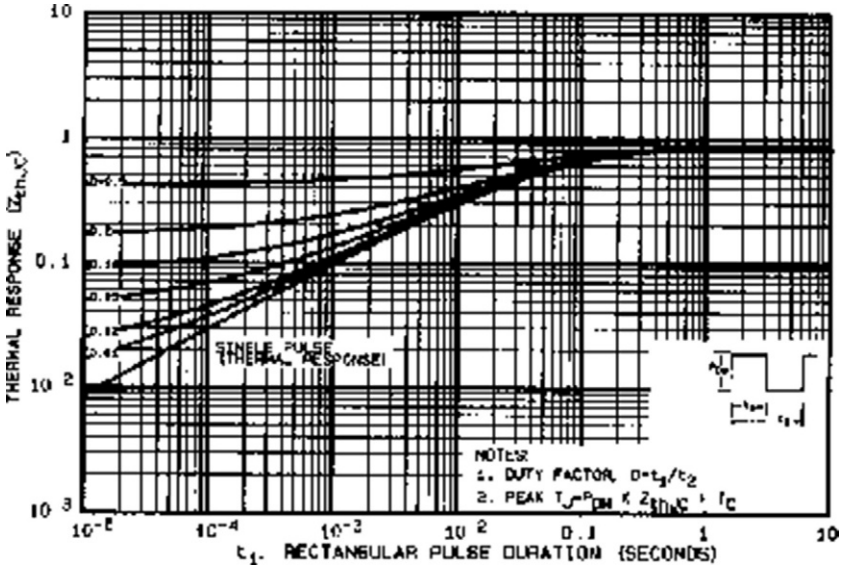


FIG. 46.10 Thermal impedance for International Rectifier IRF450.

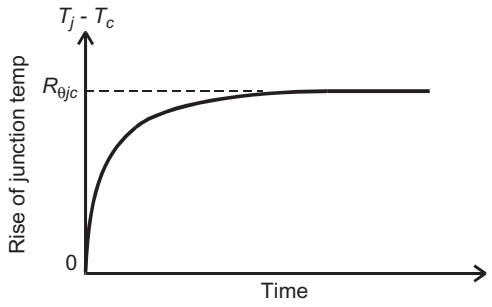


FIG. 46.11 Response of junction temperature over time.

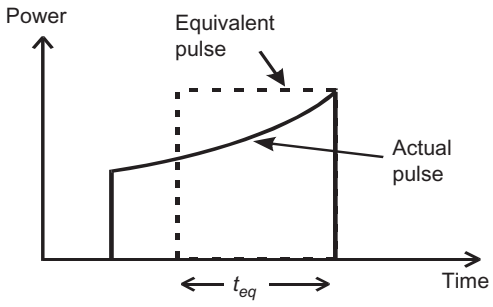


FIG. 46.13 Equivalent pulse based on actual pulse shape.

pulse of duration t. The steady-state response is a rise of temperature equal to the thermal resistance R_{qjc}.

The dynamic response of the junction temperature can be seen in Fig. 46.11, where the temperature will rise smoothly to the steady-state value.

The rise of junction temperature above the case temperature for a pulse of length t is defined as the thermal impedance for a pulse of length t. This is for a pulse of unit height. If the pulse has an amplitude P_m and duration t, the maximum junction temperature is given by Eq. (46.13):

$$T_{jmax} = T_a + Z_{\theta jc}(t) \times P_m \tag{46.13}$$

If the pulses are repetitive with a duration t and duty ratio D (Period t/D), the maximum temperature will rise above the value for a single pulse of duration t as shown in Fig. 46.12.

With multiple pulses, the temperature oscillates, the magnitude of the oscillation decreasing with increasing frequency. In the limit, the ripple will approach zero, with a temperature rise corresponding to the mean power ($P_m \times D$) multiplied by the thermal resistance. Measured values for thermal impedance can be seen on manufacturer's data sheets. The graphs show the thermal impedance normalized to the thermal resistance, as a function of pulse width and duty ratio.

46.12 Procedure to Calculate the Transient Thermal Impedance

The procedure to use thermal impedance to calculate the temperature difference between junction and case starts by calculating the approximate power pulse by an equivalent square pulse of equal area and same height based on the actual pulse as shown in Fig. 46.13. From this figure, it is possible to deduce equivalent pulse width, t_{eq}. The way to do this is to estimate the area under the actual curve (using a trapezoidal approach) and from the maximum value calculate the equivalent pulse width based on the rectangular area required. The duty ratio can then be calculated based on the ratio of the equivalent pulse width and the switching period.

With the equivalent pulse width and the derived duty ratio, the graph of thermal impedance can be used to look up the appropriate value.

The maximum difference (effectively the steady state) can then be calculated by multiplying the peak pulse power by the value of thermal impedance obtained from the data sheet. In practice, the pulsing thermal behavior we see in Fig. 46.12 will be filtered out by the time the case is taken into account, and the calculation of case temperature may be made using the average power and the external thermal resistances.

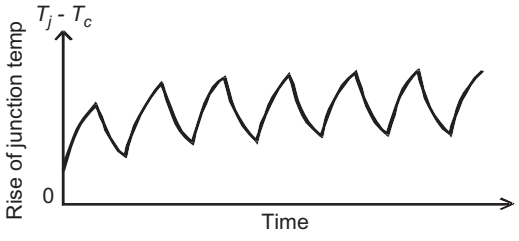


FIG. 46.12 Response of junction temperature to repeated pulses.

46.13 Finite Element Numerical Methods

The solution of the Fourier heat equation in anything but the simplest cases requires the use of numerical methods such as the finite element method. For the steady state, the Fourier equation reduces to the Laplace equation in Eq. (46.14):

$$\nabla^2 T = 0 \tag{46.14}$$

and the heat flux (power per unit area) at any point is given by Eq. (46.15):

$$Q_\theta = \sigma \nabla(T) \tag{46.15}$$

The Laplace equation occurs in many physical systems, and the solution of it is a standard problem; however, due to the complexity of most real-world systems, finite element techniques are the preferred technique to obtain a numerical solution. Solutions for the temperature distribution in physical geometries can be obtained using commercial software packages designed to implement the finite element method. In most cases, this will give the equilibrium or steady-state solution rather than the transient behavior. In order to calculate, the

transient thermal distribution requires the use of repeated finite element simulations for different initial conditions and applied heat flow values (as in the pulsed example shown in Fig. 46.13). This can take a high level of computation to complete and for complex geometries can take a long time to complete.

46.14 Dynamic Thermal Equivalent Circuit Models

When the calculations get more complex than a simple junction to case and junction to ambient calculation, then the choice for the power electronics design engineer is to either create a complex geometric model for the device, case, heat sink, and environment and then conduct extensive, repeated finite element analyses or more commonly use equivalent circuit models instead.

One obvious circuit that is often used to provide an increased level of detail, which effectively approximates the finite element model in one dimension, is the ladder circuit. For example, if we take the IRF450 device we have looked at previously, we can see that the junction to case thermal resistance R_{thJC} is 0.83°C/W; therefore, if we create a 10-section RC ladder network, then each individual thermal resistance will be 0.083 C/W (one-tenth of the overall thermal resistance). In the steady state, this will be identical to the lumped model we looked at previously in this chapter (Fig. 46.14). It is possible to calculate an appropriate value for the ladder capacitances; however, in most cases, it is just as quick (and certainly easier) to use a simulation to experiment with the capacitance values to obtain the best matching of time dependence with the data for the device.

If a heat flow (current in an electric analogous circuit) is applied, then the voltage will represent the thermal impedance over time, and this can be matched to the data sheet transient thermal impedance. For example, using the Saber simulator, we can define a thermal circuit using dedicated thermal resistance and capacitance models (although we could equally well use SPICE models for electric analogues), as shown in Fig. 46.15.

Varying the capacitance value allows the response of the transient thermal impedance to be obtained from the temperature across the whole ladder network. In this case, we can vary the capacitance on each leg from 200 to 2000 μF, with the resulting responses as shown in Fig. 46.16.

The same circuit can be used to test the behavior of the thermal circuit to a pulsed heat source, much as would be the case when a power device is switched on and off, and we can simulate this using the same test circuit, but with a pulse heat source (Fig. 46.17). Using a period of 1 ms and a duty ratio of 0.2, we can see the temperature response as follows (when the capacitance is defined as 400 μF).

When the heat source pulse period is reduced to 100 μs (i.e., 10 kHz), the ripple on the temperature reduces significantly (Fig. 46.18).

One of the limitations with the ladder network is that it will tend to underestimate the thermal impedance for higher duty ratios, and while it is certainly very useful, it must be used with caution. It is possible to increase the accuracy by increasing the number of thermal RC stages; however, obviously, there will be a price to pay in terms of simulation speed as a result.

It is also very useful to note that the thermal models can be linked directly to the electric simulations with the power electronics, either using electric analogy models (i.e., electric resistance to represent thermal resistance) or more commonly in modern multiple-domain simulators directly as thermal models. It is, however, true to say that in most cases, the time constants of the thermal circuits are much longer than the switching periods of the power electronics and the user should

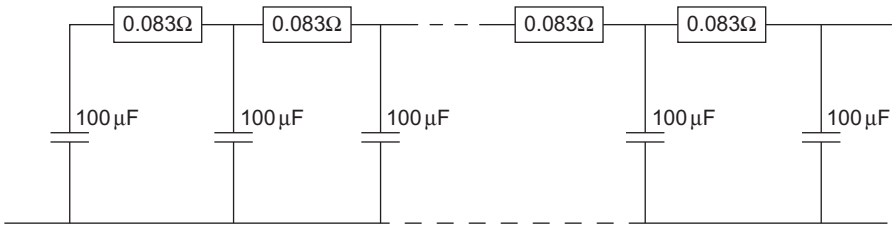


FIG. 46.14 Dynamic thermal ladder model example.

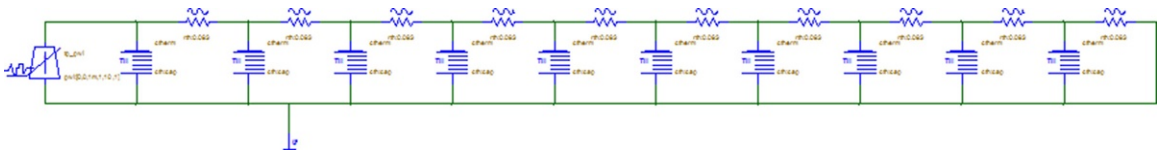


FIG. 46.15 Thermal ladder simulation test circuit.

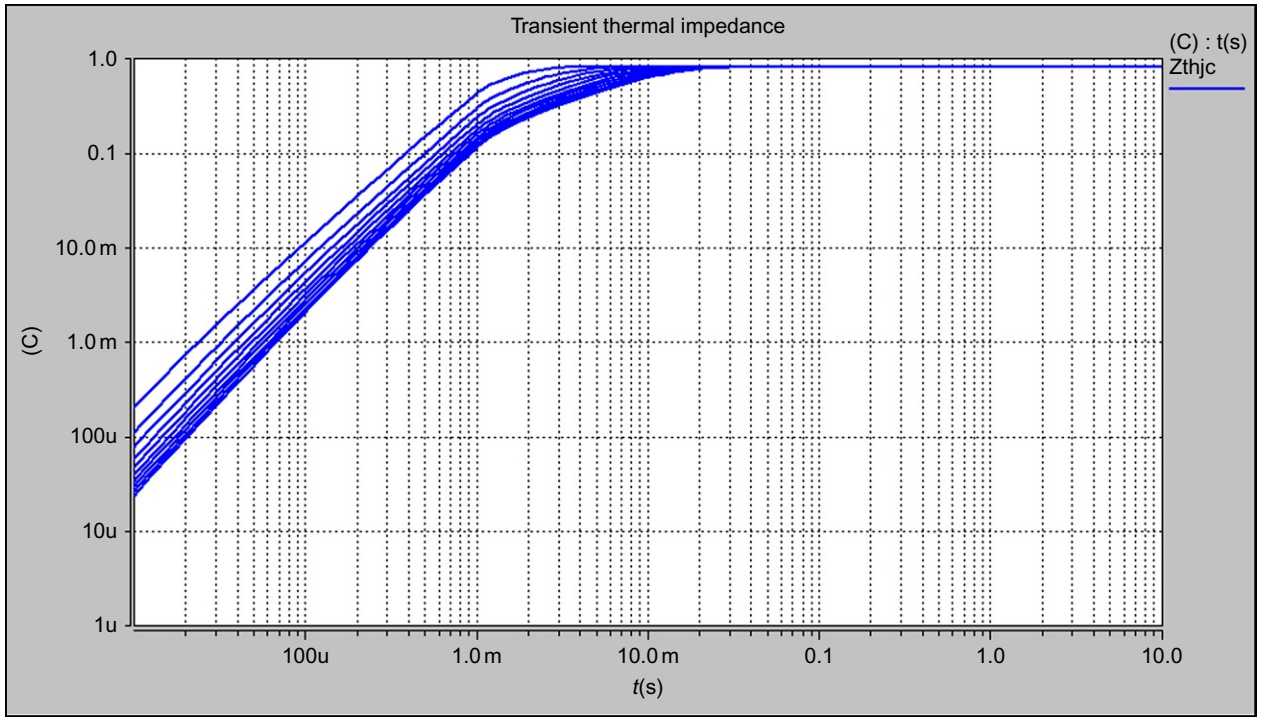


FIG. 46.16 Transient thermal impedance variation due to ladder capacitance.

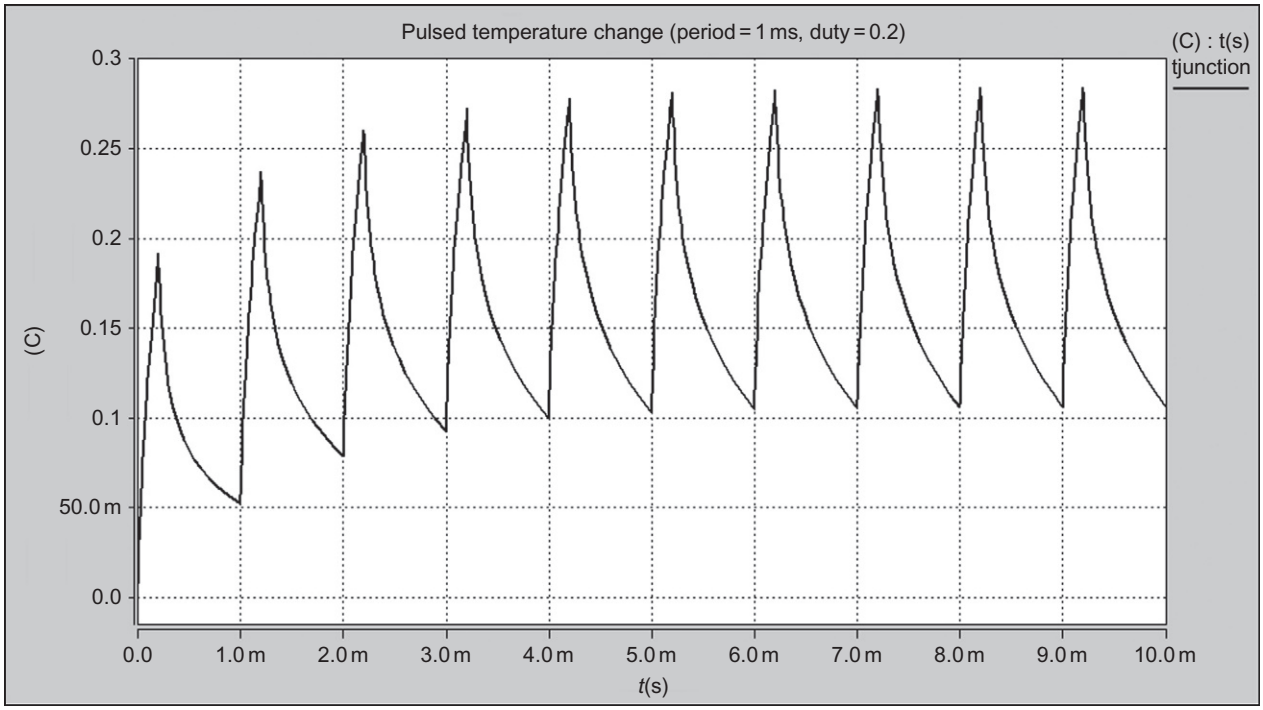


FIG. 46.17 Pulsed heat source temperature change at 1 kHz and duty ratio = 0.2.

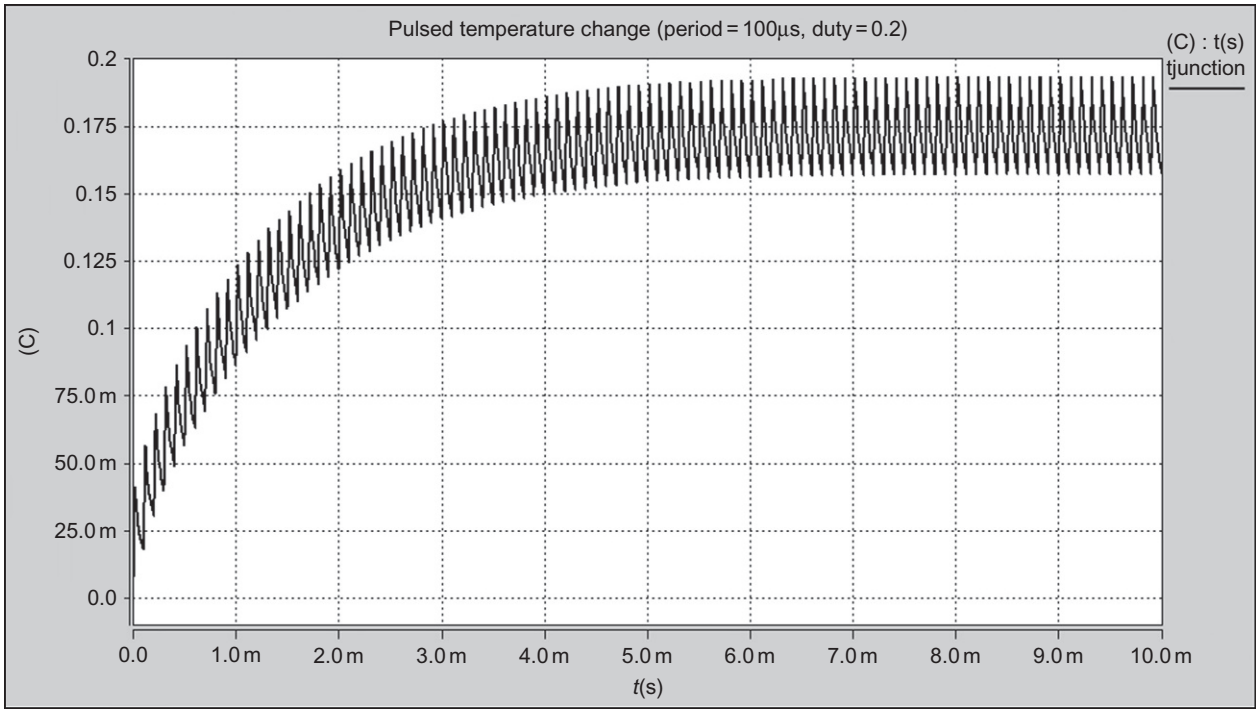


FIG. 46.18 Pulsed heat source temperature change at 10 kHz duty ratio = 0.2.

therefore be prepared for running long simulations to achieve the steady-state temperature changes. Nevertheless, it can be extremely illuminating and helpful in understanding the true thermal state of the power electronics.

46.15 Summary

Thermal properties of devices, packages, and heat sinks can be modeled in a relatively simple and efficient manner using a number of simple lumped-model techniques. While this gives a good starting point for estimating the thermal impact on circuit performance, it is clearly a complex and interlinked area that requires detailed analysis to gain highly accurate solutions. However, the use of such models can help the designer gain an insight as to the effect of temperature on device and circuit behavior and as a result can profoundly improve the ultimate design. If the designer takes a "worst-case-scenario" approach to modeling thermal behavior, then they greatly increase their chances of obtaining a robust and efficient design that can cope with extremes of temperature in the environment or due to the device behavior.

References

[1] M.W. Zemansky, Heat and Thermodynamics, fifth ed., McGraw-Hill Book Company Inc., New York, 1968.

[2] R.M. Fox, S.G. Lee, Scalable small-signal model for BJT self-heating. IEEE Electron. Device Lett. 12 (12) (1991) 649–651, http://dx.doi.org/10.1109/55.116943.

[3] K. Fukahori, P.R. Gray, Computer simulation of integrated circuits in the presence of electrothermal interaction, IEEE J. Solid-State Circuits SC-11 (1976) 834–846.

[4] R.S. Vogelsong, C. Brzezinski, Extending spice for electro-thermal simulation, in: Proceedings of IEEE Custom Integrated Circuits Conference, May 1989, pp. 21.4.1–21.4.40.

[5] P.C. Munro, F.Q. Ye, Simulating the current mirror with a self-heating BJT model. IEEE J. Solid-State Circuits 26 (9) (1991) 1321–1324, http://dx.doi.org/10.1109/4.84951.

[6] A.R. Hefner, D.L. Blackburn, Simulating the dynamic electrothermal behavior of power electronic circuits and systems, IEEE Trans. Power Electron. 8 (4) (1993) 376–385.

[7] Cliff L. Ma, Peter O. Lauritzen, Jakob Sigg, Modeling of power diodes with the lumped-charge modeling technique, IEEE Trans. Power Electron. 12 (3) (1997) 398–405.

[8] I. Budihardjo, P.O. Lauritzen, The lumped-charge power MOSFET model, including parameter extraction, IEEE Trans. Power Electron. 10 (5) (1995) 379–387.

[9] D. Patrick, T. Schmitt, M. Andres, Behavioral modeling of power semiconductors in modelica, in: Proceedings of the 10th International Modelica Conference, March 10–12, 2014, Lund; Sweden. No. 096. Linköping University Electronic Press.

[10] D.C. Jiles, D.L. Atherton, Theory of ferromagnetic hysteresis (invited), J. Appl. Phys. 55 (6) (1984) 2115–2120.

[11] D.C. Jiles, D.L. Atherton, Theory of ferromagnetic hysteresis, J. Magn. Magn. Mater. 61 (1986) 48–60.

[12] D.C. Jiles, D.L. Atherton, Ferromagnetic hysteresis, IEEE Trans. Magn. 19 (5) (1983) 2183–2185.

[13] P.R. Wilson, J.N. Ross, A.D. Brown, Simulation of magnetic component models in electric circuits including dynamic thermal effects. IEEE Trans. Power Electron. 17 (1) (2002) 55–65, http://dx.doi.org/10.1109/63.988670.

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